

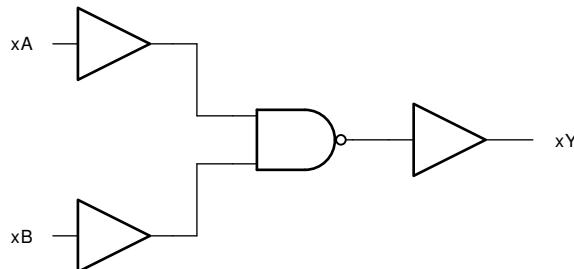
# SN74LV4T00 クワッド 2 入力正 NAND ゲート 統合変換機能付き

## 1 特長

- 幅広い動作範囲: 1.8V~5.5V
- 単一電源電圧トランスレータ (「LVxT 拡張入力電圧」を参照):
  - 昇圧変換:
    - 1.2V から 1.8V
    - 1.5V から 2.5V
    - 1.8V から 3.3V
    - 3.3V から 5.0V
  - 降圧変換:
    - 5.0V、3.3V、2.5V から 1.8V
    - 5.0V、3.3V から 2.5V
    - 5.0V から 3.3V
- 5.5V 許容入力ピン
- 標準ピン配置をサポート
- 5V または 3.3V の  $V_{CC}$  で最大 150Mbps
- JESD 17 準拠で 250mA 超のラッチアップ性能

## 2 アプリケーション

- デジタル信号のイネーブルまたはディスエーブル
- インジケータ LED の制御
- 通信モジュールとシステム・コントローラの間の変換



概略論理図 (正論理)

## 3 概要

SN74LV4T00 には、シュミット・トリガ入力採用の 4 つの独立した 2 入力 NAND ゲートが内蔵されています。各ゲートはブール関数  $Y = \overline{A \bullet B}$  を正論理で実行します。出力レベルは電源電圧 ( $V_{CC}$ ) を基準としており、1.8V、2.5V、3.3V、5V の CMOS レベルをサポートしています。

入力は低スレッショルド回路を使用して設計され、低電圧 CMOS 入力の昇圧変換 (例: 1.2V 入力から 1.8V 出力、1.8V 入力から 3.3V 出力) をサポートします。また、5V 許容の入力ピンにより、降圧変換 (例: 3.3V 入力から 2.5V 出力) が可能です。

### パッケージ情報<sup>(1)</sup>

部品番号	パッケージ	本体サイズ (公称)
SN74LV4T00	BQA (WQFN, 14)	3.00mm × 2.50mm
	PW (TSSOP, 14)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、必ず最新版の英語版をご参照ください。

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## 4 Revision History

DATE	REVISION	NOTES
April 2023	*	Initial Release

## 5 Pin Configuration and Functions

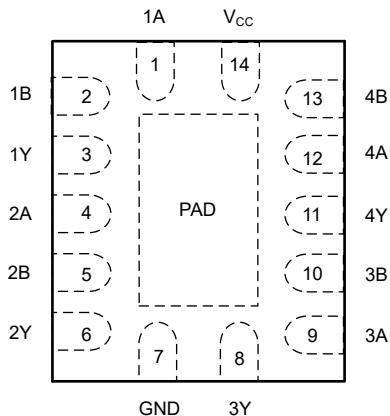


図 5-1. BQA Package, 14-Pin WQFN (Top View)

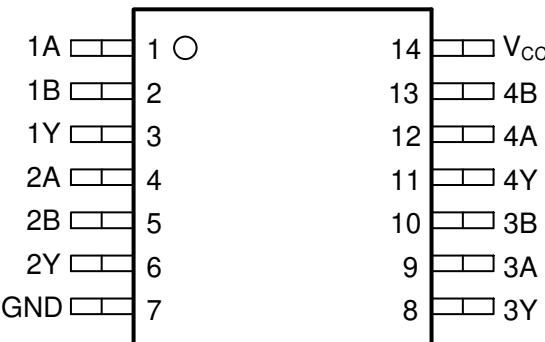


図 5-2. PW Package, 14-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
1Y	3	O	Channel 1, Output Y
2A	4	I	Channel 2, Input A
2B	5	I	Channel 2, Input B
2Y	6	O	Channel 2, Output Y
GND	7	—	Ground
3Y	8	O	Channel 3, Output Y
3A	9	I	Channel 3, Input A
3B	10	I	Channel 3, Input B
4Y	11	O	Channel 4, Output Y
4A	12	I	Channel 4, Input A
4B	13	I	Channel 4, Input B
V <sub>CC</sub>	14	—	Positive Supply
Thermal Pad <sup>(2)</sup>		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

(2) BQA package only

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < -0.5 V		-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25	mA
	Continuous output current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.6	5.5	V
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 2 V	1.1	V	
		V <sub>CC</sub> = 2.25 V to 2.75 V	1.28		
		V <sub>CC</sub> = 3 V to 3.6 V	1.45		
		V <sub>CC</sub> = 4.5 V to 5.5 V	2		
V <sub>IL</sub>	Low-Level input voltage	V <sub>CC</sub> = 1.65 V to 2 V	0.5	V	
		V <sub>CC</sub> = 2.25 V to 2.75 V	0.65		
		V <sub>CC</sub> = 3 V to 3.6 V	0.75		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.85		
I <sub>O</sub>	Output current	V <sub>CC</sub> = 1.6 V to 2 V	±3	mA	
		V <sub>CC</sub> = 2.25 V to 2.75 V	±7		
		V <sub>CC</sub> = 3.3 V to 5.0 V	±15		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.6 V to 5.0 V	20	ns/V	
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report: [Implications of Slow or Floating CMOS Inputs](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV4T00-Q1			UNIT
		WBQA (WQFN)		PW (TSSOP)	
		14 PINS		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.3	151.0		°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	90.9	80.0		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.8	94.2		°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	9.9	28.0		°C/W
$\Upsilon_{JB}$	Junction-to-board characterization parameter	56.7	93.6		°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	33.4	N/A		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	1.65 V to 2 V	1.28	1.7 <sup>(1)</sup>		1.21			
	I <sub>OH</sub> = -3 mA	2.25 V to 2.75 V	2	2.4 <sup>(1)</sup>		1.93			
	I <sub>OH</sub> = -5.5 mA	3 V to 3.6 V	2.6	3.08 <sup>(1)</sup>		2.49			
	I <sub>OH</sub> = -8 mA	4.5 V to 5.5 V	4.1	4.65 <sup>(1)</sup>		3.95			
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	1.65 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	1.65 V to 2 V	0.1 <sup>(1)</sup>	0.2		0.25			
	I <sub>OL</sub> = 3 mA	2.25 V to 2.75 V	0.1 <sup>(1)</sup>	0.15		0.2			
	I <sub>OL</sub> = 5.5 mA	3 V to 3.6 V	0.2 <sup>(1)</sup>	0.2		0.25			
	I <sub>OL</sub> = 8 mA	4.5 V to 5.5 V	0.3 <sup>(1)</sup>	0.3		0.35			
I <sub>I</sub>	V <sub>I</sub> = 0 V or V <sub>CC</sub>	0 V to 5.5 V	±0.1			±1			µA
I <sub>CC</sub>	V <sub>I</sub> = 0 V or V <sub>CC</sub> , I <sub>O</sub> = 0; open on loading	1.65 V to 5.5 V	2			20			µA
ΔI <sub>CC</sub>	One input at 0.3 V or 3.4 V, other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	5.5 V	1.35			1.5			mA
	One input at 0.3 V or 1.1 V, other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	1.8 V	10			20			µA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4			10			pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	3						pF
C <sub>PD</sub> <sup>(2) (3)</sup>	No load, F = 1 MHz	5 V	14						pF

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)

(2) C<sub>PD</sub> is used to determine the dynamic power consumption, per channel.

(3) P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> × F<sub>I</sub> × (C<sub>PD</sub> + C<sub>L</sub>) where F<sub>I</sub> = input frequency, C<sub>L</sub> = output load capacitance, V<sub>CC</sub> = supply voltage.

## 6.6 Switching Characteristics 1.8-V $V_{CC}$

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 15 pF	11.3	21	1	24	24	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	11.3	21	1	24	24	nS	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 50 pF	14.2	23.5	1	27	27	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	14.2	23.5	1	27	27	nS	

## 6.7 Switching Characteristics 2.5-V $V_{CC}$

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 15 pF	7.1	11.3	1	13.4	13.4	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	7.1	11.3	1	13.4	13.4	nS	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 50 pF	9.2	14.1	1	16.9	16.9	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	9.2	14.1	1	16.9	16.9	nS	

## 6.8 Switching Characteristics 3.3-V $V_{CC}$

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5.5	8.3	1	9.9	9.9	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5.5	8.3	1	9.9	9.9	nS	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 50 pF	7.60	11.4	1	13	13	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	7.60	11.4	1	13	13	nS	

## 6.9 Switching Characteristics 5.0-V $V_{CC}$

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 15 pF	4.3	6	1	7.3	7.3	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	4.3	6	1	7.3	7.3	nS	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.6	8	1	9.7	9.7	nS	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.6	8	1	9.7	9.7	nS	

## 6.10 Noise Characteristics

V<sub>CC</sub> = 5 V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.9	0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>	-0.8	-0.3		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>	4.4	5		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2.1			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage		0.5		V

## 7 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

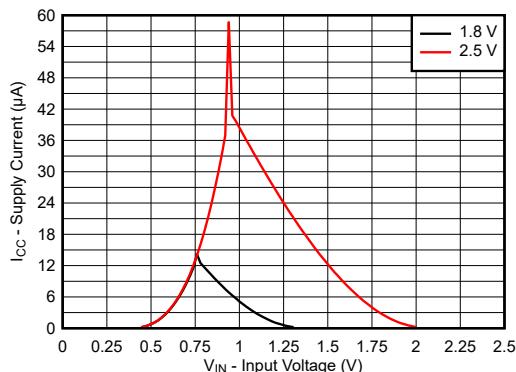


图 7-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

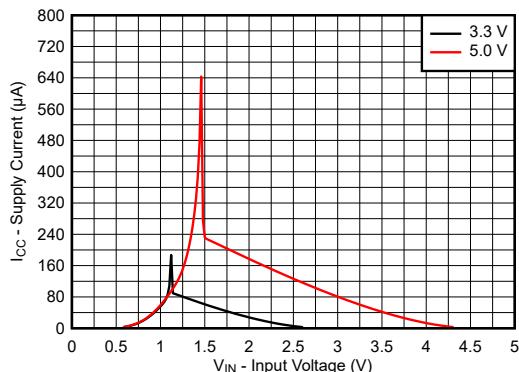


图 7-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

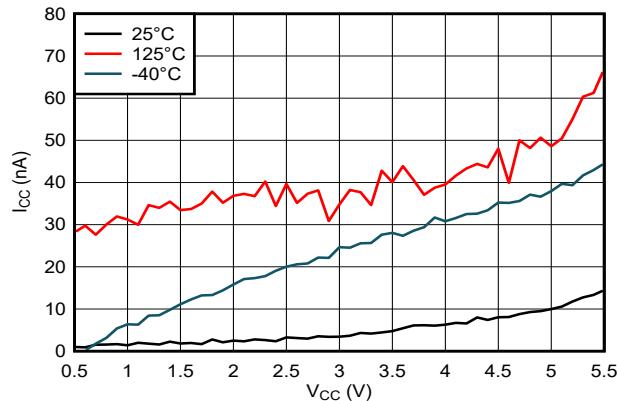


图 7-3. Supply Current Across Supply Voltage

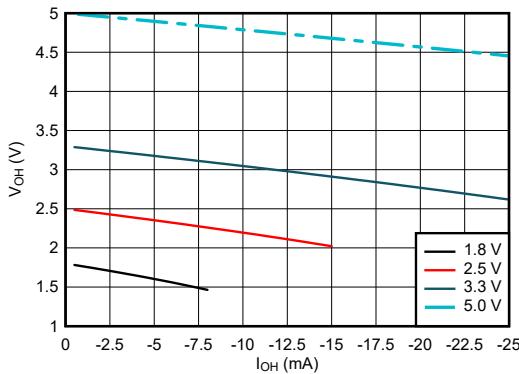


图 7-4. Output Voltage vs Current in HIGH State

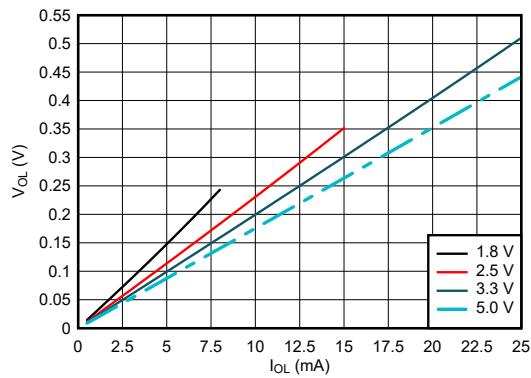


图 7-5. Output Voltage vs Current in LOW State

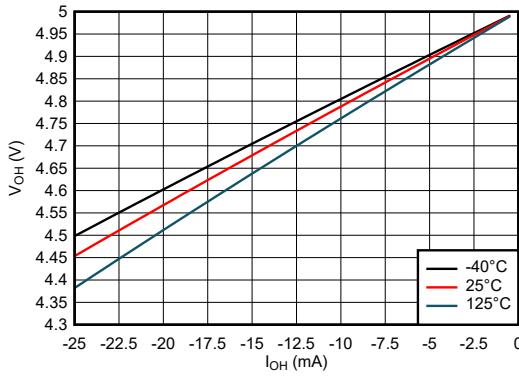


图 7-6. Output Voltage vs Current in HIGH State; 5-V Supply

## 7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

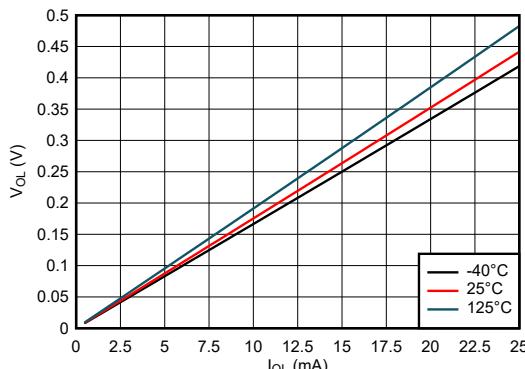


图 7-7. Output Voltage vs Current in LOW State; 5-V Supply

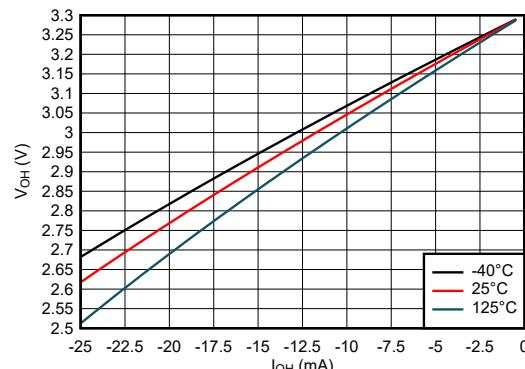


图 7-8. Output Voltage vs Current in HIGH State; 3.3-V Supply

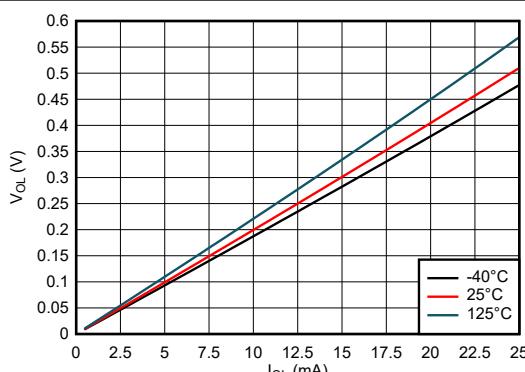


图 7-9. Output Voltage vs Current in LOW State; 3.3-V Supply

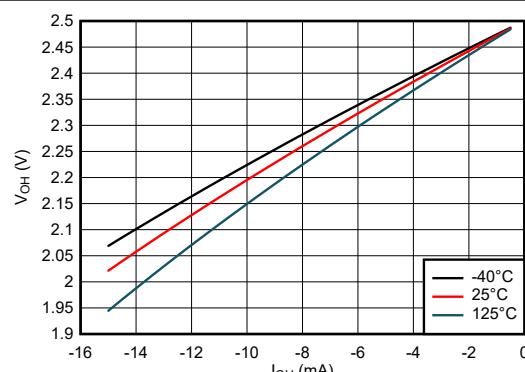


图 7-10. Output Voltage vs Current in HIGH State; 2.5-V Supply

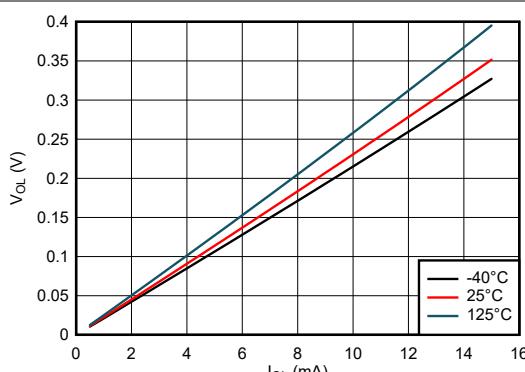


图 7-11. Output Voltage vs Current in LOW State; 2.5-V Supply

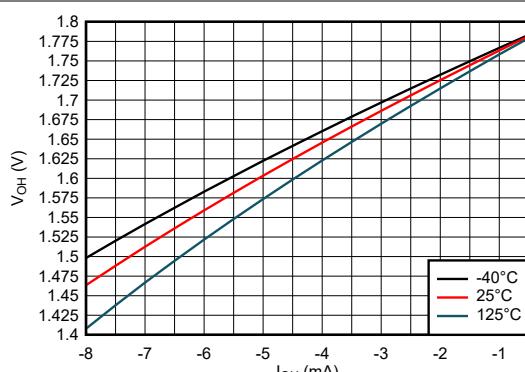


图 7-12. Output Voltage vs Current in HIGH State; 1.8-V Supply

## 7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

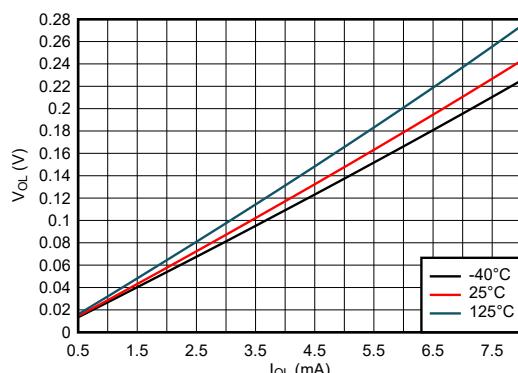


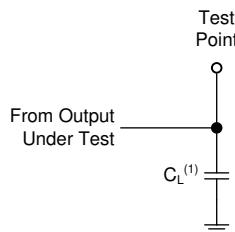
图 7-13. Output Voltage vs Current in LOW State; 1.8-V Supply

## 8 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_0 = 50 \Omega$ .

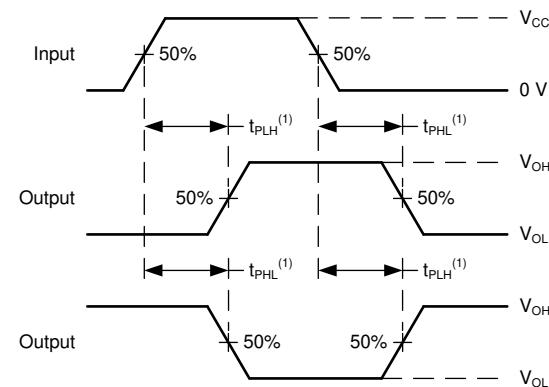
For clock inputs,  $f_{\max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



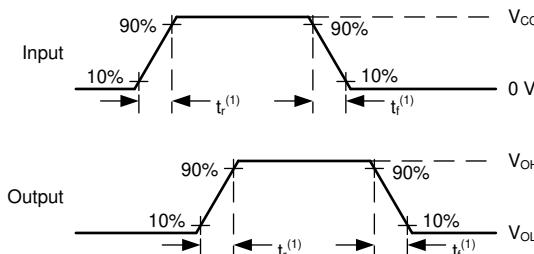
(1)  $C_L$  includes probe and test-fixture capacitance.

**图 8-1. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**图 8-2. Voltage Waveforms Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

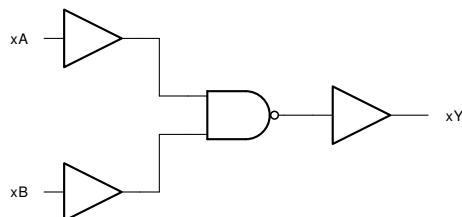
**图 8-3. Voltage Waveforms, Input and Output Transition Times**

## 9 Detailed Description

### 9.1 Overview

The SN74LV4T00 contains four independent 2-input NAND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function  $Y = \overline{A} \bullet \overline{B}$  in positive logic. The output level is referenced to the supply voltage ( $V_{CC}$ ) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-k $\Omega$  resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

#### 9.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in [图 9-1](#).

#### 注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

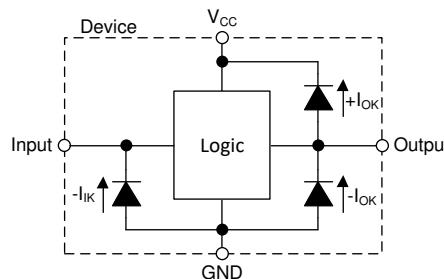


図 9-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 9.3.3 LVxT Enhanced Input Voltage

The SN74LV4T00 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage ( $V_{CC}$ ), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified  $V_{IH(MIN)}$  level for a HIGH input state, and at or below the specified  $V_{IL(MAX)}$  for a LOW input state. 図 9-2 shows the typical  $V_{IH}$  and  $V_{IL}$  levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-k $\Omega$  resistor is recommended and will typically meet all requirements.

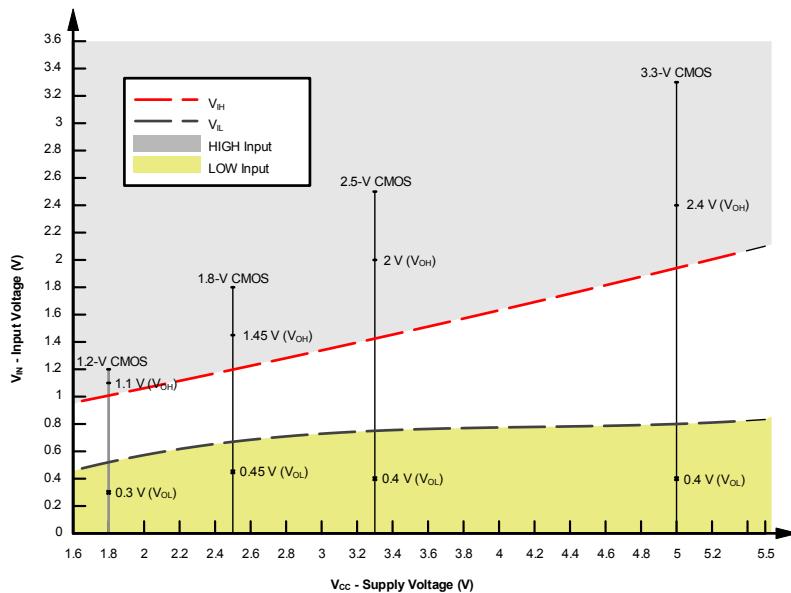


図 9-2. LVxT Input Voltage Levels

### 9.3.3.1 Down Translation

Signals can be translated down using the SN74LV4T00. The voltage applied at the  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0 V in the LOW state. As shown in [图 9-2](#), ensure that the input signals in the HIGH state are between  $V_{IH(MIN)}$  and 5.5 V, and input signals in the LOW state are lower than  $V_{IL(MAX)}$ .

As shown in [图 9-3](#) for example, the standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V  $V_{CC}$ .

*Down Translation Combinations* are as follows:

- 1.8-V  $V_{CC}$  – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V  $V_{CC}$  – Inputs from 3.3 V and 5.0 V
- 3.3-V  $V_{CC}$  – Inputs from 5.0 V

### 9.3.3.2 Up Translation

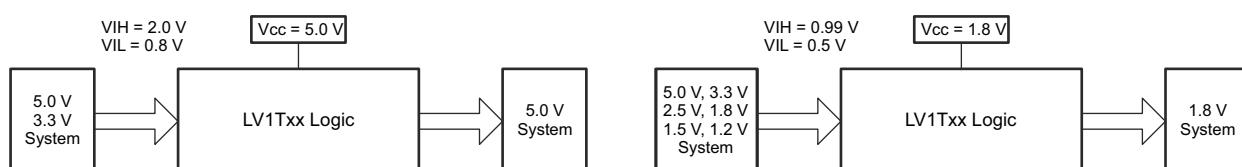
Input signals can be up translated using the SN74LV4T00. The voltage applied at  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a  $V_{IH(MIN)}$  of 3.5 V. For the SN74LV4T00,  $V_{IH(MIN)}$  with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in [图 9-3](#), ensure that the input signals in the HIGH state are above  $V_{IH(MIN)}$  and input signals in the LOW state are lower than  $V_{IL(MAX)}$ .

*Up Translation Combinations* are as follows:

- 1.8-V  $V_{CC}$  – Inputs from 1.2 V
- 2.5-V  $V_{CC}$  – Inputs from 1.8 V
- 3.3-V  $V_{CC}$  – Inputs from 1.8 V and 2.5 V
- 5.0-V  $V_{CC}$  – Inputs from 2.5 V and 3.3 V



**图 9-3. LVxT Up and Down Translation Example**

## 9.4 Device Functional Modes

[表 9-1](#) lists the functional modes of the SN74LV4T00.

**表 9-1. Function Table**

INPUTS <sup>(1)</sup>		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

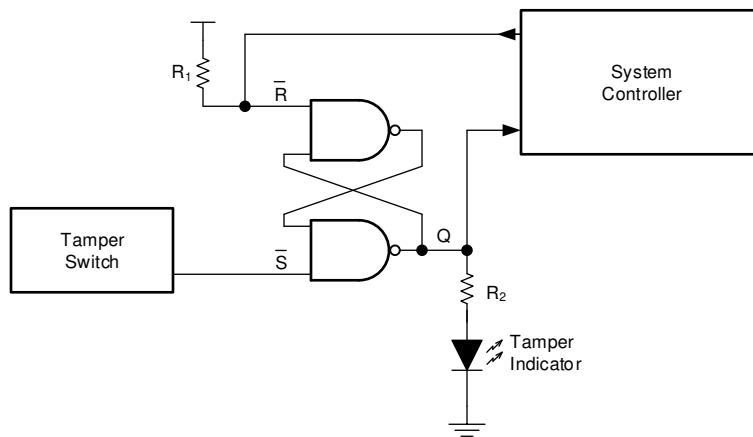
### 10.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in [图 10-1](#). The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SN74LV4T00 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the  $\bar{R}$  input which returns the Q output back to LOW.

The inputs of this active-low SR latch can often be driven by open-drain outputs which can produce slow input transition rates when they transition from LOW to Hi-Z. This makes the SN74LV4T00 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

### 10.2 Typical Application



[图 10-1. Typical Application Block Diagram](#)

#### 10.2.1 Design Requirements

##### 10.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV4T00 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV4T00 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV4T00 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV4T00 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation](#) application note.

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note.

#### 注意

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 10.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV4T00 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74LV4T00 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### 10.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 10.2.2 Application Curves

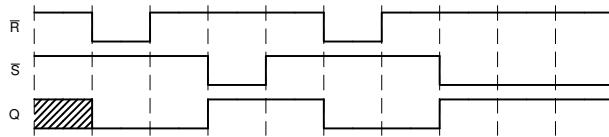


图 10-2. Application Timing Diagram

## 11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 12.2 Layout Example

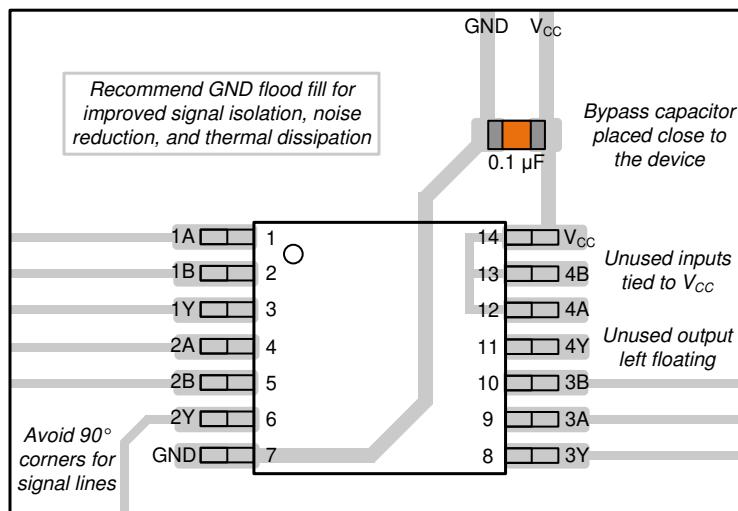


图 12-1. Example Layout for the SN74LV4T00

## 13 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

### 13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 13.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

### 13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 13.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 13.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LV4T00BQAR</a>	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV4T00
SN74LV4T00BQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV4T00
<a href="#">SN74LV4T00PWR</a>	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LV4T00
SN74LV4T00PWR.A	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4T00

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV4T00 :**

---

- Automotive : [SN74LV4T00-Q1](#)

- Enhanced Product : [SN74LV4T00-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## GENERIC PACKAGE VIEW

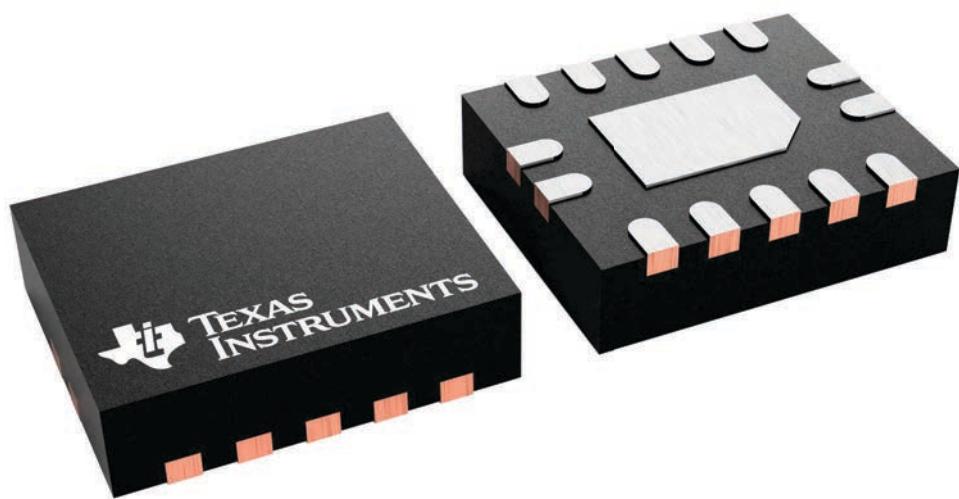
**BQA 14**

**WQFN - 0.8 mm max height**

**2.5 x 3, 0.5 mm pitch**

**PLASTIC QUAD FLATPACK - NO LEAD**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



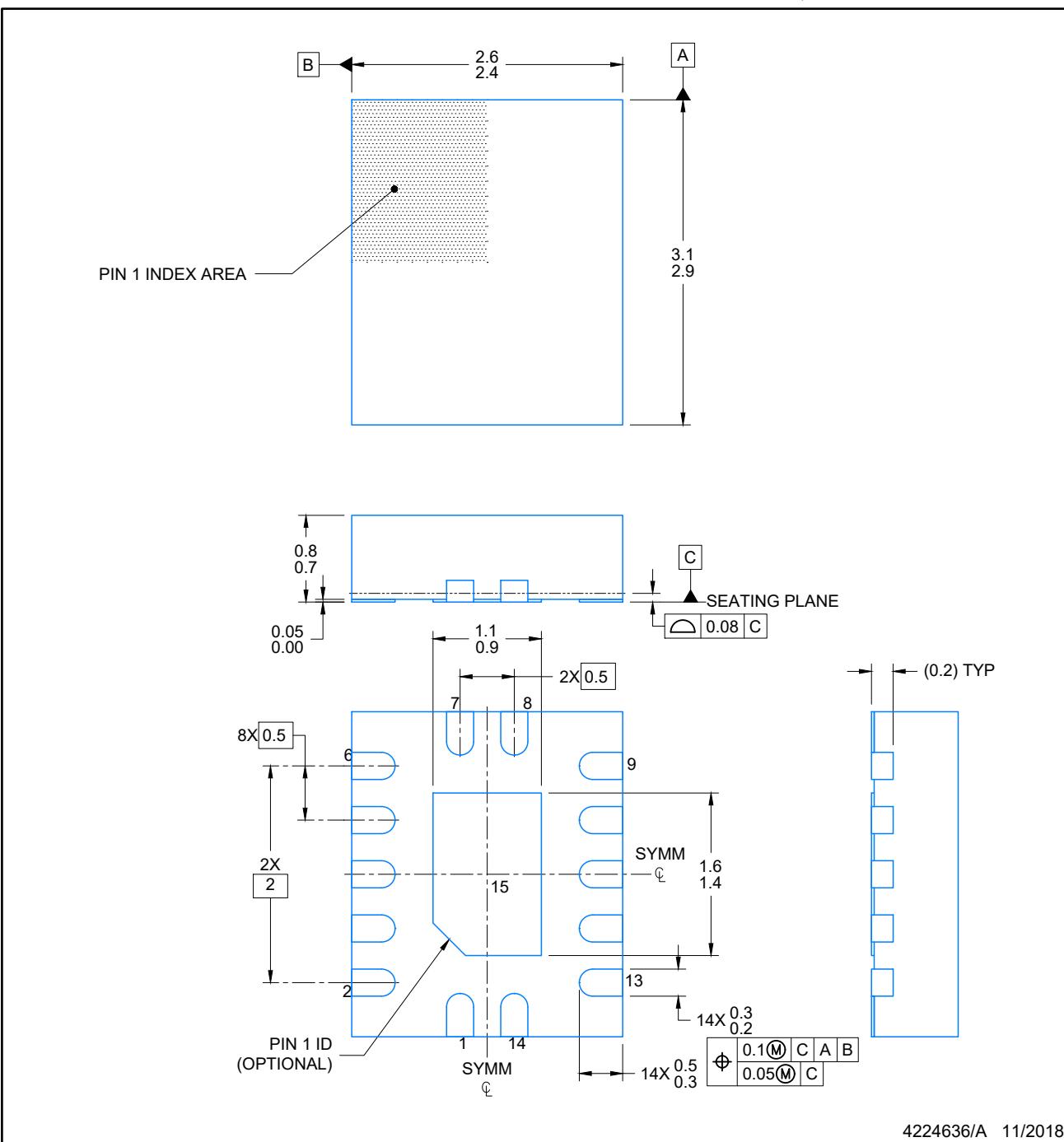
4227145/A

# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



### NOTES:

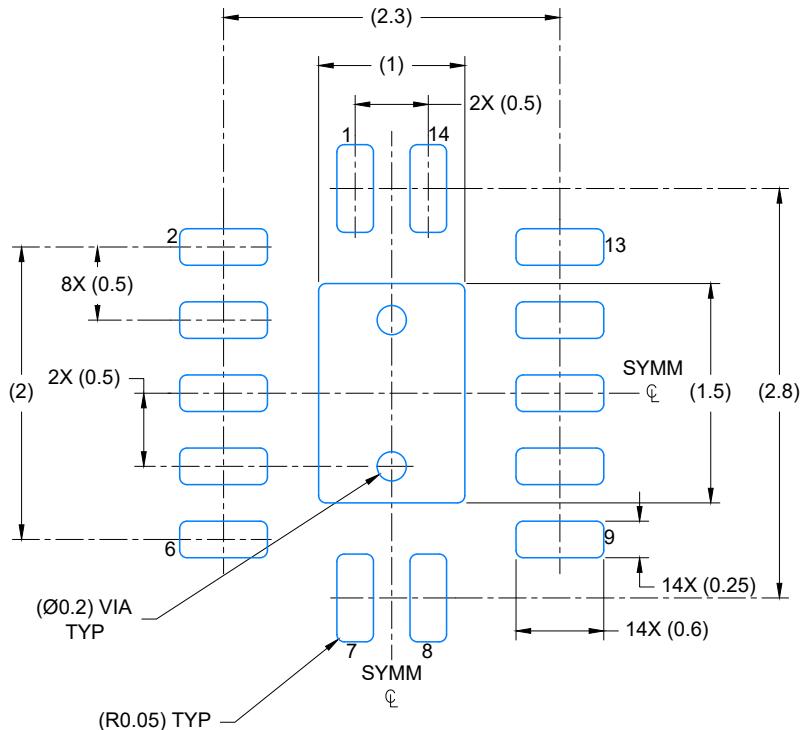
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

BQA0014A

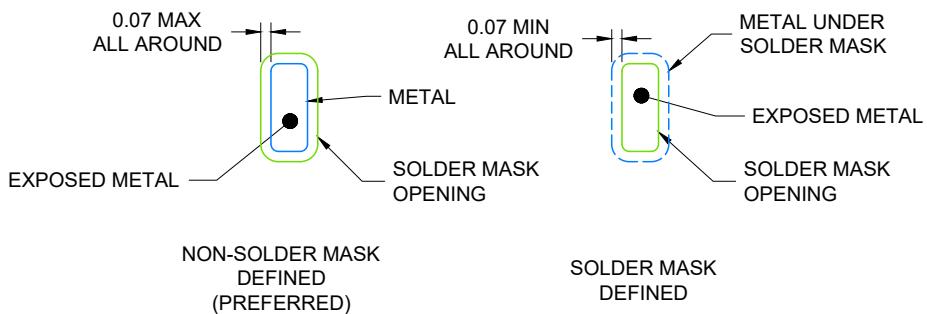
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

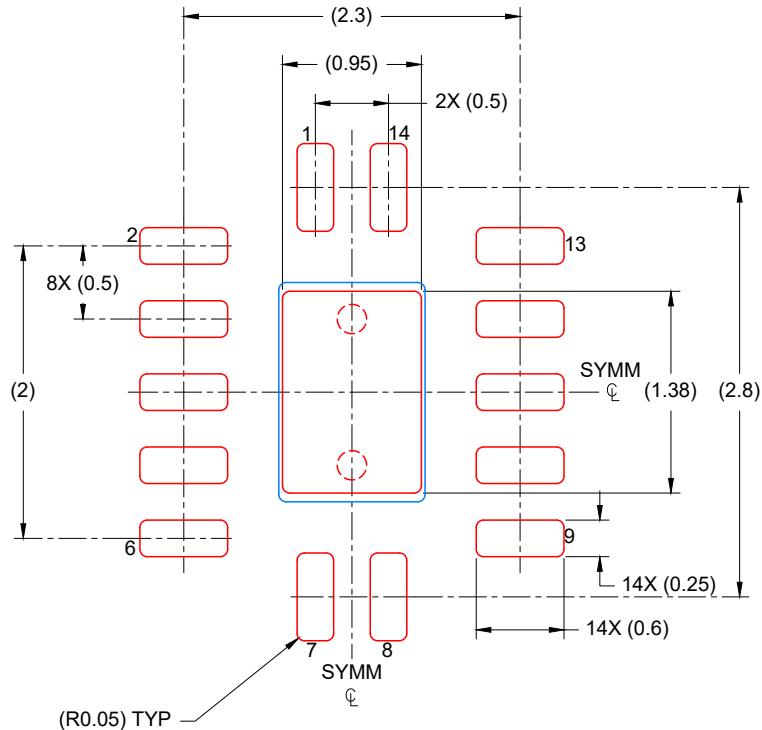
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
88% PRINTED COVERAGE BY AREA  
SCALE: 20X

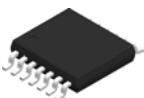
4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

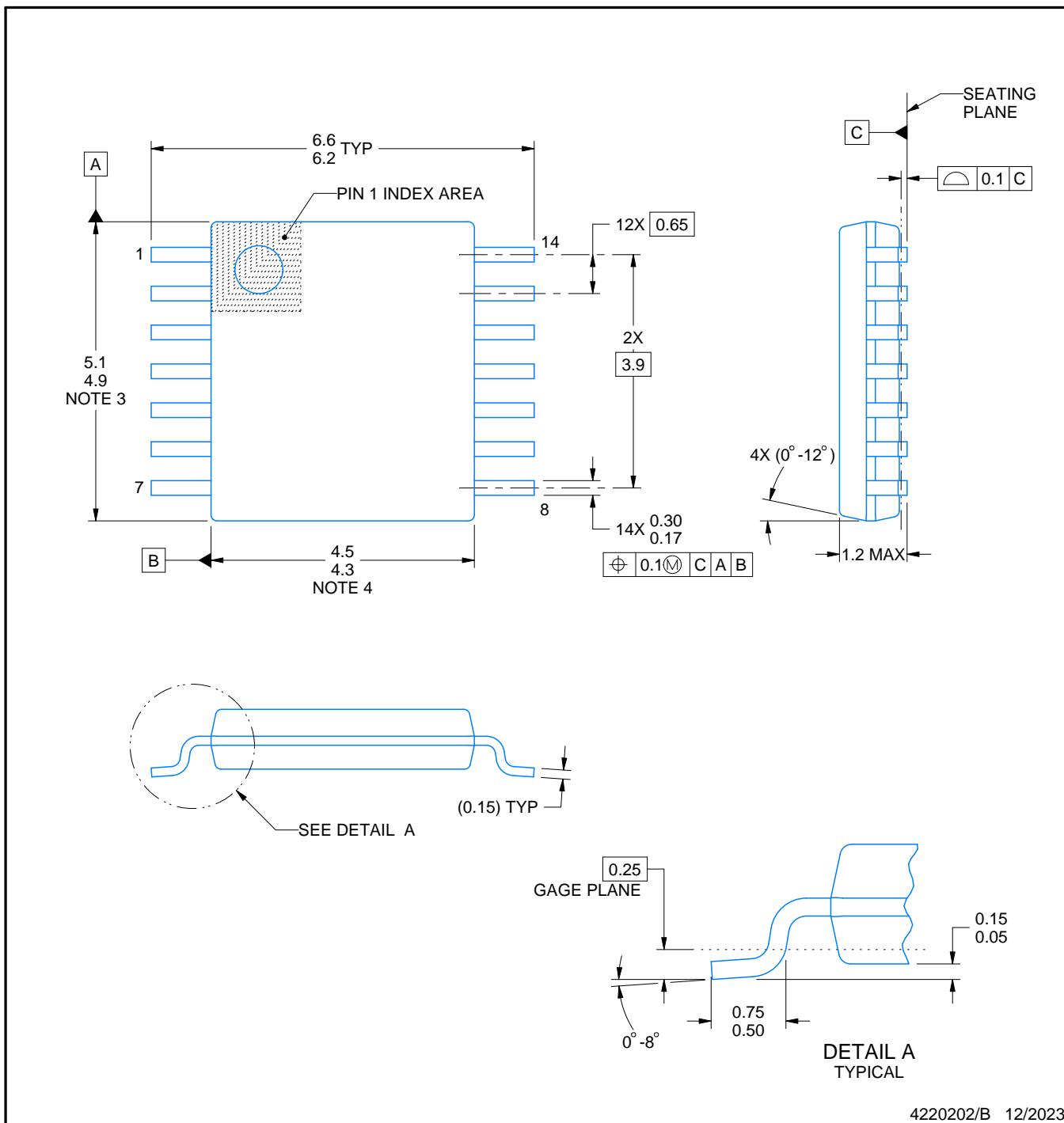
# PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

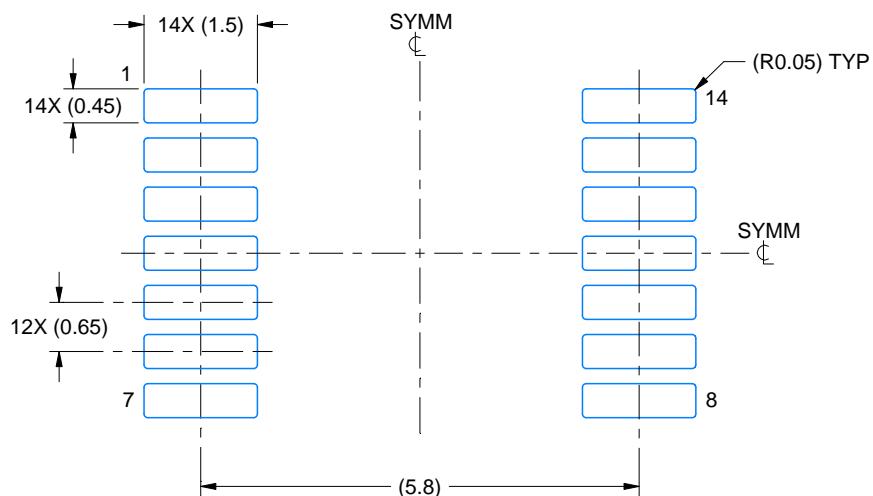
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

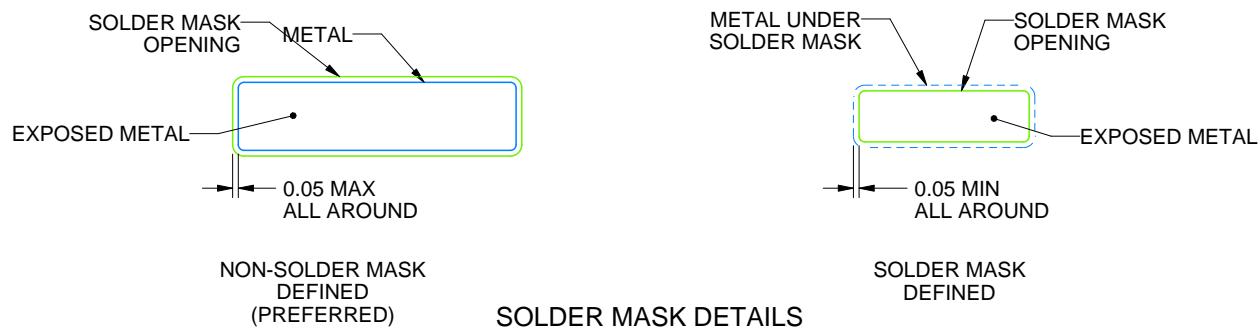
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

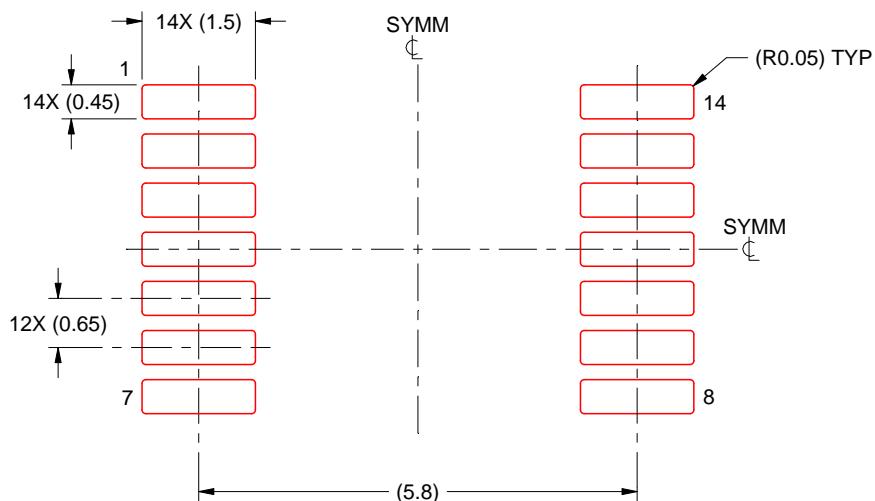
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

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