

# SN74LVC1G125-Q1 シングル・バス・バッファ・ゲート、3 ステート出力

## 1 特長

- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$  の周囲動作温度範囲
  - 人体モデル (HBM) ESD 分類レベル 2
  - デバイス帯電モデル (CDM) ESD 分類レベル C5
- 1.45mm<sup>2</sup>、0.5mm ピッチの小型パッケージ (DRY) で供給
- 5V  $V_{\text{CC}}$  動作に対応
- 過電圧許容の入力により 5.5V までの電圧に対応
- $V_{\text{CC}}$  への降圧変換をサポート
- 最大  $t_{\text{pd}}$ : 3.7ns (3.3V 時)
- 低消費電力、最大  $I_{\text{CC}}$ : 10 $\mu\text{A}$
- 3.3V において  $\pm 24\text{mA}$  の出力駆動能力
- $I_{\text{off}}$  により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

## 2 アプリケーション

- 車載アプリケーション向けに認定済み
- デジタル信号駆動能力の向上
- 最高 100MHz の方形波信号を再駆動
- 高インピーダンス・オフ状態によるデジタル信号のイネーブルまたはディセーブル

## 3 概要

このバス・バッファ・ゲートは、1.65V $\sim$ 5.5V の  $V_{\text{CC}}$  で動作するように設計されています。

SN74LVC1G125-Q1 は、3 ステート出力に対応したシングル・ライン・ドライバです。出力イネーブル ( $\overline{\text{OE}}$ ) 入力が HIGH になると、出力はディセーブルされます。

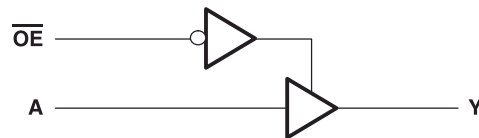
この CMOS デバイスは出力駆動能力が大きく、広い  $V_{\text{CC}}$  動作範囲にわたって静止電力消費が低く保たれます。

SN74LVC1G125-Q1 は、本体サイズ 1.45mm  $\times$  1.00mm の小型 DRY パッケージなど、各種のパッケージで供給されます。

### 製品情報

| 型番               | パッケージ <sup>(1)</sup> | 本体サイズ (公称)             |
|------------------|----------------------|------------------------|
| CLVC1G125QDBVRQ1 | SOT-23 (5)           | 2.90mm $\times$ 1.60mm |
| 1P1G125QDCKRQ1   | SC70 (5)             | 2.00mm $\times$ 1.25mm |
| 1P1G125QDRYRQ1   | SON (6)              | 1.45mm $\times$ 1.00mm |

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



## Table of Contents

|  |    |  |    |
|--|----|--|----|
| <b>1 特長</b> .....                                | 1  | 8.2 Functional Block Diagram.....                                | 10 |
| <b>2 アプリケーション</b> .....                          | 1  | 8.3 Feature Description.....                                     | 10 |
| <b>3 概要</b> .....                                | 1  | 8.4 Device Functional Modes.....                                 | 10 |
| <b>4 Revision History</b> .....                  | 2  | <b>9 Application and Implementation</b> .....                    | 11 |
| <b>5 Pin Configuration and Functions</b> .....   | 3  | 9.1 Application Information.....                                 | 11 |
| Pin Functions.....                               | 3  | 9.2 Typical Application.....                                     | 11 |
| <b>6 Specifications</b> .....                    | 4  | <b>10 Power Supply Recommendations</b> .....                     | 12 |
| 6.1 Absolute Maximum Ratings.....                | 4  | <b>11 Layout</b> .....   | 12 |
| 6.2 ESD Ratings.....                             | 4  | 11.1 Layout Guidelines.....                                      | 12 |
| 6.3 Recommended Operating Conditions.....        | 5  | 11.2 Layout Example.....   | 12 |
| 6.4 Thermal Information.....                     | 5  | <b>12 Device and Documentation Support</b> .....                 | 13 |
| 6.5 Electrical Characteristics.....              | 6  | 12.1 Receiving Notification of Documentation Updates..           | 13 |
| 6.6 Switching Characteristics.....               | 6  | 12.2 Support Resources.....                                      | 13 |
| 6.7 Operating Characteristics.....               | 6  | 12.3 Trademarks.....   | 13 |
| 6.8 Typical Characteristics.....                 | 7  | 12.4 静電気放電に関する注意事項.....  | 13 |
| <b>7 Parameter Measurement Information</b> ..... | 8  | 12.5 Glossary.....   | 13 |
| <b>8 Detailed Description</b> .....              | 10 | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | 13 |
| 8.1 Overview.....                                | 10 |  |    |

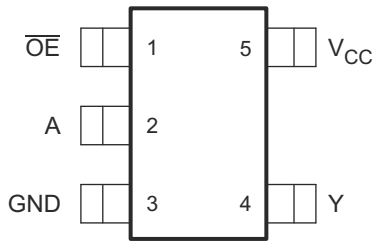
## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

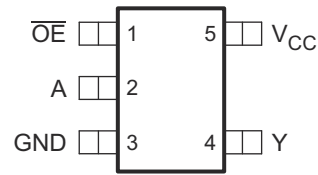
| <b>Changes from Revision D (August 2019) to Revision E (August 2020)</b> | <b>Page</b> |
|--|-------------|
| • 「製品情報」表の SC70 および SOT-23 パッケージのデバイス名を更新.....                           | 1           |
| • 文書全体にわたって表、図、相互参照の採番方法を更新.....   | 1           |

| <b>Changes from Revision C (April 2008) to Revision D (August 2019)</b>             | <b>Page</b> |
|---|-------------|
| • データシート・フォーマットを新しい TI 基準に変更.....   | 1           |
| • Added DRY package to <i>Pin Configuration and Functions</i> .....                 | 3           |
| • Added <i>Pin Functions</i> table. ....  | 3           |
| • Added <i>Handling Ratings</i> table. ....   | 4           |
| • Added <i>Thermal Information</i> table. ....                                      | 5           |
| • Added –40°C to 125°C Temperature range to <i>Electrical Characteristics</i> ..... | 6           |
| • Added <i>Detailed Description</i> section. ....                                   | 10          |
| • Added <i>Application and Implementation</i> section. ....                         | 11          |
| • Added <i>Layout</i> section. ....   | 12          |

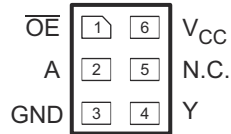
## 5 Pin Configuration and Functions



✎ 5-1. DBV package 5-pin SOT-23 (Top View)



✎ 5-2. DCK package 5-pin SC70 (Top View)



N.C. – No internal connection  
 See mechanical drawings for dimensions.

✎ 5-3. DRY package 6-pin SON (Transparent Top View)

## Pin Functions

| NAME            | PIN      |     | I/O    | DESCRIPTION                    |
|-----------------|----------|-----|--------|--------------------------------|
|                 | DBV, DCK | DRY |        |                                |
| $\overline{OE}$ | 1        | 1   | Input  | Active low Output Enable Input |
| A               | 2        | 2   | Input  | Input A                        |
| GND             | 3        | 3   | —      | Ground                         |
| Y               | 4        | 4   | Output | Output Y                       |
| $V_{CC}$        | 5        | 6   | —      | Positive supply                |
| NC              | —        | 5   | —      | No internal connection         |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   | MIN                | MAX                   | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range  | -0.5               | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>  | -0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>             | -0.5               | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current   | V <sub>I</sub> < 0 | -50                   | mA   |
| I <sub>OK</sub>  | Output clamp current  | V <sub>O</sub> < 0 | -50                   | mA   |
| I <sub>O</sub>   | Continuous output current   |                    | ±50                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND   |                    | ±100                  | mA   |
| T <sub>J</sub>   | Junction temperature  |                    | 150                   | °C   |
| T <sub>stg</sub> | Storage temperature   | -65                | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating* table.

### 6.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup><br>HBM ESD Classification Level | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per AEC Q100-011<br>CDM ESD Classification Level            | ±1000 |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

|                 |                                    | (1)   | MIN                    | MAX             | UNIT |
|-----------------|------------------------------------|---|------------------------|-----------------|------|
| V <sub>CC</sub> | Supply voltage                     | Operating                                       | 1.65                   | 5.5             | V    |
|                 |                                    | Data retention only                             | 1.5                    |                 |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V              | 0.65 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                | 1.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  | 2                      |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                | 0.7 × V <sub>CC</sub>  |                 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V              | 0.35 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                | 0.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  | 0.8                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                | 0.3 × V <sub>CC</sub>  |                 |      |
| V <sub>I</sub>  | Input voltage                      |   | 0                      | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     |   | 0                      | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V                        | –4                     |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         | –8                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           | –16                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         | –24                    |                 |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V                        | 4                      |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         | 8                      |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           | 16                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         | 24                     |                 |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | 20                     |                 | ns/V |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V                 | 10                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V                   | 5                      |                 |      |
| T <sub>A</sub>  | Operating free-air temperature     |   | –40                    | 125             | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | SN74LVC1G125-Q1                              |        |        | UNIT |      |
|-------------------------------|--|--------|--------|------|------|
|                               | DBV  | DCK    | DRY    |      |      |
|                               | 5 PINS                                       | 5 PINS | 6 PINS |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 229    | 278    | 439  | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 164    | 93     | 277  | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 62     | 65     | 271  | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 44     | 2      | 84   | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 62     | 64     | 271  | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –      | –      | –    | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS           | V <sub>CC</sub>  | –40 °C to 125 °C      |                    |     | UNIT   |
|------------------|---------------------------|--|-----------------------|--------------------|-----|--------|
|                  |                           |  | MIN                   | TYP <sup>(1)</sup> | MAX |        |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA | 1.65 V to 5.5 V  | V <sub>CC</sub> – 0.1 |                    |     | V      |
|                  | I <sub>OH</sub> = –4 mA   | 1.65 V   | 1.2                   |                    |     |        |
|                  | I <sub>OH</sub> = –8 mA   | 2.3 V  | 1.9                   |                    |     |        |
|                  | I <sub>OH</sub> = –16 mA  | 3 V  | 2.4                   |                    |     |        |
|                  | I <sub>OH</sub> = –24 mA  | 3 V  | 2.3                   |                    |     |        |
|                  |                           | 4.5 V  | 3.8                   |                    |     |        |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA  | 1.65 V to 5.5 V  | 0.1                   |                    |     | V      |
|                  | I <sub>OL</sub> = 4 mA    | 1.65 V   | 0.45                  |                    |     |        |
|                  | I <sub>OL</sub> = 8 mA    | 2.3 V  | 0.3                   |                    |     |        |
|                  | I <sub>OL</sub> = 16 mA   | 3 V  | 0.4                   |                    |     |        |
|                  | I <sub>OL</sub> = 24 mA   | 3 V  | 0.55                  |                    |     |        |
|                  |                           | 4.5 V  | 0.55                  |                    |     |        |
| I <sub>I</sub>   | A or OE inputs            | V <sub>I</sub> = 5.5 V or GND  | 0 to 5.5 V            |                    |     | ±5 μA  |
| I <sub>off</sub> |                           | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                     | 0                     |                    |     | ±10 μA |
| I <sub>OZ</sub>  |                           | V <sub>O</sub> = 0 to 5.5 V  | 3.6 V                 |                    |     | 10 μA  |
| I <sub>CC</sub>  |                           | V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0                            | 1.65 V to 5.5 V       |                    |     | 10 μA  |
| ΔI <sub>CC</sub> |                           | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 5.5 V          |                    |     | 500 μA |
| C <sub>I</sub>   |                           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V                 |                    |     | 4 pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range of –40°C to 125°C, C<sub>L</sub> = 50 pF (unless otherwise noted)

(see [7-1](#))

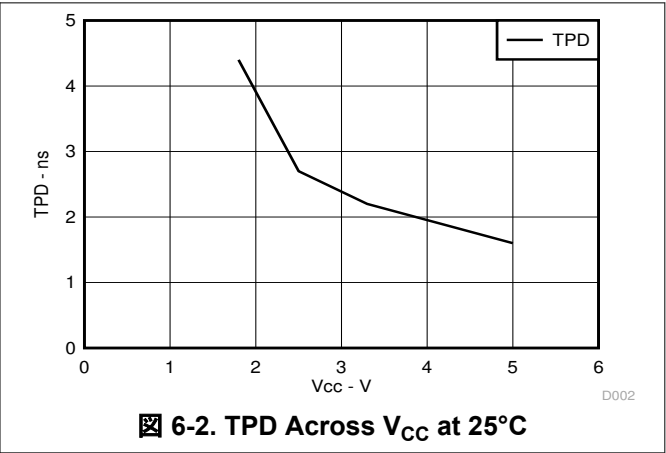
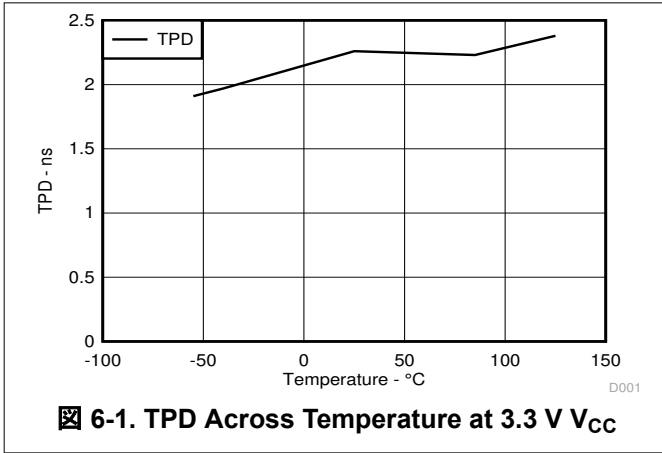
| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | V <sub>CC</sub> = 5 V ± 0.5 V |     | UNIT |
|------------------|--------------|-------------|---------------------------------|-----|-------------------------------|-----|------|
|                  |              |             | MIN                             | MAX | MIN                           | MAX |      |
| t <sub>pd</sub>  | A            | Y           | 1                               | 5.1 | 1                             | 4.1 | ns   |
| t <sub>en</sub>  | OE           | Y           | 1                               | 6   | 1                             | 5   | ns   |
| t <sub>dis</sub> | OE           | Y           | 1                               | 5   | 1                             | 4.2 | ns   |

## 6.7 Operating Characteristics

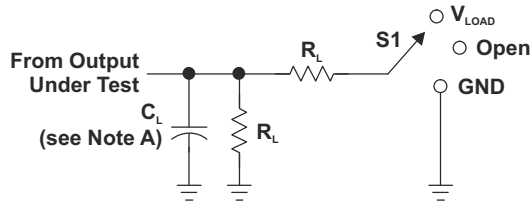
T<sub>A</sub> = 25°C

| PARAMETER                                     | TEST CONDITIONS  | V <sub>CC</sub> = 3.3 V | V <sub>CC</sub> = 5 V | UNIT |    |
|---|------------------|-------------------------|-----------------------|------|----|
|   |                  | TYP                     | TYP                   |      |    |
| C <sub>pd</sub> Power dissipation capacitance | Outputs enabled  | f = 10 MHz              | 19                    | 21   | pF |
|   | Outputs disabled |                         | 2                     | 4    |    |

## 6.8 Typical Characteristics



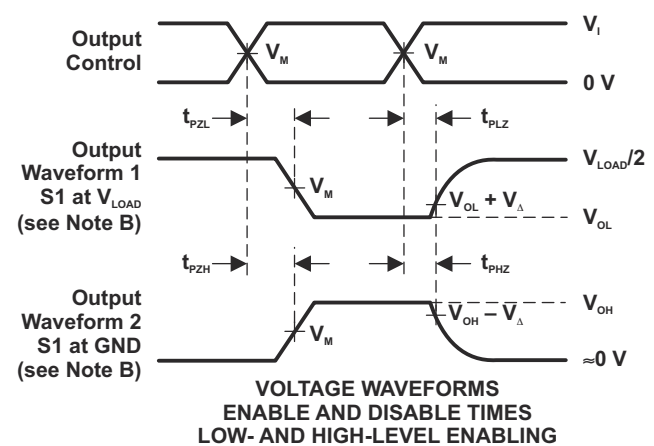
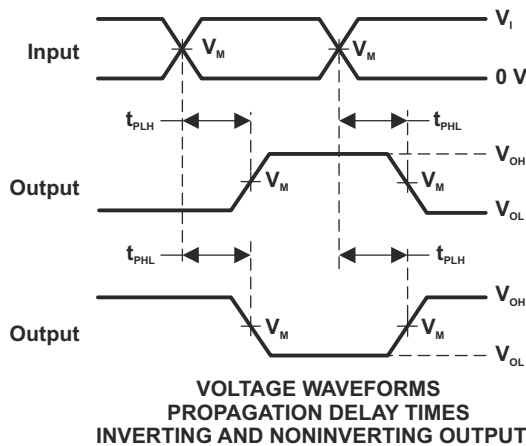
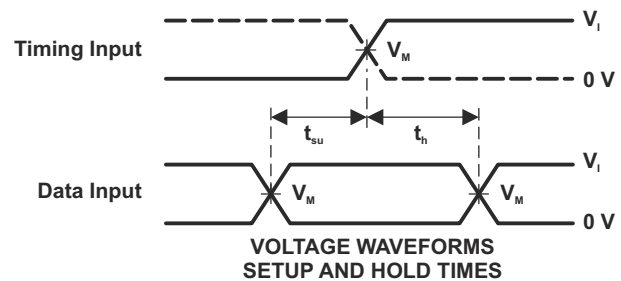
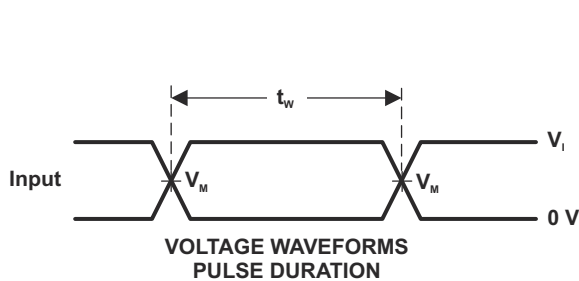
## 7 Parameter Measurement Information



LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

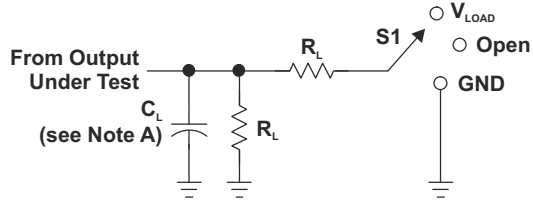
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_f/t_r$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 15 pF | 1 M $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

7-1. Load Circuit and Voltage Waveforms

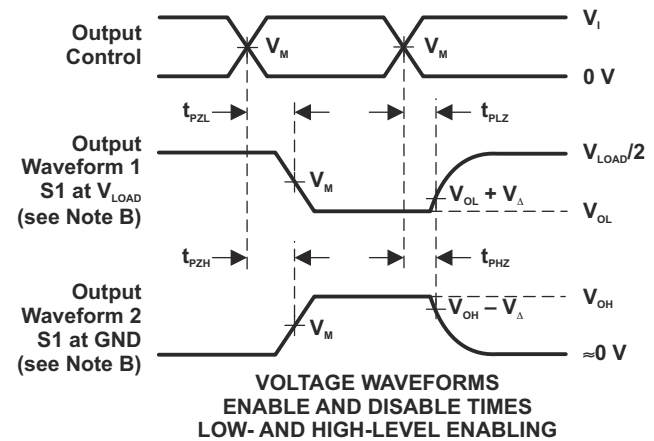
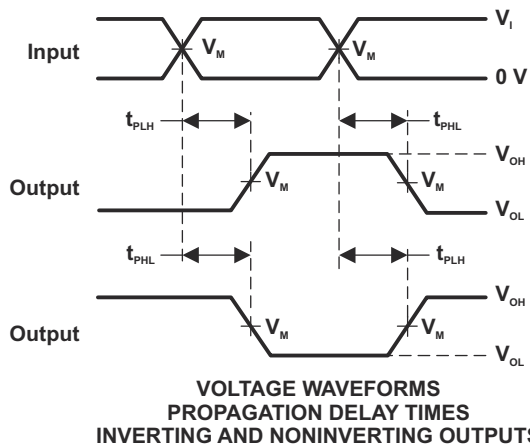
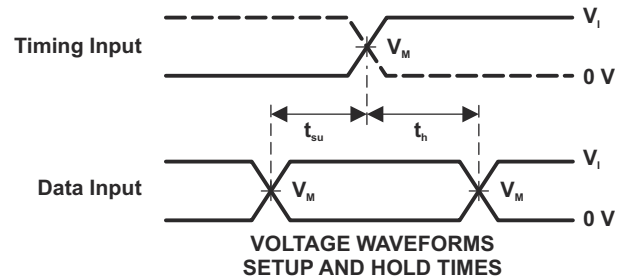
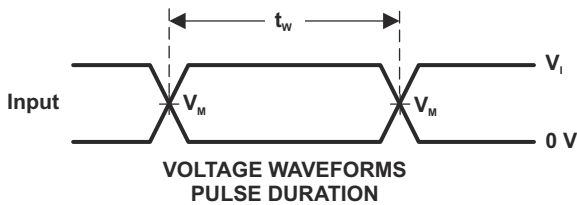




LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

## 7-2. Load Circuit and Voltage Waveforms

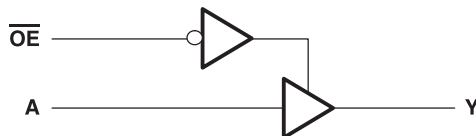
## 8 Detailed Description

### 8.1 Overview

The SN74LVC1G125-Q1 device contains one buffer gate device with output enable control and performs the Boolean function  $Y = A$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 5.5 V
- Allows down voltage translation
- Inputs accept voltages to 5.5 V
- $I_{off}$  feature allows voltages on the inputs and outputs, when  $V_{CC}$  is 0 V

### 8.4 Device Functional Modes

表 8-1. Function Table

| INPUTS          |   | OUTPUT |
|-----------------|---|--------|
| $\overline{OE}$ | A | Y      |
| L               | H | H      |
| L               | L | L      |
| H               | X | Z      |

## 9 Application and Implementation

### Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The SN74LVC1G125-Q1 device is a high drive CMOS device that can be used as an output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to  $V_{CC}$ .

### 9.2 Typical Application

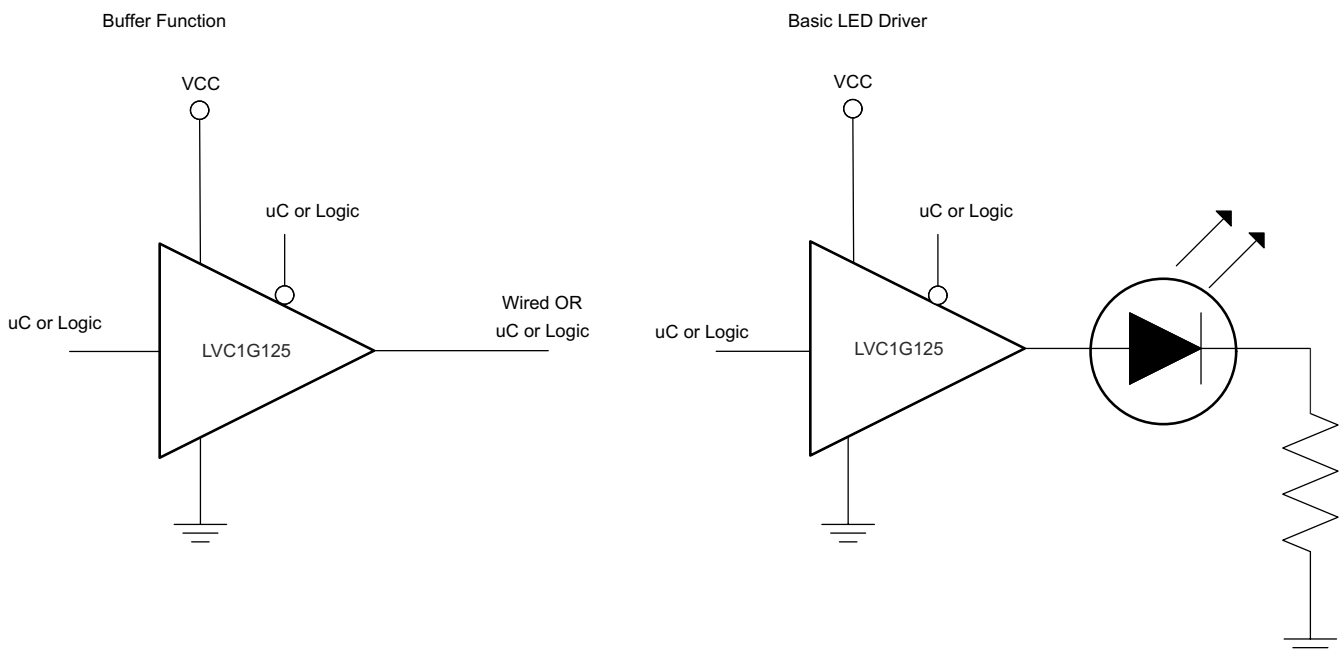


図 9-1. Typical Application Schematic

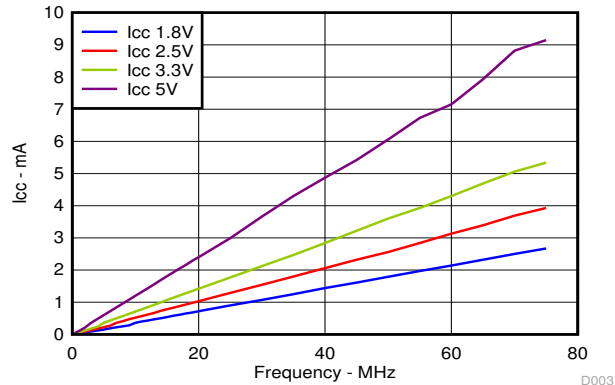
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended Input Conditions
  - Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .
- Recommend Output Conditions
  - Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curves



9-2. I<sub>CC</sub> vs Frequency, Square wave input signal

## 10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

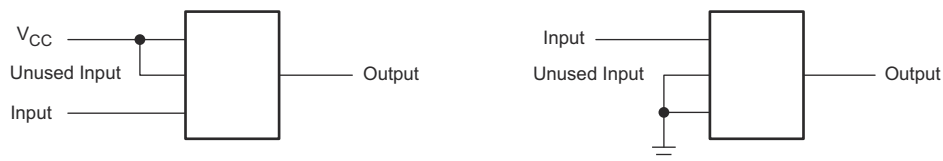
Each V<sub>CC</sub> pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- $\mu$ F capacitor is recommended and if there are multiple V<sub>CC</sub> pins then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 11-1 shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub>, whichever makes more sense or is more convenient.

### 11.2 Layout Example



11-1. Package Layout

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| 1P1G125QDCKRG4Q1 | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | CMR                     | <a href="#">Samples</a> |
| 1P1G125QDCKRQ1   | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (CMJ, CMR)              | <a href="#">Samples</a> |
| 1P1G125QDRYRQ1   | ACTIVE        | SON          | DRY             | 6    | 5000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | FX                      | <a href="#">Samples</a> |
| CLVC1G125QDBVRQ1 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | (34S5, C25O)            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G125-Q1 :**

- Catalog : [SN74LVC1G125](#)
- Enhanced Product : [SN74LVC1G125-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

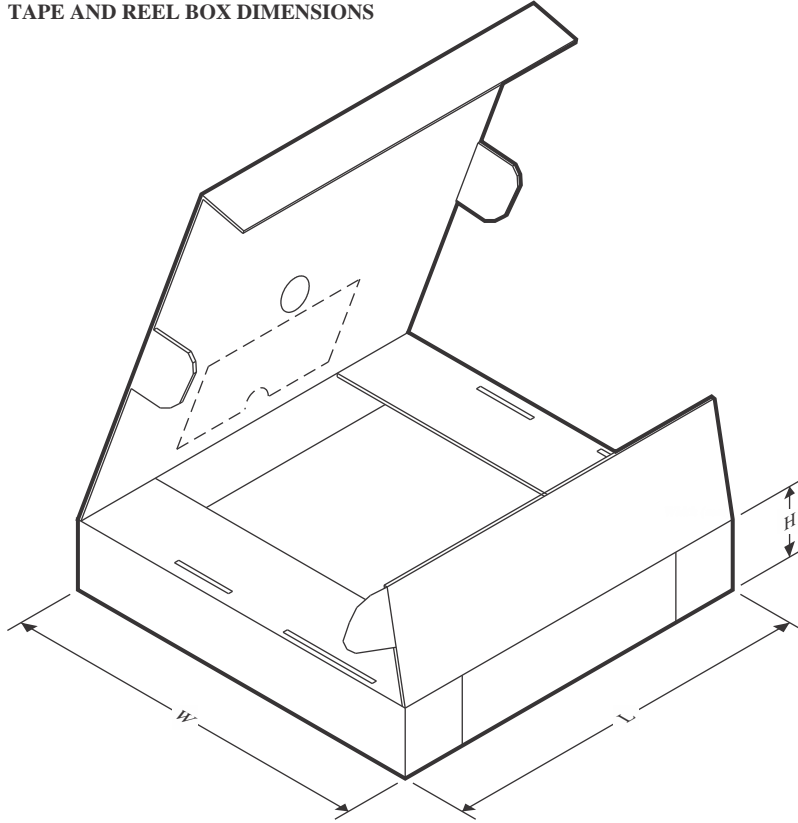
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 1P1G125QDCKRQ1   | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| 1P1G125QDRYRQ1   | SON          | DRY             | 6    | 5000 | 180.0              | 9.5                | 1.2     | 1.65    | 0.7     | 4.0     | 8.0    | Q1            |
| CLVC1G125QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 1P1G125QDCKRQ1   | SC70         | DCK             | 5    | 3000 | 190.0       | 190.0      | 30.0        |
| 1P1G125QDRYRQ1   | SON          | DRY             | 6    | 5000 | 189.0       | 185.0      | 36.0        |
| CLVC1G125QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |

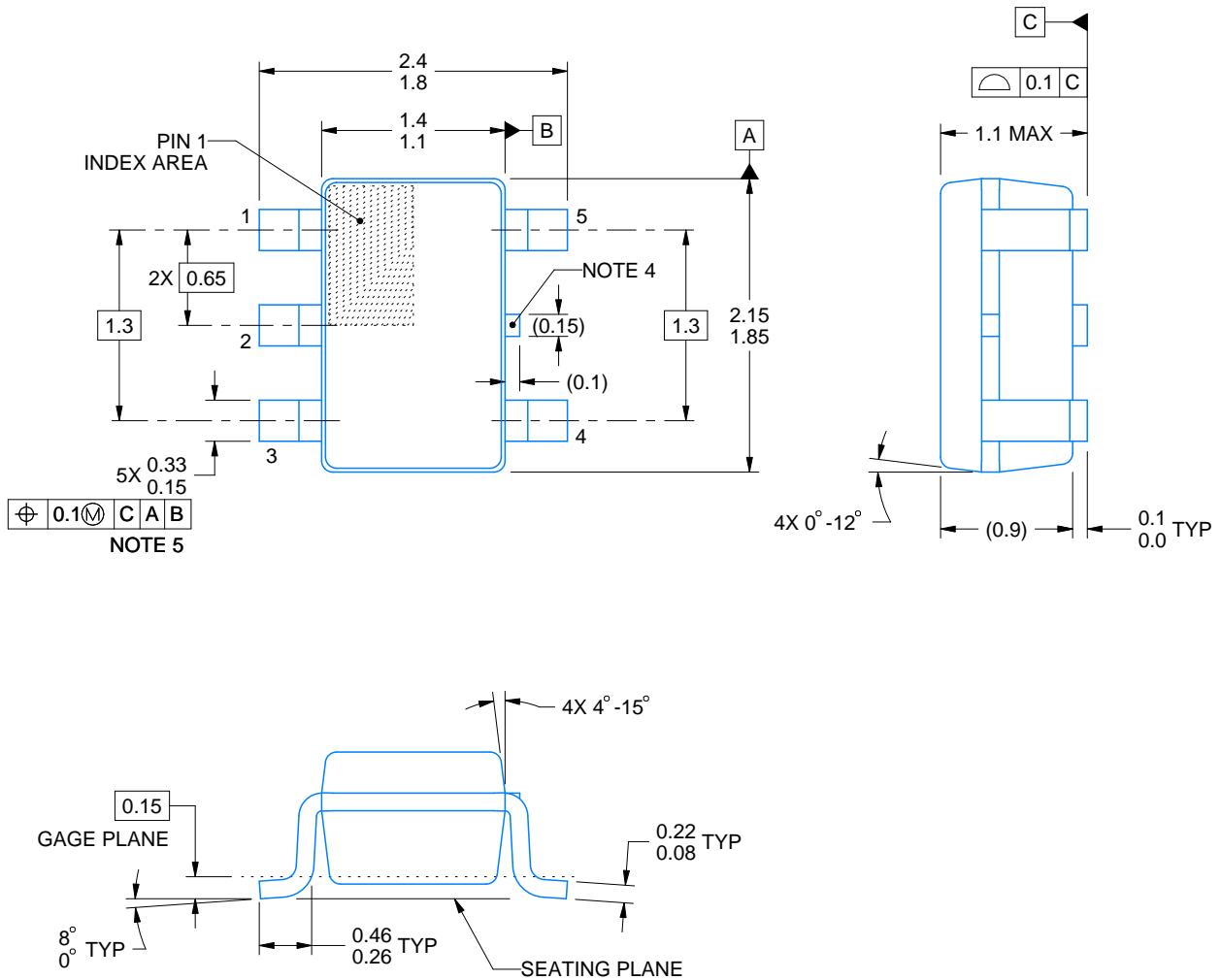
# DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

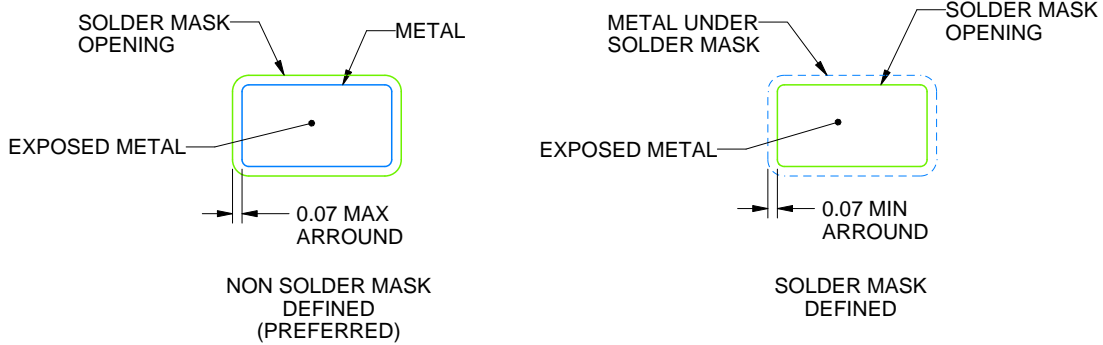
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

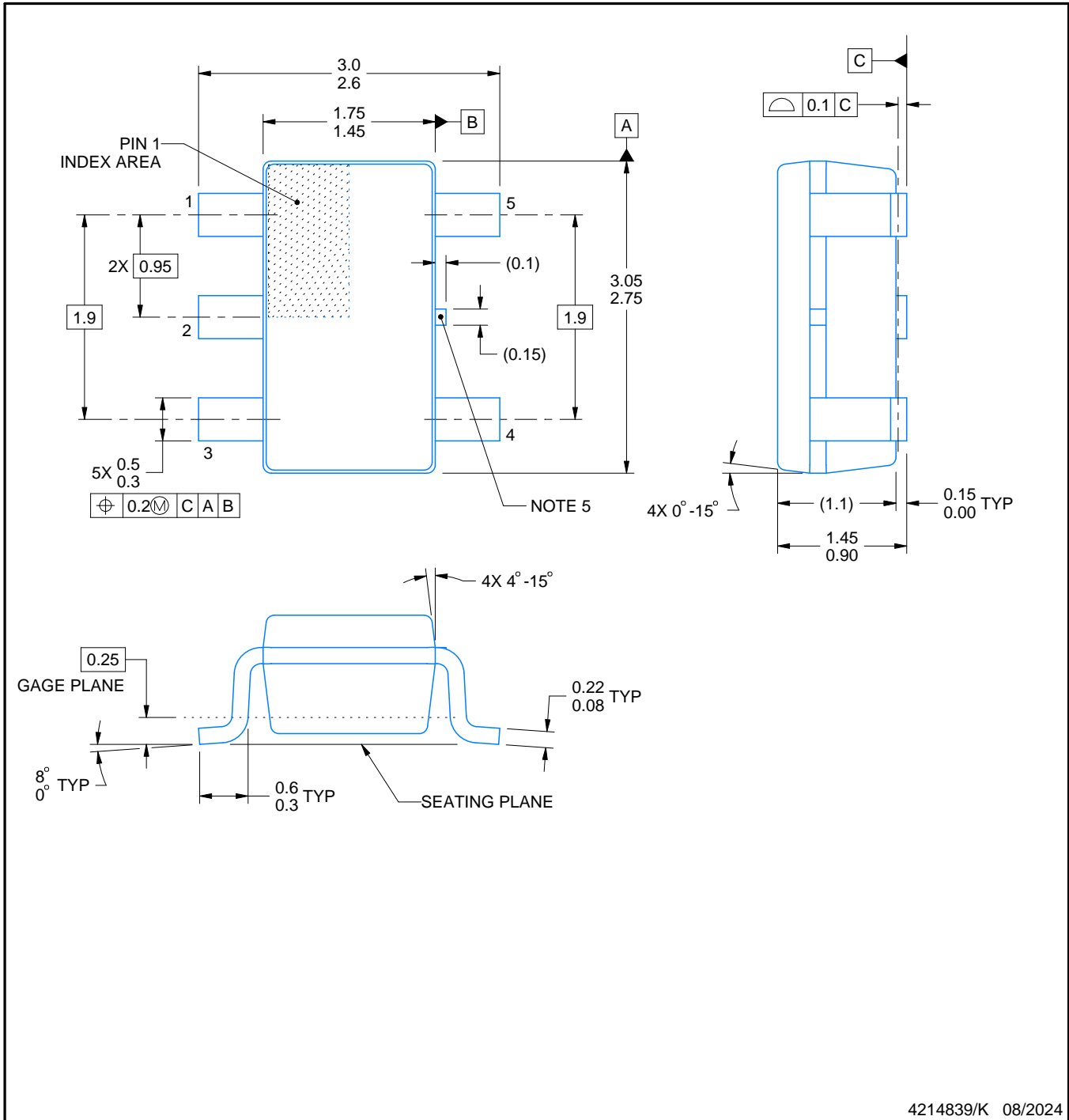
# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

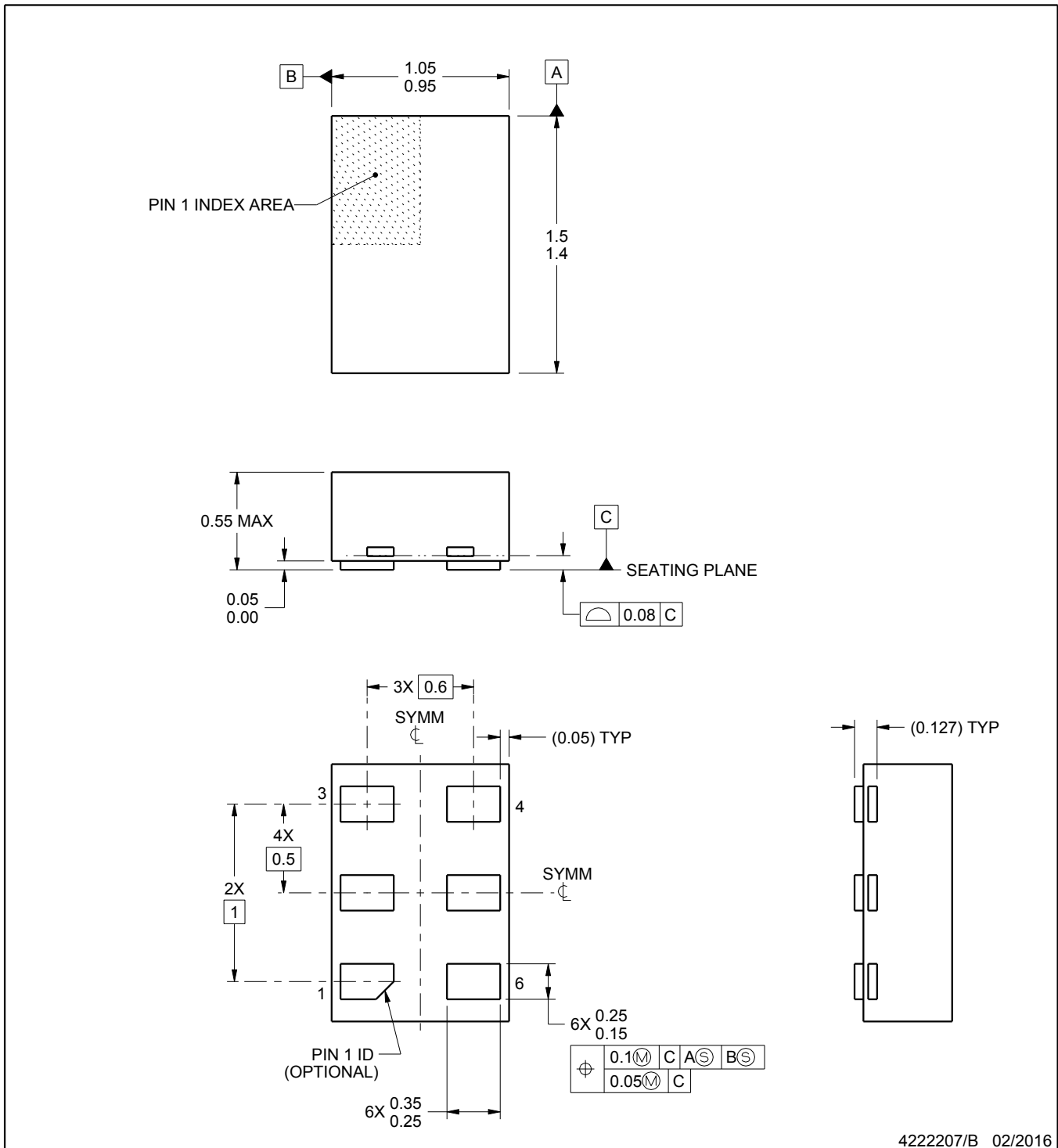
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G





4222207/B 02/2016

NOTES:

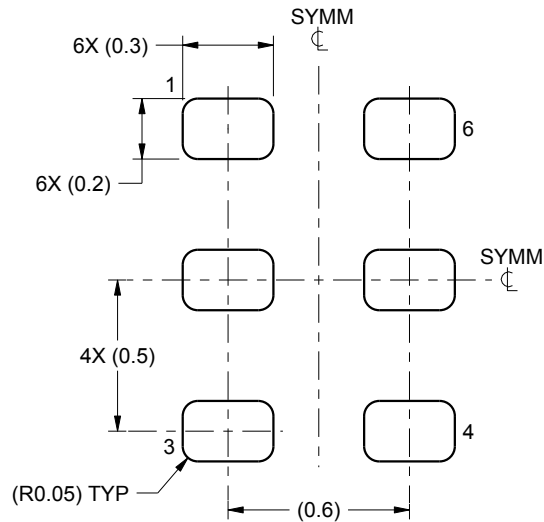
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

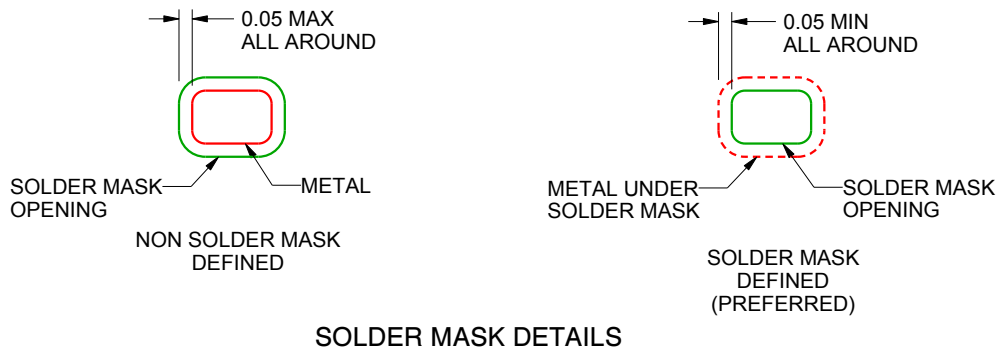
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

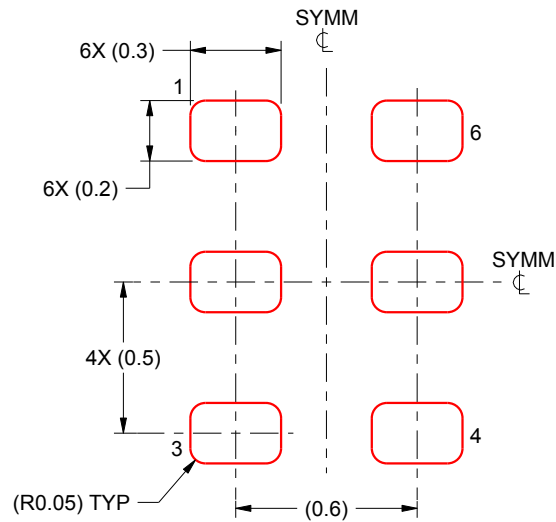
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、ます。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated