

SN74LVC1G139 2-to-4ライン・デコーダ

1 特長

- テキサス・インスツルメンツの NanoStar™ および NanoFree™ パッケージで供給
- 5V V_{CC} 動作をサポート
- 5.5Vまでの入力電圧に対応
- V_{CC} への降圧変換をサポート
- 3.3Vおよび15pFで最大 t_{pd} が4.9ns
- 低消費電力、最大 I_{CC} 10 μ A
- 3.3Vにおいて ± 24 mAの出力駆動能力
- I_{off} により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- JESD22を超えるESD保護
 - 2000V、人体モデル(A114-A)
 - 200V、マシン・モデル(A115-A)
 - 1000V、荷電デバイス・モデル(C101)

2 アプリケーション

- AVレシーバ
- ソリッド・ステート・ドライブ(SSD): クライアントおよびエンタープライズ
- テレビ: LCD、デジタル、高解像度(HD)
- タブレット: エンタープライズ
- ビデオ・アナリティクス: サーバー

3 概要

SN74LVC1G139 2-to-4ライン・デコーダは、1.65V～5.5Vの V_{CC} で動作するように設計されています。

SN74LVC1G139 2-to-4ライン・デコーダは、伝搬遅延時間を極めて短くする必要がある、高速メモリ・デコーディングやデータ・ルーティングといった用途に適しています。高性能メモリ・システムでは、このデコーダを使用することにより、システム・デコードの影響を最小限に抑制できます。高速イネーブル回路を使用する高速メモリと組み合わせた場合、このデコーダの遅延時間とメモリのイネーブル時間は通例、メモリの標準的なアクセス時間を下回ります。これは、SN74LVC1G139による実効的なシステム遅延時間は極めて短いということを意味しています。

NanoStarおよびNanoFreeパッケージは、デバイス・パッケージの概念を大きく変える技術であり、ダイをパッケージとして使用します。

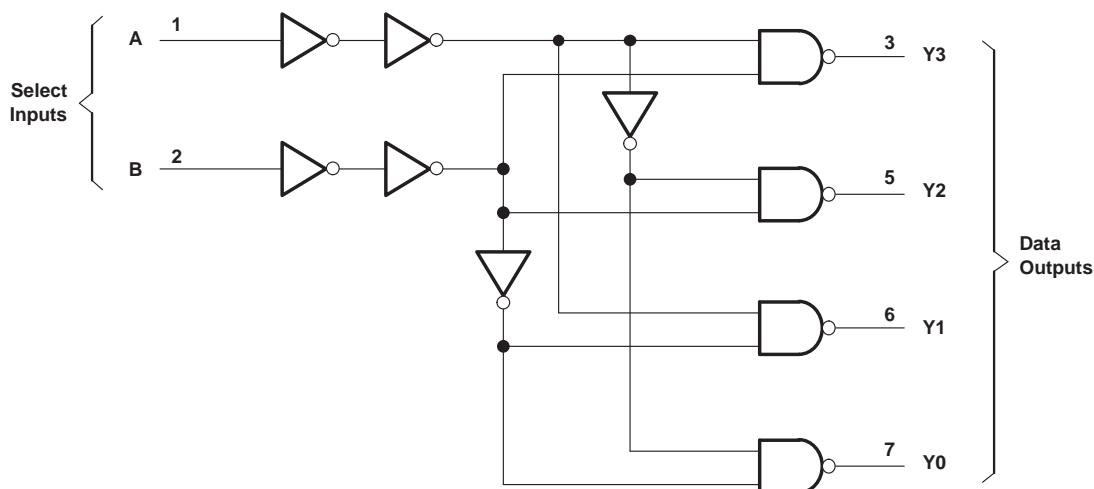
このデバイスは、 I_{off} を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。 I_{off} 回路が出力をディスエーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
SN74LVC1G139DCT	SM8 (8)	2.95mmx2.80mm
SN74LVC1G139DCU	VSSOP (8)	2.30mmx2.00mm
SN74LVC1G139YZP	DSBGA (8)	1.91mmx0.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (February 2014) から Revision E に変更 Page

- Updated the YZP package drawing

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Revision C (December 2005) から Revision D に変更 Page

- 「アプリケーション」セクション、「製品情報」の表、「ESD定格」の表、「熱に関する情報」の表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ...

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Revision B (December 2005) から Revision C に変更 Page

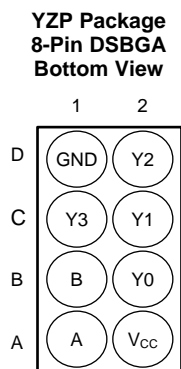
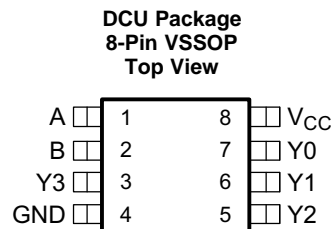
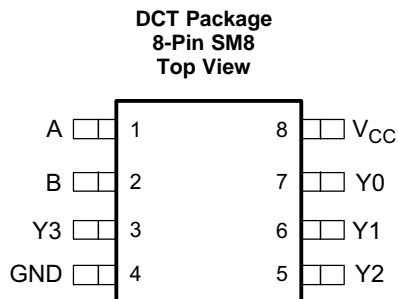
- ドキュメントを新しいTIデータシートのフォーマットに更新
- 「特長」を更新。
- 「注文情報」の表を削除。

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5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DCT, DCU	YZP		
A	1	A1	I	Adress input, bit 0
B	2	B1	I	Adress input, bit 1
Y ₃	3	C1	O	Output 3, low when B is high and A is high
GND	4	D1	—	Ground
Y ₂	5	D2	O	Output 2, low when B is high and A is low
Y ₁	6	C2	O	Output 1, low when B is low and A is high
Y ₀	7	B2	O	Output 0, low when B is low and A is low
V _{CC}	8	A2	—	Power pin

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage, V_{CC}		-0.5	6.5	V
Input Voltage, V_I		-0.5	6.5	V
Voltage applied to any output in the high-impedance or power-off state, V_O ⁽²⁾		-0.5	6.5	V
Voltage applied to any output in the high or low state, V_O ⁽²⁾⁽³⁾		-0.5	$V_{CC} + 0.5$	V
Input clamp current, I_{IK}	$V_I < 0$		-50	mA
Output clamp current, I_{OK}	$V_O < 0$		-50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND, I_{CC}			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	
	Machine model	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		mA
		V _{CC} = 2.3 V	–8		
		V _{CC} = 3 V	–16		
			–24		
		V _{CC} = 4.5 V	–32		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 3 V	16		
			24		
		V _{CC} = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V _{CC} = 3.3 V ± 0.3 V	15		
		V _{CC} = 5 V ± 0.5 V	10		
T _A	Operating free-air temperature	–40	85	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the [Implications of Slow or Floating CMOS Inputs application report](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G139			UNIT	
	DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)		
	8 PINS	8 PINS	8 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	194	195	106	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	124	74	1.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	106	74	11	°C/W
ψ _{JT}	Junction-to-top characterization parameter	48	6.7	3.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	105	73	11	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = -100 μA, V _{CC} = 1.65 V to 5.5 V		V _{CC} - 0.1			V
	I _{OH} = -4 mA, V _{CC} = 1.65 V		1.2			
	I _{OH} = -8 mA, V _{CC} = 2.3 V		1.9			
	I _{OH} = -16 mA, V _{CC} = 3 V		2.4			
	I _{OH} = -24 mA, V _{CC} = 3 V		2.3			
	I _{OH} = -32 mA, V _{CC} = 4.5 V		3.8			
V _{OL} Low-level output voltage	I _{OL} = 100 μA, V _{CC} = 1.65 V to 5.5 V		0.1			V
	I _{OL} = 4 mA, V _{CC} = 1.65 V		0.45			
	I _{OL} = 8 mA, V _{CC} = 2.3 V		0.3			
	I _{OL} = 16 mA, V _{CC} = 3 V		0.4			
	I _{OL} = 24 mA, V _{CC} = 3 V		0.55			
	I _{OL} = 32 mA, V _{CC} = 4.5 V		0.55			
I _I Inflection-point current	A or B inputs: V _I = 5.5 V or GND, V _{CC} = 0 to 5.5 V		±1			μA
I _{off} Off-state current	V _I or V _O = 5.5 V, V _{CC} = 0		±5			μA
I _{CC} Supply current	V _I = 5.5 V or GND, I _O = 0, V _{CC} = 1.65 V to 5.5 V		10			μA
ΔI _{CC} Supply current change	One input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND, V _{CC} = 3 V to 5.5 V		500			μA
C _i Input capacitance	V _I = V _{CC} or GND, V _{CC} = 3.3 V		4			pF

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

 over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT	
t _{pd} Propagation delay time	A or B-to-Y	See 表 2	V _{CC} = 1.8 V ± 0.15 V	2.7	15.3	ns
			V _{CC} = 2.5 V ± 0.2 V	1.5	7.5	
			V _{CC} = 3.3 V ± 0.3 V	0.9	4.9	
			V _{CC} = 5 V ± 0.5 V	0.8	3.6	
		See 表 3	V _{CC} = 1.8 V ± 0.15 V	3	16.7	
			V _{CC} = 2.5 V ± 0.2 V	1.6	8.2	
			V _{CC} = 3.3 V ± 0.3 V	1.2	5.9	
			V _{CC} = 5 V ± 0.5 V	1.1	4.2	

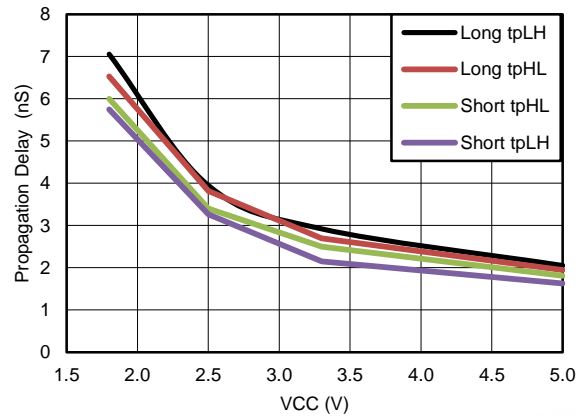
6.7 Operating Characteristics

 T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
C _{pd} ⁽¹⁾ Power dissipation capacitance	f = 10 MHz	V _{CC} = 1.8 V	31			pF
		V _{CC} = 2.5 V	34			
		V _{CC} = 3.3 V	36			
		V _{CC} = 5 V	39			

(1) Two outputs switching.

7 Typical Characteristics



(1) Short is 2 inverter path. Long is 3 inverter path.

图 1. Propagation Delay vs VCC

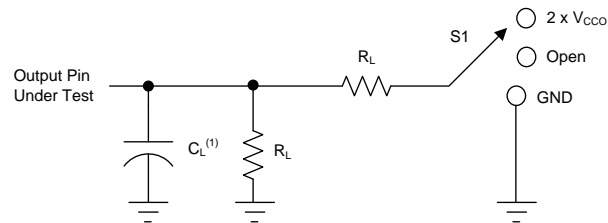
8 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators that have the following characteristics:

- $PRR \leq 10 \text{ MHz}$
- $Z_O = 50 \Omega$

注

All parameters and waveforms are not applicable to all devices.



(1) C_L includes probe and jig capacitance.

图 2. Load Circuit

表 1. Loading Conditions for Parameter

TEST	S1
$t_{PLH}^{(1)}$, $t_{PHL}^{(1)}$	Open
$t_{PLZ}^{(2)}$, $t_{PZL}^{(3)}$	V_{LOAD}
$t_{PHZ}^{(2)}$, $t_{PZH}^{(3)}$	GND

(1) t_{PLH} and t_{PHL} are the same as t_{pd} .

(2) t_{PLZ} and t_{PHZ} are the same as t_{dis} .

(3) t_{PZL} and t_{PZH} are the same as t_{en} .

表 2. Loading Conditions for V_{CC} – Case 1

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_A
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC} / 2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC} / 2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	V_{CC}	$\leq 2.5 \text{ ns}$	$V_{CC} / 2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V

表 3. Loading Conditions for V_{CC} – Case 2

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_A
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC} / 2$	$2 \times V_{CC}$	30 pF	1 M Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC} / 2$	$2 \times V_{CC}$	30 pF	500 M Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	30 pF	500 M Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	V_{CC}	$\leq 2.5 \text{ ns}$	$V_{CC} / 2$	$2 \times V_{CC}$	30 pF	500 M Ω	0.3 V

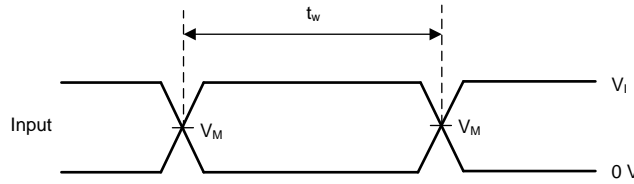
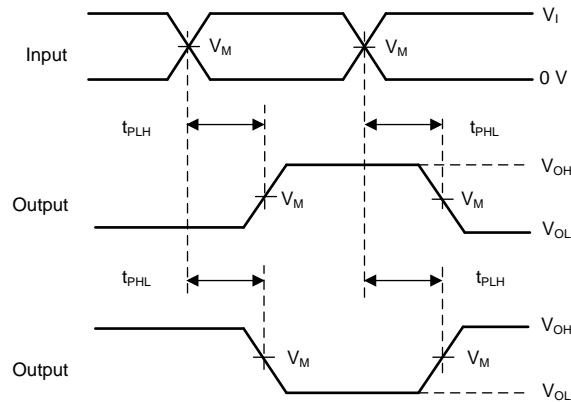


图 3. Voltage Waveforms: Pulse Duration



(1) The outputs are measured one at a time, with one transition per measurement.

图 4. Voltage Waveforms: Propagation Delay Times Inverting And Noninverting Outputs

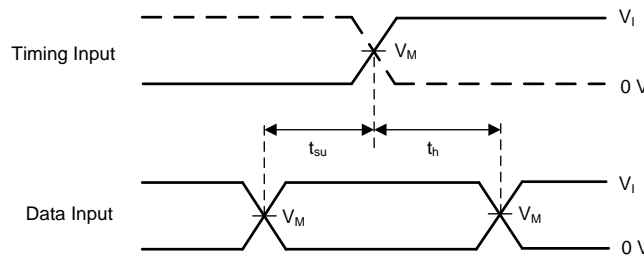
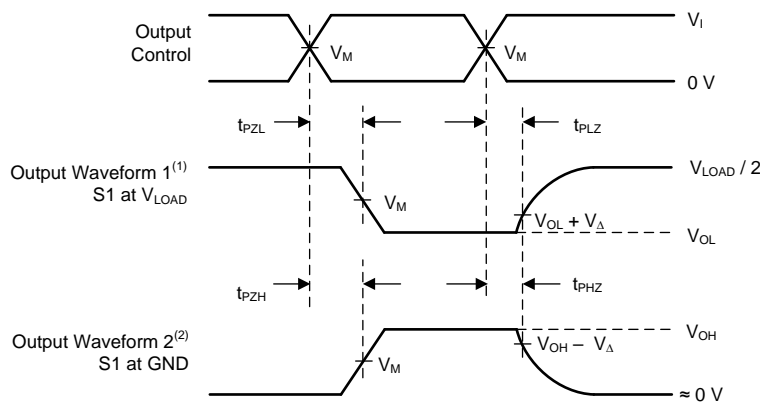


图 5. Voltage Waveforms: Setup and Hold Times



- (1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
- (2) Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- (3) The outputs are measured one at a time, with one transition per measurement.

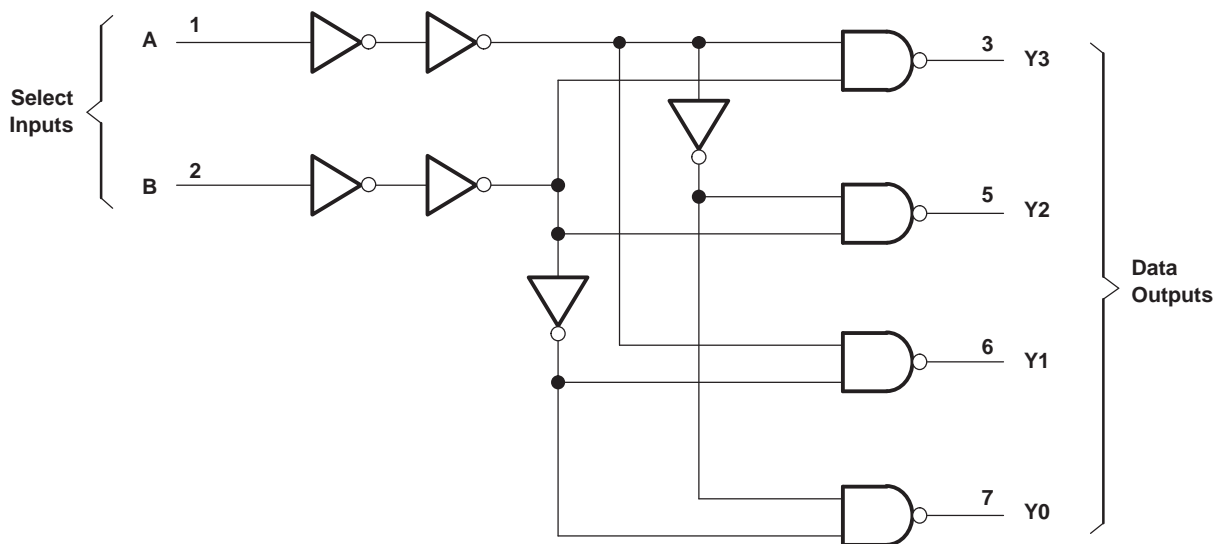
图 6. Voltage Waveforms: Enable and Disable Times, Low- and High-Level Enabling

9 Detailed Description

9.1 Overview

The LVC1G139 device decodes the 2-bit input to one of the four outputs. The B input is the most significant bit and the Y outputs are active low. The propagation delays are very short and well matched (see [Figure 1](#)). Supply voltage from 1.65-V to 5.5-V is supported.

9.2 Functional Block Diagram



9.3 Feature Description

NanoStar and NanoFree package technology is a major breakthrough in device packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.4 Device Functional Modes

[Table 4](#) lists the functional modes of the SN74LVC1G139 device.

表 4. Function Table

INPUTS		OUTPUTS			
B	A	Y ₀	Y ₁	Y ₂	Y ₃
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVC1G139 device is a 2-of-4 decoder and demultiplexer. This device decodes the 2-bit address on inputs A (bit 0) and B (bit 1) then provides a logic low on the matching address output. It can produce 24 mA of drive current at 3.3 V, making it ideal for driving multiple outputs.

10.2 Typical Application

This is an address line decoder using a 16-bit bus example; address bus lines 14 and 15 are decoded and drive four active low chip selects. Each output covers 16K address space mapped by the address bus lines 0 through 13.

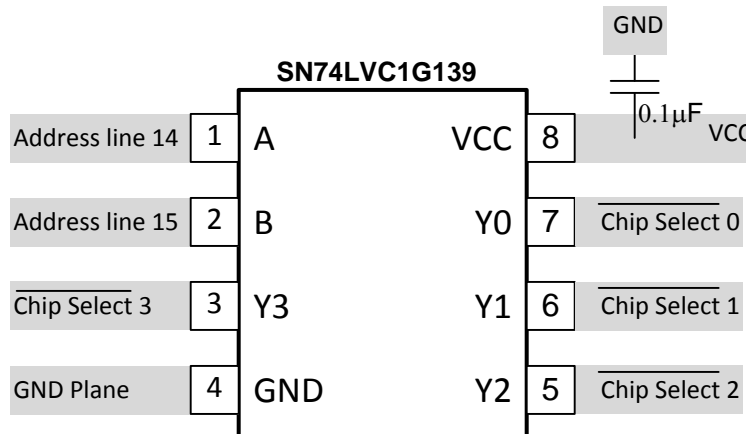


图 7. Typical Application Diagram

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:

- Rise time and fall time specifications ($\Delta t/\Delta V$) are shown in the [Recommended Operating Conditions](#) table.
- Specified high (V_{IH}) and low voltage (V_{IL}) levels are shown in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .

2. Recommend Output Conditions:

- Load currents should not exceed 50 mA per output and 100 mA total for the part.
- Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

Typical Application (continued)

10.2.3 Application Curve

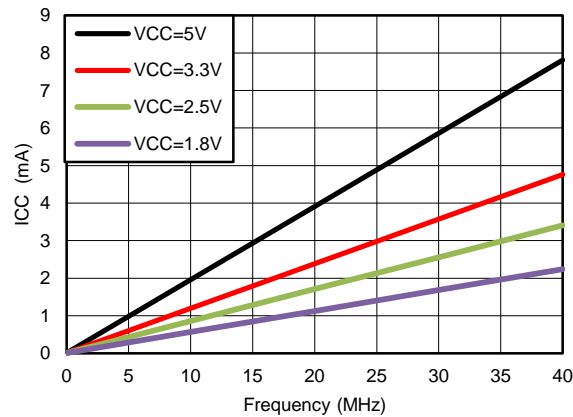


Figure 8. I_{CC} vs Frequency
Load is 15 pF

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple V_{CC} terminals, then 0.01-μF or 0.022-μF capacitors are recommended for each power terminal. Parallel multiple bypass capacitors are allowed to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 9 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

12.2 Layout Example

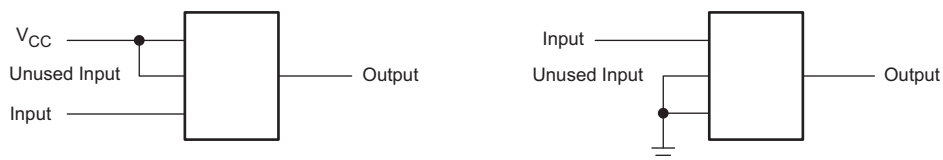


Figure 9. Layout Diagram

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ、『[低速またはフローティングCMOS入力の影響](#)』アプリケーション・レポート

13.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

13.3 商標

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13.4 静電気放電に関する注意事項



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13.5 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G139DCTRE4	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39 (R, Z)	Samples
74LVC1G139DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	Samples
SN74LVC1G139DCTR	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(2WB5, C39) (R, Z)	Samples
SN74LVC1G139DCTT	ACTIVE	SSOP	DCT	8	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(2WB5, C39) (R, Z)	Samples
SN74LVC1G139DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(C39J, C39Q, C39R)	Samples
SN74LVC1G139DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(C39J, C39Q, C39R)	Samples
SN74LVC1G139YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DFN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G139DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G139DCTT	SSOP	DCT	8	250	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G139DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G139DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G139DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC1G139DCTT	SSOP	DCT	8	250	190.0	190.0	30.0
SN74LVC1G139DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1G139DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC1G139DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G139YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCU0008A



PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



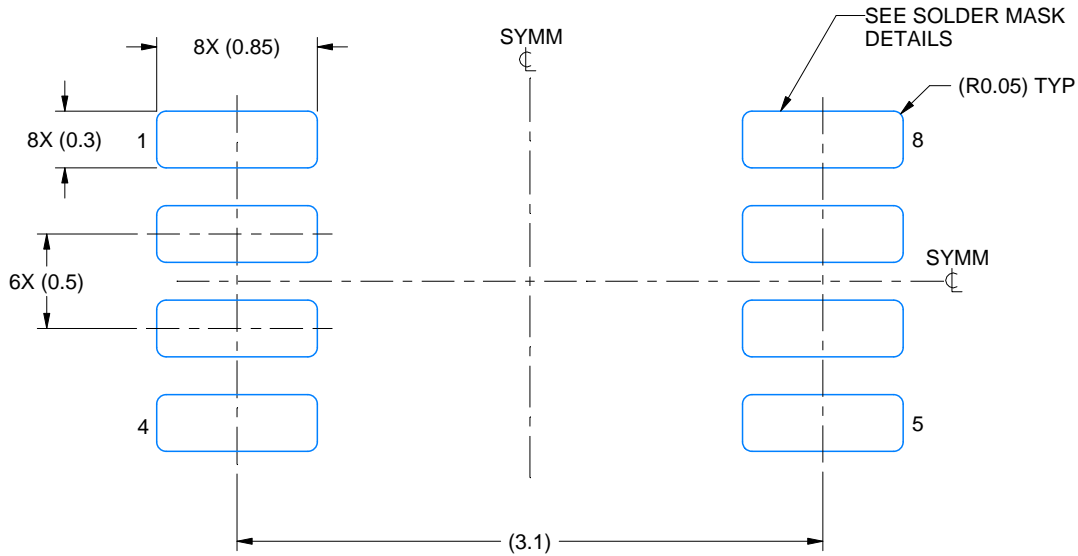
4225266/A 09/2014

EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220784/C 06/2021

NOTES:

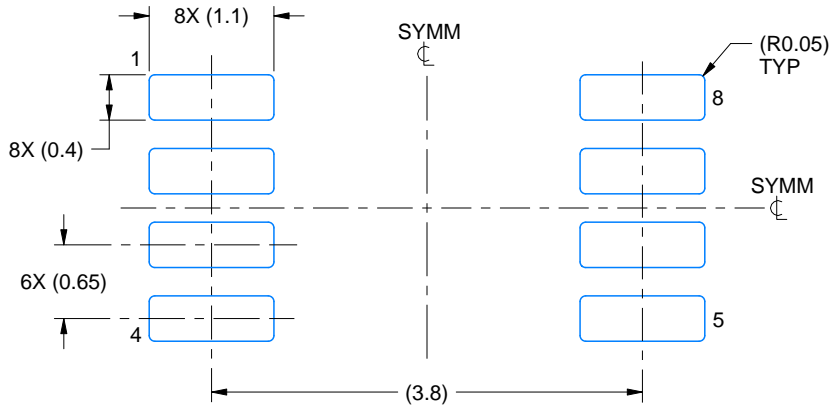
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

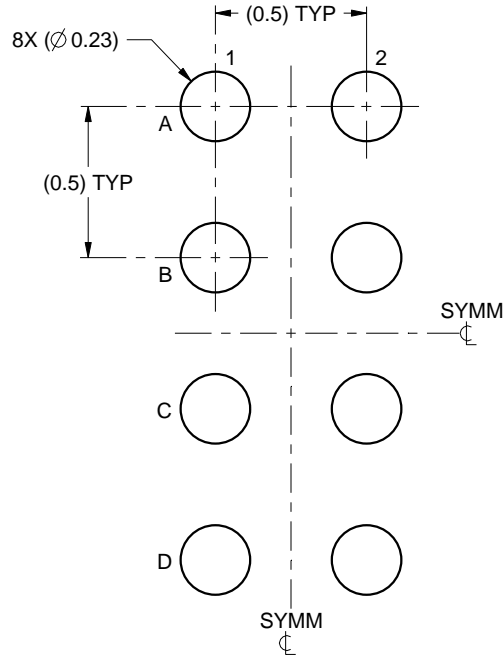
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

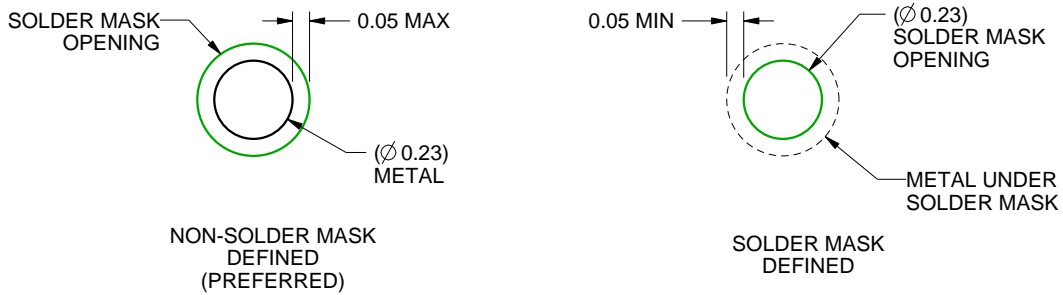
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

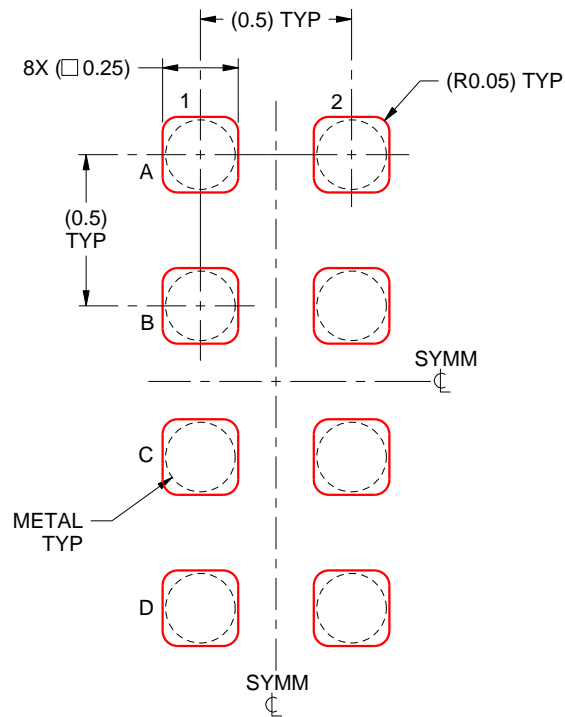
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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