SN74LVC1G80シングル正エッジ・トリガ、Dタイプ・フリップ・フロップ

1 特長

- テキサス・インスツルメンツの NanoFree™パッケージで供給
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- JESD 22を超えるESD保護
  - 2000V、人体モデル(A114-A)
  - 200V、マシン・モデル(A115-A)
  - 1000V、荷電デバイス・モデル(C101)
- 5V V_{CC}動作をサポート
- 5.5Vまでの入力電圧に対応
- V_{CC}への降圧変換をサポート
- 4.2nsの最大t_{pd} (3.3 V)
- 低消費電力、最大I_{CC} 10μA
- 3.3Vにおいて±24mAの出力駆動能力
- I_{off}により部分的パワーダウン・モードおよびバック・ドライブ保護をサポート
- JESD 78, Class II準拠で100mA超のラッチアップ性能

2 アプリケーション

- 試験および測定機器
- エンタープライズ・スイッチング
- 通信インフラ
- 個人用電子機器
- 白物家電

3 概要

SN74LVC1G80デバイスはシングル正エッジ・トリガ、Dタイプ・フリップ・フロップで、1.65V～5.5VのV_{CC}で動作するよう設計されています。

データ(D)入力のデータがセットアップ時間の要件と合致すると、クロック・パルスが正に変化するエッジで、データが$\overline{Q}$出力へ転送されます。クロックのトリガは電圧レベルで発生し、クロック・パルスの立ち上がり時間とは直接関係しません。ホールド時間のインターバルの後で、出力のレベルに影響を及ぼすことなく、D入力のデータを変化させることができます。

NanoFree™パッケージ技術はICパッケージの概念における主要なブレークスルーであり、ダイをパッケージとして使用します。

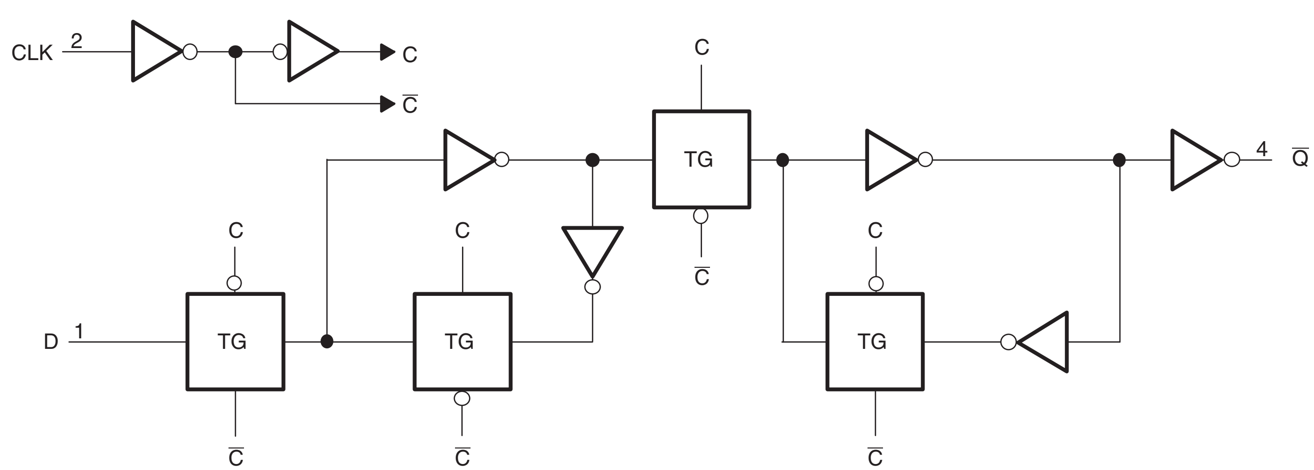
このデバイスは、I_{off}を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off}回路は、デバイスの電源がオフになったとき、出力をディセーブルします。これによってデバイスへの電流の逆流が抑止され、デバイスが損傷から保護されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
SN74LVC1G80DBV	SOT-23 (5)	2.90mm×1.60mm
SN74LVC1G80DCK	SC70 (5)	2.00mm×1.25mm
SN74LVC1G80YZP	DSBGA (5)	1.41mm×0.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ロジック図 (正論理)



(1) TG - 伝送ゲート

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision R (December 2013) から **Revision S** に変更 **Page**

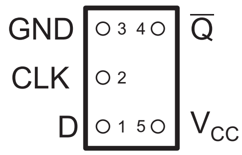
- 「*アプリケーション*」セクション、「*製品情報*」表、「*ESD定格*」表、「*熱に関する情報*」表、「*代表的特性*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Added max junction temperature to the *Recommended Operating Conditions* table ... 5
- Added operating free-air temperature for YZP package to the *Recommended Operating Conditions* table ... 5
- Changed $R_{\theta JA}$ value for DBV package from: 206°C/W to: 243.4°C/W ... 5
- Changed $R_{\theta JA}$ value for DCK package from: 252°C/W to: 278.9°C/W ... 5
- Changed $R_{\theta JA}$ value for YZP package from: 132°C/W to: 136.9°C/W ... 5

Revision Q (January 2007) から **Revision R** に変更 **Page**

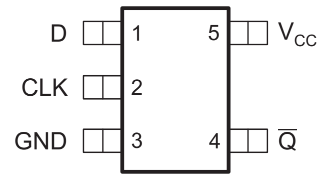
- ドキュメントを新しいTIデータシートのフォーマットに更新 ... 1
- 「*注文情報*」表を削除 ... 1
- 「特長」のI_{off}*を更新* ... 1
- Updated operating temperature range. ... 4
- ESDの警告を追加 ... 17

5 Pin Configuration and Functions

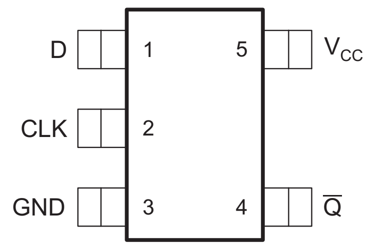
YZP Package
5-Pin DSBGA
Bottom View



DCK Package
5-Pin SC70
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions(1)

PIN		I/O	DESCRIPTION
NO.	NAME		
1	D	I	Data input
2	CLK	I	Positive-Edge-Triggered Clock input
3	GND	—	Ground pin
4	$\overline{Q}$	O	Inverted output
5	V_{CC}	—	Positive Supply

(1) See *メカニカル、パッケージ、および注文情報* for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_J	Junction temperature			150	°C
T_A	Operating free-air temperature	DBV and DCK packages	–40	125	°C
		YZP package	–40	85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G80			UNIT
		DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.4	278.9	136.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	179	121.3	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.6	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	58.4	7.5	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77	64.9	32.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.9			
		I_{OH} = –16 mA		3 V	2.4			
		I_{OH} = –24 mA			2.3			
		I_{OH} = –32 mA		4.5 V	3.8			
V_{OL}		I_{OL} = 100 µA		1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.3	
		I_{OL} = 16 mA		3 V			0.4	
		I_{OL} = 24 mA					0.55	
		I_{OL} = 32 mA		4.5 V			0.55	
I_I	CLK or D inputs	V_I = 5.5 V or GND		0 to 5.5 V			±10	µA
I_{off}		V_I or V_O = 5.5 V		0			±10	µA
I_{CC}		V_I = 5.5 V or GND,	I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 5.5 V			500	µA
C_i		V_I = V_{CC} or GND	T_A = –40°C to 85°C	3.3 V		3.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements: T_A = –40°C to +85°C

over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see Figure 3)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8 V ± 0.15 V		160	MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8 V ± 0.15 V	2.5		ns
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8 V ± 0.15 V	2.3		ns
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
		Data low	V_{CC} = 1.8 V ± 0.15 V	2.5		
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8 V ± 0.15 V	0		ns
			V_{CC} = 2.5 V ± 0.2 V	0.2		
			V_{CC} = 3.3 V ± 0.3 V	0.9		
			V_{CC} = 5.5 V ± 0.5 V	0.4		

6.7 Timing Requirements: T_A = –40°C to +125°C

over recommended operating free-air temperature range, T_A = –40°C to +125°C (unless otherwise noted) (see Figure 3)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8 V ± 0.15 V		160	MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8 V ± 0.15 V	2.5		ns
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8 V ± 0.15 V	2.3		ns
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
		Data low	V_{CC} = 1.8 V ± 0.15 V	2.5		
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8 V ± 0.15 V	0		ns
			V_{CC} = 2.5 V ± 0.2 V	0.2		
			V_{CC} = 3.3 V ± 0.3 V	0.9		
			V_{CC} = 5.5 V ± 0.5 V	0.4		

6.8 Switching Characteristics: T_A = –40°C to +85°C, C_L = 15 pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 15 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	3	9.1	ns
			V_{CC} = 2.5 V ± 0.2 V	1.5	6	
			V_{CC} = 3.3 V ± 0.3 V	1.3	4.2	
			V_{CC} = 5 V ± 0.5 V	1.1	3.8	

6.9 Switching Characteristics: T_A = –40°C to +85°C, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	4.4	9.9	ns
			V_{CC} = 2.5 V ± 0.2 V	2.3	7	
			V_{CC} = 3.3 V ± 0.3 V	2	5.2	
			V_{CC} = 5 V ± 0.5 V	1.3	4.5	

6.10 Switching Characteristics: T_A = –40°C to +125°C, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, T_A = –40°C to +125°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	4.4	12.5	ns
			V_{CC} = 2.5 V ± 0.2 V	2.3	8.5	
			V_{CC} = 3.3 V ± 0.3 V	2	6	
			V_{CC} = 5 V ± 0.5 V	1.3	5.5	

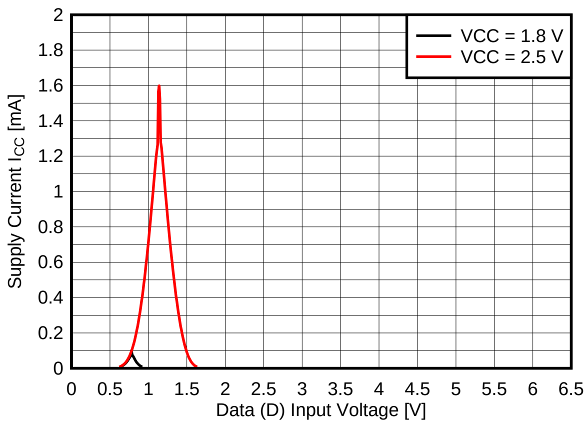
6.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	V_{CC} = 1.8 V	24	pF
			V_{CC} = 2.5 V	24	
			V_{CC} = 3.3 V	25	
			V_{CC} = 5 V	27	

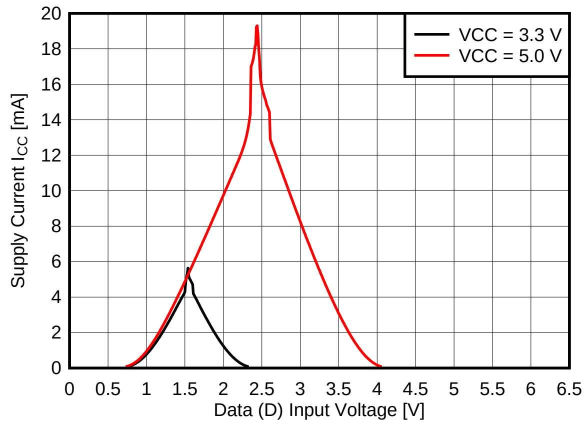
6.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0 V to 6.5 V.



VCC = 1.8 V VCC = 2.5 V

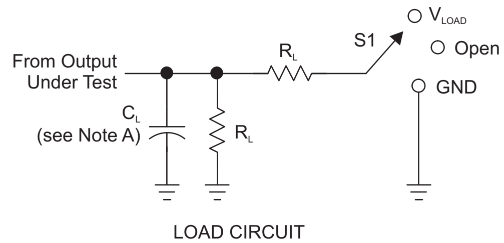
Figure 1. Supply Current (I_{CC}) vs Data (D) Input Voltage



VCC = 3.3 V VCC = 5 V

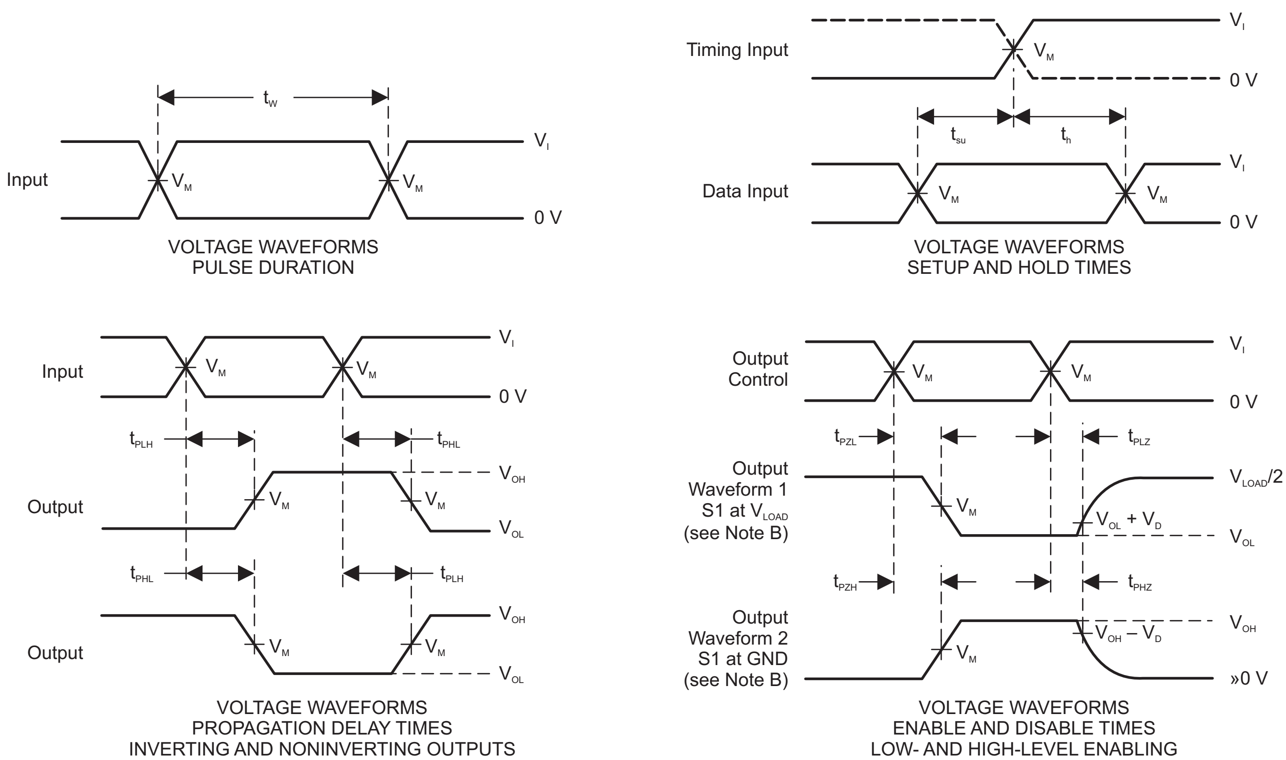
Figure 2. Supply Current (I_{CC}) vs Data (D) Input Voltage

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

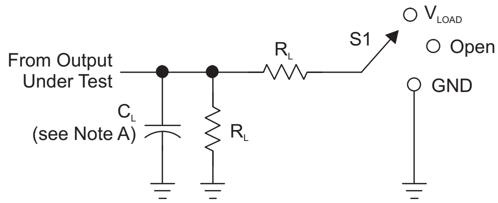
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.15 V
2.5 V ± 0.2 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.15 V
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	15 pF	1 MW	0.3 V
5 V ± 0.5 V	V_{CC}	£2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.3 V



NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, Z_O = 50 W.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

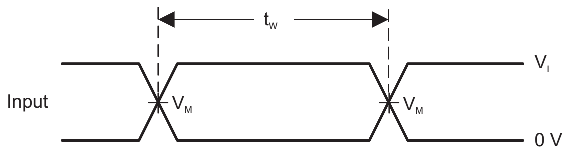
Parameter Measurement Information (continued)



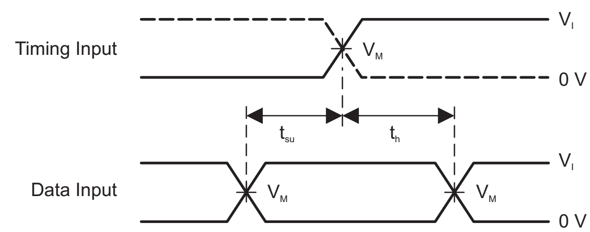
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

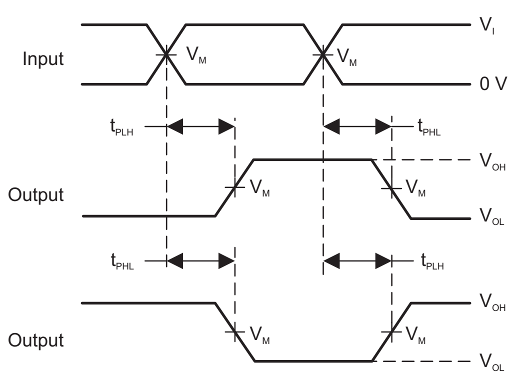
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kW	0.15 V
2.5 V ± 0.2 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 W	0.15 V
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
5 V ± 0.5 V	V_{CC}	£2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 W	0.3 V



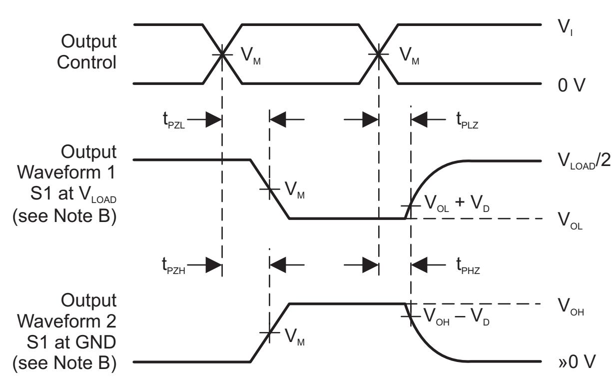
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, Z_O = 50 W.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G80 is a single positive-edge-trigger D-type flip-flop . Data at the input (D) is transferred to the output ($\overline{Q}$) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

8.2 Functional Block Diagram

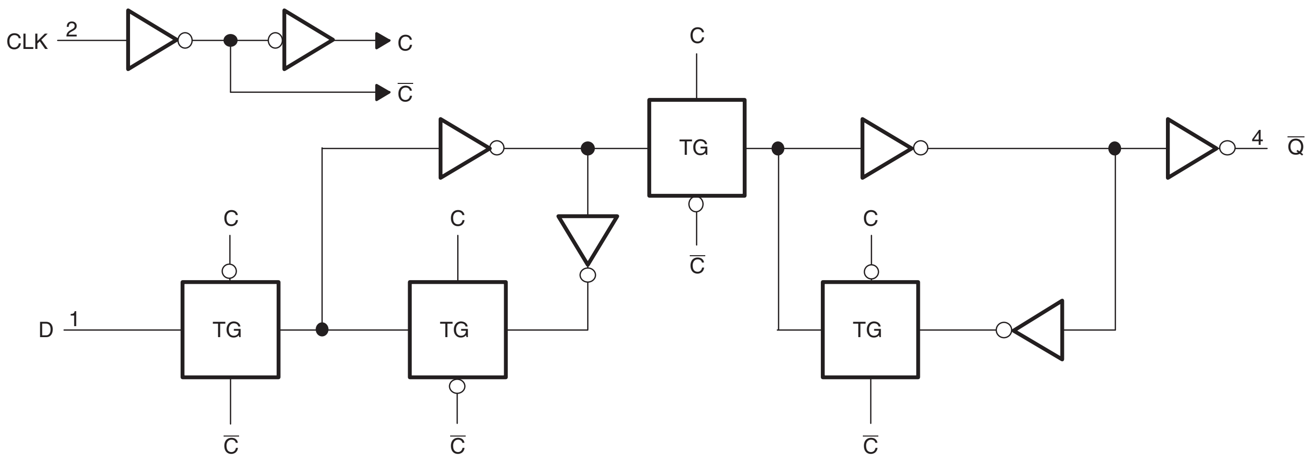


Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Recommended Operating Conditions*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

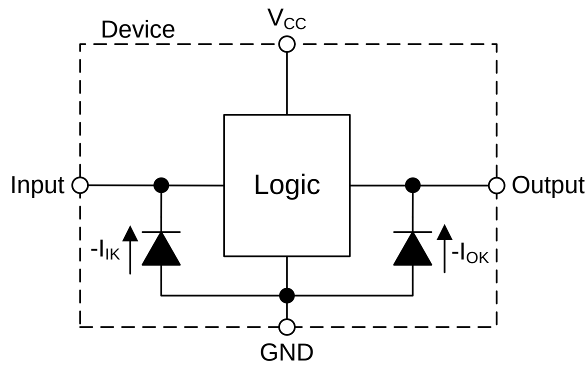


Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings* .

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G80.

Table 1. Function Table

INPUTS		OUTPUT
CLK	D	$\overline{Q}$
↑	H	L
↑	L	H
L	X	Q_0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A useful application for the SN74LVC1G80 is using it as a frequency divider. By feeding back the output ($\overline{Q}$) to the input (D), the output will toggle on every rising edge of the clock waveform. The output goes HIGH once every two clock cycles so essentially the frequency of the clock signal is divided by a factor of two. The SN74LVC1G80 does not have preset or clear functions so the initial state of the output is unknown. This application implements the use of a microcontroller GPIO pin to initially set the input HIGH, so the output LOW. Initialization is not needed, but should be kept in mind. Post initialization, the GPIO pin is set to a high impedance mode. Depending on the microcontroller, the GPIO pin could be set to an input and used to monitor the clock division.

9.2 Typical Application

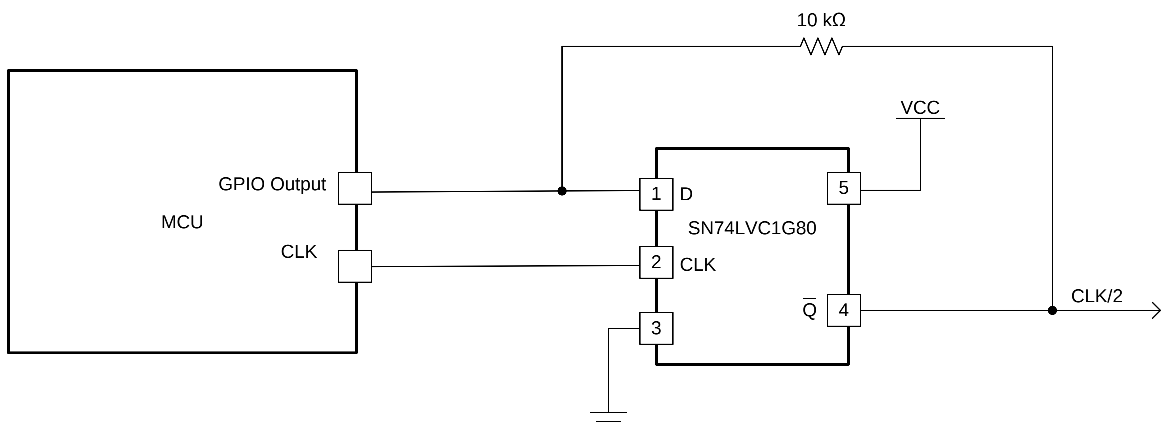


Figure 7. Clock Frequency Division

9.2.1 Design Requirements

For this application, a resistor needs to be placed on the feedback line in order for the initialization voltage from the microcontroller to overpower the signal coming from the output ($\overline{Q}$). Without it the state at the input would be challenged by the GPIO from the microcontroller and from the output of the SN74LVC1G80.

The SN74LVC1G80 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   – For rise time and fall time specifications, see Δt/Δv in *Recommended Operating Conditions*.
   – For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   – Input voltages are recommended to not go below 0 V and not exceed 5.5 V for any V_{CC}. See *Recommended Operating Conditions*.
2. Recommended output conditions:
   – Load currents should not exceed ±50 mA. See *Absolute Maximum Ratings* .
   – Output voltages are recommended to not go below 0 V and not exceed the V_{CC} voltage. See *Recommended Operating Conditions*.
3. Feedback resistor:
   – A 10-kΩ resistor is chosen here to bias the input so the microcontroller GPIO output can initialize the input and output. The resistor value is important because a resistance too high, say at 1 MΩ, would cause too much of a voltage drop, causing the output to no longer be able to drive the input. On the other hand, a resistor too low, such as a 1 Ω, would not bias enough and might cause current to flow into the microcontroller, possibly damaging the device.

9.2.3 Application Curve

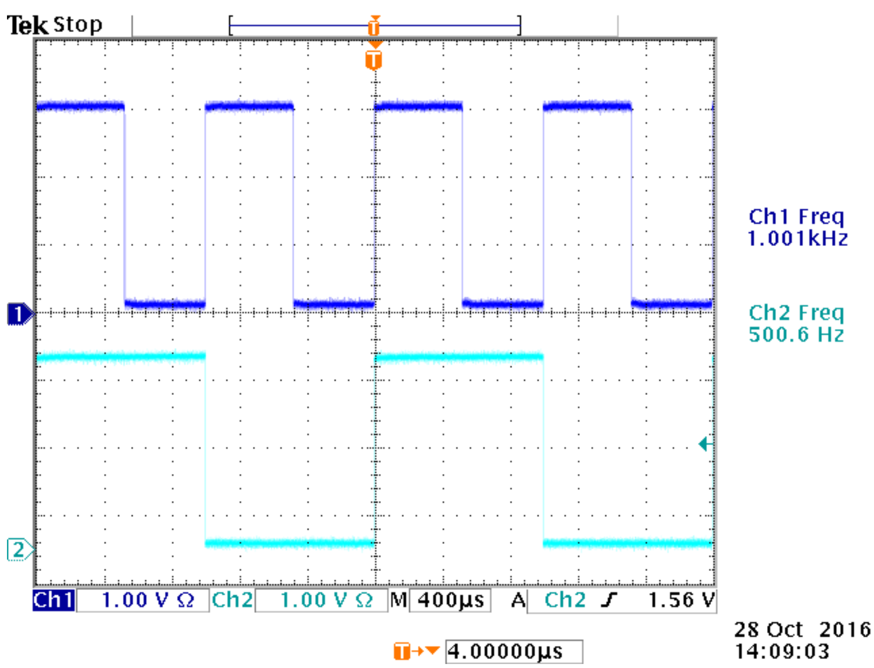


Figure 8. Frequency Division

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in *Recommended Operating Conditions*. A 0.1-µF bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

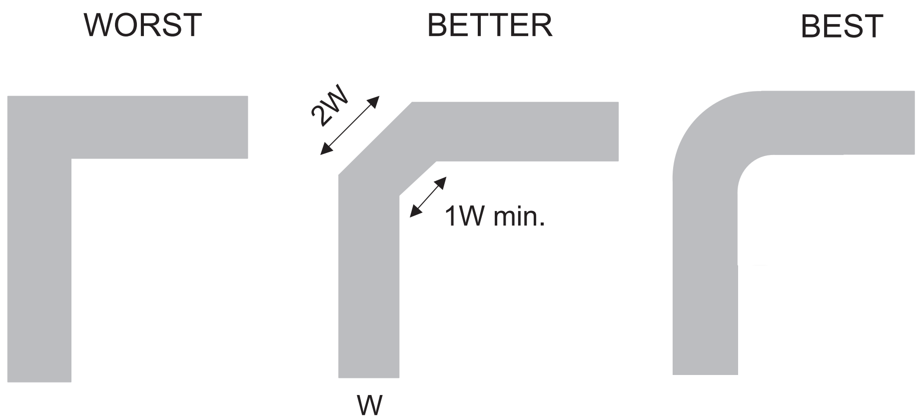


Figure 9. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『低速またはフローティングCMOS入力の影響』、SCBA004

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

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12.5 静電気放電に関する注意事項

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G80DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)	Samples
SN74LVC1G80DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F	Samples
SN74LVC1G80DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F	Samples
SN74LVC1G80DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)	Samples
SN74LVC1G80DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F	Samples
SN74LVC1G80DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CX K, CXR)	Samples
SN74LVC1G80DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX5	Samples
SN74LVC1G80DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CX K, CXR)	Samples
SN74LVC1G80YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CX7, CXN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G80 :

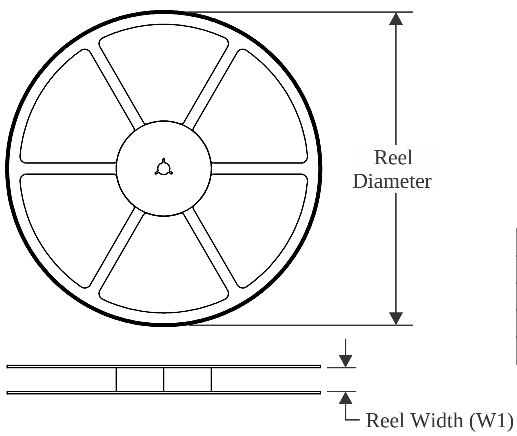
- Automotive : SN74LVC1G80-Q1

NOTE: Qualified Version Definitions:

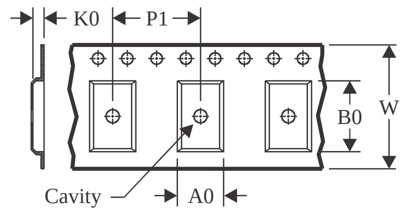
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

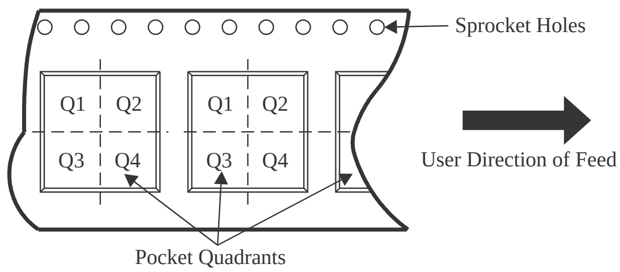


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

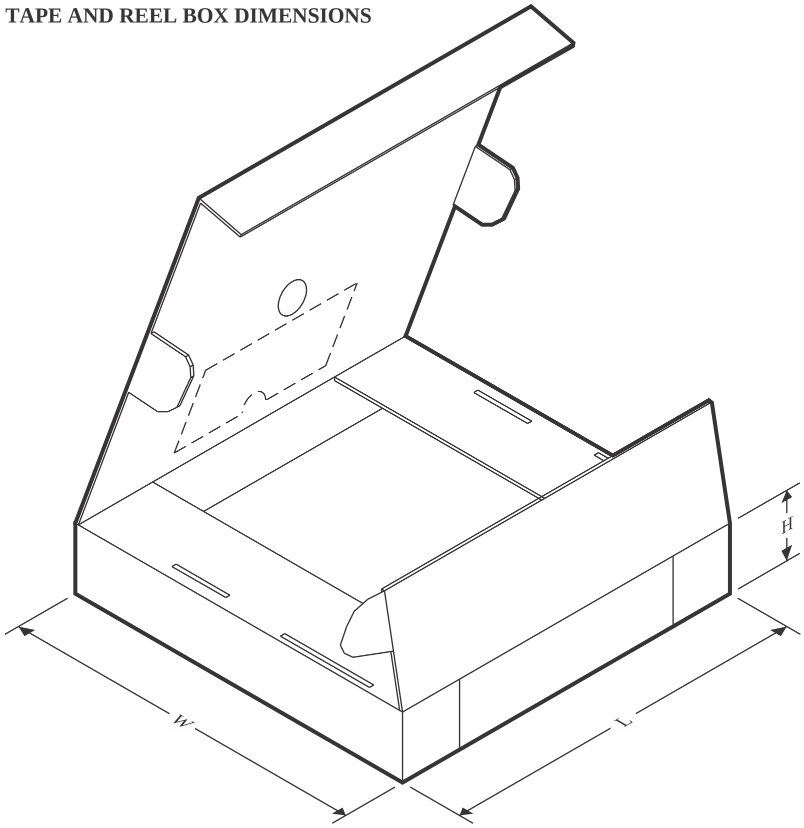
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

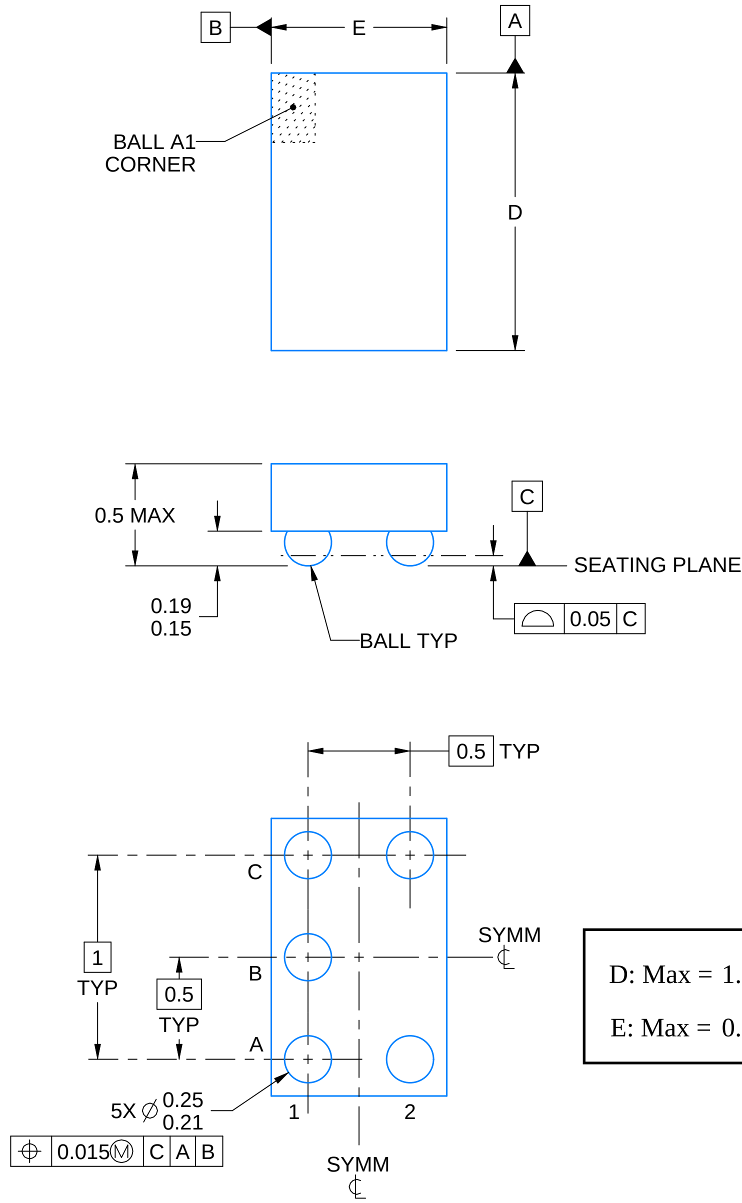
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G80DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G80DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G80DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G80DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0



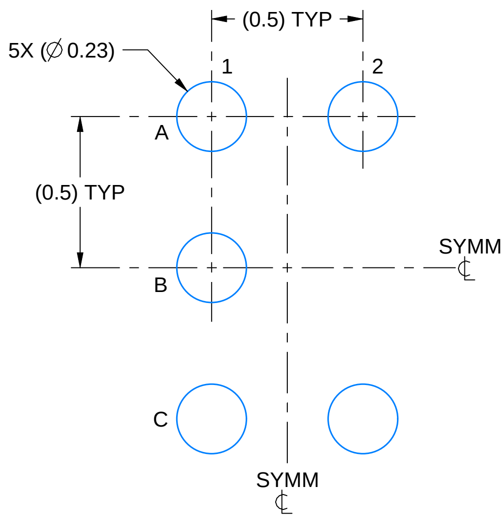
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

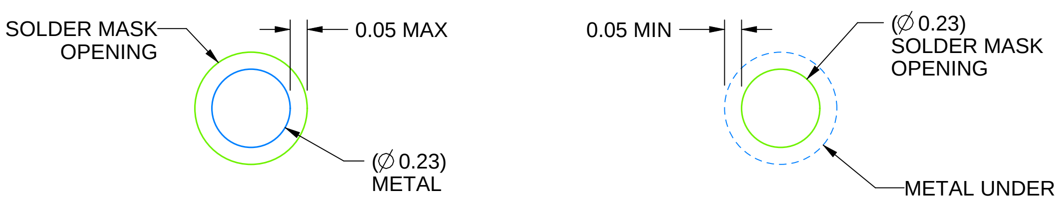
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK DEFINED (PREFERRED)

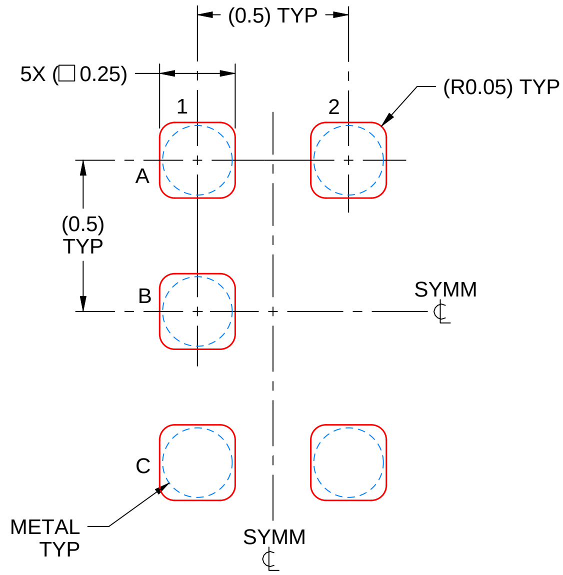
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

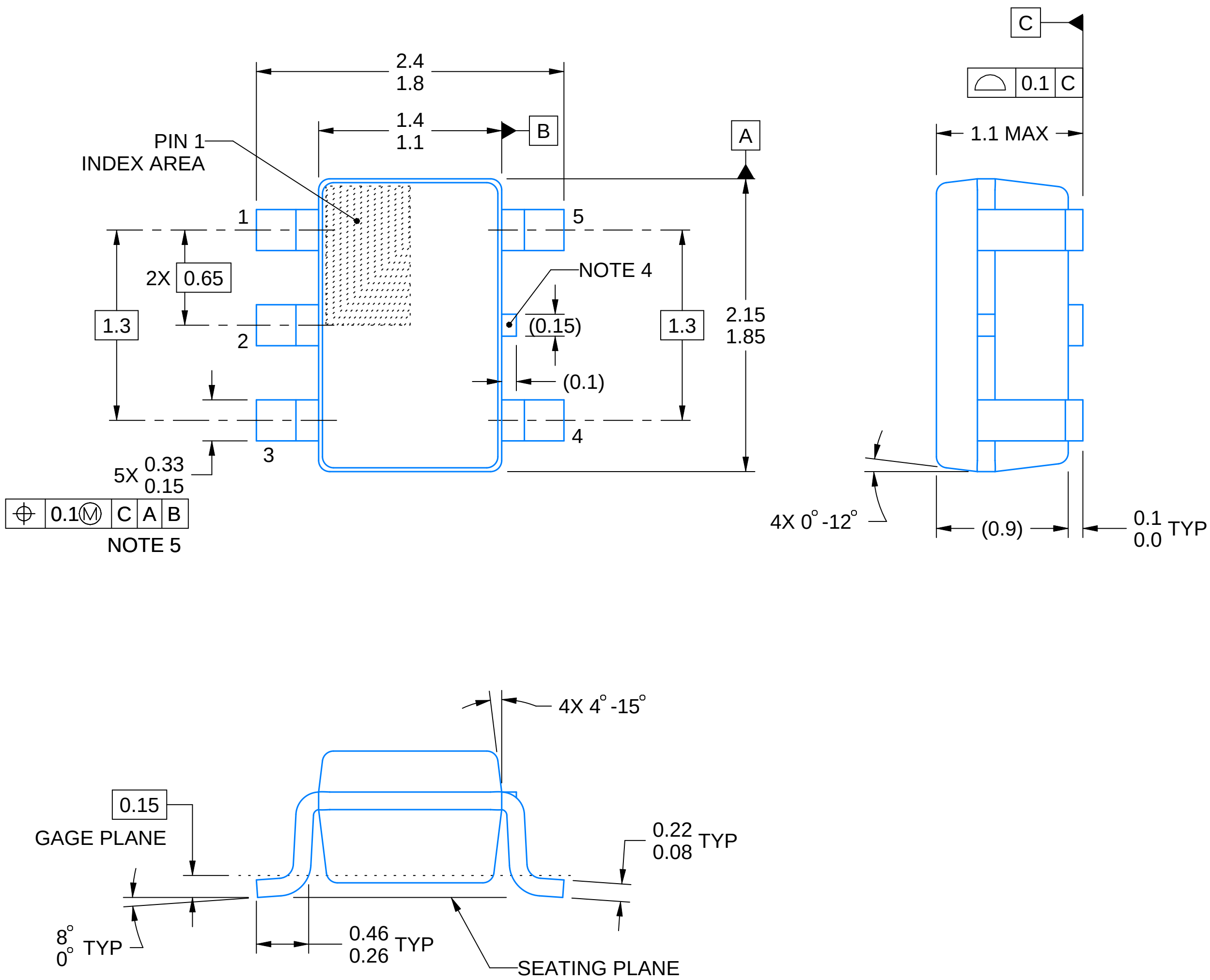


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

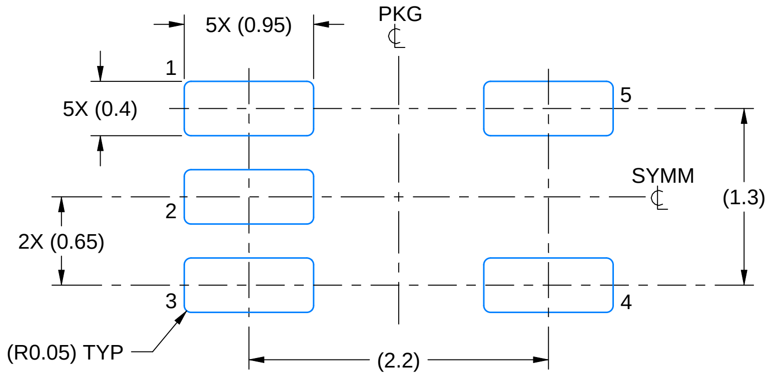
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



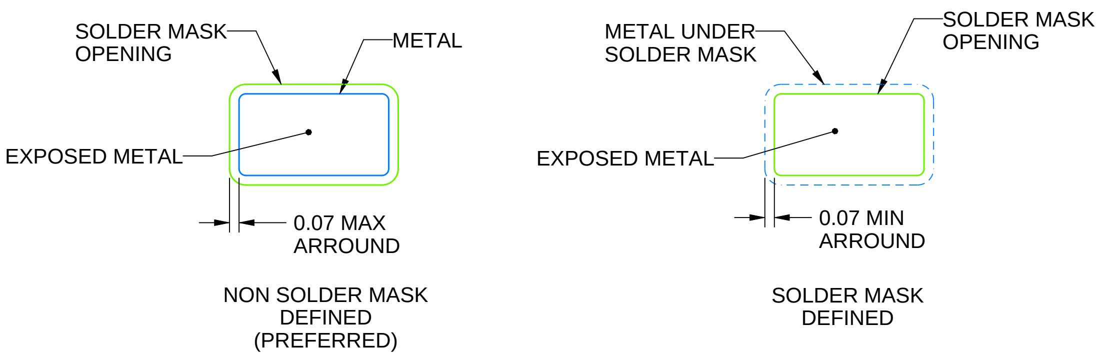
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

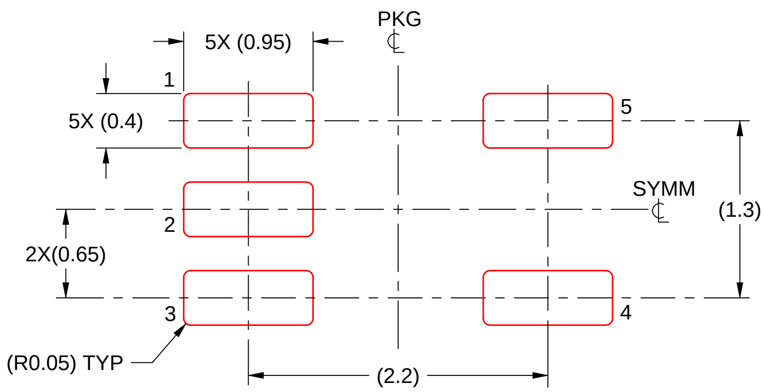


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

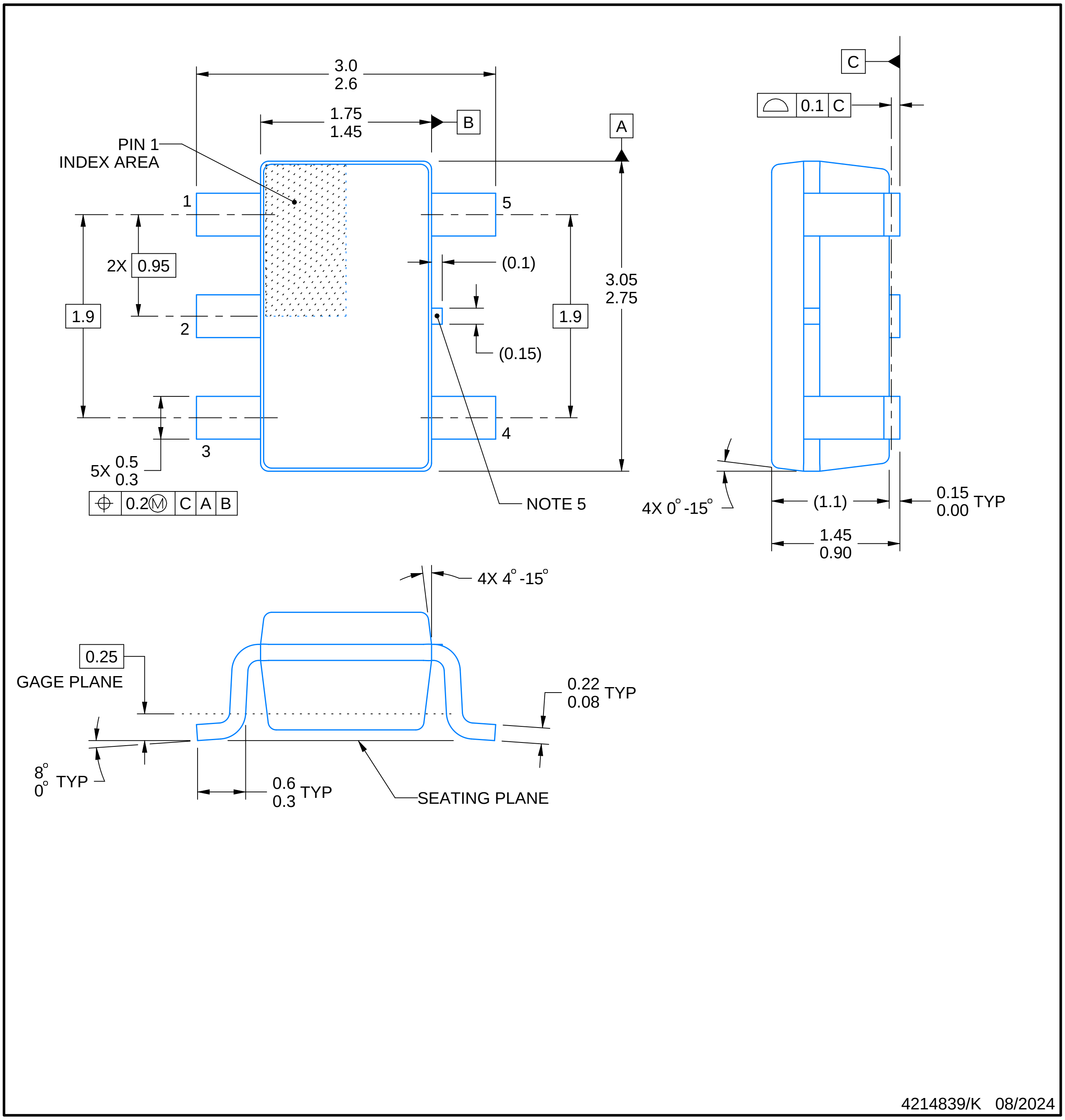


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

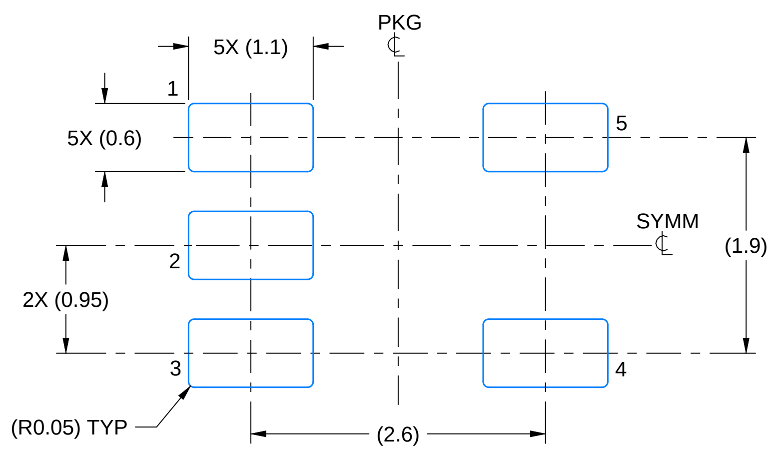
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

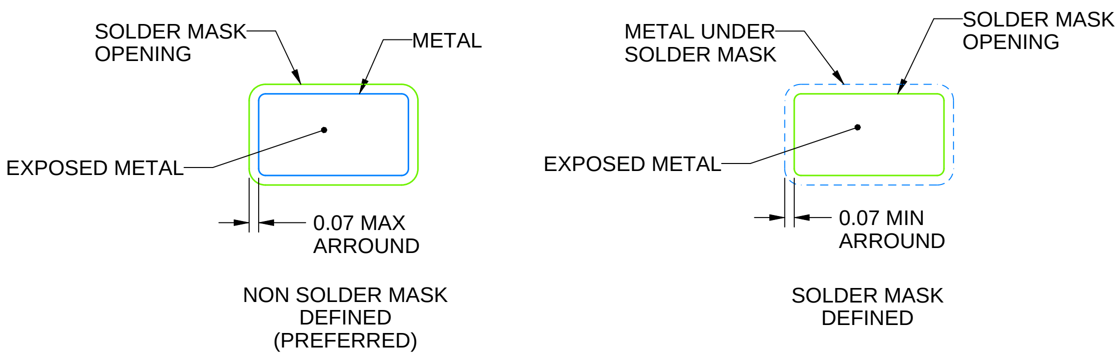


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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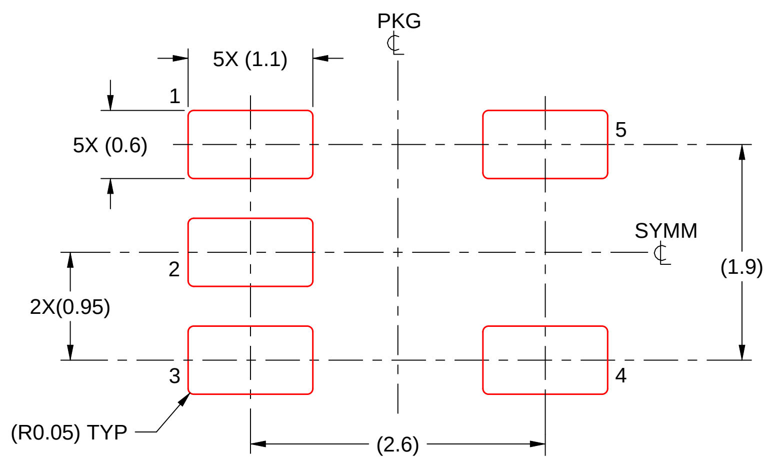
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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