

# SN74LXC1T45 シングル・ビット、デュアル電源バス・トランシーバ、構成可能なレベル・シフト機能付

## 1 特長

- 完全に構成可能なデュアル・レール設計により、各ポートは 1.1V~5.5V で動作可能
- 堅牢でグリッチの発生しない電源シーケンシング
- 3.3V~5.0V で最高 420Mbps をサポート
- シュミット・トリガ入力により低速またはノイズの多い入力に対応
- ダイナミック・プルダウン抵抗を内蔵した I/O により、外付け部品数の削減が可能
- スタティック・プルダウン抵抗を内蔵した制御入力により、制御入力のフローティングが可能
- 高い駆動強度 (5V で最大 32mA)
- 低い消費電力
  - 最大 3 $\mu$ A (25°C)
  - 最大 6 $\mu$ A (-40°C~125°C)
- V<sub>CC</sub> 絶縁および V<sub>CC</sub> 切断 (I<sub>off-float</sub>) 機能
  - どちらかの V<sub>CC</sub> 電源が 100mV 未満になった場合または切断された場合、すべての I/O がプルダウンされた後に高インピーダンス状態に移行
- I<sub>off</sub> により部分的パワーダウン・モードでの動作をサポート
- LVC ファミリのレベル・シフトと互換
- 制御ロジック (DIR および  $\overline{OE}$ ) は V<sub>CCA</sub> 基準
- 動作温度範囲: -40°C~+125°C
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 人体モデル 4000V
  - デバイス帯電モデル 1000V

## 2 アプリケーション

- 低速またはノイズの多い入力信号の除去
- インジケータ LED または ブザーの駆動
- メカニカルスイッチのデバウンス
- 汎用 I/O レベル・シフト

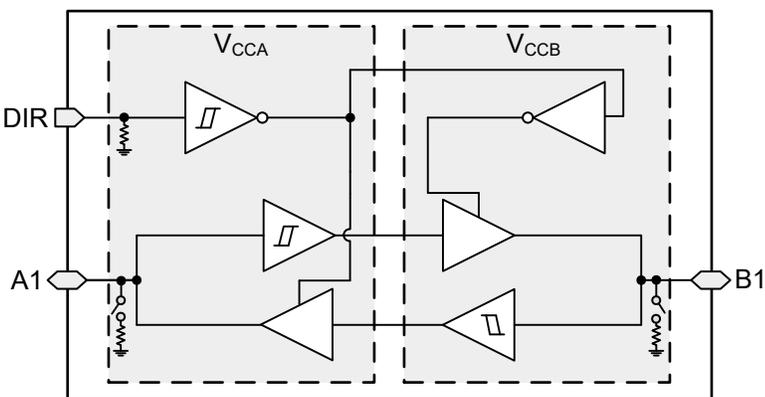
## 3 概要

SN74LXC1T45 は、1 ビット、デュアル電源、非反転双方向電圧レベル変換デバイスです。I/O ピン A および制御ピン (DIR) は V<sub>CCA</sub> のロジック・レベルを基準とし、I/O ピン B は V<sub>CCB</sub> ロジック・レベルを基準とします。A ポートは 1.1V~5.5V の範囲の I/O 電圧を受け入れ、B ポートは 1.1V~5.5V の I/O 電圧を受け入れます。DIR が HIGH のときは A から B へ、DIR が LOW のときは B から A へデータが転送されます。制御ロジックの概要については [デバイス機能モード](#) を参照してください。

### 製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN74LXC1T45DRL	SOT (6)	1.60mm × 1.20mm
SN74LXC1T45DRY	SON (6)	1.45mm × 1.00mm
SN74LXC1T45DBV	SOT-23 (6)	2.90mm × 1.60mm
SN74LXC1T45DCK	SC70 (6)	2.00mm × 1.25mm
SN74LXC1T45DTQ	X2SON (6)	1.00mm × 0.80mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



SN74LXC1T45 のブロック図

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2021) to Revision A (December 2021)	Page
• データシートのステータスを事前情報から量産データに変更.....	1

## 5 Pin Configuration and Functions

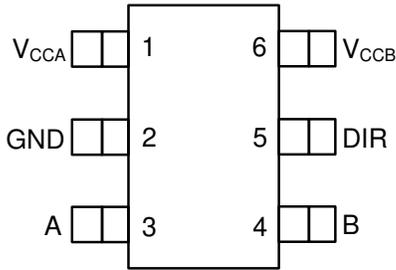


图 5-1. DBV 6-Pin SOT-23  
Top View

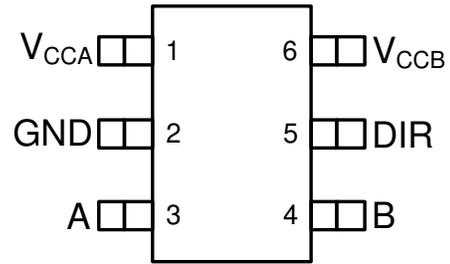


图 5-2. DCK 6-Pin SC70  
Top View

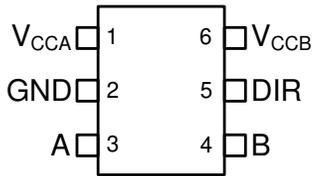


图 5-3. DRL Package Preview 6-Pin SOT  
Top View

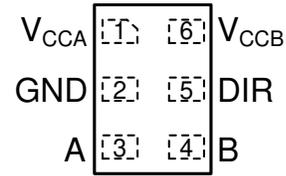


图 5-4. DRY Package Preview 6-Pin SON  
Top View

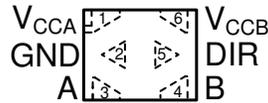


图 5-5. DTQ Package Preview 6-Pin X2SON Transparent Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DBV, DCK, DRL, DRY, DTQ		
A	3	I/O	Input or output A. Referenced to $V_{CCA}$ .
B	4	I/O	Input or output B. Referenced to $V_{CCB}$ .
DIR	5	I	Direction-control signal for all ports. Referenced to $V_{CCA}$ .
GND	2	—	Ground.
DIR	5	I	Direction-control signal for all ports. Referenced to $V_{CCA}$ .
$V_{CCA}$	1	—	A-port supply voltage. $1.1\text{ V} \leq V_{CCA} \leq 5.5\text{ V}$ .
$V_{CCB}$	6	—	B-port supply voltage. $1.1\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$ .

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage A		-0.5	6.5	V
V <sub>CCB</sub>	Supply voltage B		-0.5	6.5	V
V <sub>I</sub>	Input Voltage <sup>(2)</sup>	I/O Ports (A Port)	-0.5	6.5	V
		I/O Ports (B Port)	-0.5	6.5	
		Control Inputs	-0.5	6.5	
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A Port	-0.5	6.5	V
		B Port	-0.5	6.5	
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2) (3)</sup>	A Port	-0.5	V <sub>CCA</sub> + 0.5	V
		B Port	-0.5	V <sub>CCB</sub> + 0.5	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50		mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50		mA
I <sub>O</sub>	Continuous output current		-50	50	mA
	Continuous current through V <sub>CC</sub> or GND		-200	200	
T <sub>j</sub>	Junction Temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, this device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

		MIN	MAX	UNIT	
V <sub>CCA</sub>	Supply voltage A	1.1	5.5	V	
V <sub>CCB</sub>	Supply voltage B	1.1	5.5	V	
I <sub>OH</sub>	High-level output current	V <sub>CCO</sub> = 1.1 V	-0.1	mA	
		V <sub>CCO</sub> = 1.4 V	-4		
		V <sub>CCO</sub> = 1.65 V	-8		
		V <sub>CCO</sub> = 2.3 V	-12		
		V <sub>CCO</sub> = 3 V	-24		
		V <sub>CCO</sub> = 4.5 V	-32		
I <sub>OL</sub>	Low-level output current	V <sub>CCO</sub> = 1.1 V	0.1	mA	
		V <sub>CCO</sub> = 1.4 V	4		
		V <sub>CCO</sub> = 1.65 V	8		
		V <sub>CCO</sub> = 2.3 V	12		
		V <sub>CCO</sub> = 3 V	24		
		V <sub>CCO</sub> = 4.5 V	32		
V <sub>I</sub>	Input voltage <sup>(3)</sup>	0	5.5	V	
V <sub>O</sub>	Output voltage	Active State	0	V <sub>CCO</sub>	V
		Tri-State	0	5.5	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I<sub>I</sub> specification indicated under the [Electrical Characteristics](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LXC1T45					UNIT	
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTQ (X2SON)		
	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	217.4	216.1	TBD	TBD	TBD	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	136.0	143.6	TBD	TBD	TBD	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	98.5	75.9	TBD	TBD	TBD	°C/W
Y <sub>JT</sub>	Junction-to-top characterization parameter	75.8	58.5	TBD	TBD	TBD	°C/W
Y <sub>JB</sub>	Junction-to-board characterization parameter	98.2	75.6	TBD	TBD	TBD	°C/W
R <sub>θJC(bottom)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	Operating free-air temperature (T <sub>A</sub> )						UNIT	
				25°C			–40°C to 85°C		–40°C to 125°C		
				MIN	TYP	MAX	MIN	TYP	MAX		MIN
V <sub>T+</sub>	Positive-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V <sub>CCI</sub> )	1.1 V	1.1 V		0.44	0.88	0.44	0.88	V	
			1.4 V	1.4 V		0.60	0.98	0.60	0.98		
			1.65 V	1.65 V		0.76	1.13	0.76	1.13		
			2.3 V	2.3 V		1.08	1.56	1.08	1.56		
			3 V	3 V		1.48	1.92	1.48	1.92		
			4.5 V	4.5 V		2.19	2.74	2.19	2.74		
			5.5 V	5.5 V		2.65	3.33	2.65	3.33		
		Control Input (DIR) (Referenced to V <sub>CCA</sub> )	1.1 V	1.1 V		0.44	0.88	0.44	0.88	V	
			1.4 V	1.4 V		0.60	0.98	0.60	0.98		
			1.65 V	1.65 V		0.76	1.13	0.76	1.13		
			2.3 V	2.3 V		1.08	1.56	1.08	1.56		
			3 V	3 V		1.48	1.92	1.48	1.92		
			4.5 V	4.5 V		2.19	2.74	2.19	2.74		
			5.5 V	5.5 V		2.65	3.33	2.65	3.33		
V <sub>T-</sub>	Negative-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V <sub>CCI</sub> )	1.1 V	1.1 V		0.17	0.48	0.17	0.48	V	
			1.4 V	1.4 V		0.28	0.59	0.28	0.59		
			1.65 V	1.65 V		0.35	0.69	0.35	0.69		
			2.3 V	2.3 V		0.56	0.97	0.56	0.97		
			3 V	3 V		0.89	1.5	0.89	1.5		
			4.5 V	4.5 V		1.51	1.97	1.51	1.97		
			5.5 V	5.5 V		1.88	2.4	1.88	2.4		
		Control Input (DIR) (Referenced to V <sub>CCA</sub> )	1.1 V	1.1 V		0.17	0.48	0.17	0.48	V	
			1.4 V	1.4 V		0.28	0.6	0.28	0.6		
			1.65 V	1.65 V		0.35	0.71	0.35	0.71		
			2.3 V	2.3 V		0.56	1	0.56	1		
			3 V	3 V		0.89	1.5	0.89	1.5		
			4.5 V	4.5 V		1.51	2	1.51	2		
			5.5 V	5.5 V		1.88	2.46	1.88	2.46		
ΔV <sub>T</sub>	Input-threshold hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )	Data Inputs (Ax, Bx) (Referenced to V <sub>CCI</sub> )	1.1 V	1.1 V		0.2	0.4	0.2	0.4	V	
			1.4 V	1.4 V		0.25	0.5	0.25	0.5		
			1.65 V	1.65 V		0.3	0.55	0.3	0.55		
			2.3 V	2.3 V		0.38	0.65	0.38	0.65		
			3 V	3 V		0.46	0.72	0.46	0.72		
			4.5 V	4.5 V		0.58	0.93	0.58	0.93		
			5.5 V	5.5 V		0.69	1.06	0.69	1.06		
		Control Input (DIR) (Referenced to V <sub>CCA</sub> )	1.1 V	1.1 V		0.2	0.4	0.2	0.4	V	
			1.4 V	1.4 V		0.25	0.5	0.25	0.5		
			1.65 V	1.65 V		0.3	0.55	0.3	0.55		
			2.3 V	2.3 V		0.38	0.65	0.38	0.65		
			3 V	3 V		0.46	0.72	0.46	0.72		
			4.5 V	4.5 V		0.58	0.93	0.58	0.93		
			5.5 V	5.5 V		0.69	1.06	0.69	1.06		

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT
				25°C			–40°C to 85°C			–40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	High-level output voltage <sup>(3)</sup>	I <sub>OH</sub> = –100 μA	1.1V – 5.5V	1.1V – 5.5V				V <sub>CCO</sub> – 0.1			V		
		I <sub>OH</sub> = –4 mA	1.4 V	1.4 V				1					
		I <sub>OH</sub> = –8 mA	1.65 V	1.65 V				1.2					
		I <sub>OH</sub> = –12 mA	2.3 V	2.3 V				1.9					
		I <sub>OH</sub> = –24 mA	3 V	3 V				2.4					
		I <sub>OH</sub> = –32 mA	4.5 V	4.5 V				3.8					
V <sub>OL</sub>	Low-level output voltage <sup>(4)</sup>	I <sub>OL</sub> = 100 μA	1.1V – 5.5V	1.1V – 5.5V				0.1			V		
		I <sub>OL</sub> = 4 mA	1.4 V	1.4 V				0.3					
		I <sub>OL</sub> = 8 mA	1.65 V	1.65 V				0.45					
		I <sub>OL</sub> = 12 mA	2.3 V	2.3 V				0.3					
		I <sub>OL</sub> = 24 mA	3 V	3 V				0.55					
		I <sub>OL</sub> = 32 mA	4.5 V	4.5 V				0.55					
I <sub>I</sub>	Input leakage current	Control input (DIR) V <sub>I</sub> = V <sub>CCA</sub> or GND	1.1V – 5.5V	1.1V – 5.5V	–0.1	1	–0.1	2	–0.1	2	μA		
		Data Inputs <sup>(5)</sup> (A <sub>x</sub> , B <sub>x</sub> ) V <sub>I</sub> = V <sub>CC1</sub> or GND	1.1V – 5.5V	1.1V – 5.5V	–0.3	1	–1	1	–2	2	μA		
I <sub>off</sub>	Partial power down current	A Port or B Port V <sub>I</sub> or V <sub>O</sub> = 0 V – 5.5 V	0 V	0 V – 5.5 V	–1	1	–2	2	–2.5	2.5	μA		
		0 V – 5.5 V	0 V		–1	1	–2	2	–2.5	2.5			
I <sub>off-float</sub>	Floating supply Partial power down current	A Port or B Port V <sub>I</sub> or V <sub>O</sub> = GND	Floating <sup>(6)</sup>	0 V – 5.5 V	–1.5	1.5	–2	2	–2.5	2.5	μA		
		0 V – 5.5 V	Floating <sup>(6)</sup>		–1.5	1.5	–2	2	–2.5	2.5			
I <sub>CCA</sub>	V <sub>CCA</sub> supply current	V <sub>I</sub> = V <sub>CC1</sub> or GND I <sub>O</sub> = 0	1.1V – 5.5V	1.1V – 5.5V				2			μA		
			0 V	5.5 V	–0.2			–0.5					
		5.5 V	0 V				1						
		V <sub>I</sub> = GND I <sub>O</sub> = 0	5.5 V	Floating <sup>(6)</sup>				1					
I <sub>CCB</sub>	V <sub>CCB</sub> supply current	V <sub>I</sub> = V <sub>CC1</sub> or GND I <sub>O</sub> = 0	1.1V – 5.5V	1.1V – 5.5V				2			μA		
			0 V	5.5 V				1					
		5.5 V	0 V	–0.2			–0.5						
		V <sub>I</sub> = GND I <sub>O</sub> = 0	Floating <sup>(6)</sup>	5.5 V				1					
I <sub>CCA</sub> + I <sub>CCB</sub>	Combined supply current	V <sub>I</sub> = V <sub>CC1</sub> or GND I <sub>O</sub> = 0	1.1V – 5.5V	1.1V – 5.5V				3			μA		
ΔI <sub>CCA</sub>	V <sub>CCA</sub> additional supply current per input	Control input (DIR): V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V A port = V <sub>CCA</sub> or GND B Port = open	3.0V – 5.5V	3.0V – 5.5V				50			μA		
		A Port: V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V DIR = V <sub>CCA</sub> , B Port = open	3.0V – 5.5V	3.0V – 5.5V				50					

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	$V_{CCA}$	$V_{CCB}$	Operating free-air temperature ( $T_A$ )									UNIT
				25°C			-40°C to 85°C			-40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\Delta I_{CCB}$	$V_{CCB}$ additional supply current per input B Port: $V_I = V_{CCB} - 0.6\text{ V}$ DIR = GND, A Port = open	3.0V - 5.5V	3.0V - 5.5V						50			75	$\mu\text{A}$
$C_i$	Control Input Capacitance $V_I = 3.3\text{ V}$ or GND	3.3 V	3.3 V			2.2			5			5	pF
$C_{io}$	Data I/O Capacitance $V_{CCO} = 0\text{ V}$ $V_O = 1.65\text{ V DC} + 1\text{ MHz}$ -16 dBm sine wave	3.3 V	3.3 V			4.3			10.5			10.5	pF

- (1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port
- (2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port
- (3) Tested at  $V_I = V_{T+(MAX)}$
- (4) Tested at  $V_I = V_{T-(MIN)}$
- (5) For I/O ports, the parameter  $I_i$  includes the  $I_{OZ}$  current
- (6) Floating is defined as a node that is both not actively driven by an external device and has leakage not exceeding 10nA

## 6.6 Switching Characteristics, $V_{CCA} = 1.2 \pm 0.1 \text{ V}$

See [Figure 7-1](#) and [Table 7-1](#) for test circuit and loading. See [Figure 7-2](#), [Figure 7-3](#), and [Figure 7-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT						
					$1.2 \pm 0.1 \text{ V}$			$1.5 \pm 0.1 \text{ V}$			$1.8 \pm 0.15 \text{ V}$			$2.5 \pm 0.2 \text{ V}$				$3.3 \pm 0.3 \text{ V}$			$5.0 \pm 0.5 \text{ V}$		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	MIN	TYP	MAX
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	6	85	4	41	3	36	1	33	1	34	1	44	ns						
				-40°C to 125°C	8	55	6	37	5	33	3	30	3	30	2	33							
		B	A	-40°C to 85°C	6	85	5	71	4	67	3	60	3	57	3	58							
				-40°C to 125°C	8	55	6	47	6	43	5	38	4	37	4	36							
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	5	53	5	53	5	53	5	53	5	53	4	53	ns						
				-40°C to 125°C	7	47	7	47	7	47	7	47	7	47	7	47							
		DIR	B	-40°C to 85°C	10	85	7	47	6	41	5	34	5	33	4	32							
				-40°C to 125°C	14	71	11	48	10	41	8	34	8	33	6	32							
$t_{en}$	Enable time	DIR	A	-40°C to 85°C	21	150	17	110	16	99	13	86	13	83	12	85	ns						
				-40°C to 125°C	27	121	23	89	21	80	17	68	17	65	15	63							
		DIR	B	-40°C to 85°C	16	118	14	89	13	84	12	81	11	82	11	92							
				-40°C to 125°C	19	97	18	79	17	73	16	68	15	67	14	70							

## 6.7 Switching Characteristics, $V_{CCA} = 1.5 \pm 0.1 \text{ V}$

See [Figure 7-1](#) and [Table 7-1](#) for test circuit and loading. See [Figure 7-2](#), [Figure 7-3](#), and [Figure 7-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT						
					$1.2 \pm 0.1 \text{ V}$			$1.5 \pm 0.1 \text{ V}$			$1.8 \pm 0.15 \text{ V}$			$2.5 \pm 0.2 \text{ V}$				$3.3 \pm 0.3 \text{ V}$			$5.0 \pm 0.5 \text{ V}$		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	MIN	TYP	MAX
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	5	71	3	29	1	24	1	20	1	19	1	19	ns						
				-40°C to 125°C	6	47	4	30	3	25	2	21	2	20	1	20							
		B	A	-40°C to 85°C	4	41	3	29	2	27	1	23	1	22	1	21							
				-40°C to 125°C	6	37	4	30	4	27	3	24	3	22	2	22							
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	2	26	2	26	2	26	2	26	2	26	2	26	ns						
				-40°C to 125°C	4	27	4	27	4	27	4	27	4	27	4	27							
		DIR	B	-40°C to 85°C	8	71	6	38	5	32	3	25	3	24	2	22							
				-40°C to 125°C	12	61	10	39	9	34	6	26	6	25	4	23							
$t_{en}$	Enable time	DIR	A	-40°C to 85°C	17	106	13	63	12	54	9	44	9	41	8	39	ns						
				-40°C to 125°C	23	92	19	64	17	56	14	45	14	42	12	40							
		DIR	B	-40°C to 85°C	12	90	10	51	9	45	8	40	7	39	7	39							
				-40°C to 125°C	16	69	14	51	13	47	12	42	11	40	10	40							

## 6.8 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15 \text{ V}$

See [Figure 7-1](#) and [Table 7-1](#) for test circuit and loading. See [Figure 7-2](#), [Figure 7-3](#), and [Figure 7-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT						
					$1.2 \pm 0.1 \text{ V}$			$1.5 \pm 0.1 \text{ V}$			$1.8 \pm 0.15 \text{ V}$			$2.5 \pm 0.2 \text{ V}$				$3.3 \pm 0.3 \text{ V}$			$5.0 \pm 0.5 \text{ V}$		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	MIN	TYP	MAX
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	4	67	2	27	1	22	1	18	1	16	1	16	ns						
				-40°C to 125°C	6	43	4	27	3	22	2	18	1	17	1	16							
		B	A	-40°C to 85°C	3	36	1	24	1	22	1	19	1	18	1	17							
				-40°C to 125°C	5	33	3	25	3	22	2	19	2	18	1	18							
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	2	21	2	21	2	21	2	21	2	21	1	21	ns						
				-40°C to 125°C	3	22	3	22	3	22	3	22	3	22	3	22							
		DIR	B	-40°C to 85°C	7	65	5	35	4	29	2	22	2	21	1	19							
				-40°C to 125°C	10	56	8	36	7	30	6	24	5	22	3	20							
$t_{en}$	Enable time	DIR	A	-40°C to 85°C	15	96	11	54	10	46	8	36	7	34	6	31	ns						
				-40°C to 125°C	20	82	17	56	15	48	13	38	12	35	10	33							
		DIR	B	-40°C to 85°C	11	80	9	42	7	37	7	33	6	31	6	30							
				-40°C to 125°C	14	60	12	43	11	39	10	34	9	33	9	32							

## 6.9 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2 \text{ V}$

See [Figure 7-1](#) and [Table 7-1](#) for test circuit and loading. See [Figure 7-2](#), [Figure 7-3](#), and [Figure 7-4](#) for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT						
				$1.2 \pm 0.1 \text{ V}$			$1.5 \pm 0.1 \text{ V}$			$1.8 \pm 0.15 \text{ V}$			$2.5 \pm 0.2 \text{ V}$				$3.3 \pm 0.3 \text{ V}$			$5.0 \pm 0.5 \text{ V}$		
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	MIN	TYP	MAX
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	3	60	1	23	1	19	1	15	1	14	1	13	ns					
				-40°C to 125°C	5	38	3	24	2	19	1	15	1	14	1	13						
		B	A	-40°C to 85°C	1	33	1	20	1	18	1	15	1	14	1	14						
				-40°C to 125°C	3	30	2	21	2	18	1	15	1	14	1	14						
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	1	15	1	15	1	15	1	15	1	15	1	15	ns					
				-40°C to 125°C	1	15	1	15	1	15	1	15	1	15	1	15						
		DIR	B	-40°C to 85°C	5	54	4	30	3	25	2	19	2	18	1	16						
				-40°C to 125°C	8	47	7	31	6	26	5	21	4	19	2	17						
$t_{en}$	Enable time	DIR	A	-40°C to 85°C	12	82	9	44	8	37	6	29	6	27	5	24	ns					
				-40°C to 125°C	17	68	14	45	13	39	11	31	10	29	8	26						
		DIR	B	-40°C to 85°C	8	67	6	33	5	29	4	25	4	23	4	22						
				-40°C to 125°C	11	49	9	34	8	30	7	26	7	24	6	23						

## 6.10 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3 \text{ V}$

See [Figure 7-1](#) and [Table 7-1](#) for test circuit and loading. See [Figure 7-2](#), [Figure 7-3](#), and [Figure 7-4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT						
					$1.2 \pm 0.1 \text{ V}$			$1.5 \pm 0.1 \text{ V}$			$1.8 \pm 0.15 \text{ V}$			$2.5 \pm 0.2 \text{ V}$				$3.3 \pm 0.3 \text{ V}$			$5.0 \pm 0.5 \text{ V}$		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	MIN	TYP	MAX
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	3	57	1	22	1	18	1	14	1	13	1	12	ns						
				-40°C to 125°C	4	37	3	22	2	18	1	14	1	13	1	12							
		B	A	-40°C to 85°C	1	34	1	19	1	16	1	13	1	13	1	12							
				-40°C to 125°C	3	30	2	20	1	17	1	14	1	13	1	12							
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	1	14	1	14	1	14	1	14	1	14	1	14	ns						
				-40°C to 125°C	1	14	1	14	1	14	1	14	1	14	1	14							
		DIR	B	-40°C to 85°C	5	49	3	27	3	23	1	18	2	17	1	15							
				-40°C to 125°C	8	44	6	28	5	24	4	19	4	18	2	16							
$t_{en}$	Enable time	DIR	A	-40°C to 85°C	12	78	8	39	7	33	6	26	5	25	4	22	ns						
				-40°C to 125°C	16	64	13	40	11	35	9	28	9	26	7	23							
		DIR	B	-40°C to 85°C	8	64	6	30	5	26	4	23	4	21	4	20							
				-40°C to 125°C	11	46	9	31	8	27	7	24	6	22	6	21							

## 6.11 Switching Characteristics, $V_{CCA} = 5.0 \pm 0.5 \text{ V}$

See [Figure 7-1](#) and [Table 7-1](#) for test circuit and loading. See [Figure 7-2](#), [Figure 7-3](#), and [Figure 7-4](#) for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT						
				1.2 ± 0.1 V			1.5 ± 0.1 V			1.8 ± 0.15 V			2.5 ± 0.2 V				3.3 ± 0.3 V			5.0 ± 0.5 V		
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	MIN	TYP	MAX
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	3	58	1	21	1	17	1	14	1	12	1	11	ns					
				-40°C to 125°C	4	36	2	22	1	18	1	14	1	13	1	11						
	B	A	-40°C to 85°C	1	44	1	19	1	16	1	13	1	12	1	11							
			-40°C to 125°C	2	33	1	20	1	16	1	13	1	12	1	11							
$t_{dis}$	Disable time	DIR	A	-40°C to 85°C	1	12	1	12	1	12	1	12	1	12	1	12	ns					
				-40°C to 125°C	1	12	1	12	1	12	1	12	1	12	1	12						
		DIR	B	-40°C to 85°C	5	48	3	26	3	21	1	16	2	16	1	14						
				-40°C to 125°C	8	43	6	26	5	22	3	17	3	17	2	15						
$t_{en}$	Enable time	DIR	A	-40°C to 85°C	11	87	8	38	7	31	5	24	5	22	4	20	ns					
				-40°C to 125°C	15	66	12	39	10	32	8	25	8	24	6	21						
		DIR	B	-40°C to 85°C	7	63	5	28	4	24	3	20	3	19	2	18						
				-40°C to 125°C	9	43	7	28	6	25	5	21	4	19	4	18						

## 6.12 スイッチング特性：T<sub>sk</sub>、T<sub>MAX</sub>

自由気流での動作温度範囲内 (特に記述のない限り)

パラメータ	測定条件		V <sub>CCI</sub>	V <sub>CCO</sub>	自由気流での動作温度 (T <sub>A</sub> )			単位
					-40°C~125°C			
					最小	標準	最大	
T <sub>MAX</sub> - 最大データレート	50% デューティ・サイクル 入力 1 チャネル・スイッチング パルスの 20% > 0.7 *V <sub>CCO</sub> パルスの 20% < 0.3 *V <sub>CCO</sub>	昇圧変換	3.0V~3.6V	4.5V~5.5V	200	420	Mbps	
			2.25V~2.75V	4.5V~5.5V	150	300		
			1.65V~1.95V	4.5V~5.5V	100	200		
			1.1V~1.3V	4.5V~5.5V	20	40		
			1.65V~1.95V	3.0V~3.6V	100	210		
			1.1V~1.3V	3.0V~3.6V	10	20		
		降圧変換	4.5V~5.5V	3.0V~3.6V	100	210		
			4.5V~5.5V	2.25V~2.75V	75	140		
			4.5V~5.5V	1.65V~1.95V	50	75		
			4.5V~5.5V	1.1V~1.3V	15	30		
			3.0V~3.6V	1.65V~1.95V	40	75		
			3.0V~3.6V	1.1V~1.3V	10	20		
			1.65V~1.95V	1.1V~1.3V	5	10		

## 6.13 Operating Characteristics

T<sub>A</sub> = 25°C (1)

PARAMETER		Test Conditions	Supply Voltage (V <sub>CCB</sub> = V <sub>CCA</sub> )						UNIT
			1.2 ± 0.1V	1.5 ± 0.1V	1.8 ± 0.15V	2.5 ± 0.2V	3.3 ± 0.3V	5.0 ± 0.5V	
			TYP	TYP	TYP	TYP	TYP	TYP	
C <sub>pdA</sub> (2)	A to B	A Port CL = 0, RL = Open f = 10 MHz t <sub>rise</sub> = t <sub>fall</sub> = 1 ns	3.2	3.4	3.5	3.7	3.9	5.1	pF
	B to A		19.4	19.6	19.8	20.4	21.8	25.7	
C <sub>pdB</sub> (2)	A to B	B Port CL = 0, RL = Open f = 10 MHz t <sub>rise</sub> = t <sub>fall</sub> = 1 ns	19.3	19.5	19.7	20.4	21.6	25.3	pF
	B to A		3.3	3.5	3.6	4.0	4.4	5.0	

- (1) For more information about power dissipation capacitance, see the [CMOS Power Consumption and C<sub>pd</sub> Calculation](#) application report  
(2) C<sub>pdA</sub> and C<sub>pdB</sub> are respectively A-Port and B-Port power dissipation capacitances per transceiver

### 6.14 Typical Characteristics

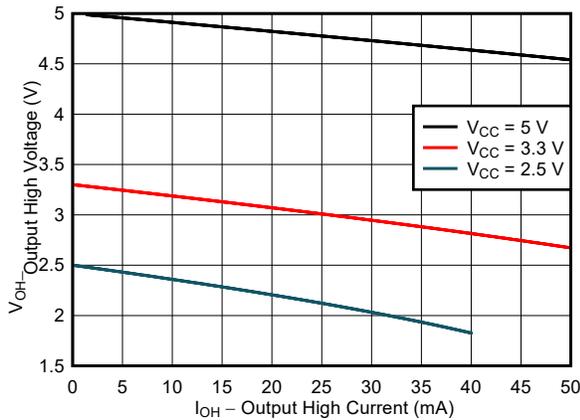


Fig 6-1. Typical ( $T_A=25^\circ\text{C}$ ) Output High Voltage ( $V_{OH}$ ) vs Source Current ( $I_{OH}$ )

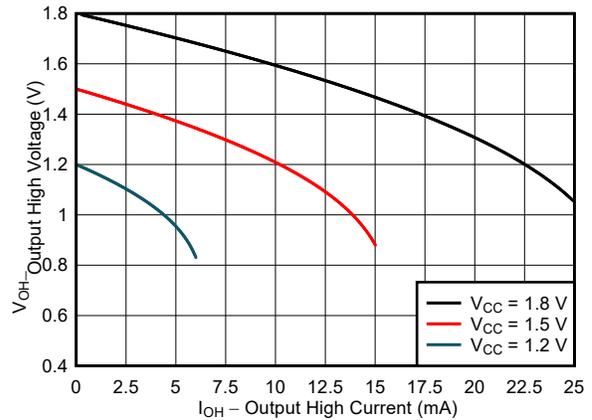


Fig 6-2. Typical ( $T_A=25^\circ\text{C}$ ) Output High Voltage ( $V_{OH}$ ) vs Source Current ( $I_{OH}$ )

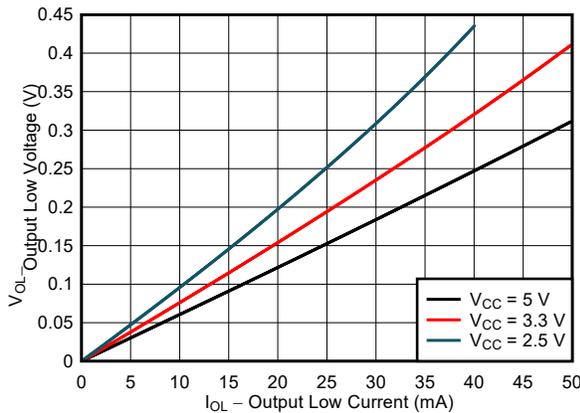


Fig 6-3. Typical ( $T_A=25^\circ\text{C}$ ) Output Low Voltage ( $V_{OL}$ ) vs Sink Current ( $I_{OL}$ )

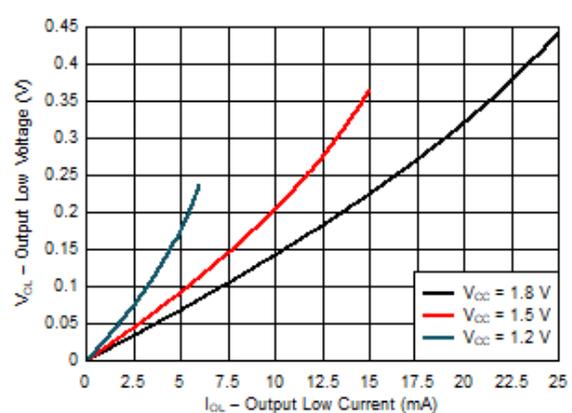


Fig 6-4. Typical ( $T_A=25^\circ\text{C}$ ) Output Low Voltage ( $V_{OL}$ ) vs Sink Current ( $I_{OL}$ )

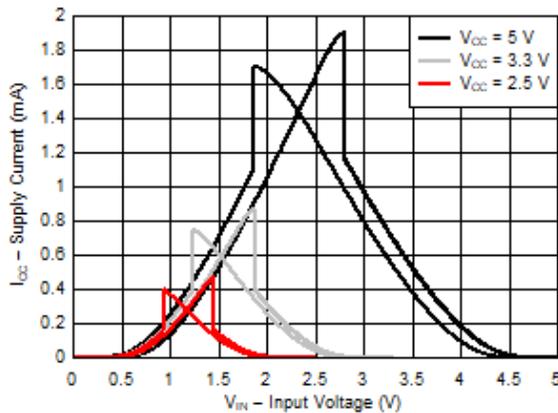


Fig 6-5. Typical ( $T_A=25^\circ\text{C}$ ) Supply Current ( $I_{CC}$ ) vs Input Voltage ( $V_{IN}$ )

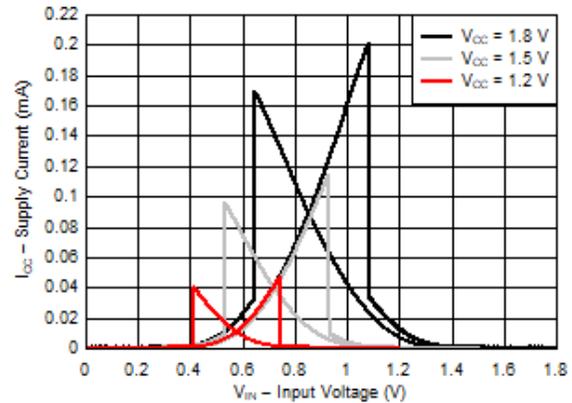


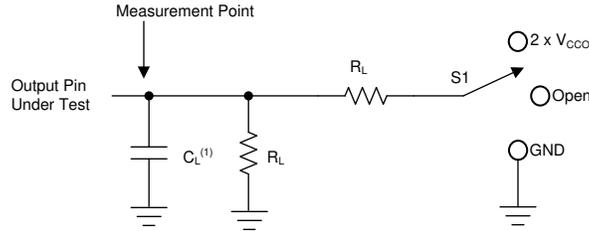
Fig 6-6. Typical ( $T_A=25^\circ\text{C}$ ) Supply Current ( $I_{CC}$ ) vs Input Voltage ( $V_{IN}$ )

## 7 Parameter Measurement Information

### 7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 1 \text{ MHz}$
- $Z_O = 50 \Omega$
- $\Delta t/\Delta V \leq 1 \text{ ns/V}$

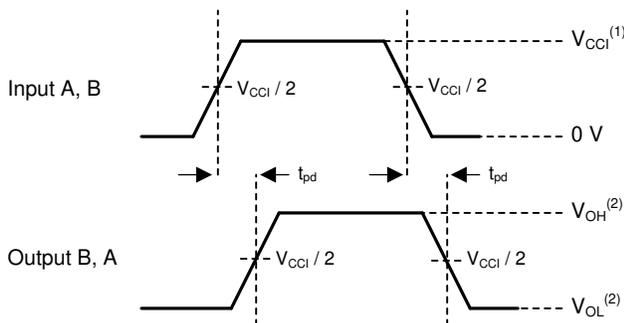


A.  $C_L$  includes probe and jig capacitance.

图 7-1. Load Circuit

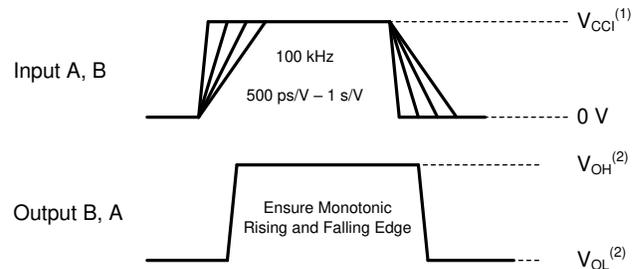
表 7-1. Load Circuit Conditions

Parameter	$V_{CCO}$	$R_L$	$C_L$	$S_1$	$V_{TP}$
$t_{pd}$ Propagation (delay) time	1.1 V – 5.5 V	2 k $\Omega$	15 pF	Open	N/A
$t_{en}, t_{dis}$ Enable time, disable time	1.1 V – 1.6 V	2 k $\Omega$	15 pF	$2 \times V_{CCO}$	0.1 V
	1.65 V – 2.7 V	2 k $\Omega$	15 pF	$2 \times V_{CCO}$	0.15 V
	3.0 V – 5.5 V	2 k $\Omega$	15 pF	$2 \times V_{CCO}$	0.3 V
$t_{en}, t_{dis}$ Enable time, disable time	1.1 V – 1.6 V	2 k $\Omega$	15 pF	GND	0.1 V
	1.65 V – 2.7 V	2 k $\Omega$	15 pF	GND	0.15 V
	3.0 V – 5.5 V	2 k $\Omega$	15 pF	GND	0.3 V



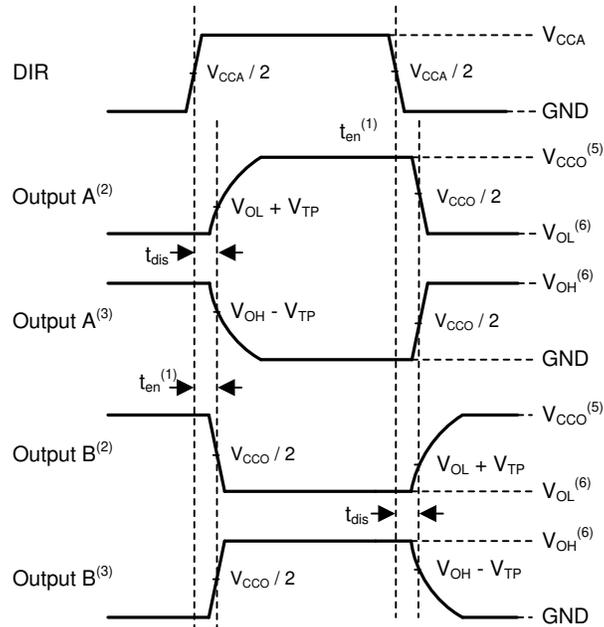
1.  $V_{CCI}$  is the supply pin associated with the input port.
2.  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels that occur with specified  $R_L$ ,  $C_L$ , and  $S_1$

图 7-2. Propagation Delay



1.  $V_{CCI}$  is the supply pin associated with the input port.
2.  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels that occur with specified  $R_L$ ,  $C_L$ , and  $S_1$

图 7-3. Input Transition Rise and Fall Rate



- A.
1. Illustrative purposes only. Enable time is a calculation as described in [Enable Times](#).
  2. Output waveform on the condition that input is driven to a valid Logic low.
  3. Output waveform on the condition that input is driven to a valid Logic high.
  4.  $V_{CCI}$  is the supply pin associated with the input port.
  5.  $V_{CCO}$  is the supply pin associated with the output port.
  6.  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .

#### 7-4. Enable Time And Disable Time

## 8 Detailed Description

### 8.1 Overview

The SN74LXC1T45 is an 1-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with both  $V_{CCA}$  and  $V_{CCB}$  supplies as low as 1.1 V and as high as 5.5 V. Additionally, the device can be operated with  $V_{CCA} = V_{CCB}$ . The A port is designed to track  $V_{CCA}$ , and the B port is designed to track  $V_{CCB}$ .

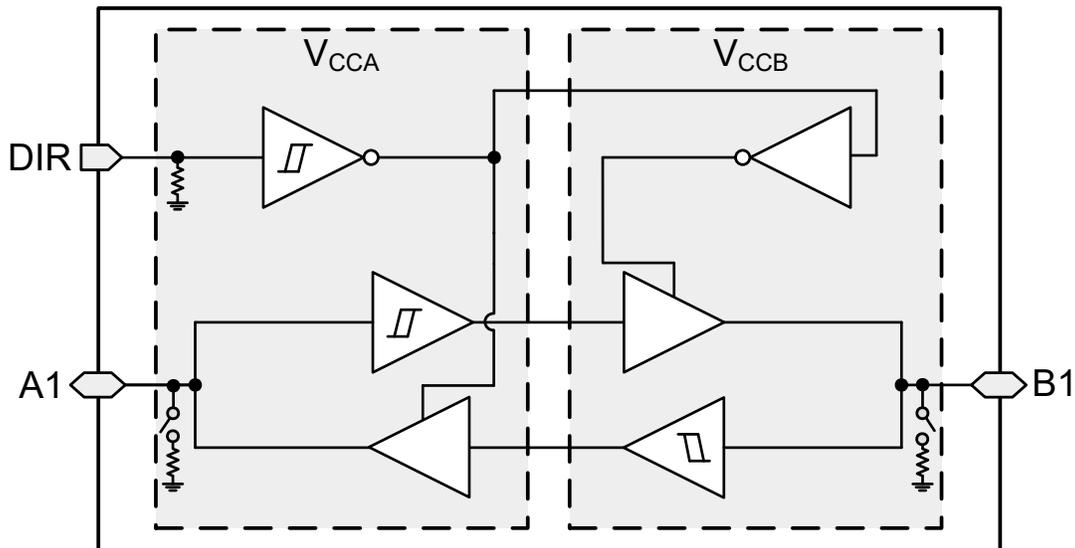
The SN74LXC1T45 device is designed for asynchronous communication between devices and transmits data from A to B or from B to A based on the logic level of the direction-control input (DIR). The control pins of the SN74LXC1T45 (DIR) is referenced to  $V_{CCA}$ . The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

This device is fully specified for partial-power-down applications using the  $I_{off}$  current. The  $I_{off}$  protection circuitry ensures that no excessive current is drawn from or sourced into an input, output, or I/O while the device is powered down.

The  $V_{CC}$  isolation or  $V_{CC}$  disconnect feature ensures that if either  $V_{CC}$  is less than 100 mV or disconnected with the complementary supply within the recommended operating conditions, then both I/O ports are weakly pulled-down and then set to the high-impedance state by disabling their outputs while the supply current is maintained. The  $I_{off-float}$  circuitry ensures that no excessive current is drawn from or sourced into an input, output, or I/O while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, see [Understanding Schmitt Triggers](#).

### 8.3.1.1 I/O's with Integrated Dynamic Pull-Down Resistors

Input circuits of the data I/O's are always active even when the device is disabled. It is recommended to keep a valid voltage level at the I/O's to avoid high current consumption. To help avoid floating inputs on the I/O's during disabling, this device has 100-k $\Omega$  typical integrated weak dynamic pull-downs on all data I/O's. When the device is disabled, the dynamic pull-downs are activated for only a short period of time to help drive and keep low any floating inputs before the device I/O's become high impedance. If the I/O lines are to be floated after the device is disabled, then it is recommended to keep them at a valid input voltage level using the external pull-downs. This feature is ideal for loads of 30 pF or less. If greater capacitive loading is present, then external pull-downs are recommended. If an external pull-up is required, then it should be no larger than 15 k $\Omega$  to avoid contention with the 100 k $\Omega$  internal pull-down.

### 8.3.1.2 Control Inputs with Integrated Static Pull-Down Resistors

Similar to the data I/O's, a floating control input can cause high current consumption. To help avoid this concern, this device has integrated weak static pull-downs of 5-M $\Omega$  typical on the control input (DIR). These pull-downs are always present. So for example if the DIR pin is left floating, then the B port will be configured as an input and the A port configured as an output.

### 8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

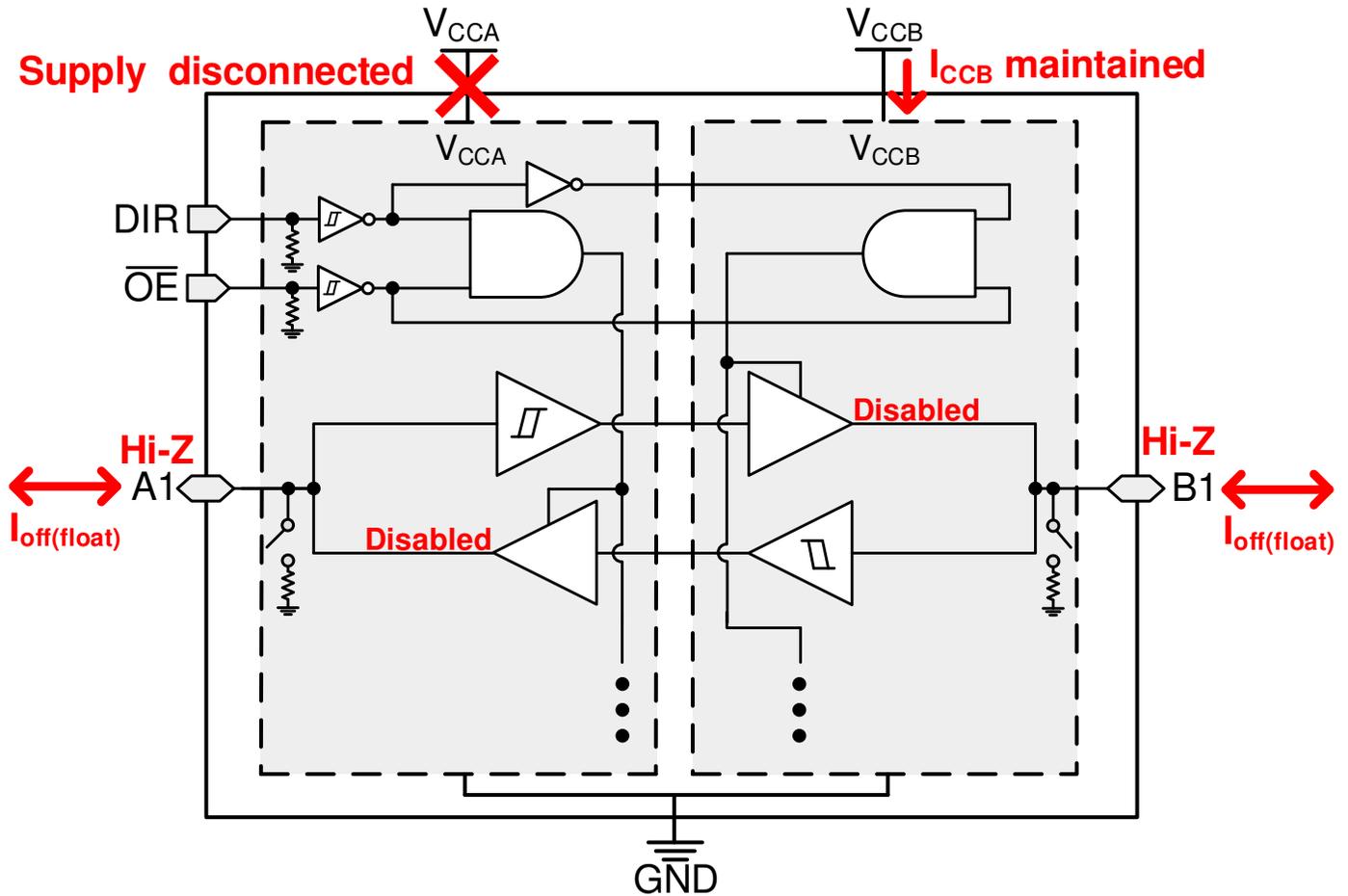
### 8.3.3 Partial Power Down ( $I_{off}$ )

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by  $I_{off}$  in the [Electrical Characteristics](#).

### 8.3.4 $V_{CC}$ Isolation and $V_{CC}$ Disconnect ( $I_{off(float)}$ )

This device has [I/O's with Integrated Dynamic Pull-Down Resistors](#). The I/O's will get pulled down and then enter a high-impedance state when either supply is < 100 mV or left floating (disconnected), while the other supply is still connected to the device. It is recommended that the I/O's for this device are not driven and kept at a logic low state prior to floating (disconnecting) either supply.

The maximum supply current is specified by  $I_{CCx}$ , while  $V_{CCx}$  is floating, in the [Electrical Characteristics](#). The maximum leakage into or out of any input or output pin on the device is specified by  $I_{off(float)}$  in the [Electrical Characteristics](#).



8-1.  $V_{CC}$  Disconnect Feature

### 8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

### 8.3.6 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to  $V_{CC}$  when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

### 8.3.7 Negative Clamping Diodes

Figure 8-2 shows the inputs and outputs to this device that have negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative voltage and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

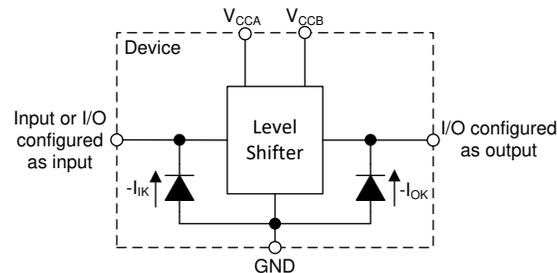


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.3.8 Fully Configurable Dual-Rail Design

Both the  $V_{CCA}$  and  $V_{CCB}$  pins can be supplied at any voltage from 1.1 V to 5.5 V, making the device suitable for translating between any of the voltage nodes (1.2 V, 1.5 V, 1.8 V, 3.3 V, and 5.0 V).

### 8.3.9 Supports High-Speed Translation

The SN74LXC1T45 device can support high data rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5.0 V.

## 8.4 Device Functional Modes

Table 8-1. Function Table

CONTROL INPUTS <sup>(1)</sup>	PORT STATUS		OPERATION
	DIR	A PORT	
L	Output (Enabled)	Input (Hi-Z)	B data to A bus
H	Input (Hi-Z)	Output (Enabled)	A data to B bus

(1) Input circuits of the data I/Os are always active and should be kept at a valid logic level.

## 9 Application and Implementation

### Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The SN74LXC1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74LXC1T45 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 420 Mbps when the device translates a signal from 3.3 V to 5.0 V.

### 9.2 Enable Times

Calculate the enable times for the SN74LXC1T45 using the following formulas:

$$t_{A\_en} (\text{DIR to A}) = t_{dis} (\text{DIR to B}) + t_{pd} (\text{B to A}) \quad (1)$$

$$t_{B\_en} (\text{DIR to B}) = t_{dis} (\text{DIR to A}) + t_{pd} (\text{A to B}) \quad (2)$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74LXC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled ( $t_{dis}$ ) before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay ( $t_{pd}$ ). To avoid bus contention, care should be taken to not apply an input signal prior to the output being disabled ( $t_{dis}$  maximum).

### 9.3 Typical Application

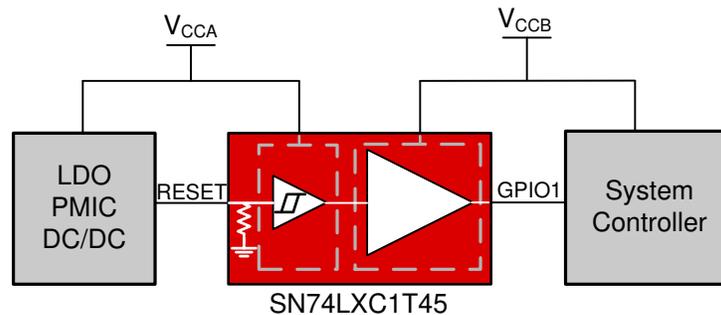


图 9-1. LED Driver Application

#### 9.3.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.1 V to 5.5 V
Output voltage range	1.1 V to 5.5 V

### 9.3.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LXC1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage ( $V_{t+}$ ) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage ( $V_{t-}$ ) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LXC1T45 device is driving to determine the output voltage range.

## 10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices, as described in [Glitch-free Power Supply Sequencing](#).

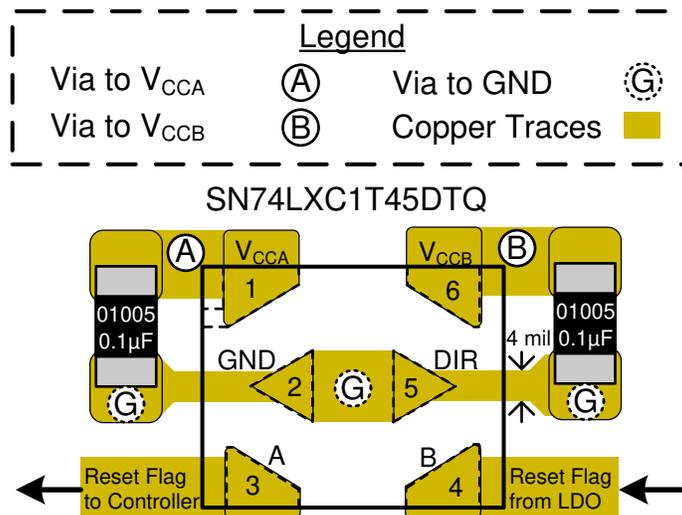
## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1  $\mu\text{F}$  capacitor is recommended, but transient performance can be improved by having both 1  $\mu\text{F}$  and 0.1  $\mu\text{F}$  capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 11.2 Layout Example



✎ 11-1. Layout Example – SN74LXC1T45

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Regulatory Requirements

No statutory or regulatory requirements apply to this device.

There are no special characteristics for this product.

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Understanding Schmitt Triggers application report](#)

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 サポート・リソース

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### 12.5 Trademarks

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### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LXC1T45DBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	2LSF
SN74LXC1T45DBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2LSF
<a href="#">SN74LXC1T45DCKR</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1L1
SN74LXC1T45DCKR.A	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1L1
<a href="#">SN74LXC1T45DRYR</a>	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MK
SN74LXC1T45DRYR.A	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MK
<a href="#">SN74LXC1T45DTQR</a>	Active	Production	X2SON (DTQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ME
SN74LXC1T45DTQR.A	Active	Production	X2SON (DTQ)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ME

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

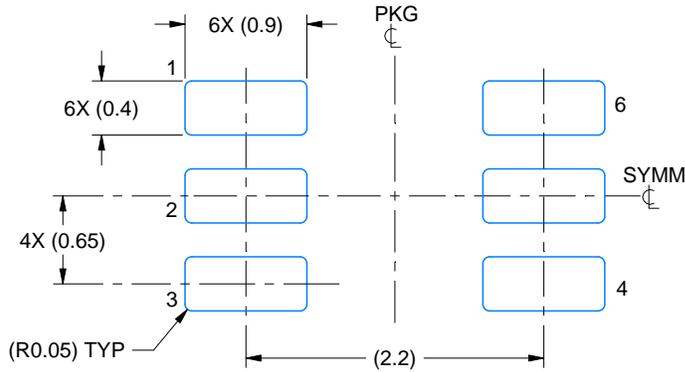
**OTHER QUALIFIED VERSIONS OF SN74LXC1T45 :**

- Automotive : [SN74LXC1T45-Q1](#)

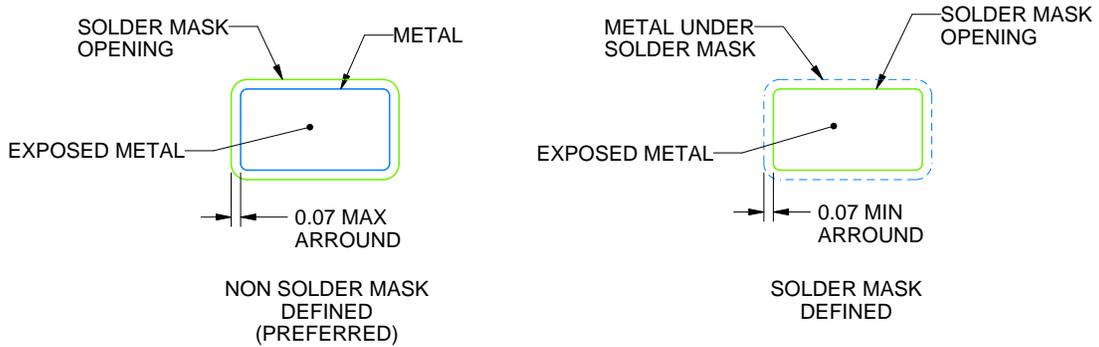
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

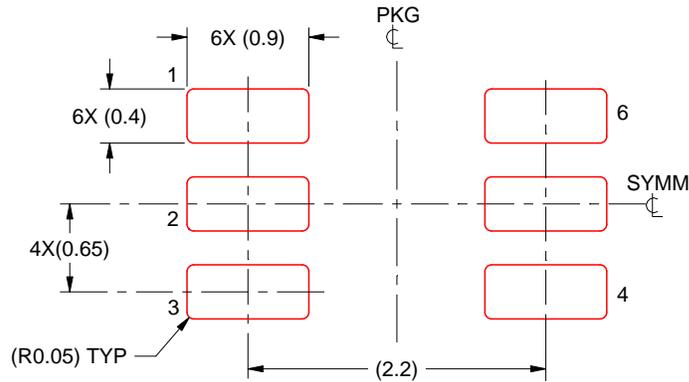


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DRY 6**

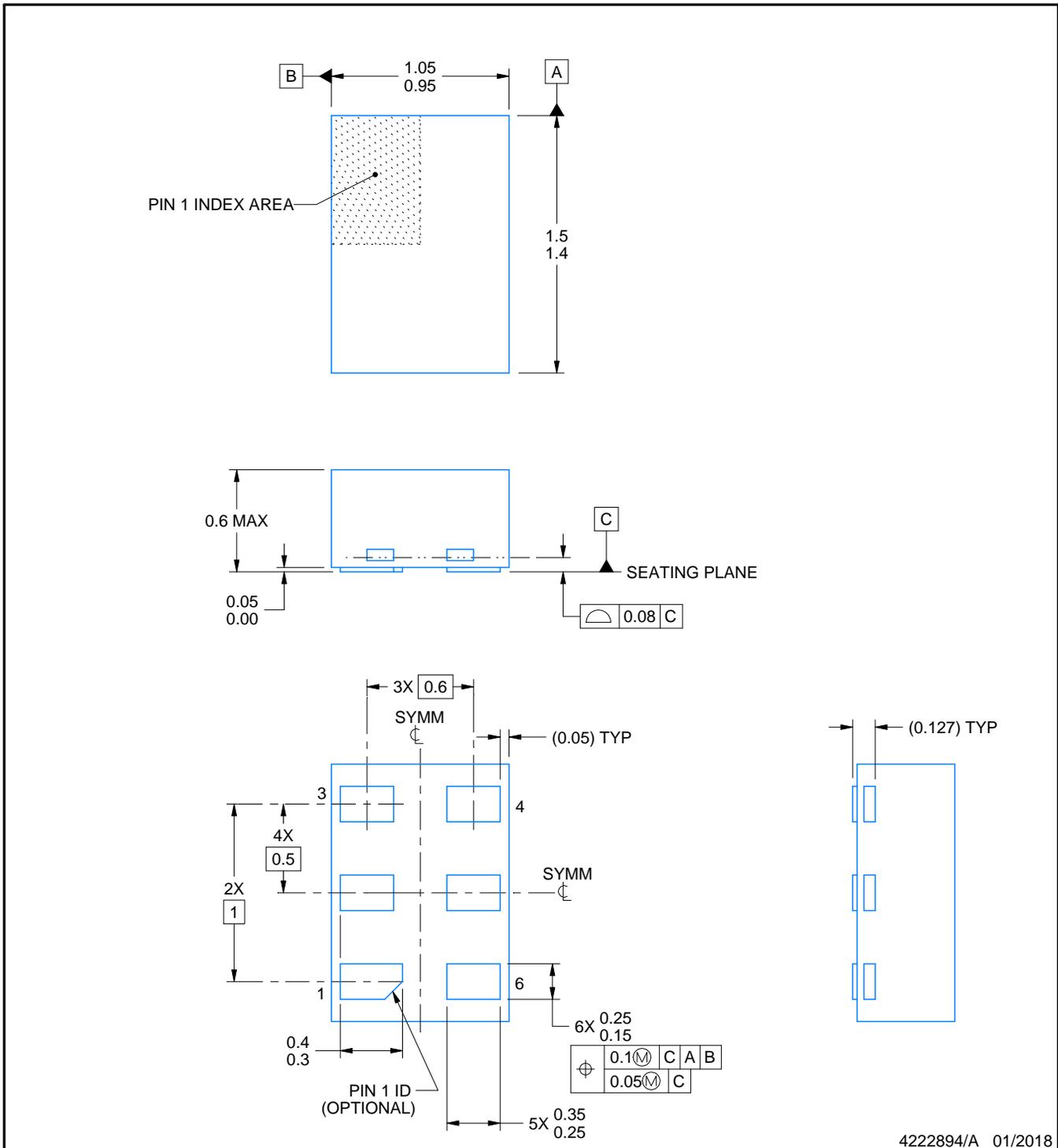
**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G



NOTES:

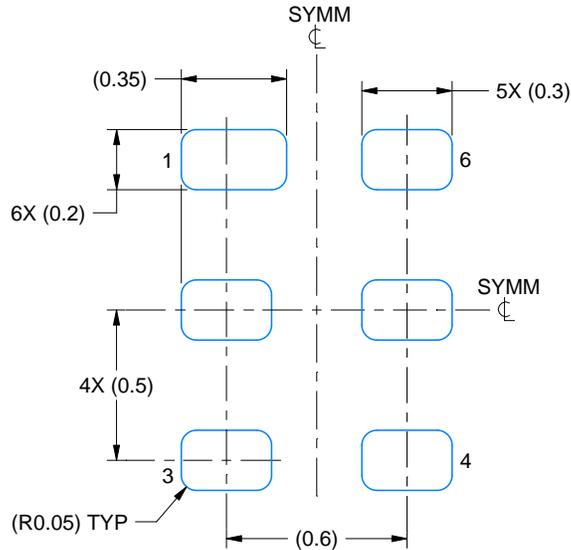
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

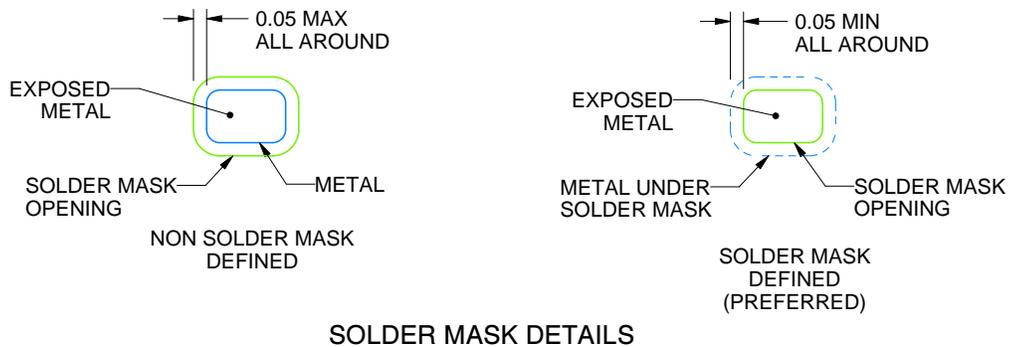
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

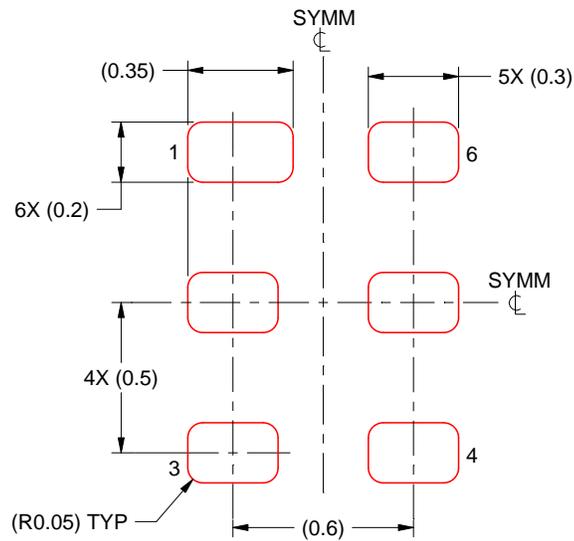
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

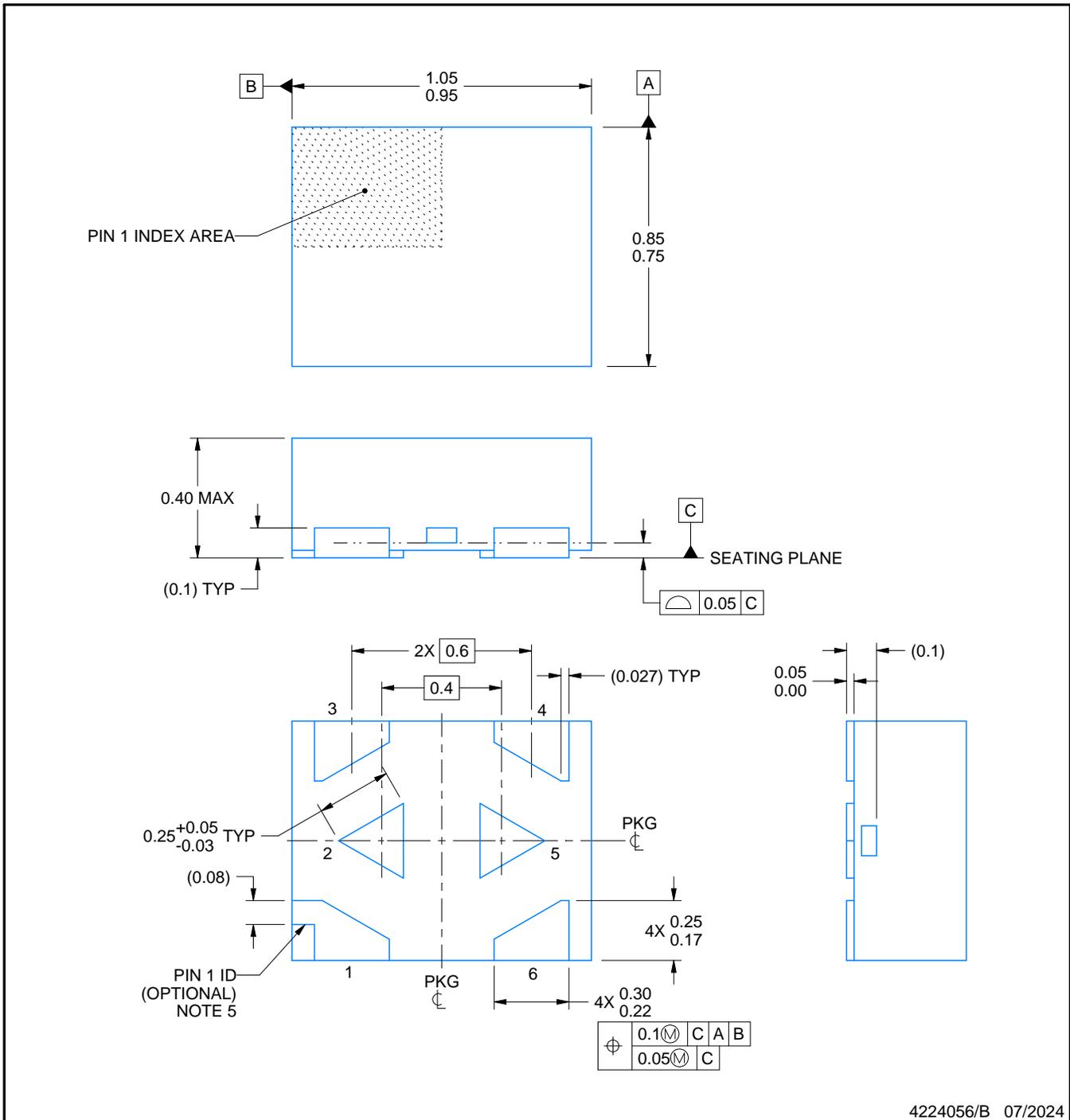


SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

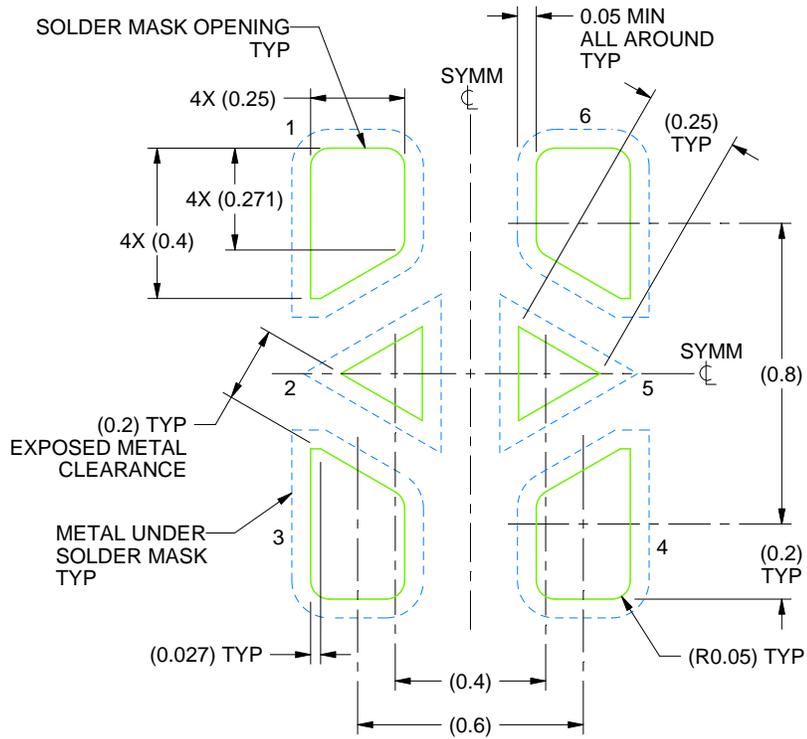
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

# EXAMPLE BOARD LAYOUT

DTQ0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:50X

4224056/B 07/2024

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



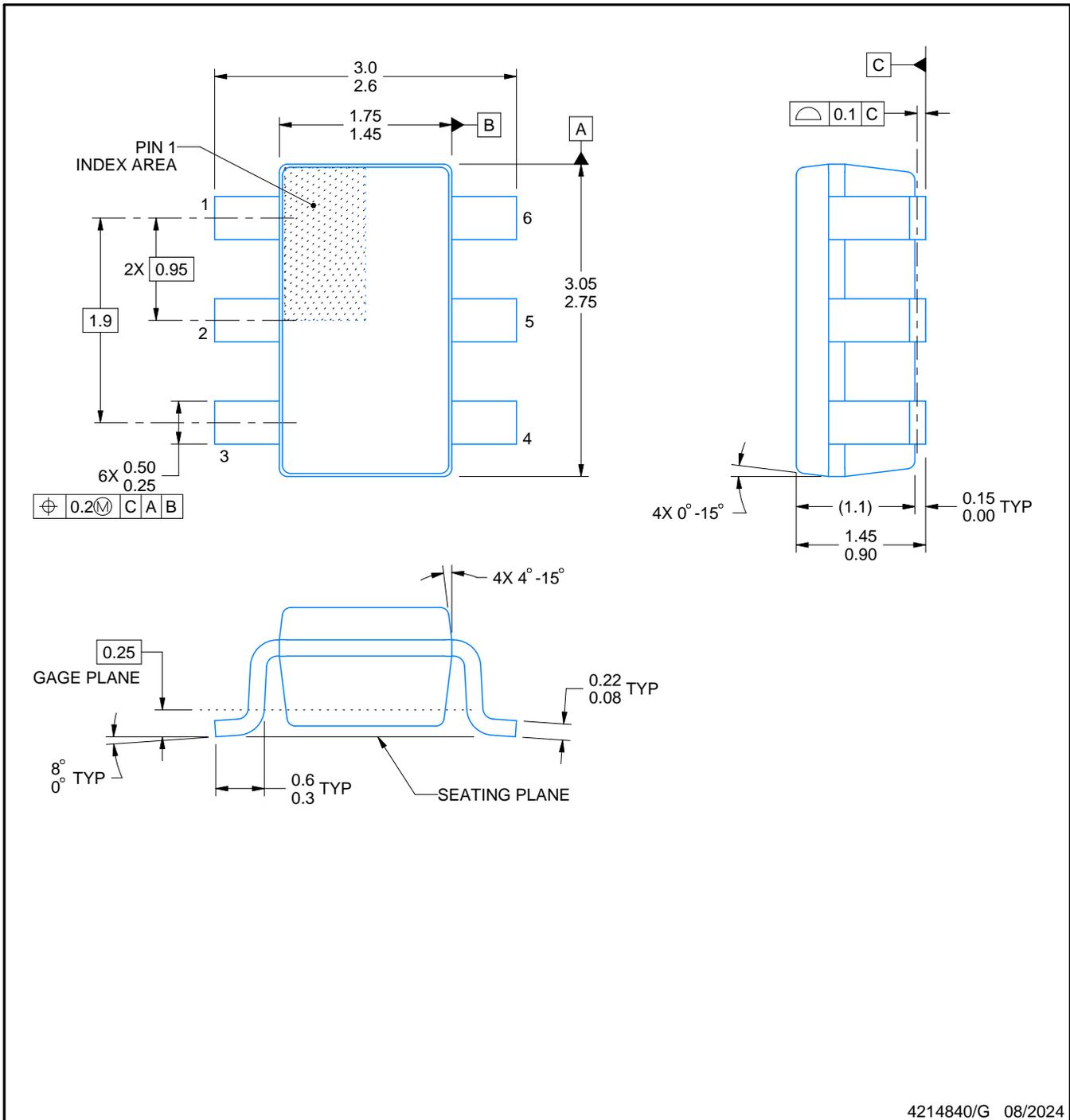
# DBV0006A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

## NOTES:

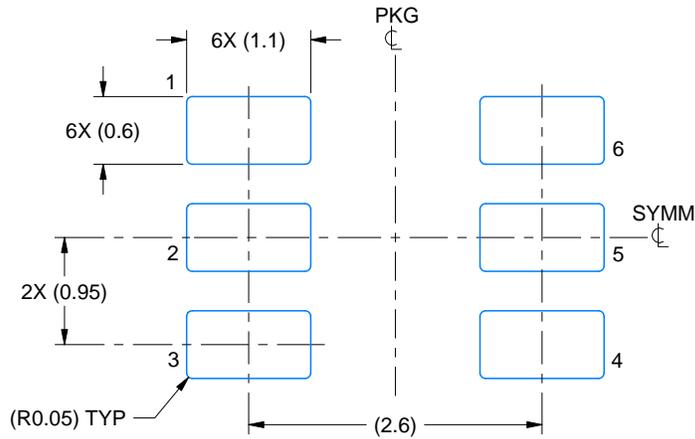
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

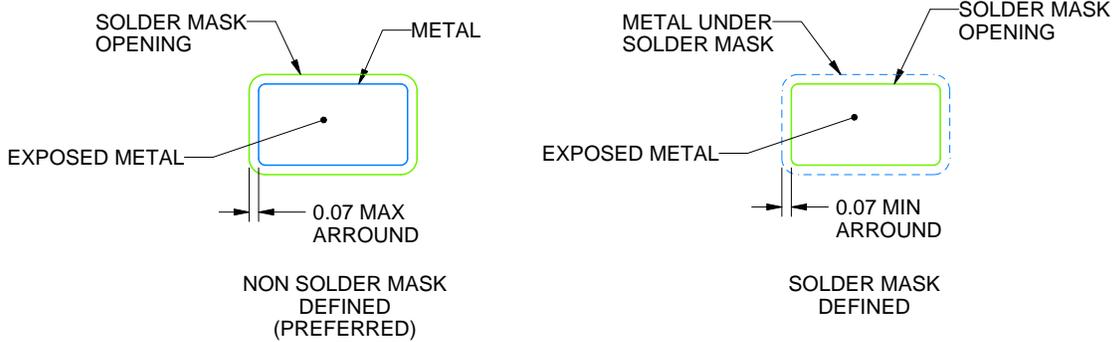
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

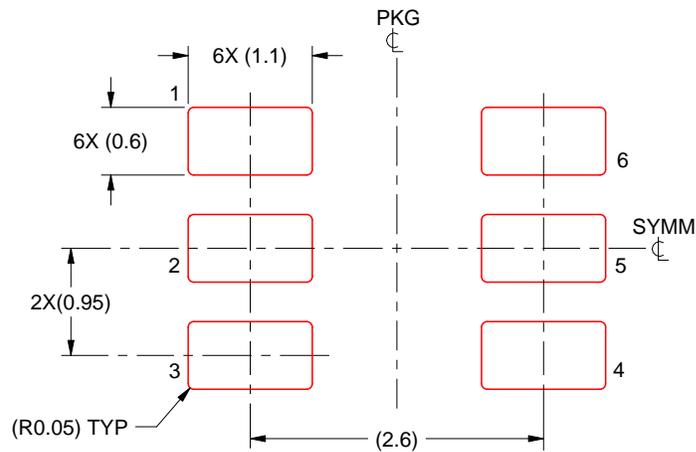
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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