SN75LVPE5421 PCIe® 5.0 32Gbps 4 チャネル リニア リドライバ、2：1 マルチプレクサ

1 特長

- 2：1 マルチプレクサを内蔵したクワッド チャネル PCIe 5.0 リニア リドライバ / リピータ
- PCIe、UPI、CCIX 、NVLink、DisplayPort、SAS、SATA、XFI 互換のプロトコル非依存リニア ドライバ
- 単一の 3.3V 電源 – PCIe 電源レール使用可能
- 4 チャネル動作用 720mW 低起動消費電力
- ヒート シンク不要
- 16GHz において最高 24dB のイコライゼーションを実現
- 8～16GHz に対して -10dB の卓越した RX/TX 差動 RL
- PRBS データによる 55fs RMS の低い追加 RJ
- 短いレイテンシ: 90ps
- 自動レシーバ検出機能と、PCIe リンク トレーニングのシームレスなサポート
- ピン制御または SMBus/I²C によるデバイス構成
- ピンによる Mux の選択
- 内部電圧レギュレータによる電源ノイズへの耐性
- 信頼性の高い製造を実現するための高速な製造テスト
- 1 つまたは複数のデバイスを使用して x4、x8、x16 バス幅をサポート
- デマルチプレクサ製品 SN75LVPE5412
- 温度範囲：-40°C～85°C
- 3.5mm × 9mm 42 ピン、0.5mm ピッチの WQFN パッケージ

2 アプリケーション

- デスクトップ PC とマザーボード
- ディスプレイ・パネル、ゲーム・コンソール
- ラック・サーバー、マイクロサーバー、タワー・サーバー
- 高性能コンピューティング、ハードウェア・アクセラレータ
- データ・ストレージ、ネットワーク接続ストレージ
- ストレージ・エリア・ネットワーク (SAN) とホスト・バス・アダプタ (HBA) カード
- ネットワーク・インターフェイス・カード (NIC)

3 概要

SN75LVPE5421 は、4 チャネルのリニア リドライバで、マルチプレクサ (mux) が内蔵されています。低消費電力高性能リニア リドライバは、PCIe 5.0 や最大 32Gbps の他のインターフェイスをサポートするよう設計されています。

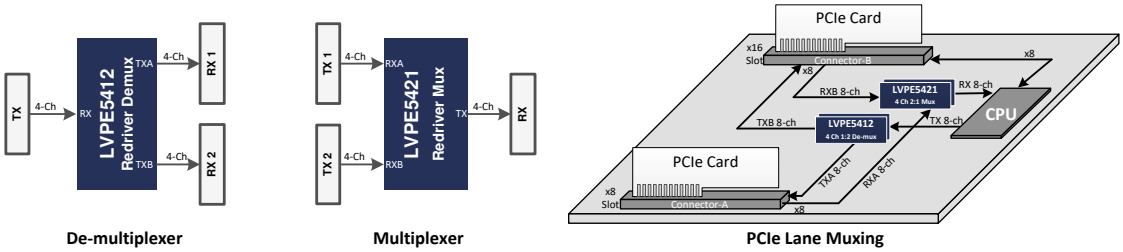
SN75LVPE5421 レシーバは、連続時間リニア イコライザ (CTLE) を搭載し、高周波数での昇圧を実現しています。イコライザは、相互接続媒体 (例：PCB 配線、ケーブル) に起因する符号間干渉 (ISI) によって完全に閉じた入力アイ パターンを開くことができます。PCIe リンク トレーニングの間に、リニア リドライバとルート コンプレックス (RC) - エンドポイント (EP) 間受動チャネルが全体として最良の送信および受信イコライゼーション設定を持つように調整され、結果的に最良の電気的リンクが得られます。チャネル間のクロストークが小さく、追加ジッタが小さく、リターンロスが非常に優れているため、デバイスはリンク内でほぼパッシブ要素になることができます。このデバイスは、内部リニア電圧レギュレータを備えており、高速データ パス用にクリーンな電源を供給し、基板上の電源ノイズへの高い耐性を実現します。

SN75LVPE5421 は、量産時に高速テストを実施しており、信頼性の高い大量生産に対応しています。また、このデバイスは AC および DC ゲインの変動が小さいため、大容量プラットフォームを展開する際の一貫したイコライゼーションにも対応しています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN75LVPE5421	RUA (WQFN、42)	9mm×3.5mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



De-multiplexer　Multiplexer　PCIe Lane Muxing

アプリケーション使用事例

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4 Pin Configuration and Functions

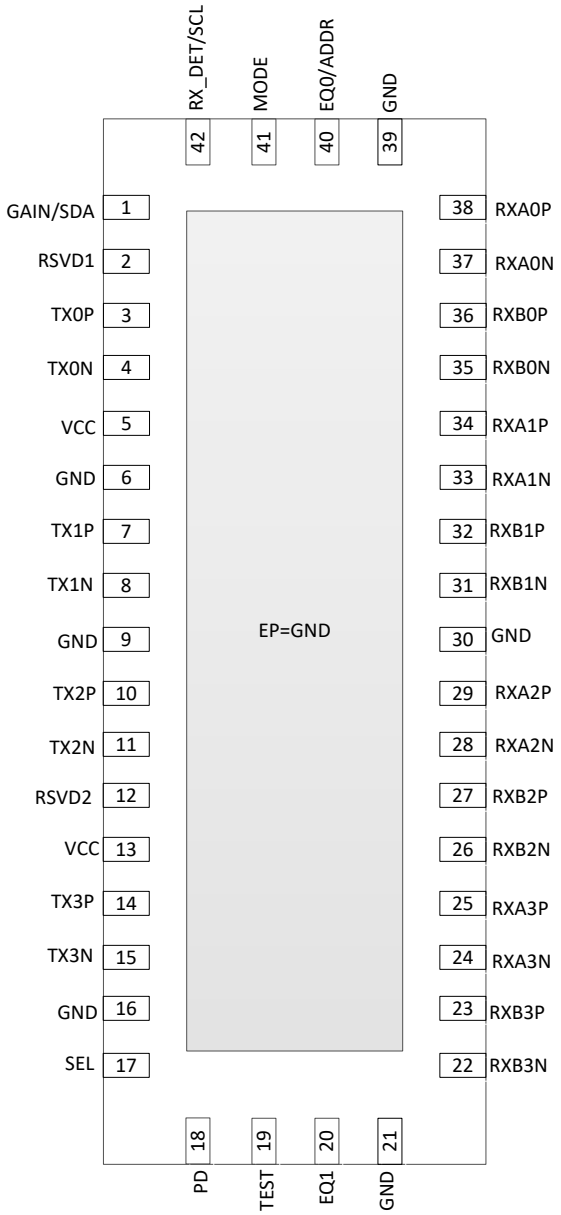


図 4-1. RUA Package, 42-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
MODE	41	I, 5-level	Sets device control configuration modes. The 5-level IO pin is defined in 表 6-1. The pin can be exercised at device power up or in normal operation mode. L0: *Pin Mode* – device control configuration is done solely by strap pins. L1 or L2: *SMBus/I²C Mode* – device control configuration is done by an external controller with SMBus/I²C primary. This pin along with ADDR pin sets devices secondary address. L3 and L4 (Float): RESERVED – TI internal test modes.
EQ0 /ADDR	40	I, 5-level	In *Pin Mode:* The EQ0 and EQ1 pins sets receiver linear equalization CTLE (AC gain) for all channels according to 表 6-2. These pins are sampled at device power-up only. In *SMBus/I²C Mode:* The ADDR pin in conjunction with MODE pin sets SMBus / I²C secondary address according to 表 6-5. The pin is sampled at device power-up only.
EQ1	20	I, 5-level	
GAIN /SDA	1	I, 5-level / IO	*In Pin Mode*: Flat gain (broadband gain – DC and AC) from the input to the output of the device for all channels. Note: the device also provides AC (high frequency) gain in the form of equalization controlled by EQ pins or SMBus/I²C registers. The pin is sampled at device power-up only. *In SMBus/I²C Mode*: 3.3V SMBus/I²C data. External pullup resistor such as 4.7 kΩ required for operation.
GND	EP, 6, 9, 16, 21, 30, 39	P	Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. It is used as the GND return for the device. The EP should be connected to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation.
PD	18	I, 3.3V LVCMOS	2-level logic controlling the operating state of the redriver. Active in both *Pin Mode* and *SMBus/I²C Mode*. The pin is used part of PCIe RX_DET state machine as outlined in 表 6-4. High: power down for all channels Low: power up, normal operation for all channels
RSVD1, 2	2, 12	—	Reserved pins – for best signal integrity performance connect the pins to GND. Alternate option would be 0 Ω resistors from pins to GND.
RX_DET /SCL	42	I, 5-level / IO	In *Pin Mode:* Sets receiver detect state machine options according to 表 6-4. The pin is sampled at device power-up only. In *SMBus/I²C Mode:* 3.3V SMBus/I²C clock. External pullup resistor such as 4.7 kΩ required for operation.
RXA0N	37	I	Inverting differential RX input – Port A, Channel 0.
RXA0P	38	I	Noninverting differential RX input – Port A, Channel 0.
RXA1N	33	I	Inverting differential RX input – Port A, Channel 1.
RXA1P	34	I	Noninverting differential RX input – Port A, Channel 1.
RXA2N	28	I	Inverting differential RX input – Port A, Channel 2.
RXA2P	29	I	Noninverting differential RX input – Port A, Channel 2.
RXA3N	24	I	Inverting differential RX input – Port A, Channel 3.
RXA3P	25	I	Noninverting differential RX input – Port A, Channel 3.
RXB0N	35	I	Inverting differential RX input – Port B, Channel 0.
RXB0P	36	I	Noninverting differential RX input – Port B, Channel 0.
RXB1N	31	I	Inverting differential RX input – Port B, Channel 1.
RXB1P	32	I	Noninverting differential RX input – Port B, Channel 1.
RXB2N	26	I	Inverting differential RX input – Port B, Channel 2.
RXB2P	27	I	Noninverting differential RX input – Port B, Channel 2.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RXB3N	22	I	Inverting differential RX input – Port B, Channel 3.
RXB3P	23	I	Noninverting differential RX input – Port B, Channel 3.
SEL	17	I, 3.3V LVCMOS	Selects the mux path. Active in both *Pin Mode* and *SMBus/I²C Mode*. The pin has a weak internal pull-down resistor. Note: the SEL pin must be exercised in system implementations for mux selection between Port A vs Port B. The pin is used for PCIe RX_DET state machine as outlined in 表 6-4. L: Port A selected. H: Port B selected.
TX0N	4	O	Inverting differential TX output, Channel 0.
TX0P	3	O	Noninverting differential TX output, Channel 0.
TX1N	8	O	Inverting differential TX output, Channel 1.
TX1P	7	O	Noninverting differential TX output, Channel 1.
TX2N	11	O	Inverting differential TX output, Channel 2.
TX2P	10	O	Noninverting differential TX output, Channel 2.
TX3N	15	O	Inverting differential TX output, Channel 3.
TX3P	14	O	Noninverting differential TX output, Channel 3.
TEST	19	O	TI internal test pin. Keep no connect.
VCC	5, 13	P	Power supply, VCC = 3.3V ± 10%. The VCC pins on this device should be connected through a low-resistance path to the board VCC plane.

(1) I = input, O = output, P = power, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage (VCC)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3V LVCMOS and open drain I/O voltage	–0.5	4.0	V
$VIO_{5LVL,ABSMAX}$	5-level input I/O voltage	–0.5	2.75	V
$VIO_{HS-RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS-TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance	DC to <50 Hz, sinusoidal[1]			250	mVpp
		50 Hz to 500 kHz, sinusoidal[1]			100	mVpp
		500 kHz to 2.5MHz, sinusoidal[1]			33	mVpp
		Supply noise, >2.5MHz, sinusoidal[1]			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0V to 3.0V	0.150		100	ms
T_J	Operating junction temperature		–40		115	°C
T_A	Operating ambient temperature		–40		85	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PD and SEL	200			µs
VCC_{SMBUS}	SMBus/I²C SDA and SCL open drain termination voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency in SMBus secondary mode		10		400	kHz
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate		1		32	Gbps

5.4 Thermal Information

THERMAL METRIC[1]		SN75LVPE5421	UNIT
		RUA, 42 Pins	
$R_{\theta JA\text{-}High\ K}$	Junction-to-ambient thermal resistance	26.1	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.1	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	℃/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	℃/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	℃/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

5.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
P_{ACT}	Device active power	All channels enabled (PD = L)		720	970	mW
P_{STBY}	Device power consumption in standby power mode	All channels disabled (PD = H)		23	36	mW
Control IO						
V_{IH}	High level input voltage	SDA, SCL, PD, SEL pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PD, SEL pins			1.08	V
V_{OH}	High level output voltage	$R_{pull\text{-}up}$ = 4.7kΩ (SDA, SCL pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = –4mA (SDA, SCL pins)			0.4	V
$I_{IH,SEL}$	Input high leakage current for SEL pins	V_{Input} = VCC, for SEL pin			100	µA
I_{IH}	Input high leakage current	V_{Input} = VCC, (SCL, SDA, PD pins)			10	µA
I_{IL}	Input low leakage current	V_{Input} = 0V, (SCL, SDA, PD, SEL pins)	-10			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6V, VCC = 0V, (SCL, SDA, PD, SEL pins)			200	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SCL, SDA, PD, SEL pins		1.6		pF
5 Level IOs (MODE, GAIN, EQ1, EQ0, RX_DET pins)						
I_{IH_5L}	Input high leakage current, 5 level IOs	VIN = 2.5V			10	µA
I_{IL_5L}	Input low leakage current for all 5 level IOs except MODE.	VIN = GND	-10			µA
$I_{IL\_5L,MODE}$	Input low leakage current for MODE pin	VIN = GND	-200			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	RX DC common mode voltage	Device is in active or standby state		1.4		V
$Z_{RX\text{-}DC}$	Rx DC single-ended impedance			50		Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	DC input CM input impedance during Reset or power-down	Inputs are at $V_{RX\text{-}DC\text{-}CM}$ voltage	20			kΩ
Transmitter						
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential Tx impedance	Impedance of Tx during active signaling, VID,diff = 1Vpp		100		Ω
$V_{TX\text{-}DC\text{-}CM}$	Tx DC common mode Voltage			1.0		V
$I_{TX\text{-}SHORT}$	Tx short circuit current	Total current the Tx can supply when shorted to GND		70		mA

5.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	50MHz to 1.25GHz		-22		dB
		1.25GHz to 2.5GHz		-22		dB
		2.5GHz to 4.0GHz		-22		dB
		4.0GHz to 8.0GHz		-16		dB
		8.0GHz to 16GHz		-9		dB
RL_{RX-CM}	Input common-mode return loss	50MHz to 2.5GHz		-20		dB
		2.5GHz to 8.0GHz		-14		dB
		8.0GHz to 16GHz		-8		dB
XT_{RX}	Receive-side pair-to-pair isolation	Pair-to-pair isolation (SDD21) between two adjacent receiver pairs from 10MHz to 16GHz.		-55		dB
Transmitter						
$V_{TX-AC-CM-PP}$	Tx AC peak-to-peak common mode voltage	Measured with lowest EQ, GAIN = L4; PRBS-7, 32Gbps, over at least 10^6 bits using a bandpass filter from 30 kHz to 500MHz			50	mVpp
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection	Measured while Tx is sensing whether a low-impedance receiver is present. No load is connected to the driver output	0		600	mV
$RL_{TX-DIFF}$	Output differential return loss	50MHz to 1.25GHz		-22		dB
		1.25GHz to 2.5GHz		-22		dB
		2.5GHz to 4.0GHz		-21		dB
		4.0GHz to 8.0GHz		-15		dB
		8.0GHz to 16GHz		-9		dB
RL_{TX-CM}	Output common-mode return loss	50MHz to 2.5GHz		-16		dB
		2.5GHz to 8.0GHz		-12		dB
		8.0GHz to 16GHz		-11		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent transmitter pairs from 10MHz to 16GHz.		-45		dB
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either low-to-high or high-to-low transition.		90	130	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	Between any two lanes within a single transmitter.			20	ps
$T_{RJ-DATA}$	Additive random jitter with data	Jitter through redriver minus the calibration trace. 32Gbps PRBS15. 800 mVpp-diff input swing.		55		fs
$T_{RJ-INTRINSIC}$	Intrinsic additive random jitter with clock	Jitter through redriver minus the calibration trace. 32GHz clock. 800 mVpp-diff input swing.		35		fs
$JITTER_{TOTAL-DATA}$	Additive total jitter with data	Jitter through redriver minus the calibration trace. 32Gbps PRBS15. 800 mVpp-diff input swing.		1.0		ps
$JITTER_{TOTAL-INTRINSIC}$	Intrinsic additive total jitter with clock	Jitter through redriver minus the calibration trace. 16GHz clock. 800 mVpp-diff input swing.		0.1		ps

5.6 High Speed Electrical Characteristics (続き)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLAT-GAIN	Broadband DC and AC flat gain - input to output, measured at DC	Minimum EQ, GAIN1/0=L0		-5.6		dB
		Minimum EQ, GAIN1/0=L1		-3.8		dB
		Minimum EQ, GAIN1/0=L2		-1.2		dB
		Minimum EQ, GAIN1/0=L3		2.6		dB
		Minimum EQ, GAIN1/0=L4 (Float)		0.6		dB
$EQ\text{-}MAX_{16G}$	EQ boost at max setting (EQ INDEX = 19)	AC gain at 16GHz relative to gain at 100MHz.		24		dB
LINEARITY-DC	Output DC linearity	at 0 dB flat gain		1700		mVpp
LINEARITY-AC	Output AC linearity at 32Gbps	at 0 dB flat gain		930		mVpp

5.7 SMBUS/I2C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Secondary Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
$t_{HD\text{-}STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
$t_{SU\text{-}STA}$	Set-up time for a repeated START condition		0.6			µs
$t_{HD\text{-}DAT}$	Data hold time		0			µs
$T_{SU\text{-}DAT}$	Data setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		120		ns
t_f	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		2		ns
$t_{SU\text{-}STO}$	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{VD\text{-}DAT}$	Data valid time				0.9	µs
$t_{VD\text{-}ACK}$	Data valid acknowledge time				0.9	µs
C_b	Capacitive load for each bus line				400	pF

5.8 Typical Characteristics

図 5-1 shows typical EQ gain curves versus frequency for different EQ settings. 図 5-2 shows EQ gain variation over temperature for maximum EQ setting of 19. 図 5-3 shows typical differential return loss for Rx and Tx pins.

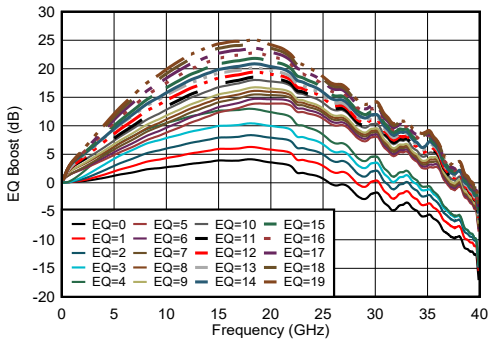


図 5-1. Typical EQ Boost vs Frequency

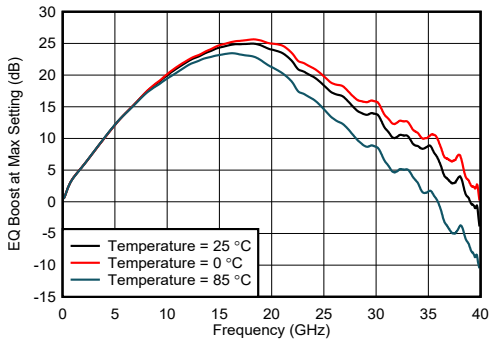


図 5-2. Typical EQ Boost vs Frequency at Different Temperature with EQ=19

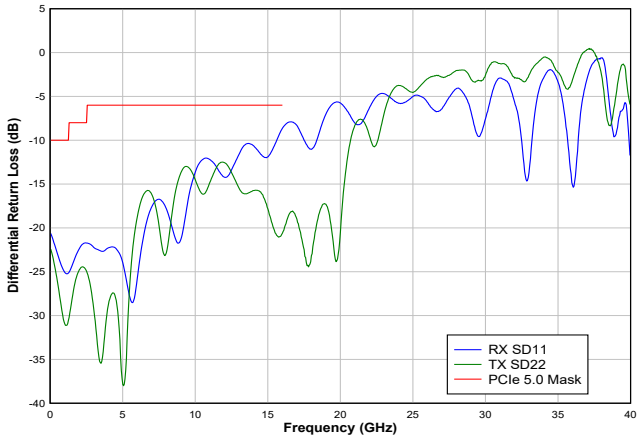


図 5-3. Typical Differential Return Loss

5.9 Typical Jitter Characteristics

図 5-4, 図 5-5, and 図 5-6 illustrate eye diagrams at source, through calibration traces, and through SN75LVPE5421 respectively.

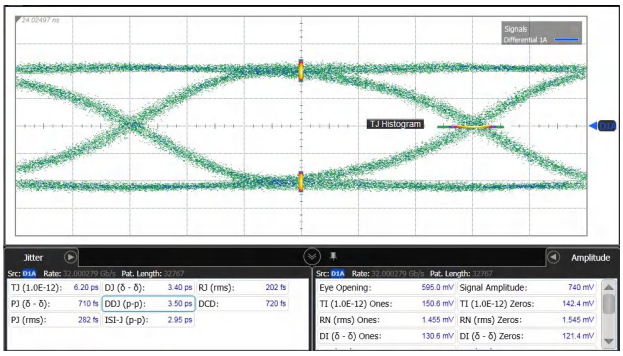


図 5-4. 32 Gbps 800 mV PRBS15 Source (1dB Loss)

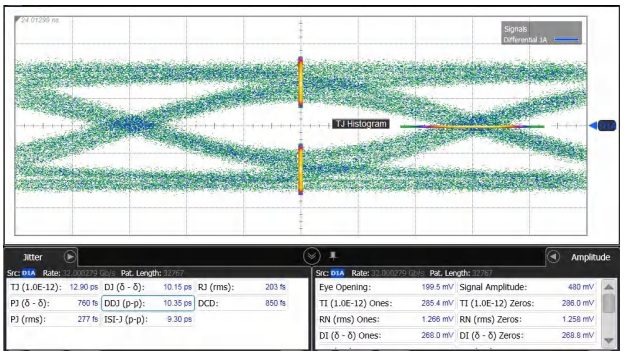


図 5-5. Through Calibration Trace (6.5dB Loss)

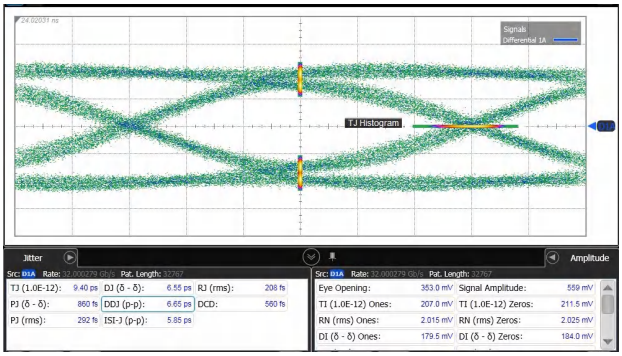


図 5-6. Through SN75LVPE5421 (6.5dB loss and DUT EQ=0)

6 Detailed Description

6.1 Overview

The SN75LVPE5421 is a four channel linear redriver with integrated multiplexer (mux). The low-power high-performance linear repeater or redriver is designed to support PCIe 1.0, 2.0, 3.0, 4.0, and 5.0. The device is a protocol agnostic linear redriver that can operate for other AC-coupled interface up to 32Gbps.

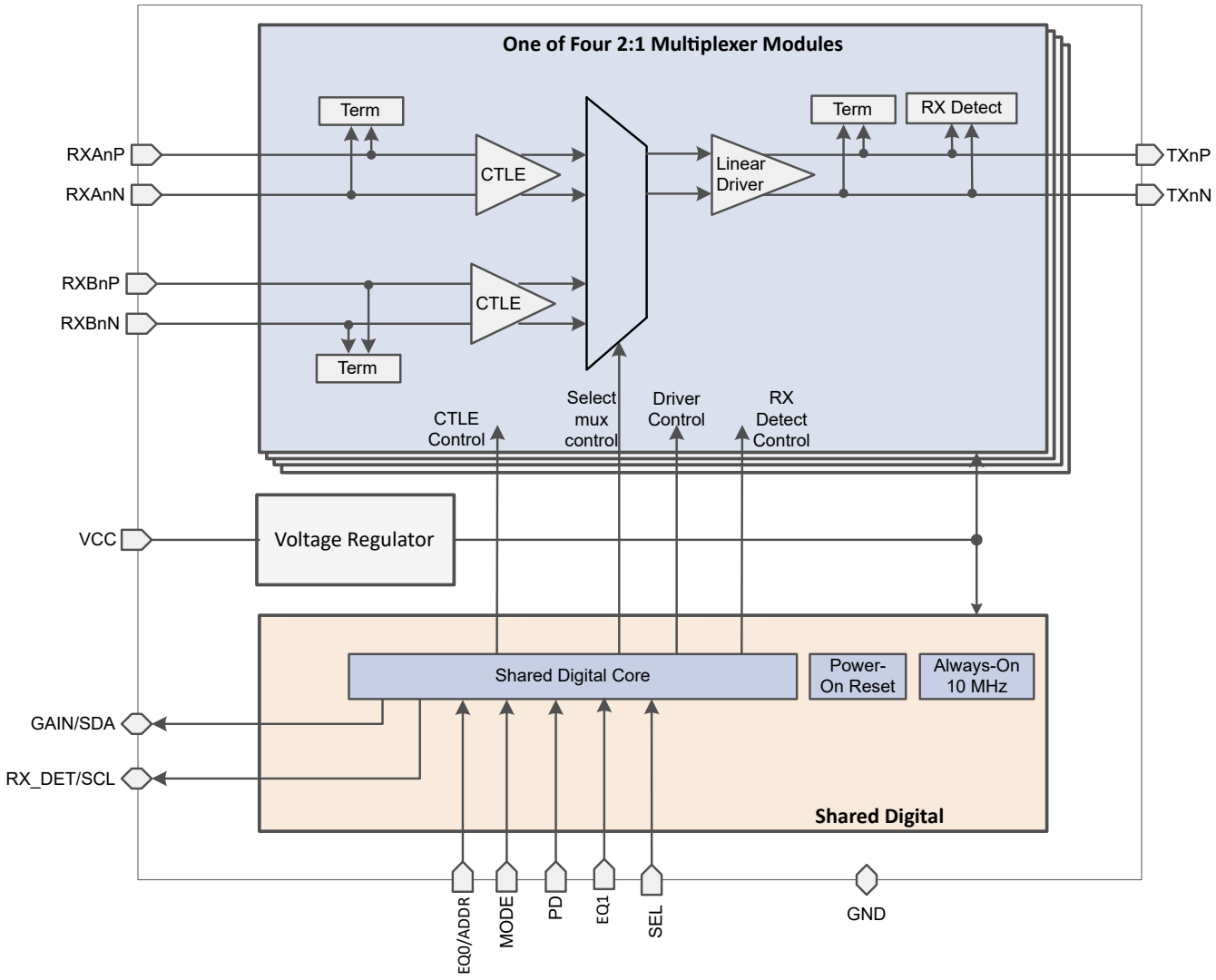
The signal channels of the SN75LVPE5421 operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping PCIe receiver's (either from Root Complex or Endpoint) equalization effective.

The SN75LVPE5421 can be configured in two different ways:

Pin Mode – device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I^{2}C Secondary Mode – provides most flexibility. Requires an external SMBus/I^{2}C primary device to configure SN75LVPE5421 though writing to its secondary address.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Five-Level Control Inputs

The SN75LVPE5421 has five 5-level inputs pins (EQ1, EQ0, GAIN, MODE, and RX_DET) that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The EQ0, EQ1, GAIN, and RX_DET pins are sampled at power-up only. The MODE pin can be exercised at device power up or in normal operation mode.

表 6-1. 5-Level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L4	F (Float)

6.3.2 Linear Equalization

The SN75LVPE5421 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of a passive channel. The receivers implement two stage linear equalizer for wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications of mid-frequency boost for best EQ gain profile match with wide range of channel media characteristics. The EQ profile control feature is only available in SMBus/I^{2}C Mode. In Pin Mode the settings are optimized for FR4 traces.

表 6-2 shows available equalization boost through EQ control pins or SMBus/I^{2}C registers. In Pin Control mode EQ1 and EQ0 pins set equalization boost for all channels. In I^{2}C Mode individual channels can be independently programmed for EQ boost.

表 6-2. Equalization Control Settings

EQUALIZATION SETTING							TYPICAL EQ BOOST (dB)	
	Pin Mode		SMBus/I^{2}C Mode					
EQ INDEX	EQ1	EQ0	eq_stage1_3:0	eq_stage2_2:0	eq_profile_3:0	eq_stage1_bypass	At 8 GHz	At 16 GHz
0	L0	L0	0	0	0	1	2.0	4.0
1	L0	L1	1	0	0	1	4.0	6.0
2	L0	L2	3	0	0	1	5.0	8.0
3	L0	L3	7	0	0	1	7.0	10.0
4	L0	L4	7	1	0	1	8.0	12.0
5	L1	L0	0	0	1	0	7.0	12.0
6	L1	L1	1	0	1	0	7.5	13.0
7	L1	L2	2	0	1	0	8.0	14.0
8	L1	L3	3	0	3	0	9.0	15.0
9	L1	L4	4	0	3	0	10.0	15.5
10	L2	L0	5	1	7	0	10.5	16.0
11	L2	L1	6	1	7	0	11.0	17.0
12	L2	L2	8	1	7	0	12.0	17.5

表 6-2. Equalization Control Settings (続き)

EQUALIZATION SETTING							TYPICAL EQ BOOST (dB)	
EQ INDEX	Pin Mode		SMBus/I²C Mode				At 8 GHz	At 16 GHz
	EQ1	EQ0	eq_stage1_3:0	eq_stage2_2:0	eq_profile_3:0	eq_stage1_bypass		
13	L2	L3	10	1	7	0	12.5	18.5
14	L2	L4	10	2	15	0	13.0	19.0
15	L3	L0	11	3	15	0	14.0	20.0
16	L3	L1	12	4	15	0	15.0	21.0
17	L3	L2	13	5	15	0	16.0	22.0
18	L3	L3	14	6	15	0	16.5	23.0
19	L3	L4	15	7	15	0	17.0	24.0

6.3.3 Flat Gain

The GAIN pin can be used to set the overall datapath flat gain (broadband gain including high frequency) of the SN75LVPE5421 when the device is in Pin Mode. The pin GAIN sets the Flat-Gain for all channels. In I²C Mode each channel can be independently set. 表 6-3 shows flat gain control configuration settings. The default recommendation for most systems will be GAIN = L4 (float) that provides flat gain of 0dB.

The flat gain and equalization of the SN75LVPE5421 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

表 6-3. Flat Gain Configuration Settings

Pin Mode GAIN	I²C Mode flat_gain_2:0	Flat Gain
L0	0	−5.6dB
L1	1	−3.8dB
L2	3	−1.2dB
L3	7	+2.6dB
L4 (float)	5	+0.6dB (default recommendation)

6.3.4 Receiver Detect State Machine

The SN75LVPE5421 deploys an RX detect state machine that governs the RX detection cycle as defined in the PCI express specifications. At device power up or through manually triggered event using PD or SEL pin or writing to the relevant I²C/SMBus register, the redriver determines whether or not a valid PCI express termination is present at the far end of the link. The RX_DET pin of SN75LVPE5421 provides additional flexibility for system designers to appropriately set the device in desired mode according to 表 6-4. For the PCIe application the RX_DET pin can be left floating for default settings.

Note: power up ramp or PD/SEL event triggers RX detect for all four channels. In applications where SN75LVPE5421 channels are used for multiple PCIe links, the RX detect function can be performed for individual channels through writing in appropriate I²C/SMBus registers.

表 6-4. Receiver Detect State Machine Settings

PD	RX_DET	RX Common-mode Impedance	COMMENTS
L	L0	Always 50 Ω	PCI Express RX detection state machine is disabled. Recommended for non PCIe interface use case where the SN75LVPE5421 is used as buffer with equalization.

表 6-4. Receiver Detect State Machine Settings (続き)

PD	RX_DET	RX Common-mode Impedance	COMMENTS
L	L1	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 3 consecutive valid detections
L	L2	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 2 consecutive valid detections
L	L3	Pre Detect: Hi-Z Post Detect: 50 Ω.	Reserved
L	L4 (Float)	Pre Detect: Hi-Z Post Detect: 50 Ω.	TX polls every ≅150 µs until valid termination is detected. RX CM impedance held at Hi-Z until detection Reset by asserting PD high for 200 µs then low. Recommended default setting for PCIe.
H	X	Hi-Z	Reset Channels and set their RX impedance to Hi-Z

6.4 Device Functional Modes

6.4.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled by RX_DET = L4 (float). This mode is recommended for PCIe use cases. In this mode, the PD pin is driven low in a system (for example, by PCIe connector *PRSNT* signal). In this mode, the device redrives and equalizes PCIe RX or TX signals to provide better signal integrity.

6.4.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled by RX_DET = L0. This mode is recommended for non-PCIe use cases. In this mode, the device is working as a buffer to provide linear equalization to improve signal integrity.

6.4.3 Standby Mode

The device is in standby mode invoked by PD = H. In this mode, the device is in standby mode conserving power.

6.5 Programming

6.5.1 Pin Mode

The SN75LVPE5421 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 5-level pins for device control and signal integrity optimum settings.

6.5.2 SMBUS/I^{2}C Register Control Interface

If MODE = L2 (SMBus / I^{2}C secondary control mode), the SN75LVPE5421 is configured for best signal integrity through a standard I^{2}C or SMBus interface that may operate up to 400 kHz. The secondary address of the SN75LVPE5421 is determined by the pin strap settings on the ADDR and MODE pins. 表 6-5 provides the eight possible secondary addresses (7-bit) for each channel banks of the device. In SMBus/I^{2}C modes the SCL, SDA pins must be pulled up to a 3.3V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7kΩ is a good first approximation for a bus capacitance of 10pF.

表 6-5. SMBUS/I2C Secondary Address Settings

MODE	ADDR	7-bit Secondary Address Channels 0-1	7-bit Secondary Address Channels 2-3
L1	L0	0x18	0x19
L1	L1	0x1A	0x1B
L1	L2	0x1C	0x1D
L1	L3	0x1E	0x1F
X	L4	Reserved	Reserved
L2	L0	0x20	0x21
L2	L1	0x22	0x23

表 6-5. SMBUS/I2C Secondary Address Settings (続き)

MODE	ADDR	7-bit Secondary Address Channels 0-1	7-bit Secondary Address Channels 2-3
L2	L2	0x24	0x25
L2	L3	0x26	0x27

The SN75LVPE5421 has two types of registers:

- **Shared Registers:** These registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers:** These registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group through broadcast writes to Bank 0 or Bank 1.

The SN75LVPE5421 features two banks of channels, Bank 0 (Channels 0-1) and Bank 1 (Channels 2-), each featuring a separate register set and requiring a unique SMBus secondary address.

Channel Registers Base Address	Channel Bank 0 Access	Channel Bank 1 Access
0x00	Channel 0 registers	Channel 2 registers
0x20	Channel 0 registers	Channel 2 registers
0x40	Channel 1 registers	Channel 3 registers
0x60	Channel 1 registers	Channel 3 registers
0x80	Broadcast write channel Bank 0 registers, read channel 0 registers	Broadcast write channel Bank 1 registers, read channel 2 registers
0xE0	Bank 0 Share registers	Bank 1 Share registers

6.5.2.1 Shared Registers

表 6-6. General Registers (Offset = 0xE2)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device reset control: Reset all I2C registers to default values (self-clearing).
5	rst_i2c_mas	R/W/SC	0x0	Reset I^2C Primary (self-clearing).
4-0	RESERVED	R	0x0000	Reserved

表 6-7. DEVICE_ID0 Register (Offset = 0xF0)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0001	Reserved
3	device_id0_3	R	0x1	Device ID0 [3:1]: 101
2	device_id0_2	R	0x0	see MSB
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	X	Reserved

表 6-8. *DEVICE_ID1 Register (Offset = 0xF1)*

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1000: SN75LVPE5421
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB

表 6-8. *DEVICE_ID1 Register (Offset = 0xF1)* (続き)

Bit	Field	Type	Reset	Description
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x1	see MSB

6.5.2.2 Channel Registers

表 6-9. RX Detect Status Register (Channel Register Base + Offset = 0x00)

Bit	Field	Type	Reset	Description
7	RX_det_comp_p	R	0x0	RX Detect positive data pin status: 0: Not detected 1: Detected – the value is latched
6	RX_det_comp_n	R	0x0	RX Detect negative data pin status: 0: Not detected 1: Detected – the value is latched
5-0	RESERVED	R	0x0	Reserved

表 6-10. EQ Gain Control Register (Channel Register Base + Offset = 0x01)

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ stage 1 bypass: 0: Bypass disabled 1: Bypass enabled
6	eq_stage1_3	R/W	0x0	EQBoost stage 1 control See 表 6-2 for details
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost stage 2 control See 表 6-2 for details
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

表 6-11. EQ Gain / Flat Gain Control Register (Channel Register Base + Offset = 0x03)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile See 表 6-2 for details
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat gain select: See 表 6-3 for details
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

表 6-12. RX Detect Control Register (Channel Register Base + Offset = 0x04)

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2	mr_RX_det_man	R/W	0x0	Manual override of RX_detect_p/n decision: 0: RX detect state machine is enabled 1: RX detect state machine is overridden – always valid RX termination detected
1	en_RX_det_count	R/W	0x0	Enable additional RX detect polling 0: Additional RX detect polling disabled 1: Additional RX detect polling enabled

表 6-12. RX Detect Control Register (Channel Register Base + Offset = 0x04) (続き)

Bit	Field	Type	Reset	Description
0	sel_RX_det_count	R/W	0x0	Select number of valid RX detect polls – gated by en_RX_det_count = 1 0: Device transmitters poll until 2 consecutive valid detections 1: Device transmitters poll until 3 consecutive valid detections

表 6-13. PD Override Register (Channel Register Base + Offset = 0x05)

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides through SMBus/I^2C 0: Manual override disabled 1: Manual override enabled
6-0	device_en	R/W	0x111111	Manual power down of redriver various blocks – gated by device_en_override = 1 111111: All blocks are enabled 000000: All blocks are disabled

表 6-14. RX Detect Reset Register (Channel Register Base + Offset = 0x0A)

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2	mr_RX_det_rst	R/W	0x0	RX Detect state machine reset. Toggle the bit if RX Detect machine needs to be reset in I^2C mode 0: state machine is not reset 1: RX detect state machine is reset
1-0	RESERVED	R/W	0x0	Reserved

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The SN75LVPE5421 is a high-speed linear repeater with integrated mux. The device extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

7.2 Typical Applications

The SN75LVPE5421 is a PCI Express linear redriver that can also be configured as interface agnostic redriver by disabling its RX detect feature. The device can be used in a wide range of interfaces including:

- PCI Express
- Ultra Path Interconnect (UPI)
- SATA
- SAS
- DisplayPort

7.2.1 PCIe x8 Lane Switching

The SN75LVPE5412 and SN75LVPE5421 can be used to switch PCIe lanes from a CPU into one of the two PCIe CEM connectors. 図 7-1 shows a simplified schematic for the following configuration:

- Two SN75LVPE5412 demultiplex eight TX channels from the CPU into one of the two PCIe slots.
- Two SN75LVPE5421 multiplex eight RX channels from one of the two PCIe slots to CPU.

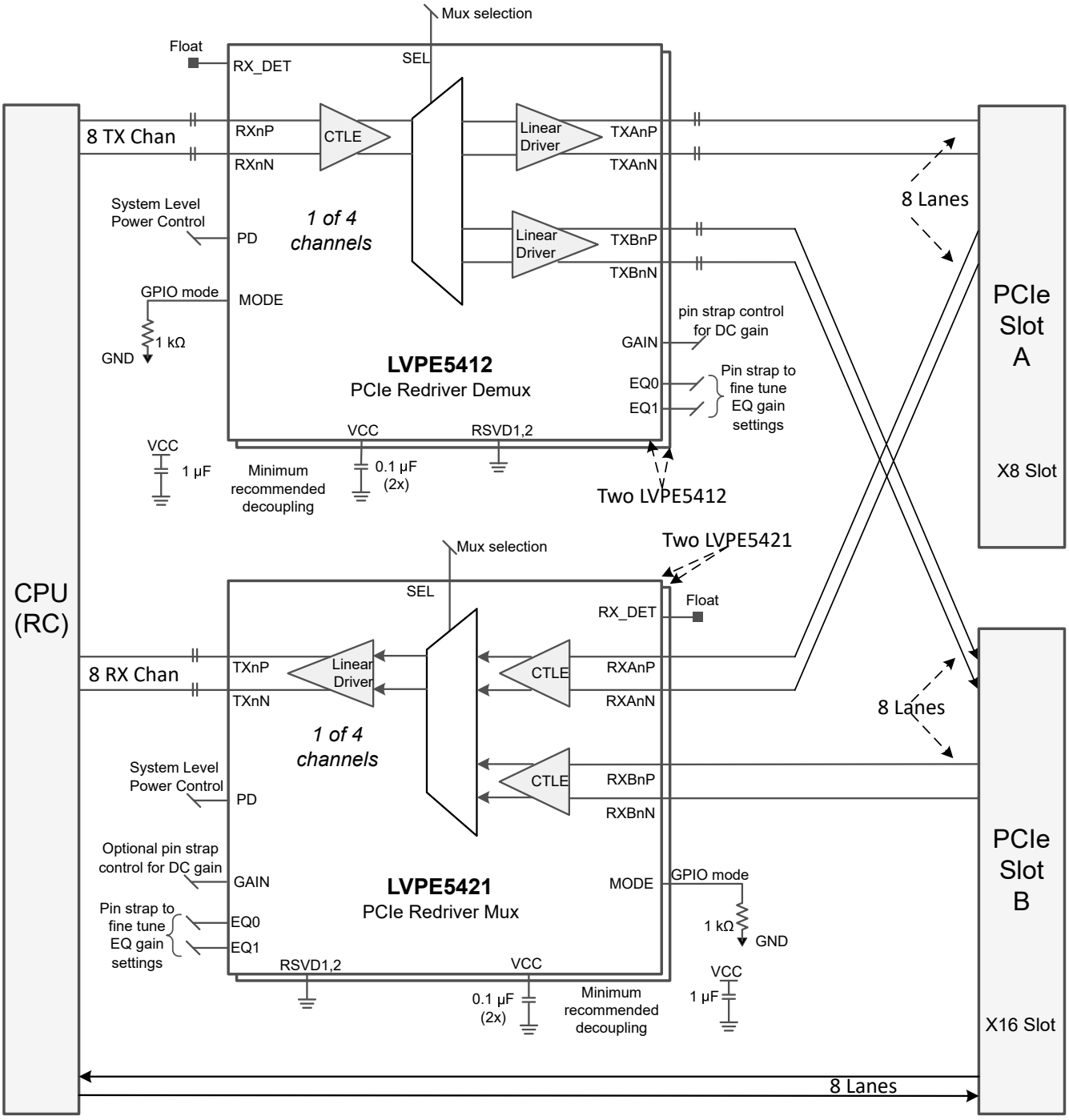


図 7-1. Simplified Schematic for PCIe Lane Switching

7.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design:

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-ended segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- For Gen 3.0, 4.0, and 5.0, AC-coupling capacitors of 220 nF are recommended, set the maximum body size to 0402, and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

7.2.1.2 Detailed Design Procedure

In PCIe Gen 3.0, 4.0, and 5.0 applications, the specification requires RX-TX link training to establish and optimize signal conditioning settings at 8.0, 16.0, and 32.0Gbps, respectively. In link training, the RX partner requests a series of FIR – pre-shoot and de-emphasis coefficients (10 presets) from the TX partner. The RX partner includes CTLE and DFE. The link training would pre-condition the signal, with an equalized link between the Root Complex and Endpoint.

Note: there is no link training in PCIe Gen 1.0 (2.5Gbps) or PCIe Gen 2.0 (5.0Gbps) applications. The SN75LVPE5421 is placed in between the TX and RX. It helps extend the PCB trace reach distance by boosting the attenuated signals with its equalization, which allows the user to recover the signal by the downstream RX more easily.

For operation in Gen 5.0, 4.0, and 3.0 links, the SN75LVPE5421 transmit outputs are designed to pass the TX Preset signaling onto the RX for the PCIe Gen 5.0, 4.0, and 3.0 link to train and optimize the equalization settings. The suggested setting for the device is GAIN = L4 (default). Adjustments to the EQ setting should be performed based on the channel loss to optimize the eye opening in the RX partner. The TX equalization presets or CTLE and DFE coefficients in the RX can also be adjusted to further improve the eye opening.

7.2.2 Protocol Agnostic Linear Redriver for High Speed Interfaces

The SN75LVPE5421 can be used as a four channel protocol agnostic linear redriver multiplexer (mux) for data rates up to 32Gbps. To use the device in a non-PCIe application, the RX_DET pin must be pin-strapped to GND with 1kΩ resistor (L0).

This section explains how the SN75LVPE5421 can be used in DisplayPort (DP) application. The device is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the device. The redriver becomes part of the electrical channel along with passive traces, cables, and so forth, resulting in optimum source and sink parameters for best electrical link.

図 7-2 shows a simplified schematic for DisplayPort multiplexing application using SN75LVPE5421. Auxiliary and Hot plug detect (HPD) are muxed outside of the device. If system use case requires implementing DP power states, then the device must be controlled by the I^2C.

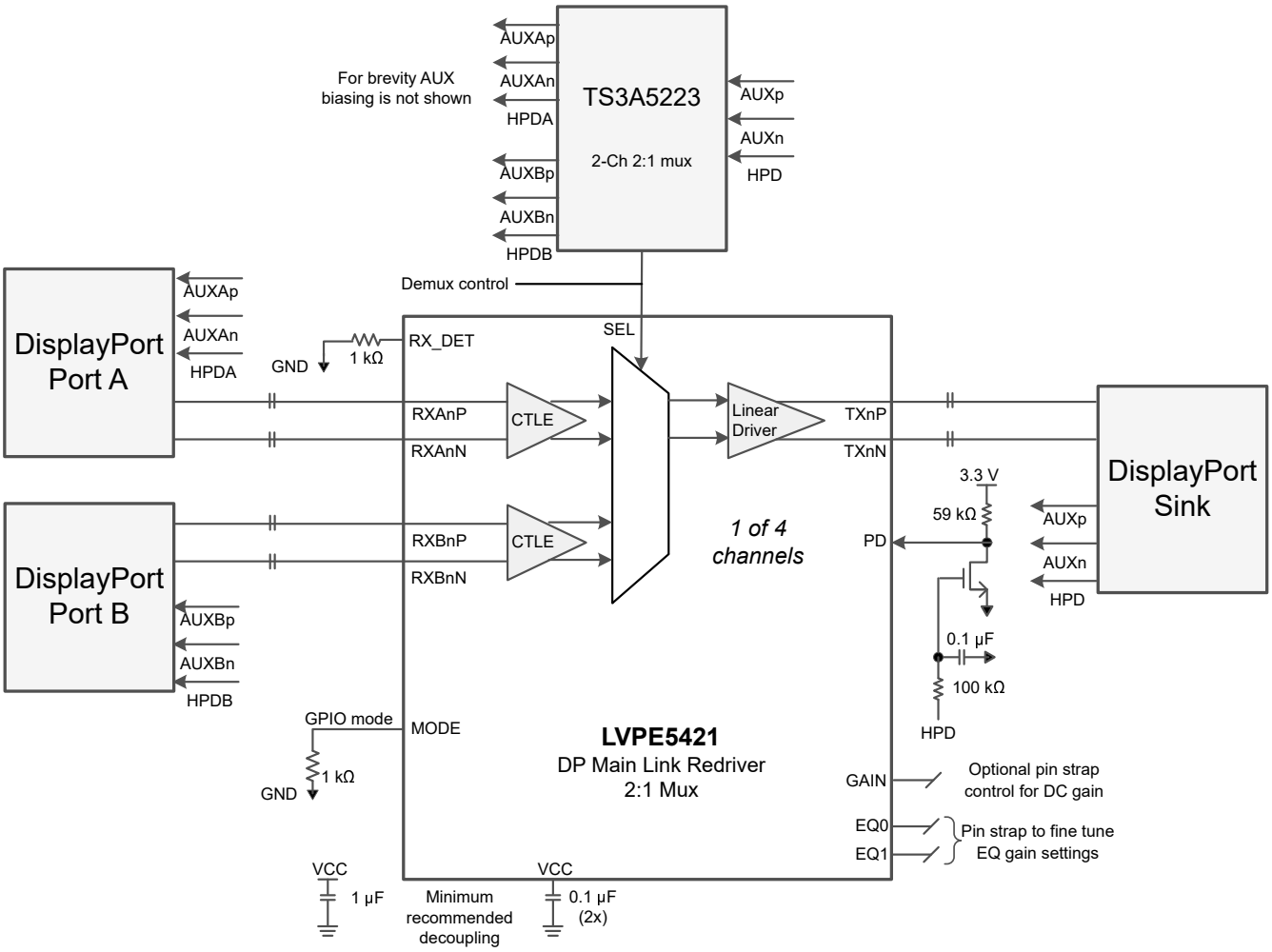


図 7-2. Simplified Schematic for DisplayPort Multiplexer Application

The inverted DisplayPort HPD signal can be used to put the device into standby mode by using its PD pin. Note: in a DisplayPort link a sink can use HPD line to create an interrupt for its link partner source. If HPD signal is used for power management, then an RC filter must be installed to filter out HPD interrupt signals.

The SN75LVPE5421 can similarly be used for other AC-coupled high speed interfaces. Care must be taken to understand the specifications of the interface to ensure feasibility.

7.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The SN75LVPE5421 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 µF capacitor per VCC pin, one 1.0 µF bulk capacitor per device, and one 10 µF bulk capacitor per power bus that delivers power to one or more devices. The local decoupling (0.1 µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the device ground pad.

7.4 Layout

7.4.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most or all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

7.4.2 Layout Example

図 7-3 shows SN75LVPE5421 layout example.

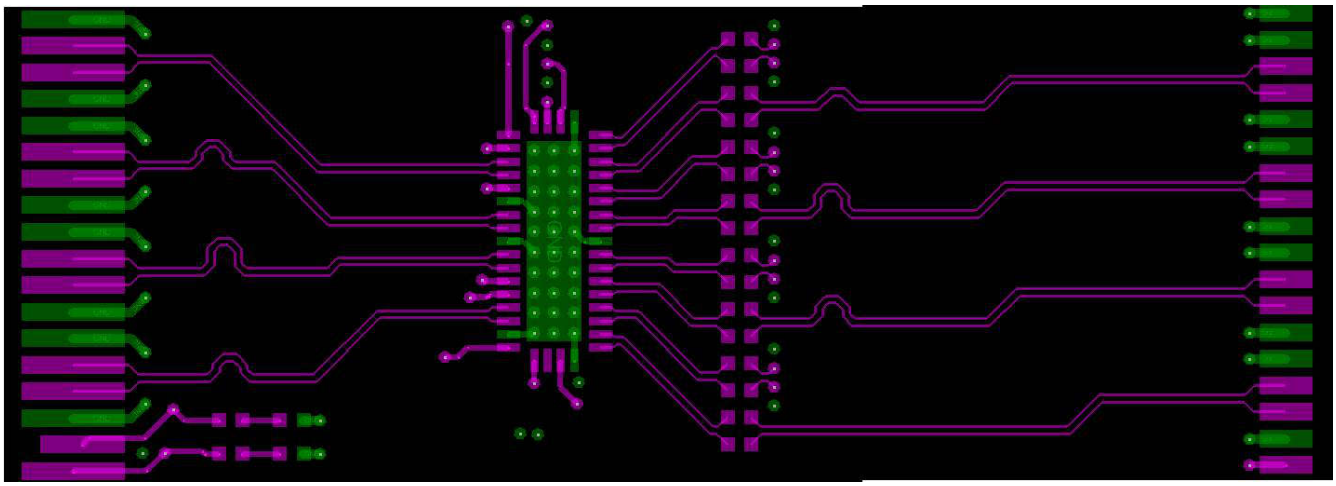


図 7-3. SN75LVPE5421 Layout Example

図 7-4 shows a layout illustration where two SN75LVPE5412 and two SN75LVPE5421 are used to switch 8 lanes between the two PCIe slots.

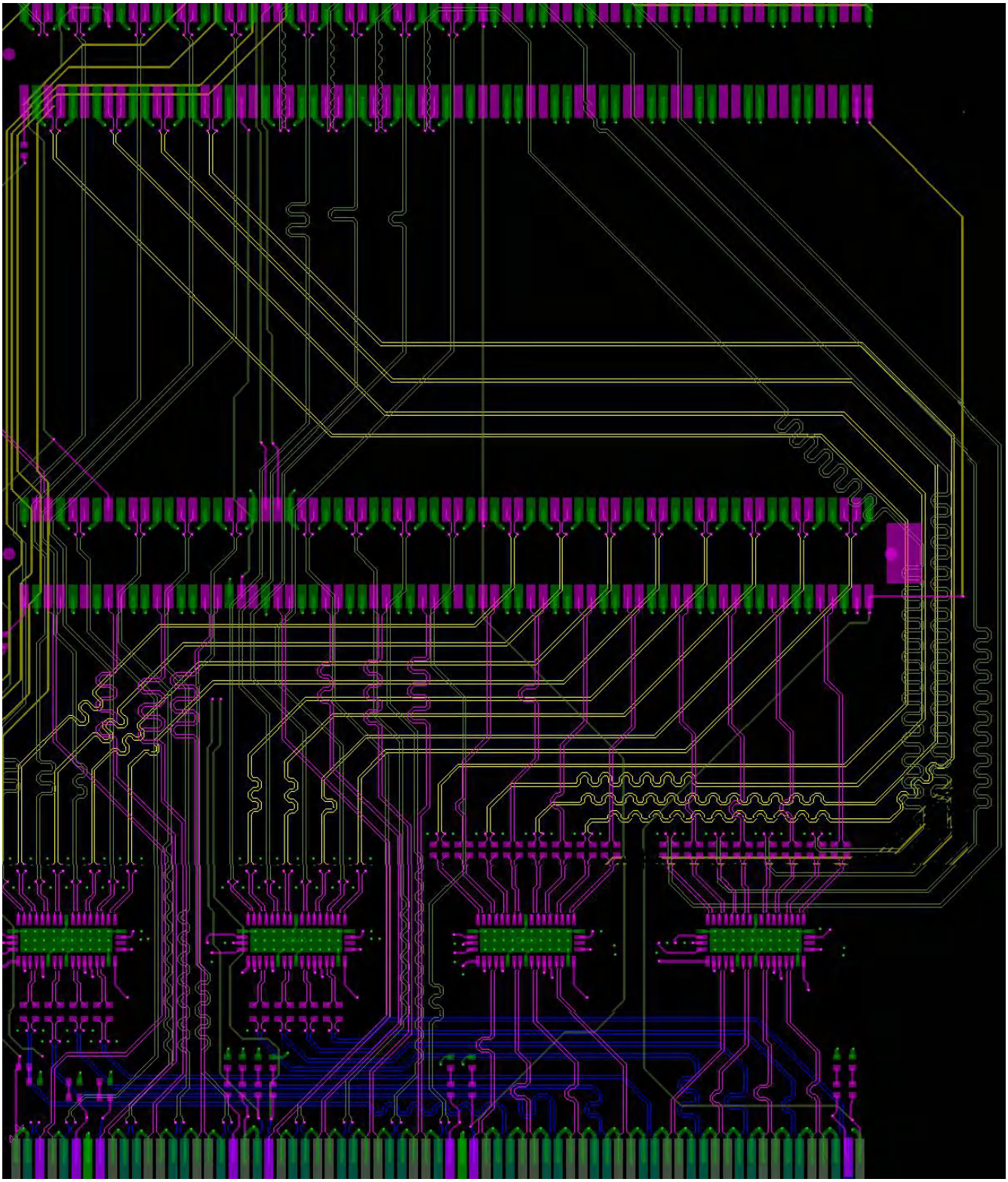


図 7-4. Layout Example for PCIe Lane Muxing Application

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2022) to Revision B (December 2023)	Page
• Changed operating ambient temperature from: *0 to 85°C* to: *-40 to 85°C*	6

Changes from Revision * (December 2021) to Revision A (October 2022)	Page
• Changed the *Reset* value for the 7-4 Bit in the *DEVICE_ID0 Register (Offset = 0xF0)* table	16

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVPE5421RUAR	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	5PR421
SN75LVPE5421RUAT	Active	Production	WQFN (RUA) | 42	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	5PR421

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

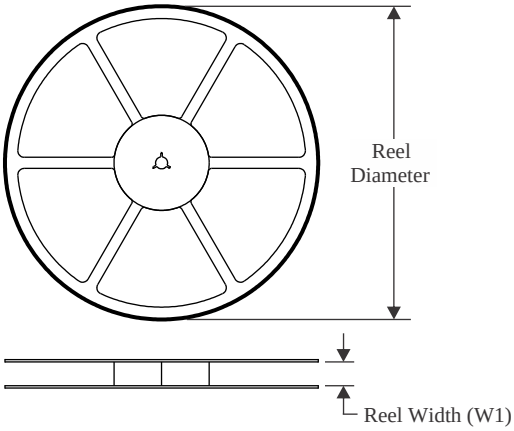
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

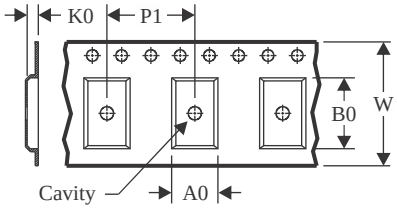
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

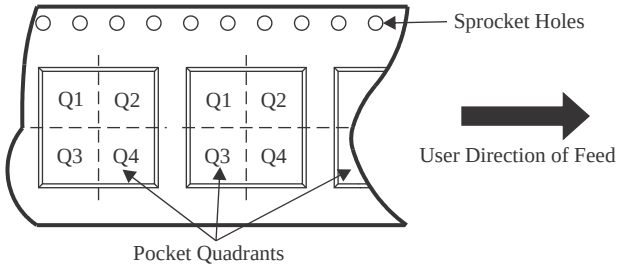


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

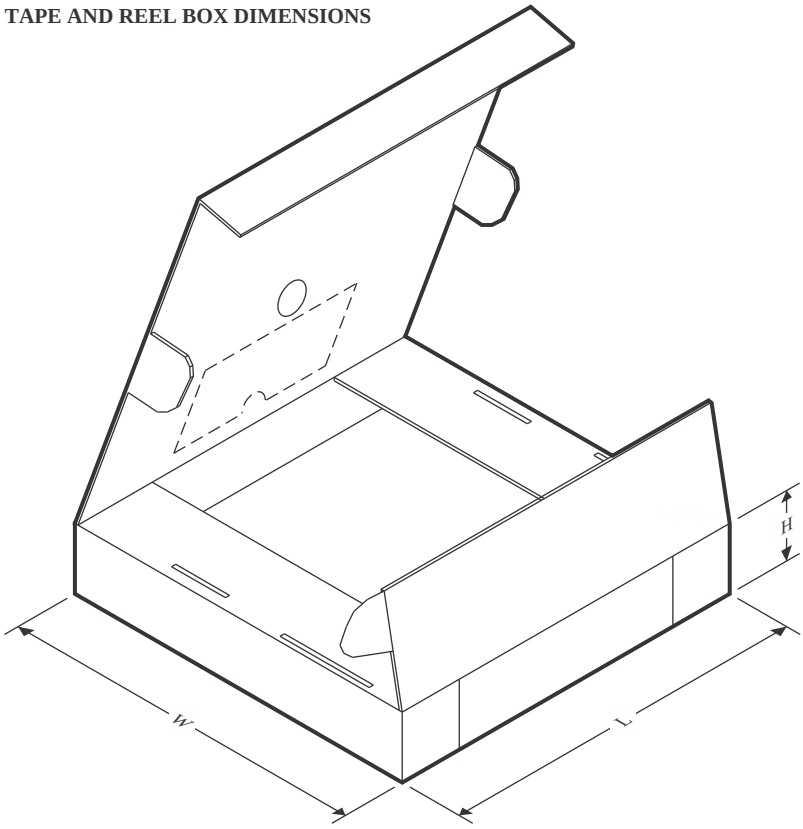
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVPE5421RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
SN75LVPE5421RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVPE5421RUAR	WQFN	RUA	42	3000	367.0	367.0	35.0
SN75LVPE5421RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

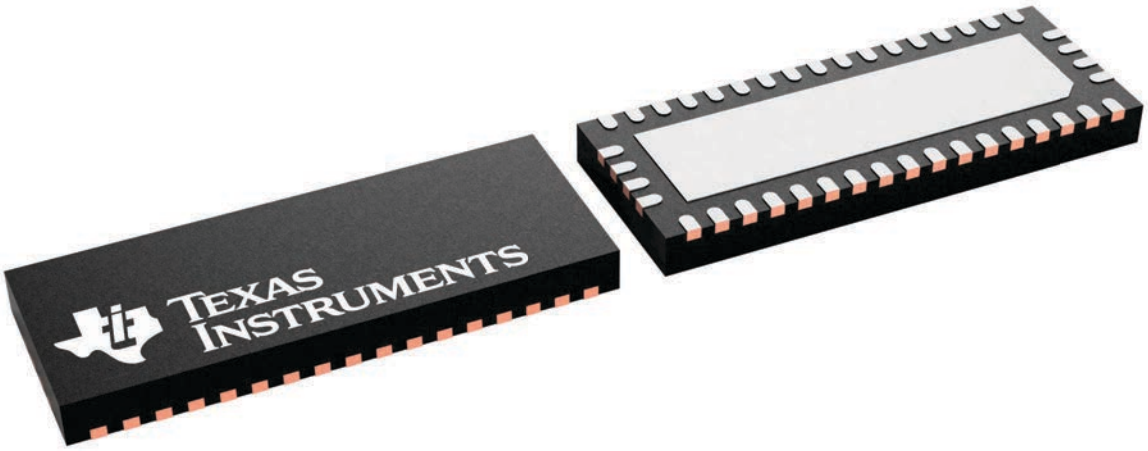
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

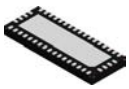
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A

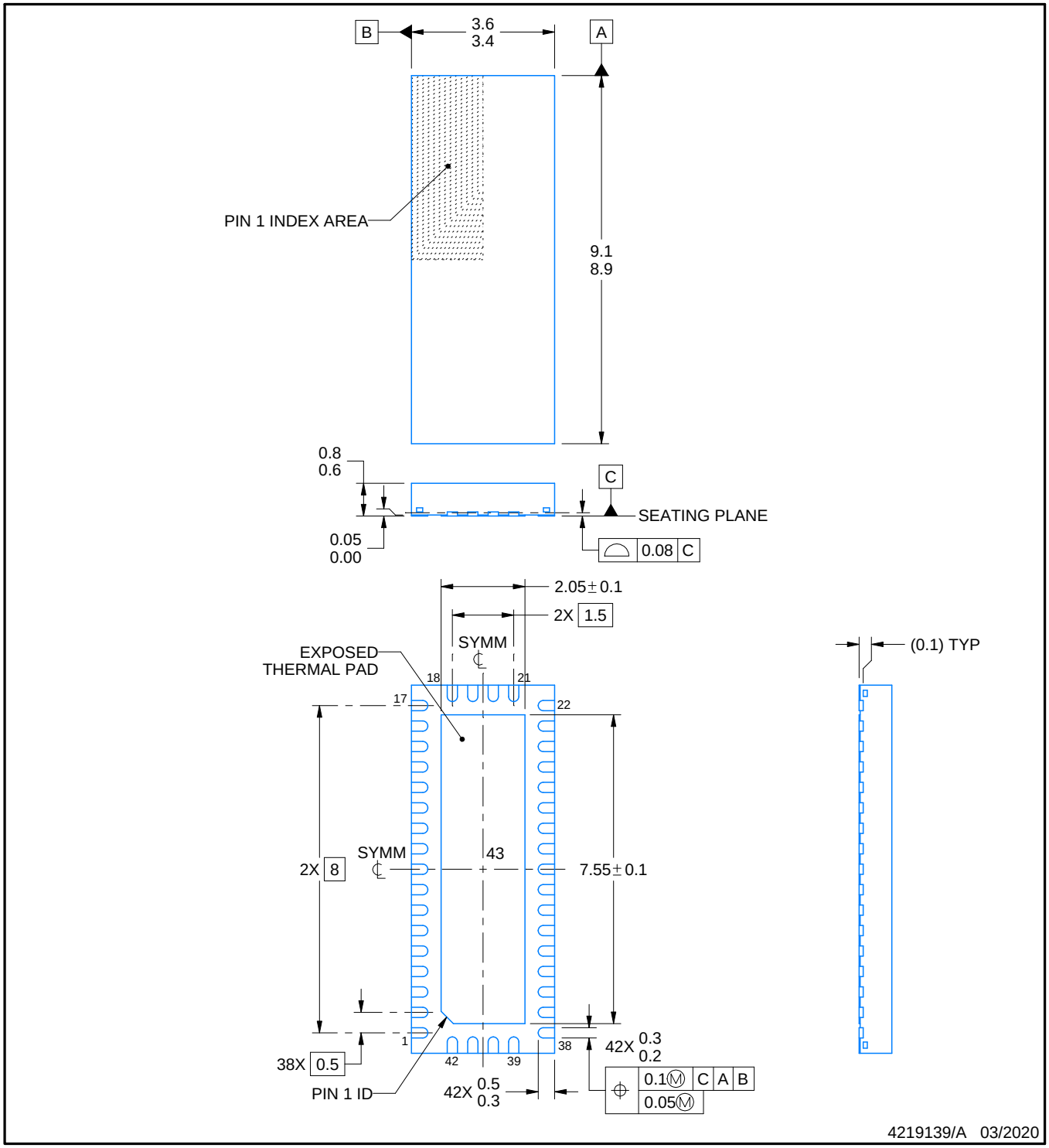
PACKAGE OUTLINE

RUA0042A



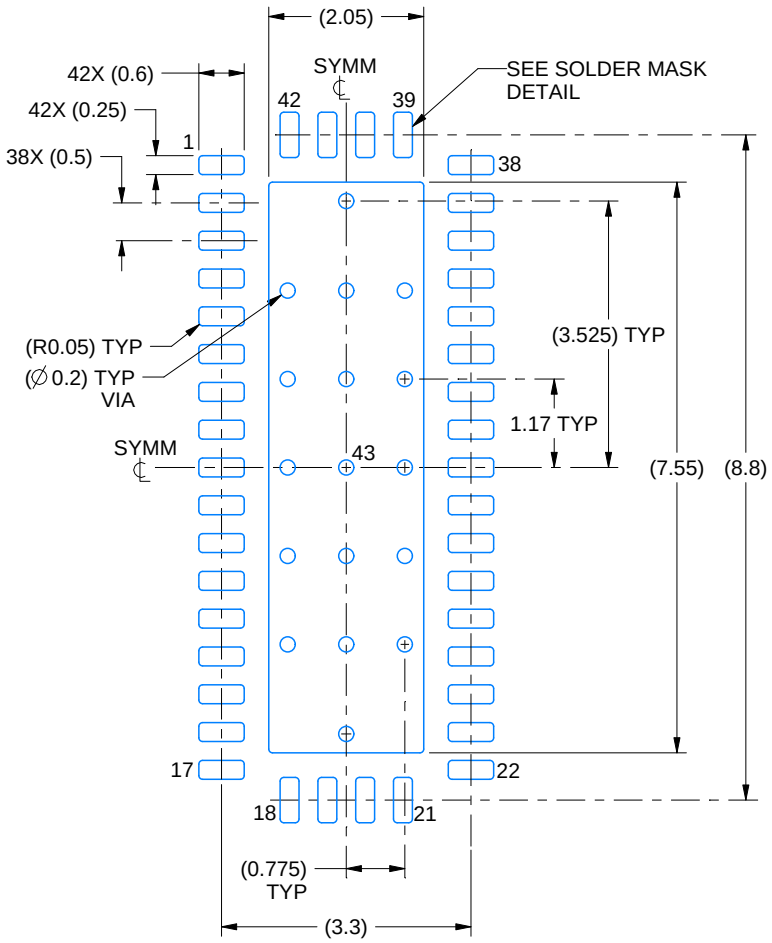
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

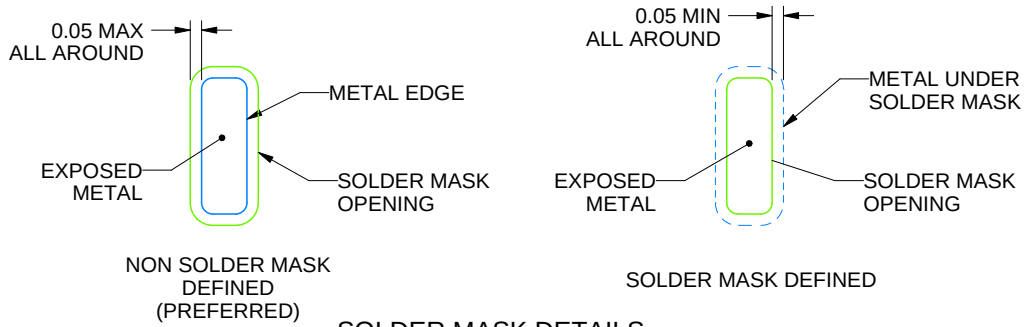


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

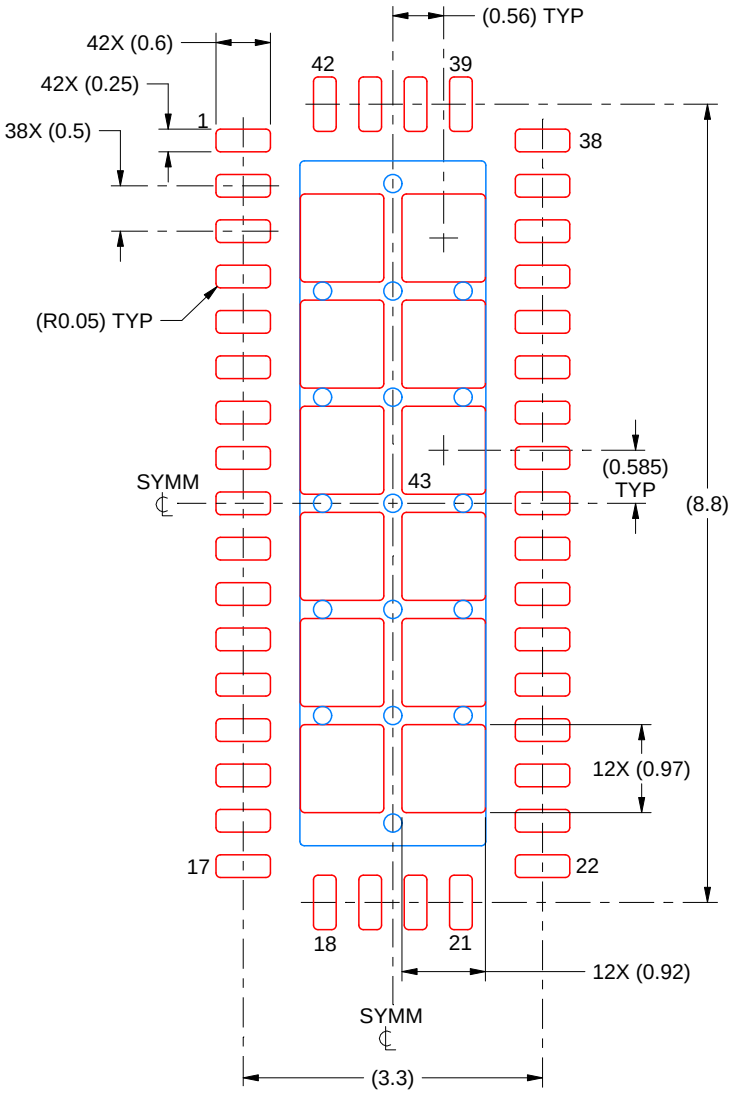
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月