TAS5815 96kHz の拡張処理機能搭載、30W、デジタル入力、ステレオ、閉ループ Class-D オーディオ アンプ

1 特長

- 複数の出力構成をサポート
  - 2.0 モードで 2 × 30W (6Ω、21V、THD+N=1%)
  - モノラル モードで 58W (3Ω、21V、THD+N=1%)
- 優れたオーディオ性能:
  - THD+N ≦ 0.03% (1W、1kHz、PVDD = 12V)
  - SNR ≥ 110dB (A-weighted)、ICN ≤ 45μVRMS
- 効率的な Class-D 動作:
  - 90% を超える電力効率、120mΩ の $R_{DS(on)}$
- 柔軟な電源構成
  - PVDD:4.5V～26.4V
  - DVDD および I/O:1.8V または 3.3V
- 柔軟なオーディオ I/O:
  - 32、44.1、48、88.2、96kHz のサンプル レートをサポート
  - I^2S、LJ、RJ、TDM
  - SDOUT によるオーディオ モニタ、サブチャネル、エコー キャンセル
  - 3 線式のデジタル オーディオ インターフェイスをサポート (MCLK 不要)
  - ステレオのブリッジ結合またはモノラルの並列ブリッジ結合の負荷をサポート (BTL および PBTL)
  - 8 ステップの Class-H DC/DC 制御をサポート。
- 高度なオーディオ処理:
  - サンプル レート コンバータ
  - 96kHz プロセッサ サンプリング
  - DC ブロッキング、2 ×15 BQ、DPEQ、THD マネージャ
  - 2 バンドの 4 次 DRC + AGL
  - 過熱フォールドバック
  - 8 つの Class-H DC/DC 制御ステップは、48k のサンプル レートにおいて、BTL モードで 2.5ms、PBTL モードで 5ms のルック アヘッド バッファを備えています。
- 優れた自己保護機能を内蔵:
  - 過電流エラー (OCE)
  - 過熱警告 (OTW)
  - 過熱エラー (OTE)
  - 低電圧または過電圧誤動作防止 (UVLO/OVLO)
- システム統合が簡単
  - I^2C ソフトウェア制御
  - ソリューション サイズの低減
    - 開ループ デバイスと比べて必要なパッシブ部品数が減少
    - 最新の EMI テクノロジーによる超低 EMI
    - ほとんどのアプリケーションで大きなインダクタが不要

2 アプリケーション

- サウンドバー、PC オーディオ
- ワイヤレス、Bluetooth スピーカー
- DTV、HDTV、UHD、および汎用モニタ

3 概要

TAS5815 は、高効率のデジタル入力 Class-D オーディオ アンプで、最大 96kHz 対応アーキテクチャのオーディオ プロセッサ、出力電力に基づく適応変調方式、低 $R_{DS(on)}$ = 120mΩ を内蔵しています。また、DPEQ プロセスもサポートしており、簡単にチューニングできます。

DPEQ を使用して、2 つの信号パス (Low レベルと High レベル) 経由でオーディオ信号をミキシングします。これら 2 つのパスは、別々のイコライゼーション プロパティで使用されます。3 番目のパスは、受信オーディオを監視し、これら 2 つの 部品間の スレッショルドとミキシング特性を決定します。したがって、2 つの High レベルと Low レベルのチャネル間のミキシングは動的性質であり、受信オーディオに依存します。

高性能の閉ループ アーキテクチャと広いスイッチング周波数範囲により、ほとんどのアプリケーションで受動部品を減らしインダクタのサイズを最小化することで、ソリューションのサイズを縮小できます。TAS5815 にはオーディオ プロセッサが内蔵されており、アーキテクチャで最高 96kHz に対応し、高度なプロセス フローをサポートしています。デバイスには、Class-H と呼ばれる独自のアルゴリズムが内蔵されています。Class-H アルゴリズムは、予測されるオーディオ電力の需要を検出し、フィードバック ピン (FB) により、前段の DC-DC コンバータに PWM 制御信号を出力します。この機能を使用して、システム レベルの効率を高め、総消費電力を削減します。TAS5815 は、オーディオ信号を先読みしてオーディオ クリッピング歪みを防止するために最大 2.5ms の遅延バッファをサポートしています。

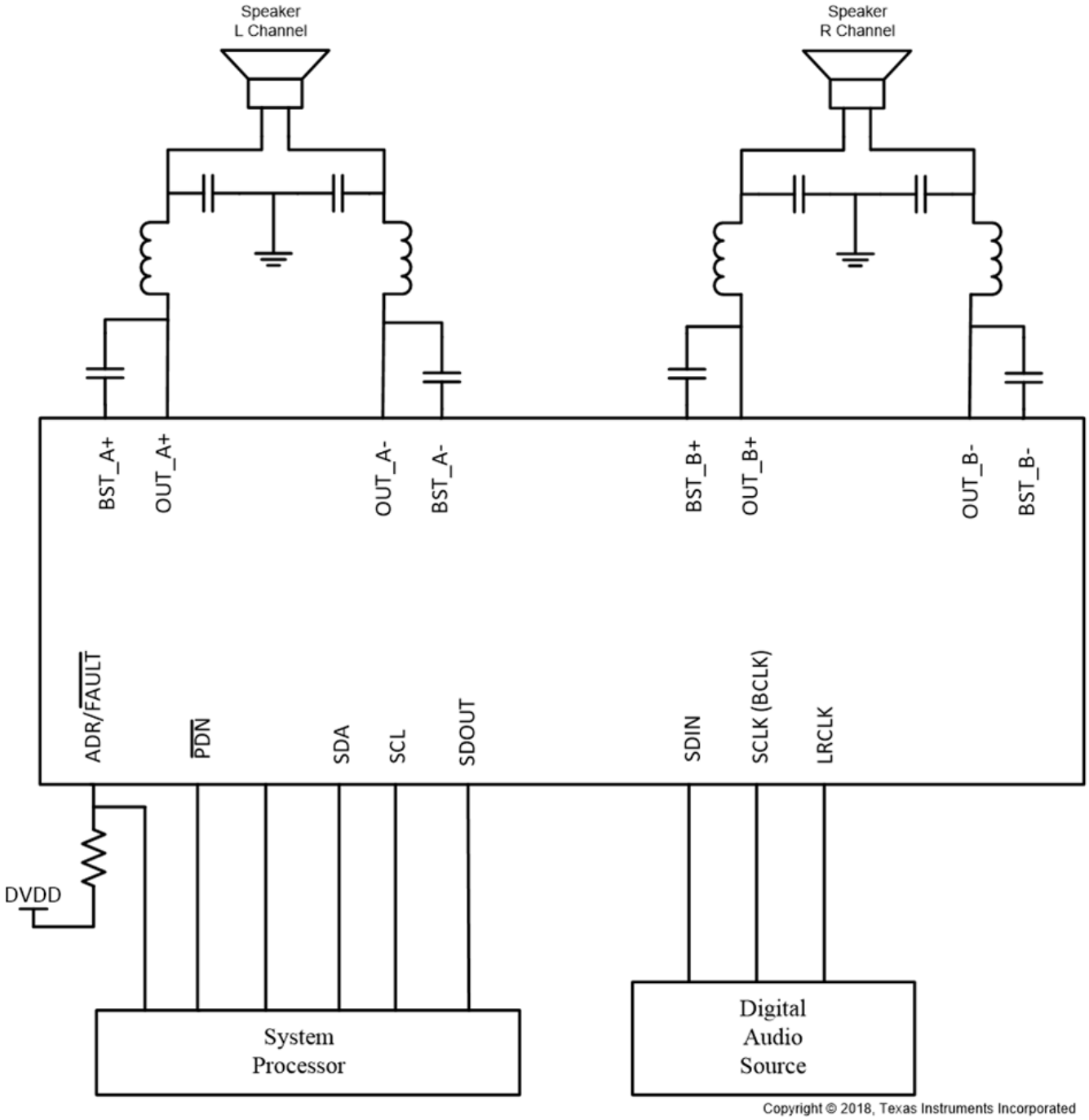
また、このデバイスは、スピーカ負荷の開放 / 短絡検出と、レジスタ レポートによるレポート検出結果をサポートしています。

製品情報

部品番号	パッケージ(1)	パッケージ サイズ(2)	本体サイズ (公称)
TAS5815PWP	TSSOP (28) PWP	9.70mm × 6.40mm	9.70mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます



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Device Comparison Table

Part Number	Recommended PVDD Range	$R_{DS(ON)}$ Option	Package	Class-H Algorithm Integrated
TAS5815	4.5V to 26.4V	120mΩ	TSSOP28(PWP)	Yes
TAS5802	4.5V to 20V	120mΩ	TSSOP28(PWP)	No
TAS5827	4.5V to 26.4V	70mΩ	QFN32(RHB)	Yes
TAS5825P	4.5V to 26.4V	90mΩ	QFN32(RHB)	Yes
TAS5828M	4.5V to 26.4V	90mΩ	TSSOP32(DAD)	Yes
TAS5822M	4.5V to 26.4V	90mΩ	HTSSOP38(DCP)	No
TAS5806M	4.5V to 26.4V	180mΩ	TSSOP38(DCP)	No
TAS5805M	4.5V to 26.4V	180mΩ	TSSOP28(PWP)	No

4 Pin Configuration and Functions

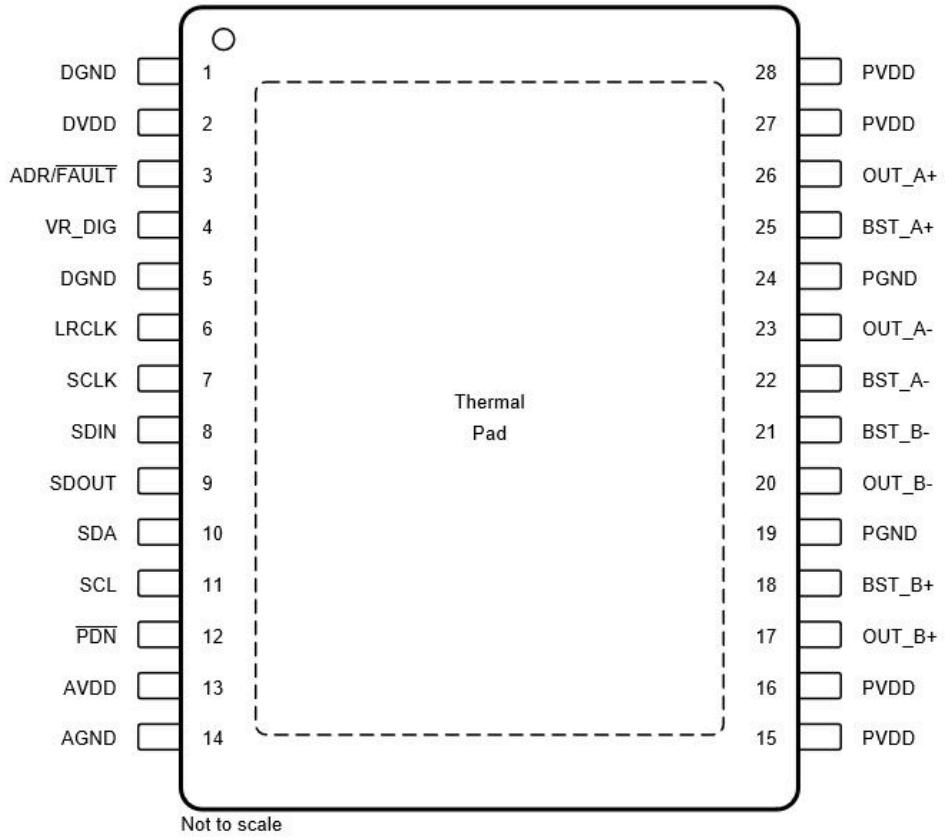


図 4-1. PWP (TSSOP) Package, 28-Pin PadDown, Top View

表 4-1. Pin Functions For TSSOP28 Package

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	DGND	P	Digital ground
2	DVDD	P	3.3-V/1.8-V digital power supply
3	ADR/FAULT	DI/O	A table of resistor value (Pull up/Down to DVDD/GND) will decide device I2C address. After power up, this pin can be programmed by writing 1 to a register bit after Power up bit. In this mode, ADR/ FAULT is redefine as FAULT.

表 4-1. Pin Functions For TSSOP28 Package (続き)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
4	VR_DIG	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices
5	DGND	P	Digital ground
6	LRCLK	DI	Input serial audio data left/right clock (sample rate clock)
7	SCLK	DI	Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
8	SDIN	DI	Serial audio data input. SDIN supports three discrete (stereo) data formats
9	SDOUT	DO	Serail audio data output, the source data can select as Pre-DSP or Post-DSP.
10	SDA	DI/O	I2C serial control data interface input/output
11	SCL	DI	I2C serial control clock input
12	$\overline{\text{PDN}}$	DI	Power down, active-low. $\overline{\text{PDN}}$ sets the amplifier in Shutdown, turn off all internal regulators.
13	AVDD	P	Internally regulated 5 V analog power voltage. This pin must not be used to drive external devices.
14	AGND	G	Analog ground
15	PVDD	P	PVDD voltage input
16	PVDD	P	PVDD voltage input
17	OUT_B+	PO	Positive pin for differential speaker amplifier output B+
18	BST_B+	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
19	PGND	G	Ground reference for power device circuitry. Connect this pin to system ground
20	OUT_B-	NO	Negative pin for differential speaker amplifier output B-
21	BST_B-	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
22	BST_A-	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
23	OUT_A-	NO	Negative pin for differential speaker amplifier output A-
24	PGND	G	Ground reference for power device circuitry. Connect this pin to system ground
25	BST_A+	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
26	OUT_A+	PO	Positive pin for differential speaker amplifier output A+
27	PVDD	P	PVDD voltage input
28	PVDD	P	PVDD voltage input
	PowerPAD™	G	Ground, connect to grounded heat sink for best system performance.

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), PO = Positive output, NO = Negative output, P = Power, G = Ground (0 V)

5 Specifications

5.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	30	V
$V_{I(DigIn)}$	DVDD referenced digital inputs(2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK\_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
T_A	Ambient operating temperature,	–40	85	°C
T_J	Operating junction temperature	-40	160	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SDIN, SDOUT, SCL, SDA, $\overline{\text{PDN}}$

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	DVDD	1.62		3.63	V
		PVDD	4.5		26.4	V
$V_{IH(DigIn)}$	Input logic high for DVDD referenced digital inputs		0.9 × V_{DVDD}		DVDD	V
$V_{IL(DigIn)}$	Input logic low for DVDD referenced digital inputs				0.1 × V_{DVDD}	V
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1			µH

5.4 Thermal Information

THERMAL METRIC(1)		TAS5815M TSSOP28 (PWP) 28 PINS JEDEC STANDARD 4-LAYER PCB	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)}$ = V_{DVDD}			10	uA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)}$ = 0 V			–10	uA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	I_{OH} = 4 mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	I_{OH} = –4 mA			20%	V_{DVDD}
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required LRCLK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		96	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
AMPLIFIER OPERATING MODE AND DC PRAMETERS						
t_{off}	Turn-off Time	Excluding volume ramp			10	ms
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD Measured at 0 dB input(1FS)			29.4	dBV
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain = 26.4 dBV		0.5		dB
f_{SPK_AMP}	Switching frequency of the speaker amplifier			384		kHz
f_{SPK_AMP}	Switching frequency of the speaker amplifier			768		kHz
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization. V_{PVDD}=24 V, $I_{(OUT)}$=500 mA, T_J=25 ℃		120		mΩ
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold	OUTxx Overcurrent Error Threshold	6	7		A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold condition		3.7	4	4.2	V
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold		27	28.1	29.2	V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		1.9		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		570		ms
OTE_{THRES}	Over temperature error threshold			160		℃
$OTE_{Hystersis}$	Over temperature error hysteresis			10		℃

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit3		135		°C
OL	Open Load Detection	Open Load Detection for ChA or ChB or both	40	70		Ω
SL	Short Load Detection	Short Load Detection for ChA or ChB or both (PVDD = 13.5 V)		1		Ω
SL	Short Load Detection	Short Load Detection for ChA or ChB or both (PVDD = 18 V)		2		Ω
SL	Short Load Detection	Short Load Detection for ChA or ChB or both (PVDD = 21 V)		3		Ω
SL	Short Load Detection	Short Load Detection for ChA or ChB or both (PVDD = 24 V)		4		Ω
AUDIO PERFORMACNE (STEREO BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4dBV analog gain, V_{PVDD} = 13.5 V	–6.5		6.5	mV
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 13.5 V, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 10%		16		W
		V_{PVDD} = 13.5 V, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 1%		13		W
		V_{PVDD} = 21 V, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 10%		50		W
		V_{PVDD} = 21 V, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 1%		42		W
		V_{PVDD} = 24 V, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 1%		39		W
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 24 V, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 10%		48		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz, R_{SPK} = 6 Ω)	V_{PVDD} = 18 V		0.03		%
		V_{PVDD} = 21 V		0.03		%
		V_{PVDD} = 24 V		0.03		%
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz, R_{SPK} = 4 Ω)	V_{PVDD} = 21 V		0.03		%
$ICN_{(SPK)}$	Idle channel noise(Aweighted, AES17)	V_{PVDD} = 13.5 V, LC-filter, Load=6 Ω		40		μVrms
		V_{PVDD} = 24 V, LC-filter ,Load=6 Ω		50		μVrms
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=24 V		111		dB
		A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=13.5 V		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 kHz, 1 Vrms, V_{PVDD} = 13.5 V, input audio signal = digital zero		72		dB
$X\text{-}talk_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 kHz, based on Inductor (DFEG7030D-4R7) from Murata		100		dB
AUDIO PERFORMANCE (MONO PBTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4 dBV Analog gain, V_{PVDD} = 18 V	–6.5		6.5	mV
$P_{O(SPK)}$	Output Power	V_{PVDD} = 24 V, R_{SPK} = 3 Ω, f = 1 kHz, THD+N = 1%		79		W
		V_{PVDD} = 24 V, R_{SPK} = 3 Ω, f = 1 kHz, THD+N = 10%		96		W
		V_{PVDD} = 18 V, R_{SPK} = 2 Ω, f = 1 kHz, THD+N = 1%		58		W
$P_{O(SPK)}$	Output Power	V_{PVDD} = 18 V, R_{SPK} = 2 Ω, f = 1 kHz, THD+N = 10%		75		W

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz)	V_{PVDD} = 18 V, LC-filter, R_{SPK} = 2 Ω		0.08		%
		V_{PVDD} = 24 V, LC-filter, R_{SPK} = 3 Ω		0.03		%
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=24 V, R_{SPK} = 4 Ω		108		dB
		A-Weighted,referenced to 1% THD+N Output Level, V_{PVDD}=13.5 V, R_{SPK} = 3 Ω		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 kHz, 1 Vrms,V_{PVDD} = 18 V, input audio signal = digital zero		72		dB

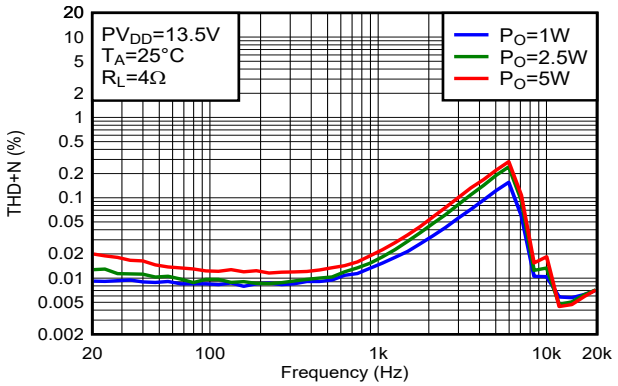
5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing - Target Mode					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCLK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I^2C Bus Timing – Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			µs
t_{S-HD}	Hold time for (repeated) START condition	4			µs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		3450	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{P-SU}	Setup time for STOP condition	4			µs
C_B	Capacitive load for each bus line			400	pf
I^2C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated)START condition	600			ns
t_{RS-HD}	Hold time for (repeated)START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_B	Capacitive load for each bus line			400	pf

6 Typical Characteristics

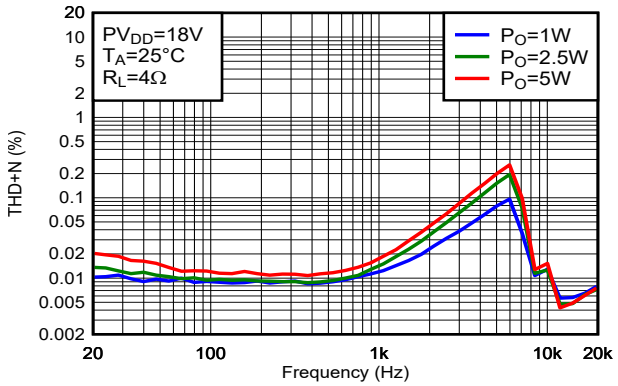
6.1 Bridge Tied Load (BTL) Configuration Curves with BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 120kHz Class D Amplifier Loop Bandwidth, LC filter with 10µH / 0.68µF, unless otherwise noted.



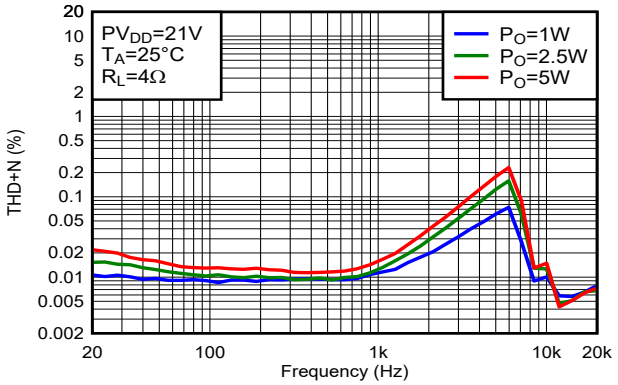
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 4Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-1. THD+N vs Frequency



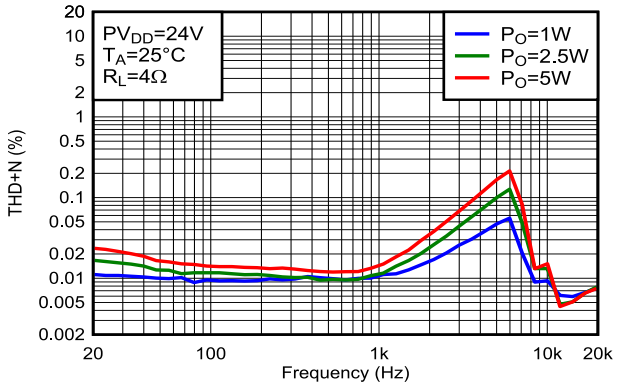
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 4Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-2. THD+N vs Frequency



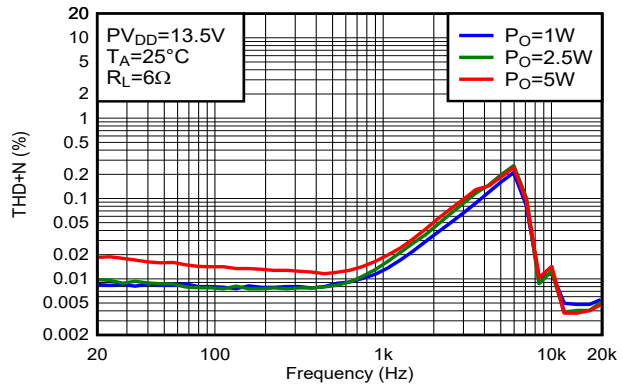
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 4Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-3. THD+N vs Frequency



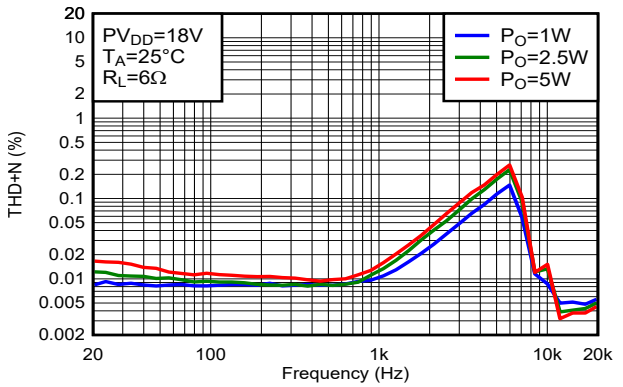
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 4Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-4. THD+N vs Frequency



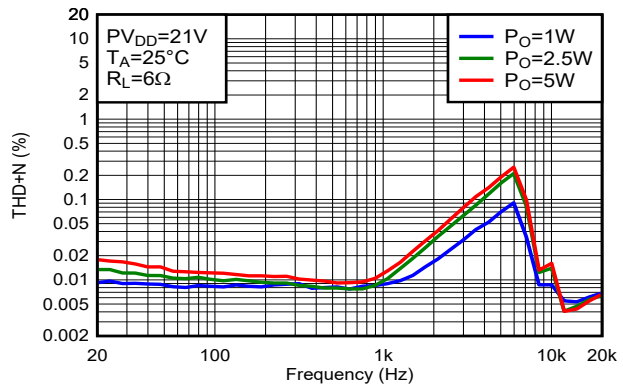
1SPW Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-5. THD+N vs Frequency



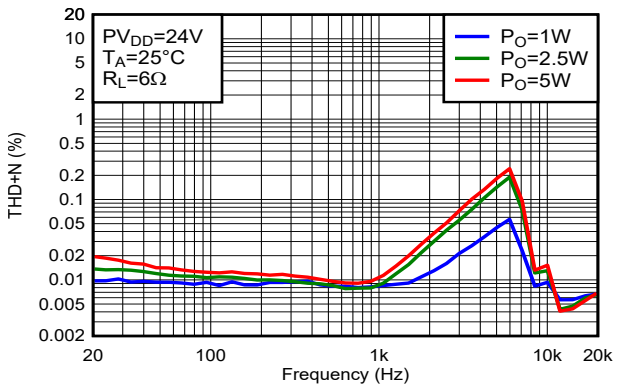
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-6. THD+N vs Frequency



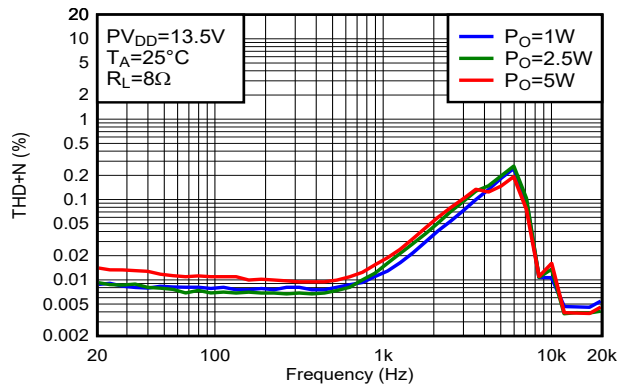
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-7. THD+N vs Frequency



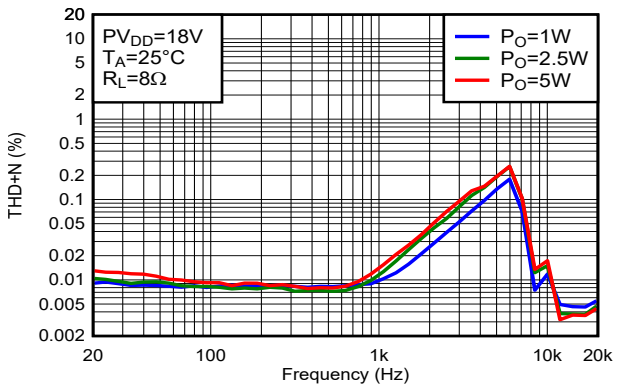
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-8. THD+N vs Frequency



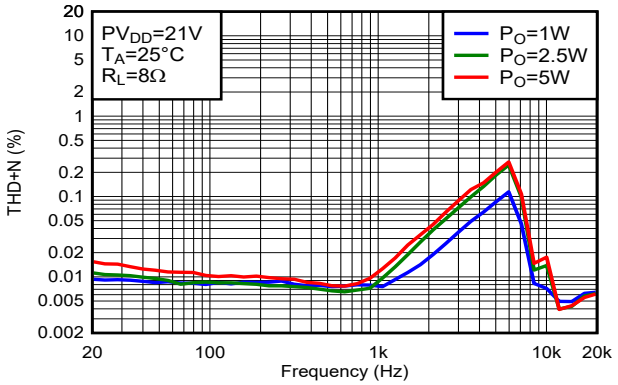
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-9. THD+N vs Frequency



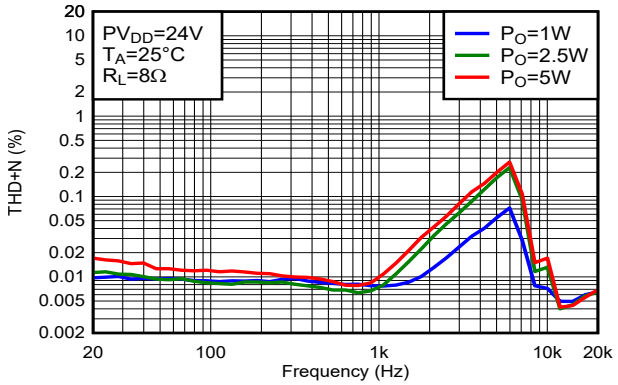
BD Modulation P_O=1W,2.5W,5W
F_{SW}=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-10. THD+N vs Frequency



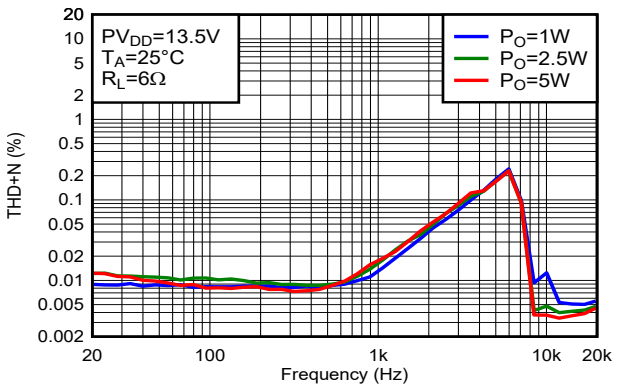
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-11. THD+N vs Frequency



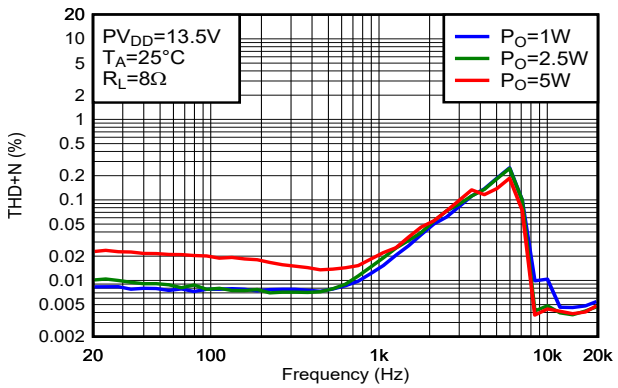
BD Modulation PO=1W,2.5W,5W
FSW=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-12. THD+N vs Frequency



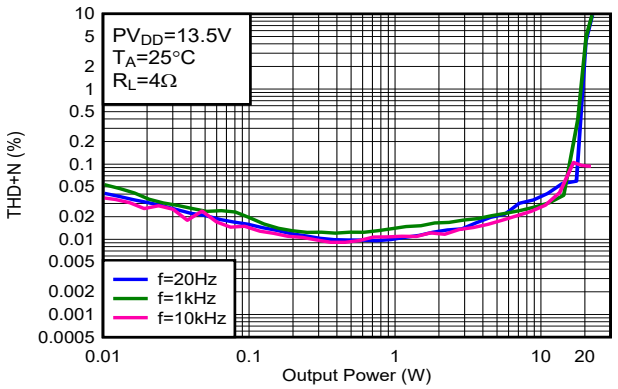
BD Modulation Ferrite Bead + Capacitor
Spread Spectrum Enable
FSW=384kHz Load = 6Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-13. THD+N vs Frequency



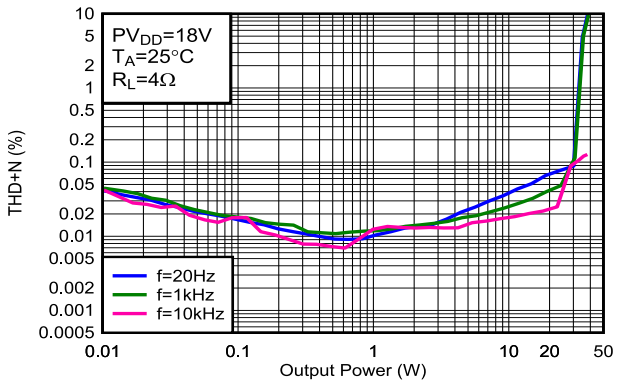
BD Modulation Ferrite Bead + Capacitor
Spread Spectrum Enable
FSW=384kHz Load = 8Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-14. THD+N vs Frequency



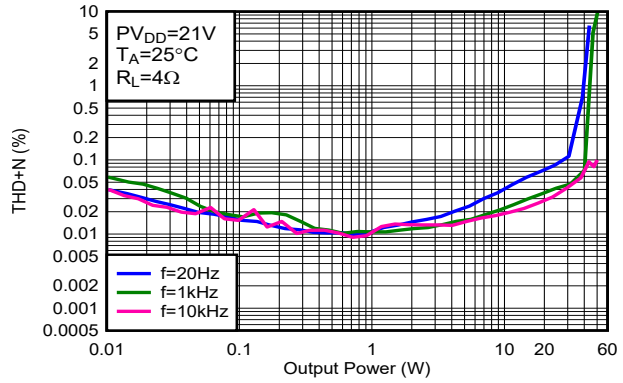
BD Modulation
FSW=384kHz PVDD = 13.5V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-15. THD+N vs Output Power



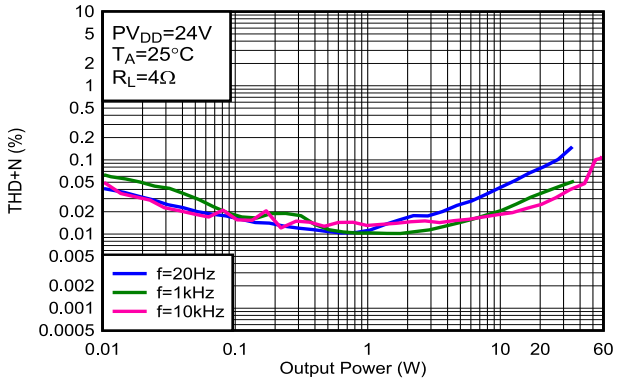
BD Modulation
FSW=384kHz PVDD = 18V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-16. THD+N vs Output Power



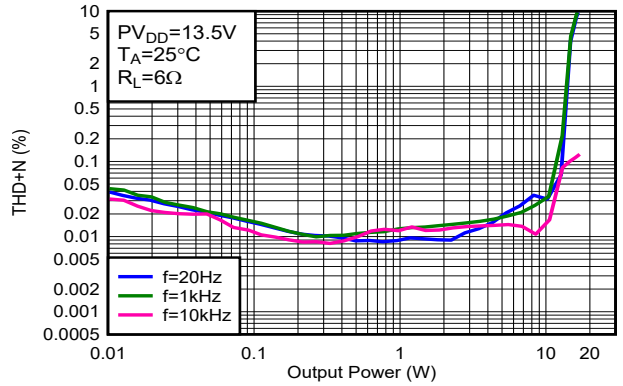
BD Modulation
FSW=384kHz PVDD = 21V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-17. THD+N vs Output Power



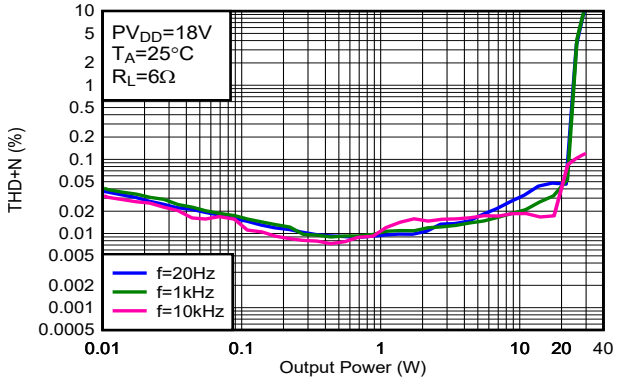
BD Modulation
FSW=384kHz PVDD = 24V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-18. THD+N vs Output Power



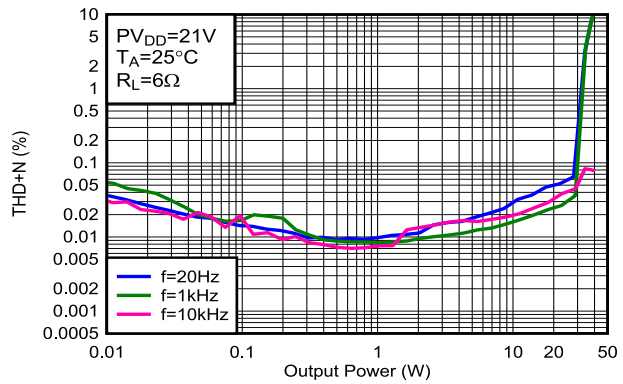
BD Modulation
FSW=384kHz PVDD = 13.5V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-19. THD+N vs Output Power



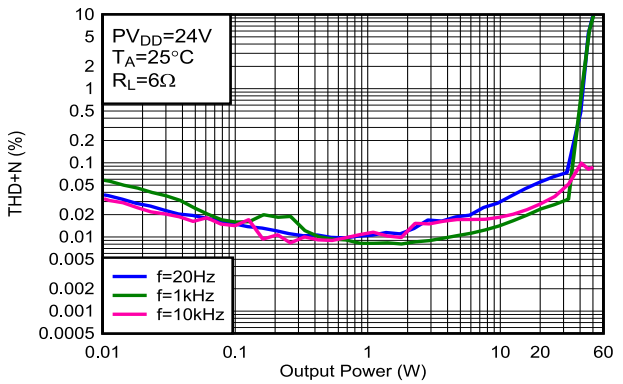
BD Modulation
FSW=384kHz PVDD = 18V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-20. THD+N vs Output Power



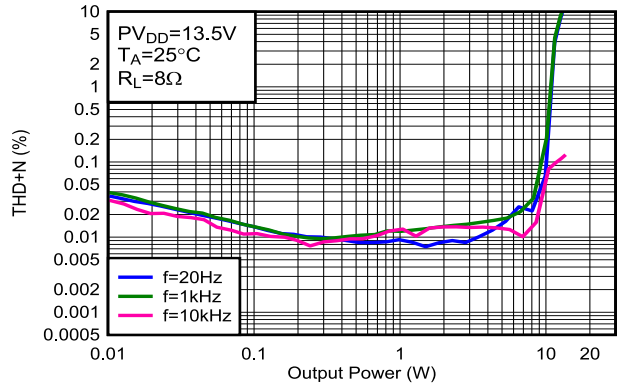
BD Modulation
FSW=384kHz PVDD = 21V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-21. THD+N vs Output Power



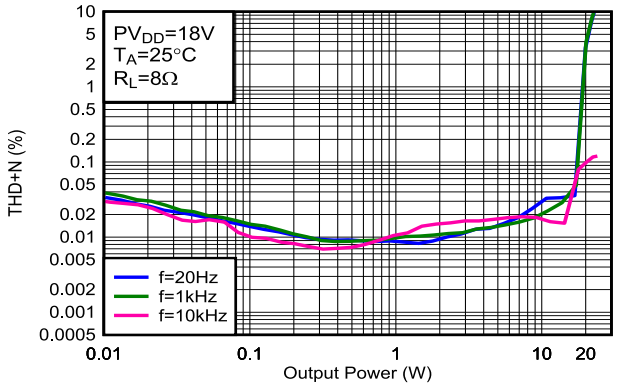
BD Modulation
FSW=384kHz PVDD = 24V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-22. THD+N vs Output Power



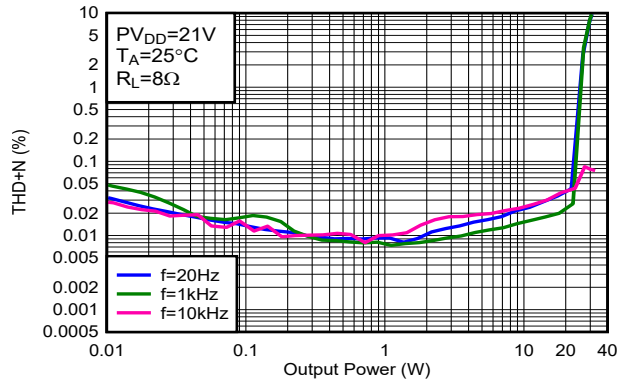
BD Modulation
FSW=384kHz PVDD = 13.5V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-23. THD+N vs Output Power



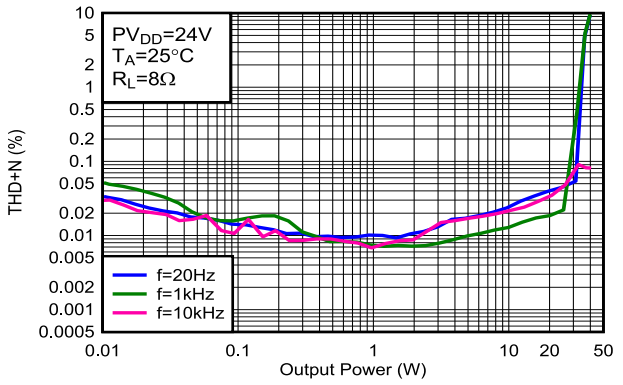
BD Modulation
FSW=384kHz PVDD = 18V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-24. THD+N vs Output Power



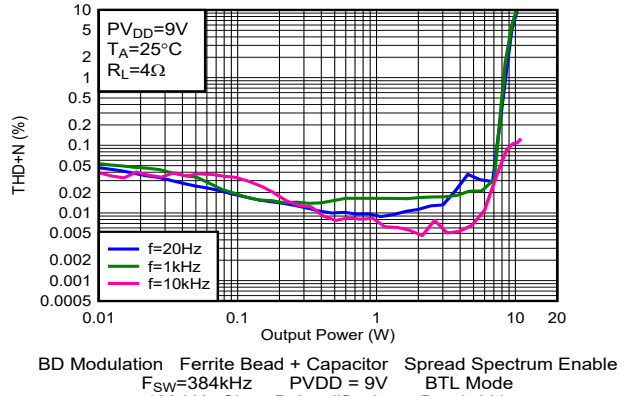
BD Modulation
FSW=384kHz PVDD = 21V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-25. THD+N vs Output Power



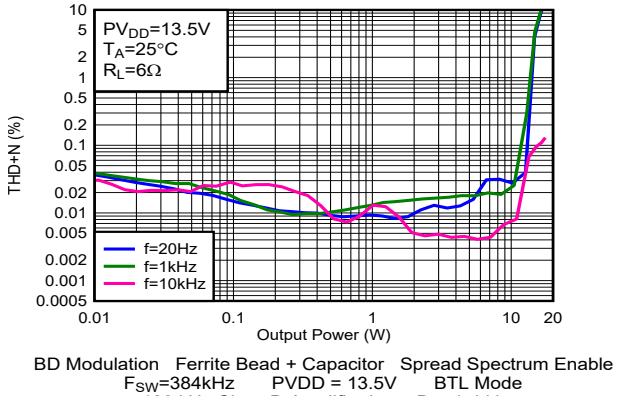
BD Modulation
FSW=384kHz PVDD = 24V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-26. THD+N vs Output Power



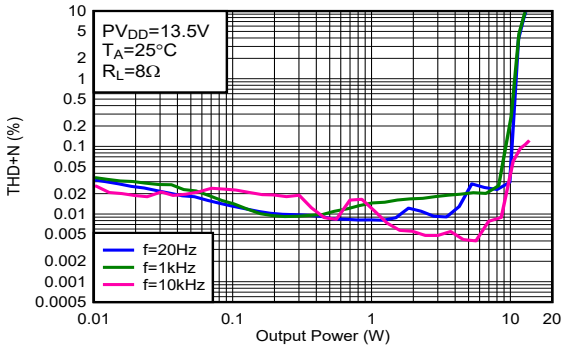
BD Modulation Ferrite Bead + Capacitor Spread Spectrum Enable
FSW=384kHz PVDD = 9V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-27. THD+N vs Output Power



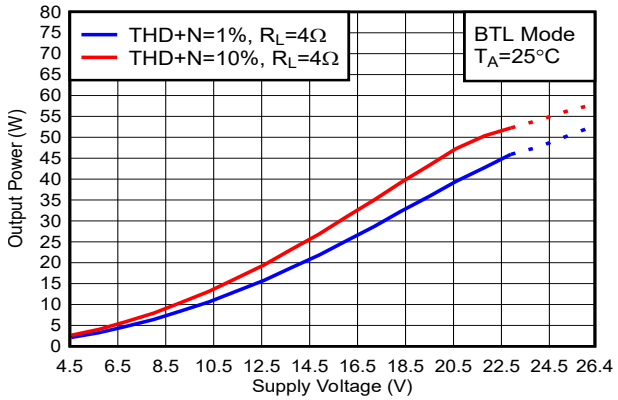
BD Modulation Ferrite Bead + Capacitor Spread Spectrum Enable
FSW=384kHz PVDD = 13.5V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-28. THD+N vs Output Power



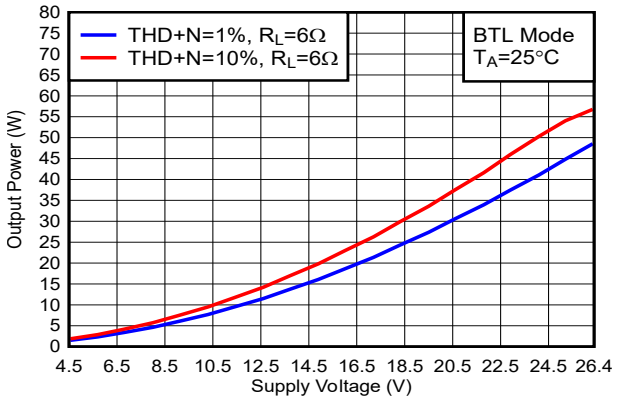
BD Modulation Ferrite Bead + Capacitor Spread Spectrum Enable
FSW=384kHz PVDD = 13.5V BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-29. THD+N vs Output Power



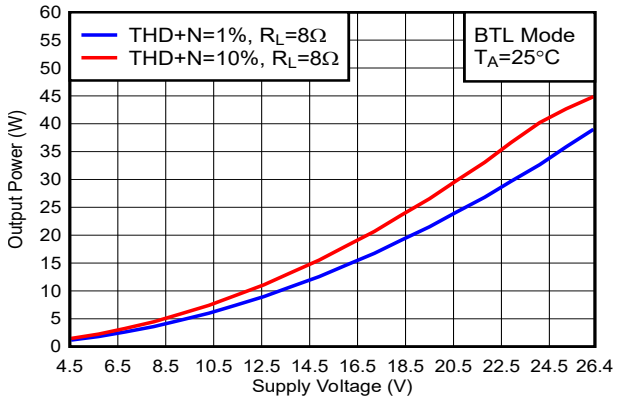
BD Modulation
FSW=384kHz Load = 4Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-30. Output Power vs Supply Voltage



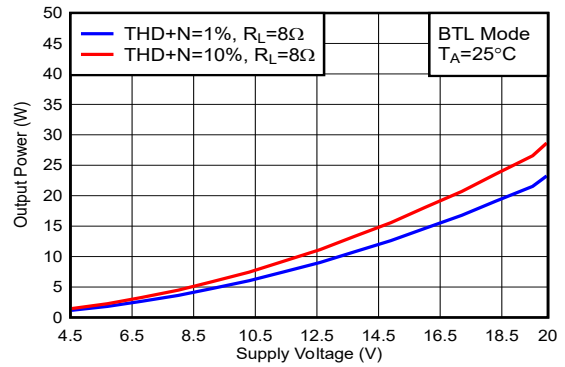
BD Modulation
FSW=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-31. Output Power vs Supply Voltage



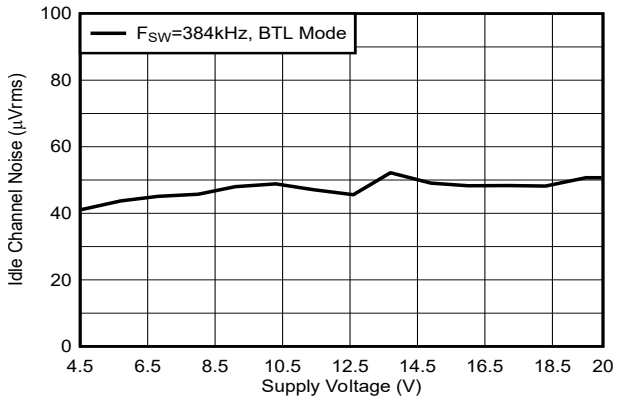
BD Modulation
FSW=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-32. Output Power vs Supply Voltage



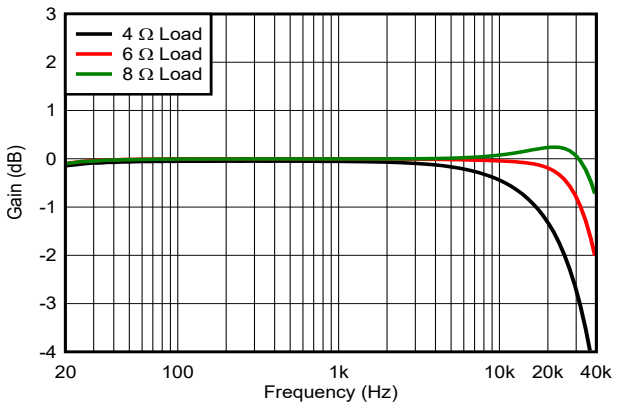
BD Modulation Ferrite Bead + Capacitor Spread Spectrum Enable
FSW=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-33. Output Power vs Supply Voltage



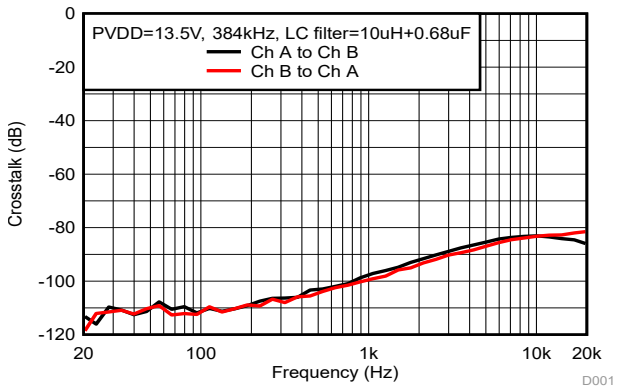
BD Modulation
FSW=384kHz Load = 8Ω BTL Mode
120kHz Class D Amplifier Loop Bandwidth

図 6-34. Idle Channel Noise vs Supply Voltage



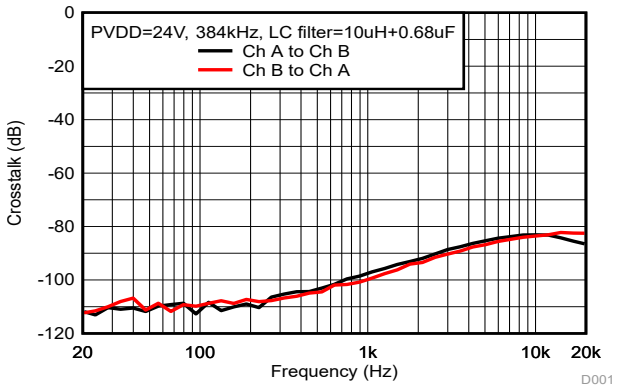
BD Modulation P_O=1W PVDD=21V
F_{SW}=384kHz BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-35. Gain vs Frequency



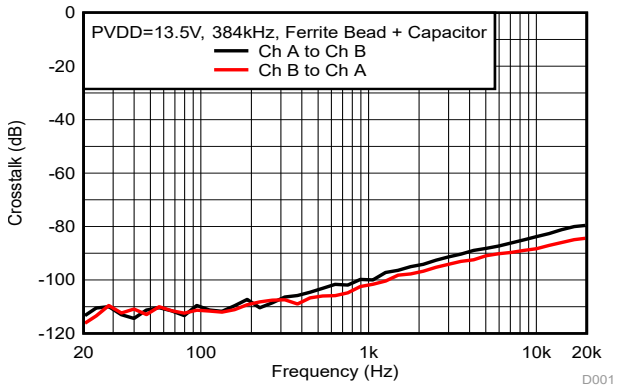
PVDD=13.5V BD Modulation Pout=1W
F_{SW}=384kHz Load = 6Ω BTL Mode

図 6-36. Crosstalk



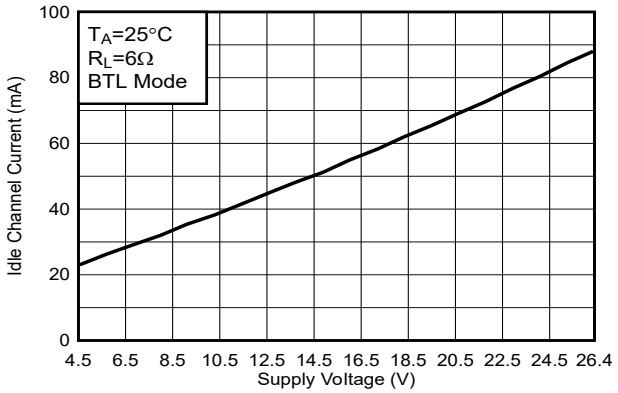
PVDD=24V BD Modulation Pout=1W
F_{SW}=384kHz Load = 6Ω BTL Mode

図 6-37. Crosstalk



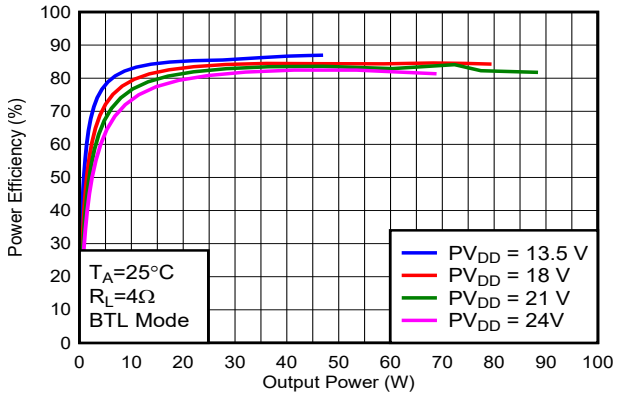
Spread Spectrum BD Modulation Pout=1W
Enable Load = 6Ω BTL Mode

図 6-38. Crosstalk



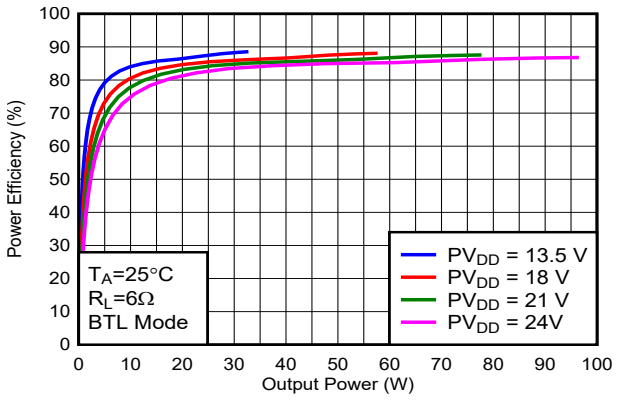
BD Modulation
F_{SW}=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-39. PVDD Idle Current vs PVDD Voltage



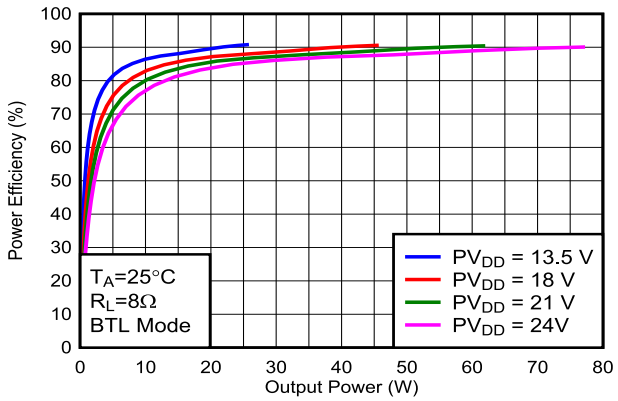
BD Modulation
F_{SW}=384kHz Load = 4Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-40. Efficiency vs Output Power



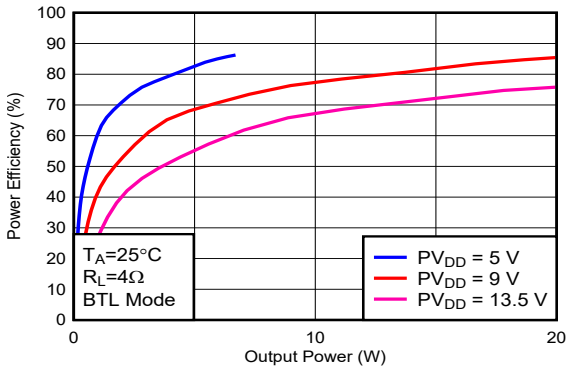
BD Modulation
FSW=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-41. Efficiency vs Output Power



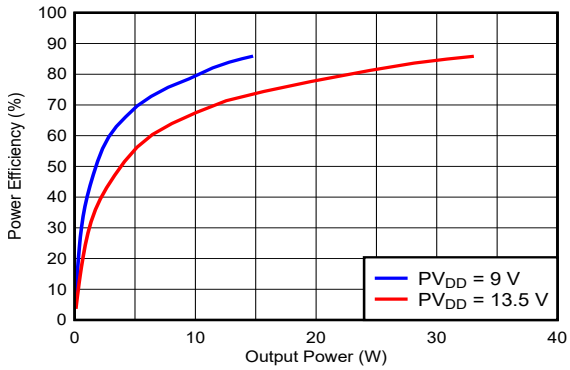
BD Modulation
FSW=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-42. Efficiency vs Output Power



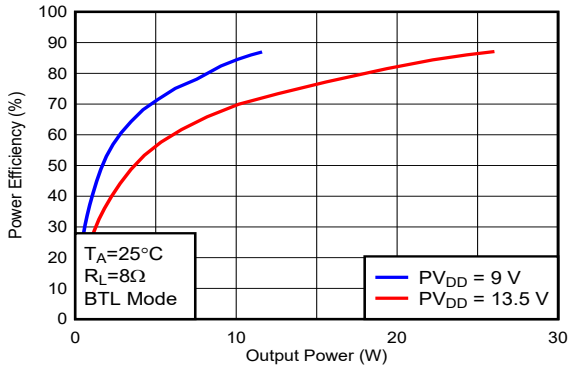
BD Modulation Ferrite Bead +Capacitor Spread Spectrum Enable
FSW=384kHz Load = 4Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-43. Efficiency vs Output Power (with FB)



BD Modulation Ferrite Bead +Capacitor Spread Spectrum Enable
FSW=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-44. Efficiency vs Output Power



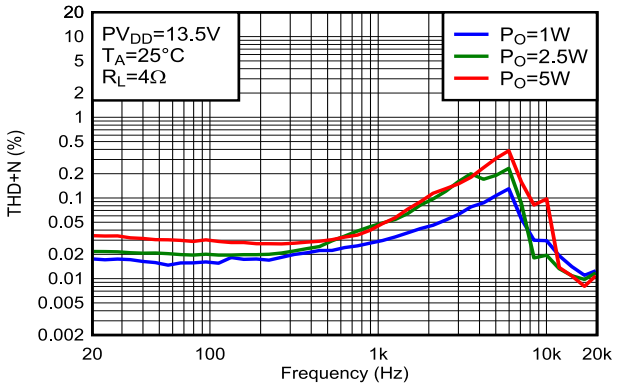
BD Modulation Ferrite Bead +Capacitor Spread Spectrum Enable
FSW=384kHz Load = 8Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-45. Efficiency vs Output Power

6.2 Bridge Tied Load (BTL) Configuration Curves with 1SPW Modulation

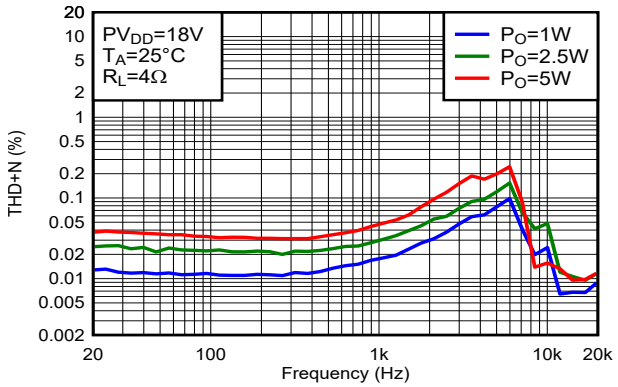
Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio

frequency set to 1kHz and device PWM frequency set to 384kHz, 175kHz Class D Loop Bandwidth, the LC filter used was 10µH / 0.68µF, unless otherwise noted.



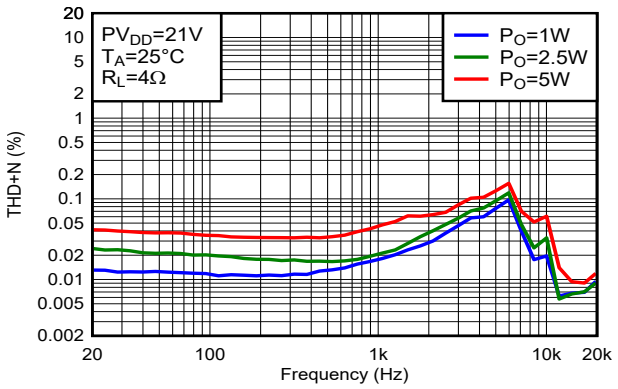
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 4Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-46. THD+N vs Frequency



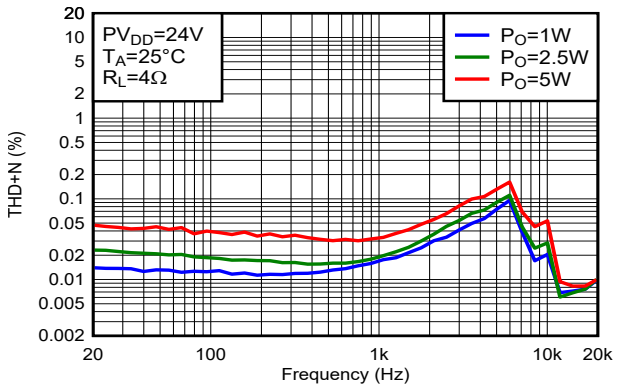
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 4Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-47. THD+N vs Frequency



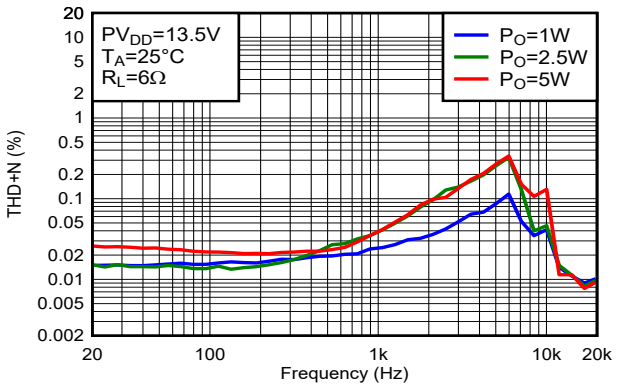
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 4Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-48. THD+N vs Frequency



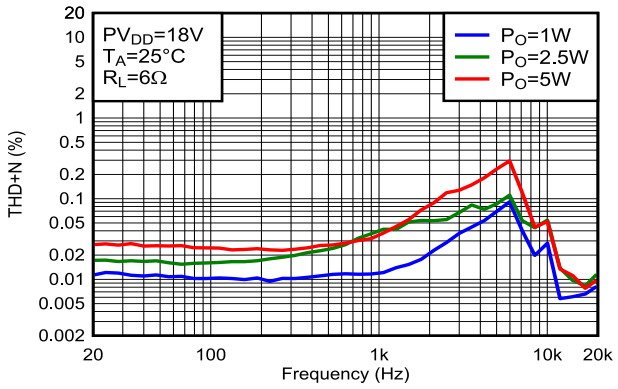
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 4Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-49. THD+N vs Frequency



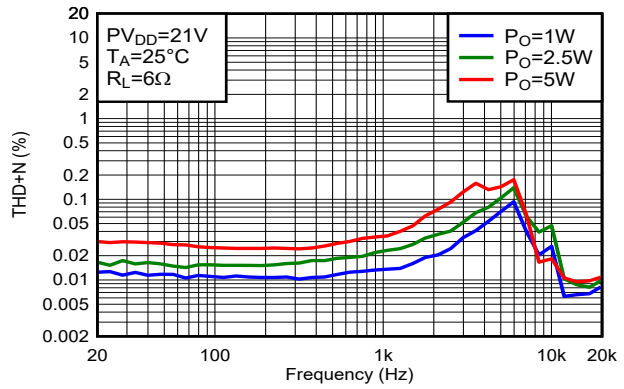
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 6Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-50. THD+N vs Frequency



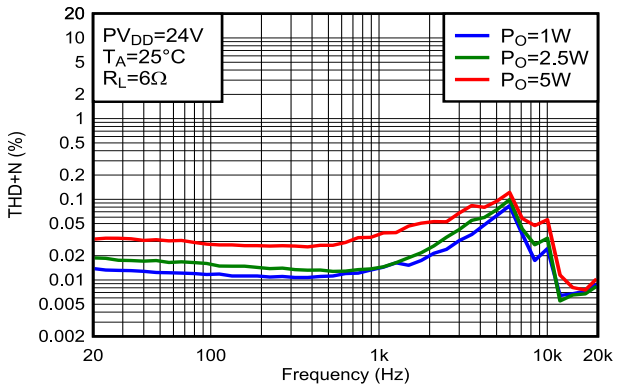
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 6Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-51. THD+N vs Frequency



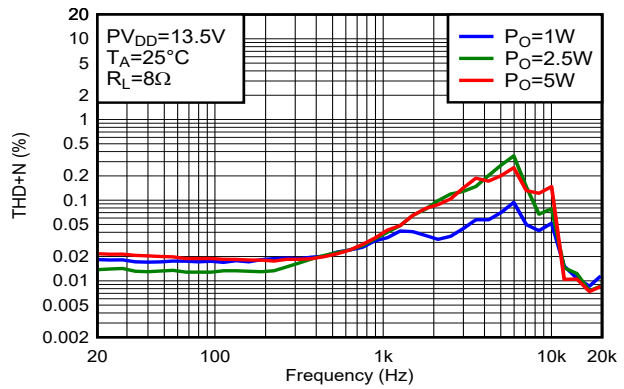
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 6Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-52. THD+N vs Frequency



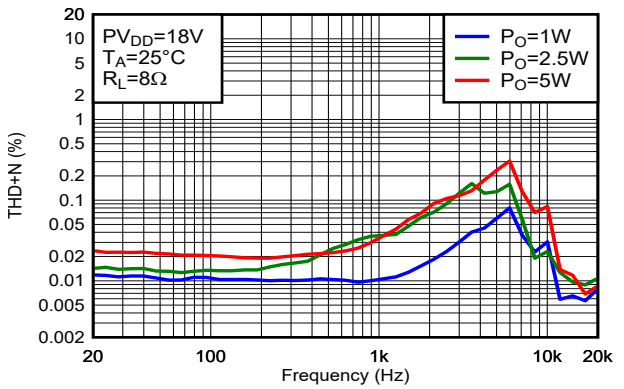
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 6Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-53. THD+N vs Frequency



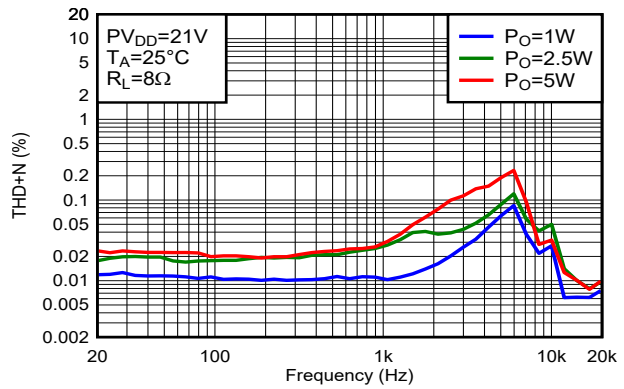
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 8Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-54. THD+N vs Frequency



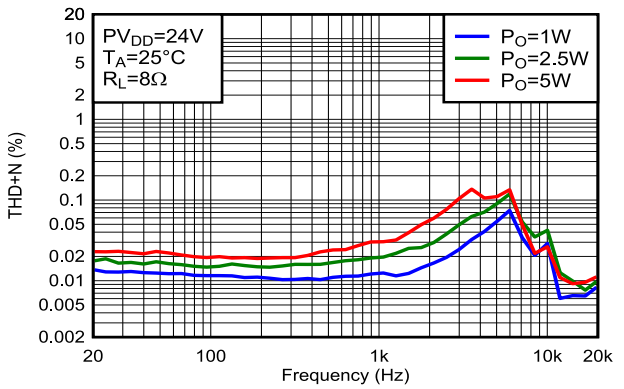
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 8Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-55. THD+N vs Frequency



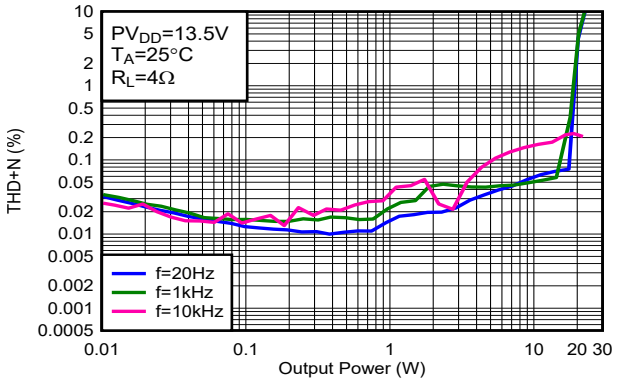
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 8Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-56. THD+N vs Frequency



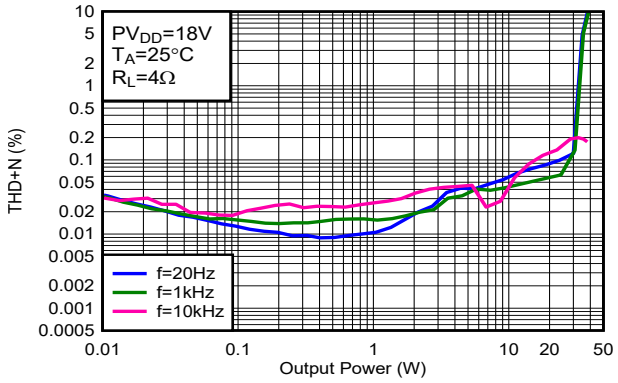
1SPW Modulation PO=1W,2.5W,5W
FSW=768kHz Load = 8Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-57. THD+N vs Frequency



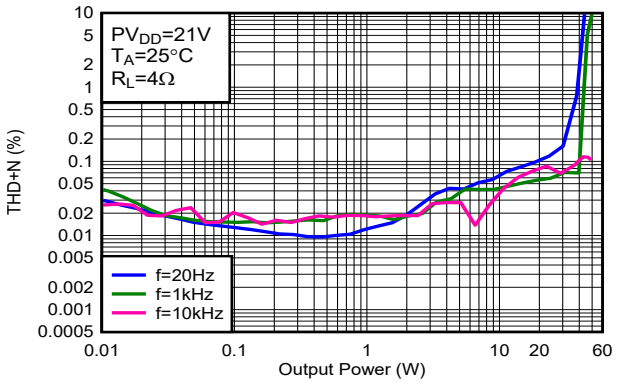
1SPW Modulation
FSW=768kHz PVDD = 13.5V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-58. THD+N vs Output Power



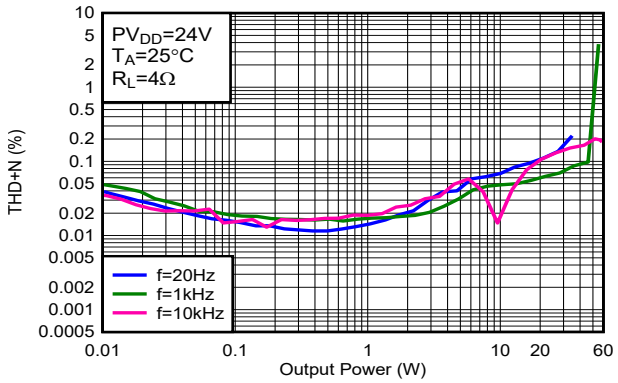
1SPW Modulation
FSW=768kHz PVDD = 18V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-59. THD+N vs Output Power



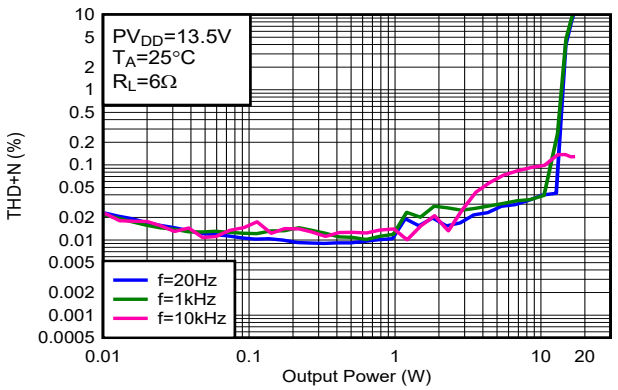
1SPW Modulation
FSW=768kHz PVDD = 21V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-60. THD+N vs Output Power



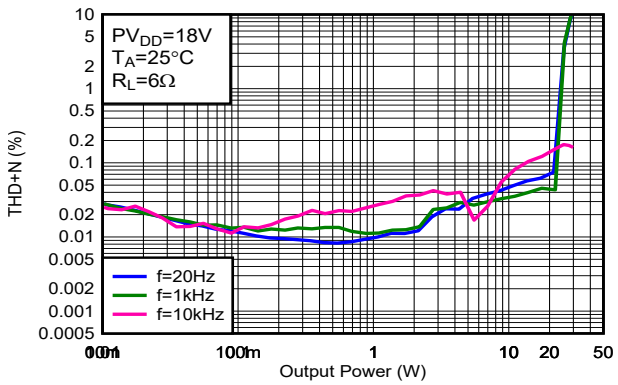
1SPW Modulation
FSW=768kHz PVDD = 24V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-61. THD+N vs Output Power



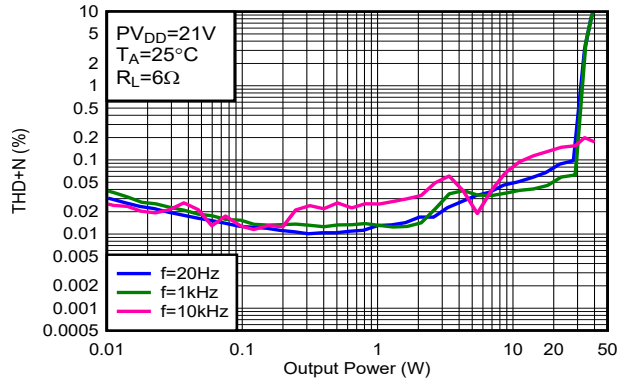
1SPW Modulation
FSW=768kHz PVDD = 13.5V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-62. THD+N vs Output Power



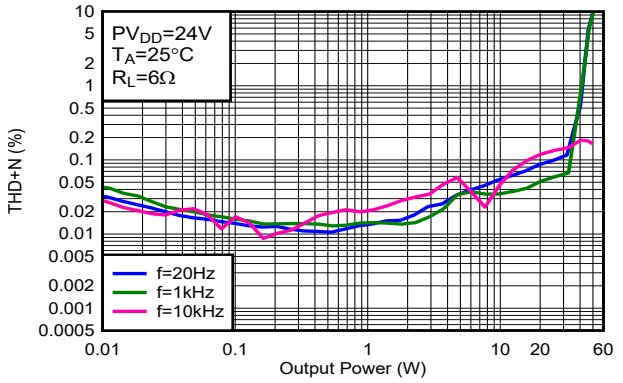
1SPW Modulation
FSW=768kHz PVDD = 18V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-63. THD+N vs Output Power



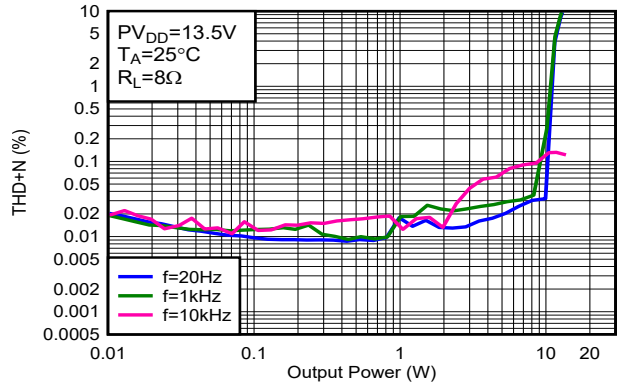
1SPW Modulation
FSW=768kHz PVDD = 21V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-64. THD+N vs Output Power



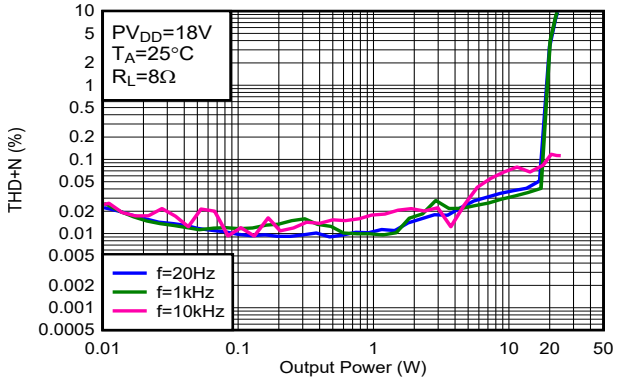
1SPW Modulation
FSW=768kHz PVDD = 24V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-65. THD+N vs Output Power



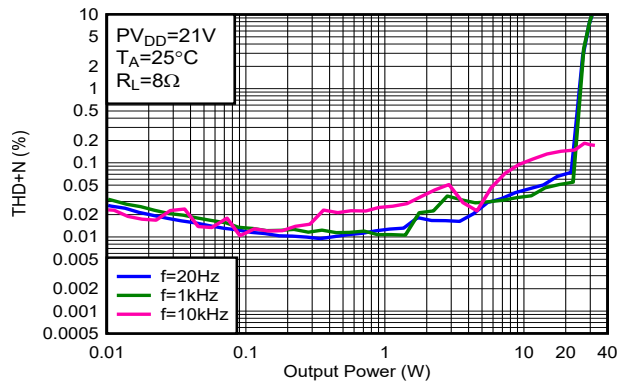
1SPW Modulation
FSW=768kHz PVDD = 13.5V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-66. THD+N vs Output Power



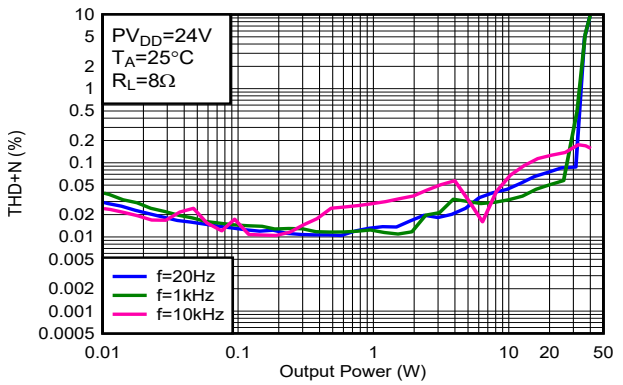
1SPW Modulation
FSW=768kHz PVDD = 18V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-67. THD+N vs Output Power



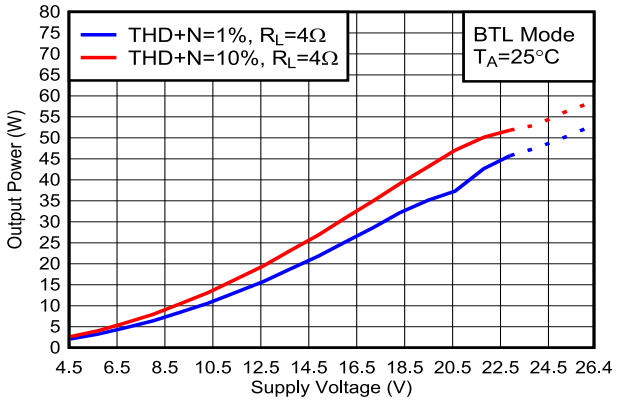
1SPW Modulation
FSW=768kHz PVDD = 21V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-68. THD+N vs Output Power



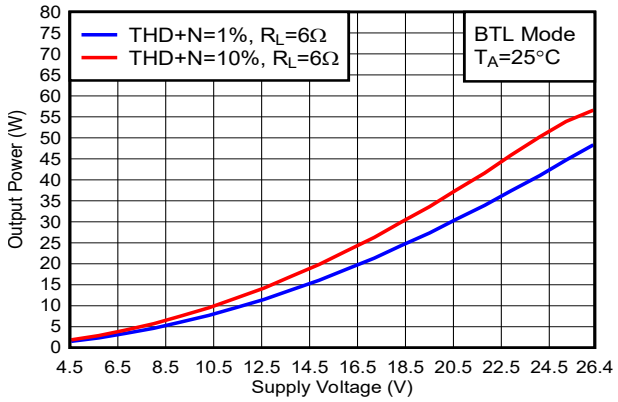
1SPW Modulation
FSW=768kHz PVDD = 24V BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-69. THD+N vs Output Power



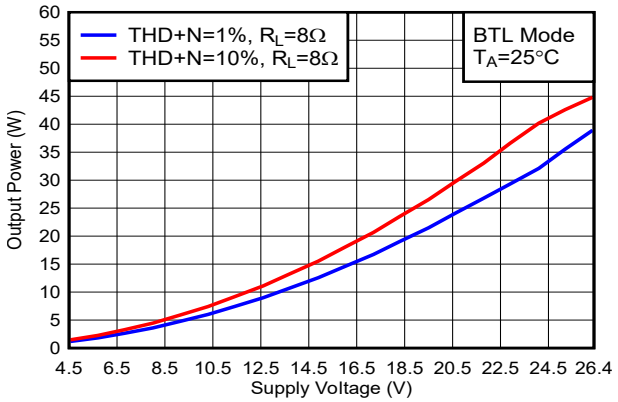
1SPW Modulation
F_{SW}=768kHz Load = 4Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-70. Output Power vs Supply Voltage (dotted line is thermally limited)



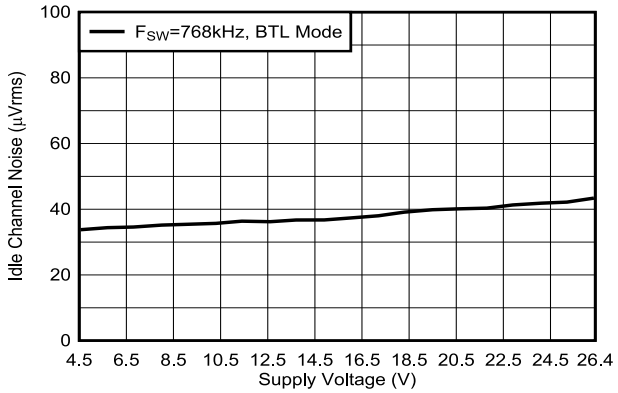
1SPW Modulation
F_{SW}=768kHz Load = 6Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-71. Output Power vs Supply Voltage



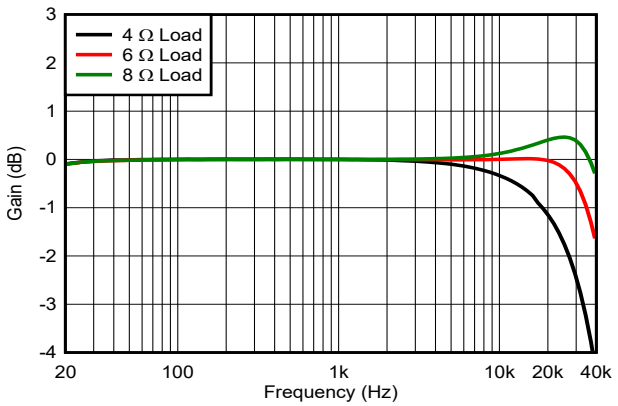
1SPW Modulation
F_{SW}=768kHz Load = 8Ω BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-72. Output Power vs Supply Voltage



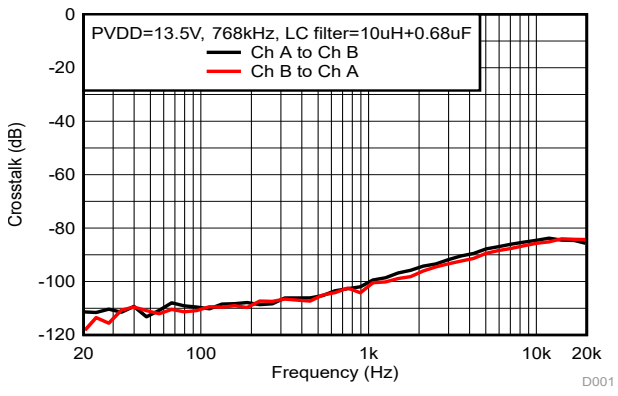
1SPW Modulation
F_{SW}=768kHz Load = 8Ω BTL Mode
175kHz Class D Amplifier Loop Bandwidth

図 6-73. Idle Channel Noise vs Supply Voltage



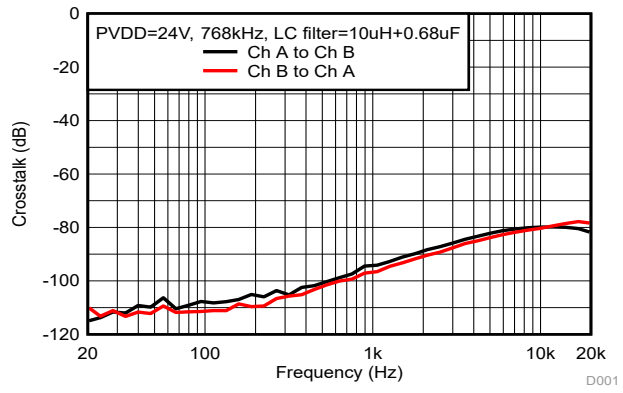
1SPW Modulation P_O=1W PVDD=21V
F_{SW}=768kHz BTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-74. Gain vs Frequency



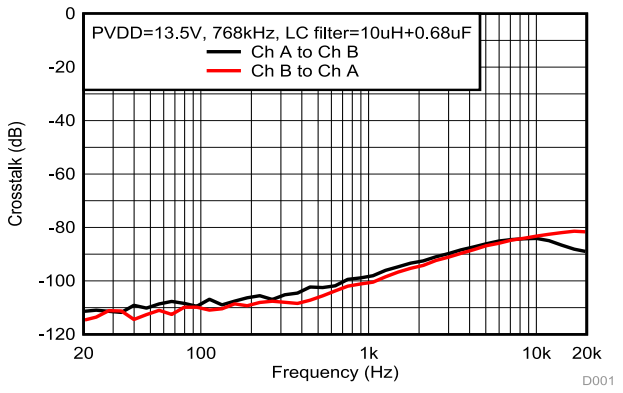
PVDD=13.5V 1SPW Modulation Pout=1W
F_{SW}=768kHz Load = 4Ω BTL Mode

図 6-75. Crosstalk



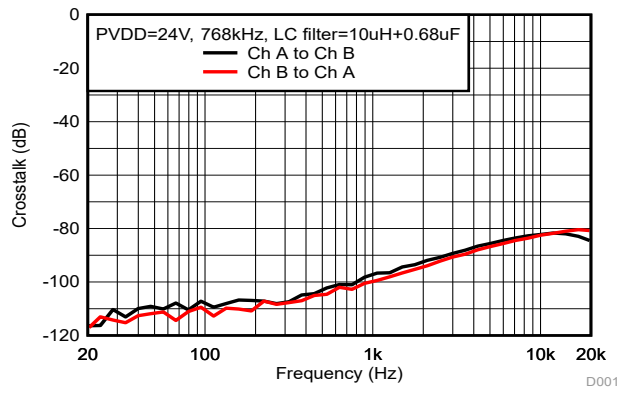
PVDD=24V 1SPW Modulation Pout=1W
F_{SW}=768kHz Load = 4Ω BTL Mode

図 6-76. Crosstalk



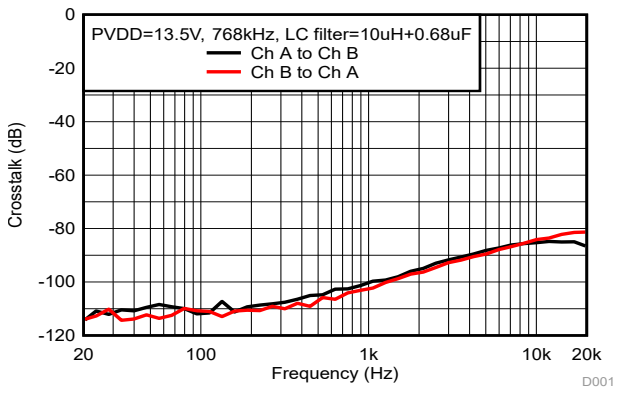
PVDD=13.5V 1SPW Modulation Pout=1W
F_{SW}=768kHz Load = 6Ω BTL Mode

図 6-77. Crosstalk



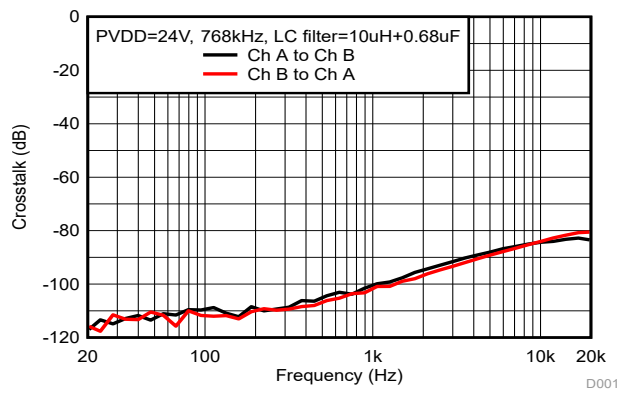
PVDD=24V 1SPW Modulation Pout=1W
F_{SW}=768kHz Load = 6Ω BTL Mode

図 6-78. Crosstalk



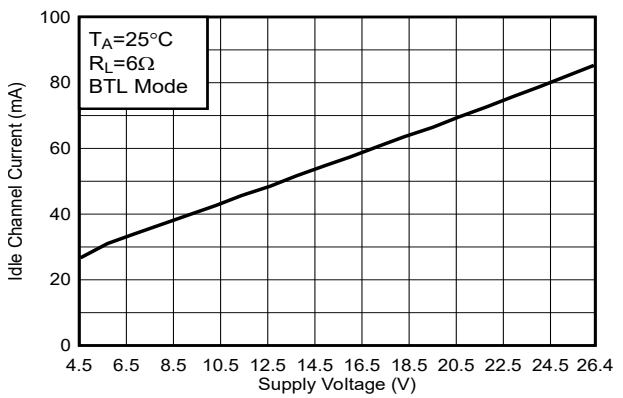
PVDD=13.5V 1SPW Modulation Pout=1W
F_{SW}=768kHz Load = 8Ω BTL Mode

図 6-79. Crosstalk



PVDD=24V 1SPW Modulation Pout=1W
F_{SW}=768kHz Load = 8Ω BTL Mode

図 6-80. Crosstalk



1SPW Modulation
F_{SW}=768kHz Load = 6Ω BTL Mode
175kHz Class D Amplifier Loop Bandwidth

図 6-81. PVDD Idle Current vs PVDD Voltage

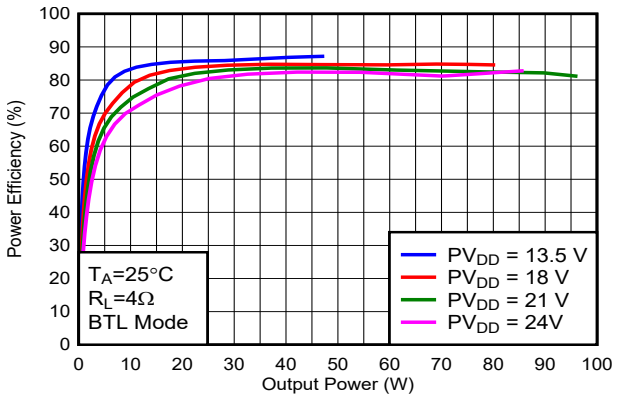


図 6-82. Efficiency vs Output Power

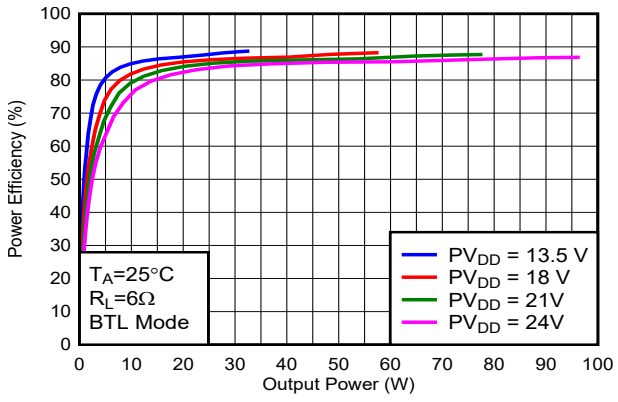


図 6-83. Efficiency vs Output Power

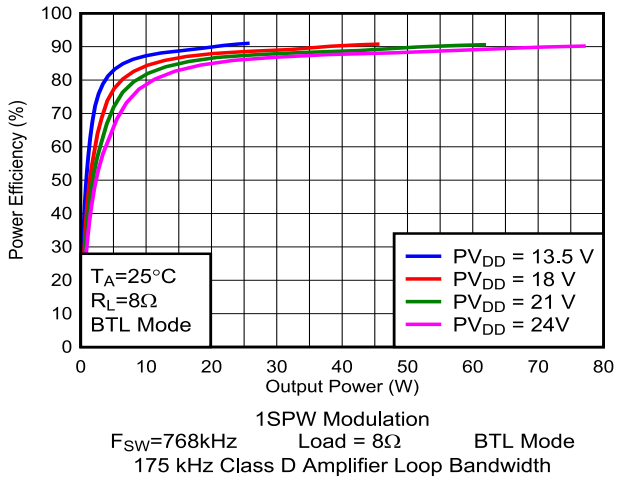


図 6-84. Efficiency vs Output Power

6.3 Parallel Bridge Tied Load (PBTL) Configuration With BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 120kHz Class D Amplifier Loop Bandwidth, LC filter with 10µH / 0.68µF（Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see details in セクション 9.2.3）, unless otherwise noted.

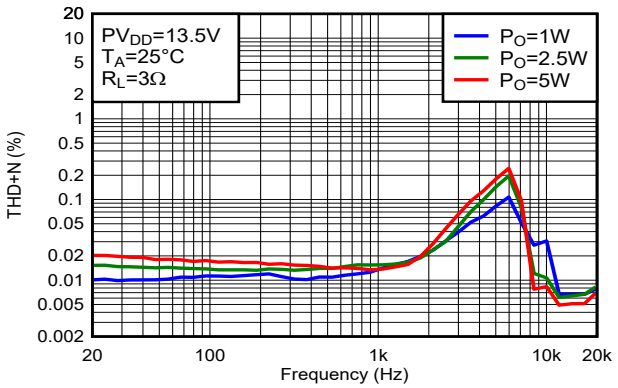


図 6-85. THD+N vs Frequency

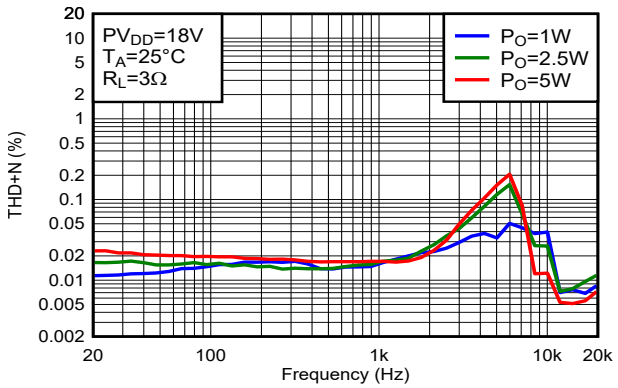


図 6-86. THD+N vs Frequency

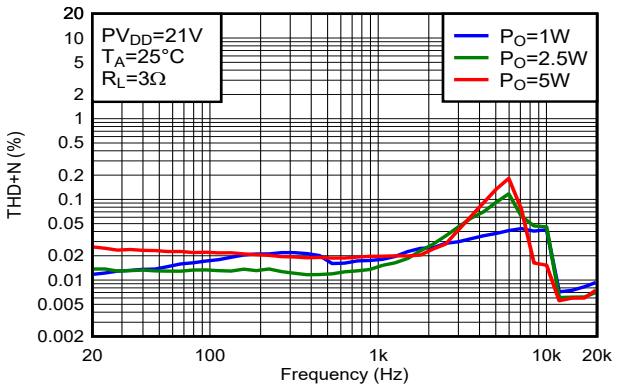


図 6-87. THD+N vs Frequency

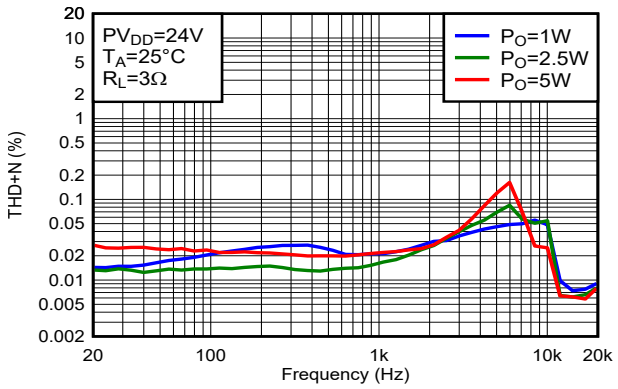
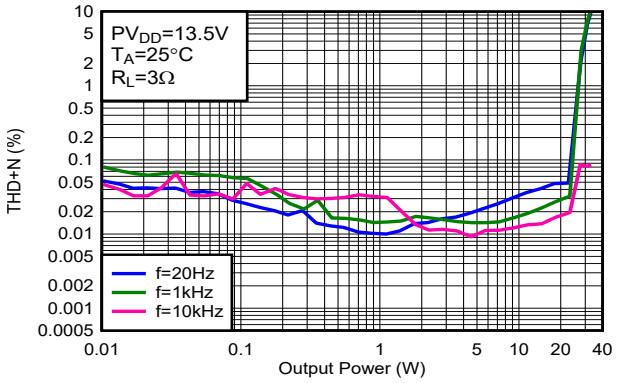
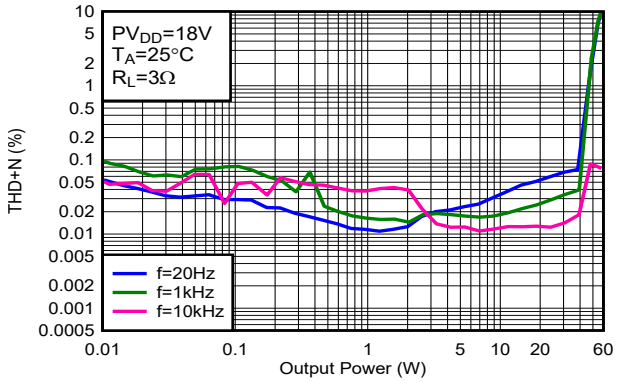


図 6-88. THD+N vs Frequency



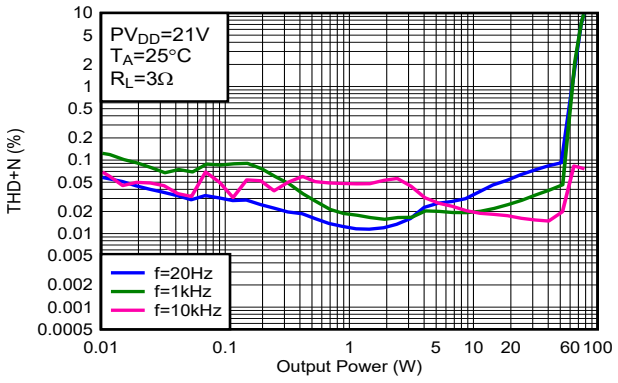
BD Modulation
FSW=384kHz PVDD = 13.5V PBTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-89. THD+N vs Output Power



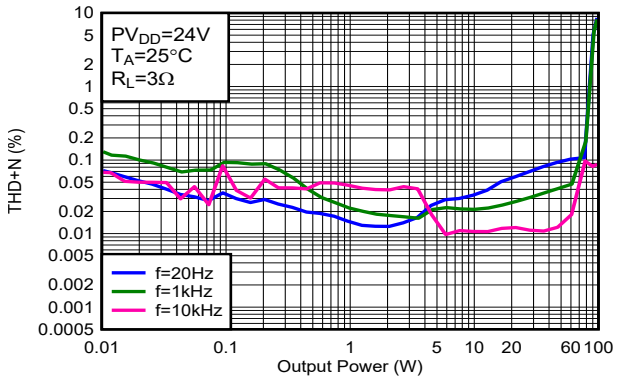
BD Modulation
FSW=384kHz PVDD = 18V PBTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-90. THD+N vs Output Power



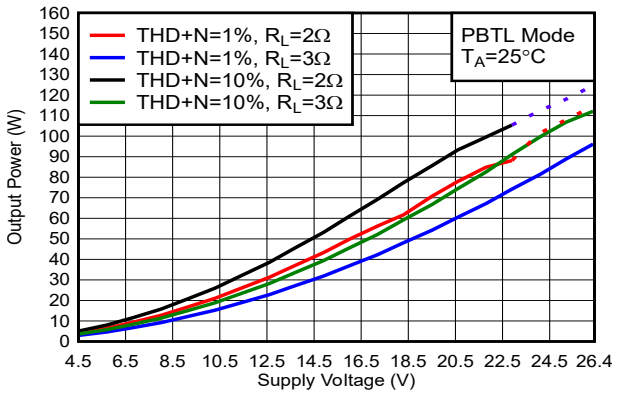
BD Modulation
FSW=384kHz PVDD = 21V PBTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-91. THD+N vs Output Power



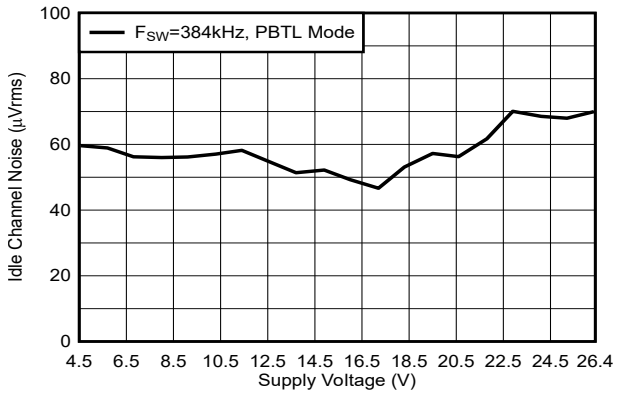
BD Modulation
FSW=384kHz PVDD = 24V PBTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-92. THD+N vs Output Power



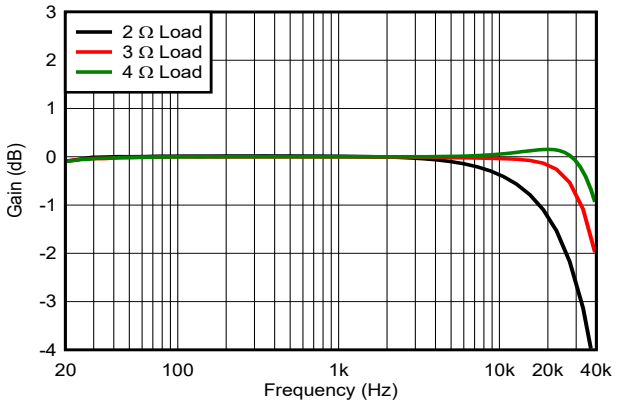
BD Modulation
FSW=384kHz Load = 3Ω PBTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-93. Output Power vs Supply Voltage (dotted line is thermally limited)



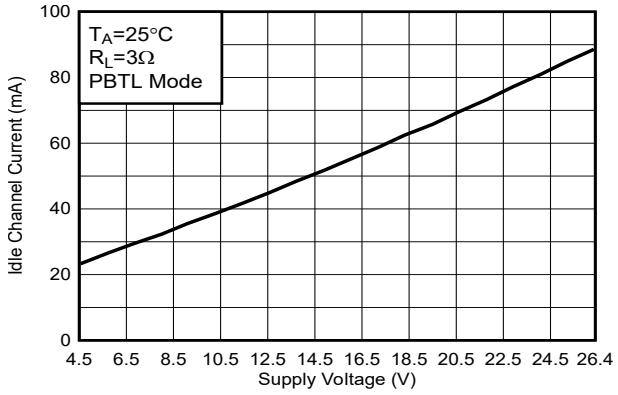
BD Modulation
FSW=384kHz Load = 3Ω PBTL Mode
120kHz Class D Amplifier Loop Bandwidth

図 6-94. Idle Channel Noise vs Supply Voltage



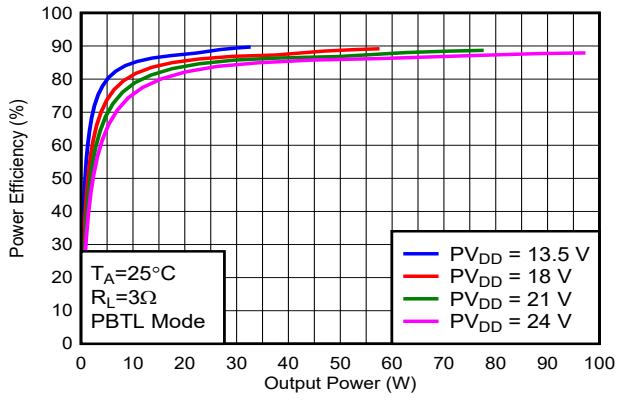
BD Modulation P_O=1W PVDD=13.5V
F_{SW}=384kHz BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-95. Gain vs Frequency



BD Modulation
F_{SW}=384kHz Load = 3Ω PBTL Mode
120kHz Class D Amplifier Loop Bandwidth

図 6-96. PVDD Idle Current vs PVDD voltage

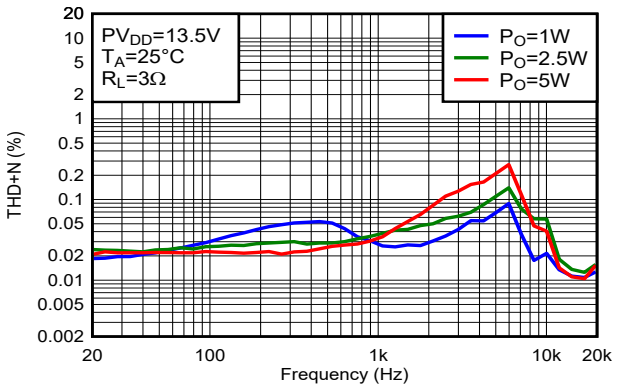


BD Modulation
F_{SW}=384kHz Load = 3Ω PBTL Mode
120 kHz Class D Amplifier Loop Bandwidth

図 6-97. Efficiency vs Output Power

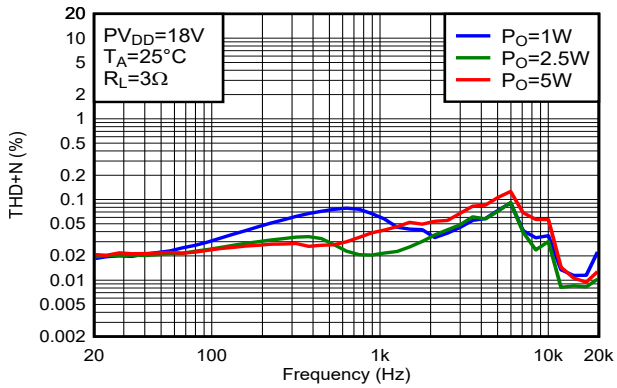
6.4 Parallel Bridge Tied Load (PBTL) Configuration With 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20kHz brickwall filter. All measurements taken with audio frequency set to 1kHz and device PWM frequency set to 384kHz, 175kHz Class D Amplifier Loop Bandwidth, the LC filter used was 10µH / 0.68µF（Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see connect method in セクション 9.2.3）, unless otherwise noted.



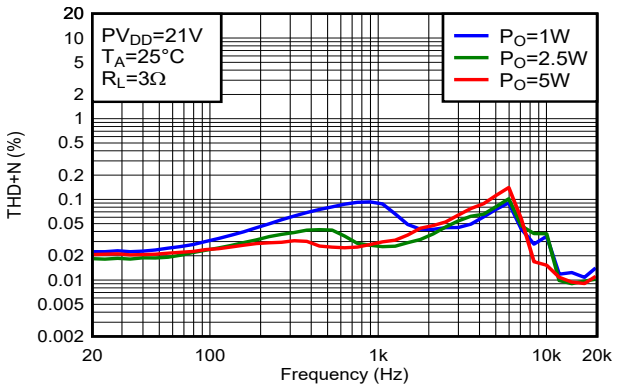
1SPW Modulation P_O=1W,2.5W,5W
F_{SW}=768kHz Load = 3Ω PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-98. THD+N vs Frequency



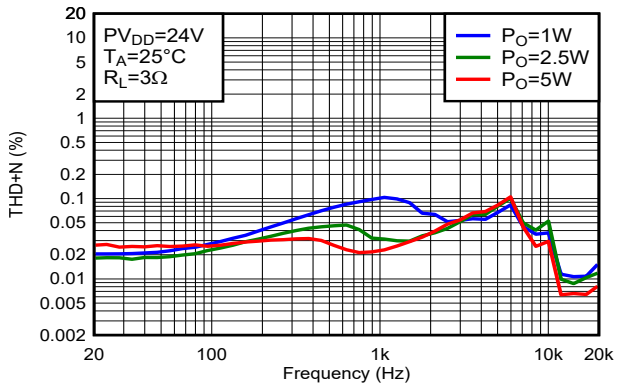
1SPW Modulation P_O=1W,2.5W,5W
F_{SW}=768kHz Load = 3Ω PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-99. THD+N vs Frequency



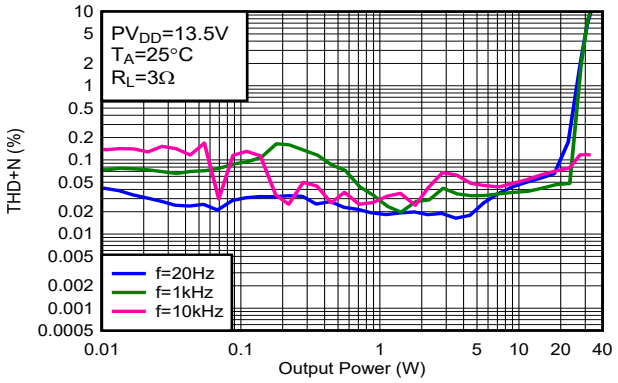
1SPW Modulation P_O=1W,2.5W,5W
F_{SW}=768kHz Load = 3Ω PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-100. THD+N vs Frequency



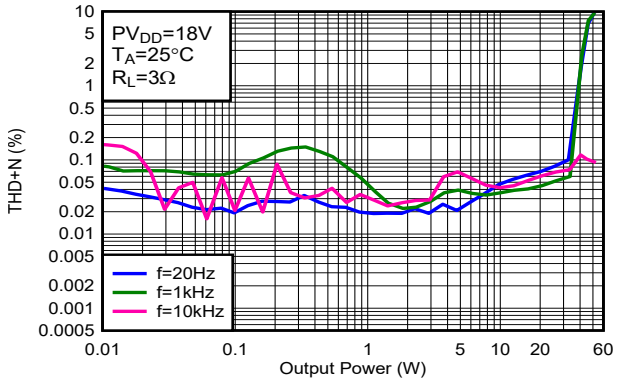
1SPW Modulation P_O=1W,2.5W,5W
F_{SW}=768kHz Load = 3Ω PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-101. THD+N vs Frequency



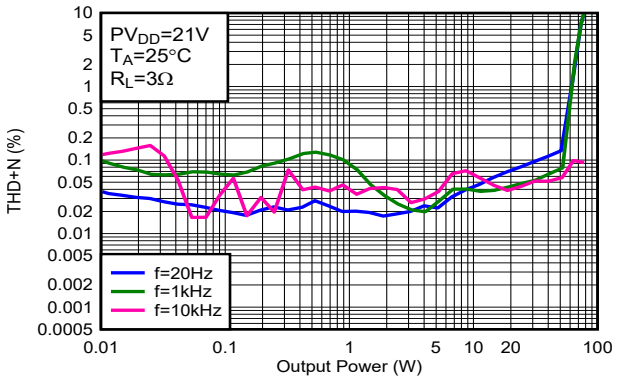
1SPW Modulation
FSW=768kHz PVDD = 13.5V PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-102. THD+N vs Output Power



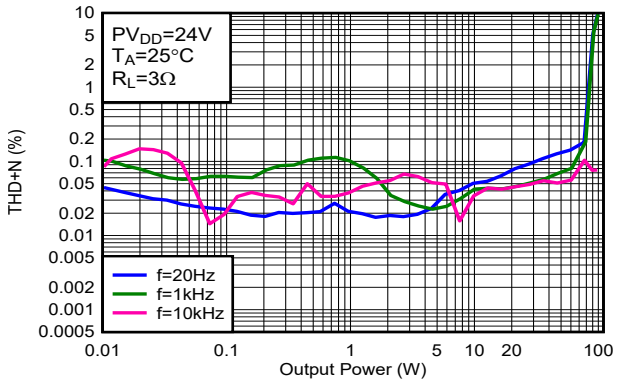
1SPW Modulation
FSW=768kHz PVDD = 18V PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-103. THD+N vs Output Power



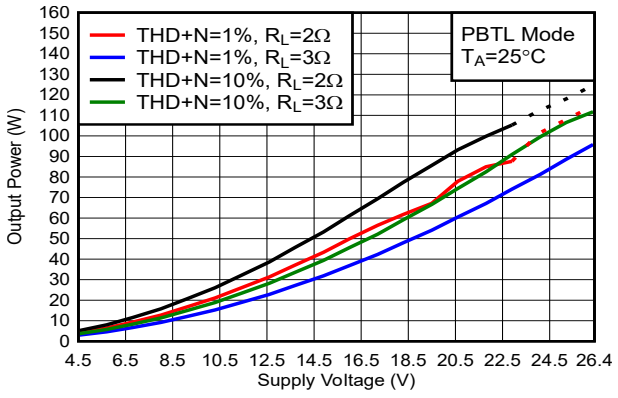
1SPW Modulation
FSW=768kHz PVDD = 21V PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-104. THD+N vs Output Power



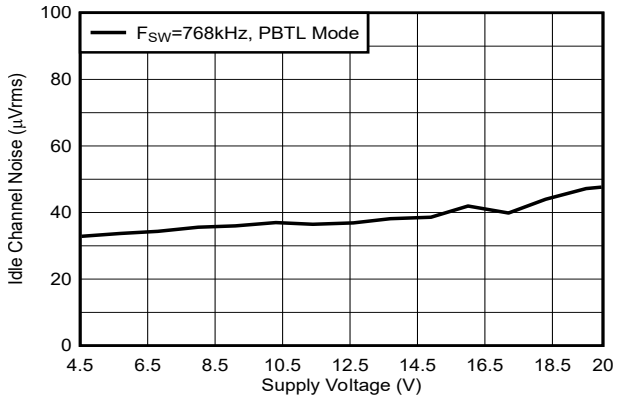
1SPW Modulation
FSW=768kHz PVDD = 24V PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-105. THD+N vs Output Power



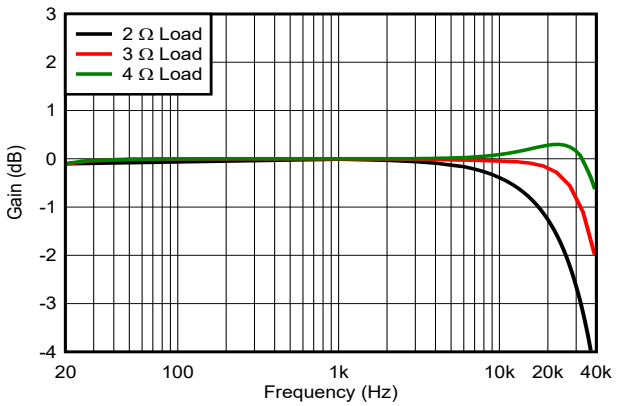
1SPW Modulation
FSW=768kHz Load = 2, 3Ω PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-106. Output Power vs Supply Voltage (dotted line is thermally limited)



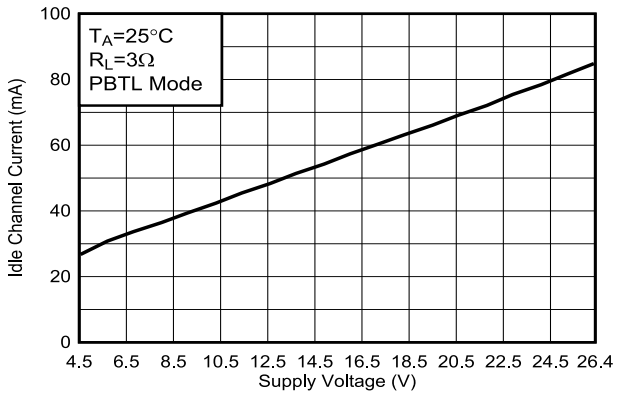
1SPW Modulation
FSW=768kHz Load = 3Ω PBTL Mode
175kHz Class D Amplifier Loop Bandwidth

図 6-107. Idle Channel Noise vs Supply Voltage



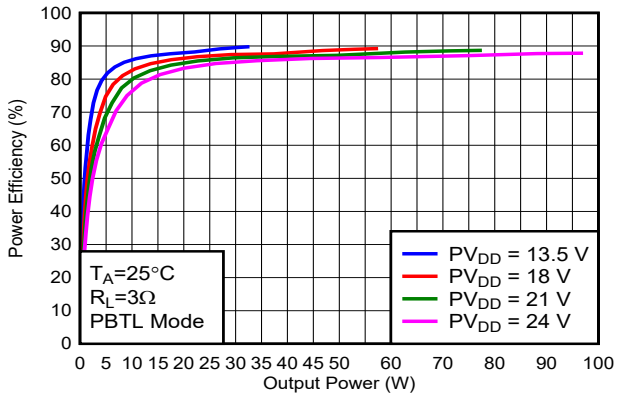
1SPW Modulation P_O=1W PVDD=13.5V
F_{SW}=768kHz PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-108. Gain vs Frequency



1SPW Modulation
F_{SW}=768kHz Load = 3Ω PBTL Mode
175kHz Class D Amplifier Loop Bandwidth

図 6-109. PVDD Idle Current vs PVDD Voltage



1SPW Modulation
F_{SW}=768kHz Load = 3Ω PBTL Mode
175 kHz Class D Amplifier Loop Bandwidth

図 6-110. Efficiency vs Output Power

7 Detailed Description

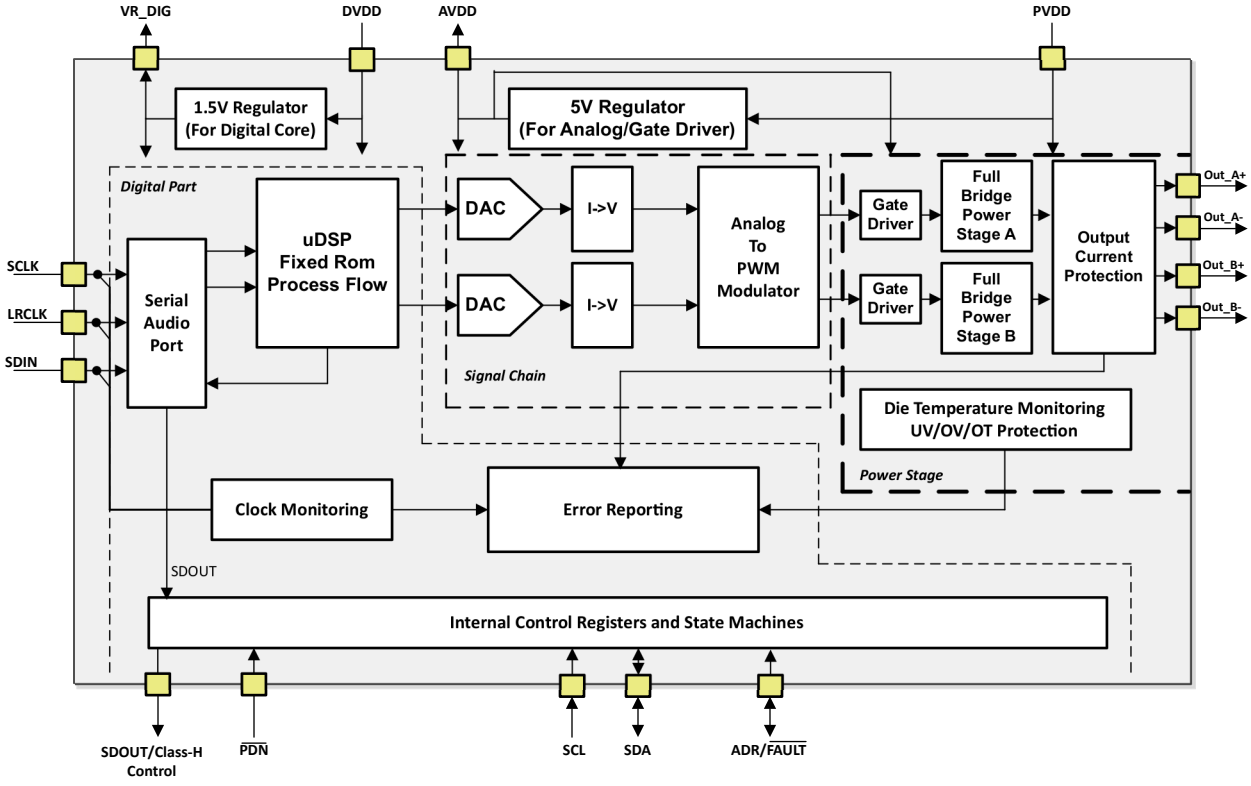
7.1 Overview

The TAS5815 device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

1. A stereo Digital to PWM Conversion block.
2. An Audio DSP subsystem.
3. A flexible close-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
4. An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. One internal LDO convert PVDD to 5 V for GVDD and AVDD.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supplies

To facilitate system design, TAS5815 needs only a 3.3V or 1.8V supply in addition to the (typical) 12V or 26.4V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (GVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

7.3.2 Device Clocking

The TAS5815 device has flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

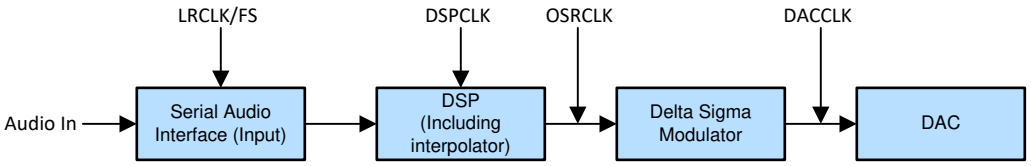


図 7-1. Audio Flow with Respective Clocks

図 7-1 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left Right Word Clock and Frame Sync)
- SDIN (Input Data)
- SDOUT (Output Data)

The device has an internal PLL that is used to take SCLK and create the higher rate clocks required by the DSP and the DAC clock.

The device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32kHz, 44.1kHz – 48kHz, 88.2kHz – 96kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

7.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK , and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

表 7-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I²S/LJ/RJ	32, 24, 20, 16	32 to 96	64, 32
		32	128
TDM	32, 24, 20, 16	44.1, 48	128, 256, 512
		96	128, 256

Before DSP register initialize with I²C during the start-up, TAS5815 requires stable I2S ready. When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

7.3.4 Serial Audio Port - Data Formats and Bit Depths

The serial audio interface port is a 3-wire serial port with the signals LRCK/FS, SCK, and SDIN. SCK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the device on the rising edge of SCK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

TAS5815 supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (Page0-Register 0x33 [5:4]). If the high width of LRCK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (Page0-Register 0x33 [3:2]) should set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in 表 7-1. The data formats are detailed in 図 6-1 through 図 6-110. The word length are selected via Register (Page0-Register 0x33 [1:0]). The offsets of data are selected via Register (Page0-Register 0x34 [7:0]). Default setting is I2S and 24 bit word length.

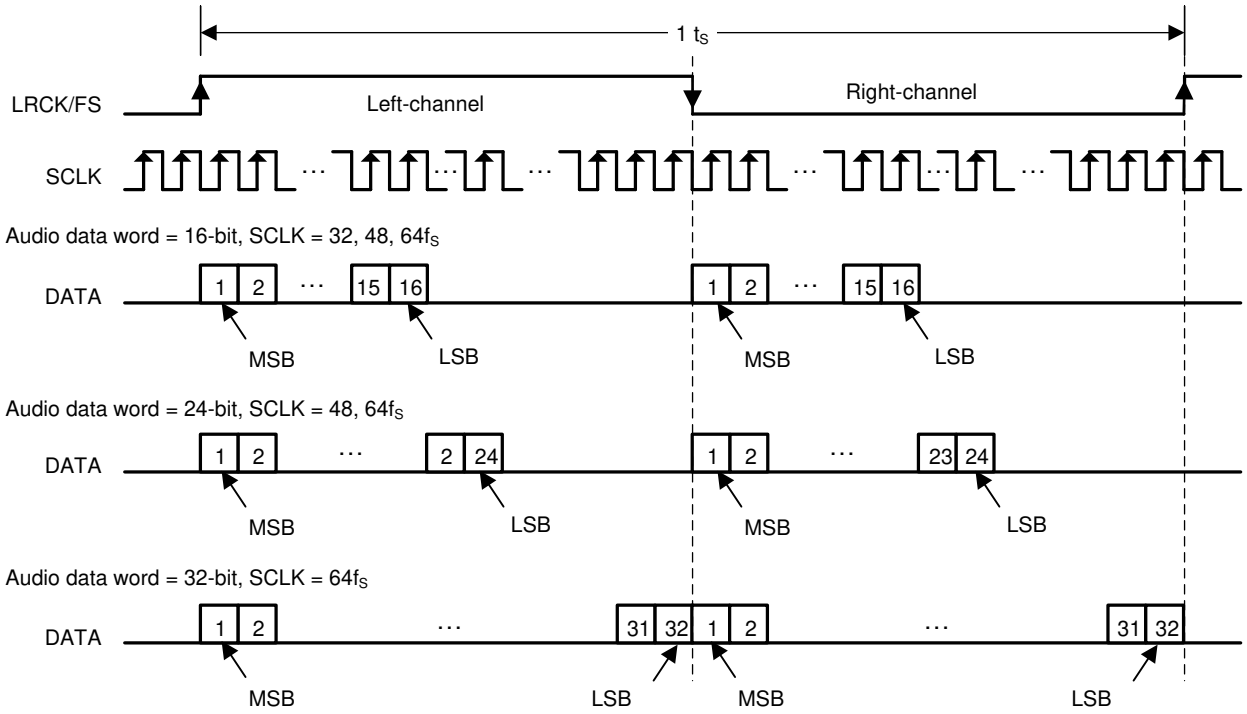
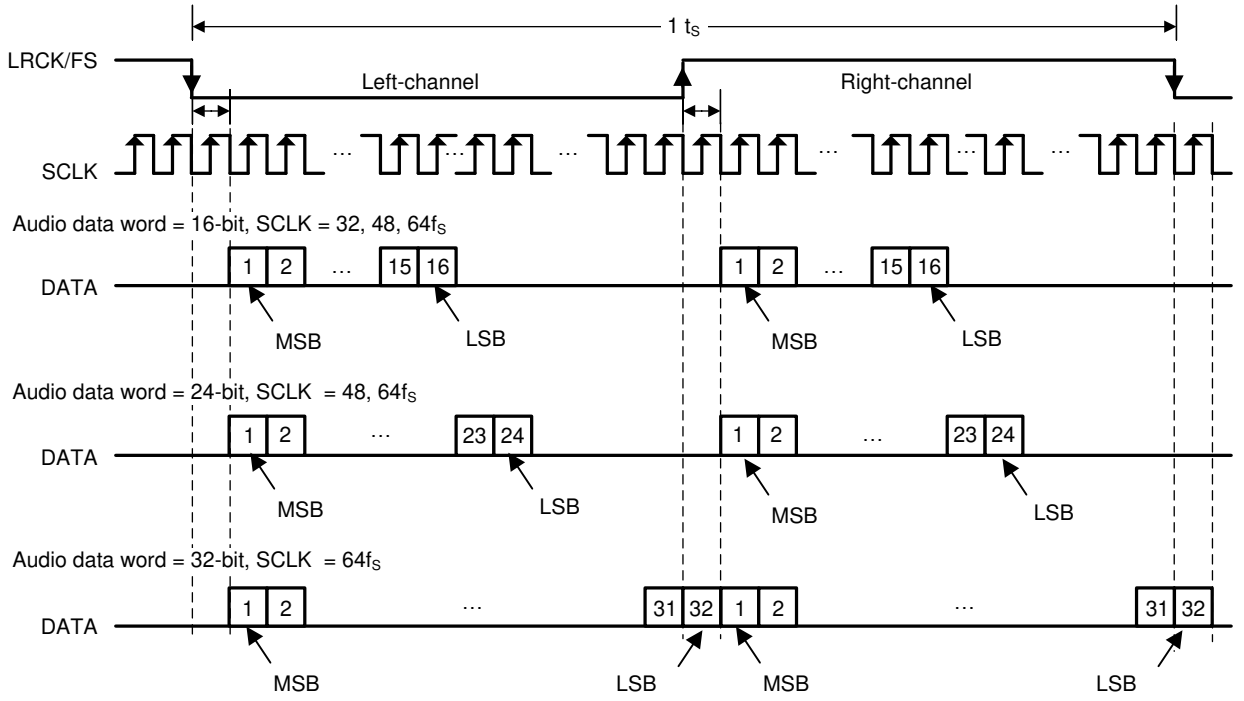
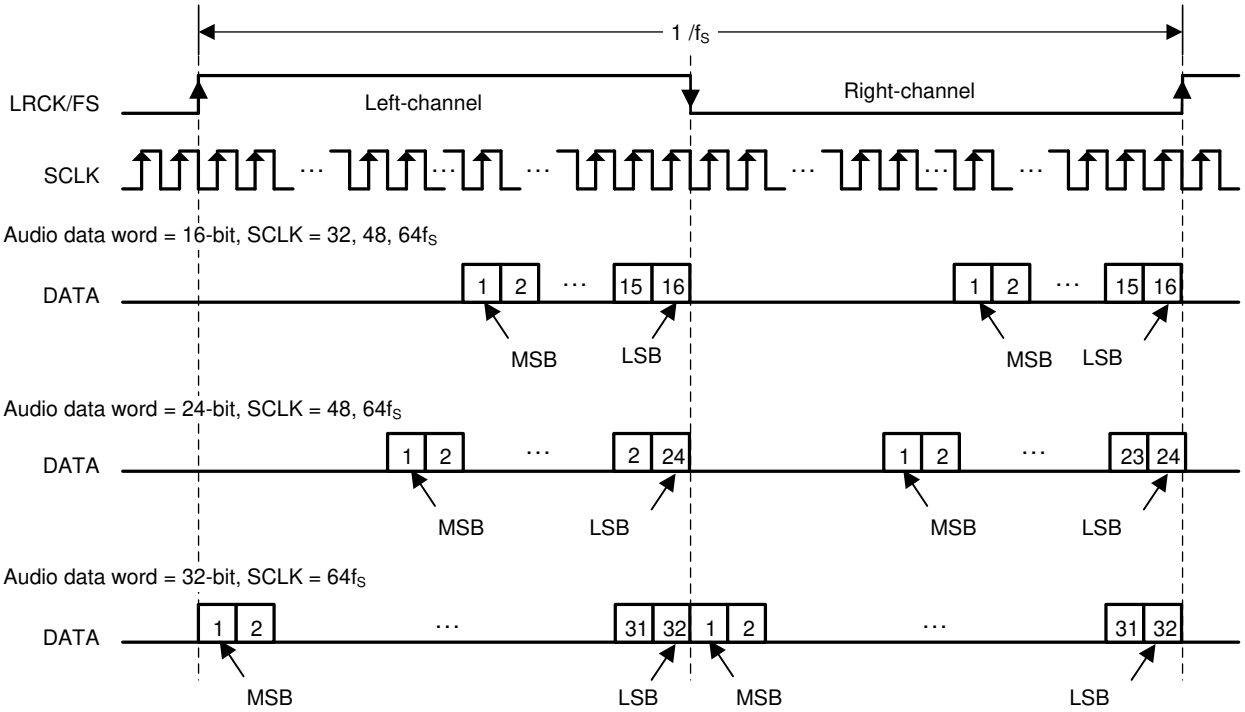


図 7-2. Left Justified Audio Data Format



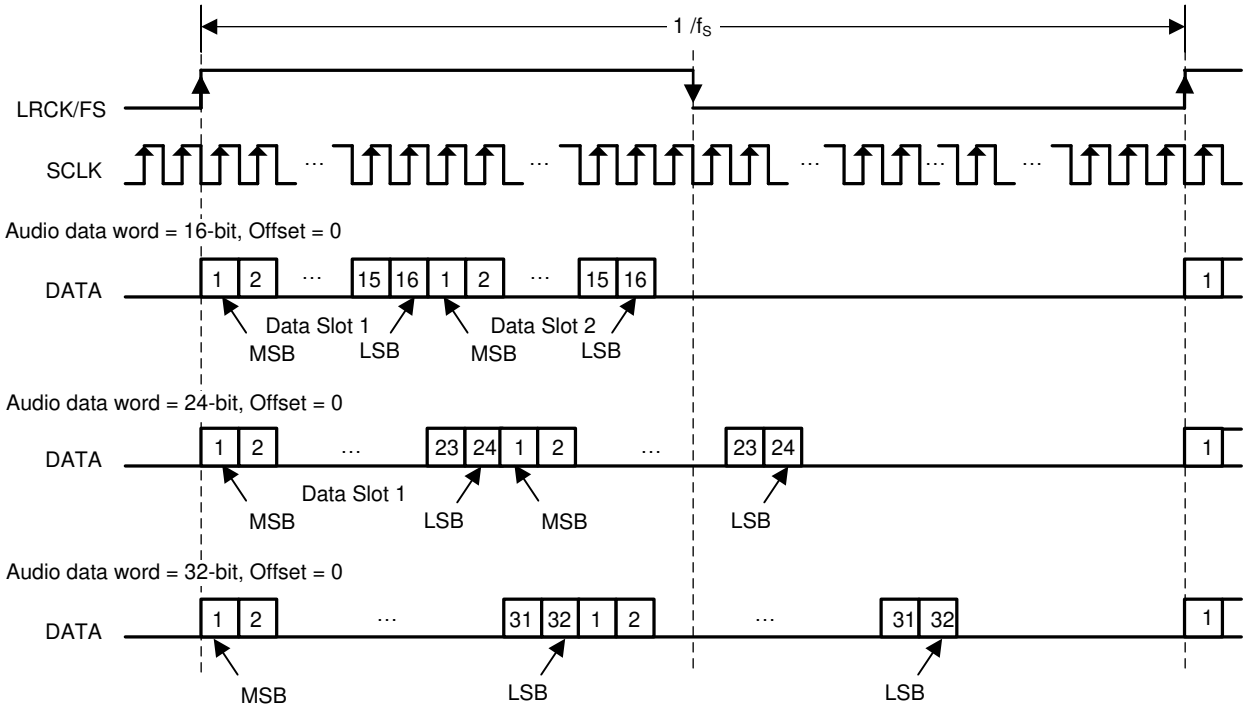
I²S Data Format; L-channel = LOW, R-channel = HIGH

図 7-3. I²S Audio Data Format



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

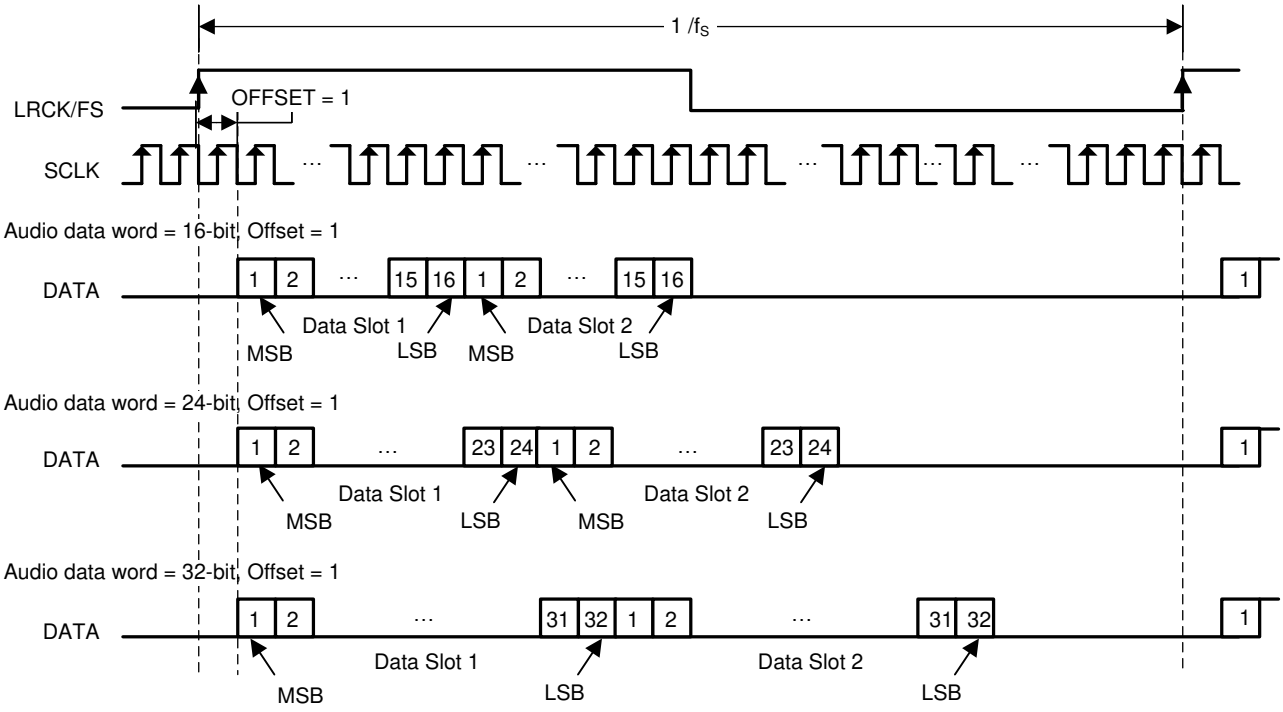
図 7-4. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

図 7-5. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

図 7-6. TDM 2 Audio Data Format

7.3.5 Clock Halt Auto-recovery

As some of host processor will Halt the I2S clock when there is no audio playing. When Clock halt, the device puts all channels into the Hi-Z state and reports Clock Error in Register 113 (Register Address 0x71). After audio clocks recovery, the device automatically returns to the previous state.

7.3.6 Sample Rate on the Fly Change

TAS5815 supports LRCLK(FS) rate on the fly change. For example, change LCRLK from 32kHz to 48kHz or 96kHz, Host processor needs to put the LRCLK(FS)/SCLK to Halt state at least 100μs before changing to the new sample rate.

7.3.7 Digital Audio Processing

TAS5815 DSP has a ROM fixed process flows which support 96kHz DSP sample rate. The digital audio processing includes 2 main functions: basic audio tuning blocks and Class-H algorithm.

Basic audio tuning blocks are SRC, stereo channel input mixer, 14 BQs for each channel, pop click free volume, multi-bands DRC and AGL.

Class-H can be used in conjunction with Hybrid Modulation, which is an innovative Class-D internal PWM modulation scheme to improve efficiency even more without compromising THD+N performance. Class-H goes beyond Hybrid PWM modulation from system efficiency perspective, by tracking audio signal envelope with an advanced look-ahead DSP structure, controlling the external PVDD supply voltage rail, and maintaining just enough margin to provide high dynamic range without clipping distortion to save as much power as possible. The Class-H details are listed here:

- 8 steps 384kHz PWM format Class-H control waveform for external DC-DC converter.
- Configurable max 2.5ms look-ahead audio signal delay buffer (5ms for PBTL mode), which provides capability to fit various application systems' DC-DC bandwidth and power supply coupling capacitance.
- Class-H Margin automatically adjusts audio signal trigger level and each step level. Fine tune it to achieve the balance between efficiency and envelope tracking speed.
- Control register to enable Class-H is DSP_MISC (0x66), bit 5. The default value, 0, disabled Class-H controller.

7.3.8 Class D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

7.3.8.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in 図 7-7, the audio path of the TAS5815 consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown in the digital audio path and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

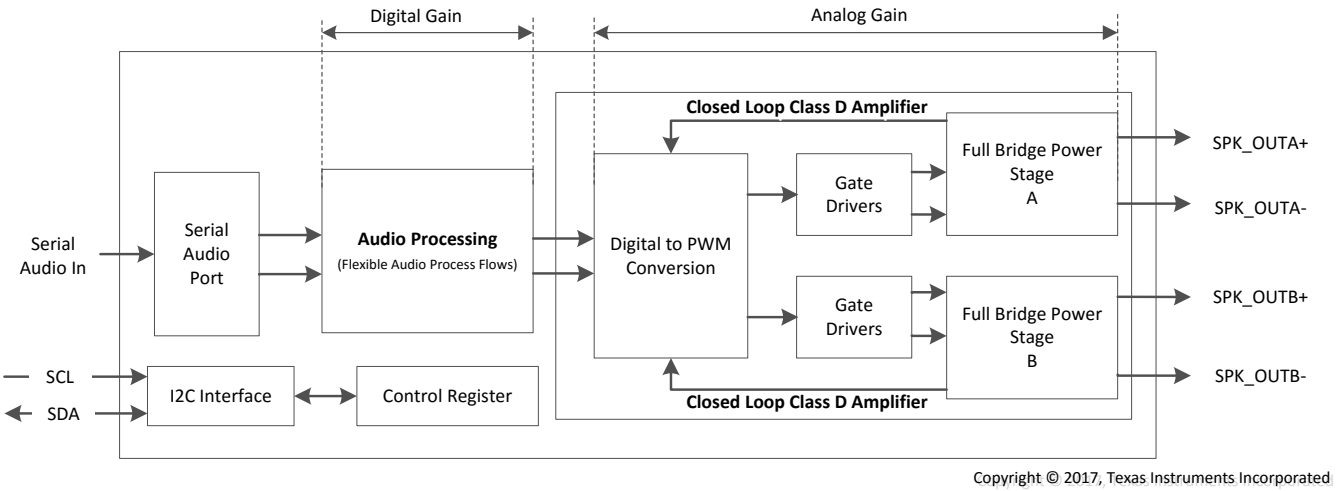


図 7-7. Speaker Amplifier Gain

As shown in 図 7-7, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0 dB by default, it does not change. For all settings of the register 0x54, AGAIN[4:0], the digital boost block remains at 0 dB. These gain settings ensure that the output signal is not clipping at different PVDD levels. 0dBFS output is 29.5-V peak output voltage

表 7-2. Analog Gain Setting

AGAIN <4:0>	GAIN (dBFS)	AMPLIFIER OUTPUT PEAK VOLTAGE (V)
00000	0	29.5
00001	-0.5	27.85
…….	……..	…….
11111	-15.5	4.95

7.4 Device Functional Modes

7.4.1 Software Control

The TAS5815 device is configured via an I^2 C communication port.

The I^2C Communication Protocol is detailed in the I^2C Communication Port section. The I^2C timing requirements are described in the I^2C Bus Timing – Standard and I^2C Bus Timing – Fast sections.

7.4.2 Speaker Amplifier Operating Modes

The TAS5815 device can be used in two different amplifier configurations:

- BTL Mode
- PBTL Mode

7.4.2.1 BTL Mode

The familiar BTL mode of operation uses the TAS5815 device to amplify two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-, the amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

7.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the TAS5815 device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor

portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the TAS5815 device, the input signal to the PBTL amplifier is left frame of I^2S or TDM data.

7.4.3 Low EMI Modes

TAS5815 employs several modes to minimize EMI during playing audio, and they can be used based on different applications.

7.4.3.1 Minimize EMI with Spread Spectrum

This device supports spread spectrum with triangle mode. Spread spectrum is used to minimize the EMI noise.

User needs to configure register RAMP_SS_CTRL0 (0x6B) to Enable triangle mode and enable spread spectrum. Select spread spectrum frequency and range with RAMP_SS_CTRL1 (0x6C). For 384 kHz FSW which configured by DEVICE_CTRL1 (0x02), the spread spectrum frequency and range are described in 表 7-3.

表 7-3. Spectrum frequency and range

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

- User Application example 1:

Central Switching Frequency is 384kHz, Triangle Frequency is 24kHz, take I^2C device address 0x58 as an example:

w A8 6b 01 //Enable Spread Spectrum

w A8 6c 03 //RAMP_SS_CTRL[3:0]0011, Triangle Frequency = 24kHz, Spread Spectrum Range should be 25% (336 kHz ~ 432 kHz)

- User Application example 2:

Central Switching Frequency is 768 kHz, Triangle Frequency is 24 kHz, take I^2C device address 0x58 as an example:

w A8 6b 01 //Enable Spread Spectrum

w A8 6c 0f //RAMP_SS_CTRL[3:0]1111, Triangle Frequency = 24 kHz, Spread Spectrum Range should be 20% (700 kHz ~ 860 kHz)

7.4.3.2 Minimize EMI with channel to channel phase shift

This device support channel to channel 180 degree PWM phase shift to minimize the EMI. Bit 0 of ANA_CTRL Register 0x53 can be used to disable or enable the phase shift.

注

Only BD mode supports channel to channel 180 degree PWM phase shift.

7.4.3.3 Minimize EMI with Multi-Devices PWM Phase Synchronization

This device support up to 4 phases selection for multiple device application systems. For example, when a system integrates four TAS5815 devices, the user can select phase 0, 1, 2, or 3 for each device by register RAMP_PHASE_CTRL (0x6A), which means there is a 45 degree phase shift between each device to minimize the EMI.

Recommend to do the Phase Synchronization with I^2S clock during the Startup Phase:

1. Halt I^2S clock.

2. Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A = 0x00 for device 0; Register 0x6A = 0x04 for device 1; Register 0x6A = 0x08 for device 2; Register 0x6A = 0x0C for device 3. There should be a 45 degree PWM phase shift between each device to minimize the EMI.
3. Configure each device into Hi-Z mode.
4. Provide I^2S to each device. Phase synchronization for all 4 devices are automatically done by internal sequence.
5. Initialize the DSP code. (This step can be skipped if only need to do the PWM Phase Synchronization).
6. Device to Device PWM phase shift should be fixed with 45 degree.

7.4.4 Thermal Foldback

The Thermal Foldback (TFB), is designed to protect TAS5815 from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the TAS5815 to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning (OTW) level (135C typ), an internal AGL (Automatic Gain Limiter) will reduce the digital gain automatically. Once the die temperature drops below the OTW, the device's digital gain gradually returns to the former setting.

7.4.5 Device State Control

TAS5815 has 5 states with different power dissipation which listed in the *Electrical Characteristics* Table.

- Shutdown Mode. With PDN pin pull down to GND. All internal LDOs (1.5V for digital core, 5V for analog) are disabled, all registers are cleared to default value.

> 注
>
> Exit from Shutdown Mode and re-enter into Play mode, need to follow up the start-up sequence and reload all register configurations (which can be generated by PurePath Console3) again.

- Deep Sleep Mode. Register 0x68h [1:0]=00, device stays in Deep Sleep Mode. In this mode, I^2C block and 1.5V LDO for digital core still working, but internal 5V LDO (For AVDD and MOSFET gate driver) is disabled for low power dissipation. This mode can be used to extend the battery life in some portable speaker applications. If the host processor stops playing audio for a long time, can be set to Deep Sleep Mode to minimize power dissipation until host processor starts playing audio again. Unlike the Shutdown Mode (Pulling $\overline{\text{PDN}}$ Low), entering or exiting Deep Sleep Mode, the DSP keeps active.
- Sleep Mode. Register 0x68h [1:0]=01, device stays in Sleep Mode. In this mode, I^2C block, Digital core, DSP Memory, 5V Analog LDO are stilling working. Unlike the Shutdown Mode (Pull PDN Low), enter or exit Sleep Mode, DSP is kept active. Exit from this mode and re-enter into play mode, only need to set Register 0x68h [1:0]=11.
- Output Hi-Z Mode. Register 0x68h [1:0]=10, device stays in Hi-Z Mode. In this mode, only output driver is set to be Hi-Z state, all other block operate normally. Exit from this mode and re-enter into play mode, only need to set Register 0x68h [1:0]=11.
- Play Mode. Register 0x68h [1:0]=11, device stays in Play Mode.

7.4.6 Device Modulation

TAS5815 has 3 modulation schemes: BD Modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for with Register 0x02 [1:0]-DEVICE_CTRL1.

7.4.6.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The

voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

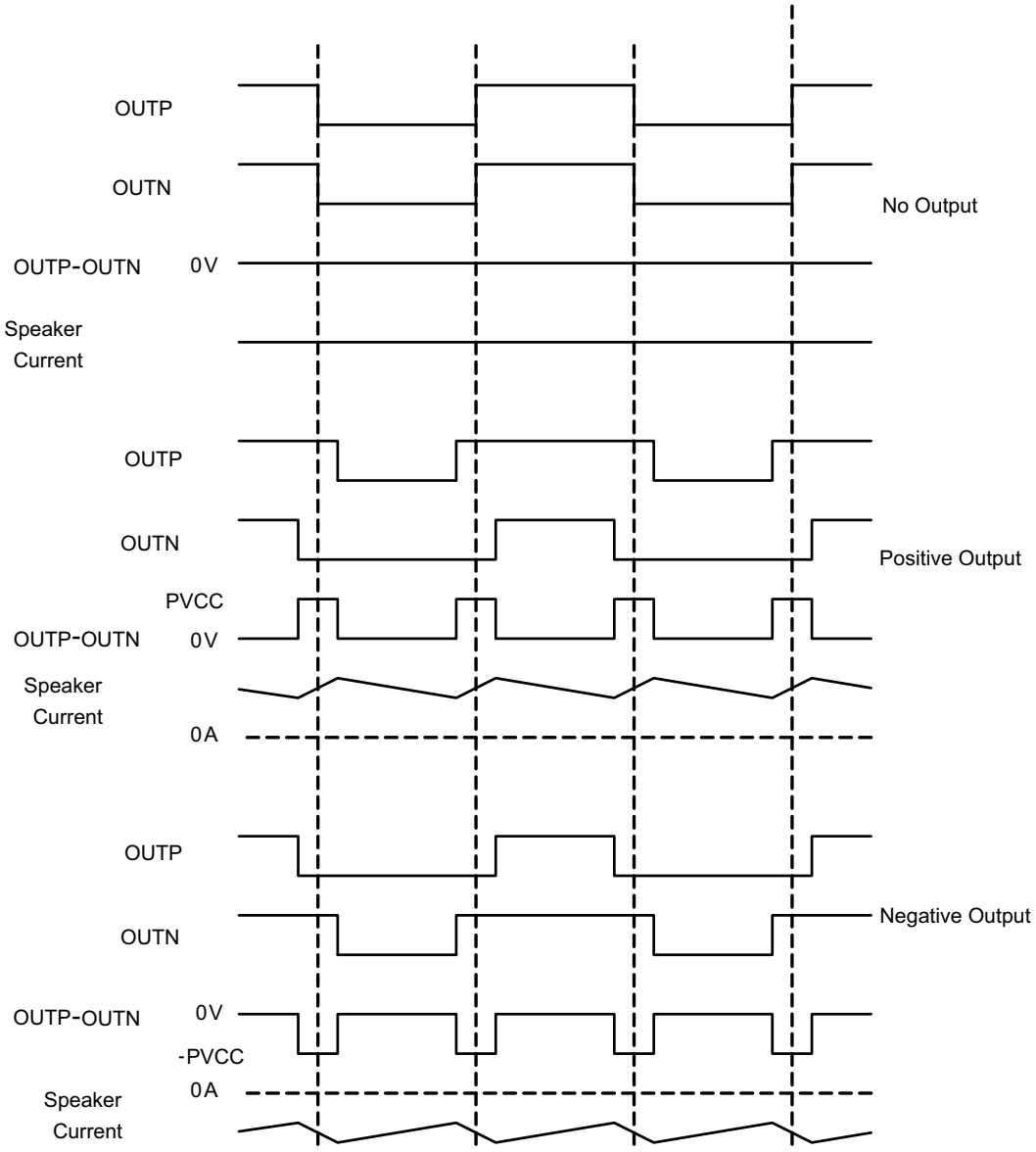


図 7-8. BD Mode Modualtion

7.4.6.2 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at ~17% modulation during idle conditions. When an audio signal is applied one output decreases and one increases. The decreasing output signal quickly rails to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

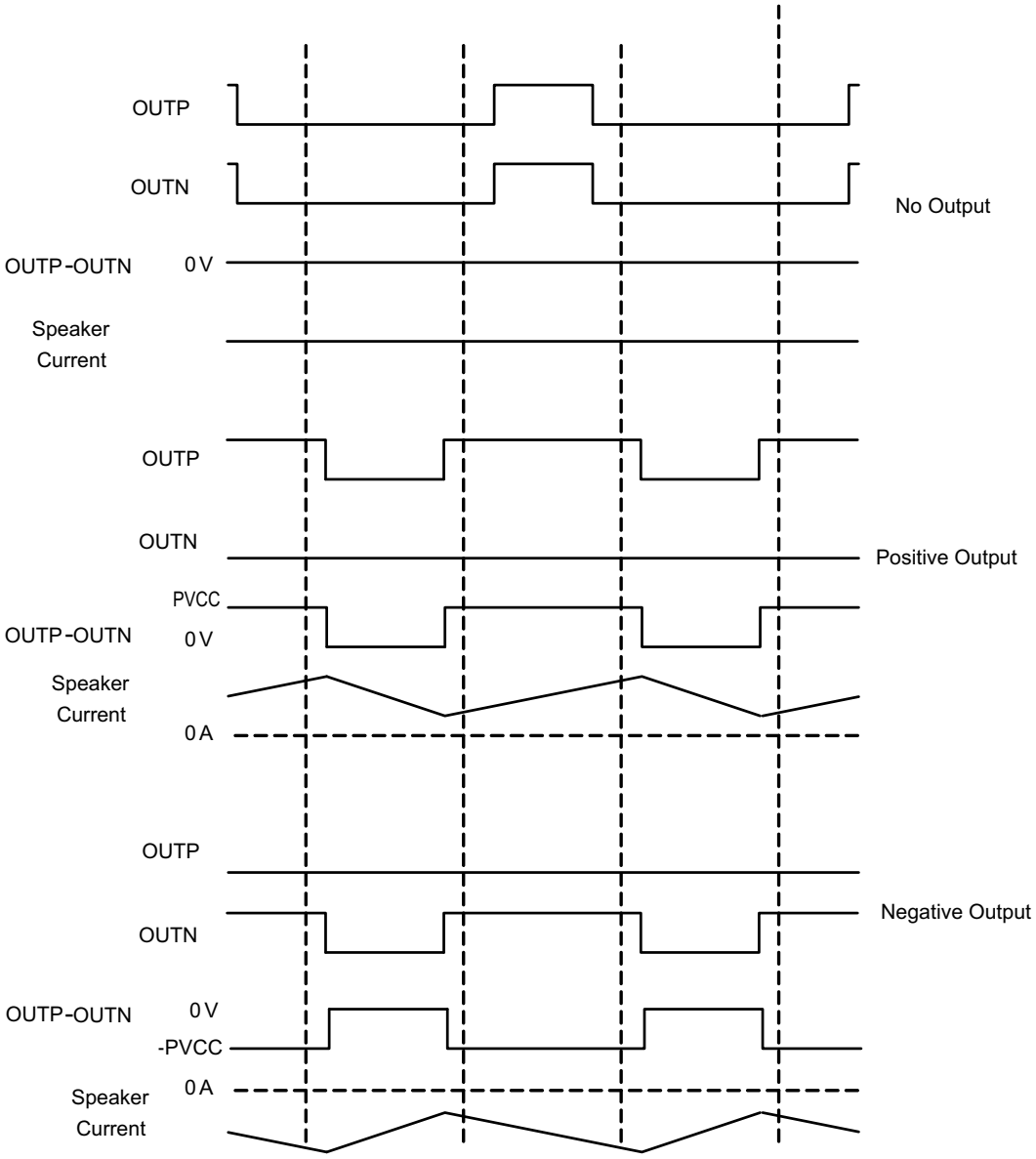


図 7-9. 1SPW Mode Modulation

7.4.6.3 Hybrid Modulation

Hybrid Modulation is designed to minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation enabled, the device detects the input signal level and adjust PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra low idle current and maintains the same audio performance level as the BD Modulation. In order to minimize the power dissipation, low switching frequency (For example, Fsw = 384kHz) with proper LC filter (15µH + 0.68µF or 22µH + 0.68µF) is recommended. Follow these steps when using Hybrid Modulation:

1) With Hybrid Modulation, users need to input the system's PVDD value via device development application.

2) With Hybrid Modulation, Change device state from Deep Sleep Mode to Play Mode, specific sequence is required:

1. Set device's PWM Modulation to BD or 1SPW mode via Register (Book0/Page0/Register0x02h, Bit [1:0]).
2. Set device to Hi-Z state via Register (Book0/Page0/Register0x03h, Bit [1:0]).
3. Delay 2ms.

4. Set device's PWM Modulation to Hybrid mode via Register (Book0/Page0/Register0x02h, Bit [1:0]).
5. Delay 15ms.
6. Set device to Play state via Register (Book0/Page0/Register0x03h, Bit [1:0]).

7.4.7 Load Detect

This device support Short Load Detect and Open Load Detect. The Short Load Detection reports if either of the channels or both has a load impedance smaller than the limits in the Specification section. The Open Load Detection reports if either of the channels or both has a load impedance greater than the limits in the Specification section

7.4.7.1 Short Load Detect

Follow these steps to use the Short Load Detection.

1. Mute the input digital signal chain, set device's output driver into play mode. Register 0x03 = 0x0F.
2. Configure and enable short load detection. Register 0x7B = 0x03; Register 0x7A = 0xC9.
3. Wait 20 ms.
4. Read back short load status from Register 0x7C. Short load result only valid when DONE bit is 1.

注

- Take Short Load Report of CH2 in PBTL mode.

7.4.7.2 Open Load Detect

Follow these steps to use the Open Load Detection.

1. Mute the input digital signal chain, set device's output driver into play mode. Register 0x03 = 0x0F.
2. Configure and enable open load detection. Register 0x7B = 0x09; Register 0x79 = 0xC0.
3. Wait 20 ms.
4. Read back open load status from Register 0x7C. Open load result only valid when DONE bit is 1.
5.

注

Take Open Load Report of CH2 in PBTL mode.

7.5 Programming and Control

7.5.1 I²C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with the Inter IC (I^2C) bus protocol and supports 100 and 400-kbps data transfer rates for random and sequential write and read operations as a target device. Because the TAS5815 register map and DSP memory spans multiple pages and books, the user should change from page to page or book to book before writing individual register or DSP memory. Changing from book to book is accomplished via register 0x7F on page 0x00 of each book. Changing from page to page is accomplished via register 0x00 on each page. This register value selects the page address, from 0 to 255.

7.5.2 Target Address

The TAS5815 device has 7 bits for the target address. The first five bits (MSBs) of the target address are factory preset to 10101(0xAx). The next two bits of address byte are the device select bits which can be user-defined by ADR pin in 表 7-4.

表 7-4. I² C Target Address Configuration

ADR/ FAULT PIN Configuration	MSBs					User Define		LSB
4.7k Ω to DVDD	1	0	1	0	1	0	0	R/ $\overline{W}$
15kΩ to DVDD	1	0	1	0	1	0	1	R/ $\overline{W}$
47kΩ to DVDD	1	0	1	0	1	1	0	R/ $\overline{W}$

表 7-4. I² C Target Address Configuration (続き)

ADR/ $\overline{\text{FAULT}}$ PIN Configuration	MSBs					User Define		LSB
120kΩ to DVDD	1	0	1	0	1	1	1	R/ $\overline{\text{W}}$

7.5.2.1 Random Write

As shown in 図 7-10, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

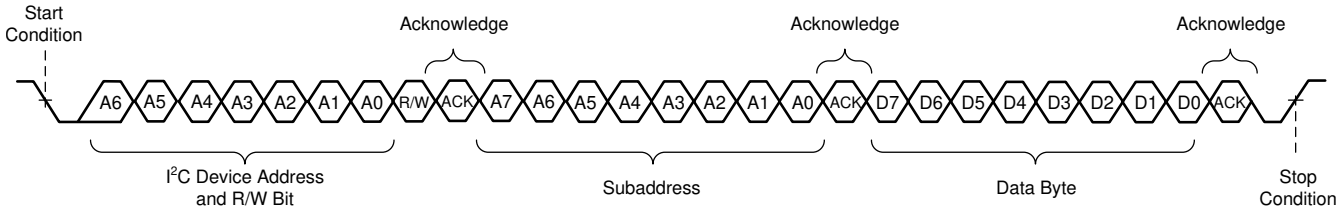


図 7-10. Random Write Transfer

7.5.2.2 Random Read

As shown in 図 7-11, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

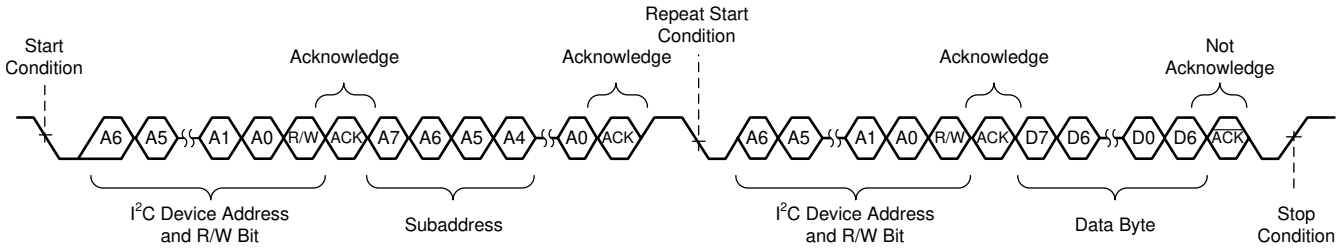


図 7-11. Random Read Transfer

7.5.2.3 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in 図 7-12. After receiving each data byte, the device responds with an acknowledge bit and the I² subaddress is automatically incremented by one.

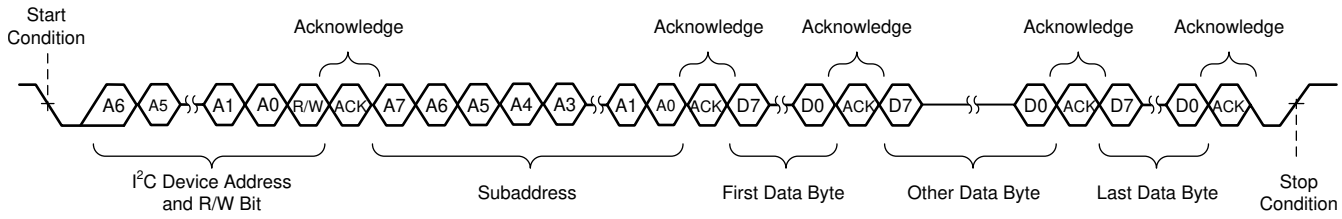


図 7-12. Sequential Write Transfer

7.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in 図 7-13. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I^2C sub address by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

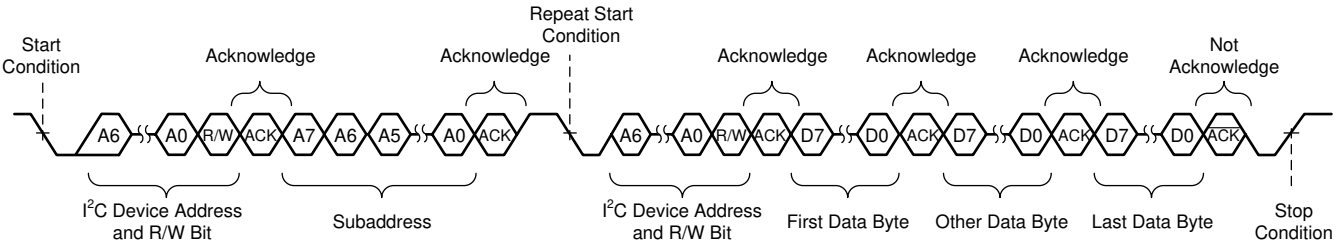


図 7-13. Sequential Read Transfer

7.5.2.5 DSP Memory Book, Page and BQ update

The TAS5815 device supports the I^2C serial bus and the data transmission protocol for standard and fast mode as a target device.

The DSP memory is arranged in books, pages, and registers. Each book has several pages and each page has several registers.

Because the TAS5815 register map spans several books and pages, the user must select the correct book and page before writing individual register bits or bytes.

To change the book, the user must be on page 0x00. In register 0x7f on page 0x00 you can change the book. On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in Book 0xAA. The five coefficients of every Biquad Filter should be written entirely and sequentially from the lowest address to the highest.

7.5.2.6 Example Use

The following is a sample script for configuring a device on I^2C target address 0xA8 and set the device switching frequency to 768kHz with Class D loop bandwidth to 175kHz, BD Modulation:

- w A8 00 00 #Go to Page0
- w A8 7f 00 #Change the Book to 0x00
- w A8 00 00 #Go to Page 0x00
- w A8 02 01 #Set switching frequency to 768kHz with 1SPW Modulation
- w A8 53 60 #Set Class D Loop Bandwidth to 175kHz

Example 2, The following is a sample script for configuring a device on I^2C target address 0xA8 and using the DSP host memory to change the digital volume to the default value of 0dB:

- w A8 00 00 #Go to Page 0
- w A8 7f 8c #Change the Book to 0x8C
- w A8 00 2a #Go to Page 0x2a
- w A8 24 00 80 00 00 #change digital volume to 0 dB

7.5.2.7 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers

will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

7.5.2.7.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1 + x1 + x2 + x8)). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I^2C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

7.5.2.7.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

7.5.3 Control via Software

- Startup Procedures
- Shutdown Procedures

7.5.3.1 Startup Procedures

1. Configure ADR/ $\overline{\text{FAULT}}$ pin with proper setting for I^2C device address.
2. Bring up power supplies (it does not matter if PVDD or DVDD comes up first).
3. Once all power supplies are stable, bring up the $\overline{\text{PDN}}$ HIGH, wait 5ms ,then start SCLK, LRCLK.
4. Once I2S clock are stable, configure the device via the I^2C control port based on the user cases (Make sure the $\overline{\text{PDN}}$ pin = HIGH before I^2C control port operating).
5. The device is now in normal operation.

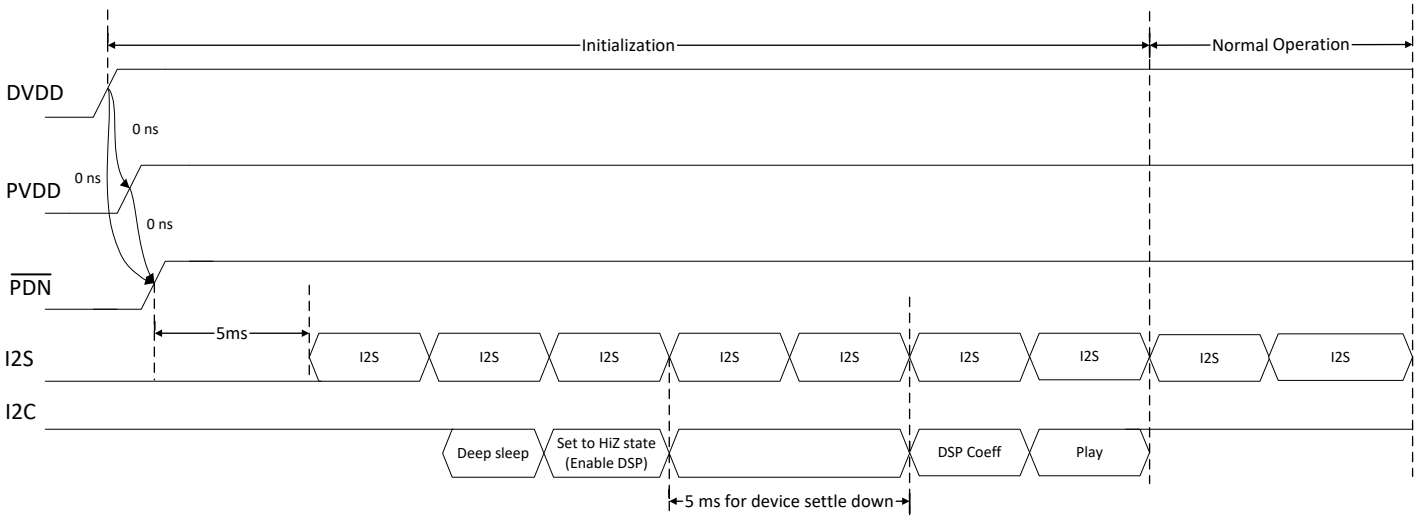
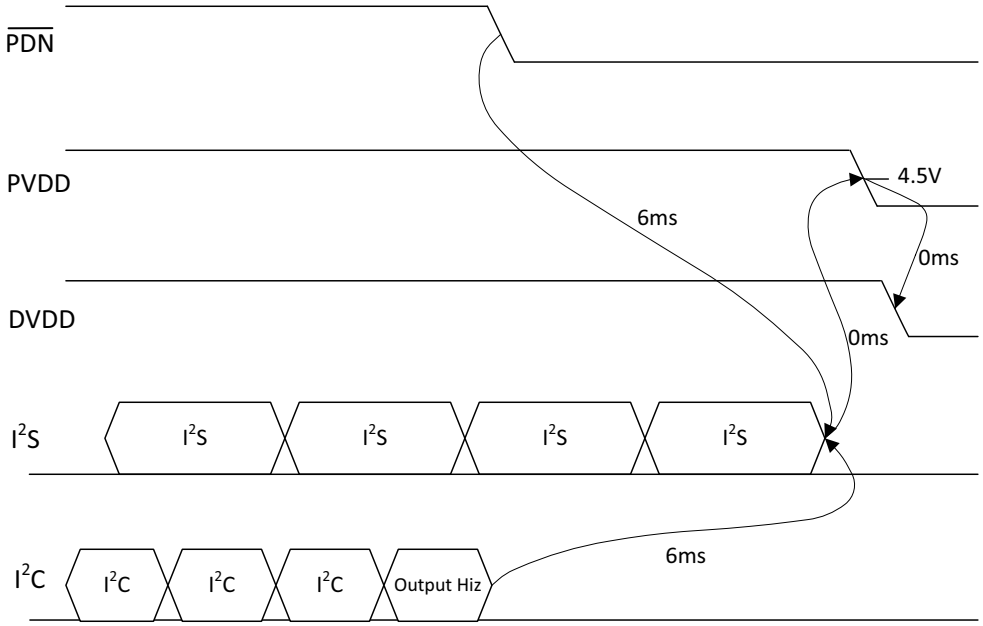


図 7-14. Startup sequence

7.5.3.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the DEVICE_CTRL2 Register [1:0]=00 (DEEP SLEEP) via the I²C control port or Pull $\overline{\text{PDN}}$ low.
3. The clocks can now be stopped and the power supplies brought down.
4. The device is now fully shutdown and powered off.



A. Before PVDD/DVDD power down, Class D Output driver needs to be disabled by $\overline{\text{PDN}}$ or by I²C.

B. At least 6ms delay needed based on: LRCLK (Fs) = 48kHz, digital volume =24dB, digital volume ramp down by 0.5dB every sample period. Changing the value of DIG_VOL_CTRL2 or DIG_VOL_CTRL3 registers or changing the or change the LRCLK rate will change the delay time.

図 7-15. Power down sequence

7.5.3.3 Protection and Monitoring

7.5.3.3.1 Overcurrent Shutdown (OCSD)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in < 100ns if the peak current are enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. The user may restart the affected channel via I^2C. An OCSD event activates the fault pin, and the I^2C fault register saves a record. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

7.5.3.3.2 DC Detect

If the TAS5815 device measures a DC offset in the output voltage, the ADR/ $\overline{\text{FAULT}}$ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault.

7.5.3.3.3 Device Over Temperature Protection

Once the die temperature exceed 160°C (Typical), device will set the output driver from Play mode to Hi-Z Mode. Over temperature shutdown fault reported by GLOBAL_FAULT2 (0x72) register in Book0/Page0. Set this fault's behavior to Auto-recovery mode, device will come back to play mode automatically once the die temperature drop down to 150°C or device needs re-enter into play mode by clearing fault with FAULT_CLEAR (0x78) register in Book0/Page0.

7.5.3.3.4 Over Voltage Protection

Once the PVDD voltage exceeds the $OVE_{THRES(PVDD)}$, device will set the output driver from Play mode to Hi-Z mode. Over voltage fault reported by GLOBAL_FAULT1 (0x71) register in Book0/Page0. Once PVDD voltage returns to normal, device will come back to Play mode. But this bit still keeps 1 unless clear it by FAULT_CLEAR (0x78) register in Book0/Page0 manually.

7.5.3.3.5 Under Voltage Protection

Once the PVDD voltage drop below the $UVE_{THRES(PVDD)}$ (4 V Typical), device will set the output driver from Play mode to Hi-Z mode. Under voltage fault reported by GLOBAL_FAULT1 (0x71) register in Book0/Page0. Once PVDD rise above 4.25 V (Typical), device will come back to Play mode. But this bit still keeps 1 unless clear it by FAULT_CLEAR (0x78) register in Book0/Page0 manually.

7.5.3.3.6 Clock Fault

Once there has any Clock error occurs (Clock Halt, SCLK/LRCLK Ratio Error, Pll unlock, FS error) , セクション 8.1.12 and セクション 8.1.14 monitor these errors and real-time report with details, device will enter into Hi-Z mode. Clock Fault reported in セクション 8.1.35 in Book0/Page0. Once the clock error been removed, device will come back to play mode automatically. But this bit still keeps 1 unless clear it by セクション 8.1.41 in Book0/Page0 manually.

8 Register Maps

8.1 CONTROL PORT Registers

表 8-1 lists the memory-mapped registers for the CONTROL_PORT registers. All register offset addresses not listed in 表 8-1 should be considered as reserved locations and the register contents should not be modified.

表 8-1. CONTROL_PORT Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Reset control	Go
2h	DEVICE_CTRL1	Device control 1	Go
3h	DEVICE_CTRL2	Device control 2	Go
Fh	I2C_PAGE_AUTO_INC	I2C DSP memory access page auto increment	Go
28h	SIG_CH_CTRL	Signal chain control	Go
29h	CLOCK_DET_CTRL	Clock detection control	Go
30h	SDOUT_SEL	SDOUT selection	Go
31h	I2S_CTRL	I2S control 0	Go
33h	SAP_CTRL1	I2S control 1	Go
34h	SAP_CTRL2	I2S control 2	Go
35h	SAP_CTRL3	I2S control 3	Go
37h	FS_MON	FS monitor	Go
38h	BCLK_MON	Bclk monitor	Go
39h	CLKDET_STATUS	Clock detection status	Go
40h	DSP_PGM_MODE	DSP program mode	Go
46h	DSP_CTRL	DSP control	Go
4Ch	DAC_GAIN_LEFT	Left digital volume	Go
4Dh	DAC_GAIN_RIGHT	Right digital volume	Go
4Eh	DIG_VOL_CTRL2	Digital volume control 2	Go
4Fh	DIG_VOL_CTRL3	Digital volume control 3	Go
50h	AUTO_MUTE_CTRL	Auto mute control	Go
51h	AUTO_MUTE_TIME	Auto mute time	Go
53h	ANA_CTRL	Analog control	Go
54h	AGAIN	Analog gain	Go
60h	ADR_CTRL	ADR control	Go
61h	ADR_SEL	ADR output selection	Go
66h	DSP_MISC	DSP misc data	Go
67h	DIE_ID	DIE ID	Go
68h	POWER_STATE	Power State	Go
69h	AUTOMUTE_STATE	Auto mute state	Go
6Ah	RAMP_PHASE_CTRL	Switching clock phase control	Go
6Bh	RAMP_SS_CTRL0	Spread spectrum control 0	Go
6Ch	RAMP_SS_CTRL1	Spread spectrum control 1	Go
70h	CHAN_FAULT	Channel fault	Go
71h	GLOBAL_FAULT1	Global fautl 1	Go
72h	GLOBAL_FAULT2	Global fautl 2	Go
73h	OT_WARNING	OT Warning	Go
74h	PIN_CONTROL1	Pin control 1	Go
75h	PIN_CONTROL2	Pin control 2	Go
76h	MISC_CONTROL	Miscellaneous control	Go
78h	FAULT_CLEAR	Fault clear	Go

表 8-1. CONTROL_PORT Registers (続き)

Offset	Acronym	Register Name	Section
79h	OLD_CONTROL	Open load detection control	Go
7Ah	SLD_CONTROL1	Short load detection control 1	Go
7Bh	SLD_CONTROL2	Short load detection control 2	Go
7Ch	LD_REPORT	Load detection report	Go

Complex bit access types are encoded to fit into small table cells. 表 8-2 shows the codes that are used for access types in this section.

表 8-2. CONTROL_PORT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 RESET_CTRL Register (Offset = 1h) [Reset = 00h]

RESET_CTRL is shown in 図 8-1 and described in 表 8-3.

Return to the Summary Table.

Reset control

図 8-1. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
W-0h			W-0h	W-0h			W-0h

表 8-3. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	W	0h	
4	RST_MOD	W	0h	WRITE CLEAR BIT Reset Modules This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in hiz mode. **0: Normal** 1: Reset modules
3-1	RESERVED	W	0h	
0	RST_REG	W	0h	WRITE CLEAR BIT Reset Registers This bit resets the mode registers back to their initial values. The RAM content is not cleared. This bit is auto cleared and must be set only when the DAC is in hiz mode (resetting registers when the DAC is running is prohibited and not supported) **0: Normal** 1: Reset mode registers

8.1.2 DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h]

DEVICE_CTRL1 is shown in 図 8-2 and described in 表 8-4.

Return to the Summary Table.

Device control 1

図 8-2. DEVICE_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	PBTL_MODE	MODULATION	
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	

表 8-4. DEVICE_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	FSW_SEL	R/W	0h	Select PWM switching frequency(Fsw) **3'b 000:768kHz** 3'b 001:384kHz 3'b 101:1.024MHz Others reserved
3	RESERVED	R/W	0h	
2	PBTL_MODE	R/W	0h	**0: Set device to BTL mode** 1:Set device to PBTL mode
1-0	MODULATION	R/W	0h	**00:BD mode** 01:1SPW mode 10:Hybrid mode 11: Reserved

8.1.3 DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h]

DEVICE_CTRL2 is shown in 図 8-3 and described in 表 8-5.

Return to the Summary Table.

Device control 2

図 8-3. DEVICE_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED			DSP_RST	CH1_MUTE	CH2_MUTE	STATE_CTL	
R/W-0h			R/W-1h	R/W-0h	R/W-0h	R/W-0h	

表 8-5. DEVICE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	DSP_RST	R/W	1h	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation **1: Reset the DSP**
3	CH1_MUTE	R/W	0h	Mute Channel 1 This bit issues soft mute request for the ch1. The volume will be smoothly ramped down/up to avoid pop/click noise. **0: Normal volume** 1: Mute
2	CH2_MUTE	R/W	0h	Mute Channel 2 This bit issues soft mute request for the ch2. The volume will be smoothly ramped down/up to avoid pop/click noise. **0: Normal volume** 1: Mute
1-0	STATE_CTL	R/W	0h	Device state control register **00: Deep Sleep** 01: Sleep 10: Hi-Z 11: PLAY

8.1.4 I2C_PAGE_AUTO_INC Register (Offset = Fh) [Reset = 00h]

I2C_PAGE_AUTO_INC is shown in 図 8-4 and described in 表 8-6.

Return to the Summary Table.

I2C DSP memory access page auto increment

図 8-4. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_INC	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

表 8-6. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	PAGE_INC	R/W	0h	Page auto increment disable Disable page auto increment mode. for non-zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. **0: Enable Page auto increment** 1: Disable Page auto increment
2-0	RESERVED	R/W	0h	

8.1.5 SIG_CH_CTRL Register (Offset = 28h) [Reset = 00h]

SIG_CH_CTRL is shown in 図 8-5 and described in 表 8-7.

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Signal chain control

図 8-5. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
BCLK_RATIO				FS_MODE			
R/W-0h				R/W-0h			

表 8-7. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BCLK_RATIO	R/W	0h	These bits indicate the configured BCLK ratio, the number of BCLK clocks in one audio frame. **4'b0000: Auto detection** 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS Others reserved.
3-0	FS_MODE	R/W	0h	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. **4'b0000 Auto detection** 4'b0110 32kHz 4'b1000 44.1kHz 4'b1001 48kHz 4'b1010 88.2kHz 4'b1011 96kHz Others Reserved

8.1.6 CLOCK_DET_CTRL Register (Offset = 29h) [Reset = 00h]

CLOCK_DET_CTRL is shown in 図 8-6 and described in 表 8-8.

Return to the Summary Table.

Clock detection control

図 8-6. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DET_PLL	BCLK_RANGE	DET_FS	DET_BCLK	DET_BCLKMISS	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

表 8-8. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	DET_PLL	R/W	0h	Ignore PLL overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. **0: Regard PLL overrate detection** 1: Ignore PLL overrate detection
5	BCLK_RANGE	R/W	0h	Ignore BCLK Range Detection This bit controls whether to ignore the BCLK range detection. The BCLK must be stable between 256kHz and 50MHz or an error will be reported. When ignored, a BCLK range error will not cause a clock error. **0: Regard BCLK Range detection** 1: Ignore BCLK Range detection
4	DET_FS	R/W	0h	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error. But CLKDET_STATUS will report fs error. **0: Regard FS detection** 1: Ignore FS detection
3	DET_BCLK	R/W	0h	Ignore BCLK Detection This bit controls whether to ignore the BCLK detection against LRCLK. The BCLK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCLK error will not cause a clock error. **0: Regard BCLK detection** 1: Ignore BCLK detection
2	DET_BCLKMISS	R/W	0h	Ignore BCLK Missing Detection This bit controls whether to ignore the BCLK missing detection. When ignored an BCLK missing will not cause a clock error. **0: Regard BCLK missing detection** 1: Ignore BCLK missing detection
1-0	RESERVED	R/W	0h	

8.1.7 SDOUT_SEL Register (Offset = 30h) [Reset = 04h]

SDOUT_SEL is shown in 図 8-7 and described in 表 8-9.

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SDOUT selection

図 8-7. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED					CLASSH_LOGIC	SDOUT_MOD	SDOUT_SEL
R/W-0h					R/W-1h	R/W-0h	R/W-0h

表 8-9. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	CLASSH_LOGIC	R/W	1h	When classH enable, device is not in play state **01: Set the SDOUT PIN to high** 00: Set the SDOUT PIN to low
1	SDOUT_MOD	R/W	0h	Set SDOUT as open drain. This bit only applies to GPO functions with Output push-pull mode and has no effect on functions that use Open Drain mode by default **0: Output Push-pull mode** 1: Open drain mode
0	SDOUT_SEL	R/W	0h	SDOUT Select This bit selects what is being output as SDOUT via GPIO pins. **0: SDOUT is the DSP output (post-processing)** 1: SDOUT is the DSP input (pre-processing)

8.1.8 I2S_CTRL Register (Offset = 31h) [Reset = 00h]

I2S_CTRL is shown in 図 8-8 and described in 表 8-10.

Return to the Summary Table.

I2S control 0

図 8-8. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_INV	RESERVED				
R/W-0h		R/W-0h	R/W-0h				

表 8-10. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	BCLK_INV	R/W	0h	BCLK Polarity This bit sets the inverted BCLK mode. In inverted BCLK mode, the DAC assumes that the LRCLK and DIN edges are aligned to the rising edge of the BCLK. Normally they are assumed to be aligned to the falling edge of the BCLK. **0: Normal BCLK mode** 1: Inverted BCLK mode
4-0	RESERVED	R/W	0h	

8.1.9 SAP_CTRL1 Register (Offset = 33h) [Reset = 02h]

SAP_CTRL1 is shown in 図 8-9 and described in 表 8-11.

Return to the Summary Table.

I2S control 1

図 8-9. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
SHIFT_MSB	RESERVED	DATA_FMT		LRCLK_PULSE		FRAME_LENGTH	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-2h	

表 8-11. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SHIFT_MSB	R/W	0h	I2S Shift MSB. Combine with the 8 bits in low register 34h.
6	RESERVED	R/W	0h	
5-4	DATA_FMT	R/W	0h	I2S Data Format These bits control both input and output audio interface formats for DAC operation. **00: I2S** 01: DSP/TDM 10: RTJ 11: LTJ
3-2	LRCLK_PULSE	R/W	0h	If the LRCLK pulse is shorter than 8 x BCLK, set bit 0-1 to '01' Otherwise, keep these bits as default value '00' **00: High width of LRCLK pulse is equal or greater than 8 cycles of BCLK** 01: High width of LRCLK pulse is less than 8 cycles of BCLK
1-0	FRAME_LENGTH	R/W	2h	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits **10: 24 bits** 11: 32 bits

8.1.10 SAP_CTRL2 Register (Offset = 34h) [Reset = 00h]

SAP_CTRL2 is shown in 図 8-10 and described in 表 8-12.

Return to the Summary Table.

I2S control 2

図 8-10. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
SHIFT_LSB							
R/W-0h							

表 8-12. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SHIFT_LSB	R/W	0h	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. **8'b00000000: offset = 0 BCLK (no offset)** 8'b00000001: ofsset = 1 BCLK 8'b00000010: offset = 2 BCLKs … 8'b11111111: offset = 512 BCLKs

8.1.11 SAP_CTRL3 Register (Offset = 35h) [Reset = 11h]

SAP_CTRL3 is shown in 図 8-11 and described in 表 8-13.

Return to the Summary Table.

I2S control 3

図 8-11. SAP_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		CH1_DAC		RESERVED		CH2_DAC	
R/W-0h		R/W-1h		R/W-0h		R/W-1h	

表 8-13. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	CH1_DAC	R/W	1h	Channel 1 DAC Data Path These bits control the channel 1 audio data path connection. 00: Zero data (mute) **01: Ch1 data** 10: Ch2 data 11: Reserved (do not set)
3-2	RESERVED	R/W	0h	
1-0	CH2_DAC	R/W	1h	Channel 2 DAC Data Path These bits control the channel 2 audio data path connection. 00: Zero data (mute) **01: Ch2 data** 10: Ch1 data 11: Reserved (do not set)

8.1.12 FS_MON Register (Offset = 37h) [Reset = 00h]

FS_MON is shown in 図 8-12 and described in 表 8-14.

Return to the Summary Table.

FS monitor

図 8-12. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		BCLKRATION_MSB		FS_MON			
R-0h		R-0h		R-0h			

表 8-14. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	BCLKRATION_MSB	R	0h	2 MSB of detected BCLK ratio. These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. Combine with the 8 bits in low register 38h. BCLK = 32 FS~512 FS
3-0	FS_MON	R	0h	These bits indicate the currently detected audio sampling rate. **4'b0000 FS Error** 4'b0010 8kHz 4'b0100 16kHz 4'b0110 32kHz 4'b1000 Reserved 4'b1001 48kHz 4'b1011 96kHz Others Reserved

8.1.13 BCLK_MON Register (Offset = 38h) [Reset = 00h]

BCLK_MON is shown in 図 8-13 and described in 表 8-15.

Return to the Summary Table.

Bclk monitor

図 8-13. BCLK_MON Register

7	6	5	4	3	2	1	0
BCLKRATIO_LSB							
R-0h							

表 8-15. BCLK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLKRATIO_LSB	R	0h	These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. BCLK = 32 FS~512 FS

8.1.14 CLKDET_STATUS Register (Offset = 39h) [Reset = 00h]

CLKDET_STATUS is shown in 図 8-14 and described in 表 8-16.

Return to the Summary Table.

Clock detection status

図 8-14. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_OVERRATE	PLL_OVERRATE	PLL_LOCKED	BCLK_MISSING	BCLK_VALID	FS_VALID
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-16. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	BCLK_OVERRATE	R	0h	This bit indicates whether the BCLK is overrate or underrate. **0: BCLK is underrate** 1: BCLK is overrate
4	PLL_OVERRATE	R	0h	This bit indicates whether the PLL is overrate or not. **0: PLL is underrate** 1: PLL is overrate
3	PLL_LOCKED	R	0h	This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. **0: PLL is locked** 1: PLL is not locked
2	BCLK_MISSING	R	0h	This bit indicates whether the BCLK is missing or not. **0: BCLK is normal** 1: BCLK is missing
1	BCLK_VALID	R	0h	This bit indicates whether the BCLK is valid or not. The BCLK ratio must be stable and in the range of 32-512FS to be valid. **0: BCLK is valid** 1: BCLK is not valid
0	FS_VALID	R	0h	In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid. In non auto detection mode(reg_fsmode!=0), FS error indicates that configured sampling frequency set by LRCLK(FS) is different with detected sampling frequency. Even if FS Error Detection Ignore is set, this flag will be also asserted. **0: Sampling rate is valid** 1: Not valid

8.1.15 DSP_PGM_MODE Register (Offset = 40h) [Reset = 01h]

DSP_PGM_MODE is shown in 図 8-15 and described in 表 8-17.

Return to the Summary Table.

DSP program mode

図 8-15. DSP_PGM_MODE Register

7	6	5	4	3	2	1	0
RESERVED				CH1_HIZ	CH2_HIZ	RESERVED	
R/W-0h				R/W-0h	R/W-0h	R/W-1h	

表 8-17. DSP_PGM_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	CH1_HIZ	R/W	0h	**0: Normal operation** 1: Force CH1 to Hi-Z mode
2	CH2_HIZ	R/W	0h	**0: Normal operation** 1: Force CH2 to Hi-Z mode
1-0	RESERVED	R/W	1h	

8.1.16 DSP_CTRL Register (Offset = 46h) [Reset = 01h]

DSP_CTRL is shown in 図 8-16 and described in 表 8-18.

Return to the Summary Table.

DSP control

図 8-16. DSP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			PROC_RATE	RESERVED			
R/W-0h			R/W-0h	R/W-1h			

表 8-18. DSP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	PROC_RATE	R/W	0h	0: 96k processing flow, 2.0 processing SRC enabled **1: 48k processing flow, 2.1 processing flow enabled**
3-0	RESERVED	R/W	1h	

8.1.17 DAC_GAIN_LEFT Register (Offset = 4Ch) [Reset = 30h]

DAC_GAIN_LEFT is shown in 図 8-17 and described in 表 8-19.

Return to the Summary Table.

Left digital volume

図 8-17. DAC_GAIN_LEFT Register

7	6	5	4	3	2	1	0
CH1_PGA							
R/W-30h							

表 8-19. DAC_GAIN_LEFT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_PGA	R/W	30h	Channel 1 Volume These bits control the ch1 digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 8'b00000000: +24.0 dB 8'b00000001: +23.5 dB … 8'b00101111: +0.5 dB **8'b00110000: 0.0 dB** 8'b00110001: -0.5 dB ... 8'b11111110: -103 dB 8'b11111111: Mute

8.1.18 DAC_GAIN_RIGHT Register (Offset = 4Dh) [Reset = 30h]

DAC_GAIN_RIGHT is shown in 図 8-18 and described in 表 8-20.

Return to the Summary Table.

Right digital volume

図 8-18. DAC_GAIN_RIGHT Register

7	6	5	4	3	2	1	0
CH2_PGA							
R/W-30h							

表 8-20. DAC_GAIN_RIGHT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_PGA	R/W	30h	Channel 2 Volume These bits control the ch2 digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 8'b00000000: +24.0 dB 8'b00000001: +23.5 dB … 8'b00101111: +0.5 dB **8'b00110000: 0.0 dB** 8'b00110001: -0.5 dB ... 8'b11111110: -103 dB 8'b11111111: Mute

8.1.19 DIG_VOL_CTRL2 Register (Offset = 4Eh) [Reset = 33h]

DIG_VOL_CTRL2 is shown in 図 8-19 and described in 表 8-21.

Return to the Summary Table.

Digital volume control 2

図 8-19. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
VNDF		VNDS		VNUF		VNUS	
R/W-0h		R/W-3h		R/W-0h		R/W-3h	

表 8-21. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VNDF	R/W	0h	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VNDS	R/W	3h	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
3-2	VNUF	R/W	0h	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	VNUS	R/W	3h	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update **11: Increment by 0.5 dB for each update**

8.1.20 DIG_VOL_CTRL3 Register (Offset = 4Fh) [Reset = 30h]

DIG_VOL_CTRL3 is shown in 図 8-20 and described in 表 8-22.

Return to the Summary Table.

Digital volume control 3

図 8-20. DIG_VOL_CTRL3 Register

7	6	5	4	3	2	1	0
VEDF		VEDS		RESERVED			
R/W-0h		R/W-3h		R/W-0h			

表 8-22. DIG_VOL_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VEDF	R/W	0h	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VEDS	R/W	3h	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update **11: Decrement by 0.5 dB for each update**
3-0	RESERVED	R/W	0h	

8.1.21 AUTO_MUTE_CTRL Register (Offset = 50h) [Reset = 00h]

AUTO_MUTE_CTRL is shown in 図 8-21 and described in 表 8-23.

Return to the Summary Table.

Auto mute control

図 8-21. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					AM_CTL	AMUTE_CH2	AMUTE_CH1
R/W-0h					R/W-0h	R/W-0h	R/W-0h

表 8-23. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	AM_CTL	R/W	0h	**0: Auto mute channel 1 and channel 2 independently** 1: Auto mute channel 1 and channel 2 only when both channels are about to be auto muted
1	AMUTE_CH2	R/W	0h	Auto Mute Channel 2 This bit enables or disables auto mute on Channel 2 **0: Disable Channel 2 auto mute** 1: Enable Channel 2 auto mute
0	AMUTE_CH1	R/W	0h	Auto Mute Channel 1 This bit enables or disables auto mute on Channel 1 **0: Disable Channel 1 auto mute** 1: Enable Channel 1 auto mute

8.1.22 AUTO_MUTE_TIME Register (Offset = 51h) [Reset = 55h]

AUTO_MUTE_TIME is shown in 図 8-22 and described in 表 8-24.

Return to the Summary Table.

Auto mute time

図 8-22. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	CH1_AMT			RESERVED	CH2_AMT		
R/W-0h	R/W-5h			R/W-0h	R/W-5h		

表 8-24. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	CH1_AMT	R/W	5h	Auto Mute Time for Channel 1 These bits specify the length of consecutive zero samples at ch1 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec **101: 1.065 sec** 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0h	
2-0	CH2_AMT	R/W	5h	Auto Mute Time for Channel 2 These bits specify the length of consecutive zero samples at ch2 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec **101: 1.065 sec** 110: 2.665 sec 111: 5.33 sec

8.1.23 ANA_CTRL Register (Offset = 53h) [Reset = 00h]

ANA_CTRL is shown in 図 8-23 and described in 表 8-25.

Return to the Summary Table.

Analog control

図 8-23. ANA_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	BW_CTL			RESERVED			PHASE_CTL
R/W-0h	R/W-0h			R/W-0h			R/W-0h

表 8-25. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-5	BW_CTL	R/W	0h	Class D Loop Bandwidth **00: 100kHz** 01: 80kHz 10: 120kHz 11: 175kHz When Fsw=384kHz, 100kHz bandwidth is selected for high audio performance. With Fsw=768kHz, 175kHz bandwidth should be selected for high audio performance.
4-1	RESERVED	R/W	0h	
0	PHASE_CTL	R/W	0h	**0: Out of phase** 1: In phase

8.1.24 AGAIN Register (Offset = 54h) [Reset = 00h]

AGAIN is shown in 図 8-24 and described in 表 8-26.

Return to the Summary Table.

Analog gain

図 8-24. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED			AGAIN				
R/W-0h			R/W-0h				

表 8-26. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-0	AGAIN	R/W	0h	Analog Gain Control This bit controls the analog gain **00000: 0 dB** 00001:-0.5 dB …… 11111: -15.5 dB

8.1.25 ADR_CTRL Register (Offset = 60h) [Reset = 00h]

ADR_CTRL is shown in 図 8-25 and described in 表 8-27.

Return to the Summary Table.

ADR control

図 8-25. ADR_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							ADR_OE
R/W-0h							R/W-0h

表 8-27. ADR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	ADR_OE	R/W	0h	ADR Output Enable This bit sets the direction of the ADR pin **0: ADR is input** 1: ADR is output

8.1.26 ADR_SEL Register (Offset = 61h) [Reset = 00h]

ADR_SEL is shown in 図 8-26 and described in 表 8-28.

Return to the Summary Table.

ADR output selection

図 8-26. ADR_SEL Register

7	6	5	4	3	2	1	0
RESERVED			ADR_SEL				
R/W-0h			R/W-0h				

表 8-28. ADR_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-0	ADR_SEL	R/W	0h	**b'00000: off (low)** b'00011: Auto mute flag (asserted when both L and R channels are auto muted) b'00100: Auto mute flag for left channel b'00101: Auto mute flag for right channel b'00110: Clock invalid flag (clock error or clock missing) b'00111: PLL lock flag b'01000: Warning b'01001: Serial audio interface data output (SDOUT) b'01011: ADR as FAULTZ output Others: reserved

8.1.27 DSP_MISC Register (Offset = 66h) [Reset = 00h]

DSP_MISC is shown in 図 8-27 and described in 表 8-29.

Return to the Summary Table.

DSP misc data

図 8-27. DSP_MISC Register

7	6	5	4	3	2	1	0
RESERVED		DSP_MISC	RESERVED				
R/W-0h		R/W-0h	R/W-0h				

表 8-29. DSP_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	DSP_MISC	R/W	0h	**0: Class-H disable** 1: Class-H enable
4-0	RESERVED	R/W	0h	

8.1.28 DIE_ID Register (Offset = 67h) [Reset = A7h]

DIE_ID is shown in 図 8-28 and described in 表 8-30.

Return to the Summary Table.

DIE ID

図 8-28. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R-A7h							

表 8-30. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	A7h	The Die ID for TAS5815

8.1.29 POWER_STATE Register (Offset = 68h) [Reset = 00h]

POWER_STATE is shown in 図 8-29 and described in 表 8-31.

Return to the Summary Table.

Power State

図 8-29. POWER_STATE Register

7	6	5	4	3	2	1	0
RESERVED						STATE_RPT	
R-0h						R-0h	

表 8-31. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1-0	STATE_RPT	R	0h	**00: Deep sleep** 01: Sleep 10: Hi-Z 11: Play

8.1.30 AUTOMUTE_STATE Register (Offset = 69h) [Reset = 00h]

AUTOMUTE_STATE is shown in 図 8-30 and described in 表 8-32.

Return to the Summary Table.

Auto mute state

図 8-30. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						CH2MUTE_STATUS	CH1MUTE_STATUS
R-0h						R-0h	R-0h

表 8-32. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	CH2MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 2. **0: Not auto muted** 1: Auto muted
0	CH1MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 1. **0: Not auto muted** 1: Auto muted

8.1.31 RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h]

RAMP_PHASE_CTRL is shown in 図 8-31 and described in 表 8-33.

Return to the Summary Table.

Switching clock phase control

図 8-31. RAMP_PHASE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				RAMPPHASE_SEL		RESERVED	
R/W-0h				R/W-0h		R/W-0h	

表 8-33. RAMP_PHASE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-2	RAMPPHASE_SEL	R/W	0h	Select ramp clock phase when multi devices are integrated in one system to reduce EMI and peak supply peak current, it is recomended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. **00: 0 degree** 01: 45 degree 10: 90 degree 11: 135 degree all of above have a 45 degree of phase shift
1-0	RESERVED	R/W	0h	Use I2S to synchronize output PWM phase 0: Disable 1: Enable
0	PHASE_SYNC_EN	R/W	0h	0: RAMP phase sync disable 1: RAMP phase sync enable

8.1.32 RAMP_SS_CTRL0 Register (Offset = 6Bh) [Reset = 00h]

RAMP_SS_CTRL0 is shown in 図 8-32 and described in 表 8-34.

Return to the Summary Table.

Spread spectrum control 0

図 8-32. RAMP_SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED						RDM_EN	TRI_EN
R/W-0h						R/W-0h	R/W-0h

表 8-34. RAMP_SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	RDM_EN	R/W	0h	**0: Random SS disable** 1: Random SS enable
0	TRI_EN	R/W	0h	**0: Triangle SS disable** 1: Triangle SS enable

8.1.33 RAMP_SS_CTRL1 Register (Offset = 6Ch) [Reset = 00h]

RAMP_SS_CTRL1 is shown in 図 8-33 and described in 表 8-35.

Return to the Summary Table.

Spread spectrum control 1

図 8-33. RAMP_SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RDM_CTL			TRI_CTL			
R/W-0h	R/W-0h			R/W-0h			

表 8-35. RAMP_SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	RDM_CTL	R/W	0h	Random SS range control For Fsw of 384kHz **3'b000: SS range +/- 0.62%** 3'b010: SS range +/- 1.88% 3'b011: SS range +/- 4.38% 3'b100: SS range +/- 9.38% 3'b101: SS range +/- 19.38% Others: reserved For Fsw of 768kHz 3'b000: SS range - 1.25% 3'b001: SS range +/- 1.25% 3'b010: SS range +/- 3.75% 3'b011: SS range +/- 8.75% 3'b100: SS range +/- 18.75% 3'b101: SS range +/- 38.75% Others: reserved
3-0	TRI_CTL	R/W	0h	Triangle SS frequency and range control **4'b0000: 24kHz SS +/- 5%** 4'b0001: 24kHz SS +/- 10% 4'b0010: 24kHz SS +/- 20% 4'b0011: 24kHz SS +/- 25% 4'b0100: 48kHz SS +/- 5% 4'b0101: 48kHz SS +/- 10% 4'b0110: 48kHz SS +/- 20% 4'b0111: 48kHz SS +/- 25% 4'b1000: 32kHz SS +/- 5% 4'b1001: 32kHz SS +/- 10% 4'b1010: 32kHz SS +/- 20% 4'b1011: 32kHz SS +/- 25% 4'b1100: 16kHz SS +/- 5% 4'b1101: 16kHz SS +/- 10% 4'b1110: 16kHz SS +/- 20% 4'b1111: 16kHz SS +/- 25%

8.1.34 CHAN_FAULT Register (Offset = 70h) [Reset = 00h]

CHAN_FAULT is shown in 図 8-34 and described in 表 8-36.

Return to the Summary Table.

Channel fault

図 8-34. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1DC	CH2DC	CH1OC	CH2OC
R-0h				R-0h	R-0h	R-0h	R-0h

表 8-36. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	CH1DC	R	0h	Channel 1 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
2	CH2DC	R	0h	Channel 2 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	CH1OC	R	0h	Channel 1 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	CH2OC	R	0h	Channel 2 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

8.1.35 GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h]

GLOBAL_FAULT1 is shown in 図 8-35 and described in 表 8-37.

Return to the Summary Table.

Global fautl 1

図 8-35. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
RESERVED	BQWRTFAULT_FLAG	RESERVED			CLKFAULT_FLAG	PVDDOV_FLAG	PVDDUV_FLAG
R-0h	R-0h	R-0h			R-0h	R-0h	R-0h

表 8-37. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	BQWRTFAULT_FLAG	R	0h	**0: The recent BQ is written successfully** 1: The recent BQ is written failed
5-3	RESERVED	R	0h	
2	CLKFAULT_FLAG	R	0h	Clock fault. Once there is a Clock fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clock fault works with an auto-recovery mode, once the clock error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	PVDDOV_FLAG	R	0h	PVDD OV fault. Once there is a OV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	PVDDUV_FLAG	R	0h	PVDD UV fault. Once there is a UV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). UV fault works with an auto-recovery mode, once the UV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

8.1.36 GLOBAL_FAULT2 Register (Offset = 72h) [Reset = 00h]

GLOBAL_FAULT2 is shown in 図 8-36 and described in 表 8-38.

Return to the Summary Table.

Global fautl 2

図 8-36. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED							OTSD_FLAG
R-0h							R-0h

表 8-38. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	OTSD_FLAG	R	0h	Over temperature shut down fault Once there is a OT fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an autorecovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

8.1.37 OT_WARNING Register (Offset = 73h) [Reset = 00h]

OT_WARNING is shown in 図 8-37 and described in 表 8-39.

Return to the Summary Table.

OT Warning

図 8-37. OT_WARNING Register

7	6	5	4	3	2	1	0
RESERVED					OTW_FLAG	RESERVED	
R-0h					R-0h	R-0h	

表 8-39. OT_WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	OTW_FLAG	R	0h	**0: No temperature warning** 1: Over temperature warning is triggered
1-0	RESERVED	R	0h	

8.1.38 PIN_CONTROL1 Register (Offset = 74h) [Reset = 00h]

PIN_CONTROL1 is shown in 図 8-38 and described in 表 8-40.

Return to the Summary Table.

Pin control 1

図 8-38. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDDUV	MASK_DVDDOV	MASK_CLKERROR	MASK_PVDDUV	MASK_PVDDOV	MASK_DC	MASK_OC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-40. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0h	**0: Enable OTSD fault report** 1: Mask OTSD fault report
6	MASK_DVDDUV	R/W	0h	**0: Enable DVDD UV fault report** 1: Mask DVDD UV report
5	MASK_DVDDOV	R/W	0h	**0: Enable DVDD OV fault report** 1: Mask DVDD OV fault report
4	MASK_CLKERROR	R/W	0h	**0: Enable CLK fault report** 1: Mask CLK fault report
3	MASK_PVDDUV	R/W	0h	**0: Enable UV fault report** 1: Mask UV fault report
2	MASK_PVDDOV	R/W	0h	**0: Enable OV fault report** 1: Mask OV fault report
1	MASK_DC	R/W	0h	**0: Enable DC fault report** 1: Mask DC fault report
0	MASK_OC	R/W	0h	**0: Enable OC fault report** 1: Mask OC fault report

8.1.39 PIN_CONTROL2 Register (Offset = 75h) [Reset = F8h]

PIN_CONTROL2 is shown in 図 8-39 and described in 表 8-41.

Return to the Summary Table.

Pin control 2

図 8-39. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
RESERVED		CLKFAULTLATCH_EN	OTSDLATCH_EN	OTWLATCH_EN	MASK_OTW	RESERVED	
R/W-3h		R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	

表 8-41. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	3h	
5	CLKFAULTLATCH_EN	R/W	1h	0: Disable CLK fault latch **1: Enable CLK fault latch**
4	OTSDLATCH_EN	R/W	1h	0: Disable OTSD fault latch **1: Enable OTSD fault latch**
3	OTWLATCH_EN	R/W	1h	0: Disable OTW warning latch **1: Enable OTW warning latch**
2	MASK_OTW	R/W	0h	**0: Enable OTW warning report** 1: Mask OTW warning report
1-0	RESERVED	R/W	0h	

8.1.40 MISC_CONTROL Register (Offset = 76h) [Reset = 00h]

MISC_CONTROL is shown in 図 8-40 and described in 表 8-42.

Return to the Summary Table.

Miscellaneous control

図 8-40. MISC_CONTROL Register

7	6	5	4	3	2	1	0
CLKDET_LATCH	RESERVED		OTSD_AUTOREC	RESERVED			
R/W-0h	R/W-0h		R/W-0h	R/W-0h			

表 8-42. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLKDET_LATCH	R/W	0h	1:Latch clock detection status **0:No latch clock detection status**
6-5	RESERVED	R/W	0h	
4	OTSD_AUTOREC	R/W	0h	**0: Disable OTSD auto recovery** 1: Enable OTSD auto recovery
3-0	RESERVED	R/W	0h	

8.1.41 FAULT_CLEAR Register (Offset = 78h) [Reset = 00h]

FAULT_CLEAR is shown in 図 8-41 and described in 表 8-43.

Return to the Summary Table.

Fault clear

図 8-41. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
FAULT_CLR	RESERVED						
W-0h	W-0h						

表 8-43. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT_CLR	W	0h	WRITE CLEAR BIT **0: No fault clear** 1: Clear analog fault
6-0	RESERVED	W	0h	

8.1.42 OLD_CONTROL Register (Offset = 79h) [Reset = 00h]

OLD_CONTROL is shown in 図 8-42 and described in 表 8-44.

Return to the Summary Table.

Open load detection control

図 8-42. OLD_CONTROL Register

7	6	5	4	3	2	1	0
DET_EN	PLUSE_EN	WAIT_TIME		DISCHG_TIME		CHG_TIME	
W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	

表 8-44. OLD_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DET_EN	W	0h	**0: Open load detection enable** 1: Open load detection disable
6	PLUSE_EN	R/W	0h	**0: OLD pulse injection disable** 1: OLD pulse injection enable
5-4	WAIT_TIME	R/W	0h	**00: 0.5 ms** 01: 1 ms 10: 2 ms 11: 4 ms
3-2	DISCHG_TIME	R/W	0h	**00: 3 ms** 01: 6 ms 10: 12 ms 11: 24 ms
1-0	CHG_TIME	R/W	0h	**00: 1 ms** 01: 2 ms 10: 4 ms 11: 8 ms

8.1.43 SLD_CONTROL1 Register (Offset = 7Ah) [Reset = 09h]

SLD_CONTROL1 is shown in 図 8-43 and described in 表 8-45.

Return to the Summary Table.

Short load detection control 1

図 8-43. SLD_CONTROL1 Register

7	6	5	4	3	2	1	0
DET_EN	STATUS_SET	WIN_SET			DUTY_SET		
W-0h	W-0h	W-1h			W-1h		

表 8-45. SLD_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DET_EN	W	0h	**0: Short load detection disable** 1: Short load detection enable
6	STATUS_SET	W	0h	**0: Exit to PLAY after OL detection** 1: Exit to Hi-Z, then return to PLAY once this bit manually cleared
5-3	WIN_SET	W	1h	b'000: 15 us **b'001: 20 us** b'010:30 us b'011:40 us b'100:50 us b'101:60 us b'110:70 us b'111:80 us
2-0	DUTY_SET	W	1h	b'000: 100% duty square wave **b'001: 20% duty square wave** b'010:40% duty square wave b'011:50% duty square wave b'100:60% duty square wave b'101:70% duty square wave b'110:80% duty square wave b'111:90% duty square wave

8.1.44 SLD_CONTROL2 Register (Offset = 7Bh) [Reset = 03h]

SLD_CONTROL2 is shown in 図 8-44 and described in 表 8-46.

Return to the Summary Table.

Short load detection control 2

図 8-44. SLD_CONTROL2 Register

7	6	5	4	3	2	1	0
DISCHG_TIME		STATUS_SET	RESERVED				
R/W-0h		R/W-0h	R/W-3h				

表 8-46. SLD_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DISCHG_TIME	R/W	0h	**00: 1 ms** 01: 2 ms 10: 4 ms 11: 8 ms
5	STATUS_SET	R/W	0h	**0: Exit to PLAY after SL detection** 1: Exit to Hi-Z, then return to PLAY once this bit manually cleared
4-0	RESERVED	R/W	3h	

8.1.45 LD_REPORT Register (Offset = 7Ch) [Reset = 00h]

LD_REPORT is shown in 図 8-45 and described in 表 8-47.

Return to the Summary Table.

Load detection report

図 8-45. LD_REPORT Register

7	6	5	4	3	2	1	0
RESERVED	SLD_STATUS2	SLD_STATUS1	SLDET_FLAG	RESERVED	OLD_STATUS2	OLD_STATUS1	OLDET_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-47. LD_REPORT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SLD_STATUS2	R	0h	**0: No short load on Channel 2** 1: Short load on Channel 2
5	SLD_STATUS1	R	0h	**0: No short load on Channel 1** 1: Short load on Channel 1
4	SLDET_FLAG	R	0h	**0: Short load detection is on going** 1: Short load detection done
3	RESERVED	R	0h	
2	OLD_STATUS2	R	0h	**0: No open load on Channel 2** 1: Open load on Channel 2
1	OLD_STATUS1	R	0h	**0: No open load on Channel 1** 1: Open load on Channel 1
0	OLDET_FLAG	R	0h	**0: Open load detection is on going** 1: Open load detection done

9 Application Information Disclaimer

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5815 device into the larger system.

9.1.1 Bootstrap Capacitors

The output stage of the TAS5815 uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22µF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.22µF capacitor between OUT_A and BST_A for bootstrapping the A channel. Similarly, connect another 0.22µF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

9.1.2 Inductor Selections

It is required that the peak current is smaller than the OCP (Over current protection) value which is 7A (Typical), there are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to θ.

$$I_{peak\_power\_up} \approx PVDD \times \sqrt{C/L} \times \sin(1/\sqrt{L \times C} \times \theta / F_{sw}) \quad (1)$$

注

θ=0.5 (BD Modulation), 0.14 (1SPW Modulation), 0.14 (Hybrid Modulation). This formula just provide a rough estimation, suggest to measure the start-up current based on your LC filter.

表 9-1. Peak Current During Power Up

PVDD	L (uH)	C (uF)	Fsw (kHz)	$I_{peak\_power\_up}$
24	4.7	0.68	384	6.07A
24	4.7	0.68	768	3.25A
24	10	0.68	384	3A
24	10	0.68	768	1.55A
12	4.7	0.68	384	3.32A
12	10	0.68	384	1.55A

2. During music playing, some audio burst signal (high frequency) with hard PVDD clipping causes PWM duty cycle increase dramatically. This is the worst case and it rarely happens.

$$I_{peak\_clipping} \approx PVDD \times (1-\theta)/(F_{sw} \times L) \quad (2)$$

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak\_output\_power} \approx \sqrt{2 \times Max\_Output\_Power / R_{speaker\_Load}} \quad (3)$$

Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. It's suggested that inductor saturation current I_{SAT}, is larger than the amplifier peak current during power-up and play audio.

$$I_{SAT} \geq \max(I_{peak\_power\_up}, I_{peak\_clipping}, I_{peak\_output\_power}) \quad (4)$$

In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in 表 9-2 to meet datasheet specifications.

表 9-2. LC filter recommendation

Switching Frequency (kHz)	Modulation Scheme	Recommended Minimum Inductance (uH) for LC filter design
1024	1SPW	3.3 µH (or larger) + Capacitor (0.22uF~0.68uF)
768		4.7 µH (or larger) + Capacitor (0.22uF~0.68uF)
384 or 480		10 µH (or larger) +Capacitor (0.22uF~0.68uF)
384~1024	BD	8.2uH (or Larger) +Capacitor (0.22uF~0.68uF)

For inductor selection refer to LCFILTER-CALC-TOOL.

9.1.3 Power Supply Decoupling

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22µF. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1µF or 0.1µF capacitors as close as possible to the PVDD pins of the device.

9.1.4 Output EMI Filtering

The TAS5815 device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the LC Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The LC filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the LC filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report Class-D LC Filter Design (SLOA119) for a detailed description on the proper component selection and design of an LC filter based upon the desired load and response.

9.2 Typical Application

9.2.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

図 9-1 and 図 9-2 shows the 2.0 (Stereo BTL) system application with a ferrite bead filter and L-C filter, respectively.

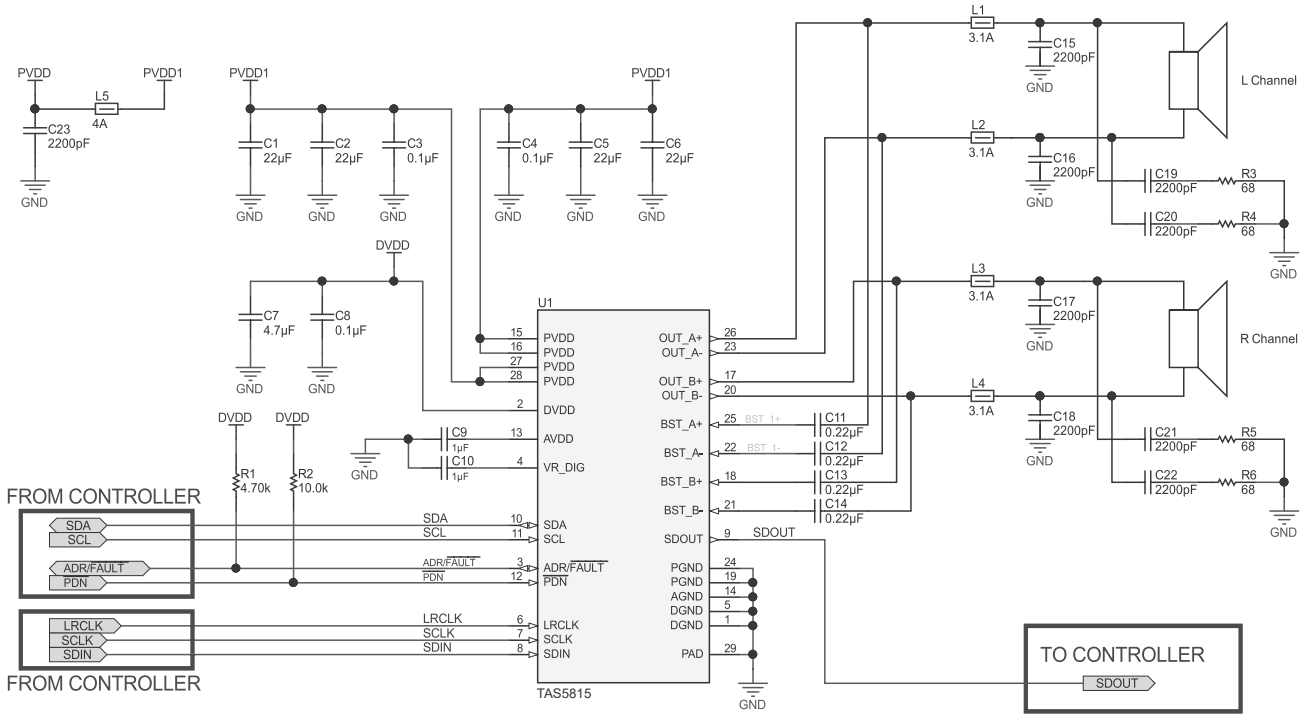

図 9-1. 2.0 (Stereo BTL) System Application Schematic with Ferrite Bead as the output filter

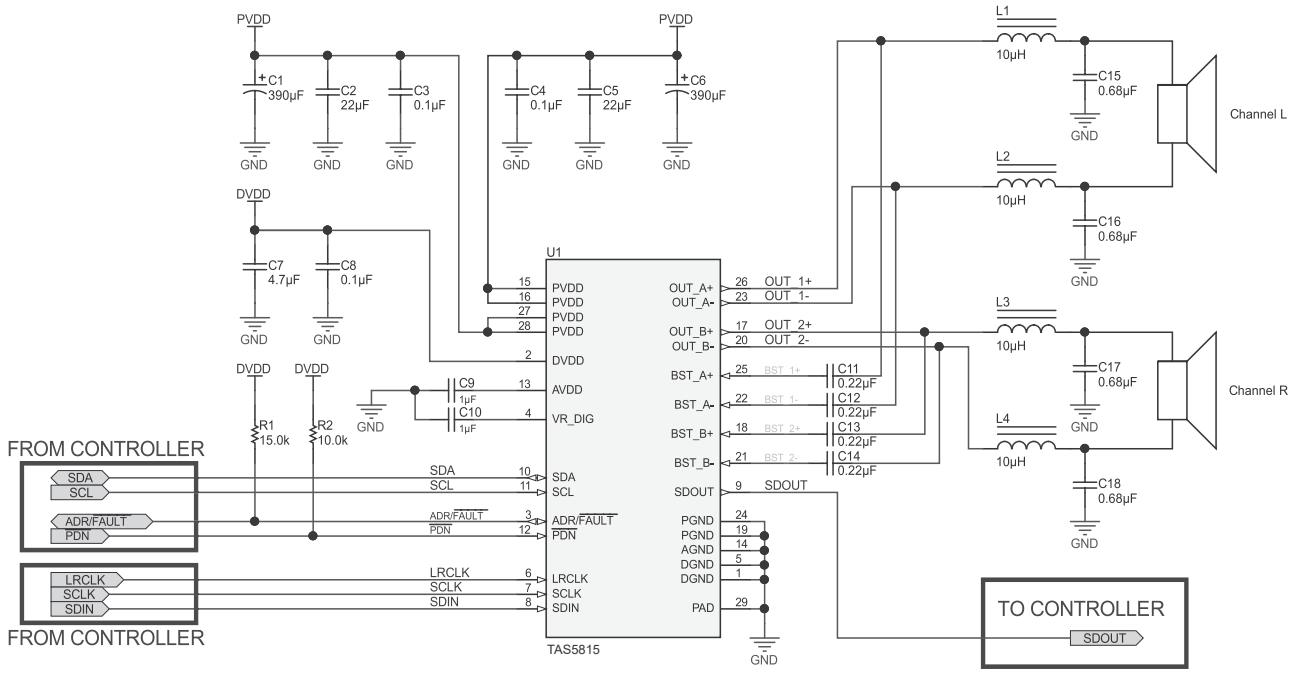

図 9-2. 2.0 (Stereo BTL) System Application Schematic with Inductor as the output filter

9.2.1.1 Design Requirements

- Power supplies:
  - 3.3V or 1.8V supply for DVDD.
  - 4.5V to 26.4V supply for PVDD.
- Communication: host processor serving as I2C compliant master.
- External memory (Such as EEPROM and FLASH) used for coefficients.

The requirements for the supporting components for the TAS5815 device in a Stereo 2.0 (BTL) system are provide in 表 9-3 \ and 表 9-4.

表 9-3. Supporting Component Requirements for Stereo 2.0 (BTL) system (With Ferrite bead as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1,C2,C5,C6	22uF	0805	CAP, CERM, 22µF, 35V, +/- 20%, JB, 0805
C3,C4	0.1uF	0402	CAP, CERM, 0.1µF, 50V, +/- 10%, X7R, 0402
C7	4.7uF	0603	CAP, CERM, 4.7µF, 10V, +/- 10%, X5R, 0603
C8	0.1uF	0603	CAP, CERM, 0.1µF, 16V, +/- 10%, X7R, 0603
C9,C10	1uF	0603	CAP, CERM, 1µF, 16V, +/- 10%, X5R, 0603
R1	4.70kΩ	0402	RES, 4.70kΩ, 1%, 0.0625W, 0402
R2	10.0kΩ	0404	RES, 10.0kΩ, 1%, 0.063W, 0402
C11,C12,C13,C14	0.22uF	0603	CAP, CERM, 0.22µF, 50V, +/- 10%, X7R, 0603
C15,C16,C17,C18,C19,C20,C21,C22,C23	2200pF	0603	CAP, CERM, 2200pF, 100V,+/- 10%, X7R, 0603
R3,R4,R5,R6	68ohm	0603	ES, 68Ω, 5%, 0.1W, 0603
L1,L2,L3,L4	300ohm	0806	Ferrite Bead, 300Ω @ 100MHz, 3.1A, 0806
L5	100 ohm	0806	Ferrite Bead, 100ohm @ 100MHz, 4A, 0806

With Low EMI technology, TAS5815 keeps enough EMI margin for most of application cases where PVDD < 14V with ferrite bead (Low BOM cost). With Ferrite Bead and capacitor as the output filter, 表 9-3 includes a good configuration (proper value of ferrite bead, capacitor, resistor) to achieve enough EMI margin for the typical case which PVDD = 12V, Speaker Load = 8Ω/6Ω, each speaker wire with 1m length, Output Power = 1W/4W/8W for each channel.

- Select Ferrite bead (L1~L5). The trade-off is impedance and rated current. If the rated current meet the system's requirement, larger impedance means larger EMI margin for the EMI, especially for the frequency band 5 MHz~50 MHz. The typical ferrite bead recommend for TAS5815 is NFZ2MSM series (Murata) and UPZ2012E series (Sunlord). 300 ohm at 100 MHz ferrite bead is a typical value which can pass EMI for most of application cases.
- Select capacitor (C15~C23). The trade-off is capacitor value and idle current. Larger capacitor means larger idle current, increase the capacitor value from 1nF to 2.2nF makes much help for frequency band 5 MHz~100 MHz.
- Using Ferrite bead as the output filter, recommend designer to use Fsw = 384 kHz with Spread spectrum enable, BD Modulation, refer to セクション 7.4.3.1.
- With Ferrite bead as the output power. In order to pass EMI (AC Conducted Emission) standard, an AC to DC adapter with EMI filter in it is needed. For most of applications (TV/Voice Control Speaker/Wireless speaker/ Soundbar) which need a 110V~220V power supply usually has a EMI filter in the AC to DC adapter. Some cases use DC power supply and also need to test the DC Conducted Emission , this applications (Automotive/Industry) need a simple EMI filter on PVDD for TAS5815. Refer to application note: AN-2162 Simple Success With Conducted EMI From DC to DC Converters.

表 9-4. Supporting Component Requirements for Stereo 2.0 (BTL) system (With Inductor as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1,C6	390µF	10mmx10mm	CAP, AL, 390µF, 35V, ±20%, 0.08 ohm, SMD
C2,C5	22µF	0603	CAP, CERM, 22µF, 35V, ±20%, JB, 0805
C3,C4	0.1µF	0402	CAP, CERM, 0.1µF, 50V, ±10%, X7R, 0402
C7	4.7µF	0603	CAP, CERM, 4.7µF, 10V, ±10%, X5R, 0603
C8	0.1µF	0603	CAP, CERM, 0.1µF, 16V, ±10%, X7R, 0603
C9,C10	1µF	0603	CAP, CERM, 1µF, 16V, ±10%, X5R, 0603
R1	15.0kΩ	0402	RES, 15.0kΩ, 1%, 0.0625 W, 0402
R2	10.0kΩ	0404	RES, 10.0kΩ, 1%, 0.063W, 0402
C11,C12,C13,C14	0.22µF	0603	CAP, CERM, 0.22µF, 50V, ±10%, X7R, 0603
C15,C16,C17,C18	0.68µF	0805	CAP, CERM, 0.68µF, 50V, ±10%, X7R, 0805
L1,L2,L3,L4	10µH		Inductor, Shielded, 10µH, 4.4A, 0.023Ω, SMD

With an inductor as the output filter, designers can achieve ultra low idle current (with Hybrid Modulation or 1SPW Modulation) and keep large EMI margin. As the switching frequency of TAS5815 can be adjustable from 384 kHz to 768 kHz. Higher switching frequency means smaller Inductor value needed.

- With 768kHz switching frequency. Designers can select 10uH + 0.68µF or 4.7µH +0.68µF as the output filter, this will help customer to save the Inductor size with the same rated current during the inductor selection. With 4.7uH + 0.68uF, make sure PVDD ≤ 12V to avoid the large ripple current to trigger the OC threshold (5A).
- With 384kHZ switching frequency. Designers can select 22µH + 0.68µF or 15µH + 0.68µF or 10µH + 0.68µF as the output filter, this will help customer to save power dissipation for some battery power supply application. With 10µH + 0.68µF, make sure PVDD ≤ 12V to avoid the large ripple current to trigger the OC threshold (5A).

9.2.2 Detailed Design Procedure

The design procedure can be used for Stereo 2.0, Mono, 2.1 systems.

9.2.2.1 Step 1: Hardware Integration

- Use the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Follow the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
  - For questions and support, go to the E2E forums (E2E.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

9.2.2.2 Step 2: Speaker Tuning

Use the TAS5815EVM board and PPC3 tuning software to configure the desired device settings

9.2.2.3 Step 3: Software Integration

- Use the End System Integration feature of the PPC3 tuning software app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

9.2.3 MONO (PBTL) System

In MONO mode, TAS5815 can be used as PBTL mode to drive sub-woofer with more output power.

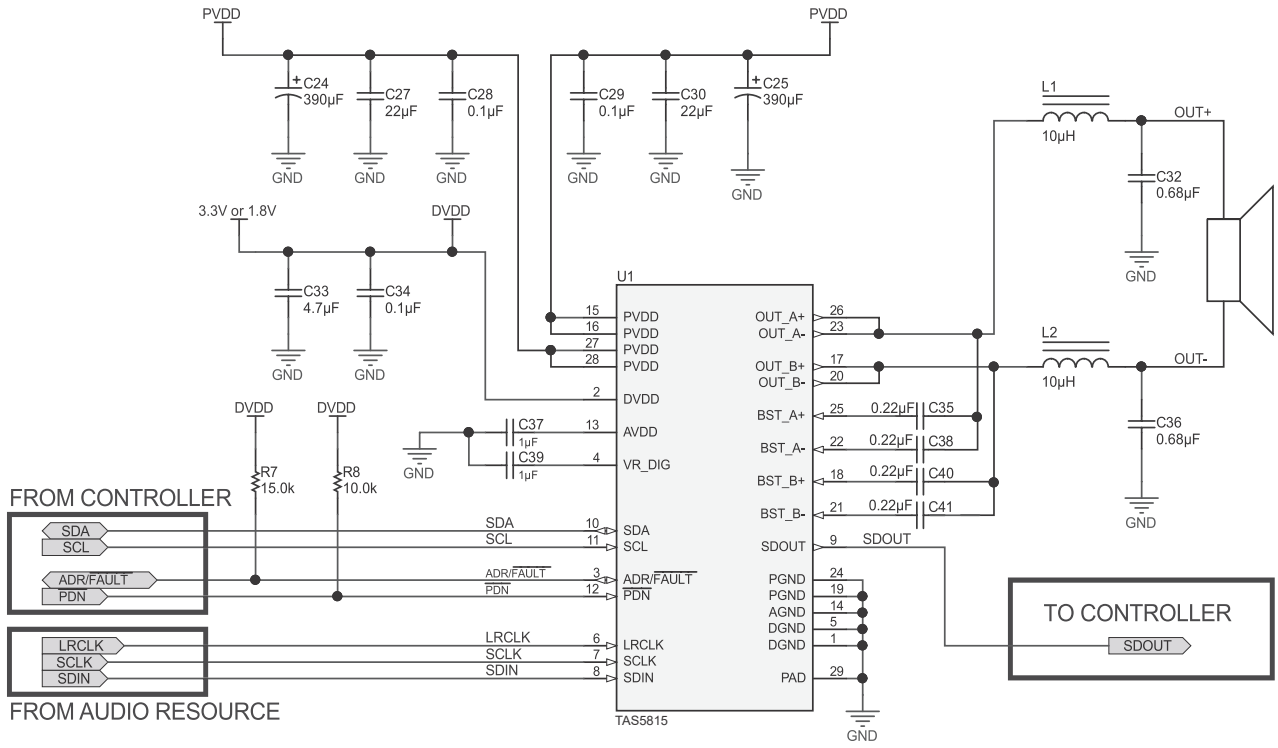

図 9-3. Mono (PBTL) System Application Schematic

9.2.3.1 Design Requirements

- Power supplies:
  - 3.3V or 1.8V supply
  - 4.5V to 26.4V supply
- Communication: host processor serving as I^2C compliant master
- External memory (Such as EEPROM and FLASH) used for coefficients

The requirement for the supporting components for the TAS5815 device in a MONO (PBTL) system is provide in 表 9-5.

表 9-5. Supporting Component Requirements for MONO (PBTL) system (With Inductor as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C24,C25	390uF	10mmx10mm	CAP, AL, 390µF, 35V, +/- 20%, 0.08 ohm, SMD
C27,C30	22uF	0603	CAP, CERM, 22µF, 35V, +/- 20%, JB, 0805
C28,C29	0.1uF	0402	CAP, CERM, 0.1µF, 50V, +/- 10%, X7R, 0402
C33	4.7uF	0603	CAP, CERM, 4.7µF, 10V, +/- 10%, X5R, 0603
C34	0.1uF	0603	CAP, CERM, 0.1µF, 16V, +/- 10%, X7R, 0603
C37,C39	1uF	0603	CAP, CERM, 1µF, 16V, +/- 10%, X5R, 0603
R7	4.70kΩ	0402	RES, 4.70kΩ, 1%, 0.0625W, 0402
R8	10.0kΩ	0404	RES, 10.0kΩ, 1%, 0.063W, 0402
C35,C38,C40,C41	0.22uF	0603	CAP, CERM, 0.22µF, 50V, +/- 10%, X7R, 0603
C32,C36	0.68uF	0805	CAP, CERM, 0.68µF, 50V, +/- 10%, X7R, 0805
L1,L2	10uH		Inductor, Shielded, 10µH, 7A, 0.023Ω, SMD

For information about the Detailed Design Procedure, see the セクション 9.2.2.

9.2.4 Advanced 2.1 System (Two TAS5815 Devices)

In higher performance systems, the subwoofer output can be enhanced using digital audio processing as was done in the high-frequency channels. To accomplish this, two TAS5815 devices are used - one for the high frequency left and right speakers and one for the mono subwoofer speaker. In this system, the audio signal can be sent from the TAS5815 device through the SDOUT pin. Alternatively, the subwoofer amplifier can accept the same digital input as the stereo, which might come from a central systems processor. 図 9-4 shows the 2.1 (Stereo BTL with Two TAS5815 devices) system application.

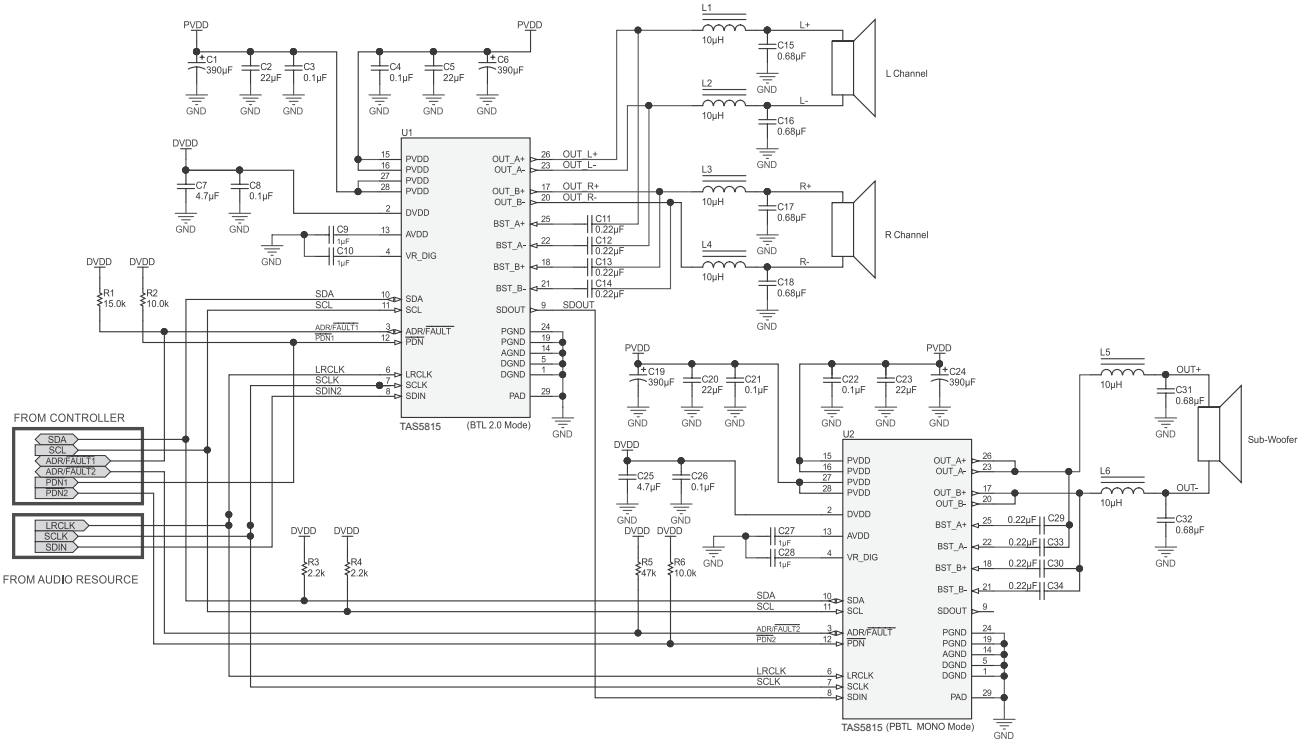

図 9-4. 2.1 (2.1 CH with Two TAS5815 Devices) Application Schematic

10 Power Supply Recommendations

The TAS5815 device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. One low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD, DVDD supply are listed in the Recommended Operating Conditions table. The two power supplies do not have a required power-up sequence. The power supplies can be powered on in any order, but once the device has been initialized, PVDD must keep within the normal operation voltage. If PVDD lower than 3.5 V, then all registers need re-initialize again. Recommends waiting 1 ms to 5 ms for the DVDD power supplies to stabilize before starting I^2C communication and providing stable I^2S clock before enabling the device outputs.

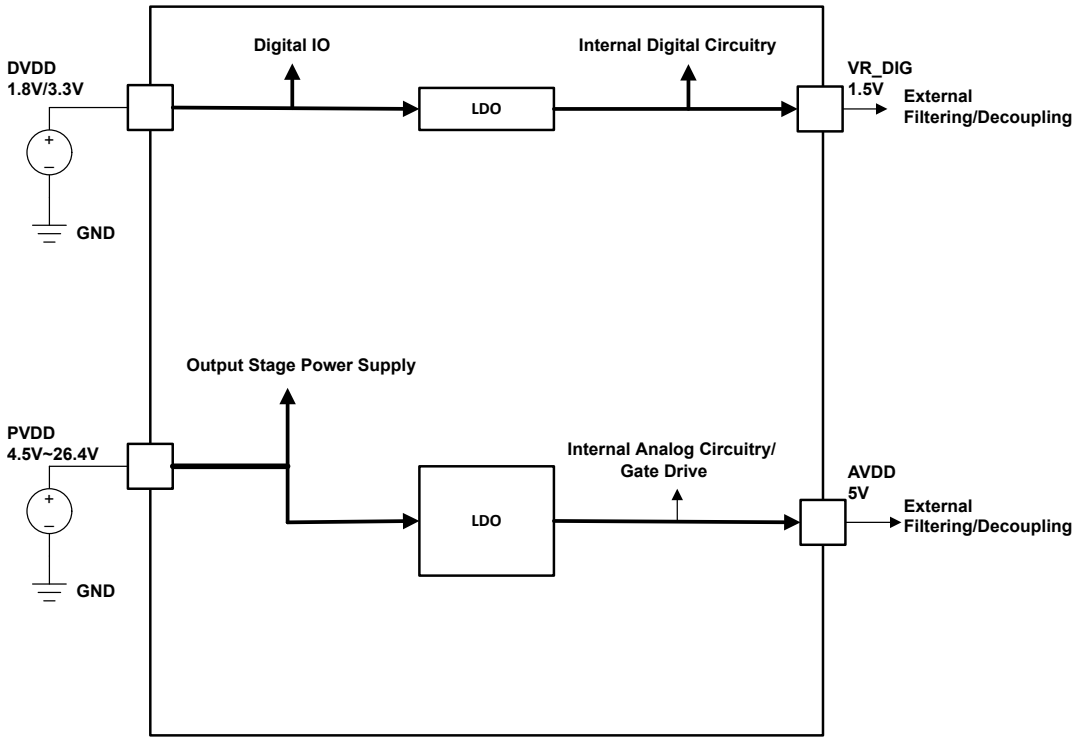

図 10-1. Power Supply Function Block Diagram

10.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in 図 10-1, it provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the Application Information section and the Layout section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5815 device includes an integrated low

dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the DVDD pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuit. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

10.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5815EVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5815 device Application Information. Lack of proper decoupling results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5815 internal circuitry. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

11 Layout

11.1 Layout Guidelines

11.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in the Layout Example. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the Layout Example and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

11.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, GVDD and PVDD. However, the capacitors on the PVDD net for the TAS5815 device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only dose placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5815 device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the deice. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the Layout Example.

11.1.3 Optimizing Thermal Performance

Follow the layout example shown in the to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

11.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5815 device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5815 device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5815 device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.

- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5815 device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

11.1.3.2 Stencil Pattern

The recommended drawings for the TAS5815 device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

注

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

11.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5815 device is soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5815 device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5815 device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the section, this interface can benefit from improved thermal performance.

注

Vias can obstruct heat flow if they are not constructed properly.

More notes on the construction and placement of vias are as follows:

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drill must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the Layout Example.
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5815 device to open up the current path to and from the device.

11.1.3.2.2 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to out gas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the Layout Example. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

11.2 Layout Example

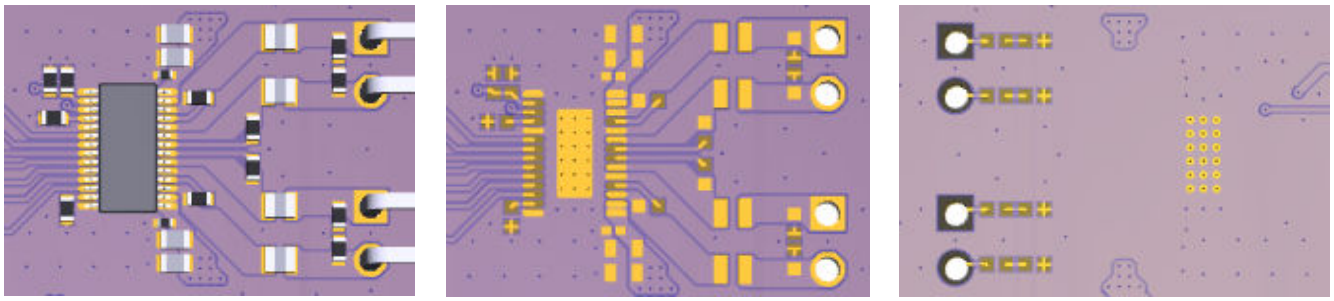

図 11-1. 2.0 (Stereo BTL with Ferrite Bead as Output Filter) Layout View

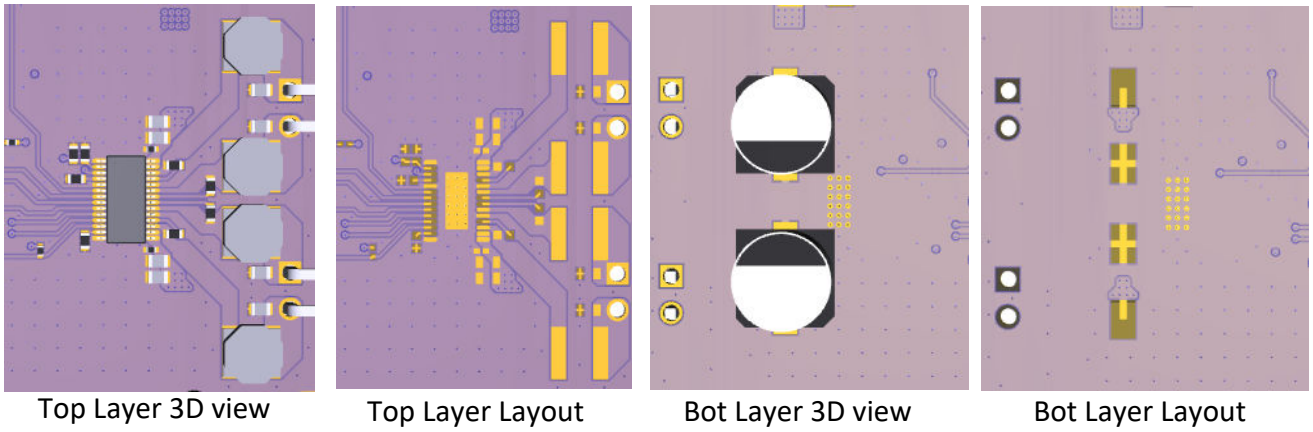

図 11-2. 2.0 (Stereo BTL with Inductor as Output Filter) Layout View

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

The glossary listed in this section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplfier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. It is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to device which serves as a central system controller, providing control information to devices connected to it as well as gathering audio source data from devices upstream from it and distributing it to other devices. This device often configures the controls of the audio processing devices (like the TAS5815) in the audio path in order to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that their temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$r_{DS(on)}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

12.2 サポート・リソース

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12.3 Trademarks

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

14 Mechanical and Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
TAS5815PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	5815
TAS5815PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	5815

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5815PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR		5815	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

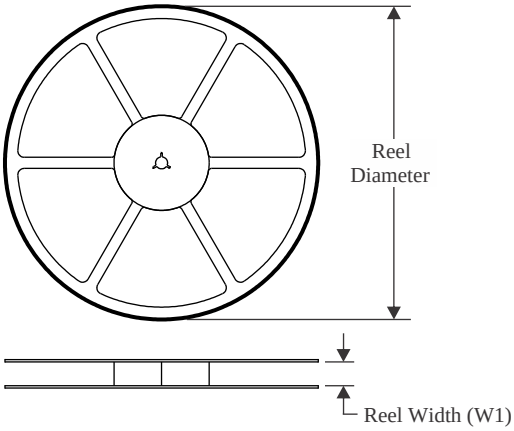
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

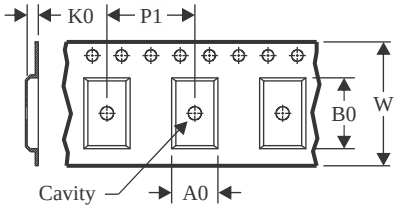
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

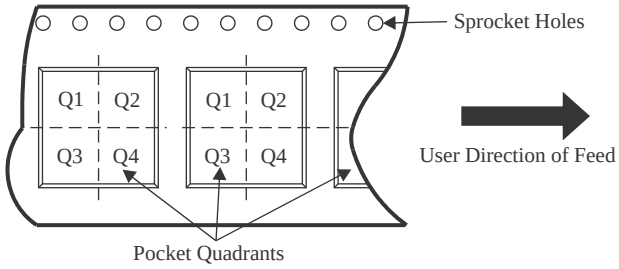


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

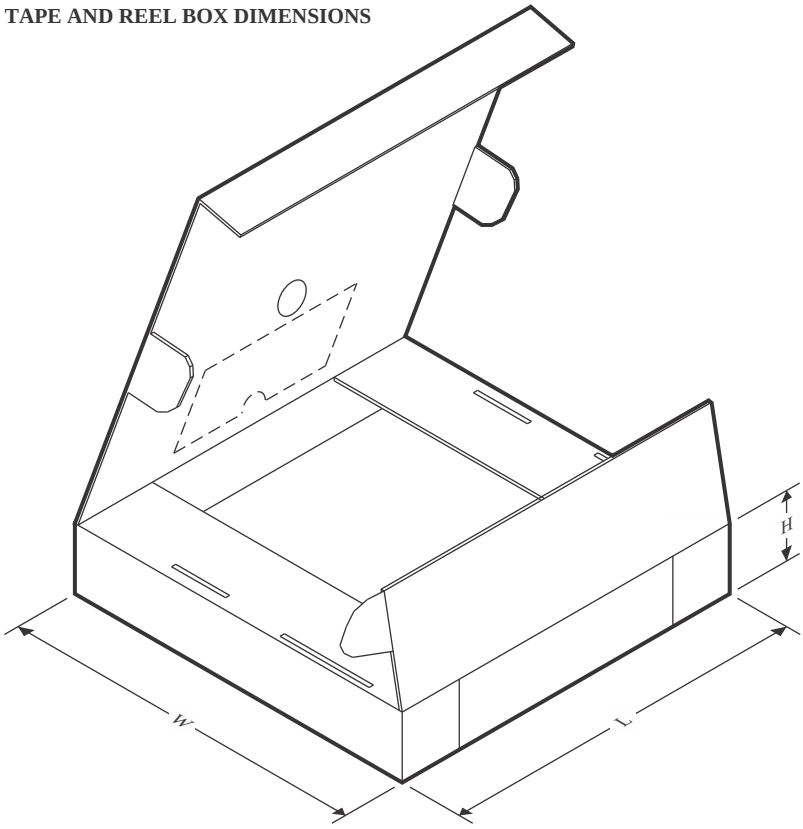
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5815PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5815PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

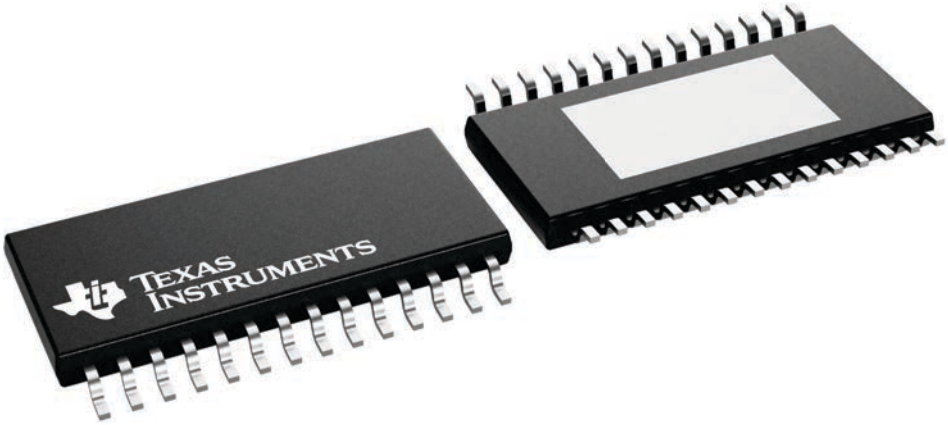
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

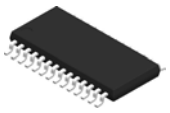
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

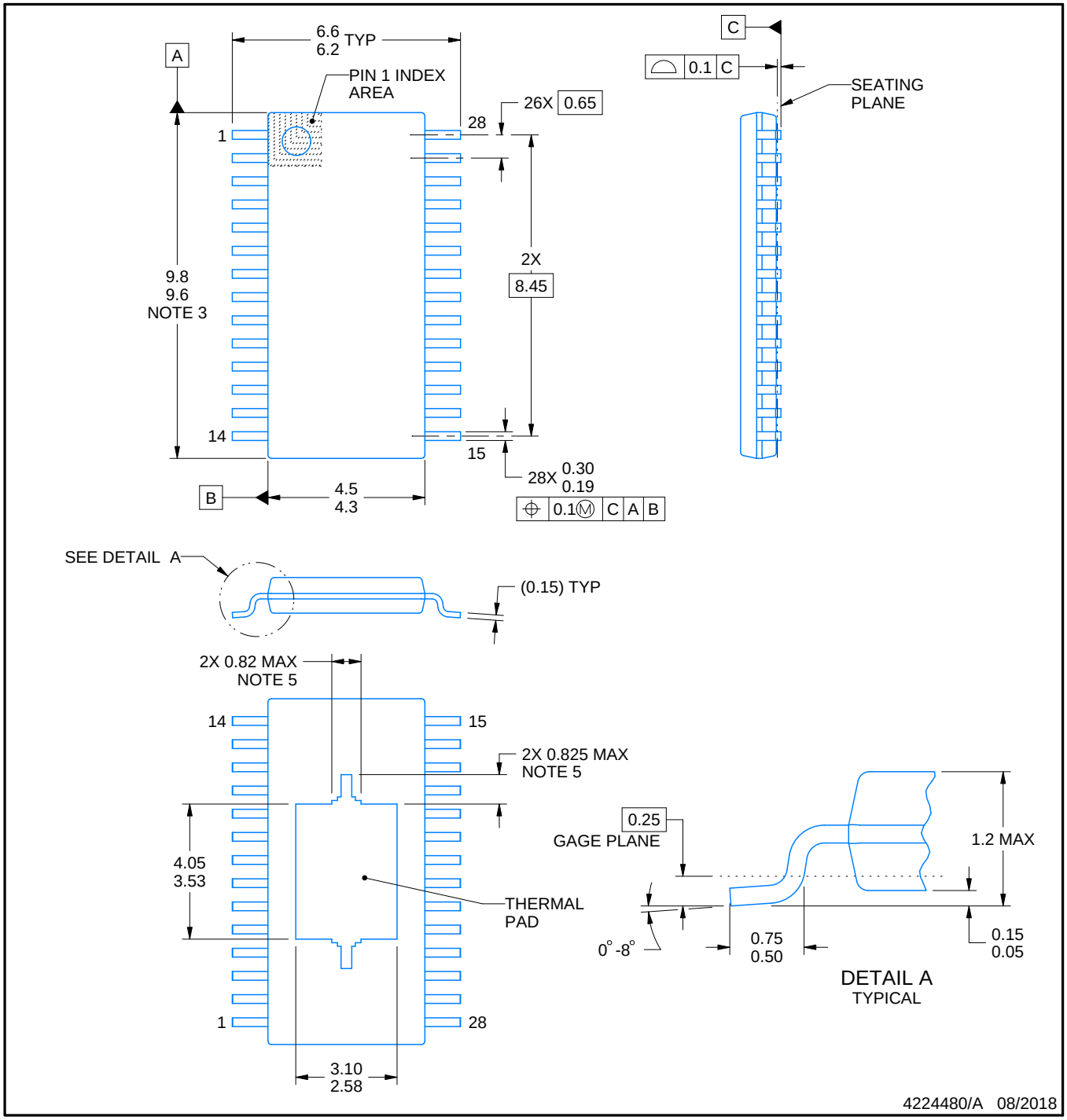
PACKAGE OUTLINE

PWP0028M



PowerPAD™ TSSOP - 1.2 mm max height

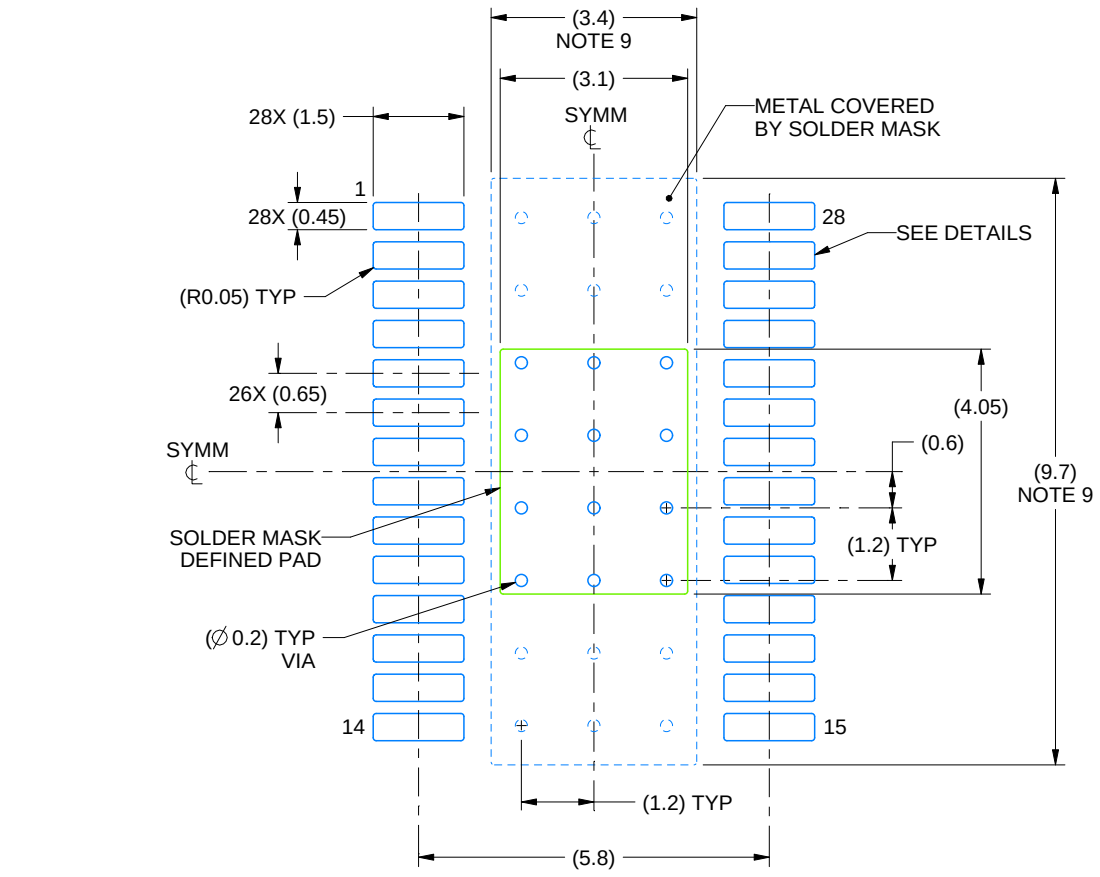
SMALL OUTLINE PACKAGE



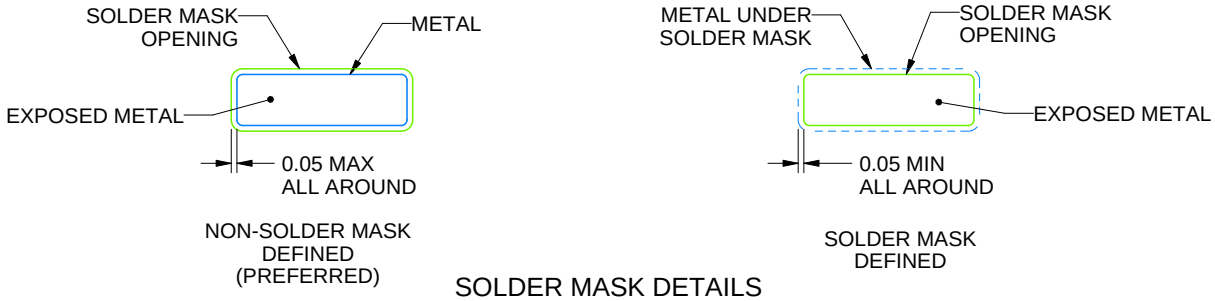
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

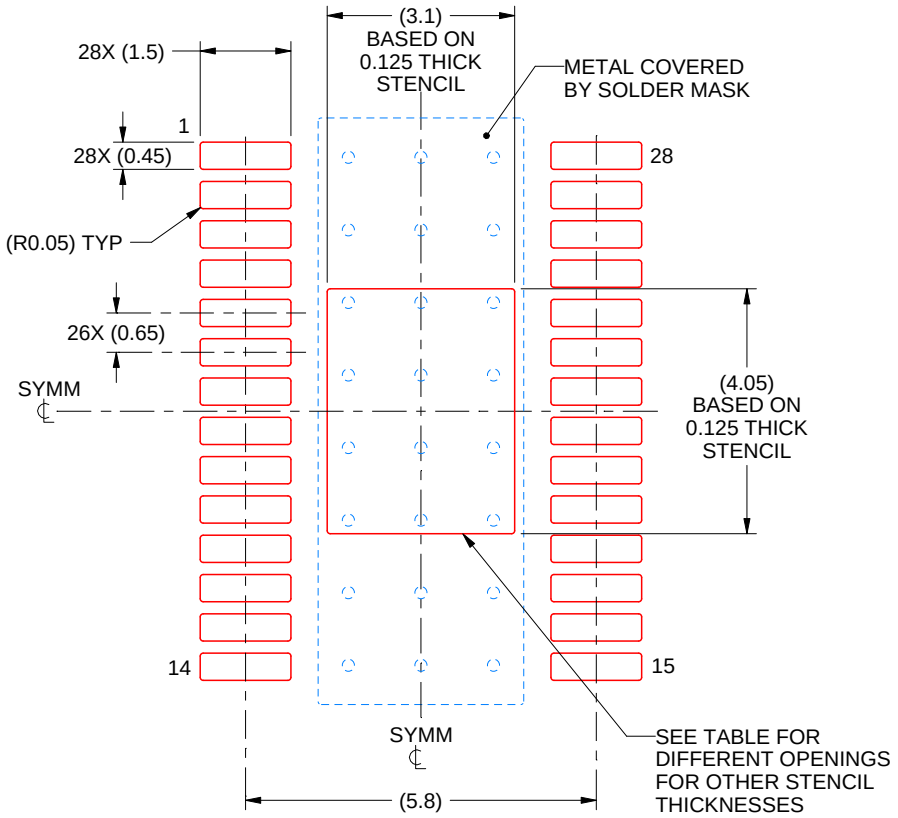


SOLDER MASK DETAILS

4224480/A 08/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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