

TCA9803 レベル変換I²Cバス・バッファリピータ

1 特長

- 2チャンネルの双方向バッファ
- B側に電流ソースを内蔵し、外付けのB側抵抗が不要
- 超低消費電力
- 静的電圧オフセットなし、低V_{OL}
- I²Cバスおよび SMBus 互換
- A側の動作電源電圧範囲：0.8V～3.6V
- B側の動作電源電圧範囲：1.65V～3.6V
- アクティブ HIGH のリピータ・イネーブル入力
- 電源オフ時、A側のI²Cバスのピンは高インピーダンス
- 電源オフ時、I²Cバスのピンのバック・パワー保護
- クロック・ストレッチングおよびマルチマスタ調停のサポート
- 電流ソースの0.5mAから3mAまでのオプションをファミリーとして用意

2 アプリケーション

- サーバー
- ルーター (ルーティング機器)
- 産業用機器
- パーソナル・コンピュータ
- 電力検出アプリケーション

3 概要

TCA9803は、デュアル・チャンネルの双方向バッファで、I²CバスおよびSMBus/PMBusのシステム用に設計されています。低電圧(最低0.8V)と高電圧(1.65V～3.6V)との間で、双方向のレベル・シフト(上方変換および下方変換)を行います。TCA9803はデバイスのB側に内部電流ソースがあるため、B側の外付けプルアップ抵抗を取り除くことができます。この電流ソースにより、立ち上がり時間の短縮と、非常に低い消費電力も実現されています。

TCA9803は、静的な電圧オフセットや増分的オフセットを使用せずに、真のバッファリング(パスFETソリューションではなく)を提供できます。すなわち、TCA9803のAおよびB側の両方でV_{OL}が非常に低く(約0.2V)、固定V_{IL}スレッショルドの結果として通信の問題が発生することを防止するため役立ちます。TCA9803の他の主要な特長は、電源シーケンスの要件や、電源の依存性が存在しないことです。V_{CCA}はV_{CCB}よりも大きくても、小さくても、同じでもかまいません。このためシステム設計者は、TCA9803を柔軟に使用できます。

TCA9803は、それぞれ電流ソース強度の異なる4つのデバイスからなるファミリーの1つです(デバイス比較表を参照)。

製品情報⁽¹⁾

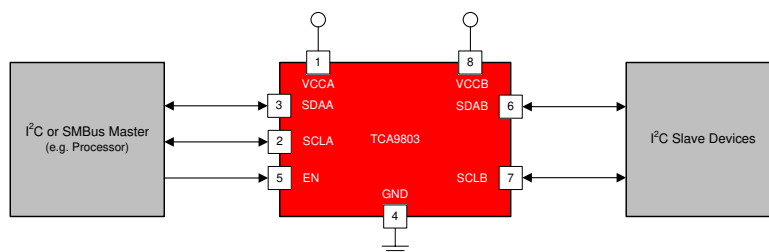
| 型番 | パッケージ | 本体サイズ(公称) |
|---------|-----------|---------------|
| TCA9803 | VSSOP (8) | 3.00mm×3.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

デバイスの比較

| 型番 | I _{CS} : 電流ソースの値(標準値) |
|---------|--------------------------------|
| TCA9800 | 0.54mA |
| TCA9801 | 1.1mA |
| TCA9802 | 2.2mA |
| TCA9803 | 3.3mA |

概略回路図



Copyright © 2017, Texas Instruments Incorporated



目次

| | | | | | |
|----------|--|-----------|-----------|---|-----------|
| 1 | 特長 | 1 | 9.2 | Functional Block Diagram | 11 |
| 2 | アプリケーション | 1 | 9.3 | Feature Description | 12 |
| 3 | 概要 | 1 | 9.4 | Device Functional Modes | 13 |
| 4 | 改訂履歴 | 2 | 10 | Application and Implementation | 16 |
| 5 | Device Comparison Table | 3 | 10.1 | Application Information | 16 |
| 6 | Pin Configuration and Functions | 3 | 10.2 | Typical Application | 18 |
| 7 | Specifications | 4 | 11 | Power Supply Recommendations | 29 |
| 7.1 | Absolute Maximum Ratings | 4 | 12 | Layout | 30 |
| 7.2 | ESD Ratings | 4 | 12.1 | Layout Guidelines | 30 |
| 7.3 | Recommended Operating Conditions | 4 | 12.2 | Layout Example | 30 |
| 7.4 | Thermal Information | 4 | 13 | デバイスおよびドキュメントのサポート | 31 |
| 7.5 | Electrical Characteristics | 5 | 13.1 | ドキュメントのサポート | 31 |
| 7.6 | Timing Requirements | 6 | 13.2 | ドキュメントの更新通知を受け取る方法 | 31 |
| 7.7 | Switching Characteristics | 6 | 13.3 | サポート・リソース | 31 |
| 7.8 | Typical Characteristics | 7 | 13.4 | 商標 | 31 |
| 8 | Parameter Measurement Information | 9 | 13.5 | 静電気放電に関する注意事項 | 31 |
| 9 | Detailed Description | 10 | 13.6 | Glossary | 31 |
| 9.1 | Overview | 10 | 14 | メカニカル、パッケージ、および注文情報 | 31 |

4 改訂履歴

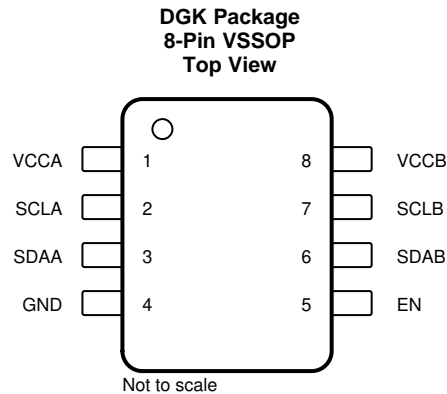
| Revision A (March 2017) から Revision B に変更 | Page |
|--|------|
| • Added last sentence: "When enable is a logic LOW while VCCB is powered on, the internal current source on B side is still enabled...." to the <i>Active-High Repeater Enable Input</i> section | 12 |

| 2017年3月発行のものから更新 | Page |
|--|------|
| • Updated I _{CS} typical values in <i>Device Comparison Table</i> | 3 |

5 Device Comparison Table

| Part Number | I _{CS} : Current Source Value (Typical) |
|-------------|--|
| TCA9800 | 0.54 mA |
| TCA9801 | 1.1 mA |
| TCA9802 | 2.2 mA |
| TCA9803 | 3.3 mA |

6 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----|------|--------|---|
| NO. | NAME | | |
| 1 | VCCA | Supply | A-side supply voltage (0.8 V to 3.6 V) |
| 2 | SCLA | I/O | Serial clock bus, A-side. Connect to V _{CCA} through a pull-up resistor, even if unused |
| 3 | SDAA | I/O | Serial data bus, A-side. Connect to V _{CCA} through a pull-up resistor, even if unused |
| 4 | GND | — | Ground |
| 5 | EN | I | Active-high repeater enable input, referenced to V _{CCA} |
| 6 | SDAB | I/O | Serial data bus, B-side. Do NOT connect to V _{CCB} through a pull-up resistor for proper operation. If unused, leave floating |
| 7 | SCLB | I/O | Serial clock bus, B-side. Do NOT connect to V _{CCB} through a pull-up resistor for proper operation. If unused, leave floating |
| 8 | VCCB | Supply | B-side and device supply voltage (1.65 V to 3.6 V) |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------------------------|---|------|-----|------|
| V _{CCA} | Supply voltage on A-side | -0.5 | 4 | V |
| V _{CCB} | Supply voltage on B-side | -0.5 | 4 | V |
| V _{EN} | Enable input voltage | -0.5 | 4 | V |
| V _{I/O} | I ² C bus voltage | -0.5 | 4 | V |
| I _{OL} | Maximum SDAA, SCLA I _{OL} current | | 20 | mA |
| I _{IK} | Input clamp current (SDAB/SCLB) | | -20 | mA |
| | Input clamp current (EN, VCCA, VCCB, SDAA, SCLA) | | -20 | mA |
| I _{OK} | Output clamp current (SDAB/SCLB) | | -20 | mA |
| | Output clamp current (EN, VCCA, VCCB, SDAA, SCLA) | | -20 | mA |
| Operating junction temperature | T _J | | 130 | °C |
| Storage temperature | T _{stg} | -60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|--------------------------------|------------|-----|------|
| T _A | Operating free-air temperature | -40 | 125 | °C |
| V _{CCA} | Supply voltage | 0.8 | 3.6 | V |
| V _{CCB} | Supply voltage | 1.65 | 3.6 | V |
| V _{I/O} | Input-output voltage | SDAA, SCLA | 0 | 3.6 |
| | | SDAB, SCLB | 0 | 3.6 |
| | | EN | 0 | 3.6 |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TCA9803 | UNIT |
|-------------------------------|--|-------------|------|
| | | DGK (VSSOP) | |
| | | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 174.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 85 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 104.4 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 18.3 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 102.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | | |
|-----------------------------------|---|---|---|--------------------|------------------------|------|-----|---|
| OUTPUT CHARACTERISTICS | | | | | | | | |
| V _{OL} | Low-level output voltage | SDAA, SCLA | I _{OL} = 6 mA, V _{ILB} = 0 V | | 0.04 | 0.13 | V | |
| | | SDAB, SCLB | V _{IA} = 0 V | | 0.22 | 0.26 | | |
| I _{EXT-I} ⁽²⁾ | Allowed input leakage current of I _{CS} | SDAB, SCLB | 0 | | 100 | μA | | |
| I _{EXT-O} ⁽²⁾ | Allowed output leakage current of I _{CS} | SDAB, SCLB | 0 | | 200 | μA | | |
| I _{CS} | Current source value | | | 3.3 | | mA | | |
| | Current source tolerance | | -25 | | 25 | % | | |
| INPUT CHARACTERISTICS | | | | | | | | |
| R _{EN} | Enable pin pull-up | | 150 | 250 | 450 | kΩ | | |
| V _{IH} | High-level input voltage | SDAA, SCLA | 0.7 × V _{CCA} | | V _{CCA} | V | | |
| | | SDAB, SCLB ⁽³⁾ | 0.7 × V _{CCB} | | V _{CCB} | | | |
| | | EN | 0.7 × V _{CCA} | | V _{CCA} | | | |
| V _{IL} | Low-level input voltage | SDAA, SCLA | 0 | | 0.3 × V _{CCA} | V | | |
| | | SDAB, SCLB ^{(4) (3)} | 0 | | 0.3 × V _{CCB} | | | |
| | | EN | 0 | | 0.3 × V _{CCA} | | | |
| I _{IILC} | Low-level input current contention | SDAB, SCLB ⁽⁴⁾ | 1000 | | | μA | | |
| R _{IILC} | Low-level allowed pull-down resistance | SDAB, SCLB ⁽³⁾ | | | 150 | Ω | | |
| C _{BUS} | Bus capacitance limit | SDAB, SCLB ⁽⁵⁾ | 0 | | 400 | pF | | |
| DC CHARACTERISTICS | | | | | | | | |
| UVLO | Under-voltage lock out | V _{CCA} | V _{CCA} rising and falling; V _{CCB} = 1.65 or 3.6 V | | 0.3 | 0.55 | 0.8 | V |
| | | V _{CCB} | V _{CCB} rising; V _{CCA} = 0.8 or 3.6 V | | 1.3 | 1.51 | 1.6 | |
| | | | V _{CCB} falling; V _{CCA} = 0.8 or 3.6 V | | 1.2 | 1.4 | 1.6 | |
| I _{CCA} | Quiescent supply current for V _{CCA} | SDAA = SCLA = V _{CCA} or GND, SDAB = SCLB = open, EN = V _{CCA} | V _{CCA} = 0.8 V | | 0.1 | 7 | μA | |
| | | | V _{CCA} = 1.8 V | | 0.1 | 8 | | |
| | | | V _{CCA} = 2.5 V | | 0.2 | 9 | | |
| | | | V _{CCA} = 3.6 V | | 0.2 | 12 | | |
| I _{CCB} | Quiescent supply current for V _{CCB} | Both channels high, SDAA = SCLA = pulled up to V _{CCA} , SDAB = SCLB = open, EN = V _{CCA} | V _{CCB} = 1.8 V | | 44 | 75 | μA | |
| | | | V _{CCB} = 2.5 V | | 47 | 80 | | |
| | | | V _{CCB} = 3.6 V | | 52 | 90 | mA | |
| | | | V _{CCB} = 1.8 V | | 6.4 | 7.7 | | |
| | | | V _{CCB} = 2.5 V | | 6.5 | 7.8 | | |
| V _{CCB} = 3.6 V | | 6.7 | 7.9 | | | | | |

(1) All typical values are at nominal supply voltage (1.8 V) and T_A = 25 °C unless otherwise specified.

(2) SDAB, SCLB may not sink current from external sources. It is required that no source of external current be used on these pins for proper device operation due to the internal current source.

(3) Parameter specified by design. Not tested in production.

(4) V_{IL} specification is for the first low-level seen by the SDAB and SCLB pins. I_{IILC} must also be satisfied in order to be interpreted as a low.

(5) SDAB, SCLB have a maximum supported capacitive load for device operation. If this load capacitance maximum is violated, the device does not function properly. SDAA, SCLA have no maximum capacitance limit.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---------------------|--------------------------------|--|--|--------------------|----------|---------------|
| $I_{CCA} + I_{CCB}$ | Total quiescent supply current | $V_{CCA} = V_{CCB} = 1.8\text{ V}$, SDAA/SCLA = V_{CCA} , SDAB/SCLB = V_{CCB} | | 45 | | μA |
| I_I | Input leakage current | SDAA, SCLA | $V_I = V_{CCA}$, EN = GND | | ± 10 | μA |
| | | | $V_I = \text{GND}$, EN = GND | | ± 10 | |
| | | SDAB, SCLB | $V_{CCB} = 0\text{ V}$, $V_I = 3.6\text{ V}$ | | ± 10 | |
| C_{IO} | I/O Capacitance | SDAA, SCLA | $V_I = 0\text{ V}$ or 3.3 V , $f = 1\text{ MHz}$ | 2 | 10 | pF |
| | | SDAB, SCLB | $V_{CCB} = \text{GND}$, $V_I = 0\text{ V}$, $f = 1\text{ MHz}$ | 8 | | |

7.6 Timing Requirements

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-----------------------|-------------------------------|-----------------------------------|-----|-----|------|
| $f_{SCL(\text{MAX})}$ | Max SCL clock frequency | 400 | | | kHz |
| $t_r^{(1)}$ | Rise time | Port A | 57 | 70 | ns |
| | | Port B; $V_{CCB} = 1.65\text{ V}$ | 11 | 25 | |
| | | Port B; $V_{CCB} = 2.5\text{ V}$ | 16 | 40 | |
| | | Port B; $V_{CCB} = 3.6\text{ V}$ | 24 | 65 | |
| $t_f^{(1)}$ | Fall time | Port A | 9 | 30 | ns |
| | | Port B | 35 | 75 | |
| $t_{PHL}^{(1)}$ | Propagation delay high-to-low | Port A to Port B | 75 | 200 | ns |
| | | Port B to Port A | 85 | 250 | |
| $t_{PLH}^{(1)}$ | Propagation delay low-to-high | Port A to Port B | 15 | 90 | ns |
| | | Port B to Port A | 120 | 260 | |

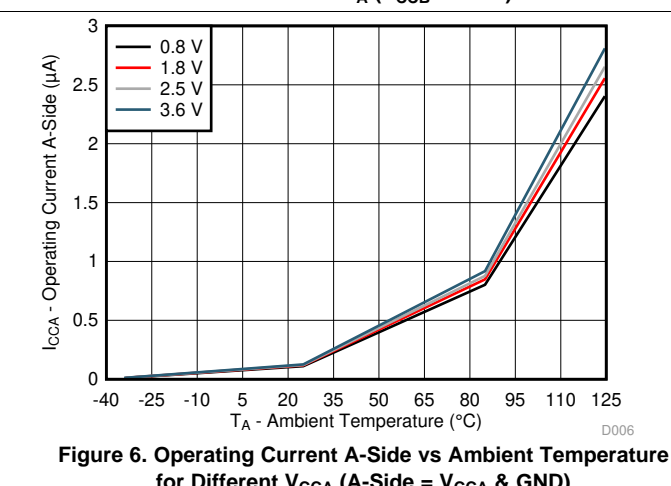
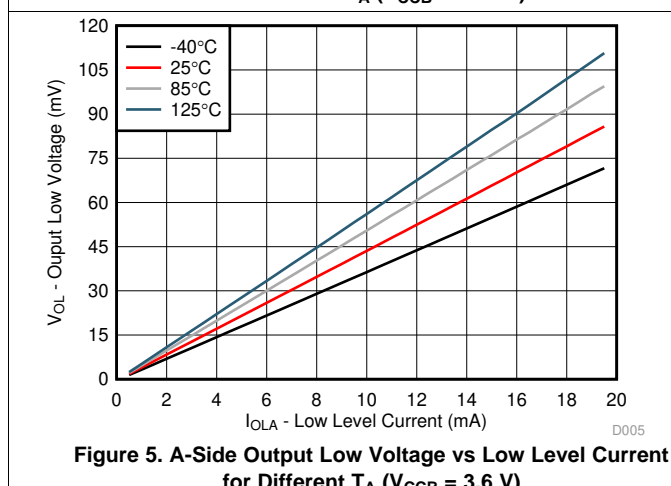
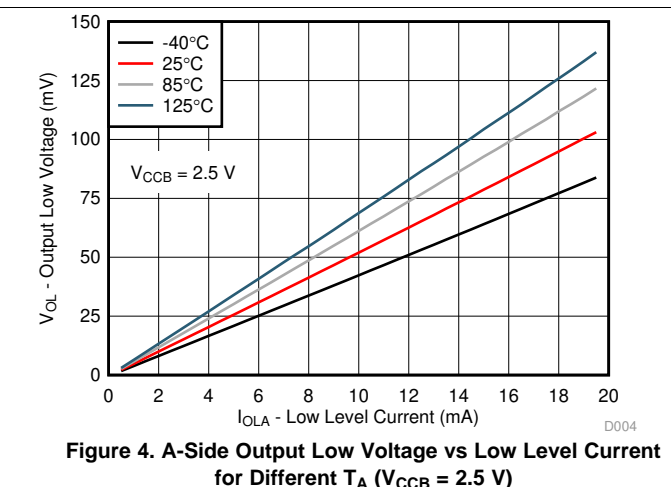
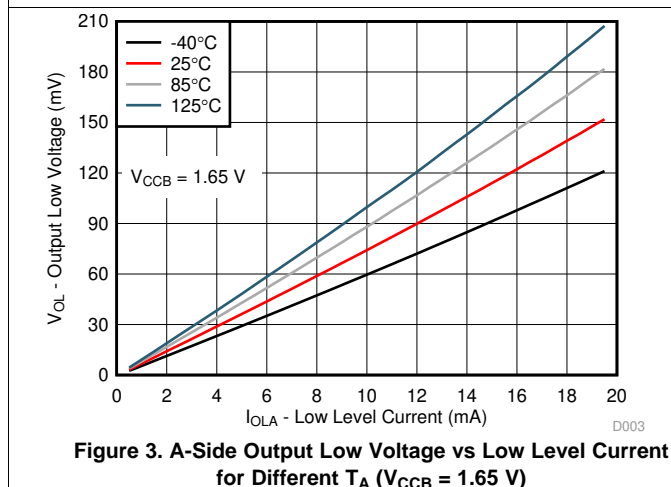
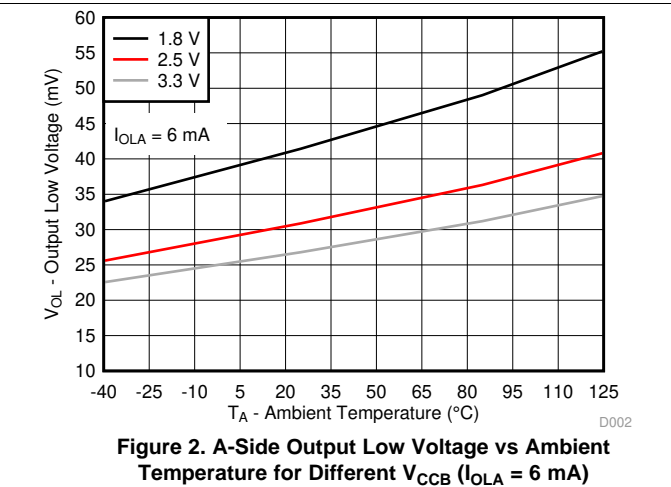
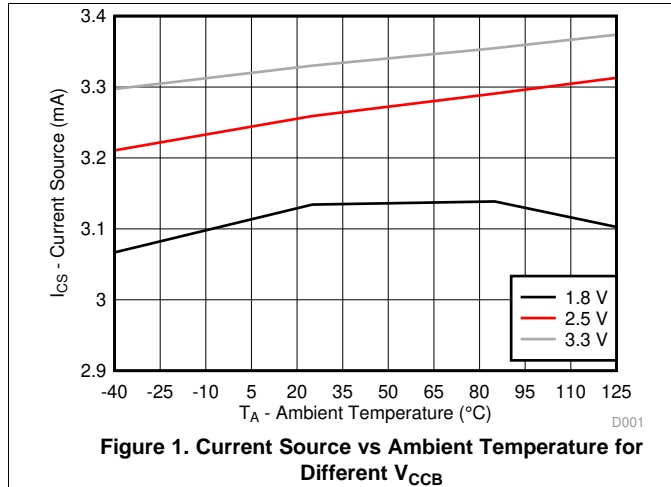
(1) Times are specified with loads of 1.35 k Ω and 50 pF on A-side and 50 pF on B-side. Different load resistance and capacitance alter the rise and fall times, thereby changing the propagation delay.

7.7 Switching Characteristics

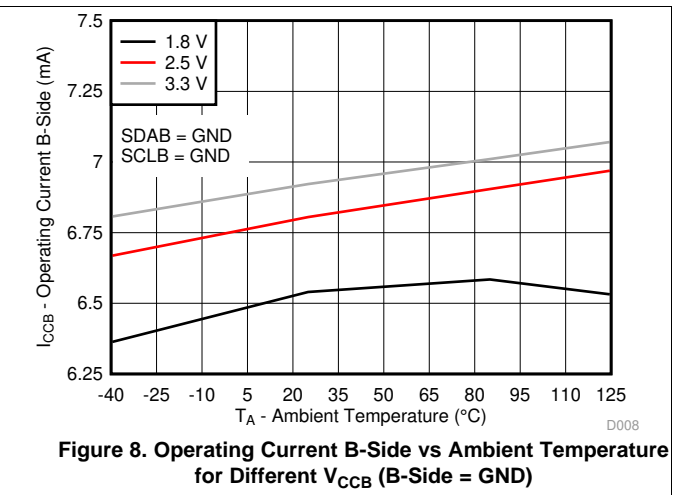
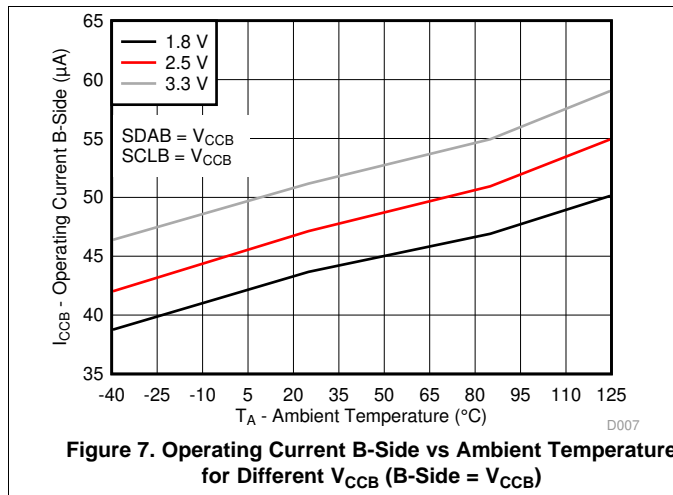
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|----------------------|--------------|-----|-----|------|---------------|
| t_{startup} | Startup time | | 60 | 350 | μs |
| t_{en} | Enable time | | 280 | 1000 | ns |
| t_{dis} | Disable time | | 700 | 1800 | ns |

7.8 Typical Characteristics



Typical Characteristics (continued)



8 Parameter Measurement Information

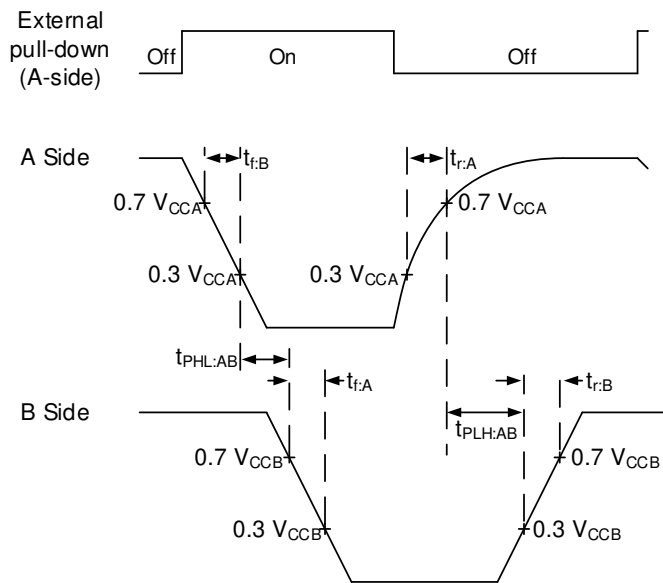
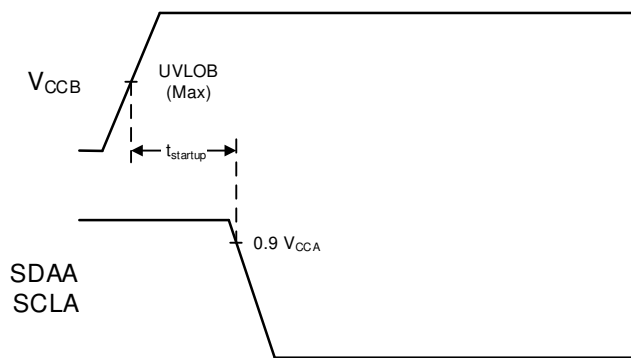
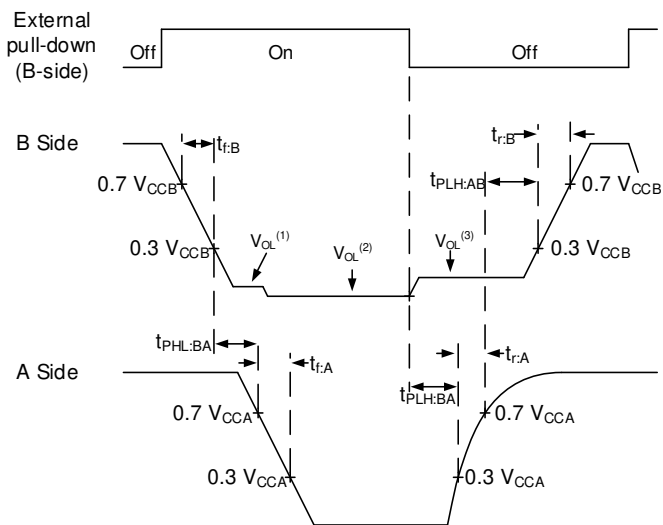


Figure 9. Propagation Delay and Transition Times for A-Side to B-Side



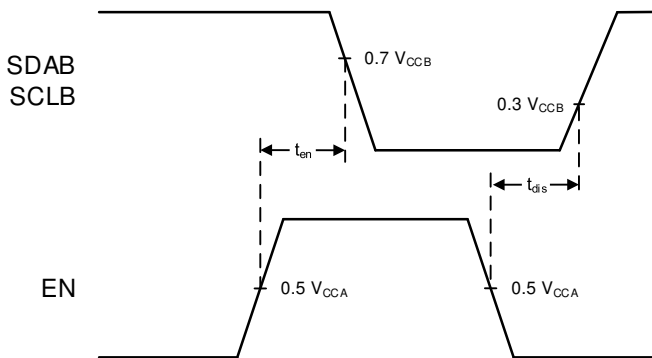
1) V_{CCA} is powered, SDAB/SCLB are connected to GND

Figure 11. Startup Time ($t_{startup}$)



- 1) The V_{OL} of only the external device, pulling down on the bus
- 2) The V_{OL} of both the external device and the TCA980x translator
- 3) The V_{OL} of only the TCA980x, after the external device releases

Figure 10. Propagation Delay for B-Side to A-Side



1) V_{CCA} is powered, SDA/SCLA are connected to GND

Figure 12. Enable and Disable Time (t_{en} and t_{dis})

9 Detailed Description

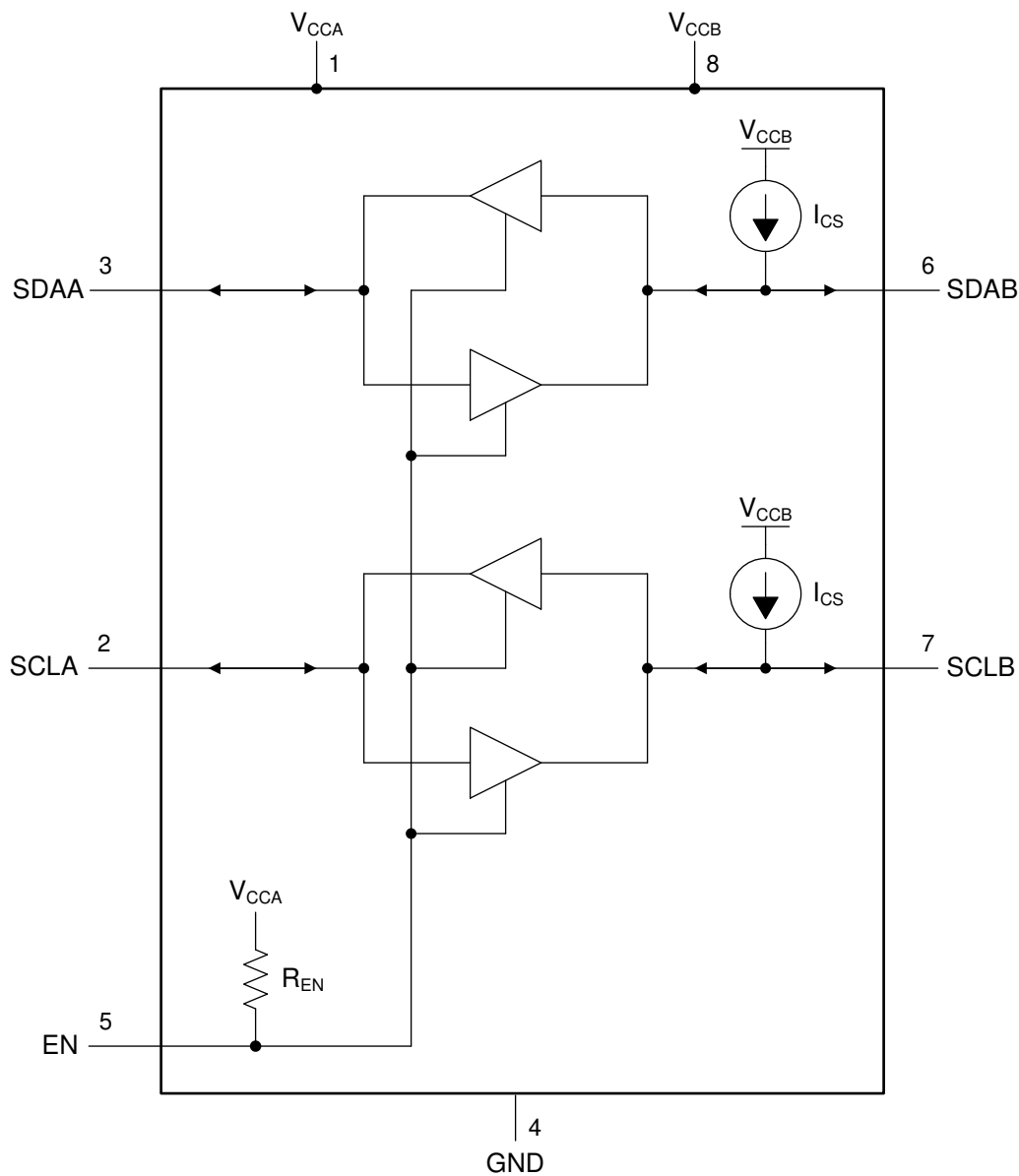
9.1 Overview

The TCA9803 is a dual-channel bidirectional buffer intended for I²C bus and SMBus/PMBus systems. It provides bidirectional level shifting (up-translation and down-translation) between low voltages (down to 0.8 V) and higher voltages (1.65 V to 3.6 V). The TCA9803 features an internal current source on the B-side of the device, allowing the removal of external pull-up resistors on the B-side. The current source also provides an improved rise time and ultra-low power consumption.

The TCA9803 is able to provide true buffering (rather than a pass-FET solution) without using a static voltage offset or incremental offset. This means that the V_{OL} on both the A and B sides of the TCA9803 are very low (approximately 0.2 V), helping to eliminate communication issues as a result of fixed V_{IL} thresholds. Another key feature of the TCA9803 is that there are no power sequencing requirements, or power supply dependencies. V_{CCA} can be greater than, less than, or equal to V_{CCB} . This gives the system designer flexibility with how the TCA9803 is used.

The TCA9803 is part of a four device family with varying current source strengths (see the [Device Comparison Table](#)).

9.2 Functional Block Diagram



For proper device operation, no external current sources (pull-up resistors) must be used on the SDAB and SCLB ports

9.3 Feature Description

9.3.1 Integrated Current Source

The TCA980x family has an integrated current source on the B side. By using an integrated current source, the device is able to measure current to determine if an external device is pulling down on the bus or not. This innovative detection method removes the need for a static voltage offset on the B side.

9.3.2 Ultra-Low Power Consumption

The TCA980x family features ultra low power consumption, to help maximum battery life, or cut down on power dissipation in sensitive applications.

9.3.3 No Static-Voltage Offset

The TCA980x family has no static-voltage offset, which are commonly used in buffered translators to prevent a device lock-up situation where the buffer's own output low could trip the input low threshold. The removal of the static voltage offset is significant because it allows the device to have low a low V_{OL} on the B side, which helps prevents communication issues that arise from connecting a static-voltage offset output device to an input with an input low threshold which is below the static voltage V_{OL} .

9.3.4 Active-High Repeater Enable Input

The TCA980x has an active-high enable (EN) input with an internal pull-up to VCCA, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. The EN input must change state only when the global bus and repeater port are in an idle state, to prevent system or communication failures. When enable is a logic LOW while VCCB is powered on, the internal current source on B side is still enabled. The enable pin does not disable the internal current source.

9.3.5 Powered Off High Impedance I²C Bus Pins on A-Side

The SCLA and SDAA pins enter a high impedance state when either VCCA or VCCB fall below their UVLO voltages. These pins are safe to continue having I²C communication on, even when the device is disabled or has no power.

The SCLB and SDAB pins remain powered by their current source (I_{CS}), even when VCCA is below UVLO. When VCCB falls below UVLO, the current source turns off, and a weak pull-up is connected to prevent the B-pins from floating. This is intended behavior, because no external pull-up resistors are to be used on the SDAB or SCLB pins. This behavior prevents the bus pins from floating, and allows it to follow VCCB.

9.3.6 Powered-Off Back-Power Protection for I²C Bus Pins

All I²C bus pins have protection circuitry to prevent current from flowing to the VCC pins from the I²C bus pins.

9.3.7 Clock Stretching and Multiple Master Arbitration Support

The TCA980x family supports clock stretching and multiple master arbitration methods, and helps to minimize overshoot during these hand offs between master and slave (or multiple masters).

9.4 Device Functional Modes

Table 1 shows the TCA980x function table.

Table 1. Enable Function Table

| INPUT EN | FUNCTION |
|----------|----------------------------|
| L | Outputs disabled |
| H | SDAA = SDAB SCLA = SCLB |

Table 2 lists the TCA980x B-Side current source functions.

Table 2. B-Side Current Source Function Table

| VCCB | FUNCTION |
|------|--|
| L | Current sources disabled, weak pull-up is connected with back-power protection |
| H | Current sources enabled |

9.4.1 Device Operation Considerations

9.4.1.1 B-Side Input Low ($V_{IL}/I_{ILC}/R_{ILC}$)

The TCA980x family utilizes the current source on the B side to determine whether an external device is driving the bus low, or if it is driving the bus low itself. As such, there are some parameters that must be met to ensure a successful transmission of a low from the B-side to the A-side. These parameters are listed in Table 3.

Table 3. B-side Input Low-Level Parameters

| PARAMETER | SHORT DESCRIPTION | DETAILED INFORMATION |
|--|---|---------------------------------------|
| V_{IL} Low-level input voltage | The input voltage that is interpreted as a low. On the B-side, I_{ILC} must also be satisfied to maintain a low | See the V_{ILC} & I_{ILC} section |
| I_{ILC} Low-level input current (contention) | The minimum amount of current that an external device must be sinking from the TCA980x to transmit a low. V_{IL} must also be satisfied | See the V_{ILC} & I_{ILC} section |
| R_{ILC} Low-level allowed pull-down resistance | The maximum allowed pull-down resistance of an external device in order to successful transmit a low | See the R_{ILC} section |

9.4.1.1.1 V_{ILC} & I_{ILC}

The I_{ILC} parameter is the minimum amount of current that the external device must sink from the TCA980x in order for the TCA980x to accept the low on the B-side.

In order for the TCA980x to accept a low on the B-side, both V_{IL} and I_{ILC} parameters must be satisfied. In an idle bus condition (both A and B sides are high), meeting the V_{IL} threshold with an external device pull-down meets the I_{ILC} requirement, since the pull-down has to sink the entire I_{CS} (current source value) current before the voltage on the pin falls.

In a contention situation (the A-side is being driven low externally, and the B-side is driven low by the TCA980x), the V_{IL} requirement is already satisfied by the TCA980x alone (Since the output low voltage is less than the V_{IL} threshold). In order for a device on the B-side to over-drive the A-side, it must sink the I_{ILC} value for the TCA980x to accept that the low is now being driven by the B-side. This helps reduce or eliminate overshoot during the hand off between a slave an master during a clock-stretching event, or an acknowledge.

External pull-up resistors on the B-side are not allowed for this reason. As the additional current provided by them may hinder an external device from being able to satisfy the TCA980x's I_{ILC} requirement. For more information on this and allowed external current into the device, see the [Input and Output Leakage Current \(\$I_{EXT-}/I_{EXT-O}\$ \)](#) section.

9.4.1.1.2 R_{ILC}

The R_{ILC} parameter describes the maximum allowed pull-down resistance. This parameter comes from the combination of I_{ILC} and I_{CS} , and states the maximum resistance that can satisfy the I_{ILC} parameter. Note that series resistors on the bus are going to affect this, as seen with other types of buffers (voltage delta across the series resistor. This increases the effective V_{OL} of the external device pulling the bus low).

The calculated resistance of the internal pull-down FET of an external device can be calculated from the V_{OL} and I_{OL} measurements of the external device in question using Equation 1. Take care to consider any series resistors placed in the path from the TCA980x to any external device. Note that R_{PD} is the calculated resistance of the internal pull-down FET, and not a resistor to ground. This is for determining if the external device's output characteristics meet the TCA980x R_{ILC} requirement (150 Ω).

$$R_{PD} = V_{OL} / I_{OL} \tag{1}$$

9.4.1.2 Input and Output Leakage Current (I_{EXT-I}/I_{EXT-O})

The Input external current (I_{EXT-I}) and output external current (I_{EXT-O}) parameters describe the amount of parasitic current either injected into the device or pulled from the device (such as leakage from ESD cells) without affecting device operation as shown in Table 4.

Table 4. B-Side Input and Output Leakage Current

| PARAMETER | SHORT DESCRIPTION | DETAILED INFORMATION |
|------------------------------------|--|-----------------------------|
| I_{EXT-I} Input leakage current | Current that is external, but pulled up to supply, leaking current into the TCA980x B-side. An example is a leaky ESD cell from VCC, or an external pull-up resistor. | See the I_{EXT-I} section |
| I_{EXT-O} Output leakage current | Current that is pulled from the TCA980x B-side. ESD cells are the most common form of output leakage. Care must be taken not to violate this spec, otherwise the leakage current can create a false low. | See the I_{EXT-O} section |

9.4.1.2.1 I_{EXT-I}

I_{EXT-I} is a current source that is external to the TCA980x B-side, but leaks current into the device. This type of input leakage may not exceed the I_{EXT-I} maximum spec, or else the minimum I_{ILC} value does not apply.

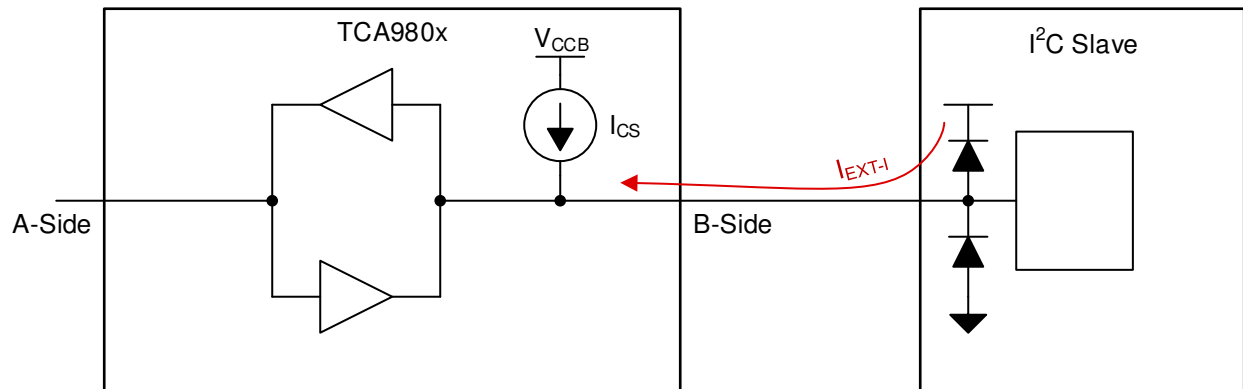


Figure 13. I_{EXT-I} Example

As shown in Figure 13, I_{EXT-I} is a source of additional current into the device, shown as a leaky ESD cell. The user must keep I_{EXT-I} as close to 0 as possible, since the TCA980x has a current source as a pull-up internally, and uses this current source to help detect which side is driving a low. As I_{EXT-I} increases, it increases the minimum I_{ILC} value, requiring that an external device sink more current from the TCA980x in order to transmit a low. There must be no external pull-up resistor on the B-side to contribute to I_{EXT-I} .

9.4.1.2.2 I_{EXT-O}

I_{EXT-O} is an unintentional current from the TCA980x's internal current source that is external. Leaking ESD cells are a common contributor to leakage current. This type of input leakage may not exceed the I_{EXT-O} maximum spec, or else the TCA980x can interpret this excessive current as an external device transmitting a low, causing the bus to latch. It is important to consider the total sum of I²C slave device's leakage to ground, and that it does not violate I_{EXT-O} . An example showing a typical I_{EXT-O} leakage path through an ESD cell is shown in Figure 14.

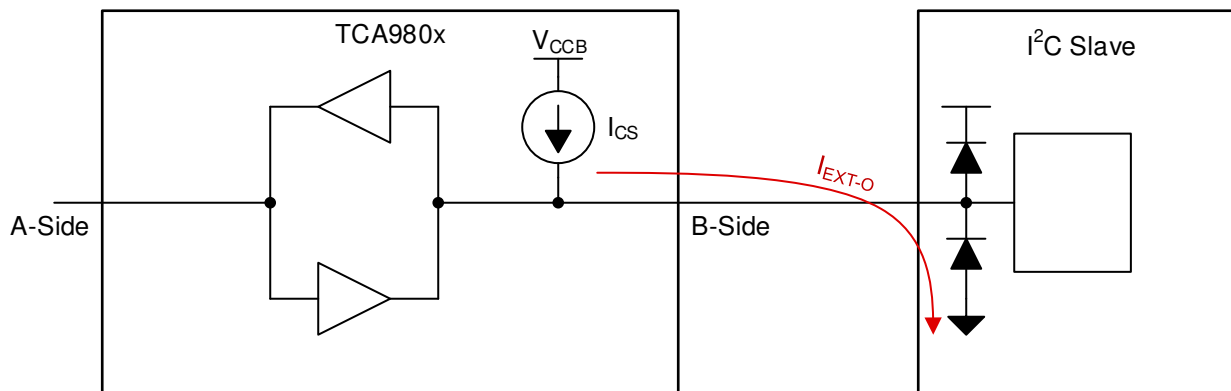


Figure 14. I_{EXT-O} Example

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Device Selection Guide

The TCA980x family has 4 different variants, with different strengths of the internal current source as shown in [Table 5](#).

Table 5. TCA980x Family

| Part Number | I _{CS} : Current Source Value |
|-------------|--|
| TCA9800 | 0.54 mA |
| TCA9801 | 1.1 mA |
| TCA9802 | 2.2 mA |
| TCA9803 | 3.3 mA |

It is acceptable to select the TCA9803 as the default, since it is able to drive 400-pF bus capacitance loads at 400 kHz. For system designers looking to optimize selection, see the [Detailed Design Procedure](#) section for single device for detailed examples of how to select a part number for a specific application.

10.1.2 Special Considerations for the B-side

The TCA980x supports many types of connections between other TCA980x and other buffers/translators. Care must be taken to ensure that all of the B-side requirements be satisfied. For example, FET/pass-gate based translators typically cannot be used on the B-side, because they require pull-up resistors on both sides, and when one side is pulling low, the FET/switch closes, likely causing I_{EXT-I} to be violated (See the [I_{EXT-I}](#) section for more information).

The [FET or Pass-Gate Translators](#) and [Buffered Translators/Level-shifters](#) sections list some use-cases that are not supported or require special considerations when connected to the B-ports, note that these considerations only apply to the B-side of the TCA980x family.

10.1.2.1 FET or Pass-Gate Translators

Some translators are based on pass-gates for translation support. In most of the use cases, external pull-up resistors are required to pull the bus to the voltage rail.

It is important to note that these special operating requirements apply only to the B-side ports of the TCA980x. For example, the TCA9517 B-side can be safely connected to the A-side of the TCA980x, but not to the B-side of the TCA980x. However, it is OK to connect the A-side of the TCA9517 to the B-side (or A-side) of the TCA980x, because the A-side does not have a static voltage offset based output.

Figure 17 shows an example of the incorrect connection on the B-side to a buffer with a static voltage offset output. The reason this is unacceptable is because the equivalent output resistance of the output buffer is greater than the maximum R_{ILC} allowed. See the R_{ILC} section for more information.

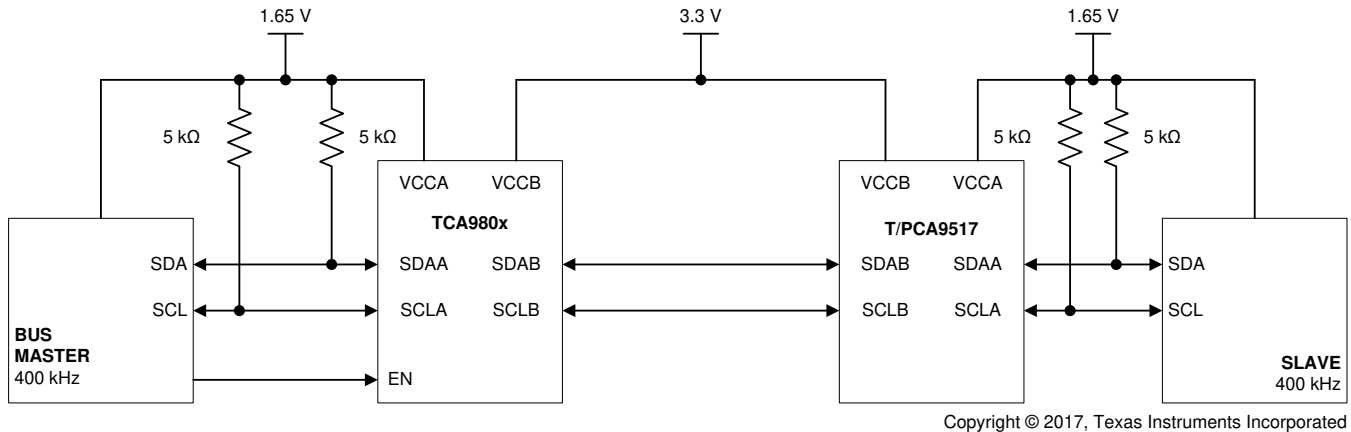


Figure 17. Incorrect B-Side Static Voltage Offset Buffer Connection

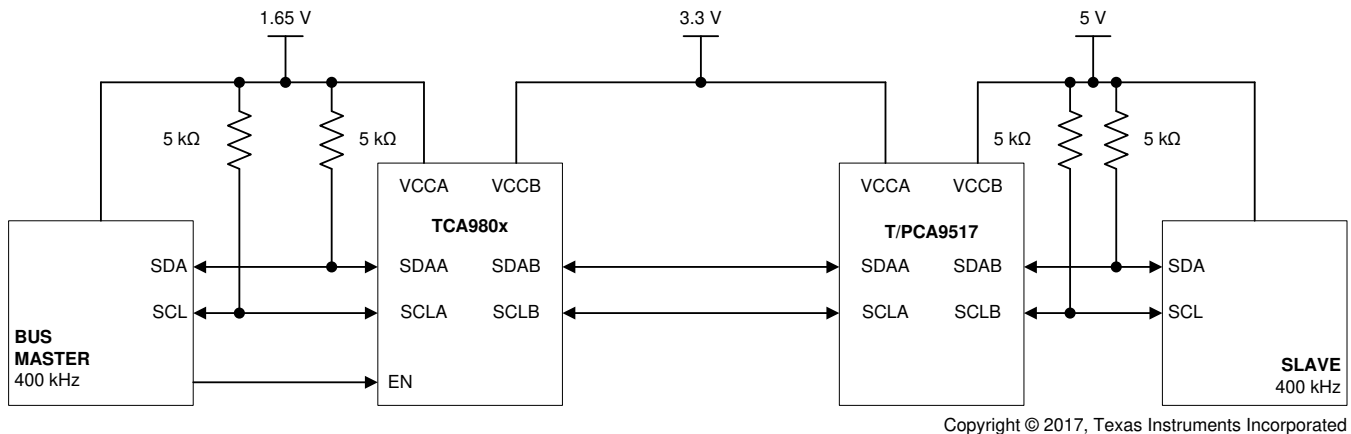


Figure 18. Correct Connection With Other Buffers

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 μ F and 0.1 μ F) must be placed close to each power supply pin.

As shown in Figure 18, this connection is acceptable for use on the B-side ports of the TCA980x, because the equivalent R_{ILC} of the A-side of this example buffer is less than 150 Ω .

10.2 Typical Application

10.2.1 Single Device

The typical application for the TCA980x family is to be used as a buffering translator, where the V_{CCA} and V_{CCB} are at different values in order to level-shift the I²C bus voltages.

Typical Application (continued)

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation as shown in the *I_{EXT-I}* section.

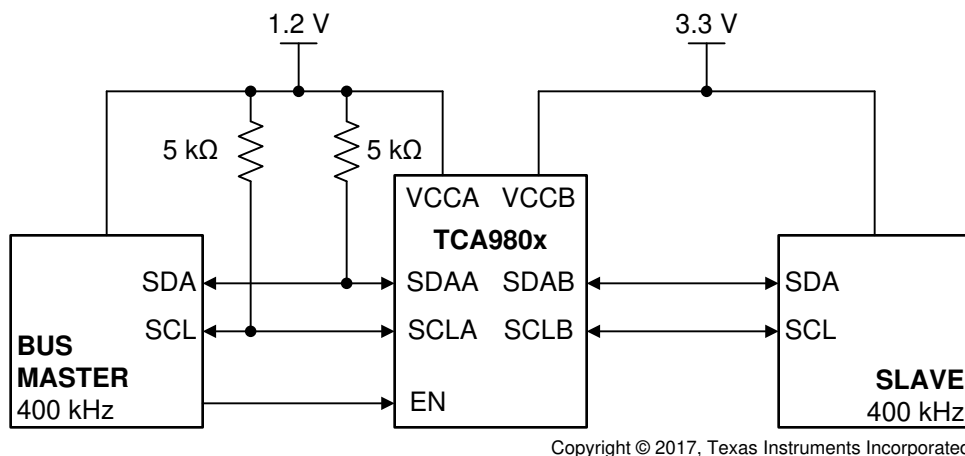


Figure 19. Typical Level-Shifting Application Example (Master on A-side)

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 μF and 0.1 μF) must be placed close to each power supply pin.

As shown in Figure 20, the I²C master can be on the B-side, and that it is ok to have $V_{CCA} > V_{CCB}$. The only requirements are that no external source of current (pull-up resistor or current source) be on the B-pins of the TCA9803, and that both V_{CCA}/V_{CCB} values are within the recommended range. As a note, since the EN pin is referenced to the VCCA supply voltage, when the master is on the A-side, the system designer must ensure that the enable pin voltage is pulled up to V_{CCA} (either with an external or the internal pull-up resistor) to ensure that the device is enabled.

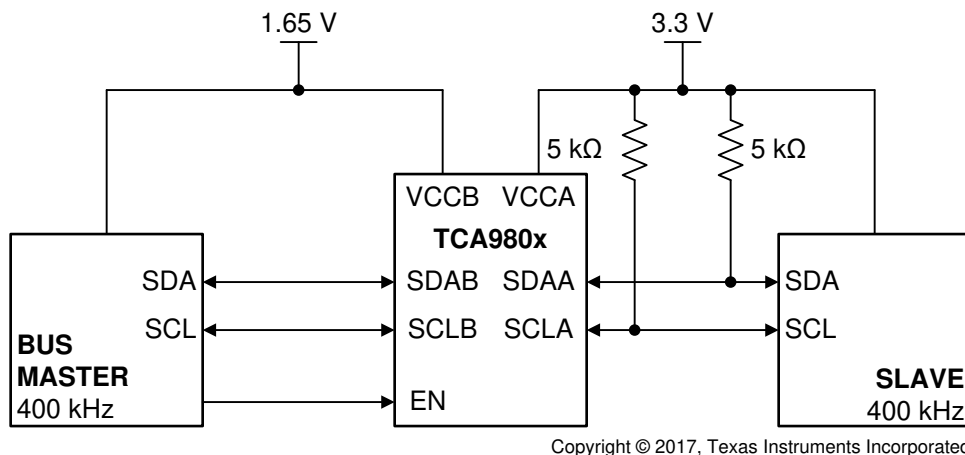


Figure 20. Typical Level-Shifting Application Example (Master on B-side)

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 μF and 0.1 μF) must be placed close to each power supply pin.

Typical Application (continued)

10.2.1.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information in [Table 6](#) must be known. The setup in [Figure 19](#) is used for these example design requirements.

C_L is the capacitance of the bus, including the pin capacitance of each slave device connected, and the capacitance of the board trace. It is possible to estimate the bus capacitance by summing up the pin capacitances of each slave device on the node (using 10-pF per slave is a safe estimate, since this is the maximum allowed per the I²C specification), but trace capacitance requires an estimation through simulation or by getting the capacitance per unit length from the board manufacturer.

Table 6. Design Requirements

| Parameter | Description | Acceptable Range | Example Value/Target |
|-----------|--|------------------|----------------------|
| C_L | Load capacitance (bus capacitance) on B-side | up to 400 pF | 100 pF |
| t_r | Rise time | up to 300 ns | ≤ 150 ns |
| V_{CCA} | VCCA supply voltage | 0.8 V-3.6 V | 1.2 V |
| V_{CCB} | VCCB supply voltage | 1.65 V-3.6 V | 3.3 V |
| f_{SCL} | I ² C clock frequency | | 400 kHz |

10.2.1.2 Detailed Design Procedure

Selection of the correct device is important for designers wanting optimize power consumption while transmitting.

Selecting the pull-up resistor required for the A-side is well documented already, see the [I²C Bus Pullup Resistor Calculation](#) application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

Since the B-ports of the TCA980x family have an integrated current source, the rise time is easily calculated with [Equation 2](#). The graphs in the [Application Curves](#) section show the maximum capacitance load that each device can drive (based on minimum I_{CS} value) to achieve a desired rise time, for different V_{CCB} voltages.

$$t_r = C_L \frac{(0.4 \times V_{CCB})}{I_{CS}} \quad (2)$$

The target design requirements example is intended for 400-kHz I²C, so the appropriate selection graph to use is [Figure 22](#), and specifically [Figure 27](#) since VCCB supply voltage is 3.3 V. In [Figure 21](#), the graph has the appropriate regions shaded to help illustrate how to select the appropriate device. When looking at the general selection graphs, note that voltage line shifts evenly between the 1.65 V and 3.6 V traces in the general selection graphs. For example, if VCCB in another example is 2.5 V, then the selection graph is based on a line in the middle of the 1.65 V and the 3.6 V trace.

As shown in [Figure 21](#), the shaded region is the appropriate region based on design requirements listed in [Table 6](#). Any line that touches this shaded region is able to meet the design requirements. In this example, the TCA9803 and the TCA9802 both are able to satisfy the design requirements, since they both touch the shaded region. The TCA9800 and the TCA9801 both fall below the shaded region. While the TCA9801 is able to meet a rise time of about 190 ns at 100 pF (acceptable by the fast-mode rise time requirements), the design target in this example was ≤ 150 ns. This is a consideration a system designer can make, sacrificing rise time for a lower-power device, but in this example, the 150 ns limit is going to be upheld).

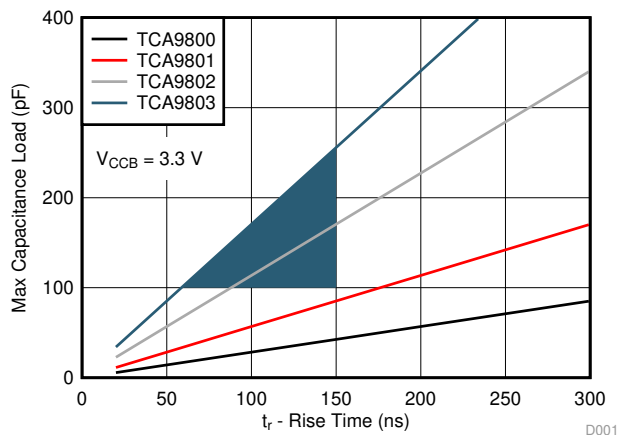


Figure 21. Selection Guide Based on Example Design Requirements

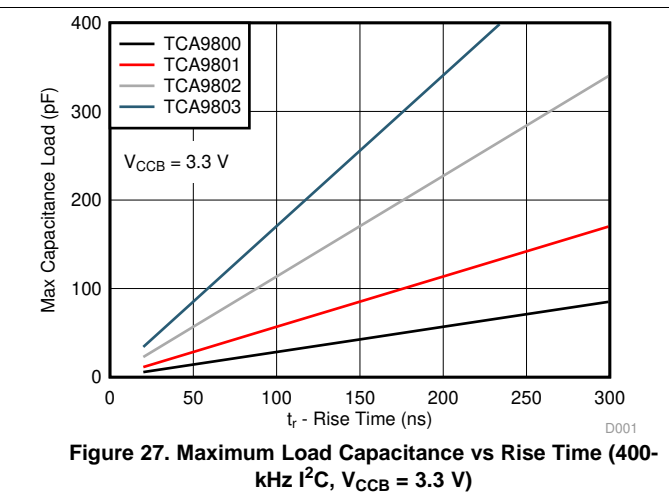
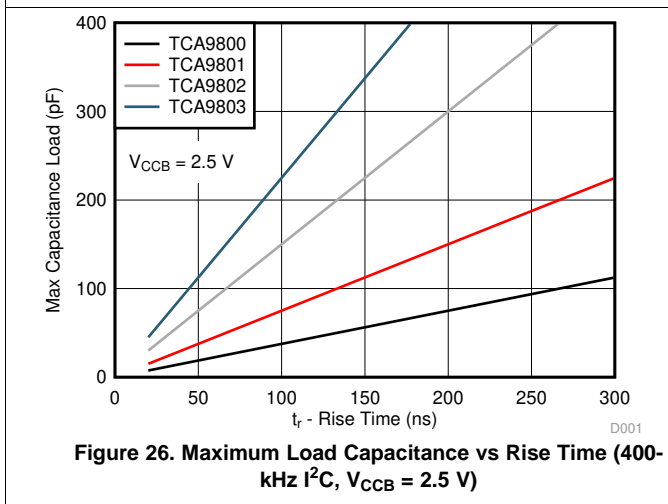
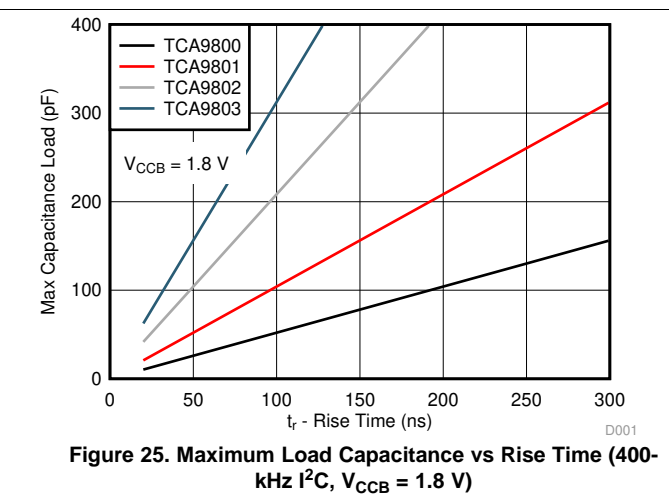
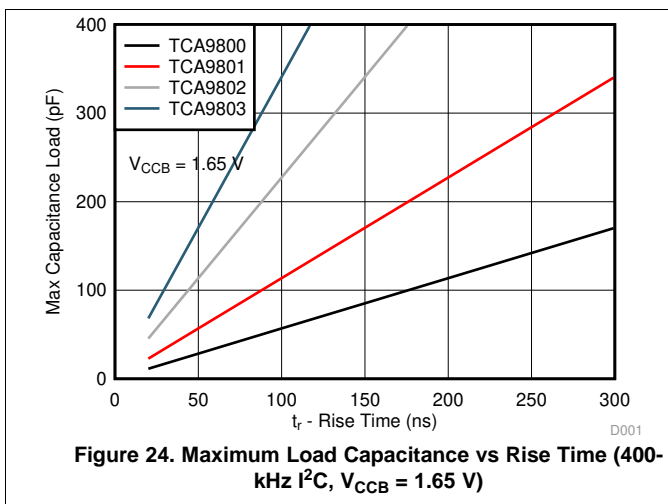
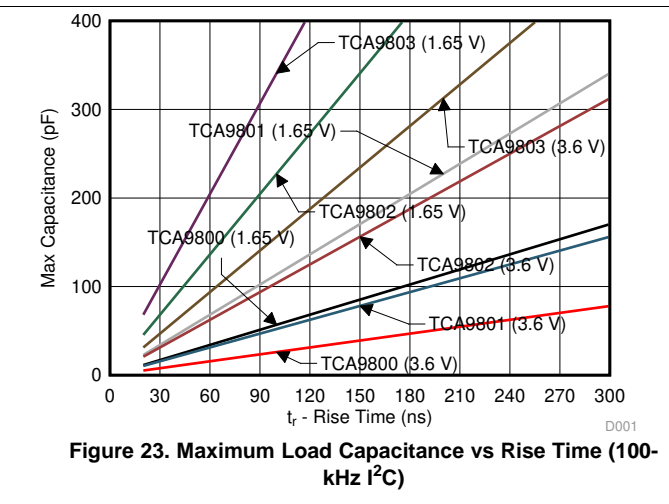
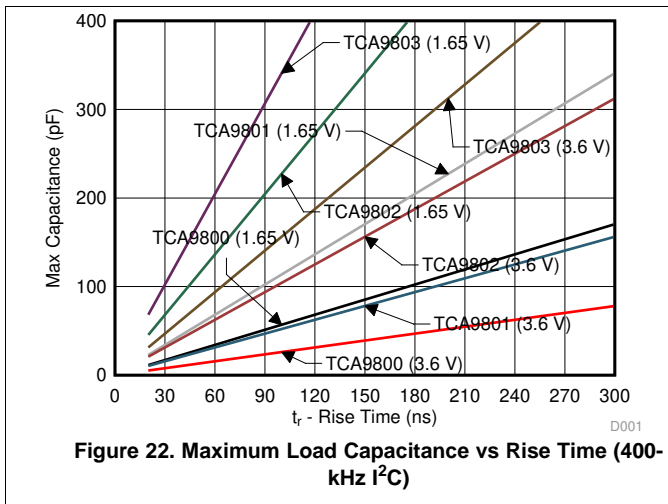
NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 μ F and 0.1 μ F) must be placed close to each power supply pin.

Based on the selection graph shown above, the TCA9802 is selected, since it is the lowest-power device's trace (grey trace) which touches the shaded region. The TCA9803 may also be used without any consequences.

10.2.1.3 Application Curves

The application curves can be used to select the appropriate part for a given design requirement, or to estimate the rise-time.



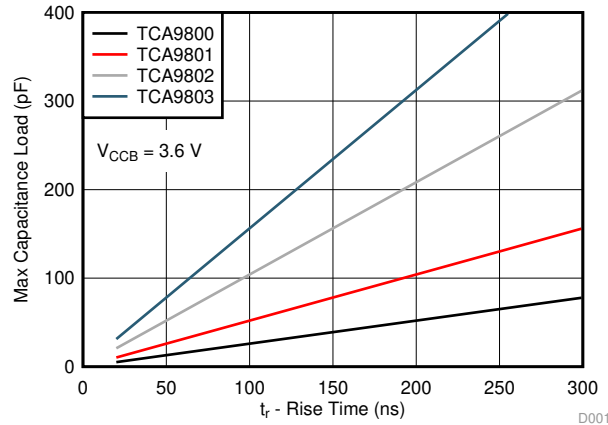
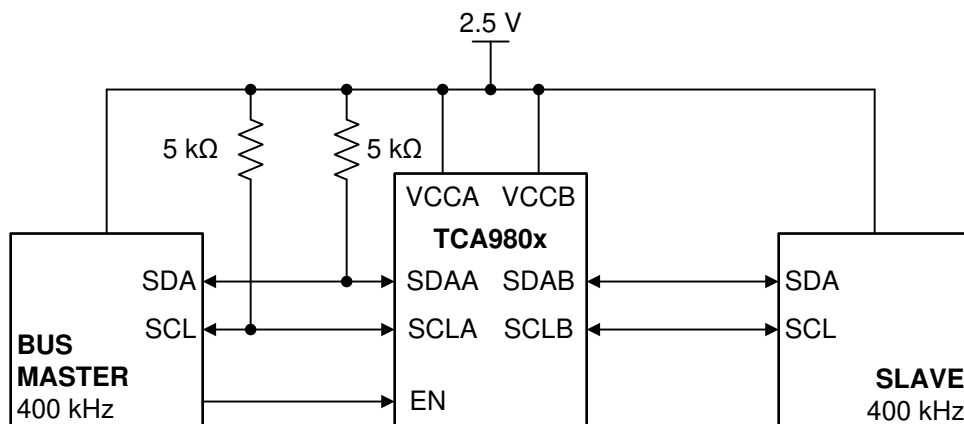


Figure 28. Maximum Load Capacitance vs Rise Time (400-kHz I²C, V_{CCB} = 3.6 V)

10.2.2 Buffering Without Level-Shifting

The TCA980x family supports buffering use cases which do not need level-shifting or voltage-translation.

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation as shown in the [I_{EXT-I}](#) section.



Copyright © 2017, Texas Instruments Incorporated

Figure 29. Buffering Use Case Without Level-Shifting

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 μF and 0.1 μF) must be placed close to each power supply pin.

10.2.2.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information in [Table 7](#) must be known. The setup in [Figure 29](#) is used for these example design requirements.

Table 7. Design Requirements

| Parameter | Description | Acceptable Range | Example Value/Target |
|----------------|--|------------------|----------------------|
| C _L | Load capacitance (bus capacitance) on B-side | up to 400 pF | 200 pF |
| t _r | Rise time | up to 300 ns | ≤ 300 ns |

Table 7. Design Requirements (continued)

| Parameter | Description | Acceptable Range | Example Value/Target |
|------------------|----------------------------------|------------------|----------------------|
| V _{CCA} | V _{CCA} supply voltage | 0.8 V-3.6 V | 2.5 V |
| V _{CCB} | V _{CCB} supply voltage | 1.65 V-3.6 V | 2.5 V |
| f _{SCL} | I ² C clock frequency | | 400 kHz |

10.2.2.2 Detailed Design Procedure

Selecting the pull-up resistor required for the A-side is well documented already, see the [I2C Bus Pullup Resistor Calculation](#) application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

Selection process of each device is identical to the procedure described in the [Device Selection Guide](#) section, except that it must be done for each individual TCA980x. This section jumps straight to the selection graphs to show the selection process. See the [Detailed Design Procedure](#) section for single device for detailed information.

As shown in [Figure 30](#), the shaded region is the appropriate region based on design requirements listed in [Table 7](#). Any line that touches this shaded region is able to meet the design requirements. In this example, the TCA9803, TCA9802, and TCA9801 are able to satisfy the design requirements, since they all touch the shaded region. The TCA9800 falls below the shaded region.

Based on the selection graph shown above, the TCA9801 is selected, since it is the lowest-power device which touches the shaded region (red trace). The TCA9803 or the TCA9802 may also be used without any consequences.

10.2.2.3 Application Curve

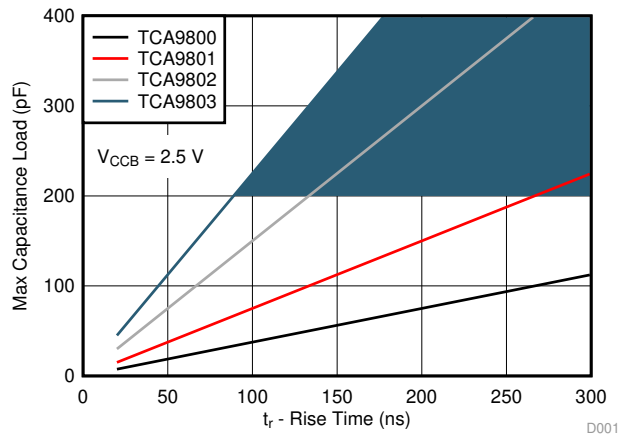


Figure 30. Selection Guide Based On Example Design Requirements

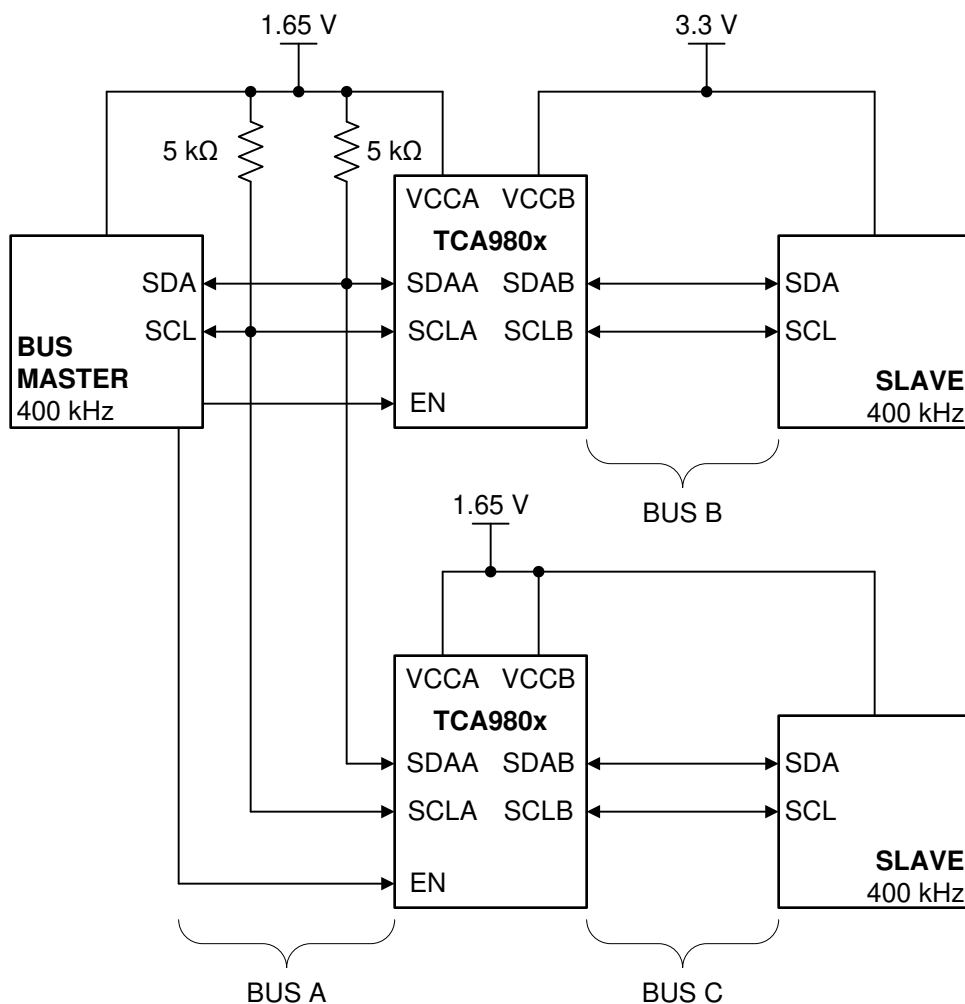
10.2.3 Parallel Device Use Case

The TCA980x family supports multiple TCA980x used in parallel. The A-sides of the TCA980x are allowed to be connected together.

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation shown in the [I_{EXT-I}](#) section.

NOTE: B-sides of TCA980x devices may never be connected to each other, because the I_{EXT-I} specification limit is violated. See the [I_{EXT-I}](#) section for more information.

NOTE: The B-side may not be connected to another translator if it uses a static-voltage offset. The R_{ILC} spec is violated since the static voltage offset adjusts the output resistance to ground to be outside of the R_{ILC} spec requirement, causing the TCA980x to be unable to recognize a low.



Copyright © 2017, Texas Instruments Incorporated

Figure 31. Parallel Use Case

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 μ F and 0.1 μ F) must be placed close to each power supply pin.

10.2.3.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information shown in Table 8 and Table 9 must be known. The setup in Figure 31 is used for these example design requirements.

Table 8. Design Requirements for Bus B

| Parameter | Description | Acceptable Range | Example Value/Target |
|-----------|--|------------------|----------------------|
| C_L | Load capacitance (bus capacitance) on B-side | up to 400 pF | 300 pF |
| t_r | Rise time | up to 300 ns | ≤ 300 ns |
| V_{CCA} | VCCA supply voltage | 0.8 V-3.6 V | 1.65 V |
| V_{CCB} | VCCB supply voltage | 1.65 V-3.6 V | 3.3 V |

Table 8. Design Requirements for Bus B (continued)

| Parameter | Description | Acceptable Range | Example Value/Target |
|------------------|----------------------------------|------------------|----------------------|
| f _{SCL} | I ² C clock frequency | | 400 kHz |

Table 9. Design Requirements for Bus C

| Parameter | Description | Acceptable Range | Example Value/Target |
|------------------|--|------------------|----------------------|
| C _L | Load capacitance (bus capacitance) on B-side | up to 400 pF | 40 pF |
| t _r | Rise time | up to 300 ns | ≤ 300 ns |
| V _{CCA} | VCCA supply voltage | 0.8 V-3.6 V | 1.65 V |
| V _{CCB} | VCCB supply voltage | 1.65 V-3.6 V | 1.65 V |
| f _{SCL} | I ² C clock frequency | | 400 kHz |

10.2.3.2 Detailed Design Procedure

Selecting the pull-up resistor required for the A-side (Bus A) is well documented already, see the [I2C Bus Pullup Resistor Calculation](#) application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

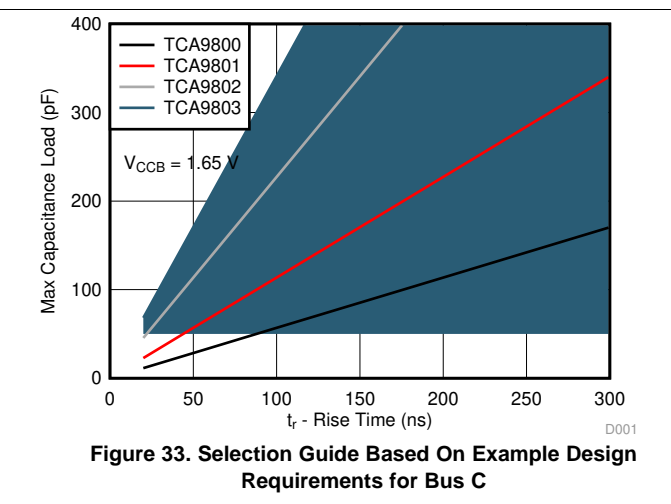
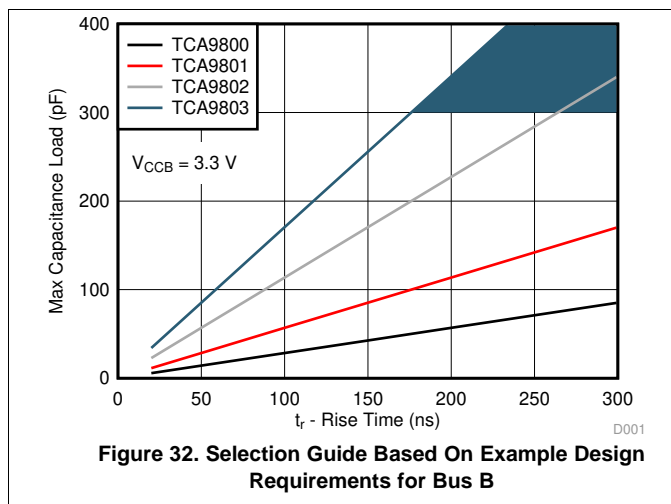
Selection process of each device is identical to the procedure described in the [Device Selection Guide](#) section, except that it must be done for each individual TCA980x. This section jumps straight to the selection graphs to show the selection process. See the [Detailed Design Procedure](#) section for single device for detailed information.

Based on [Figure 32](#), the TCA9802 or the TCA9803 are the devices which are able to meet the design requirements. The TCA9802 is the most optimized selection, but the TCA9803 can be used without issue.

Based on [Figure 33](#), all 4 variants of the TCA980x family meet the design requirements. The TCA9800 is the most optimized selection, but any of the variants can be used without issue.

As the system designer, the choice can be made to go for the most optimized part selections (TCA9802 for bus B and TCA9800 for bus C), but it is also ok to use the TCA9802 or the TCA9803 on both busses, because they both satisfy the design requirements of both busses.

10.2.3.3 Application Curves



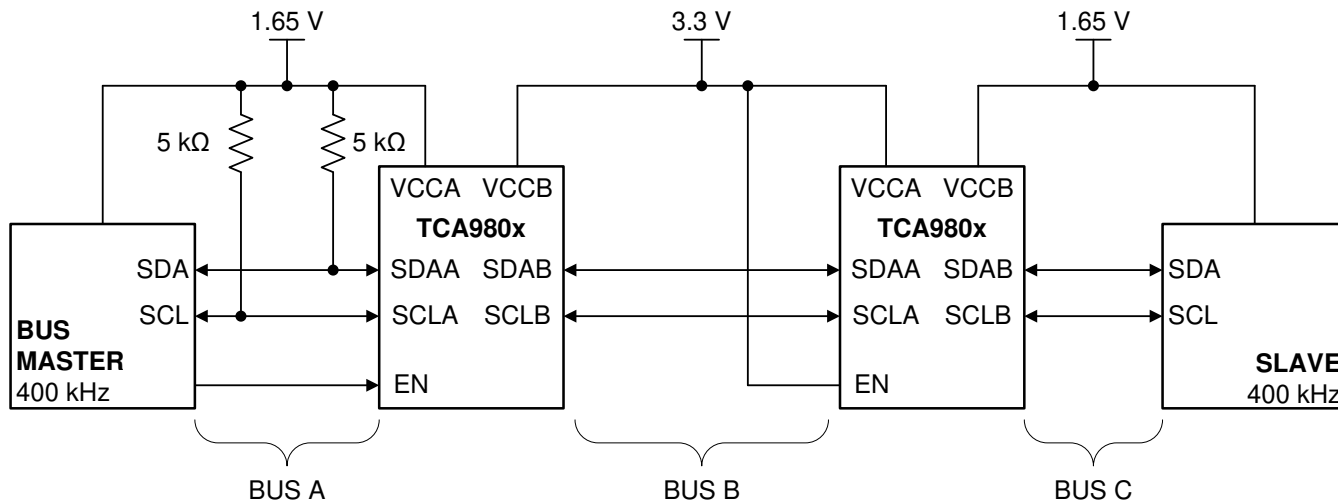
10.2.4 Series Device Use Case

The TCA980x family supports multiple TCA980x used in series. It is acceptable to connect A sides together, or have A sides connect to B sides, but B-sides may never be connected together.

It is critical to note that there are no external sources of current allowed on the B-side ports, since this can affect device operation as shown in the [I_{EXT-I}](#) section.

NOTE: B-sides of TCA980x devices may never be connected to each other, because the I_{EXT-I} specification limit is violated. See the I_{EXT-I} for more information.

NOTE: The B-side may not be connected to another translator if it uses a static-voltage offset. The R_{ILC} spec is violated since the static voltage offset adjusts the output resistance to ground to be outside of the R_{ILC} spec requirement, causing the TCA980x to be unable to recognize a low.



Copyright © 2017, Texas Instruments Incorporated

Figure 34. Series Use Case

NOTE

Decoupling capacitors are not shown to keep the illustration simple. Decoupling capacitors (1 μ F and 0.1 μ F) must be placed close to each power supply pin.

10.2.4.1 Design Requirements

The system designer must first select the correct variant of the TCA980x family for the load. In order to do this, the information in Table 10 and Table 11 must be known. The setup in Figure 34 is used for these example design requirements.

Table 10. Design Requirements for Bus B / 1st TCA980x

| Parameter | Description | Acceptable Range | Example Value/Target |
|-----------|--|------------------|----------------------|
| C_L | Load capacitance (bus capacitance) on B-side | up to 400 pF | 300 pF |
| t_r | Rise time | up to 300 ns | ≤ 200 ns |
| V_{CCA} | VCCA supply voltage | 0.8 V-3.6 V | 1.65 V |
| V_{CCB} | VCCB supply voltage | 1.65 V-3.6 V | 3.3 V |
| f_{SCL} | I ² C clock frequency | | 400 kHz |

Table 11. Design Requirements for Bus C / 2nd TCA980x

| Parameter | Description | Acceptable Range | Example Value/Target |
|-----------|--|------------------|----------------------|
| C_L | Load capacitance (bus capacitance) on B-side | up to 400 pF | 100 pF |
| t_r | Rise time | up to 300 ns | ≤ 250 ns |
| V_{CCA} | VCCA supply voltage | 0.8 V-3.6 V | 3.3 V |
| V_{CCB} | VCCB supply voltage | 1.65 V-3.6 V | 1.65 V |
| f_{SCL} | I ² C clock frequency | | 400 kHz |

10.2.4.2 Detailed Design Procedure

Selecting the pull-up resistor required for the A-side (Bus A) is well documented already, see the [I2C Bus Pullup Resistor Calculation](#) application report. The rest of this section deals only with selection of a device based on the B-side design requirements.

Selection process of each device is identical to the procedure described in the [Device Selection Guide](#) section, except that it must be done for each individual TCA980x. This section jumps straight to the selection graphs to show the selection process. See the [Detailed Design Procedure](#) section for single device for detailed information.

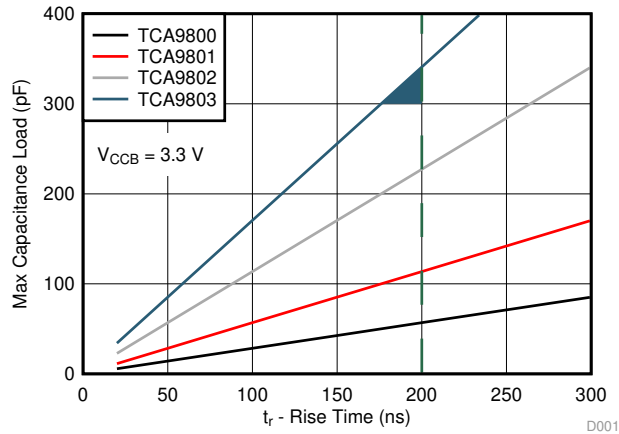


Figure 35. Selection Guide Based on Example Design Requirements for Bus B

Based on [Figure 35](#), the TCA9803 is the only device which can satisfy the design requirements. Had the rise time requirement been ≤ 300 ns, then the TCA9802 also works, but the design requirement was 200 ns.

Based on [Figure 36](#), all 4 variants of the TCA980x family meet the design requirements. The TCA9800 is the most optimized selection, but any of the variants can be used without issue.

As the system designer, the choice can be made to go for the most optimized part selections (TCA9803 for bus B and TCA9800 for bus C), but it is also ok to use the TCA9803 on both busses, because it can satisfy the design requirements of both busses.

10.2.4.3 Application Curve

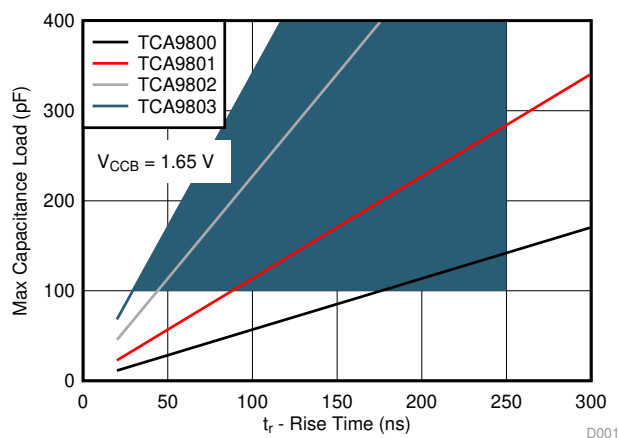


Figure 36. Selection Guide Based on Example Design Requirements for Bus C

11 Power Supply Recommendations

The following need to be ensured when designing with the TCA980x family:

- V_{CCA} is within the recommended voltage range
- V_{CCB} is within the recommended voltage range

There are no supply sequencing requirements, V_{CCA} may ramp before, after, or at the same time as V_{CCB} .

There are no supply dependency requirements. V_{CCA} may be greater than, less than, or equal to V_{CCB} . Each supply has its own requirement of voltage range, but there is no required relationship between V_{CCA} and V_{CCB} values.

It is recommended that decoupling capacitors be used on the power supplies (0.1 μF and 1 μF) and that they be placed as close as possible to the V_{CCA} and V_{CCB} pins.

12 Layout

12.1 Layout Guidelines

There are no special considerations required for most I²C translators, but there are common practices which are always recommended.

It is recommended that decoupling capacitors be used on the power supplies (0.1 μ F and 1 μ F) and that they be placed as close as possible to the VCCA and VCCB pins.

12.2 Layout Example

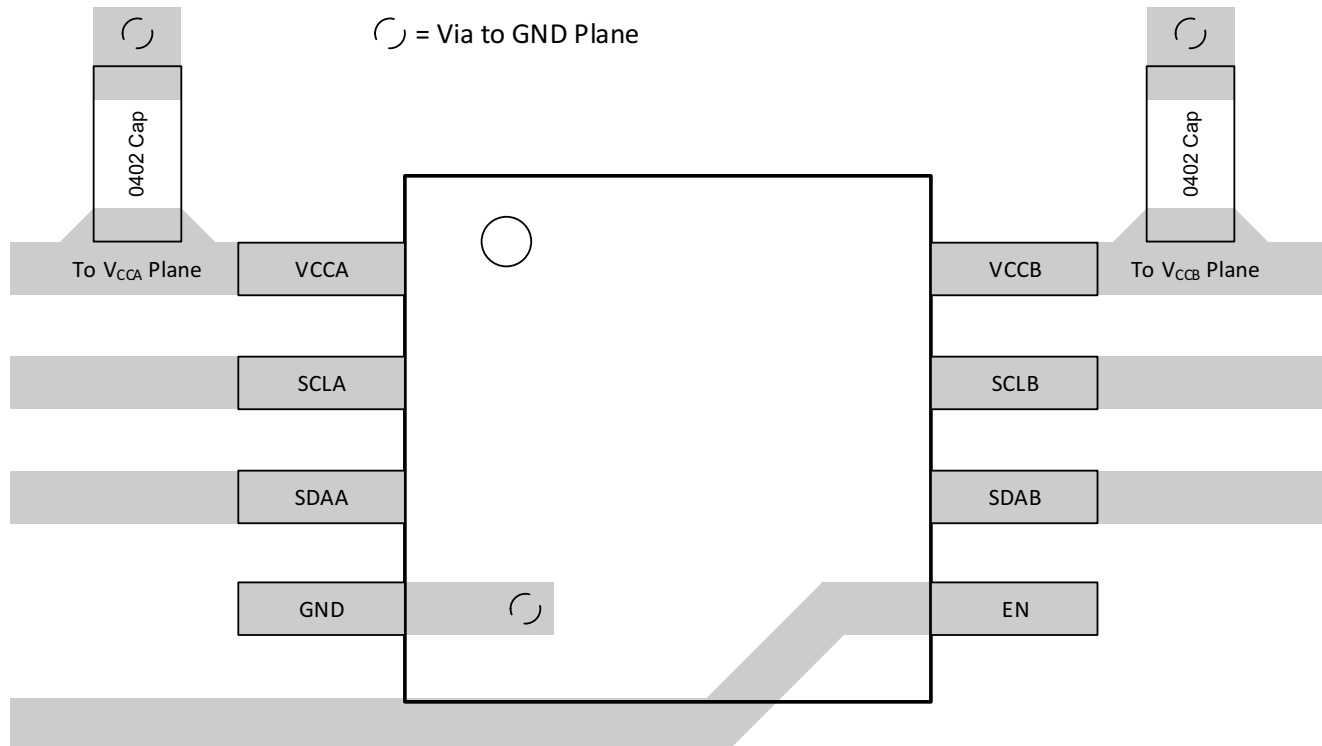


Figure 37. TCA980x DGK Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

関連資料については、以下を参照してください。

- 『[I2Cバスのプルアップ抵抗値の計算](#)』
- 『[リピータを使用するI2Cバスの最大クロック周波数](#)』
- 『[ロジックへの入門](#)』
- 『[I2Cバスについて理解する](#)』
- 『[新しい設計用の適切なI2Cデバイスの選択](#)』

13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.3 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.4 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TCA9803DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG SN | Level-1-260C-UNLIM | -40 to 125 | 15C | Samples |
| TCA9803DGKT | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | NIPDAUAG SN | Level-1-260C-UNLIM | -40 to 125 | 15C | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated