TEXAS INSTRUMENTS
TCAN1046A-Q1
JAJSJE4 – JULY 2021

TCAN1046A-Q1 車載用、デュアル CAN FD トランシーバ、スタンバイ・モード付き

ADVANCE INFORMATION

1 特長

- AEC-Q100 (グレード 1): 車載アプリケーション認定済み
- モード制御を備えた 2 つの独立した高速 CAN FD トランシーバ
- ISO 11898-2:2016 物理層規格の要件に適合
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- Classical CAN のサポートと最適化された CAN FD 性能 (2、5、8Mbps)
  - 短く対称的な伝搬遅延時間によりタイミング・マージンを強化
- 12V および 24V バッテリ・アプリケーションに対応
- レシーバ同相入力電圧: ±12V
- 保護機能:
  - バス・フォルト保護: ±58V
  - 低電圧保護
  - TXD ドミナント・タイムアウト (DTO)
    - 最小 9.2kbps のデータ・レート
  - サーマル・シャットダウン保護 (TSD)
- 動作モード:
  - 通常モード
  - リモート・ウェイクアップ要求をサポートする、低消費電力スタンバイ・モード
- 電源非接続時の最適化された挙動
  - バスおよびロジック・ピンは高インピーダンス (動作中のバス、アプリケーションに対して無負荷)
  - ホットプラグ対応: 電源オン / オフ時のバスおよび RXD 出力のグリッチ・フリー動作
- 接合部温度範囲: -40℃～150℃
- SOIC (14) パッケージおよび自動光学検査 (AOI) 性能を向上させたリードレス VSON (14) パッケージ (4.5mm × 3.0mm) で供給

2 アプリケーション

- 自動車および輸送システム
  - 車体制御モジュール
  - 車載ゲートウェイ
  - 先進運転支援システム (ADAS)
  - インフォテインメント

3 概要

TCAN1046A-Q1 は、ISO 11898-2:2016 高速 CAN (Controller Area Network) 仕様の物理層要件を満たすデュアル高速 CAN トランシーバです。

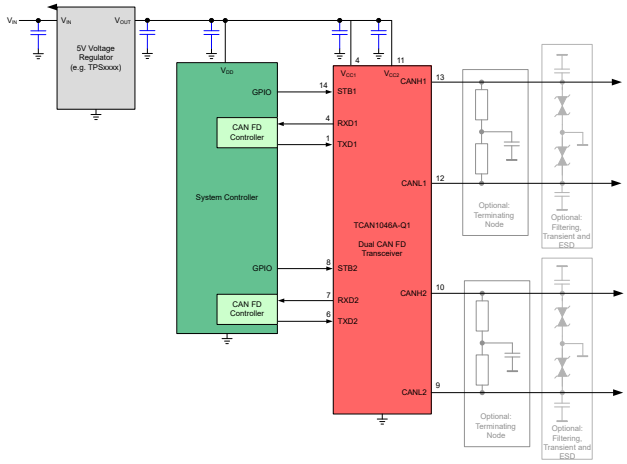
このデバイスは、Classical CAN ネットワークおよび最高 8 メガビット/秒 (Mbps) の CAN FD ネットワークの両方に対応しています。このデバイスには 2 つの CAN FD チャネルがあり、独立した電源 (V_{CC1} と V_{CC2}) とモード制御 (STB1 ピンと STB2 ピン) を備えているため、各 CAN チャネルは完全に独立して動作できます。各チャネルが互いに独立して動作できることは、冗長性が要求されるアプリケーションや、システム障害時にバックアップとして追加の CAN FD チャネルが動作する必要があるアプリケーションにおいて重要です。

このデバイスは、サーマル・シャットダウン (TSD)、TXD ドミナント・タイムアウト (DTO)、最高 ±58V のバス・フォルト保護を含む多くの保護および診断機能も備えています。このデバイスは、電源低電圧またはフローティング・ピンのシナリオでフェイルセーフ動作を定義しています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TCAN1046A-Q1	VSON (DMT) (14)	4.50mm × 3.00mm
	SOIC (D) (14)	8.95mm × 3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

4 Pin Configuration and Functions

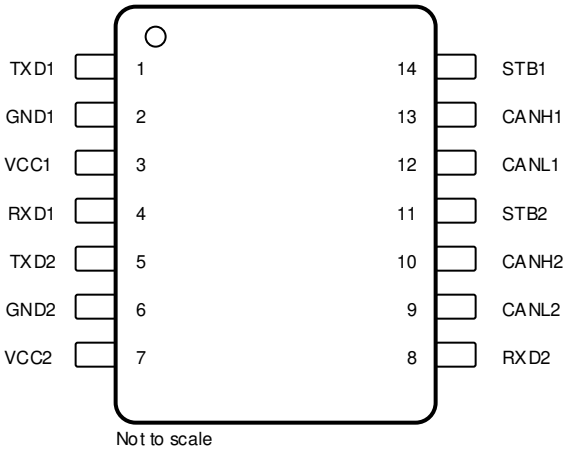


図 4-1. D Package, 14 Pin SOIC, Top View

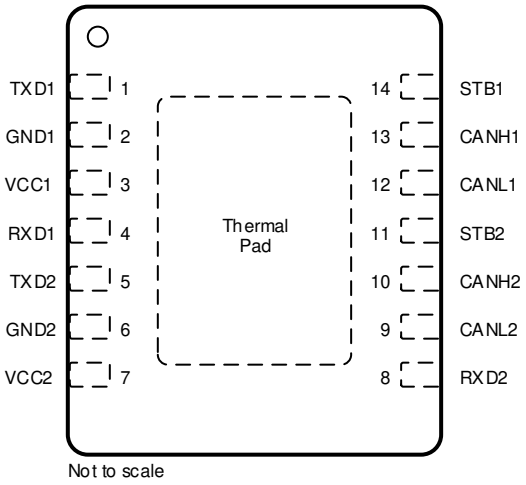


図 4-2. DMT Package, 14 Pin VSON, Top View

表 4-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input 1, integrated pull-up
GND1	2	GND1	Ground connection, transceiver 1
V_{CC1}	3	Supply	5-V supply voltage, transceiver 1
RXD1	4	Digital Output	CAN receive data output 1, tri-state when $V_{CC} < UV_{VCC}$
TXD2	5	Digital Input	CAN transmit data input 2, integrated pull-up
GND2	6	GND2	Ground connection, transceiver 2
V_{CC2}	7	Supply	5-V supply voltage, transceiver 2
RXD2	8	Digital Output	CAN receive data output 2, tri-state when $V_{CC} < UV_{VCC}$
CANL2	9	Bus IO	Low-level CAN bus 2 input/output line
CANH2	10	Bus IO	High-level CAN bus 2 input/output line
STB2	11	Digital Input	Standby input 2 for mode control, integrated pull-up
CANL1	12	Bus IO	Low-level CAN bus 1 input/output line
CANH1	13	Bus IO	High-level CAN bus 1 input/output line
STB1	14	Digital Input	Standby input 1 for mode control, integrated pull-up
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

5 Device and Documentation Support

5.1 Device Support

This device conforms to the following CAN standards. The core of what is needed is covered within this system specification; however, reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources are helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

5.1.1 Device Nomenclature

CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016 High speed medium access unit (original High Speed CAN transceiver standard)
- ISO 11898-5 High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode).
- ISO 11898-6 High speed medium access unit with selective wake.
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- CAN FD 1.0 Spec and Papers
- Bosch “Configuration of CAN Bit Timing”, Paper from 6th International CAN Conference (ICC), 1999. This is repeated a lot in the DCAN IP CAN Controller spec copied into this system spec.
- GMW3122: GM requirements for HS CAN
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps

EMC requirements:

- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for HS CAN

Conformance Test requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

5.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ADVANCE INFORMATION

5.6 Glossary

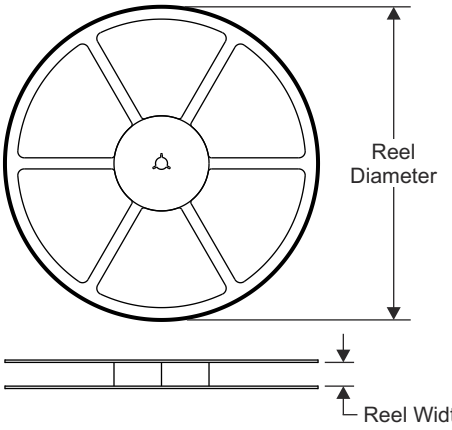
TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

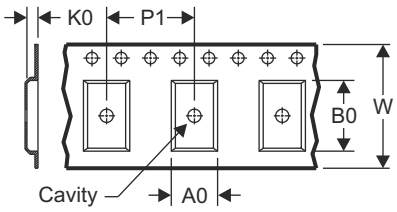
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Tape and Reel Information

REEL DIMENSIONS

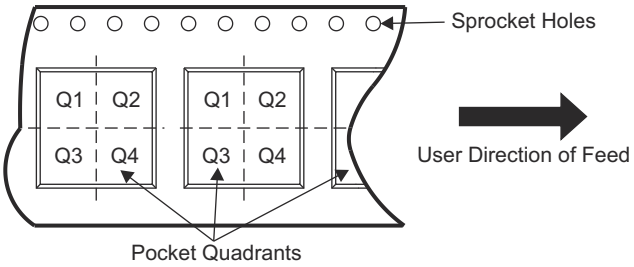


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

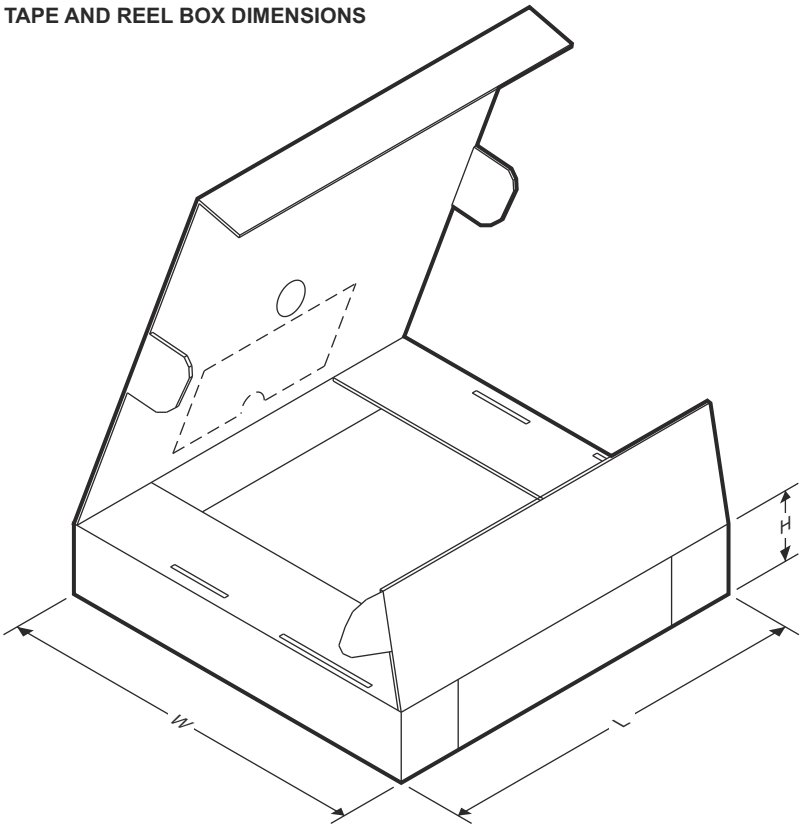


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1046ADMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.2	4.7	1.15	8.0	12.0	Q1
TCAN1046ADRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



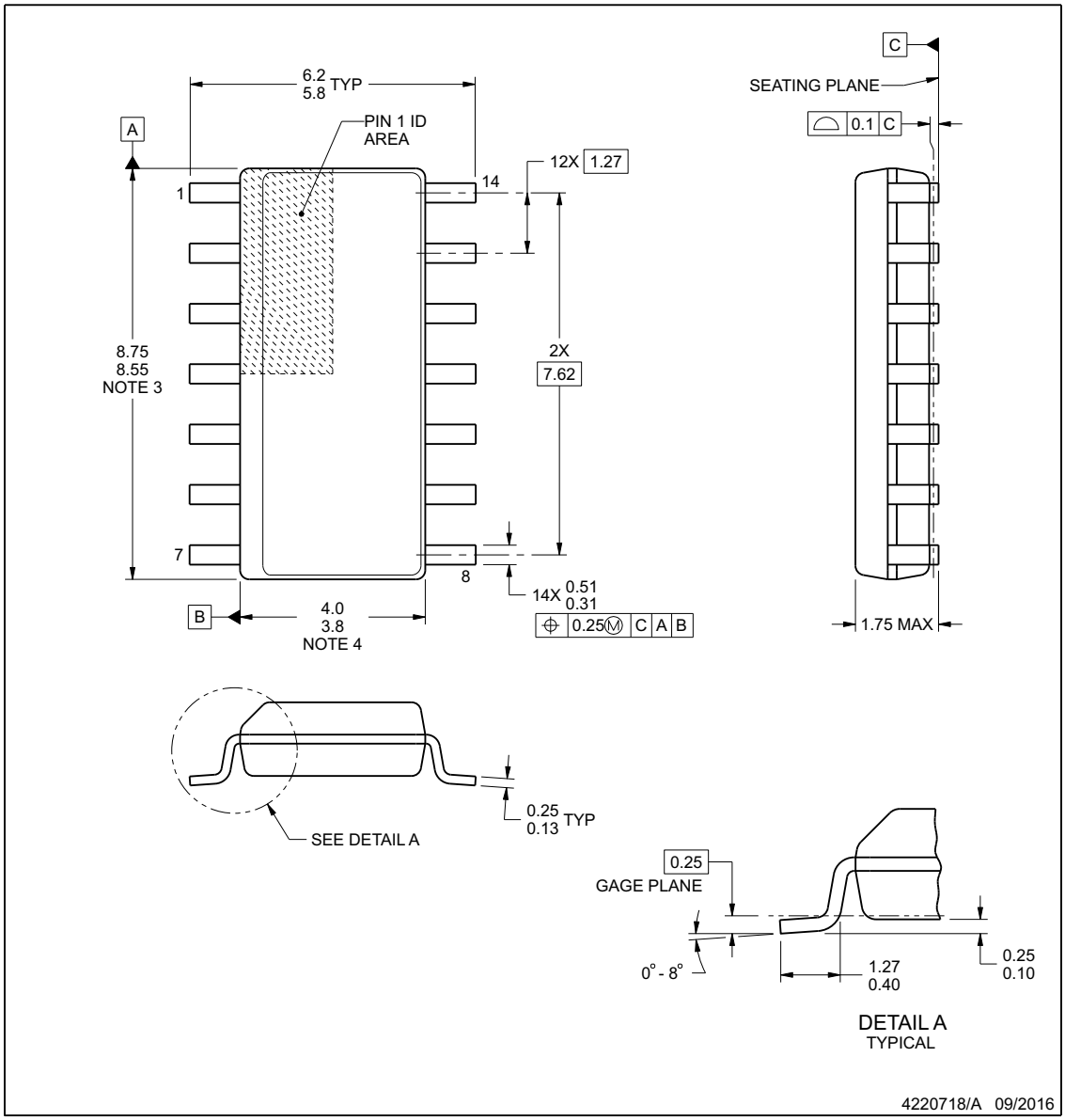
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1046ADMTRQ1	VSON	DMT	14	3000	370.0	355.0	55.0
TCAN1046ADRQ1	SOIC	D	14	2500	853.0	449.0	35.0

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

ADVANCE INFORMATION

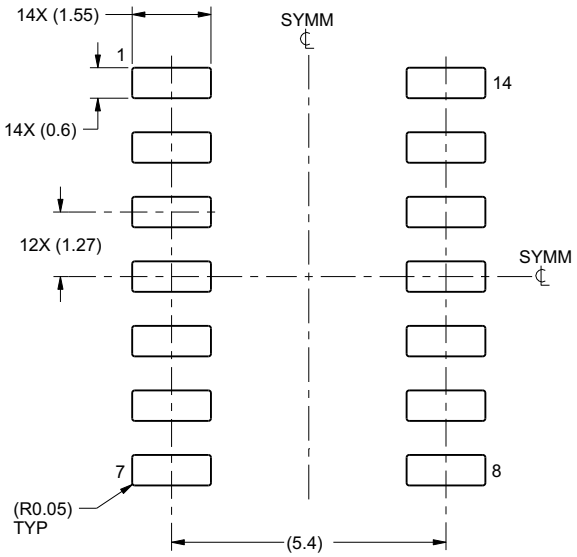
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

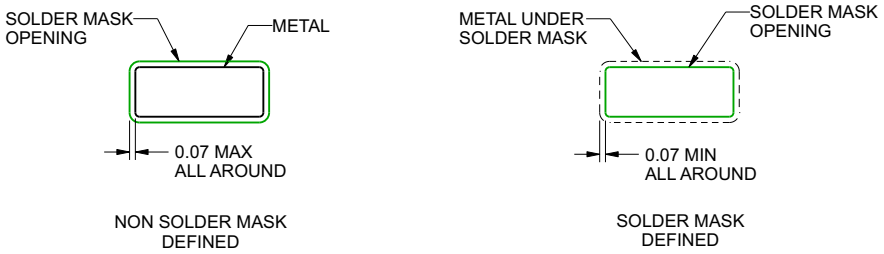
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

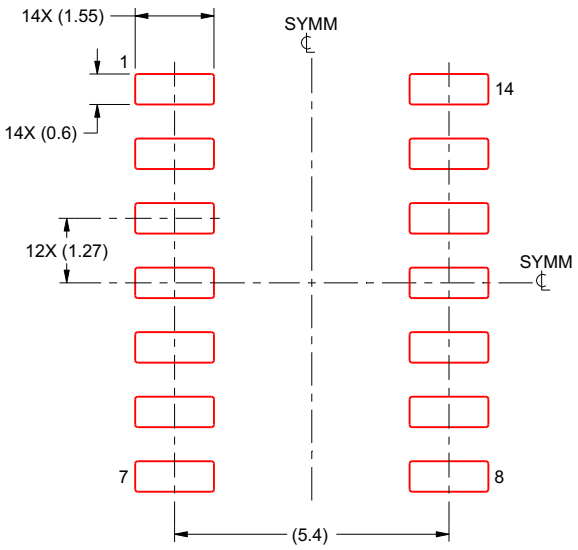
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

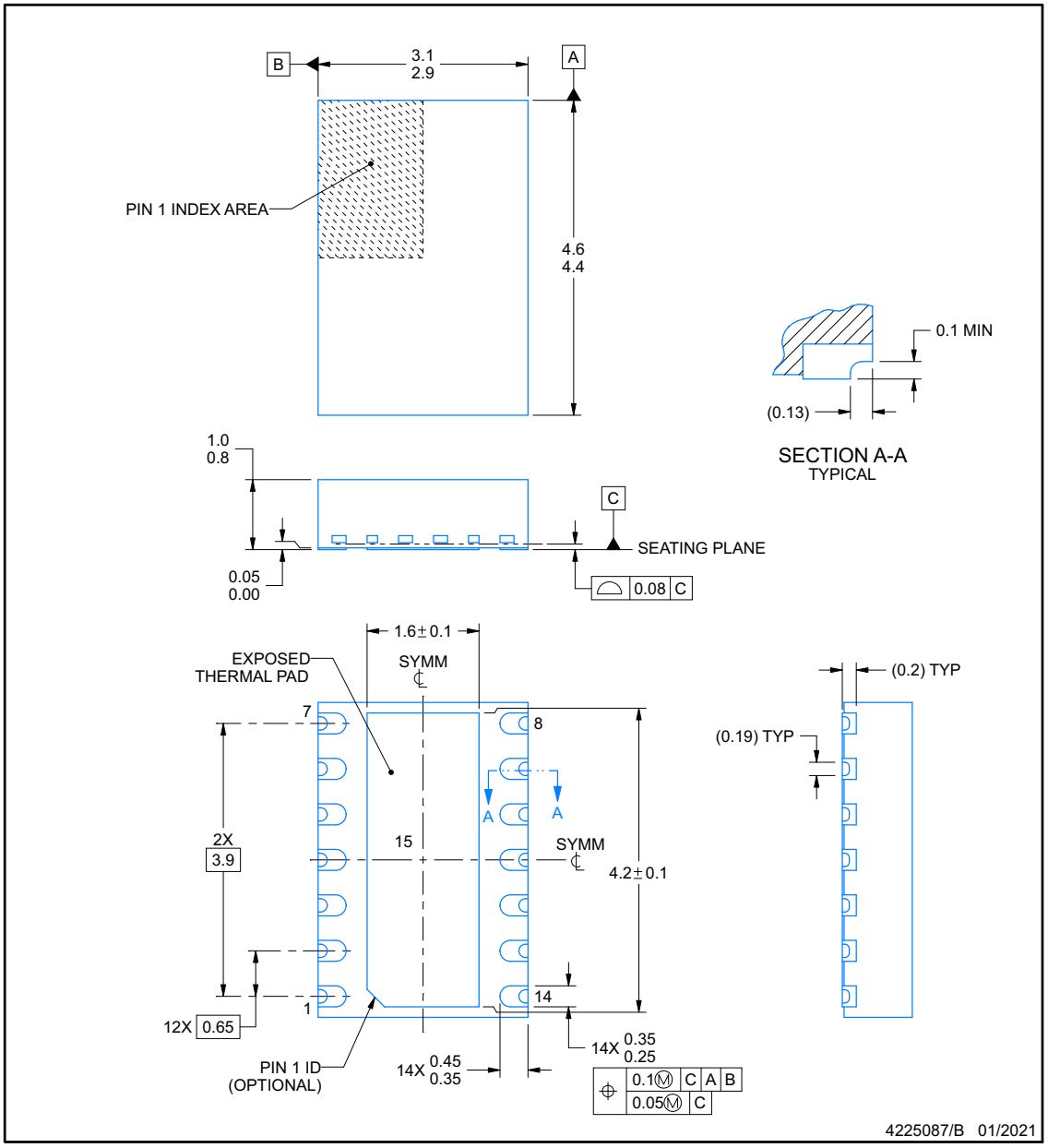
ADVANCE INFORMATION

PACKAGE OUTLINE

DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

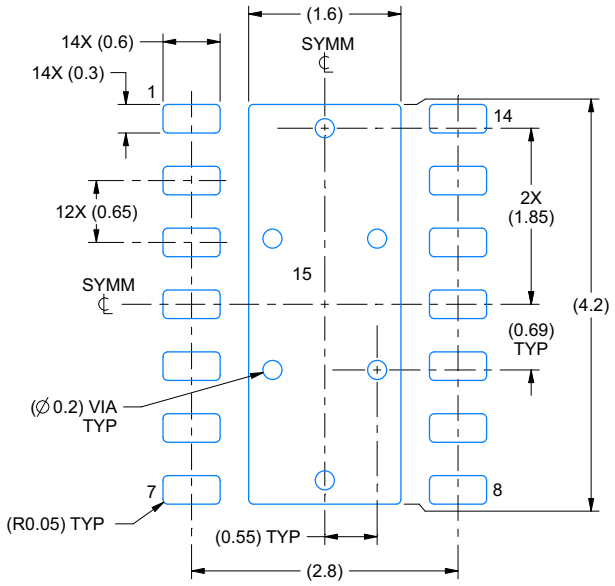
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

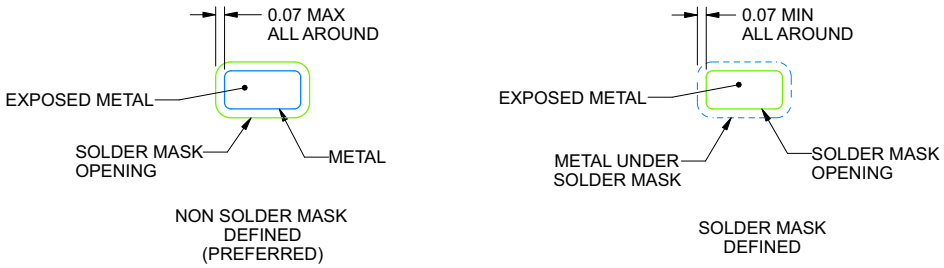
DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

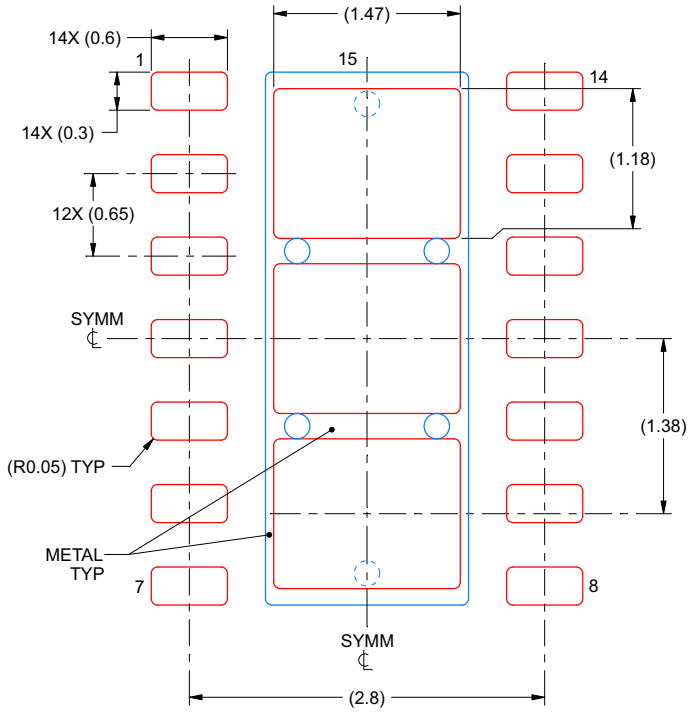
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DMT0014B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1046ADMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1046A	Samples
TCAN1046ADRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

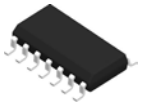
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

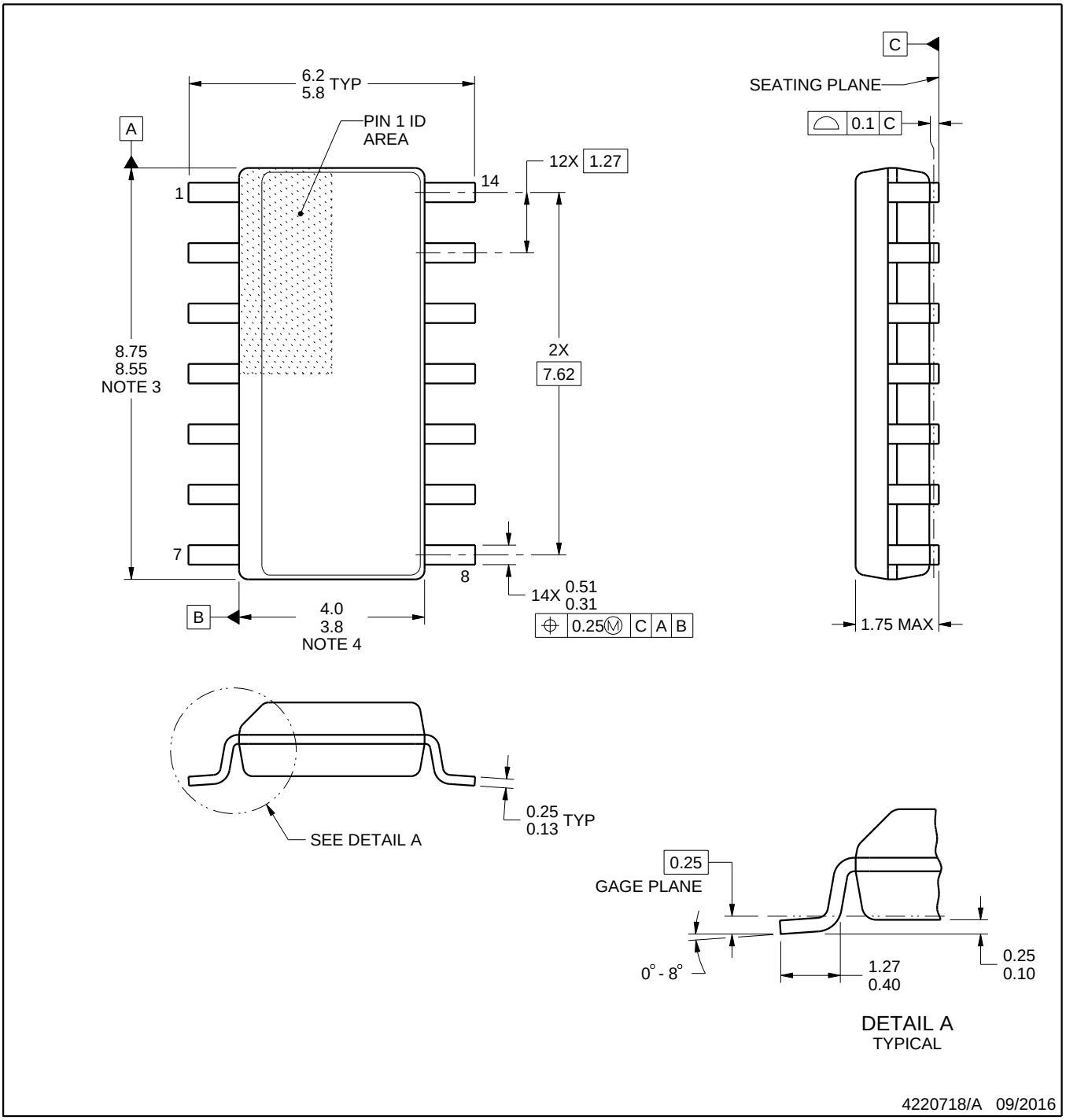


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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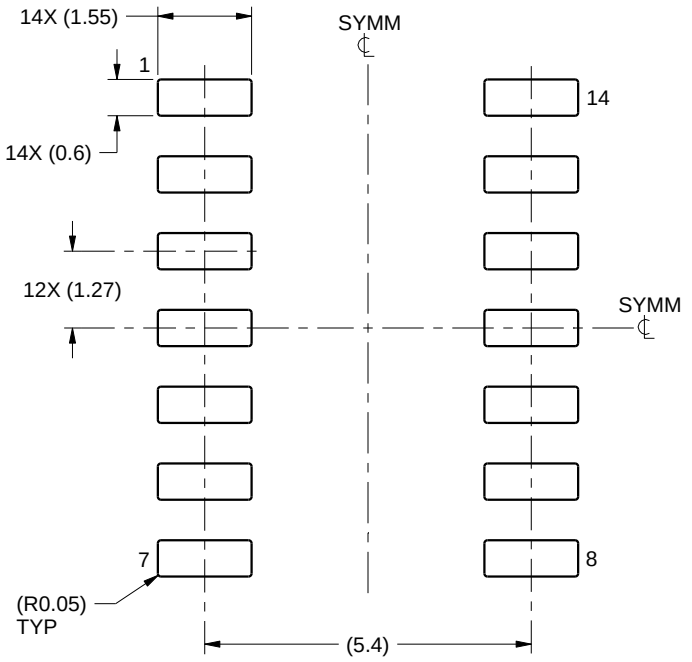
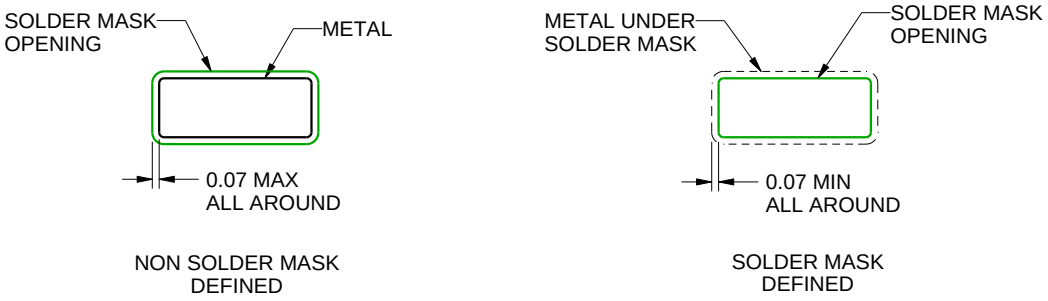
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

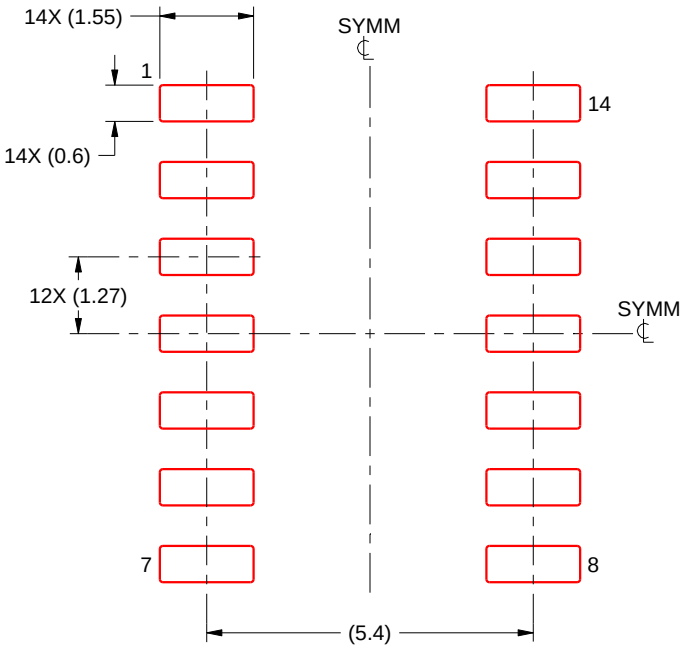
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

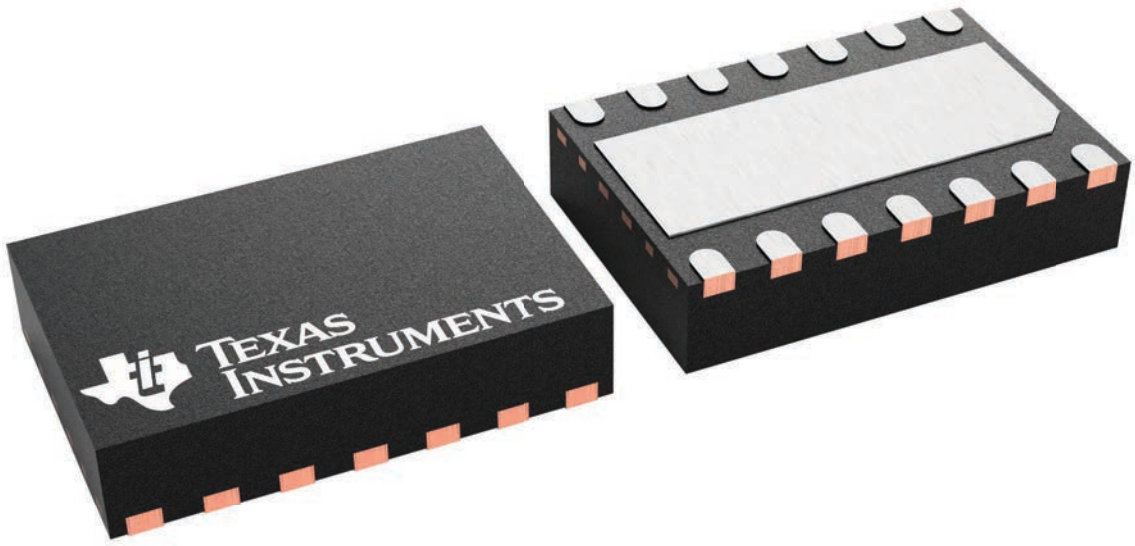
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



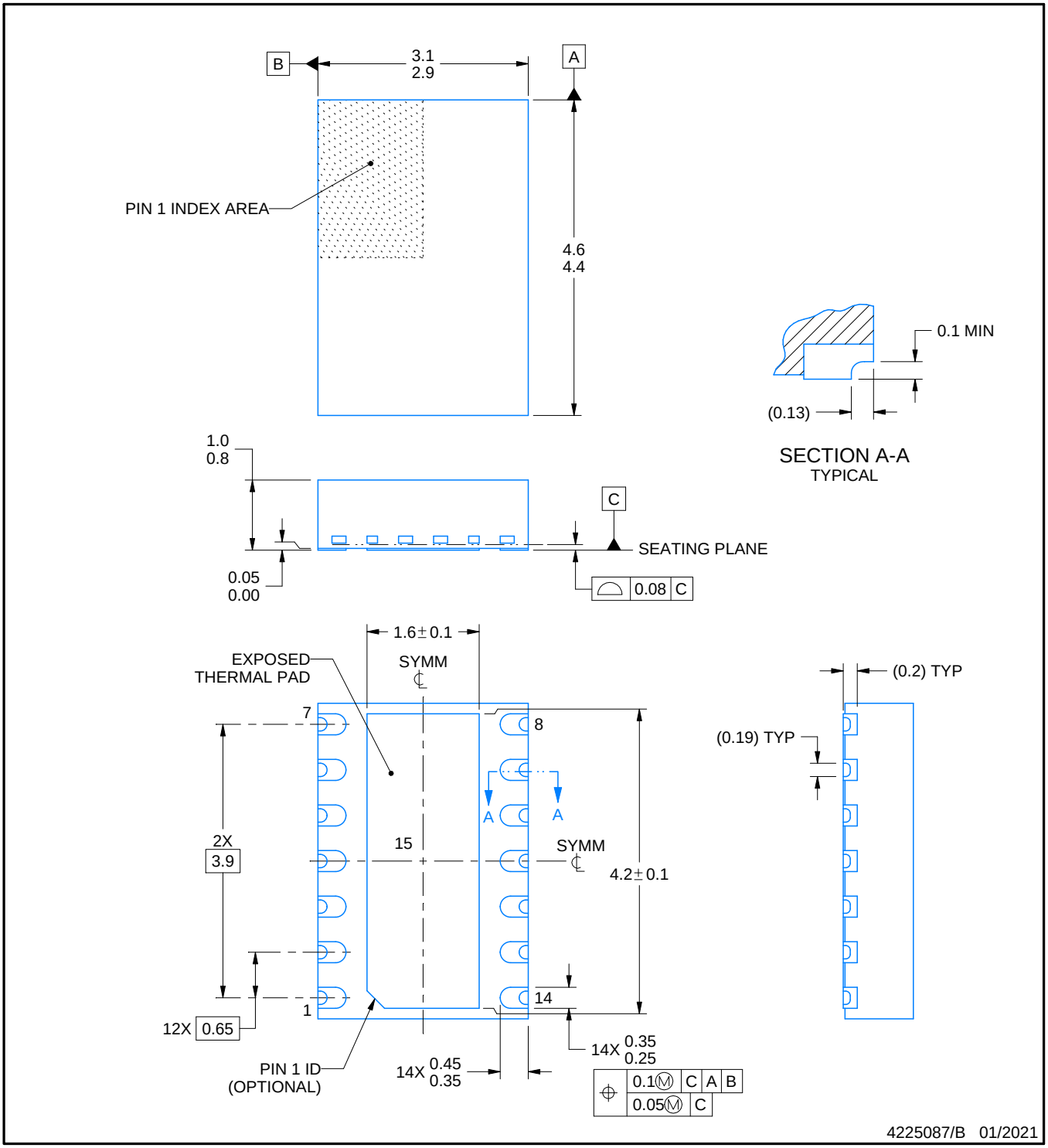
4225088/A

PACKAGE OUTLINE

DMT0014B

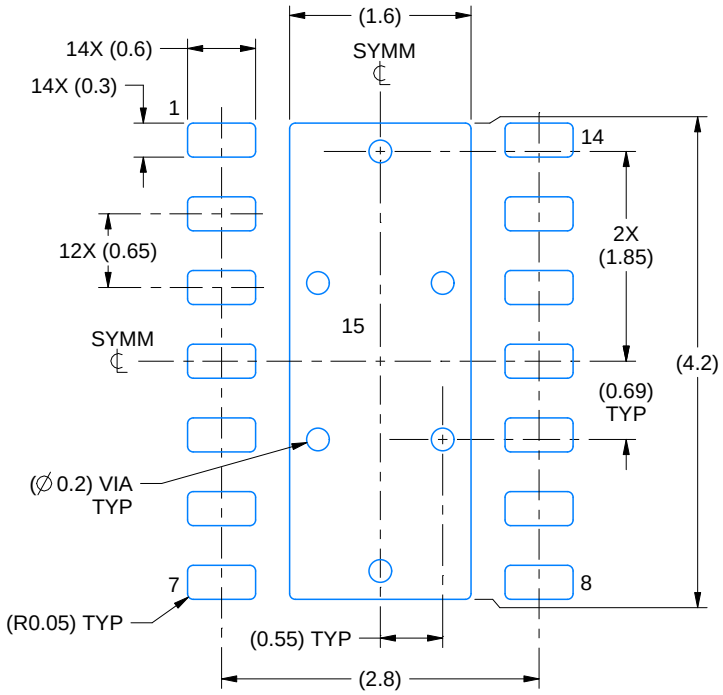
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

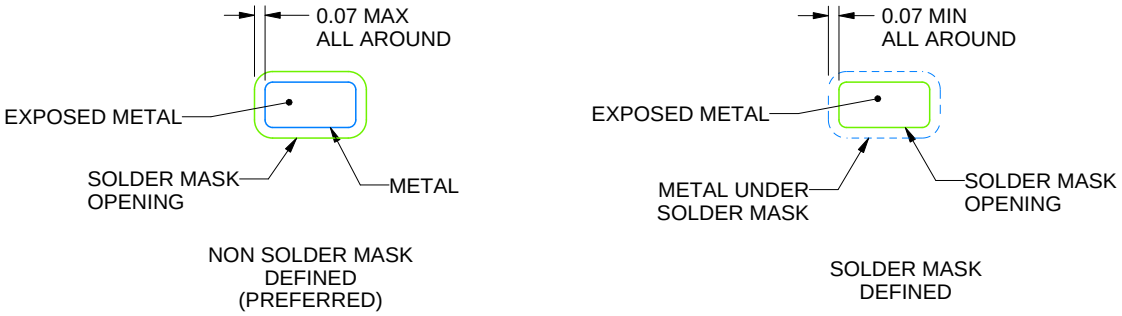


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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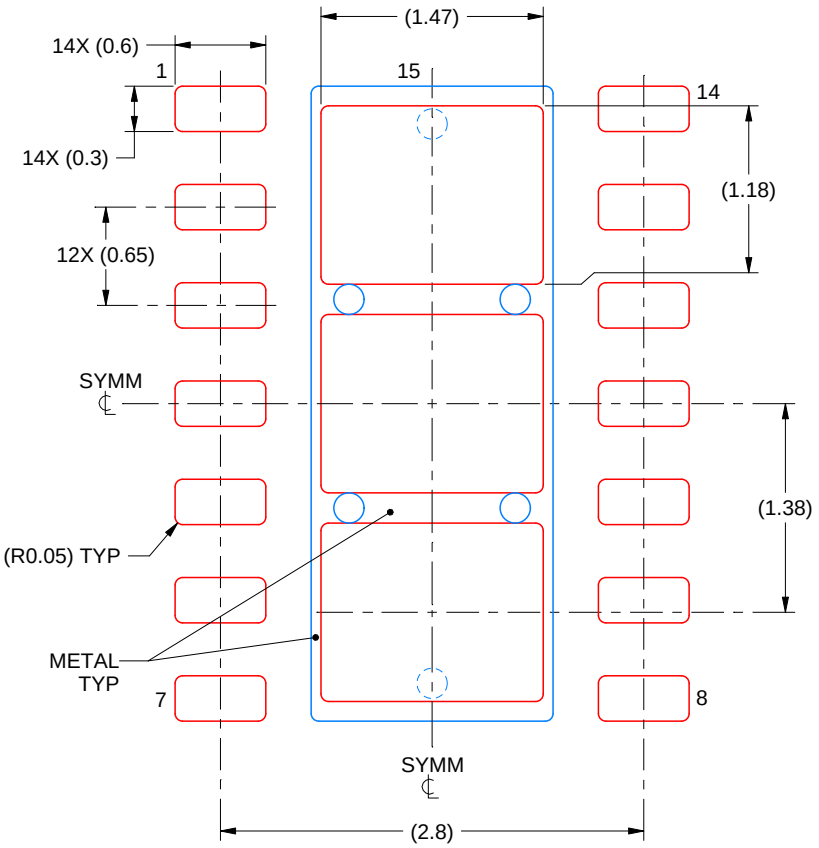
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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