TEXAS INSTRUMENTS
THS4561
JAJSIB3D – AUGUST 2017 – REVISED FEBRUARY 2021

THS4561 低消費電力、高電力範囲、60MHz、完全差動アンプ

1 特長

- 帯域幅:60MHz (G = 1V/V)
- スルーレート:230V/µs
- ゲイン帯域幅積:68MHz
- 電圧ノイズ:
  - 1/f 電圧ノイズ・コーナー:8Hz
  - 広帯域ノイズ (≥ 500Hz):4nV/√Hz
- 入力オフセット:±250µV 以下
  - ドリフト:±4µV/℃以下
- 電源動作範囲:2.85V～12.6V
- 消費電流:775µA
- 負のレール入力 (NRI)
- レール・ツー・レール出力 (RRO)
- 非常に小さい高調波歪み:
  - HD2:2V_{PP}、100kHz において –117dBc
  - HD3:2V_{PP}、100kHz において –124dBc
- 0.01% セトリング (2V ステップ):90ns

2 アプリケーション

- 16 ビットから 20 ビットまでの差動、SAR および ΔΣ ドライバ
- 差動アクティブ・フィルタ
- 高出力スイングの PCM オーディオ DAC 出力
- 超音波医療機器
- バッテリ・テスタ
- 電力分析
- THS4551 の低消費電力の代替品

3 概要

THS4561 完全差動アンプ (FDA) は、高精度アナログ / デジタル・コンバータ (ADC) に必要な、シングルエンド信号源から差動出力への簡単なインターフェイスとして機能します。THS4561 は、わずか 775µA の静止電流でありながら、8Hz の非常に低い 1/f 電圧ノイズ・コーナーと -130dB の小さな全高調波歪み (THD) を実現するように設計されているため、アンプと ADC の組み合わせによる最高水準の信号対雑音比 (SNR) とスプリアス・フリー・ダイナミック・レンジ (SFDR) が必要とされる、電力の制約が厳しいデータ・アクイジション (DAQ) システムに最適です。

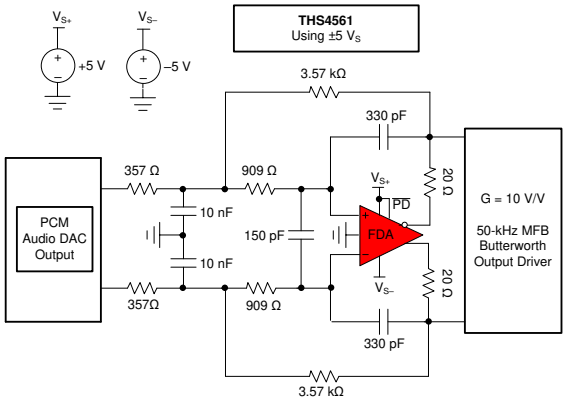
THS4561 は、DC 結合、グランド中心のソース信号と、単一電源の差動入力 ADC とを接続するために必要な負レール入力機能を備えています。DC 誤差とドリフトが小さいため、新しい高速高分解能の逐次比較型 (SAR) およびデルタ・シグマ (ΔΣ) ADC の入力要件をサポートできます。2.85V～12.6V の電源範囲に対応し、出力同相モード電圧を柔軟に設定でき、電源へのヘッドルームが小さくて済むため、幅広い ADC 入力および DAC 出力要件をサポートできます。

THS4561 デバイスは、–40℃～+125℃で動作が規定されています。

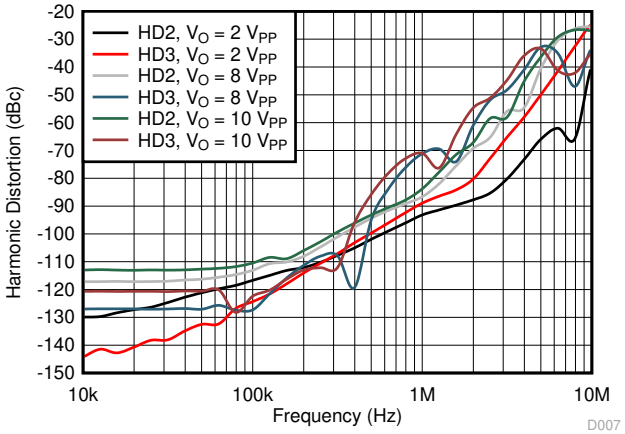
デバイス情報

部品番号	パッケージ(1)	本体サイズ (公称)
THS4561	VSSOP (8)	3.00mm × 3.00mm
	WQFN (10)	2.00mm × 2.00mm
	VQFN (16)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



50kHz の 2 次 MFB フィルタを使用する 10V/V ゲインの PCM オーディオ DAC 出力



高調波歪みと周波数との関係

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4 Revision History

Changes from Revision C (December 2020) to Revision D (February 2021) — **Page**

- Changed the status of the RGT package from *preview* to *production* ... 4

Changes from Revision B (August 2020) to Revision C (December 2020) — **Page**

- 「*特長*」セクションのスルーレートを 315V/µs から 230V/µs に変更 ... 1
- 「特長」セクションの「2 次 MFB フィルタを使用する 10V/V ゲインの PCM オーディオ DAC 出力」を更新 ... 1
- THS4561 デバイスの WQFN (10) パッケージをリリース ... 1
- Changed the status of the RUN package from *preview* to *production* ... 4
- Seperated slew rate specification into rising and falling specifications lines ... 5
- Changed the VOCM small-signal bandwidth test condition from *100 mV_{PP}* to *10 mV_{PP}* and the typical value from *23 MHz* to *22 MHz* ... 5
- Changed the VOCM large-signal bandwidth typical value from *10 MHz* to *1.9 MHz* ... 5
- Changed the maximum VOCM drift specification from *300 µV/°C* ... 5
- Updated the Common-Mode Voltage, Small-Signal and Large-Signal Response (VOCM Pin Driven) figure in the *Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 3-V to 12-V Supply Range* section ... 16
- Updated the MFB Filter Driving an ADC Application figure in the *Typical Application* section ... 33

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- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Added the *VQFN-10* and *VQFN-16* Package Outlines ... 37

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- デバイスのステータスを事前情報から量産データに変更 ... 1

5 Device Comparison Table

DEVICE	BW, G = 1 (MHz)	I_Q, 5 V (mA)	INPUT NOISE (nV/√Hz)	THD (dBc) 2 V_{PP} AT 10 kHz	RAIL-TO-RAIL	DUAL VERSIONS
THS4561	60	0.78	4	–130	Negative in and out	—
THS4551	150	1.37	3.3	–138	Negative in and out	THS4552
THS4521	145	1.14	5.6	–120	Negative in and out	THS4522
THS4531A	36	0.25	10	–118	Negative in and out	THS4532
THS4541	620	10.1	2.2	–140	Negative in and out	—

6 Pin Configuration and Functions

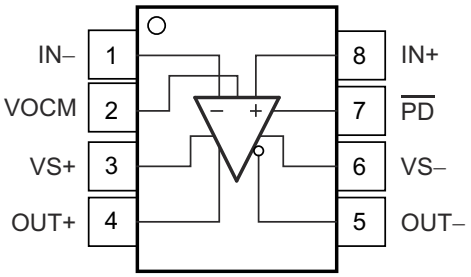


図 6-1. DGK Package 8-Pin VSSOP Top View

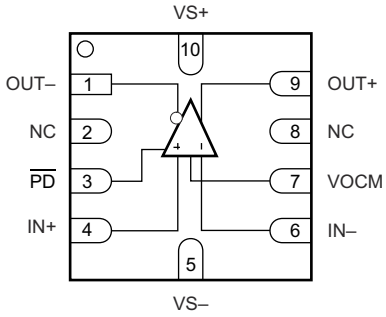


図 6-2. RUN Package 10-Pin WQFN Top View

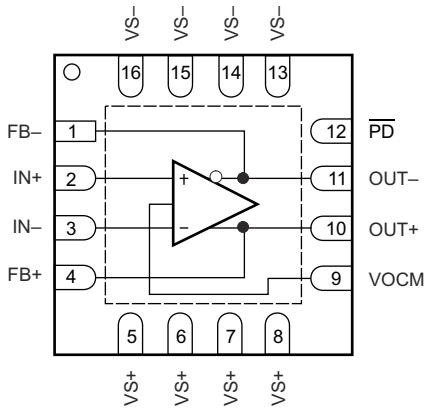


図 6-3. RGT Package 16-Pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN				TYPE[2]	DESCRIPTION
NAME	DGK	RUN	RGT[1]		
FB–	—	—	1	O	Inverting (negative) output feedback
FB+	—	—	4	O	Noninverting (positive) output feedback
IN–	1	6	3	I	Inverting (negative) amplifier input
IN+	8	4	2	I	Noninverting (positive) amplifier input
NC	—	2, 8	—	—	No internal connection
OUT–	5	1	11	O	Inverting (negative) amplifier output
OUT+	4	9	10	O	Noninverting (positive) amplifier output
$\overline{PD}$	7	3	12	I	Power down. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VOCM	2	7	9	I	Common-mode voltage input
VS–	6	5	13, 14, 15, 16	P	Negative power-supply input
VS+	3	10	5, 6, 7, 8	P	Positive power-supply input

(1) Solder the exposed RGT package thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.
(2) I = input, O = output, P = power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Total supply voltage, $V_S = (V_{S+} – V_{S–})$		13.5	V
	Supply turn-on/off dV/dT(2)		±0.35	V/µs
	Input, output, power down and common-mode pin voltage range	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Differential input voltage		±1	V
Current	Continuous input current		±10	mA
	Continuous output current(3)		±20	mA
Temperature	Junction temperature, T_J		150	°C
	Operating free-air temperature, T_A	–40	125	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These stress-only ratings do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Staying below this specification ensures that the edge-triggered ESD absorption devices across the supply pins remains off.
(3) Long-term continuous output current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	2.85		12.6	V
T_A	Operating free-air temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS4561			UNIT
		DGK (VSSOP)	RUN (WQFN)	RGT (VQFN)	
		8 PINS	10 PINS	16 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	183.1	134.6	55.9	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	70.3	83.6	64.5	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	104.9	67.7	30.5	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	10.8	7.2	3.5	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	103.2	67.5	30.5	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	15.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: $V_{S+} – V_{S–}$ = 5 V to 12 V

at T_A ≈ 25°C, VOCM[1] = midsupply, differential output (V_O) = $V_{OUT+} – V_{OUT–}$ = 2 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential closed-loop gain (G) = 1 V/V, single-ended input (SE-in), differential output (diff-out), and input and output referenced to midsupply for AC-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_S = 5 V, V_O = 200 mV_{PP}, 2-dB peaking			60		MHz
		V_S = 5 V, V_O = 200 mV_{PP}	G = 2 V/V		45		
			G = 5 V/V		12.5		
			G = 10 V/V		6.3		
GBWP	Gain-bandwidth product	V_O = 200 mV_{PP}, G = 20 V/V, R_F = 10 kΩ			68		MHz
LSBW	Large-signal bandwidth	V_O = 4 V_{PP}			20		MHz
	Bandwidth for 0.1-dB flatness				5		MHz
SR	Slew rate (20% – 80%)	V_S = 5 V, V_O = 2-V step	Rising		325		V/µs
			Falling		230		V/µs
	Overshoot and undershoot	V_O = 2-V step, input t_r = 10 ns	V_S = 12 V		5%		
			V_S = 5 V		11%		
	0.1% settling time	V_O = 2-V step, input t_r = 10 ns			40		ns
	0.01% settling time	V_O = 2-V step, input t_r = 10 ns			90		ns
	Rise and fall time (10% – 90%)	V_O = 100-mV step, input t_r = 2 ns			5.7		ns
HD2	Second-order harmonic distortion	V_S = 5 V, f = 100 kHz	V_o = 2 V_{PP}		–117		dBc
			V_o = 8 V_{PP}		–110		
HD3	Third-order harmonic distortion	V_S = 5 V, f = 100 kHz	V_o = 2 V_{PP}		–124		
			V_o = 8 V_{PP}		–106		
e_n	Input differential voltage noise	f ≥ 500 Hz			4		nV/√Hz
		1/f corner			8		Hz
i_n	Input current noise, each input	f ≥ 50 kHz			0.35		pA/√Hz
	Overdrive recovery time	V_S = 5 V, G = 2 V/V, 2x output overdrive, dc-coupled			210		ns
Z_{OUT}	Closed-loop output impedance	f = 100 kHz (differential)			0.06		Ω
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_o = ±2 V		104	115		dB
V_{OS}	Input offset voltage	T_A = 25°C		–250	±50	250	µV
	Input offset voltage drift	T_A = 0°C to 85°C, T_A = –40°C to 125°C		–4	±0.5	4	µV/°C
I_{B+}, $I_{B–}$	Input bias current[3]	T_A = 25°C			370	600	nA
	Input bias current drift	T_A = –40°C to 125°C			4.1	8	nA/°C
I_{OS}	Input offset current[4]	T_A = 25°C		–20	±2	20	nA
	Input offset current drift	T_A = –40°C to 125°C		–200	±40	200	pA/°C
INPUT							
V_{ICML}	Common-mode input low	T_A = –40°C to 125°C, 3-dB A_{OL} degradation from midsupply VOCM A_{OL}			$V_{S–}$ – 0.1	$V_{S–}$	V
V_{ICMH}	Common-mode input high	3-dB A_{OL} degradation from midsupply VOCM A_{OL}	T_A = 25°C	V_{S+} – 1.2	V_{S+} – 1.1		V
			T_A = –40°C to 125°C	V_{S+} – 1.35	V_{S+} – 1.2		
CMRR	Common-mode rejection ratio	Midsupply inputs		95	110		dB
		Midsupply inputs, T_A = –40°C to 125°C			108		
	Differential input impedance	Inputs at midsupply			150 || 2.4		kΩ || pF

7.5 Electrical Characteristics: $V_{S+} – V_{S–}$ = 5 V to 12 V (continued)

at T_A ≈ 25°C, VOCM[1] = midsupply, differential output (V_O) = $V_{OUT+} – V_{OUT–}$ = 2 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential closed-loop gain (G) = 1 V/V, single-ended input (SE-in), differential output (diff-out), and input and output referenced to midsupply for AC-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Output voltage range low	V_S = 5 V		$V_{S–}$ + 0.13	$V_{S–}$ + 0.25	V
		V_S = 5 V, T_A = –40°C to 125°C		$V_{S–}$ + 0.15	$V_{S–}$ + 0.3	
		V_S = 5 V, R_L = 10 kΩ		$V_{S–}$ + 0.07		
		V_S = 12 V		$V_{S–}$ + 0.26	$V_{S–}$ + 0.4	
	Output voltage range high	V_S = 5 V	V_{S+} – 0.25	V_{S+} – 0.16		V
		V_S = 5 V, T_A = –40°C to 125°C	V_{S+} – 0.3	V_{S+} – 0.18		
		V_S = 5 V, R_L = 10 kΩ		V_{S+} – 0.09		
		V_S = 12 V	V_{S+} – 0.35	V_{S+} – 0.2		
	Continuous output current	V_O = ±3.6 V, V_{OCM} offset < 15 mV	±27	±31		mA
		T_A = –40°C to +125°C, V_O = ±2.25 V, V_{OCM} offset < 15 mV	±17			
	Linear output current	V_S = 5 V, V_O = ±2.7 V,, A_{OL} > 80 dB	±20	±22		mA
		V_S = 12 V, V_O = ±4.6 V, A_{OL} > 80 dB	±22	±27		
		V_S = 12 V, T_A = –40°C to +125°C, V_O = ±3.1 V, A_{OL} > 80 dB	±15			
OUTPUT COMMON-MODE VOLTAGE (VOCM) CONTROL[1]						
	Small-signal bandwidth	VOCM = 10 mV_{PP}		22		MHz
	Large-signal bandwidth	VOCM = 1 V_{PP}		1.9		MHz
	Slew rate[2] (20% – 80%)	VOCM = 0.5-V step		4		V/µs
	DC output balance	VOCM fixed midsupply, V_{OCM}/V_O (V_O = ±1 V)		86		dB
	Output balance	VOCM fixed midsupply, V_{OCM}/V_O (–3-dB from dc)		800		Hz
	Gain	VOCM = 0 V	0.997	1	1.003	V/V
	Input bias current		–0.5	–0.1	0.5	µA
	+PSR to V_{OCM}	VOCM = midsupply	72	78		dB
	–PSR to V_{OCM}	VOCM = midsupply	70	76		dB
	Input impedance			200 || 1.5		kΩ || pF
	Default VOCM offset	Relative to midsupply, VOCM pin floating	–40	8	40	mV
	Default VOCM offset voltage drift	T_A = –40°C to 125°C	120	200	600	µV/°C
	V_{OCM} offset voltage	VOCM driven to midsupply	–3.5	0.25	3.5	mV
	V_{OCM} offset voltage drift	T_A = –40°C to 125°C	–15	3	15	µV/°C
	VOCM range low	T_A = 25°C, < ±4-mV shift from midsupply offset		$V_{S–}$ + 0.45	$V_{S–}$ + 0.5	V
		T_A = –40°C to 125°C, < ±4-mV shift from midsupply offset			$V_{S–}$ + 0.6	
	VOCM range high	T_A = 25°C, < ±4-mV shift from midsupply offset	V_{S+} – 1.2	V_{S+} – 1.1		V
		T_A = –40°C to 125°C, < ±5-mV shift from midsupply offset	V_{S+} – 1.3			

7.5 Electrical Characteristics: V_{S+} – $V_{S–}$ = 5 V to 12 V (continued)

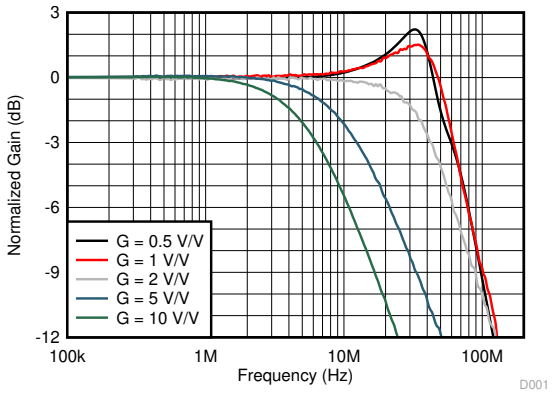
at T_A ≈ 25°C, VOCM(1) = midsupply, differential output (V_O) = V_{OUT+} – $V_{OUT–}$ = 2 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential closed-loop gain (G) = 1 V/V, single-ended input (SE-in), differential output (diff-out), and input and output referenced to midsupply for AC-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
	Specified operating voltage		2.85		12.6	V
I_Q	Quiescent current	V_S = 2.85 V, no load, T_A = 25°C	710	760	810	µA
		V_S = 5 V, no load, T_A = 25°C	725	775	825	
		V_S = 5 V, no load, T_A = –40°C to 125°C	700		900	
		V_S = 12 V, no load, T_A = 25°C	770	825	880	
		V_S = 12 V, no load, T_A = –40°C to 125°C	740		1000	
	Quiescent current drift	No load, T_A = –40°C to 125°C		0.7	1.3	µA/°C
PSRR	Power-supply rejection ratio	Either supply to input V_{OS}	92	110		dB
POWER DOWN						
V_{EN}	Enable voltage threshold	$\overline{PD}$ = V_{EN}, guaranteed *on* above		V_{S+} – 1.2	V_{S+} – 0.5	V
V_{DIS}	Disable voltage threshold	$\overline{PD}$ = V_{DIS}, guaranteed *off* below		V_{S+} – 1.7	V_{S+} – 1.8	V
	$\overline{PD}$ pin bias current	$\overline{PD}$ = V_{S+} – 0.5 V (amplifier enabled)		1.2	3.5	µA
	$\overline{PD}$ pin bias current	$\overline{PD}$ = $V_{S–}$ (amplifier disabled)	–3	–1.9		µA
	Peak $\overline{PD}$ pull-down bias current	Switch amplifier *on* to *off*		175		µA
	Power-down quiescent current	No load	3	15	40	µA
	Turnon time delay	Time from $\overline{PD}$ = high to V_O = 90% of final value		600		ns
	Turnoff time delay	Time from $\overline{PD}$ = low to V_O = 10% of original value		1.5		µs

(1) VOCM refers to the voltage at VOCM pin. V_{OCM} = [(V_{OUT+} + $V_{OUT–}$)/2] refers to the average output voltage.
(2) Average of the rising and falling slew rate.
(3) Current out of the node is considered positive.
(4) I_{OS} = I_{B+} – $I_{B–}$.

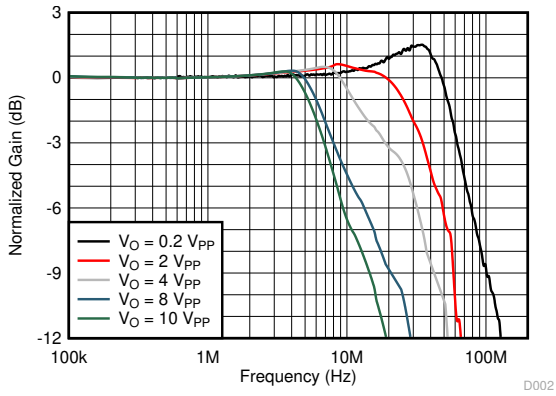
7.6 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 12$ V

at $T_A \approx 25°C$, VOCM pin = midsupply, R_F = 1.5 kΩ, R_L = 1 kΩ, V_O = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input (SE-in), differential output (diff-out), and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.



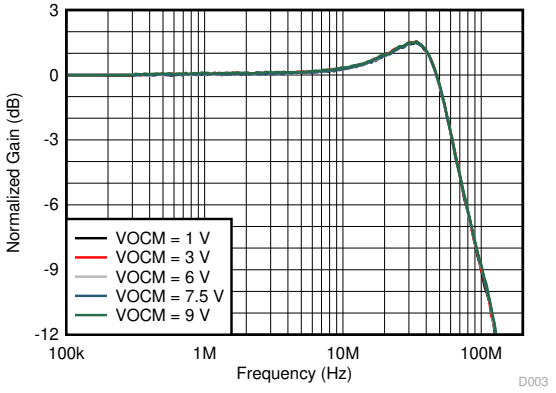
V_O = 200 mV_{PP}, see 図 8-1 and 表 10-1 for resistor values

図 7-1. Small-Signal Frequency Response vs Gain



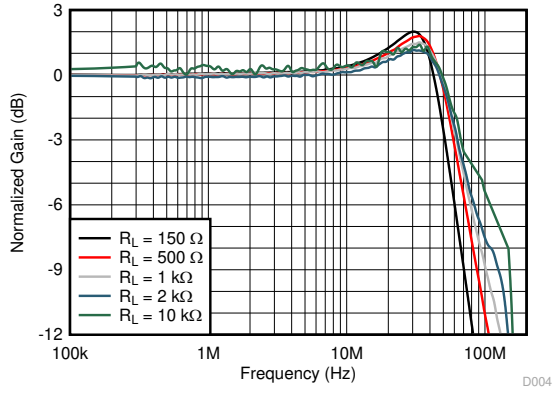
See 図 8-1

図 7-2. Frequency Response vs V_O



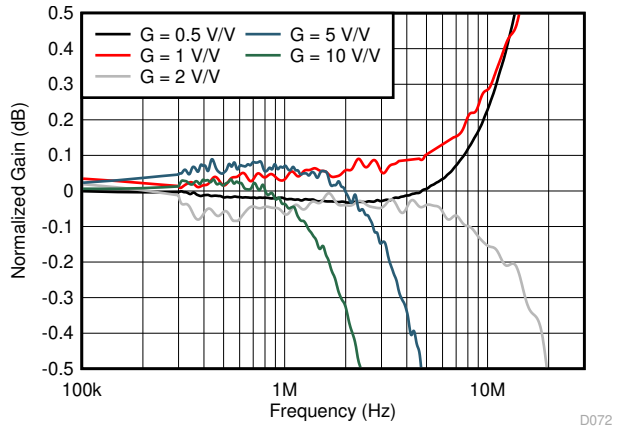
V_O = 200 mV_{PP} , see 図 8-1 with VOCM adjusted

図 7-3. Small-Signal Frequency Response vs VOCM



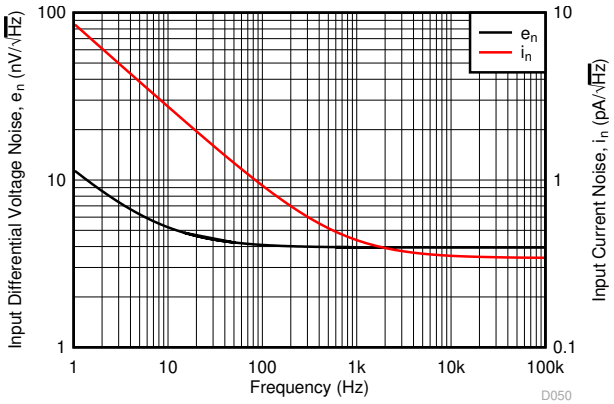
V_O = 200 mV_{PP}, see 図 8-1 with load resistance (R_L) adjusted

図 7-4. Small-Signal Frequency Response vs R_L



V_O = 200 mV_{PP}

図 7-5. Gain Flatness vs Frequency



1/f corners: e_n = 8 Hz, i_n = 700 Hz

図 7-6. Input Noise Density vs Frequency

7.6 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 12$ V (continued)

at $T_A \approx 25°C$, VOCM pin = midsupply, $R_F = 1.5$ kΩ, $R_L = 1$ kΩ, $V_O = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input (SE-in), differential output (diff-out), and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.

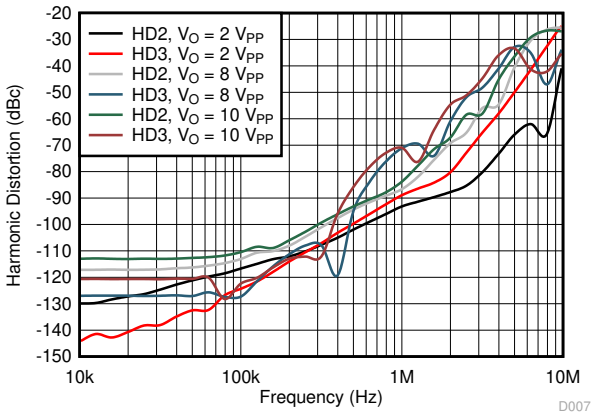


図 7-7. Harmonic Distortion vs Frequency

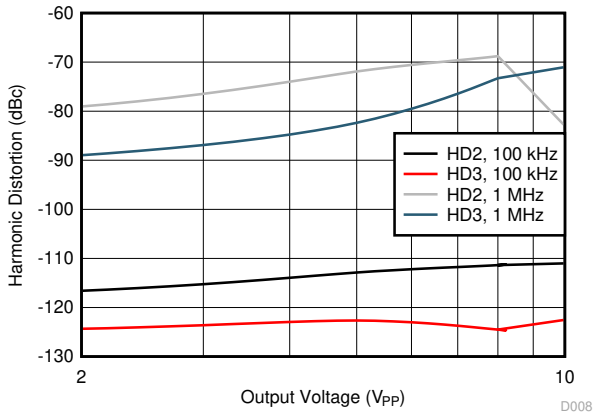
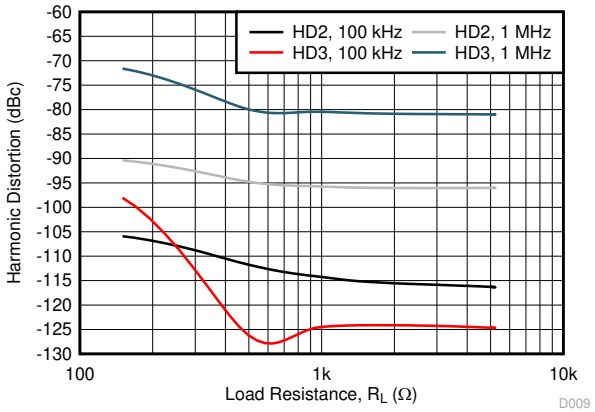
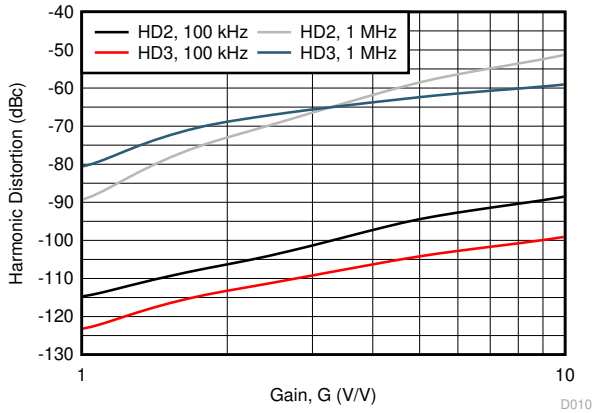


図 7-8. Harmonic Distortion vs V_O



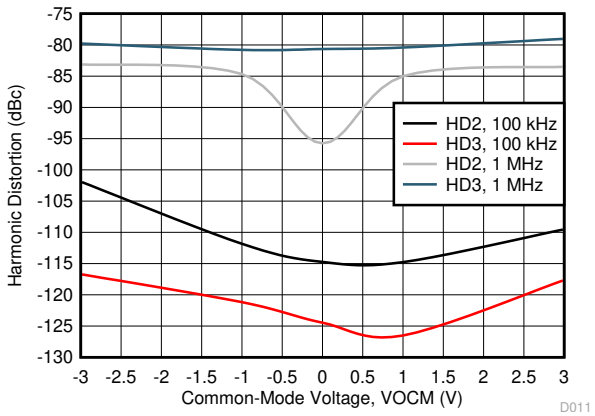
$V_O = 5$ V_{PP} with R_L adjusted

図 7-9. Harmonic Distortion vs R_L



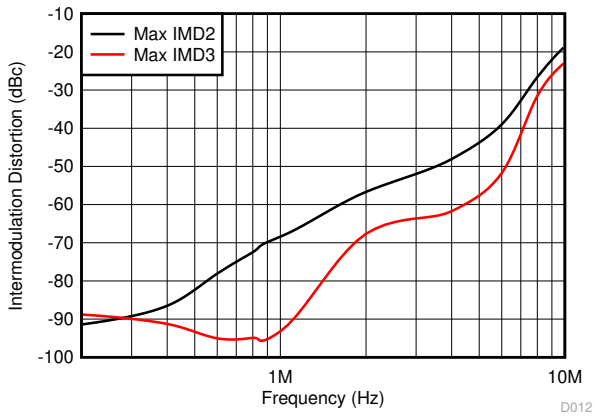
$V_O = 5$ V_{PP}, see 表 10-1 for gain setting

図 7-10. Harmonic Distortion vs Gain



$V_O = 5$ V_{PP} with VOCM adjusted

図 7-11. Harmonic Distortion vs VOCM

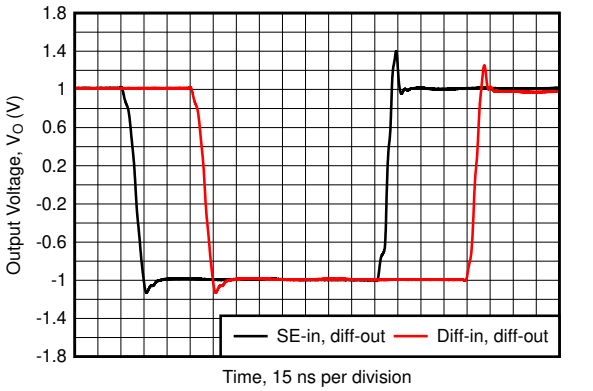


$V_O = 2$ V_{PP} per tone, ±50-kHz tone spacing

図 7-12. Intermodulation Distortion (IMD2 and IMD3) vs Frequency

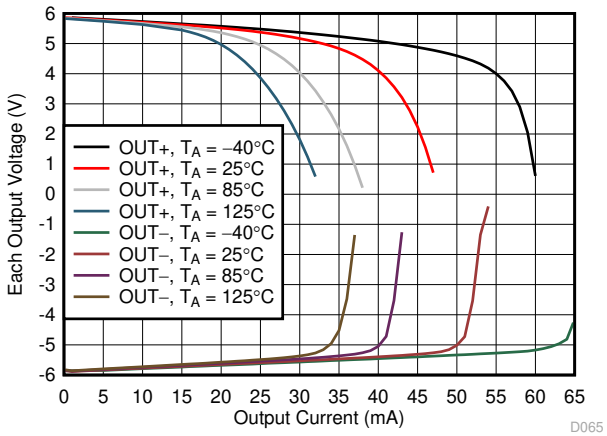
7.6 Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 12 V (continued)

at T_A ≈ 25°C, VOCM pin = midsupply, R_F = 1.5 kΩ, R_L = 1 kΩ, V_O = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input (SE-in), differential output (diff-out), and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.



V_O = 2-V step,
SE-in, diff-out: rising SR = 350 V/µs, falling SR = 200 V/µs,
diff-in, diff-out: rising SR = 285 V/µs, falling SR = 285 V/µs

図 7-13. Large-Signal Step Response

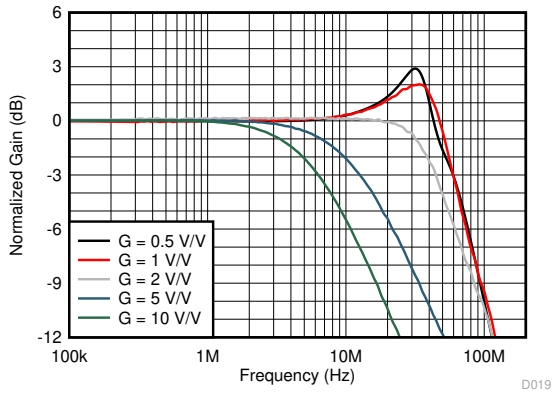


V_S = 12 V, VOCM at midsupply, average of 30 units

図 7-14. ±Maximum Output Voltage vs Output Current and Temperature

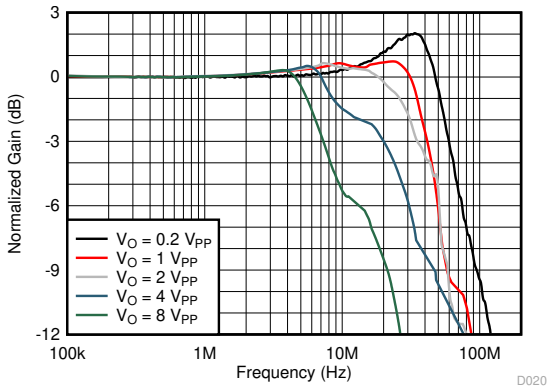
7.7 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1.5$ kΩ, $R_L = 1$ kΩ, $V_O = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input (SE-in), differential output (diff-out), and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.



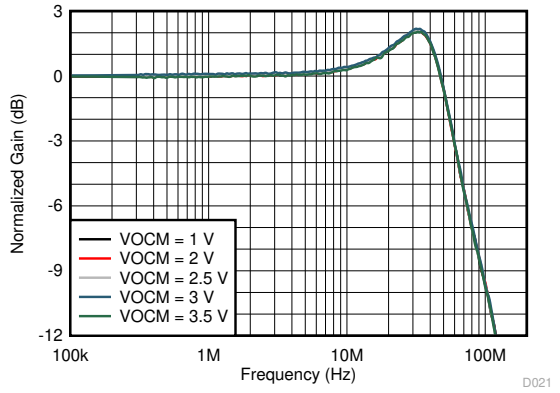
$V_O = 200$ mV_{PP}, see 図 8-1 and 表 10-1 for resistor values

図 7-15. Small-Signal Frequency Response vs Gain



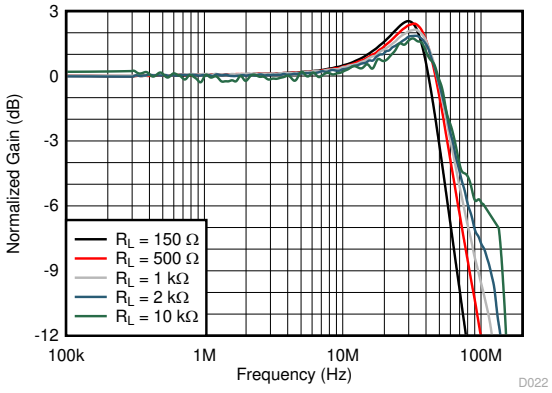
See 図 8-1

図 7-16. Frequency Response vs V_O



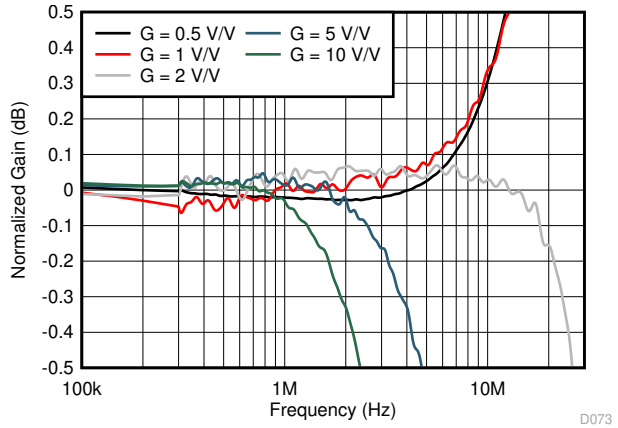
$V_O = 200$ mV_{PP}, see 図 8-1 with VOCM adjusted

図 7-17. Small-Signal Frequency Response vs VOCM



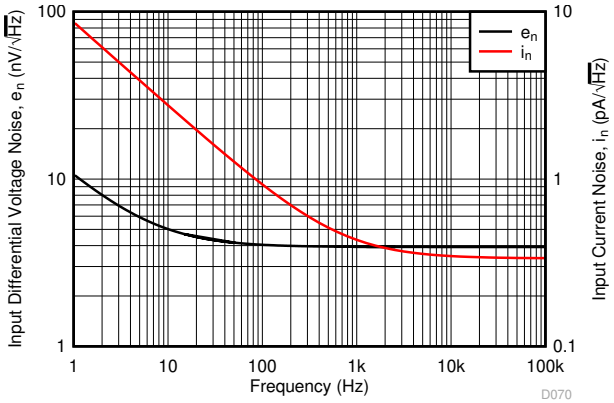
$V_O = 200$ mV_{PP}, see 図 8-1 with R_L adjusted

図 7-18. Small-Signal Frequency Response vs R_L



$V_O = 200$ mV_{PP}

図 7-19. Gain Flatness vs Frequency



1/f corners: $e_n = 8$ Hz, $i_n = 700$ Hz

図 7-20. Input Noise Density vs Frequency

7.7 Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 5 V (continued)

at T_A ≈ 25°C, VOCM pin = open, R_F = 1.5 kΩ, R_L = 1 kΩ, V_O = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input (SE-in), differential output (diff-out), and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.

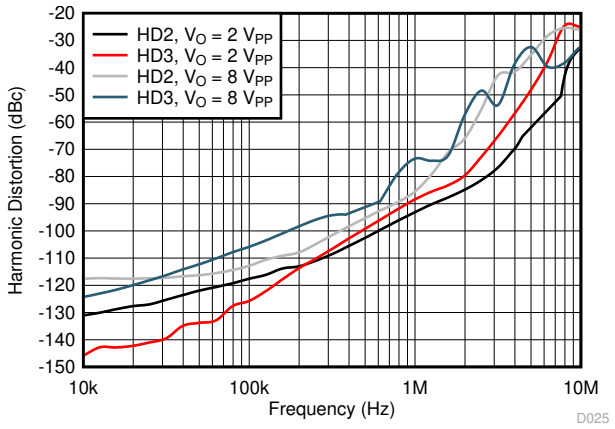


図 7-21. Harmonic Distortion vs Frequency

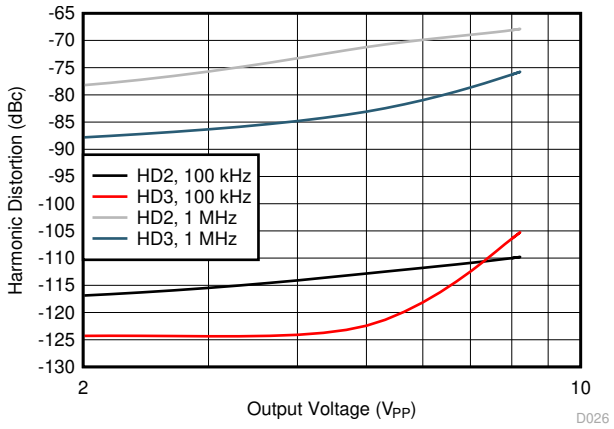
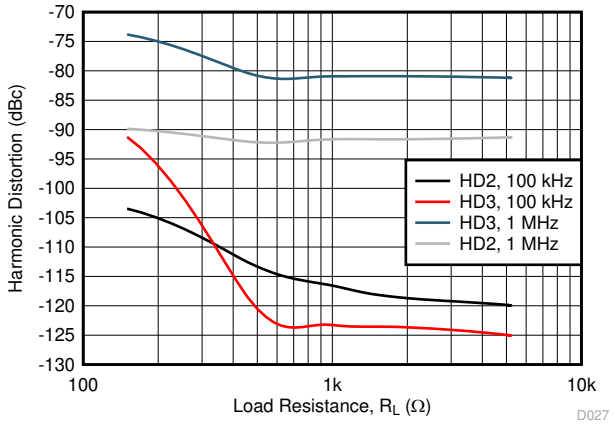
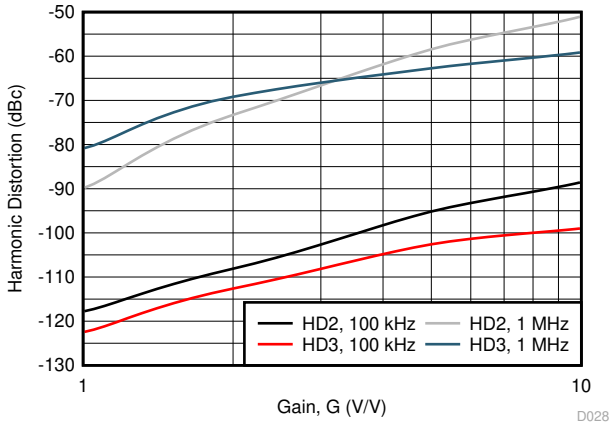


図 7-22. Harmonic Distortion vs V_O



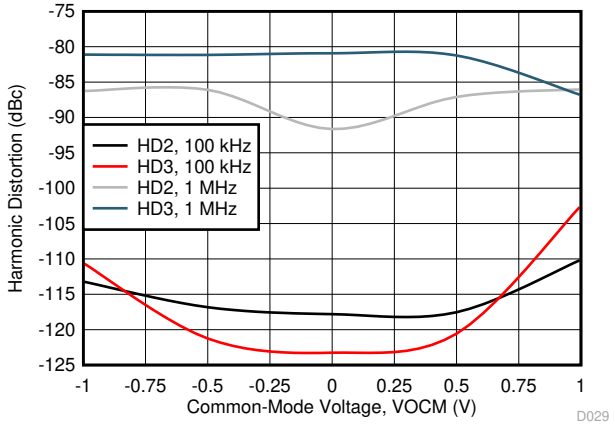
V_O = 5 V_{PP} with R_L adjusted

図 7-23. Harmonic Distortion vs R_L



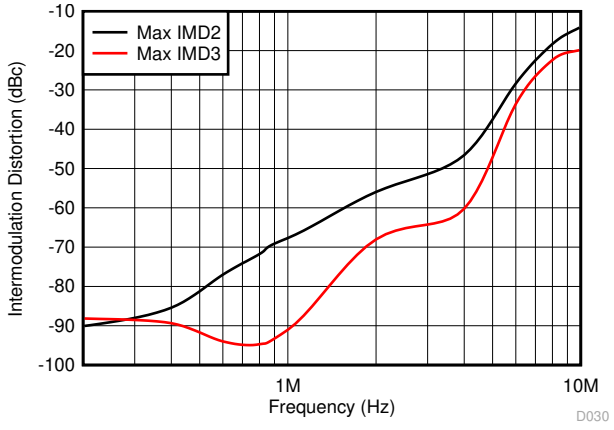
V_O = 5 V_{PP}, see 表 10-1 for gain setting

図 7-24. Harmonic Distortion vs Gain



V_O = 5 V_{PP} with VOCM adjusted

図 7-25. Harmonic Distortion vs VOCM

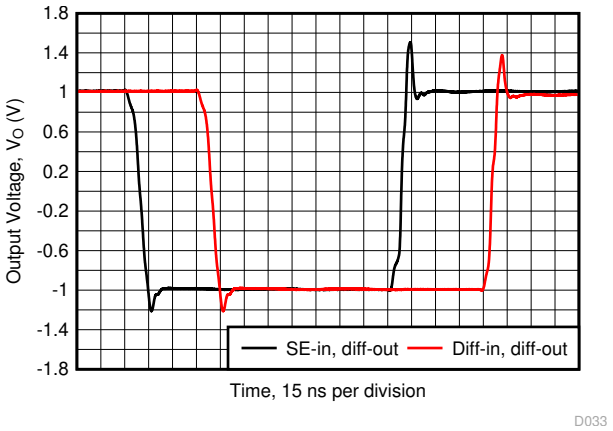


V_O = 2 V_{PP} per tone, ±50-kHz tone spacing

図 7-26. Intermodulation Distortion (IMD2 and IMD3) vs Frequency

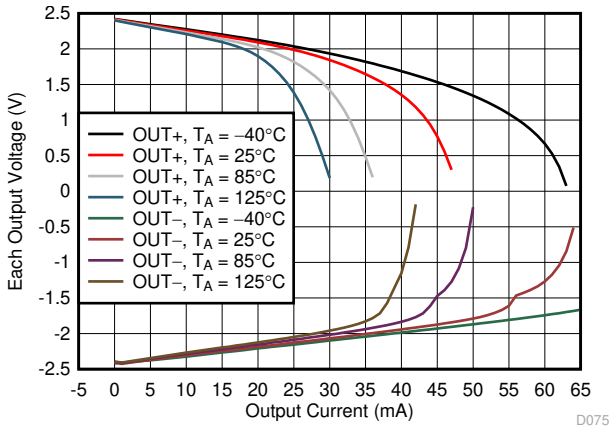
7.7 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V (continued)

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1.5$ kΩ, $R_L = 1$ kΩ, $V_O = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input (SE-in), differential output (diff-out), and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.



V_O = 2-V step,
SE-in, diff-out: rising SR = 325 V/µs, falling SR = 230 V/µs,
diff-in, diff-out: rising SR = 305 V/µs, falling SR = 310 V/µs

図 7-27. Large-Signal Step Response

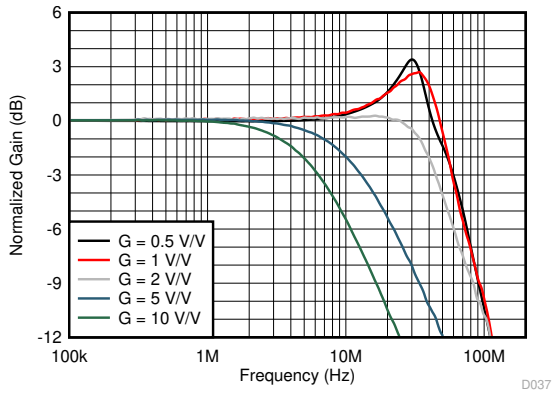


V_S = 5 V, VOCM at midsupply, average of 30 units

図 7-28. ±Maximum Output Voltage vs Output Current and Temperature

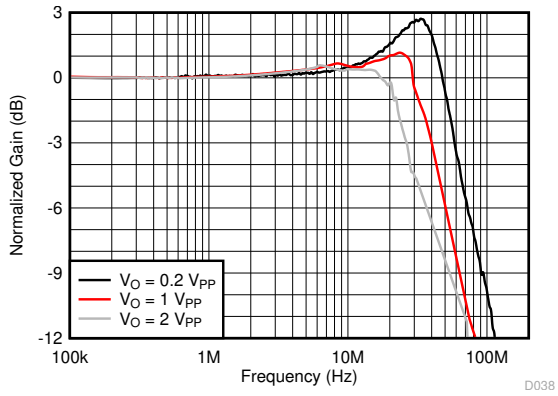
7.8 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 3$ V

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1.5$ kΩ, $R_L = 1$ kΩ, $V_O = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input (SE-in), differential output (diff-out), and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.



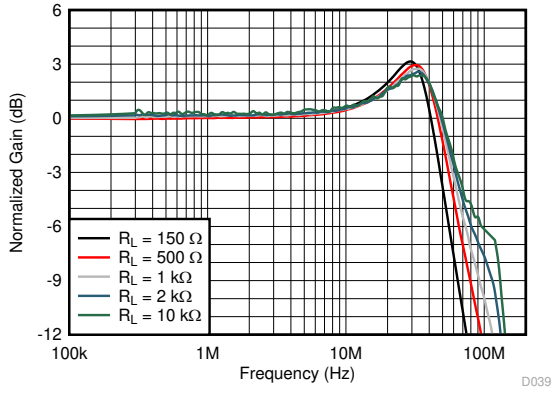
$V_O = 200$ mV_{PP}, see 図 8-1 and 表 10-1 for resistor values

図 7-29. Small-Signal Frequency Response vs Gain



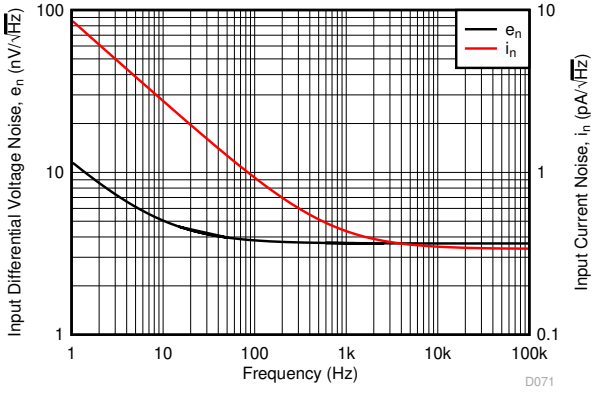
See 図 8-1

図 7-30. Frequency Response vs V_O



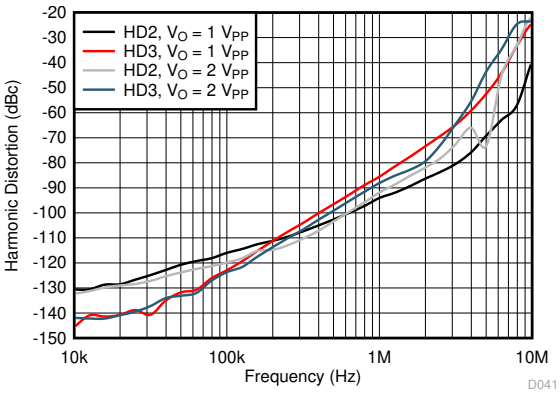
$V_O = 200$ mV_{PP}, see 図 8-1 with R_L adjusted

図 7-31. Small-Signal Frequency Response vs R_L



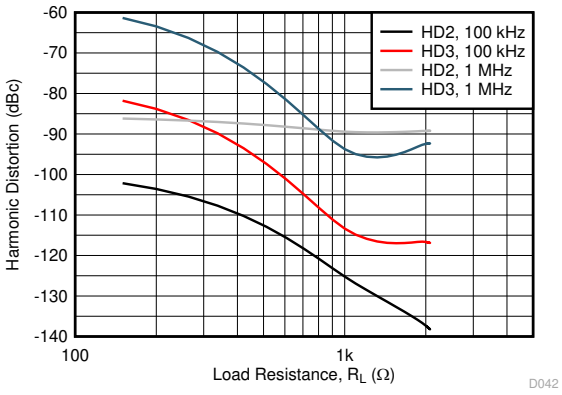
1/f corners: $e_n = 9$ Hz, $i_n = 700$ Hz

図 7-32. Input Noise Density vs Frequency



G = 1 V/V

図 7-33. Harmonic Distortion vs Frequency

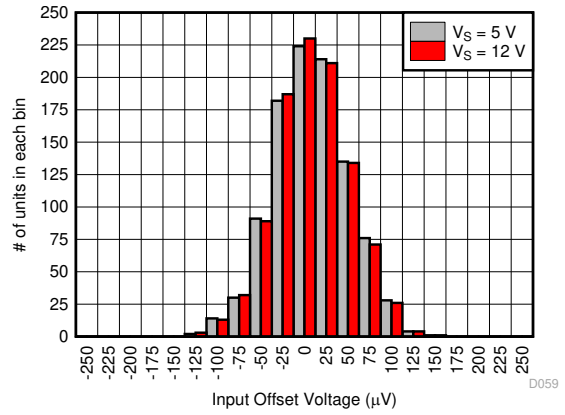


G = 1 V/V, $V_O = 4$ V_{PP}, with R_L adjusted

図 7-34. Harmonic Distortion vs R_L

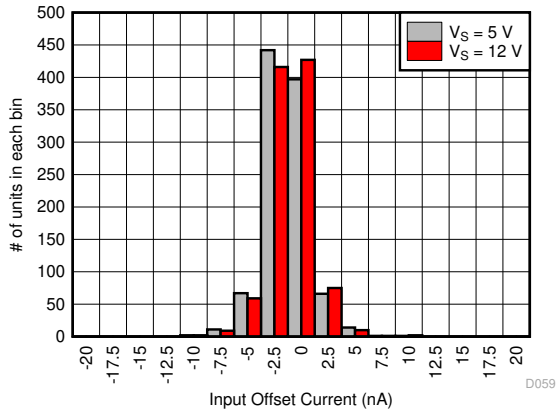
7.9 Typical Characteristics: $(V_{S+}) – (V_{S–})$ = 3-V to 12-V Supply Range

at $T_A \approx 25°C$, VOCM pin = open, R_F = 1.5 kΩ, R_L = 1 kΩ, V_O = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.



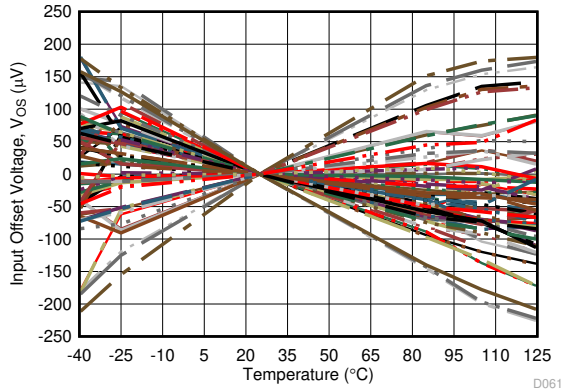
1000 DGK units at each V_S

図 7-35. Input Offset Voltage (V_{OS})



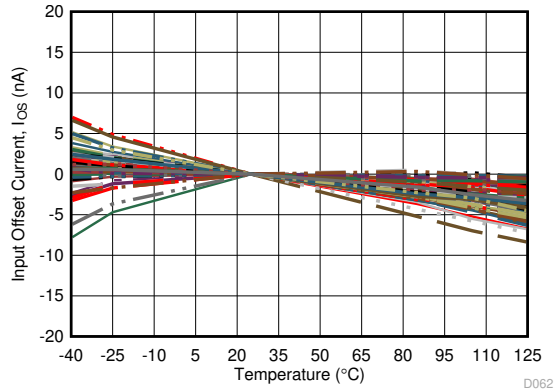
1000 DGK units at each V_S

図 7-36. Input Offset Current (I_{OS})



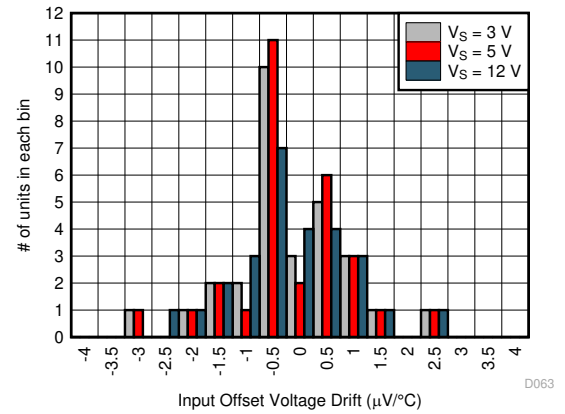
V_S = 12 V, 5 V, and 3 V,
delta from 25°C V_{OS}, 30 DGK units for each V_S

図 7-37. Input Offset Voltage vs Temperature



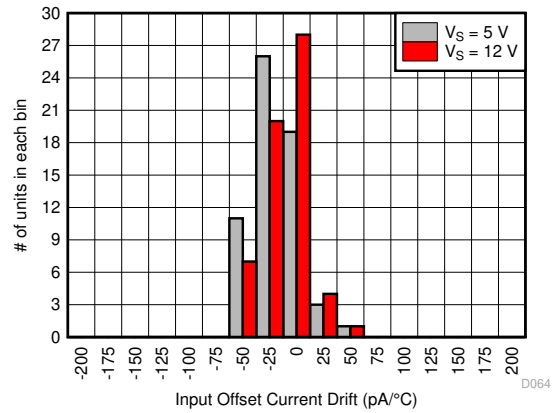
V_S = 12 V and 5 V,
delta from 25°C I_{OS}, 50 DGK units for each V_S

図 7-38. Input Offset Current vs Temperature



–40°C to +125°C endpoint drift, 30 DGK units for each V_S

図 7-39. Input Offset Voltage Drift Histogram

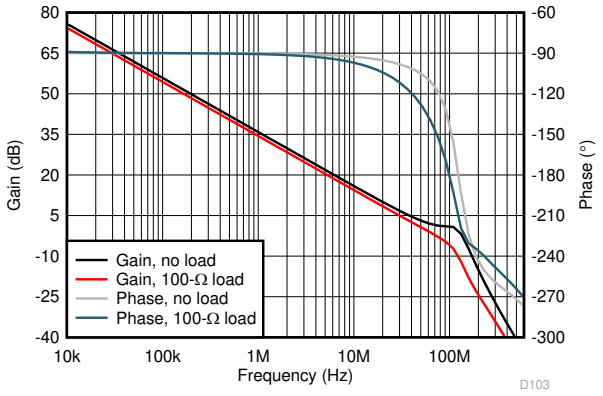


–40°C to +125°C endpoint drift, 50 DGK units for each V_S

図 7-40. Input Offset Current Drift Histogram

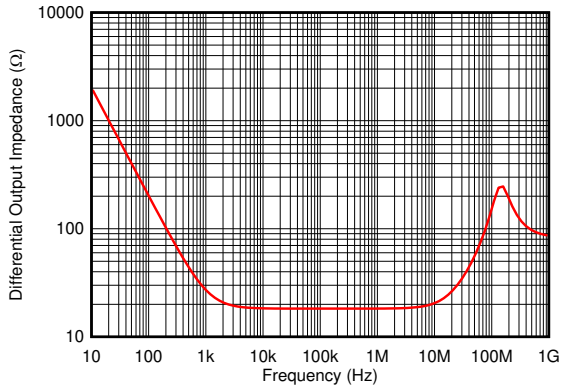
7.9 Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 3-V to 12-V Supply Range (continued)

at T_A ≈ 25°C, VOCM pin = open, R_F = 1.5 kΩ, R_L = 1 kΩ, V_O = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input, differential output, and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.



Simulated

図 7-41. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency



Simulated

図 7-42. Open-Loop Output Impedance vs Frequency

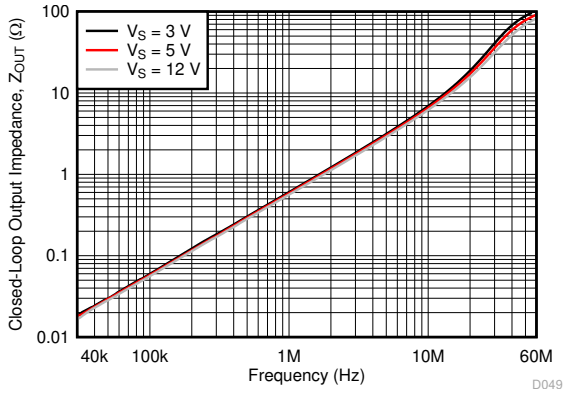
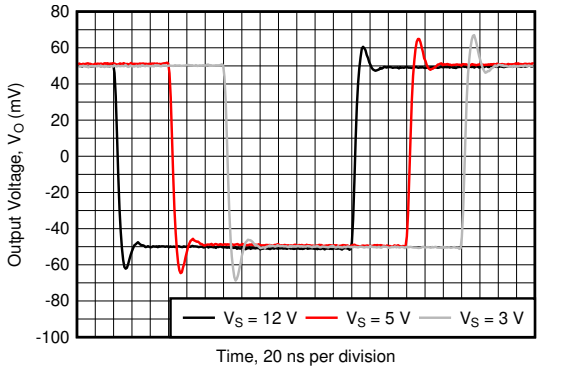
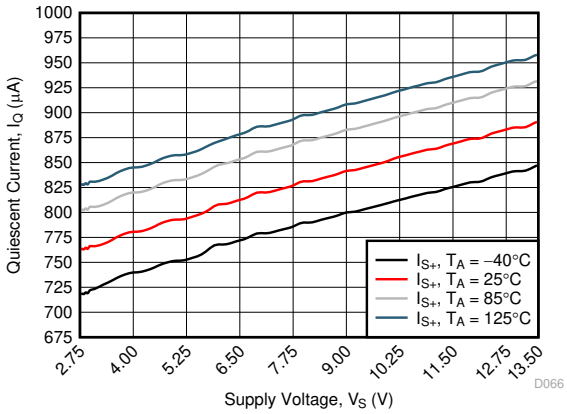


図 7-43. Closed-Loop Output Impedance vs Frequency



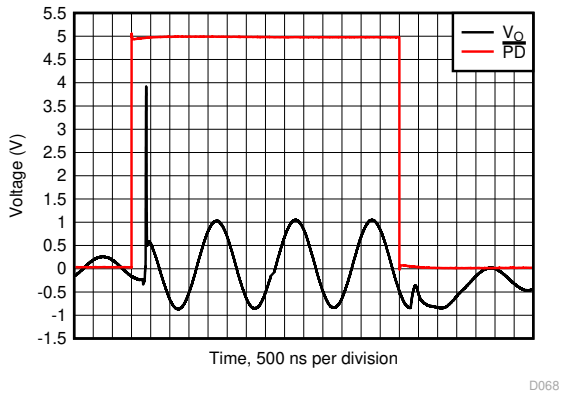
V_O = 100-mV step, t_r (10% - 90%) = 5.7 ns

図 7-44. Small-Signal Step Response



Average of 30 units

図 7-45. Quiescent Current vs V_S



5 MHz, 2-V_{PP} input, G = 1 V/V, see 図 8-1

図 7-46. $\overline{PD}$ Turnon and Turnoff Waveform

7.9 Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 3-V to 12-V Supply Range (continued)

at $T_A \approx 25°C$, VOCM pin = open, R_F = 1.5 kΩ, R_L = 1 kΩ, V_O = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input, differential output, and input and output referenced to default midsupply for AC-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit.

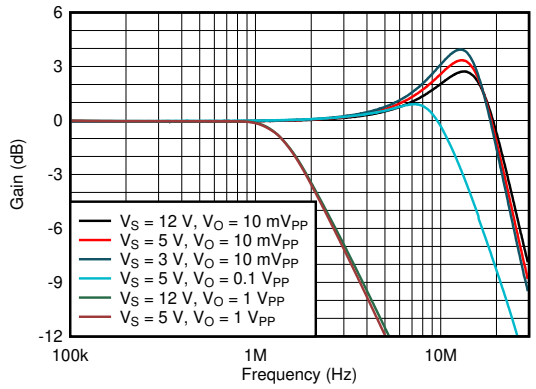
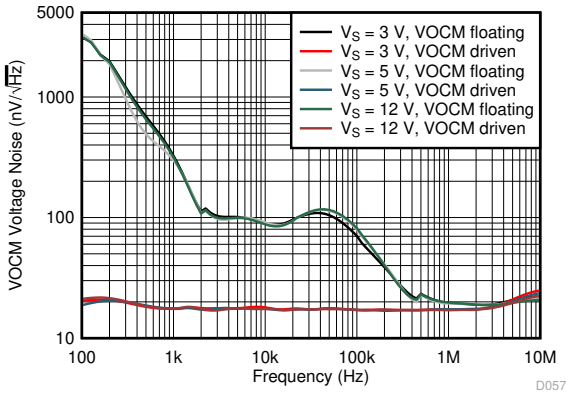
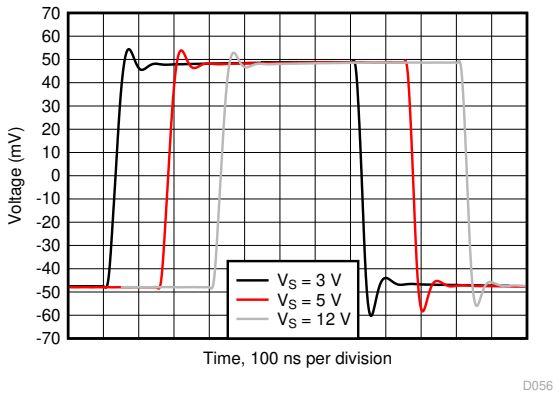


図 7-47. Common-Mode Voltage, Small-Signal and Large-Signal Response (VOCM Pin Driven)



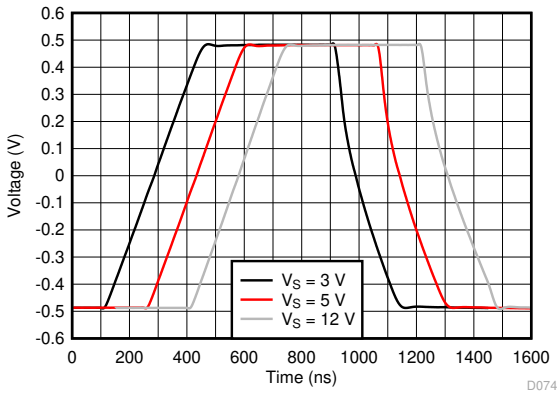
The VOCM pin is either driven to midsupply by low-impedance source or allowed to float and default to midsupply

図 7-48. Output Common-Mode (V_{OCM}) Noise vs Frequency



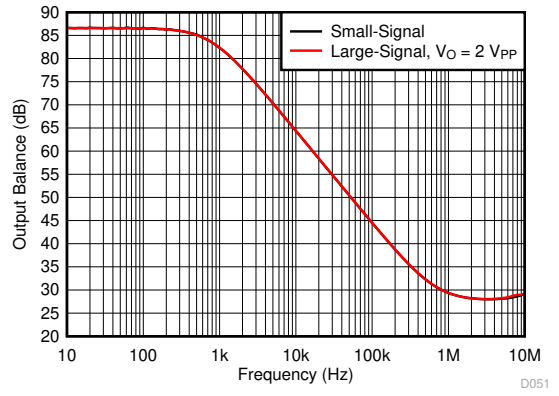
VOCM pin driven, 0.1-V VOCM step

図 7-49. Common-Mode Voltage Small-Signal Step Response



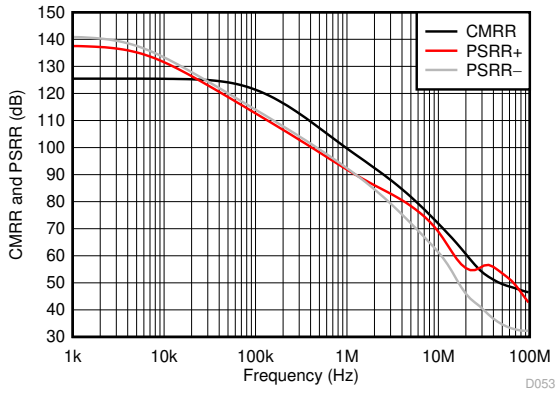
VOCM pin driven, 1-V VOCM step

図 7-50. Common-Mode Voltage Large-Signal Step Response



Simulated

図 7-51. Output Balance vs Frequency



Simulated

図 7-52. CMRR and PSRR vs Frequency

8 Parameter Measurement Information

8.1 Example Characterization Circuits

The THS4561 offers the advantages of a fully differential amplifier (FDA) design with the trimmed input offset voltage and low drift of a precision op amp. The FDA is a flexible device where the main aim is to provide a purely differential output signal centered on a user-configurable common-mode voltage usually matched to the input common-mode voltage required by an analog-to-digital converter (ADC) following the FDA stage. The primary options revolve around the choices of single-ended or differential inputs, AC-coupled or DC-coupled signal paths, gain targets, and resistor value selections. The characterization circuits described in this section focus on single-ended input to differential output designs as the more challenging application requirement. Differential sources are supported and are simple to implement and analyze.

The characterization circuits are typically operated with a single-ended, matched, 50-Ω, input termination to a differential output at the FDA output pins because most lab equipment is single-ended. The FDA differential output is then translated back to single-ended through a variety of baluns (or transformers) depending on the test and frequency range. DC-coupled step response testing uses two 50-Ω scope inputs with trace math to measure the differential output. Single-supply operation is most common in end equipment designs. However, using split balanced supplies allows simple ground referenced testing without adding further blocking capacitors in the signal path beyond those capacitors already within the test equipment. The starting point for any single-ended input to differential output measurements (such as any of the frequency response curves) is shown in 図 8-1.

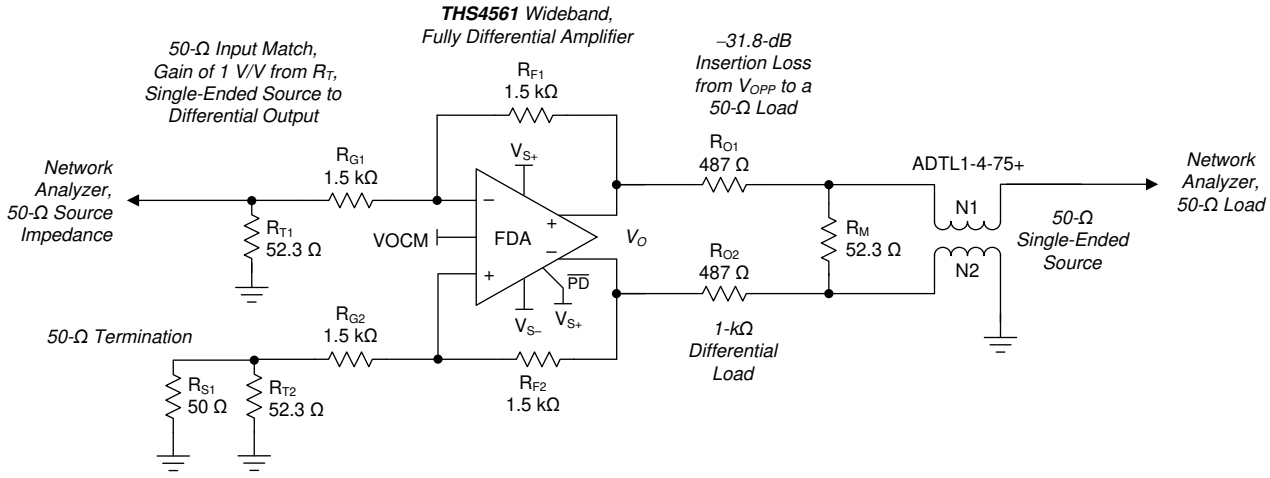


図 8-1. Single-Ended Source to a Differential Gain of a 1-V/V Test Circuit

Most characterization plots fix the R_F (R_{F1} = R_{F2}) value at 1.5 kΩ, as shown in 図 8-1. This element value is flexible in application, but 1.5 kΩ provides a good compromise for the parasitic issues linked to this value, specifically:

- Added output loading: The FDA functions similarly to an inverting op amp design with feedback resistors appearing as an added load across the outputs (the approximate total differential load in 図 8-1 is 1.5 kΩ || 1 kΩ = 857 Ω). The 1.5-kΩ value reduces the power dissipated in the feedback networks.
- Noise contributions resulting from resistor values. These contributions are both the $4kTR_F$ terms and the current noise times the R_F term referred to the output (see *セクション 10.1.3*).
- Parasitic feedback pole at the input summing nodes. This pole is created by the feedback resistor (R_F) value and the 2.4-pF differential input capacitance (as well as any board layout parasitic) and introduces a zero in the noise gain, which decreases the phase margin in most situations. This effect must be managed for best frequency response flatness or step response overshoot.

The frequency domain characterization curves start with the circuit and component selections of 図 8-1. Some of the features in this test circuit include:

- The elements on the non-signal input side match the signal input resistors. This feature closely matches the divider networks on each side of the FDA. The three resistors (R_{G2}, R_{T2}, and R_{S1}) on the non-signal input side can be replaced by a single resistor to ground using a standard value of 1.5 kΩ with some loss in gain balancing between the two sides.
- Translating from a 1-kΩ differential load to a 50-Ω environment introduces considerable insertion loss in the measurements (–31.8 dB in 図 8-1). The measurement path insertion loss normalizes when reporting the frequency response curves to show the gain response to the FDA output pins.
- In the pass band for the output balun, the 50-Ω load of the network analyzer reflects in parallel with the 52.3-Ω shunt termination, R_M. These elements combine to show a differential 1-kΩ load at the output pins of the THS4561. The source impedance presented to the balun is a differential 50-Ω source. 図 8-2 and 図 8-3 show the TINA-TI™ model (available as a TINA-TI™ simulation file) and resulting response flatness for this relatively low-frequency balun providing 0.1-dB flatness through 100 MHz.

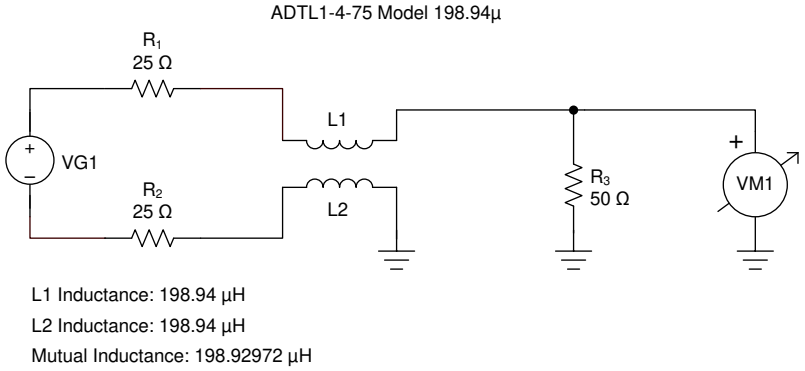


図 8-2. Output Measurement Balun Simulation Circuit in TINA-TI™

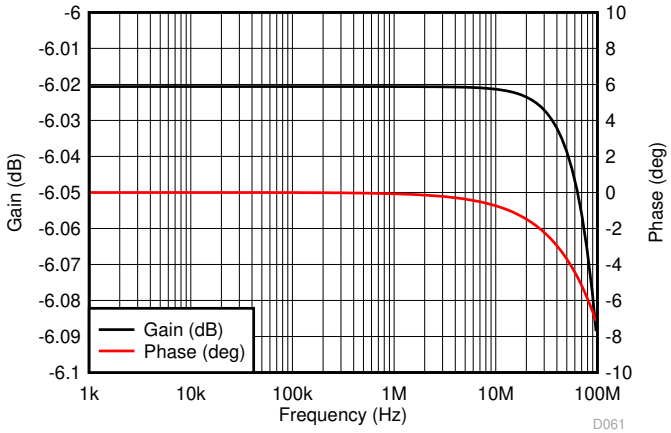


図 8-3. Output Measurement Balun Flatness Test

Starting from the test circuit of 図 8-1, various elements are modified to show the effect of these elements over a range of design targets, specifically:

- The gain setting is changed by adjusting the two R_T and the R_G resistors to provide a 50-Ω input match and setting the feedback resistors to 1.5 kΩ.
- Resistive and capacitive output load testing. Changing to lower resistive loads is accomplished by adding parallel resistors across the output pins in 図 8-1. Changing to capacitive loads adds series output resistors to a differential capacitance before the 1-kΩ sense path of 図 8-1.
- Power-supply settings. Most often, balanced bipolar supplies are used; a 12-V tests use ±6-V supplies, 5-V tests use ±2.5-V supplies, and 3-V tests use ±1.5-V supplies with the VOCM input control grounded.
- The disable control pin ($\overline{PD}$) is tied to the positive supply (V_{S+}) for any active channel test.

8.2 Output Interface Circuit for DC-Coupled Differential Testing

The pulse response plots are measured using the output circuit of 図 8-4. The two sides of this circuit present a 500-Ω load to ground (for a differential 1-kΩ load) with a 50-Ω source to the two scope inputs. Trace math function of the scope combines the two sides to generate the step response plots of 図 7-13, 図 7-27, and 図 7-44. Use balanced bipolar supplies for this test so that the THS4561 outputs deliver a ground-centered differential swing. This setup produces no DC load currents using the circuit of 図 8-4.

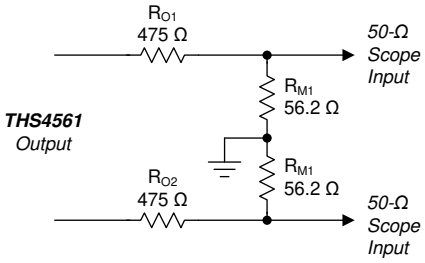


図 8-4. Output Interface for DC-Coupled Differential Outputs

8.3 Output Common-Mode Measurements

The circuit of 図 8-5 is a typical setup for common-mode measurements.

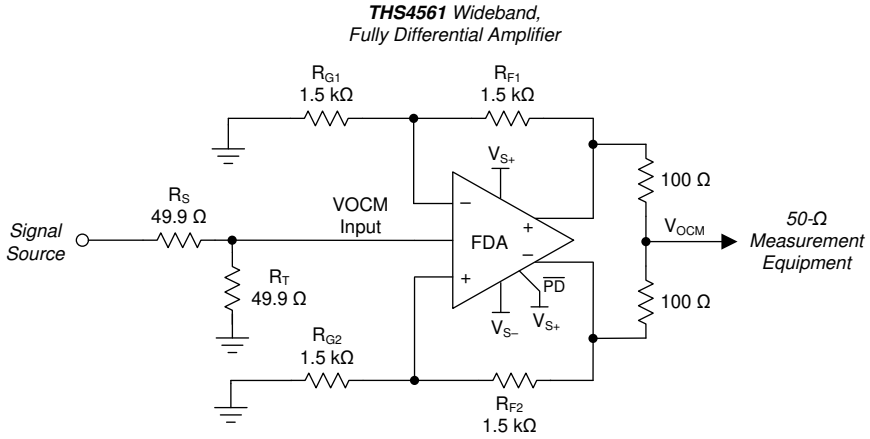


図 8-5. Output Common-Mode Measurements

In 図 8-5, the differential path is terminated back to ground with the two 1.5-kΩ input resistors and the VOCM control input is driven from a 50-Ω matched source for the frequency response and step response curves of 図 7-47, 図 7-49, and 図 7-50. The outputs are summed to a center point (to obtain the average, or common-mode output, V_{OCM}) through two 100-Ω resistors. These 100-Ω resistors form an equivalent 50-Ω source to the common-mode output for measurements. 図 7-48 illustrates the common-mode output noise measurements with

a ground on the VOCM input pin or with the VOCM input pin floating. The higher noise in 図 7-48 for a floated input can be reduced by including a capacitor to ground at the VOCM control input pin.

8.4 Differential Amplifier Noise Measurements

To extract the input-referred noise terms from the total output noise, a measurement of the differential output noise is required under two external conditions to emphasize the different noise terms. A high-gain, low resistor value condition is used to emphasize the differential input voltage noise and a higher R_F at low gains is used to emphasize the two input current noise terms. The differential output noise must be converted to single-ended with added gain before being measured by a spectrum analyzer. At low frequencies, a zero 1/f noise, high-gain, differential to single-ended instrumentation amplifier (such as the INA188) is used. At higher frequencies, a differential to single-ended balun is used to drive into a high-gain, low-noise, op amp (such as the LMH6629). In this case, the THS4561 outputs drive 25-Ω resistors into a 1:1 balun where the balun output is terminated single-endedly at the LMH6629 input with 50 Ω. This termination provides a modest 6-dB insertion loss for the THS4561 differential output noise that is then followed by a 40-dB gain setting in the very wideband LMH6629.

8.5 Balanced Split-Supply Versus Single-Supply Characterization

Although most end applications use a single-supply implementation, most characterizations are done on a bipolar balanced supply. Using a bipolar balanced supply keeps the I/O common-mode inputs near midsupply and provides the most output swing with no DC bias currents for level shifting. These characterizations include the frequency response, harmonic distortion, and noise plots. The time domain plots are in some cases done through single-supply characterization to obtain the correct movement of the input common-mode voltage.

8.6 Simulated Characterization Curves

In some cases, a characteristic curve can only be generated through simulation. A good example of this scenario is the output balance plot of 図 7-51. This plot shows the best-case output balance (output differential signal versus output common-mode signal) using exact matching of the external resistors in simulation using a single-ended input to differential output configuration. The actual output balance is set by resistor mismatch at low frequencies but intersects and follows the high-frequency portion of 図 7-51 at higher frequencies.

The remaining simulated plots include:

- A_{OL} gain and phase; see 図 7-41.
- CMRR and PSRR vs frequency; see 図 7-52.

8.7 Terminology and Application Assumptions

There are common terms that are unique to this device. This section identifies and explains these terms.

- Fully differential amplifier (FDA). This term is restricted to devices offering what is similar to a differential inverting op amp design element that requires an input resistor (not a high-impedance input) and includes a second internal control loop that sets the output average voltage (V_{OCM}) to a default or set point. This second common-mode control loop interacts with the differential loop in certain configurations.
- The desired output signal at the two output pins is a differential signal that swings symmetrically around a common-mode voltage, V_{OCM}, which is the average voltage of the two outputs.
- Single-ended to differential. Generally the output is always used differentially in an FDA; however, the source signal can be either a single-ended or a differential source. For an FDA operating in single-ended to differential, the input is applied only to one of the two inputs via input resistors.
- The common-mode control loop has limited bandwidth from the input VOCM pin to the common-mode output voltage. The internal loop bandwidth beyond the input VOCM buffer is a much wider bandwidth than the reported VOCM bandwidth, but is not directly discernable. A very wide bandwidth in the internal VOCM loop is required to perform an effective and low-distortion single-ended to differential conversion.

Several features in the application of the THS4561 are not explicitly stated, but are necessary for correct operation. These features are:

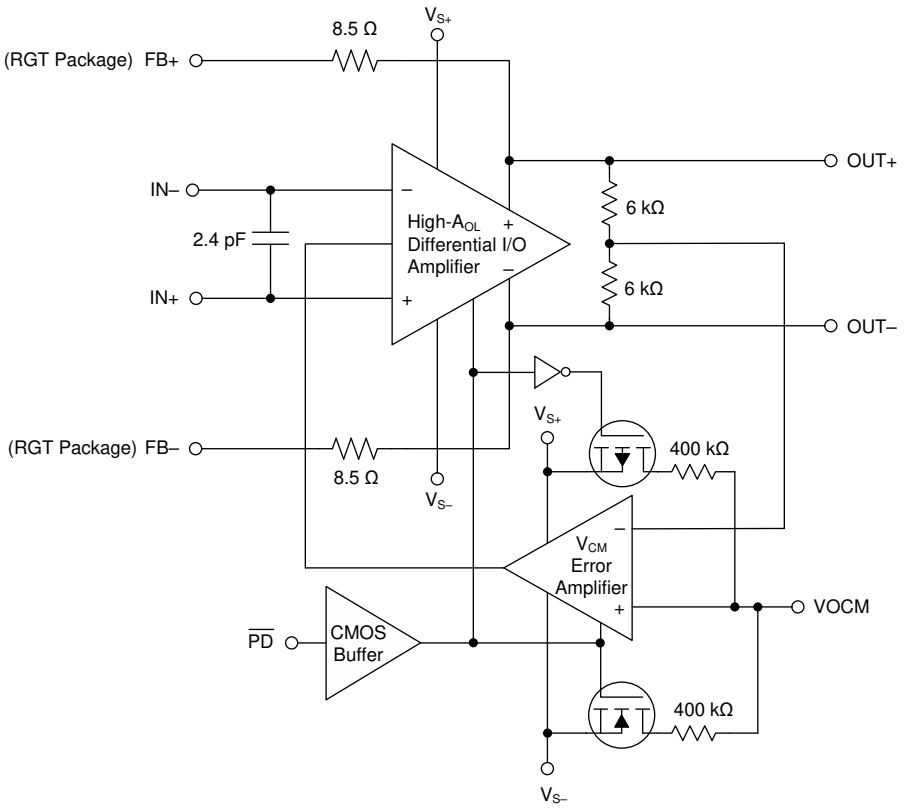
- Although often not stated, the disable pin ($\overline{PD}$) is tied to the positive supply when an enabled channel is desired.
- Virtually all ac characterization equipment expects a 50-Ω termination from the 50-Ω source and a 50-Ω, single-ended source impedance from the device outputs to the 50-Ω sensing termination. This condition is achieved in all characterizations (often with some insertion loss) but is not necessary for most applications. Matching impedance is most often required when transmitting over longer distances. Tight layouts from a source, through the THS4561, and to an ADC input do not require doubly-terminated lines or filter designs. The only exception is if the source requires a defined termination impedance for correct operation (for example, mixer outputs).
- The amplifier signal path is flexible for use as single-supply or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used as long as the total supply voltage across the TH4561 is less than 12.6 V and the required input, output, and common-mode pin headrooms to each supply are taken into account. When left open, the VOCM pin defaults to near midsupply for any combination of split or single supplies used.
- External element values are normally assumed to be accurate and matched. In an FDA, this assumption translates to equal feedback resistor values and a matched impedance from each input summing junction to either a signal source or a DC bias reference on each side of the inputs. Unbalancing these values introduces non-idealities in the signal path. For the signal path, imbalanced resistor ratios on the two sides creates a common-mode to differential conversion. Furthermore, mismatched R_F values and feedback ratios create additional differential output error terms from any common-mode DC or AC signal or noise terms. Using standard 1% resistor values is a typical approach and generally leads to some nominal feedback ratio mismatch. Modestly mismatched resistors or ratios do not by themselves degrade harmonic distortion. Where there is a meaningful common-mode noise or distortion in the input signal, that gets converted to differential via an element or ratio mismatch. For the best DC precision, use 0.1% accuracy resistors that are readily available in E96 values.

9 Detailed Description

9.1 Overview

The THS4561 is a fully differential amplifier featuring an extremely flexible supply voltage range of 2.85 V to 12.6 V, which makes this device an excellent choice for driving differential ADCs and buffering DAC outputs. This device features a low-power mode with a unique active-pullup resistor (not a conventional pullup resistor) that improves EMI reliability of the shutdown pin when left floating. This pin draws very little bias current when enabled, but increases the bias current as it nears the threshold point of shutdown. The increased current prevents the pin from unintentionally turning the device off in the presence of EMI on the disable pin. Similar to other fully differential amplifiers, the THS4561 also includes an output common-mode control pin that can be used to independently set the output common mode to match that of an ADC or other load circuit.

9.2 Functional Block Diagram



9.3 Feature Description

In addition to the core differential I/O voltage feedback gain block, there are two 6-kΩ resistors internally across the outputs to sense the average voltage at the outputs. These resistors feed the average voltage back into a V_{CM} error amplifier where the voltage is compared to either a default voltage divider across the supplies or an externally set VOCM target voltage. When the amplifier is disabled, the default midsupply bias string is disabled to save power.

To achieve the very-low noise at the low power provided by the THS4561, the input stage transistors are relatively large, thus resulting in a higher differential input capacitance (2.4 pF in *セクション 9.2*). When using the 16-pin WQFN package and the internal feedback traces to the input side of the package, include the nominal trace impedance of 8.5 Ω in the design. These elements are not included in the TINA-TI™ model and must be added externally to a design intending to use the RGT package.

9.4 Device Functional Modes

The wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either on with the $\overline{PD}$ pin asserted to a voltage greater than (V_{S+}) – 0.5 V, or turned off by asserting $\overline{PD}$ low (1.8 V below the positive supply). Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors, which provides poor signal isolation from the input to output in power-down mode.

Internal protection diodes remain present across the input pins in both operating and shutdown mode. Large input signals during disable can turn on the input differential protection diodes, thus producing a load current in the supply even in power-down.

The VOCM control pin sets the output average voltage. The VOCM defaults to an internal midsupply value if left open. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal V_{CM} error amplifier. If floated to obtain a default midsupply reference for VOCM, an external decoupling capacitor is recommended to be added on the VOCM pin to reduce the otherwise high output noise for the internal high-impedance bias (see 図 7-48).

9.4.1 Power-Down Mode

The power down ($\overline{PD}$) pin must be asserted to the desired voltage for proper power-down mode operation. A physical internal pullup resistor is not provided on the $\overline{PD}$ pin so that if the pin is floated, the device defaults to an ON state. Tie the $\overline{PD}$ pin to the positive supply voltage for applications that simply require the device to power on when the supplies are present. For single-supply operation, a minimum of 0.5 V within the positive supply is required for operation.

The disable operation is referenced from the positive supply. For an OFF state condition, the disable control pin must be 1.8 V below the positive supply. The THS4561 has a unique power-down circuit that requires overcoming the specified peak $\overline{PD}$ pulldown current when the $\overline{PD}$ voltage is pulled low. When this current threshold is overcome, the $\overline{PD}$ current drops to a very small value. The benefit of the circuit is that the device stays disabled without having to use an active pullup resistor that wastes crucial power to keep the amplifier disabled in power-sensitive applications.

9.4.2 Single-Ended Source to Differential Output Mode

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. Although the output side is relatively straightforward, the device input pins move in a common-mode manner with the input signal. The common-mode voltage at the input pins, which moves with the input signal, increases the apparent input impedance to be greater than the R_G value. The input active impedance issue applies to both AC-coupled and DC-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as discussed in *セクション 10.1.2*.

9.4.2.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversions

When the signal path can be AC-coupled, the DC biasing for the THS4561 becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The AC-coupling requirement can be separated for the input and output sides of an FDA design. The input can be AC-coupled and the output DC-coupled, or the output can be AC-coupled and the input DC-coupled, or both can be AC-coupled. One situation where the output can be DC-coupled (for an AC-coupled input), is when driving directly into an ADC where the VOCM control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode voltage to the required ADC input common-mode voltage. In any case, the design starts by setting the desired V_{OCM}. When an AC-coupled path follows the output pins, the best linearity is achieved by operating VOCM at midsupply, which can be easily delivered by floating the VOCM pin. The VOCM voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications. If the output path is also AC-coupled, simply letting the VOCM control pin float is usually preferred in order to obtain a midsupply default V_{OCM} bias with minimal elements. To limit noise, place a 0.1-µF decoupling capacitor on the VOCM control pin to ground.

After V_{OCM} is defined, check the target output voltage swing to make certain that the V_{OCM} plus the positive and negative output swing on each side does not clip into the supplies. If the desired peak-to-peak output differential swing is defined as V_{OPP}, divide by 4 to obtain the $\pm V_P$ (peak voltage) swing around V_{OCM} at each of the two output pins (each pin operates 180° out of phase with the other). Check that $V_{OCM} \pm V_P$ does not exceed the absolute supply rails for the rail-to-rail output (RRO) device. Common-mode current does not flow from the common-mode output voltage set by the VOCM pin towards the device input pins side, because both the source and balancing resistor on the non-signal input side are DC blocked. The AC-coupled input path sets the input pin common-mode voltage equal to the output common-mode voltage. If the VOCM voltage is within the headroom requirement, then the input pins are also in range for the AC-coupled input configuration. This headroom requirement functions similarly for when the V_{OCM} voltage approaches the negative supply.

The input pin voltages move in a common-mode manner with the input signal. Confirm that the VOCM voltage plus the input V_{PP} common-mode swing also stays in the V_{ICM} specification range for the input pins.

9.4.2.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversions

The output considerations remain the same as for the AC-coupled design. Again, the input can be DC-coupled when the output is ac coupled. A DC-coupled input with an AC-coupled output can have some advantages to move the input V_{ICM} down by adjusting the V_{OCM} down if the source is ground referenced. When the source is DC-coupled into the THS4561 (see 図 10-3), both sides of the input circuit must be DC-coupled to retain differential balance. Normally, the non-signal input side has an R_G element biased to whatever the source midrange is expected to be, provided that this midscale reference gives a balanced differential swing around V_{OCM} at the outputs. Often, R_{G2} is simply grounded for DC-coupled, bipolar-input applications. This configuration provides a balanced differential output if the source swings around ground. If the source swings from ground to some positive voltage, grounding R_{G2} gives a unipolar output differential swing from both outputs at V_{OCM} (when the input is at ground) to one polarity of the swing. Biasing R_{G2} to an expected midpoint for the input signal creates a differential output swing around V_{OCM}.

One significant consideration for a DC-coupled input is that VOCM sets up a common-mode bias current from the output back through R_F and R_G to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this dc current. After the input signal range and biasing on the other R_G element is set, check that the voltage divider from V_{OCM} to V_{IN} through R_F and R_G (and possibly R_S) establishes an input V_{ICM} at the device input pins that is within the specification range. If the average source is at ground, the negative rail input stage for the THS4561 is in range for applications using a single positive supply and a positive output V_{OCM} setting because this dc common-mode current lifts the average FDA input summing junctions above ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA). TINA-TI™ simulations of the intended circuit offer a good check for input and output pin voltage swings.

9.4.3 Differential Input to a Differential Output Mode

In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, assuming that the two sides of the circuit are balanced with equal R_F and R_G elements, the differential input impedance is now just the sum of the two R_G elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal but must be dc biased in the design range for the input pins and must take into account the voltage headroom required to each supply. Slightly different considerations apply to AC-coupled or DC-coupled differential input to differential output designs, as described in the following sections.

9.4.3.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

The most common way to use the THS4561 with an AC-coupled differential source is to simply couple the input into the R_G resistors through the blocking capacitors. 図 9-1 shows a typical blocking capacitor approach to a differential input. An optional input differential termination resistor (R_M) is included in this design. The R_M element allows the input R_G resistors to be scaled up and still delivers lower differential input impedance to the source. In this example, the R_G elements sum to show a 1-kΩ differential impedance and the R_M element combines in parallel to provide a net 500-Ω ac differential impedance to the source. Again, the design ideally proceeds by selecting the R_F element values, then the R_G to set the differential gain, and then an R_M element (if needed) to achieve a target input impedance. Alternatively, the R_M element can be eliminated, with the 2 × R_G elements set to the desired input impedance and R_F set to obtain the differential gain (equal to R_F / R_G).

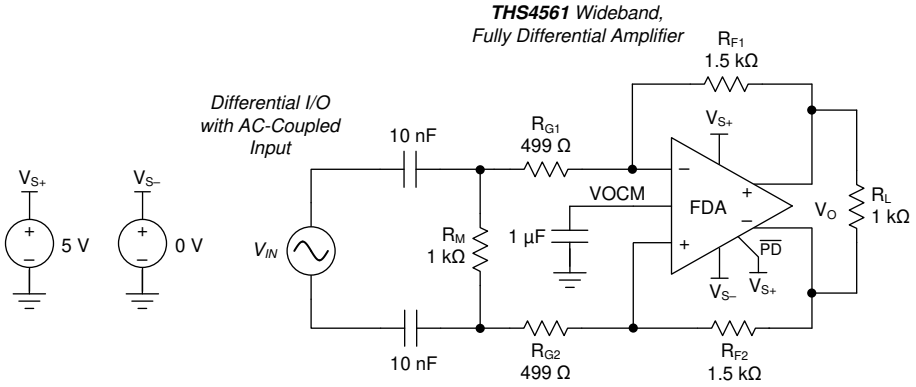


図 9-1. Example AC-Coupled Differential Input Design

The DC biasing for an AC-coupled differential input design is very simple. The output V_{OCM} is set by the VOCM input control voltage and, because there is no DC current path for the output common-mode voltage (as long as R_M is only differential and not split and connected to ground for instance), the VOCM DC bias also sets the common-mode operating points for the input pins. For a purely differential input, the voltages on the input pins remain fixed at the output V_{OCM} setting and do not move with the input signal (unlike the single-ended input configurations where the input pin common-mode voltages do move with the input signal).

10 Application and Implementation

Note

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10.1 Application Information

Most applications for the THS4561 strive to deliver the best dynamic range in a design that delivers the desired signal processing along with adequate phase margin for the amplifier itself. The following sections detail some of the design issues with analysis and guidelines for improved performance.

10.1.1 Differential Open-Loop Gain and Output Impedance

The most important elements to the closed-loop performance are the open-loop gain and open-loop output impedance. 図 10-1 shows the simulated differential open-loop gain and phase from the differential inputs to the differential outputs with no load and with a 100-Ω load. Operating with no load removes any effect introduced by the open-loop output impedance to a finite load. 図 10-2 shows the simulated differential open-loop output impedance.

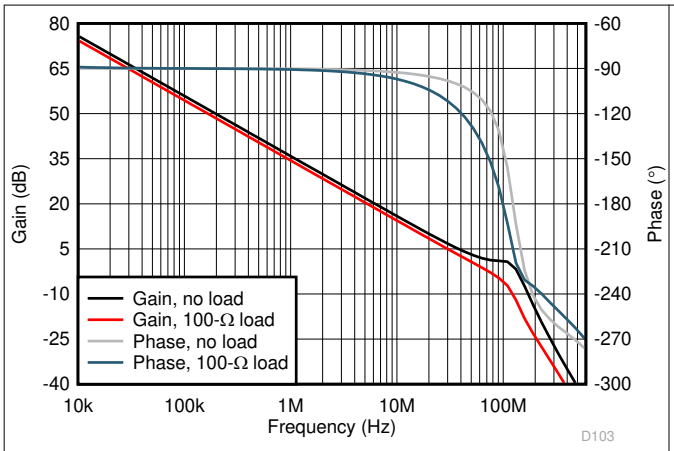


図 10-1. No-Load and 100-Ω Loaded A_{OL} Gain and Phase

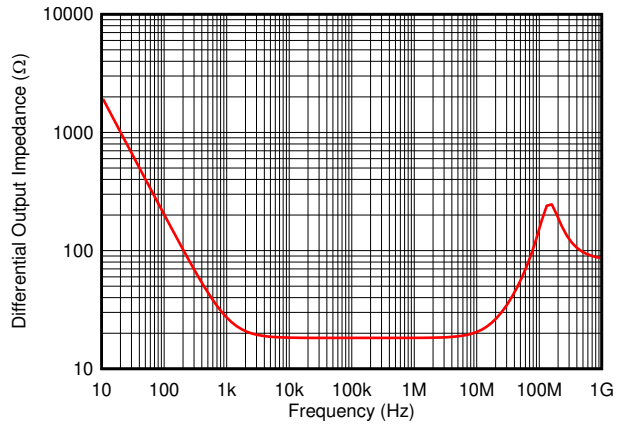


図 10-2. Differential Open-Loop Output Impedance

This open-loop output impedance combines with the load to shift the apparent open-loop gain and phase to the output pins when the load changes. The rail-to-rail output stage shows a very high impedance at low frequencies that reduces with frequency to a lower midrange value and then peaks again at higher frequencies. The maximum value at low frequencies is set by the common-mode sensing resistors to be a 6-kΩ dc value (see *セクション 9.2.*) This high impedance at a low frequency is significantly reduced in closed-loop operation by the loop gain, as shown in the closed-loop output impedance of 図 7-43. 図 10-1 compares the no load A_{OL} gain to the A_{OL} gain driving a 100-Ω load that shows the effect of the output impedance. The heavier loads pull the A_{OL} gain down faster to lower crossovers with more phase shift at the lower frequencies.

The much faster phase rolloff for the 100-Ω differential load explains the greater peaked response illustrated in 図 7-4 and 図 7-18 when the load decreases. This same effect happens for the RC loads common with converter interface designs. Use the TINA-TI™ model to verify loop phase margin in any design.

10.1.2 Setting Resistor Values Versus Gain

The THS4561 offers considerable flexibility in the configuration and selection of resistor values. The design starts with the selection of the feedback resistor value. The 1.5-kΩ feedback resistor value used for the characterization curves is a good compromise between power, noise, and phase margin considerations. With the feedback resistor values selected (and set equal on each side) the input resistors are set to obtain the desired gain with input impedance also set with these input resistors. Differential I/O designs provide an input impedance that is the sum of the two input resistors. Single-ended input to differential output designs present a more complicated input impedance. Most characteristic curves implement the single-ended to differential design as the more challenging requirement over differential-to-differential I/O.

For single-ended, matched, input impedance designs, 表 10-1 illustrates the suggested standard resistors set to approximately a 1.5-kΩ feedback. This table assumes a 50-Ω source and a 50-Ω input match and uses a single resistor on the non-signal input side for gain matching. Better matching is possible using the same three resistors on the non-signal input side as on the input side. 図 10-3 shows the element values and naming convention for the gain of 1-V/V configuration where the gain is defined from the matched input at R_T to the differential output.

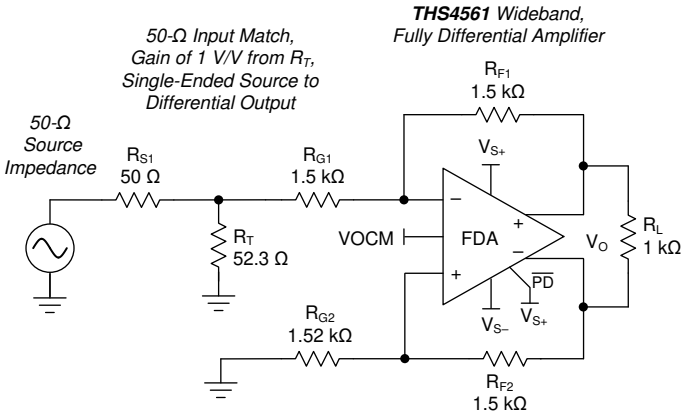


図 10-3. Single-Ended to Differential Gain of 1 V/V with Input Matching Using Standard Resistor Values

Starting from a target feedback resistor value, the desired input matching impedance, and the target gain (A_V), the required input R_T value is given by solving the quadratic of 式 1.

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F(2+A_V) - R_S A_V(4+A_V)} - \frac{2R_F R_S^2 A_V}{2R_F(2+A_V) - R_S A_V(4+A_V)} = 0 \quad (1)$$

When this value is derived, the required input side gain resistor is given by 式 2 and then the single value for R_{G2} on the non-signal input side is given by 式 3:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \quad (2)$$

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \quad (3)$$

Using these expressions to generate a swept gain table of values results in 表 10-1, where the best standard 1% resistor values are shown to minimize input impedance and gain error to target.

表 10-1. Swept Gain 50-Ω Input Match with R_F = 1.5-kΩ (±1 Standard Values)

GAIN (V/V)	R_F	R_{G1}	R_T	R_{G2}	Z_{IN}	A_V
0.1	1500	15000	49.9	15000	49.74	0.09973
1	1500	1500	51.1	1500	49.82	0.994
2	1500	750	52.3	768	49.98	1.978
5	1500	287	54.9	316	49.6	5.014
10	1500	137	61.9	165	50.4	10.08

Where an input impedance match is not required, simply set the input resistor to obtain the desired gain without an additional resistor to ground (remove R_T in 図 10-3). This scenario is common when coming from the output of another single-ended op amp (such as the OPA810 or OPA192). This single-ended to differential stage shows a higher input impedance than the physical R_G as given by the expression for Z_A (active input impedance) shown as 式 4.

$$Z_A = R_{G1} \frac{\left(1 + \frac{R_{G1}}{R_{G2}}\right)\left(1 + \frac{R_F}{R_{G1}}\right)}{2 + \frac{R_F}{R_{G2}}} \tag{4}$$

Using 式 4 for the gain of 1 V/V with all resistors equal to 1.5-kΩ shows an input impedance of 2 kΩ. The increased input impedance comes from the common-mode input voltage at the amplifier pins moving in the same direction as the input signal. The common-mode input voltage must move to create the current in the non-signal input R_G resistor to produce the inverted output. The current flow into the signal-side input resistor is impeded because the common-mode input voltage moves with the input signal, thus increasing the apparent input impedance in the signal input path.

10.1.3 Noise Analysis

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground. 図 10-4 shows the simplest analysis circuit with the FDA and resistor noise terms to be considered.

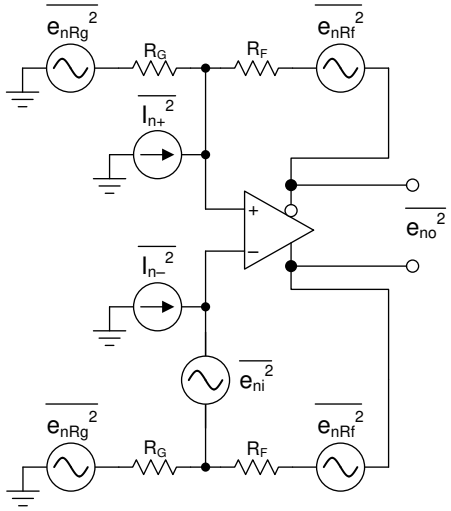


図 10-4. FDA Noise Analysis Circuit

The noise powers are shown in 図 10-4 for each term. When the R_F and R_G terms are matched on each side, the total differential output noise is the root sum squared (RSS) of these separate terms. Using NG ≡ 1 + R_F / R_G, the total output noise is given by 式 5. Each resistor noise term is a 4kT × R power (4kT = 1.6E-20J at 290K).

$$e_o = \sqrt{(e_{ni}NG)^2 + 2(i_N R_F)^2 + 2(4kTR_FNG)} \tag{5}$$

The first term is simply the differential input spot noise times the noise gain, the second term is the input current noise terms times the feedback resistor (and because there are two uncorrelated current noise terms, the power is two times one of them), and the last term is the output noise resulting from both the R_F and R_G resistors, at again twice the value for the output noise power of each side added together. Running a wide sweep of gains when holding R_F close to 1.5 kΩ and setting the input up for a 50-Ω match gives the standard values and resulting noise listed in 表 10-2.

When the gain increases, the input-referred noise approaches only the gain of the FDA input voltage noise term at 5 nV/√Hz.

表 10-2. Swept Gain of the Output- and Input-Referred Spot Noise Calculations

GAIN (V/V)	R_F	R_{G1}	R_T	R_{G2}	Z_{IN}	A_V	e_O (nV/√Hz)	e_I (nV/√Hz)
0.1	1500	15000	49.9	15000	49.74	0.09973	9.15	91.53
1	1500	1500	51.1	1500	49.82	0.994	14.03	14.03
2	1500	750	52.3	768	49.98	1.978	18.99	9.49
5	1500	287	54.9	316	49.6	5.014	33.20	6.64
10	1500	137	61.9	165	50.4	10.08	55.05	5.51

10.1.4 Factors Influencing Harmonic Distortion

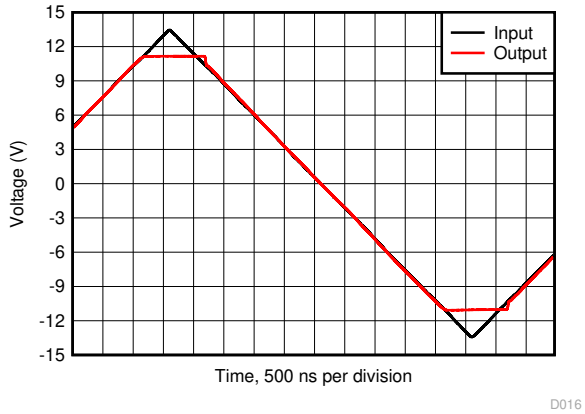
As illustrated in the swept frequency harmonic distortion plots (図 7-7 and 図 7-21), the THS4561 provides extremely low distortion at lower frequencies. In general, an FDA output harmonic distortion mainly relates to the open-loop linearity in the output stage corrected by the loop gain at the fundamental frequency. When the total load impedance decreases, including the effect of the feedback resistor elements in parallel for loading purposes, the output stage open-loop linearity degrades, thus increasing the harmonic distortion; see 図 7-9 and 図 7-23. When the output voltage swings increase, very fine scale open-loop output stage nonlinearities increase that also degrade the harmonic distortion; see 図 7-8 and 図 7-22. Conversely, decreasing the target output voltage swings drops the distortion terms rapidly. 図 7-8 and 図 7-22 illustrate the effect of going up to a 10-V_{PP} and 8-V_{PP} differential output, respectively, that is more common with SAR converters.

Increasing the noise gain functions to decrease the loop gain resulting in the increasing harmonic distortion terms; see 図 7-10 and 図 7-24. One advantage of capacitive compensation that is typical in attenuator designs is that the noise gain is shaped up with frequency to achieve a crossover at an acceptable phase margin at higher frequencies. This technique holds the loop gain high at frequencies lower than the noise gain zero, thus improving distortion at lower frequencies.

The THS4561 does an exceptional job of converting from single-ended inputs to differential outputs with very low harmonic distortions. External resistors of 1% tolerance are used in characterization with good results. Unbalancing the feedback divider ratios does not degrade distortion directly. However, imbalanced feedback ratios convert common-mode inputs to a differential mode at the outputs that can result in increased output errors.

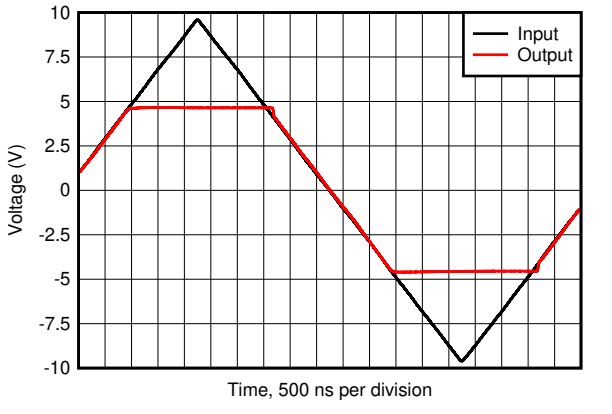
10.1.5 Input Overdrive Performance

図 10-5 and 図 10-6 show a 2-V and a 2X output overdrive triangular waveform, respectively, for the THS4561. When the output maximum swing is reached at approximately the supply values, increasing input voltage beyond this condition turns on the internal protection diodes across the two input pins. The internal protection diodes are two diodes in series in both polarities. This feature clamps the maximum differential voltage across the inputs to approximately 1.5 V when the output is limited at the supplies but the input exceeds the available range. The input resistors on both sides limit the current flow in the internal diodes under these conditions.



V_S = 12 V, Single-ended to differential gain of 2, 2-V output overdrive,
overdrive recovery = 250 ns

図 10-5. Overdrive Recovery Performance



V_S = 5 V, Single-ended to differential gain of 2, 2x input overdrive,
overdrive recovery = 210 ns

図 10-6. Overdrive Recovery Performance

10.2 Typical Application

One common application for the THS4561 is to take a single-ended, high V_{PP} voltage swing (from a high-voltage precision amplifier such as the OPA810 or OPA192) and deliver that swing to precision SAR ADC as a single-ended to differential conversion with output common-mode control and implement an active 2nd-order multiple feedback (MFB) filter design. Designing for a 16-V_{PP} maximum input down to an 8-V_{PP} differential swing requires a gain of 0.5 V/V. Targeting a 170-kHz Butterworth response with the RC elements tilted towards low noise gives the example design of 図 10-7. The V_{CM} control is set to half of a 4.096-V reference, which is typical for 5-V differential SAR applications. With the high voltage capabilities of the THS4561, the design can be easily adopted for 20-V_{PP} input swing to the FDA for a full 10-V_{PP} swing into 5-V differential SAR ADC by simply using wider power supplies for the THS4561 to allow for increased output swing headroom with minimal performance degradation.

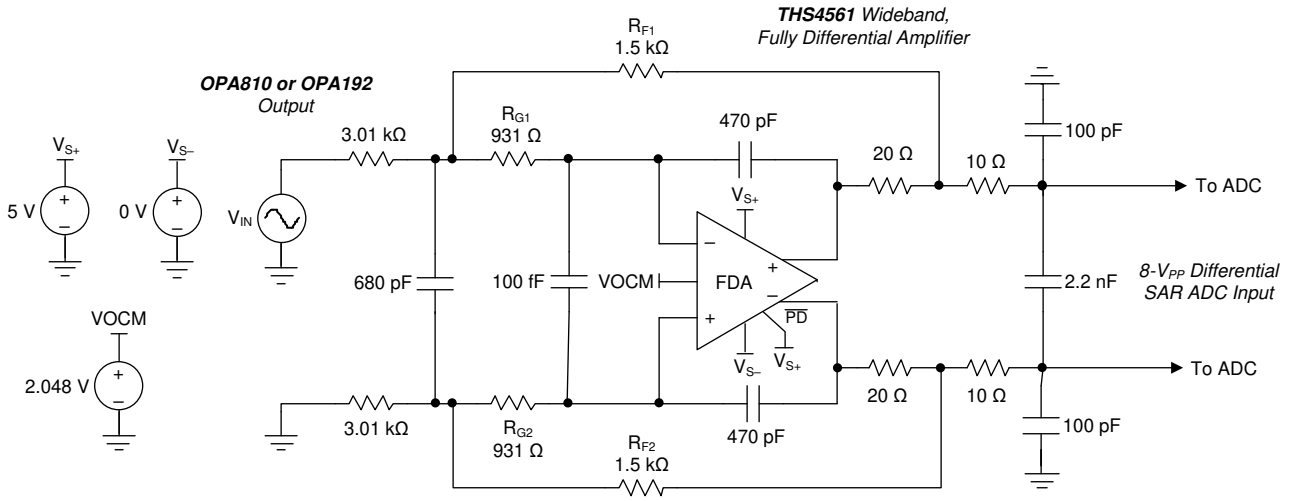


図 10-7. MFB Filter Driving an ADC Application: Example 170-kHz Butterworth Response

10.2.1 Design Requirements

The requirements for this application are:

- Single-ended to differential conversion
- Attenuation by 0.5-V/V gain
- Active filter set to a Butterworth, 170-kHz response shape
- Output RC elements set by SAR input requirements (not part of the filter design)
- Filter element resistors and capacitors are set to limit added noise over the THS4561 and noise peaking

10.2.2 Detailed Design Procedure

The design proceeds using the techniques and tools suggested in the *Design Methodology for MFB Filters in ADC Interface Applications* application note. The process includes:

- Scale the resistor values to not meaningfully contribute to the output noise produced by the THS4561 by itself
- Select the RC ratios to hit the filter targets when reducing the noise gain peaking within the filter design
- Set the output resistor to 10 Ω into a 2.2-nF differential capacitor
- Add 100-pF common-mode capacitors to the load capacitor to improve common noise filtering
- Inside the loop, add 20-Ω output resistors after the filter feedback capacitor to increase the isolation to the load capacitor
- Include a place for a differential input capacitor (illustrated as 100 fF in 図 10-7)

10.2.3 Application Curves

図 10-8 and 図 10-9 show the gain response and the noise results of the circuit shown in 図 10-7. 図 10-7 shows a place for a differential input capacitor (shown as 100 fF) but is not used for the simulation results shown in this

section. Results in 図 10-8 illustrate a flat Butterworth filter response at the output nodes going to the ADC. Obtaining the SNR to the ADC input pins, and assuming an 8-V_{PP} full scale (2.83 V_{RMS}), gives the result of 図 10-9. The 116-dB SNR and 13-μV_{RMS} total noise shown in 図 10-9 does not limit the performance for any SAR application.

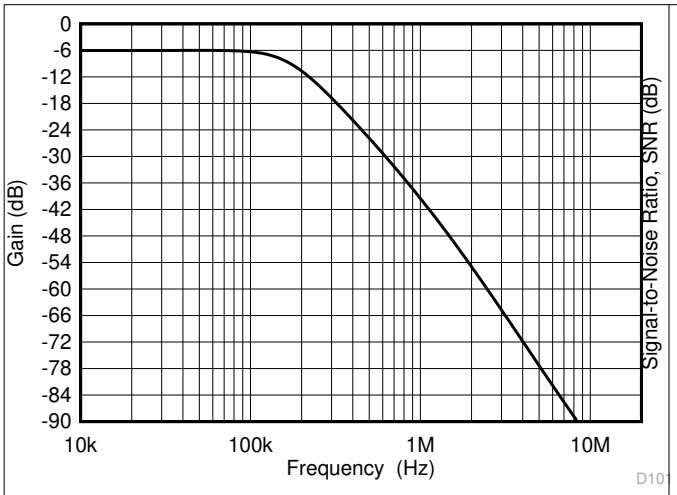


図 10-8. Gain Plot for a 170-kHz Butterworth Filter

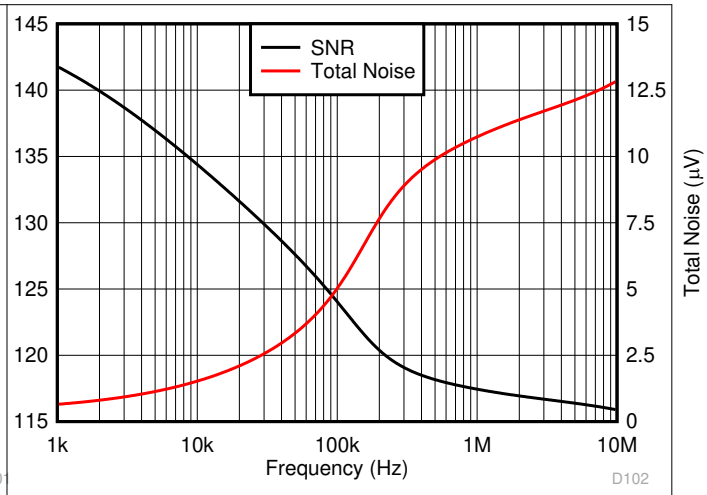


図 10-9. Signal-to-Noise Ratio and Total Noise Plot

11 Power Supply Recommendations

The THS4561 is principally intended to operate with a nominal single-supply voltage of 3 V to 12 V. Supply voltage tolerances are supported with the specified operating range of 2.85 V (10% low on a 3-V nominal supply) and 12.6 V (5% high on a 12-V nominal supply). Supply decoupling is required, as described in *セクション 8.7*. Split (or bipolar) supplies can be used with the THS4561, as long as the total value across the device remains less than that specified in セクション 7.3.

Using a negative supply to deliver a true swing to ground output when driving SAR ADCs can be desired. Although the THS4561 quotes a rail-to-rail output, linear operation requires approximately 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed, negative-supply generator can accept a 3-V to 5-V positive supply and provides a fixed –230-mV supply for the negative power supply. Using the LM7705 provides an effective solution, as discussed in the *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* reference guide.

12 Layout

12.1 Layout Guidelines

12.1.1 Board Layout Recommendations

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. The provides a good example of high-frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes that may not apply to some applications. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.1 µF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2 µF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Any R_G elements must connect into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the R_G elements can have more trace length if needed to the source or to GND.

12.2 Layout Examples

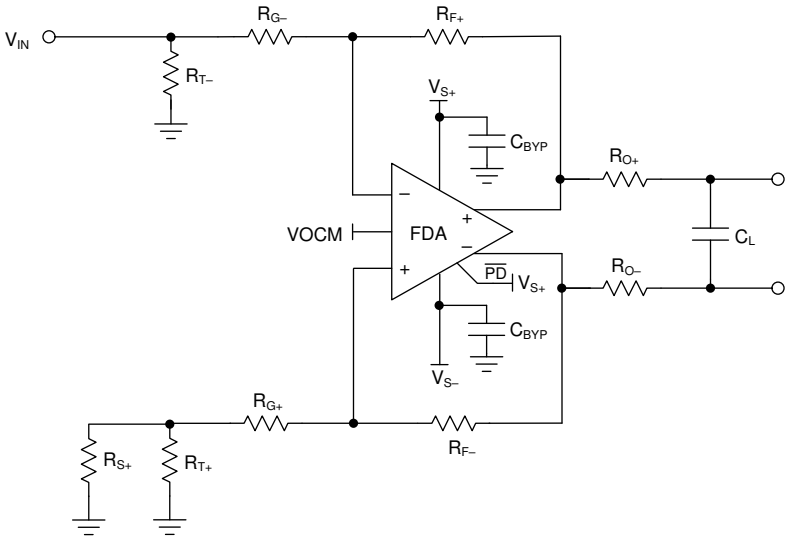


図 12-1. Representative Schematic for the Layout in

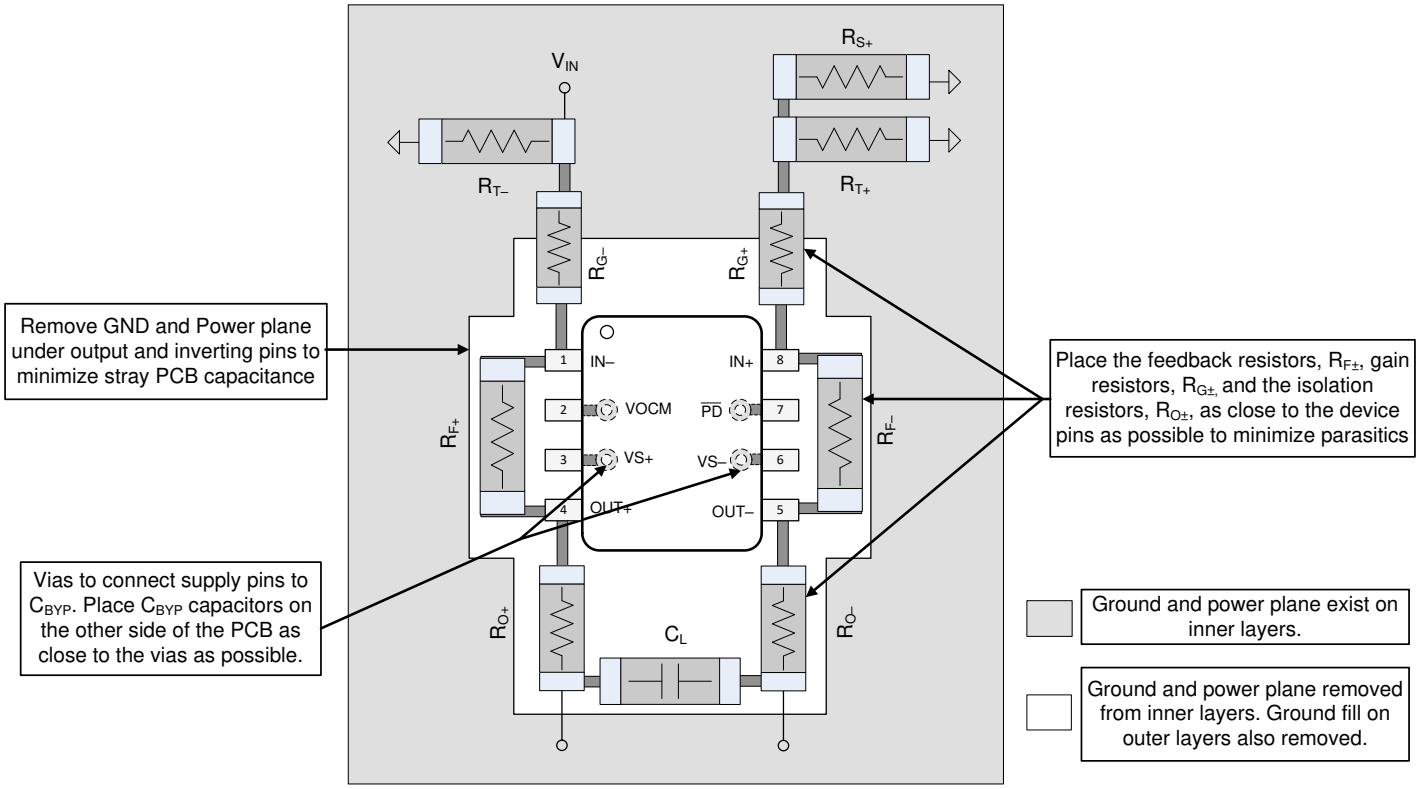


図 12-2. Layout Recommendations

13 Device and Documentation Support

13.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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13.5 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4561IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	4561	Samples
THS4561IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	4561	Samples
THS4561IRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TH4561	Samples
THS4561IRUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4561	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

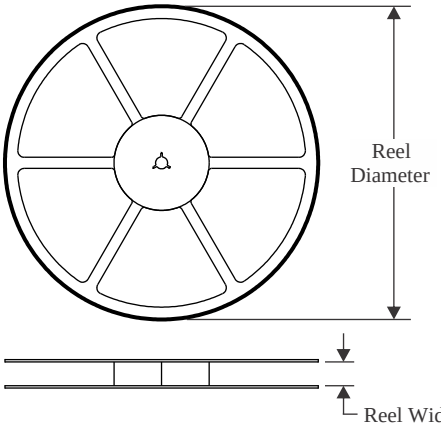
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

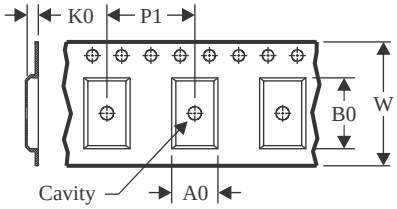
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

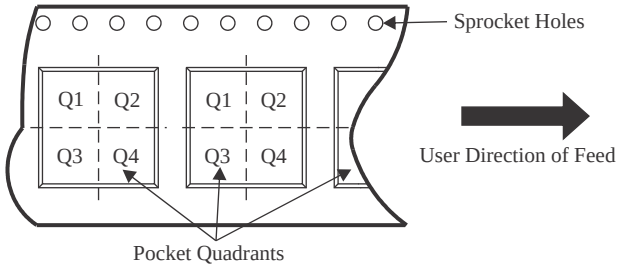


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

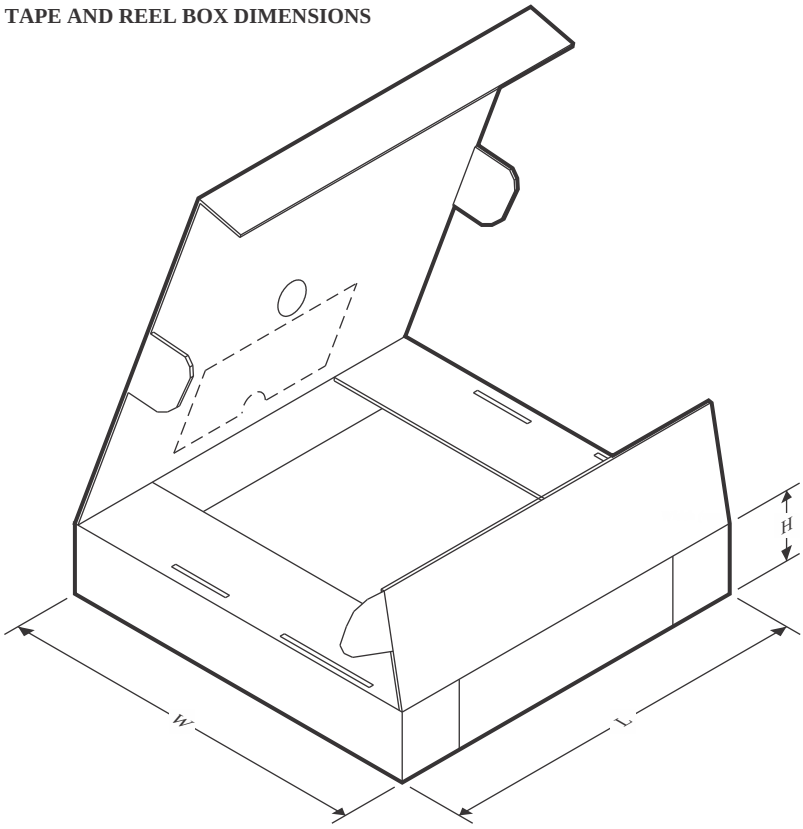
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4561IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4561IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4561IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4561IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4561IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4561IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4561IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
THS4561IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
THS4561IRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
THS4561IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

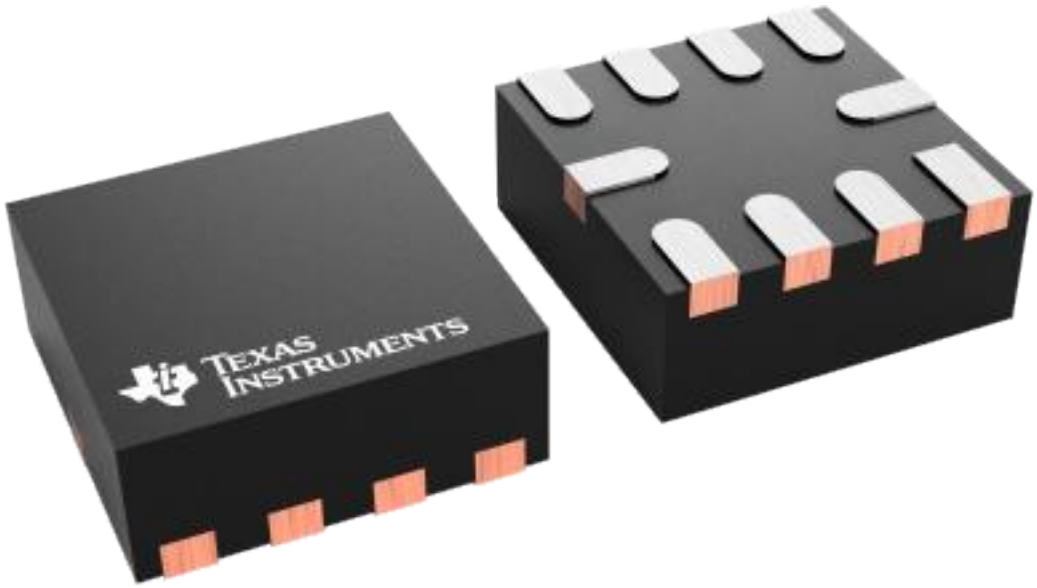
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



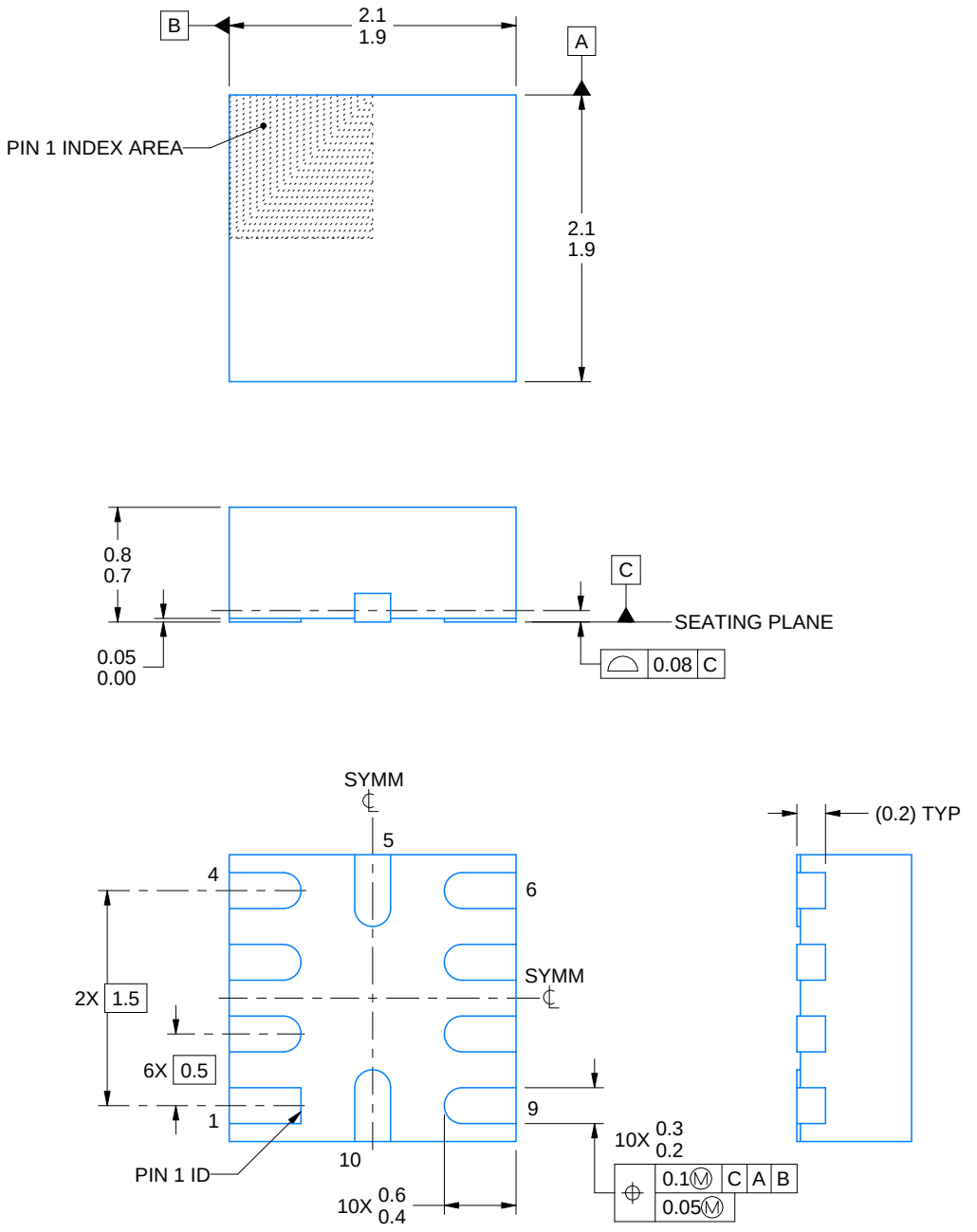
4228249/A

RUN0010A

PACKAGE OUTLINE

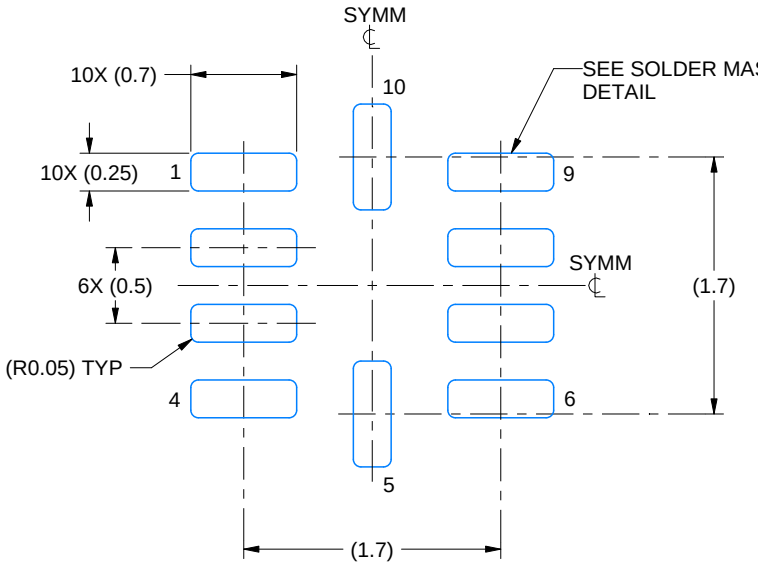
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

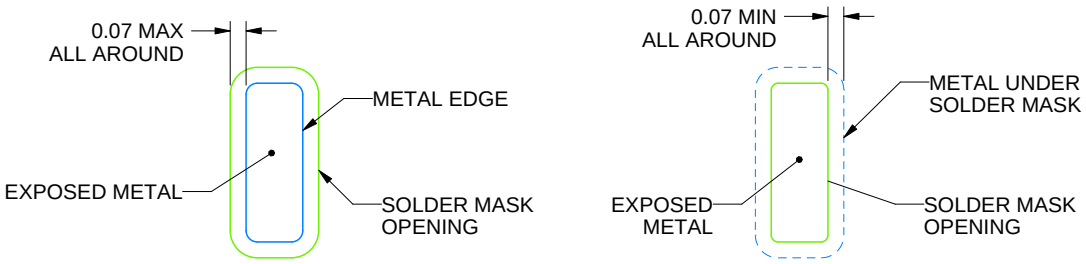


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

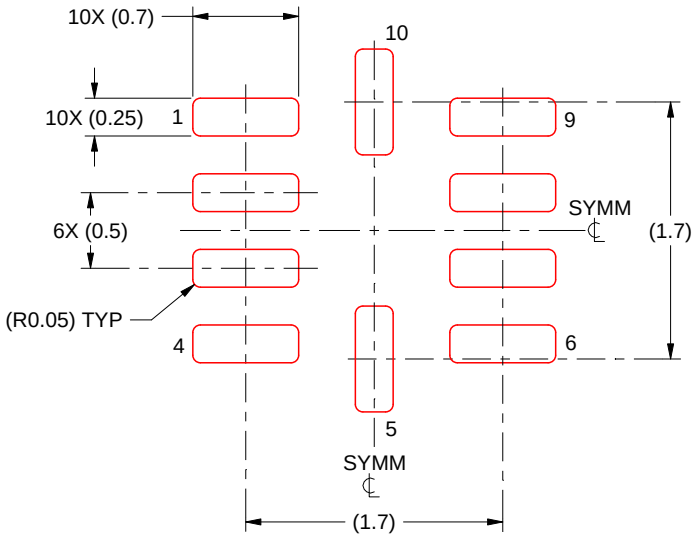
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

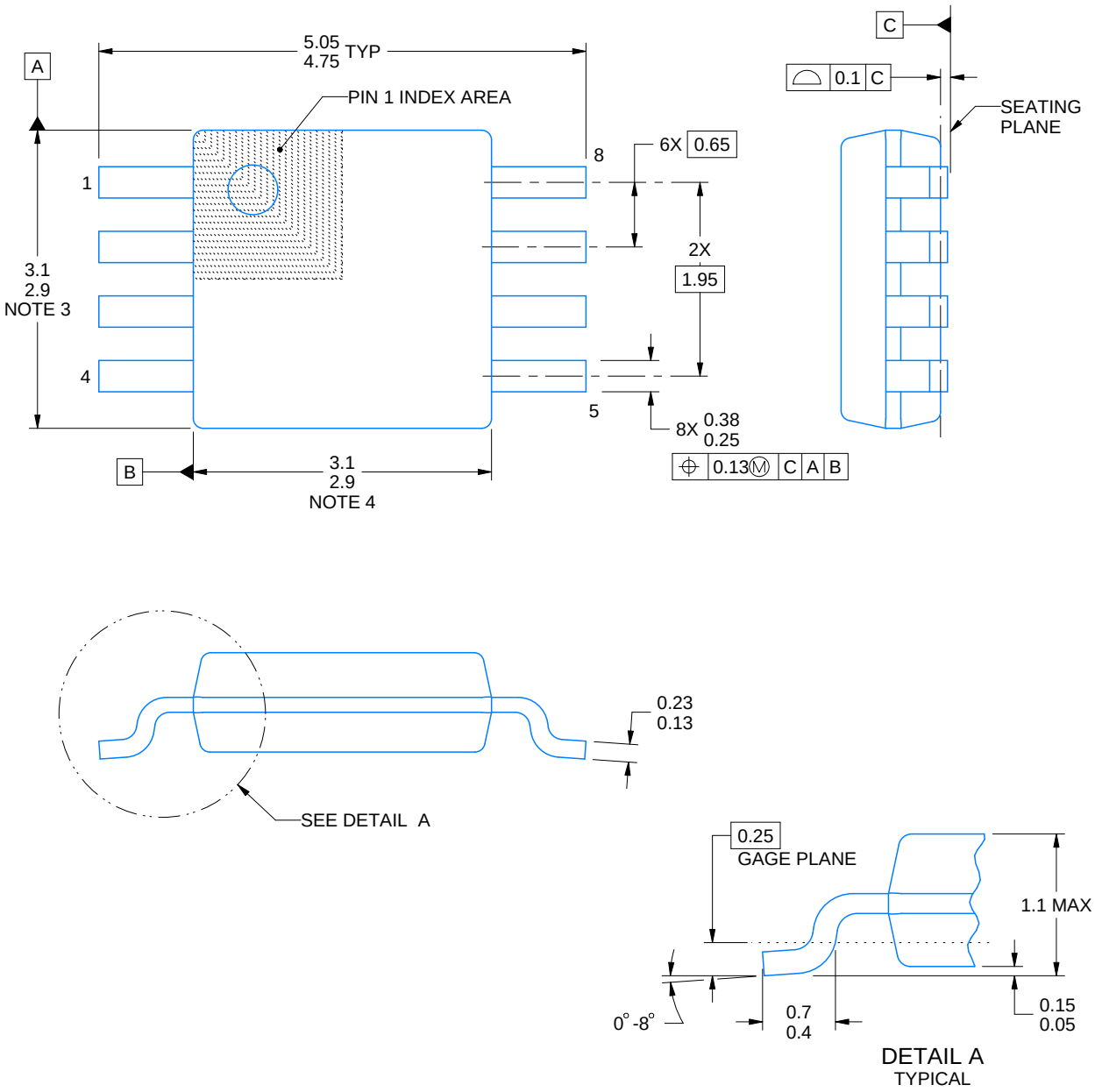
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

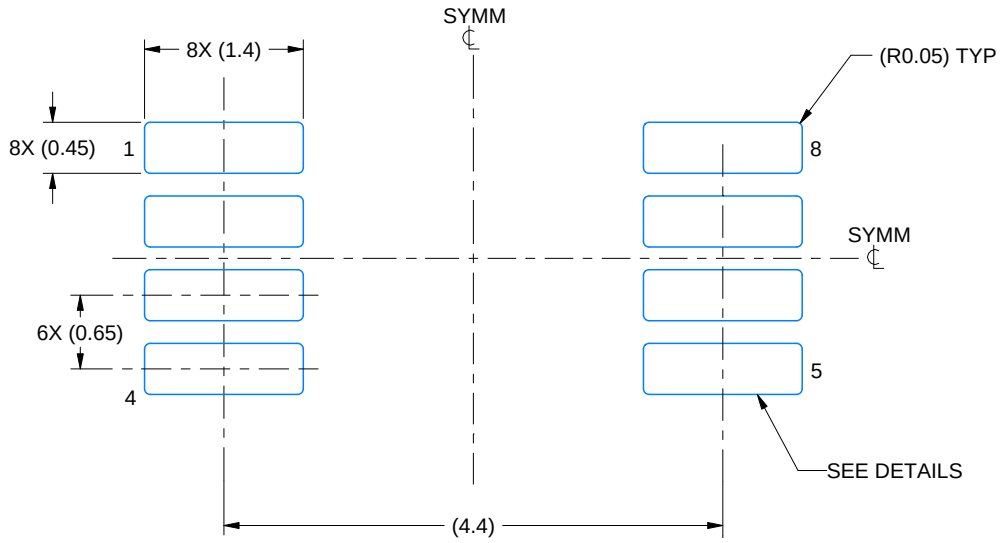
SMALL OUTLINE PACKAGE



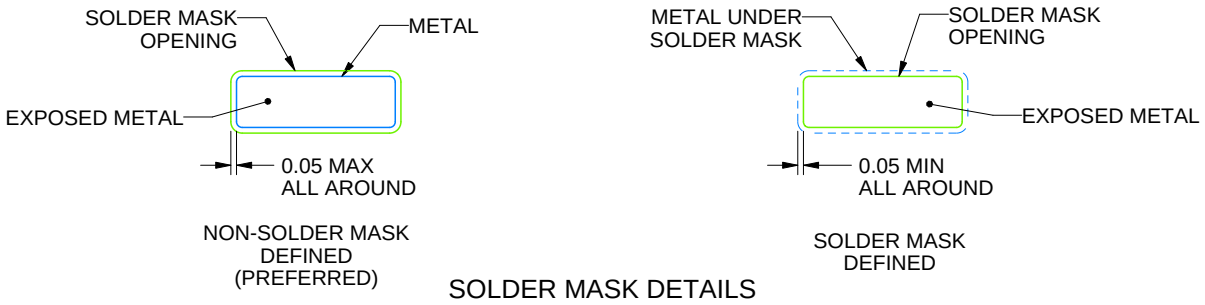
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

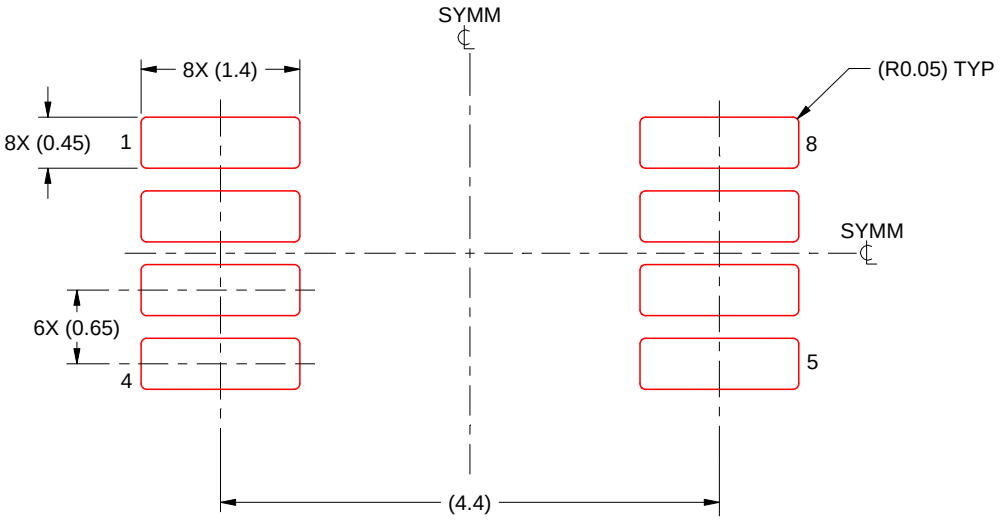


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

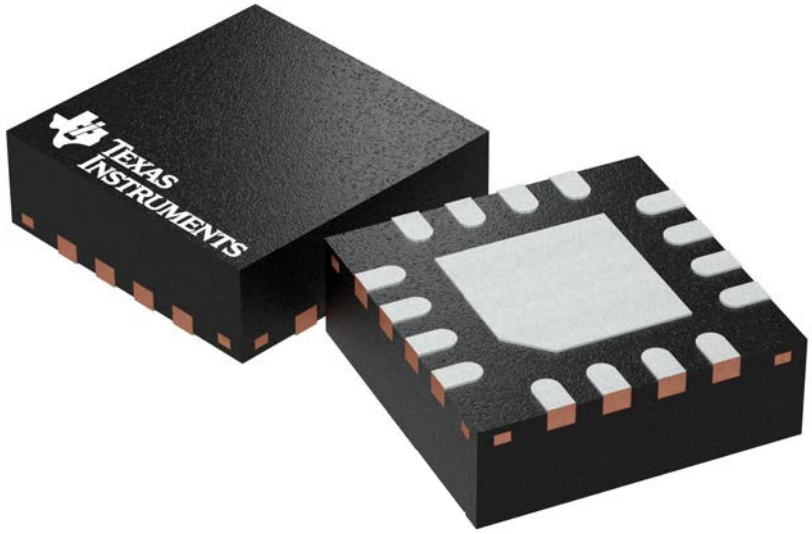
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



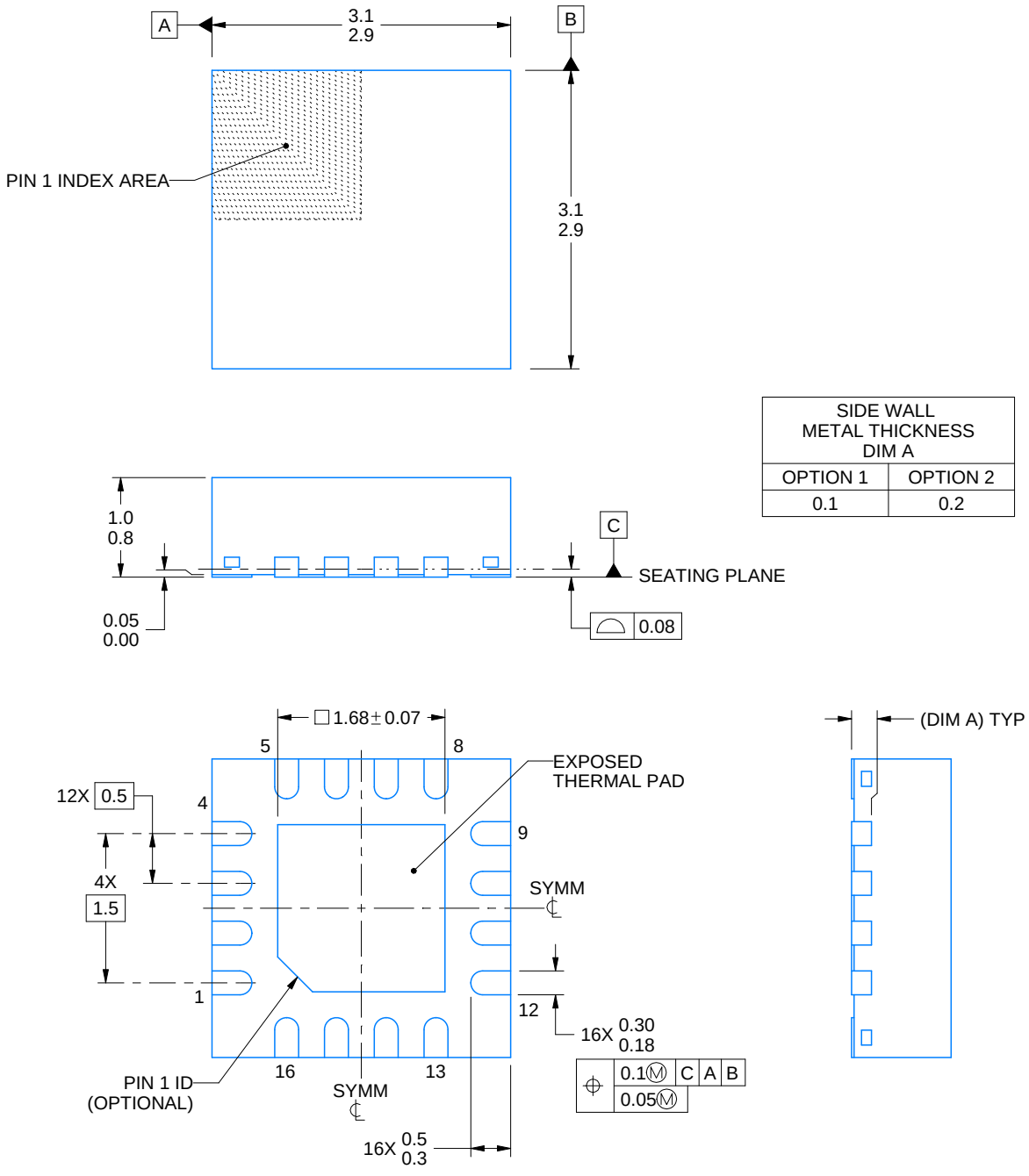
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

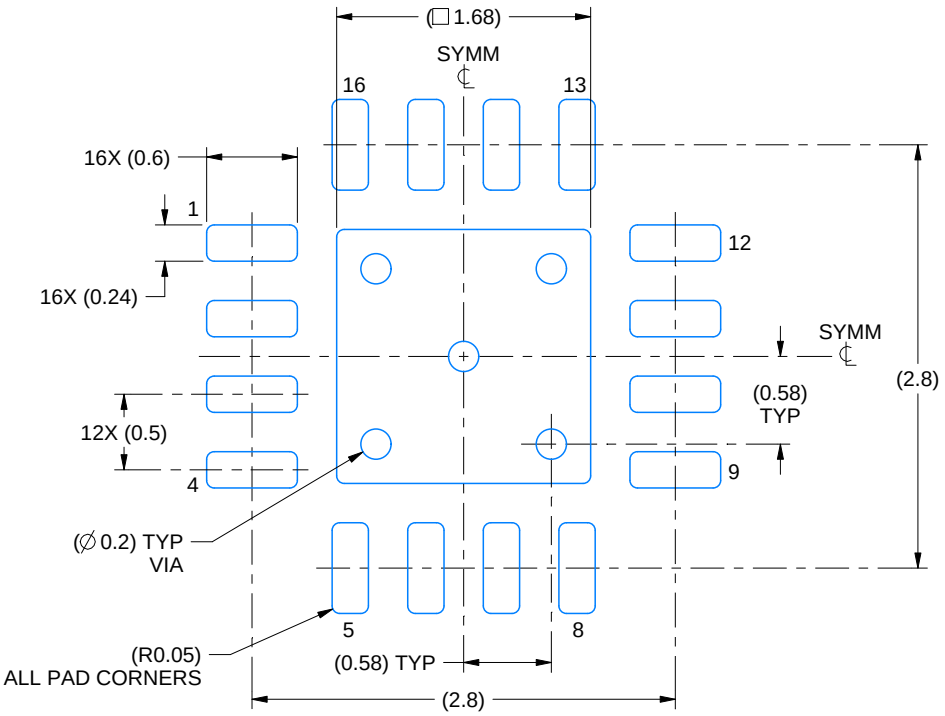
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

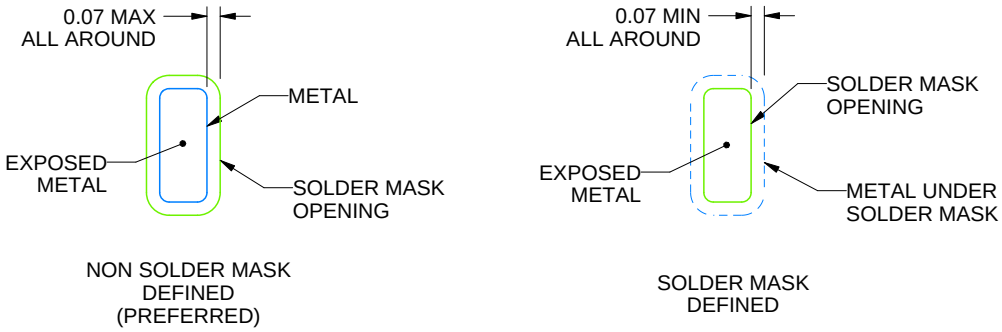


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

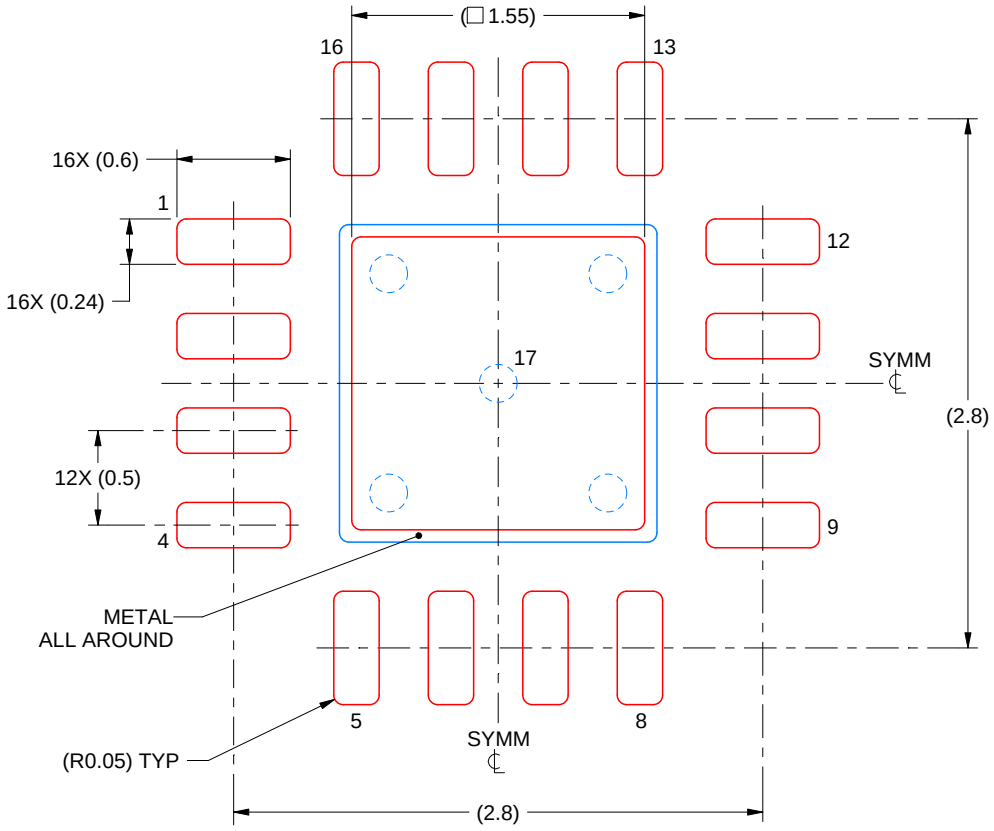


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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