THVD4421 120Ω の切り替え可能終端抵抗と IEC-ESD 保護機能を内蔵したマルチプロトコル (RS-232、RS-422、RS485) トランシーバ

1 特長

- TIA/EIA-485A および TIA/EIA-232F 規格の要件に適合またはそれを上回る性能
- RS-232 仕様のトランスミッタ 2 個とレシーバ 2 個
- RS-485 仕様のトランスミッタ 1 個とレシーバ 1 個
- RS-485 モード用のオンチップの切り替え可能な 120Ω 終端抵抗
- RS-232 信号伝送用チャージ ポンプを内蔵
- 電源電圧:3V～5.5V
- ロジック データおよび制御信号用の 1.65V～5.5V 電源
- 5V 電源で 2.1V を超える RS-485 差動出力により PROFIBUS に準拠
- RS-232 モードでの大きな出力スイング (代表値 ±9V)
- SLR ピンで選択可能なデータ レート:
  - RS-232 3T5R モード:250kbps、1Mbps
  - RS-485 の半二重および全二重モード:500kbps、20Mbps
- バス I/O 保護
  - ±16kV HBM ESD
  - ±8kV IEC 61000-4-2 接触および ±15kV 気中放電
  - ±4kV IEC 61000-4-4 高速過渡バースト
- RS-232 モードに対する診断ループバック
- ディセーブル状態でシャットダウン ピン使用により大幅に消費電流を低減 (標準値 10µA)
- グリッチのない電源投入 / 切断によるホット プラグイン機能
- RS-485 仕様の 1/8 単位負荷 (最大 256 個のバス ノード)
- RS-485 レシーバに対する開放、短絡、アイドル バスのフェイルセーフ
- バス短絡保護、サーマル シャットダウン
- 拡張周囲温度範囲:-40℃～125℃
- 省スペースで熱効率の高い 5mm × 5mm VQFN-32 パッケージ

2 アプリケーション

- 産業用 PC
- ファクトリ オートメーション / 制御
- HVAC システム
- ビル オートメーション
- POS 端末
- グリッド インフラ
- 産業用輸送

3 概要

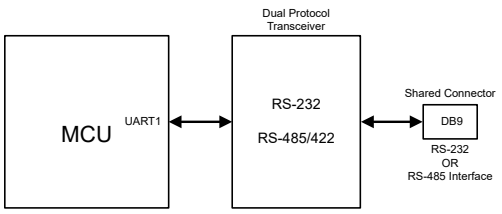
THVD4421 は、RS-232、RS-422、RS-485 の各物理層をサポートする、高集積で堅牢なマルチプロトコル トランシーバです。このデバイスは、2 つのトランスミッタと 2 つのレシーバを搭載しており、2T2R RS-232 ポートを実現します。また、このデバイスには 1 つのトランスミッタと 1 つのレシーバが内蔵されており、半二重と全二重の RS-485 ポートを実現できます。モード選択ピンにより、プロトコルの共有バスおよびロジック ピンが共通の単一のコネクタを共有できるようになります。RS-485 バス ピンと RS-232 レシーバ入力の終端が内蔵されているため、外付け部品なしで完全な機能を持つ通信ポートを実現できます。これらのデバイスはスルーレート選択機能を備えています。このスルーレート選択機能を使うと、SLR ピンの設定に基づいて 2 つの最大速度でこれらのデバイスを使うことができます。

レベル 4 IEC ESD 保護機能を内蔵しているため、システムレベルの外部保護部品は不要です。RS-232 には、ロジックからバスへ、およびバスからロジック パスへの機能の完全性をチェックし、また、ケーブルとコネクタの短絡をチェックする、診断ループバック モードが搭載されています。さらに、RS-485 レシーバのフェイルセーフ機能は、バス入力が開放または短絡しているとき、またはバスがアイドル状態のときに、受信したロジック出力をロジック High に駆動します。シャットダウン モードの消費電流は非常に小さく (代表値 10µA)、消費電力の制約が厳しいアプリケーションに最適です。このデバイスには、RS-232 用のチャージ ポンプ、および RS-232 と RS-485 の両方のドライバ / レシーバに電力を供給する 3V～5.5V の電源が必要です。独立したロジック電源 V_{IO} (1.65V～5.5V) により、低レベルのマイクロコントローラとのインターフェイスが可能です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
THVD4421	VQFN (32)	5mm × 5mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



THVD4421 の概略回路図

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4 Pin Configuration and Functions

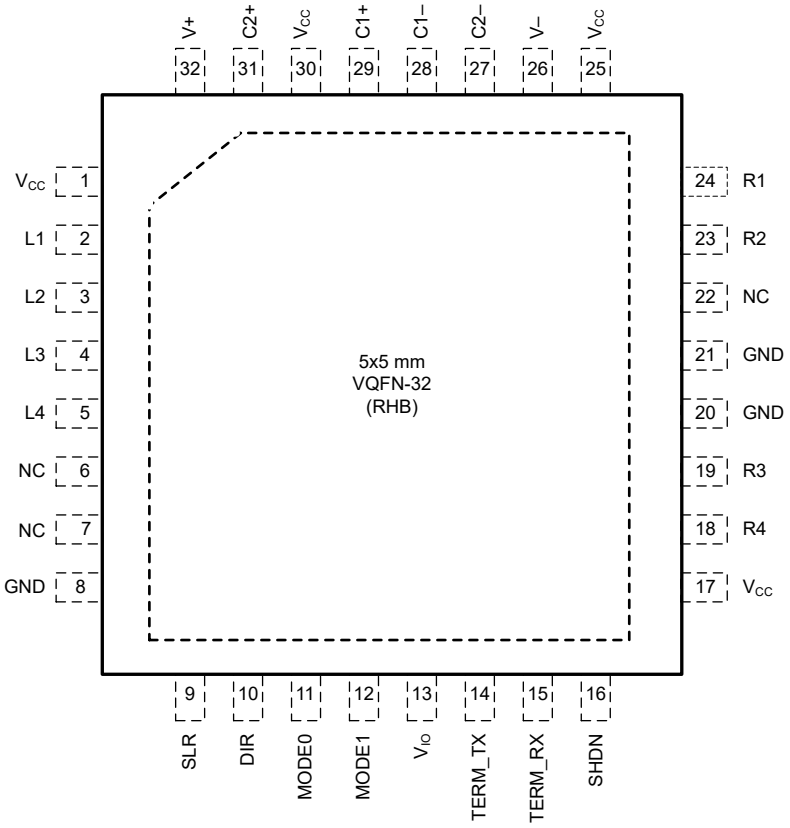


図 4-1. THVD4421
32-Pin VQFN Package (RHB)
Top View

表 4-1. Pin Functions

NAME	NO.	TYPE	DESCRIPTION
V_{CC}	1	P	3V to 5.5V supply voltage
L1	2	O	Logic output
L2	3	O	Logic output (RS-232/RS-485)
L3	4	I	Logic input (RS-232/RS-485)
L4	5	I	Logic input
NC	6		Not connected internally. Can be left open or Grounded on PCB.
V_{CC}	7	P	3V to 5.5V supply voltage
GND(1)	8	G	Ground
SLR	9	I	Slew rate control, internal pull-down. SLR=H enables slow speed (250kbps for RS-232, 500kbps for RS-485)
DIR	10	I	RS-485 TX/RX enable/disable. Internal pull-down
MODE0	11	I	MODE control pins
MODE1	12	I	
V_{IO}	13	P	1.65V to 5.5V logic supply voltage
TERM_TX	14	I	120Ω Termination enable/disable across R1/R2 terminals. Internal Pull down
TERM_RX	15	I	120Ω Termination enable/disable across R3/R4 terminals. Internal Pull down
$\overline{SHDN}$	16	I	Device enable/disable. Internal pull-down

表 4-1. Pin Functions (続き)

NAME	NO.	TYPE	DESCRIPTION
V_{CC}	17	P	3V to 5.5V supply voltage
R4	18	I/O	RS-232 driver output or RS-485 inverting receiver input (B)
R3	19	I/O	RS-232 driver output or RS-485 non-inverting receiver input (A)
GND(1)	20, 21	G	Ground
NC	22		Not connected internally. Can be left open or Grounded on PCB.
R2	23	I/O	RS-232 receiver input or RS-485 bus pin (Y or A)
R1	24	I/O	RS-232 receiver input or RS-485 bus pin (Z or B)
V_{CC}	25	P	3V to 5.5V supply voltage
V-	26		Negative charge pump rail
C2-	27		Negative terminal of charge pump capacitor
C1-	28		Negative terminal of charge pump capacitor
C1+	29		Positive terminal of charge pump capacitor
V_{CC}	30	P	3V to 5.5V supply voltage
C2+	31		Positive terminal of charge pump capacitor
V+	32		Positive charge pump rail

(1) GND pins 8, 20, 21 all must be grounded on PCB.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Bus supply voltage	V_{CC} to GND	–0.5	6	V
Logic supply voltage	V_{IO} to GND	–0.5	V_{CC} + 0.2	V
Charge pump positive-output supply voltage	V+ to GND	–0.3	14	V
Charge pump negative-output supply voltage	V- to GND	0.3	-14	V
Charge pump capacitor terminals	C1+ to GND	V_{CC} - 0.3	V+	V
Charge pump capacitor terminals	C2+ to GND	-0.3	V+	V
Charge pump capacitor terminals	C1- to GND	-0.3	V_{CC}	V
Charge pump capacitor terminals	C2- to GND	V-	-0.3	V
Bus voltage	Voltage at any bus pin (R1, R2, R3, R4) with respect to GND	–16	16	V
Differential bus voltage	(R1-R2) or (R2-R1), (R3-R4) or (R4-R3) with termination disabled	-22	22	V
Differential bus voltage RS485 mode	(R1-R2) or (R2-R1), (R3-R4) or (R4-R3) with termination enabled	-6	6	V
Input voltage	Range at any logic pin (L3, L4, SLR, $\overline{SHDN}$, TERM_TX, TERM_RX, MODE0, MODE1, DIR)	–0.3	V_{IO} + 0.2	V
Receiver output current	I_O (L1, L2)	–8	8	mA
Storage temperature	T_{stg}	–65	150	°C
Junction temperature	T_J	-40	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals (R1, R2, R3, R4) and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, Device in powered or unpowered state, In powered condition- either shutdown or RS232 or RS485 mode, on chip termination ON or OFF, loopback ON or OFF	Contact discharge, per IEC 61000-4-2	Bus terminals (R1, R2, R3, R4) and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2		±15,000	
$V_{(EFT)}$	Electrical fast transient in RS485 HD or FD mode	Per IEC 61000-4-4	Bus terminals (R1, R2, R3, R4)	±4,000	V

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		V_{CC}	V
$V_{I\ (RS-485)}$	Input voltage at any bus terminal (R1, R2, R3, R4) in RS-485 mode(1)		–7		12	V
V_{ID}	Differential input voltage in RS-485 mode [(R1-R2) or (R2-R1), (R3-R4) or (R4-R3)]		-12		12	V
$V_{I\ (RS-232)}$	Receiver input voltage in RS-232 mode		-15		15	V
V_{IH}	High-level input voltage (L3, L4, SLR, $\overline{SHDN}$, TERM_TX, TERM_RX, MODE0, MODE1, DIR inputs)		0.7*V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (L3, L4, SLR, $\overline{SHDN}$, TERM_TX, TERM_RX, MODE0, MODE1, DIR inputs)		0		0.3*V_{IO}	V
I_O	Output current, driver in RS-485 mode		–60		60	mA
I_{OR}	Output current, receiver	V_{IO} = 1.8 V or 2.5 V	–2		2	mA
I_{OR}	Output current, receiver	V_{IO} = 3.3 V or 5 V	–4		4	mA
R_L	Differential load resistance in RS-485 mode		54	60		Ω
$1/t_{UI}$	Signaling rate in RS-485 mode	SLR = V_{IO}			500	kbps
		SLR = GND or floating			20	Mbps
	Signaling rate in RS-232 mode	SLR = V_{IO}			250	kbps
		SLR = GND or floating			1	Mbps
$1/t_{UI\ (loopback)}$	Signaling rate in RS-232 loopback mode				1	Mbps
T_A (2)	Operating ambient temperature		-40		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver and receiver when the junction temperature reaches 170°C.

5.5 Thermal Information

THERMAL METRIC(1)		THVD4421 RHB (QFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the yes application report.

5.6 Power Dissipation

PARAMETER		TEST CONDITIONS			Typical	Max	UNIT
$P_{D\ (RS-485)}$	Driver outputs externally shorted to receiver inputs, MODE1, MODE0 = 11, DIR = V_{IO}, V_{IO} = V_{CC} = 5.5 V, T_A = 125 °C, L3 = square wave 50% duty	Unterminated, TERM_TX = L, TERM_RX = L	SLR = H	500 kbps	160	200	mW
			SLR = L	20Mbps	390	450	
		TERM_RX = TERM_TX = V_{IO}	SLR = H	500 kbps	430	500	mW
			SLR = L	20Mbps	500	575	

5.6 Power Dissipation (続き)

PARAMETER		TEST CONDITIONS			Typical	Max	UNIT
$P_{D\ (RS-232)}$	RS-232 mode with MODE1, MODE0 = 01	V_{CC} = V_{IO} = 5.5V, R3, R4 bus lines loaded with 3 kΩ, R3 load cap = 1000 pF, L3 toggling	SLR = L	1 Mbps	310	490	mW
		V_{CC} = V_{IO} = 5.5V, R3, R4 bus lines loaded with 3 kΩ, R3 load cap = 2500 pF, L3 toggling	SLR = H	250 kbps	180	200	mW

5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver_RS-485							
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V (See 図 6-1)		1.5	2		V
		R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V, 4.5 V ≤ V_{CC} ≤ 5.5 V (See 図 6-1)		2.1	3		V
		R_L = 100 Ω (See 図 6-2)		2	2.5		V
		R_L = 54 Ω, 4.5 V ≤ V_{CC} ≤ 5.5 V (See 図 6-2)		2.1	3.3		V
		R_L = 54 Ω (See 図 6-2)		1.5	3.3		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 54 Ω or 100 Ω (See 図 6-2)		–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See 図 6-2)			V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See 図 6-2)		–50		50	mV
I_{OS}	Short-circuit output current (bus terminals)	DIR = V_{IO}, -7 V ≤ (V_{R2} or V_{R1}) ≤ 12 V, or R1 shorted to R2		–250		250	mA
I_{OZD}	Driver High impedance output leakage current on R1 and R2 in Full duplex mode	MODE1, MODE0 = 11, TERM_TX = GND, DIR = GND, V_{CC} = GND or 5.5V, V_O = -7V, +12V		-125		125	µA
		MODE1, MODE0 = 11, TERM_TX = V_{IO}, DIR = GND, V_{CC} = 5.5V, V_O = -7V, +12V		- 325		350	µA
Receiver_RS-485							
I_I	Bus input current (termination disabled)	Half and full duplex modes, DIR = 0 V, V_{CC} and V_{IO} = 0 V or 5.5 V	V_I = 12 V		75	125	µA
			V_I = –7 V	–125	–70		µA
I_{RXT}	Receiver bus input leakage current with termination enabled	Full duplex mode, V_{CC} and V_{IO} = 5.5 V, TERM_RX = V_{IO}	VI = - 7 to 12 V	-325		325	µA
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of - 7 V to 12 V			- 70	- 40	mV
V_{TH-}	Negative-going input threshold voltage(1)			–200	–150		mV
V_{HYS}	Input hysteresis			25	80		mV
$C_{A,B}$	Input differential capacitance	Measured between R3 and R4, f = 1 MHz			45		pF
V_{OH}	Output high voltage, L2 pin	I_{OH} = –4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage, L2 pin	I_{OL} = 4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			0.2	0.4	V
V_{OH}	Output high voltage, L2 pin	I_{OH} = –2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage, L2 pin	I_{OL} = 2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V			0.2	0.4	V
I_{OZ}	Output high-impedance current, L2 pin	V_O = 0 V or V_{IO}, DIR = VIO, MODE1, MODE0= 10 (half duplex mode)		–2		2	µA
Driver_RS-232							
V_{OH}	High-level output voltage	All DOUT (R3, R4) at R_L = 3 kΩ to GND, DIN (L3, L4) = GND; V_{CC} = 3 V to 3.6 V		5	5.5	7	V
V_{OL}	Low-level output voltage	All DOUT (R3, R4) at R_L = 3 kΩ to GND, DIN (L3, L4) = V_{IO} ; V_{CC} = 3 V to 3.6 V		–7	–5.5	-5	V

5.7 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT (R3, R4) at R_L = 3 kΩ to GND, DIN (L3, L4) = GND; V_{CC} = 4.5 V to 5.5 V			7.8	9	11	V
V_{OL}	Low-level output voltage	All DOUT (R3, R4) at R_L = 3 kΩ to GND, DIN (L3, L4) = V_{IO} ; V_{CC} = 4.5 V to 5.5 V			–11	–9	-7.7	V
I_{OS}	Short-circuit output current (2)	V_{CC} = 3.6 V	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V	V_O = 0 V					
r_o	Output resistance on R3, R4	V_{CC} = 0 V, V_+ = 0 V, and $V_–$ = 0 V	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current on R3, R4	$\overline{SHDN}$ = GND	V_O = ±12 V	V_{CC} = 3 to 3.6 V			±125	µA
			V_O = ±10 V	V_{CC} = 4.5 to 5.5 V			±125	µA
Receiver_RS-232								
V_{OH}	High-level output voltage L1/L2	I_{OH} = –4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			V_{IO} – 0.5	V_{IO} – 0.2		V
		I_{OH} = –2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V			V_{IO} – 0.46	V_{IO} – 0.2		V
V_{OL}	Low-level output voltage L1/L2	I_{OL} = 4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V					0.4	V
		I_{OL} = 2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V					0.4	V
V_{IT+}	Positive-going input threshold voltage on RS-232 receiver inputs (R1, R2)	V_{CC} = 3.3 V				1.6	2.4	V
		V_{CC} = 5 V				1.9	2.4	V
$V_{IT–}$	Negative-going input threshold voltage on RS-232 receiver inputs (R1, R2)	V_{CC} = 3.3 V			0.6	1.1		V
		V_{CC} = 5 V			0.8	1.4		V
V_{hys}	Input hysteresis on receiver inputs (V_{IT+} – $V_{IT–}$)				0.4	0.5		V
I_{off}	Output leakage current on receiver output pins L1/L2	$\overline{SHDN}$ = 0 V				±0.05	±10	µA
r_I	Input resistance on receiver input pins	-15 V ≤ V_I ≤ 15 V			3	5	7	kΩ
Thermal Protection								
T_{SHDN}	Thermal shutdown threshold	Temperature rising			150	170		°C
T_{HYS}	Thermal shutdown hysteresis					15		°C
Supply								
UV_{VCC} (rising)	Rising under-voltage threshold on V_{CC}					2.5	2.7	V
UV_{VCC} (falling)	Falling under-voltage threshold on V_{CC}				1.9	2.1		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}				100	400		mV
UV_{VIO} (rising)	Rising under-voltage threshold on V_{IO}					1.5	1.6	V
UV_{VIO} (falling)	Falling under-voltage threshold on V_{IO}				1.2	1.4		V
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				85	100		mV

5.7 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC_SHDN}	Supply current in shutdown mode	V_{CC} = 4.5 V to 5.5 V, $\overline{SHDN}$ = GND, all other logic input pins floating, no load on bus, $T_A \le 125$ °C			5	20	µA
		V_{CC} = 3 V to 3.6 V, $\overline{SHDN}$ = GND, all other logic input pins floating, no load on bus, $T_A \le 125$ °C			3	15	µA
		V_{CC} = 4.5 V to 5.5 V, $\overline{SHDN}$ = GND, all other logic input pins floating, no load on bus, $T_A \le 105$ °C			5	15	µA
		V_{CC} = 3 V to 3.6 V, $\overline{SHDN}$ = GND, all other logic input pins floating, no load on bus, $T_A \le 105$ °C			3	10	µA
I_{IO_SHDN}	Logic supply current in shutdown mode	V_{IO} = 1.65 V to 5.5 V, $\overline{SHDN}$ = GND, all other logic input pins floating				2	µA
I_{CC_485}	Supply current (quiescent), V_{CC} = 4.5 V to 5.5 V TERM_RX, TERM_TX= Floating or low, SLR = X	Driver and receiver enabled, DIR = V_{IO}, MODE1, MODE0 = 11 (Full duplex)	No load		1.7	3.4	mA
		Driver enabled, receiver disabled, DIR = V_{IO}, MODE1, MODE0 = 10 (Half duplex)	No load		1.3	2.8	mA
		Driver disabled, receiver enabled, DIR = GND, MODE1, MODE0 = 10 (Half duplex)	No load		0.8	1.5	mA
I_{CC_485}	Supply current (quiescent), V_{CC} = 3 V to 3.6 V TERM_RX, TERM_TX= Floating or low, SLR = X	Driver and receiver enabled, DIR = V_{IO}, MODE1, MODE0 = 11 (Full duplex)	No load		1.5	2.8	mA
		Driver enabled, receiver disabled, DIR = V_{IO}, MODE1, MODE0 = 10 (Half duplex)	No load		1	2.3	mA
		Driver disabled, receiver enabled, DIR = GND, MODE1, MODE0 = 10 (Half duplex)	No load		0.7	1.3	mA
I_{IO_485}	Logic supply current (quiescent), V_{IO} = 3 to 3.6 V TERM_RX, TERM_TX= Floating	Driver disabled, Receiver enabled, SLR = GND, DIR = GND; MODE1, MODE0 = 10 (half duplex)	No load		7	17	µA
		Driver disabled, Receiver enabled, SLR = V_{IO}; DIR = GND; MODE1, MODE0 = 10 (half duplex)	No load		8	21	µA
I_{CCDT_485}	Supply current in RS-485 driver termination mode	Driver enabled with termination ON; MODE1, MODE0 = 11 (full duplex)	DIR= V_{IO}, TERM_TX = V_{IO}		38	50	mA
I_{CCRT_485}	Supply current in RS-485 receiver termination mode	Receiver enabled with termination ON; MODE1, MODE0 = 11 (full duplex)	DIR = GND, TERM_RX = V_{IO}		1	1.5	mA
I_{CC_RS232}	Supply current in RS-232 mode	MODE1, MODE0 = 01, $\overline{SHDN}$ = V_{IO}; other logic inputs floating	No load		3.2	4	mA
$I_{CC\_RS232\_LB}$	Supply current in RS-232 loopback mode	MODE1 = 0, MODE0 = 0; L3 = L4 = static logic high, -40 °C ≤ T_A ≤ 85 °C	No extra load on RS-232 drivers or on logic output		12	14	mA
On-Chip termination resistor_RS-485							
R_{TERM_TX}	120 Ω termination across Driver output R1/R2 terminals	MODE1, MODE0 = 11 (Full duplex) or 10 (half duplex); DIR = GND, TERM_TX = V_{IO}, V_{R2R1} = 2 V, V_{R1} = -7 V, 0 V, 10 V, See 図 6-9		102	120	138	Ω
R_{TERM_RX}	120 Ω termination across receiver output R3/R4 terminals	MODE1, MODE0 = 11 (Full duplex); TERM_RX = V_{IO}, V_{R3R4} = 2 V, V_{R4} = -7 V, 0 V, 10 V, See 図 6-9		102	120	138	Ω
Logic							
I_{IN}	Input current (L3, L4, DIR, $\overline{SHDN}$, SLR, TERM_TX, TERM_RX, MODE1, MODE0)	1.65 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}		-20		5	µA
$V_{IT+(IN)}$	Rising threshold: logic inputs	1.65 V ≤ V_{IO} ≤ 5.5 V			0.6*V_{IO}	0.7*V_{IO}	V
$V_{IT-(IN)}$	Falling threshold: logic inputs			0.3*V_{IO}	0.4*V_{IO}		V
$V_{IN(HYS)}$	Input threshold: logic inputs			0.1*V_{IO}	0.2*V_{IO}		V

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-}.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

5.8 Switching Characteristics_RS-485_500kbps

500-kbps (with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 図 6-3	V_{CC} = 3 to 3.6 V, Typical at 3.3V	210	300	600	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	250	300	600	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3V		250	450	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		250	450	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		V_{CC} = 3 to 3.6 V, Typical at 3.3V		2	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		2	15	ns
t_{PHZ}, t_{PLZ}	Disable time	MODE1, MODE0 = 10 (half duplex) or 11 (full duplex)	See 図 6-4 and 図 6-5		80	150	ns
t_{PZH}, t_{PZL}	Enable time	MODE1, MODE0 = 11 (full duplex): receiver enabled			200	650	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 図 6-6		13	20	ns
t_{PHL}, t_{PLH}	Propagation delay				700	1200	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				10	45	ns
t_{PHZ}, t_{PLZ}	Disable time in half duplex mode	MODE1, MODE0 = 10, TERM_TX = V_{IO}	See 図 6-7		30	80	ns
$t_{PZH(1)}$	Enable time in half duplex mode				60	155	ns
$t_{PZL(1)}$					450	1250	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time from shutdown with TX disabled in full duplex mode	DIR = 0 V; MODE1, MODE0 = 11	See 図 6-8		7	16	µs

(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode

5.9 Switching Characteristics_RS-485_20Mbps

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 図 6-3	V_{CC} = 3 to 3.6 V, Typical at 3.3 V	5	10	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	5	10	15	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{IO} = 1.65 V to 1.95V	14	25	58	ns
			V_{IO} = 3 V to 3.6 V	9	20	46	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		1	3.5	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		1	3.5	ns
t_{PHZ}, t_{PLZ}	Disable time	MODE1, MODE0 = 10 (half duplex) or 11 (full duplex)	See 図 6-4 and 図 6-5		11	65	ns
t_{PZH}, t_{PZL}	Enable time	MODE1, MODE0 = 11 (full duplex): receiver enabled			8	80	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 図 6-6		5	10	ns
t_{PHL}, t_{PLH}	Propagation delay				40	70	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					10	ns

5.9 Switching Characteristics_RS-485_20Mbps (続き)

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHZ}, t_{PLZ}	Disable time in half duplex mode	MODE1, MODE0 = 10, TERM_TX = V_{IO}	See 図 6-7		20	80	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time in half duplex mode				50	160	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time from shutdown with TX disabled in full duplex mode	DIR = 0 V; MODE1, MODE0 = 11	See 図 6-8		4	15	µs

(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode.

5.10 Switching Characteristics, Driver_RS232

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
250 kbps							
	Maximum data rate	R_L = 3 kΩ One DOUT switching	C_L = 2500 pF See 図 6-15	250	500		kbps
t_{PHL}, t_{PHL}	Transmitter propagation delay	R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 2500 pF See 図 6-15		0.8	2	µs
$t_{sk(p)}$	Transmitter Pulse skew(3)				220	600	ns
SR(tr)	Slew rate, transition region	V_{CC} = 3.3 V ± 10%, 5 V ± 10%, R_L = 3 kΩ to 7 kΩ, See 図 6-16	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	
1 Mbps							
	Maximum data rate	R_L = 3 kΩ One DOUT switching, See 図 6-15	C_L = 250 pF, V_{CC} = 3 to 3.6 V	1000			kbps
			C_L = 1000 pF, V_{CC} = 4.5 to 5.5 V	1000			kbps
t_{PLH}, t_{PHL}	Transmitter propagation delay	R_L = 3k to 7 kΩ, See 図 6-15	C_L = 150 pF to 1000 pF		300	800	ns
$t_{sk(p)}$	Pulse skew(3)				25	150	ns
SR(tr)	Slew rate, transition region	R_L = 3k to 7 kΩ, VCC = 4.5 V to 5.5 V	C_L = 150 pF to 1000 pF, See 図 6-16	18		150	V/µs
		R_L = 3k to 7 kΩ, VCC = 3 V to 3.6 V		15		150	V/µs

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V + 0.3 V; V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.11 Switching Characteristics, Receiver_RS232

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
250 kbps						
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 図 6-17		150	550	ns
t_{PHL}	Propagation delay time, high- to low-level output			150	550	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF, See 図 6-17		130	520	ns
t_{PHL}	Propagation delay time, high- to low-level output			130	520	ns
t_{R_232}, t_{F_232}	Rise/fall time (receiver buffer output), V_{IO} = 3 to 5.5 V	C_L = 150 pF, See 図 6-17		20	50	ns
		C_L = 15 pF, See 図 6-17		5	10	ns
	Rise/fall time (receiver buffer output), V_{IO} = 1.65 to 2.75 V	C_L = 150 pF, See 図 6-17		40	90	ns
		C_L = 15 pF, See 図 6-17		10	20	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 図 6-18		6	14	us
t_{dis}	Output disable time			100	200	ns
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF, See 図 6-17		50	135	ns
		C_L = 15 pF, See 図 6-17		50	135	ns

5.11 Switching Characteristics, Receiver_RS232 (続き)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
1 Mbps						
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 図 6-17		150	550	ns
t_{PHL}	Propagation delay time, high- to low-level output			150	550	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF, See 図 6-17		130	520	ns
t_{PHL}	Propagation delay time, high- to low-level output			130	520	ns
t_{R_232}, t_{F_232}	Rise/fall time (receiver buffer output), V_{IO} = 3 to 5.5 V	C_L = 150 pF, See 図 6-17		20	50	ns
		C_L = 15 pF, See 図 6-17		5	10	ns
	Rise/fall time (receiver buffer output), V_{IO} = 1.65 to 2.75 V	C_L = 150 pF, See 図 6-17		40	90	ns
		C_L = 15 pF, See 図 6-17		10	20	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 図 6-18		6	14	us
t_{dis}	Output disable time			100	200	ns
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF, See 図 6-17		50	125	ns
		C_L = 15 pF, See 図 6-17		50	125	ns

(1) Test conditions are C1–C4 = 0.1 µF atV_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.12 Switching Characteristics_MODE switching

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RDY}	Time from Shutdown to RS-232 ready	MODE1, MODE0 = 00 or floating; $\overline{SHDN}$ = GND to V_{IO}; rest of logic input pins floating, V_{CC} = 4.5 V to 5.5 V Time from 50% of rising SHDN to charge pump V-supply reaching -8 V; See 図 6-11		0.05	0.11	ms
		MODE1, MODE0 = 00 or floating; SHDN = GND to V_{IO}; rest of logic input pins floating, V_{CC} = 3 V to 3.6 V Time from 50% of rising SHDN to charge pump V-supply reaching -5 V; See 図 6-11		0.1	0.4	ms
t_{R2_R4}	Time to switch from RS-232 2T2R mode to RS-485 Full duplex mode	L3 = Vio, MODE1 from GND to Vio, MODE0 = Vio; $\overline{SHDN}$ = DIR = $V_{IO;}$ SLR, TERM_TX, TERM_RX= floating; Time from 50% of MODE1 rising edge to R2 reaching 2V; See 図 6-12		0.04	0.1	µs
t_{R4_R2}	Time to switch from RS-485 full duplex mode to RS-232 3T5R mode	L3 = Vio, MODE1 from Vio to GND, MODE0 = Vio; $\overline{SHDN}$ = DIR = $V_{IO;}$ SLR, TERM_TX, TERM_RX= floating; Time from 50% of MODE1 falling edge to R2 reaching 300 mV; See 図 6-12		2	2.1	µs
t_{LP_RS232}	Time to switch from RS-232 loopback mode to normal RS-232 mode	MODE1 = GND, MODE0 from GND to V_{IO}; $\overline{SHDN}$ = V_{IO}, L3 = GND; Time from 50% of MODE0 rising edge to L2 50% rising edge, -40 °C ≤ T_A ≤ 85 °C; See 図 6-13		2	2.4	µs
t_{RS232_LP}	Time to switch from normal RS-232 mode to RS-232 loopback mode	MODE1 = GND, MODE0 from V_{IO} to GND; $\overline{SHDN}$ = V_{IO}, L3 = GND; Time from 50% of MODE0 falling edge to L2 50% falling edge, -40 °C ≤ T_A ≤ 85 °C; See 図 6-13		2	15	µs
t_{FHD_RS485}	Time to switch from RS-485 full duplex to half duplex mode	DIR= V_{IO}, MODE1 = V_{IO}; MODE0 from V_{IO} to GND; $\overline{SHDN}$ = V_{IO}, SLR, TERM_TX, TERM_RX= floating; L3= GND, 10k pull down resistor on L2, Time from 50% of MODE0 falling edge to 50% falling edge on L2; See 図 6-14		0.5	1	µs

5.12 Switching Characteristics_MODE switching (続き)

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HFD_RS485}	Time to switch from RS-485 half duplex to full duplex mode	DIR= V_{IO}, MODE1 = V_{IO}; MODE0 from GND to V_{IO} ; $\overline{SHDN}$ = V_{IO}, SLR, TERM_TX, TERM_RX= floating; L3= GND, 10k pull down resistor on L2, Time from 50% of MODE0 rising edge to 50% rising edge on L2; See 図 6-14		0.5	1	µs

5.13 Switching Characteristics_RS-485_Termination resistor

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

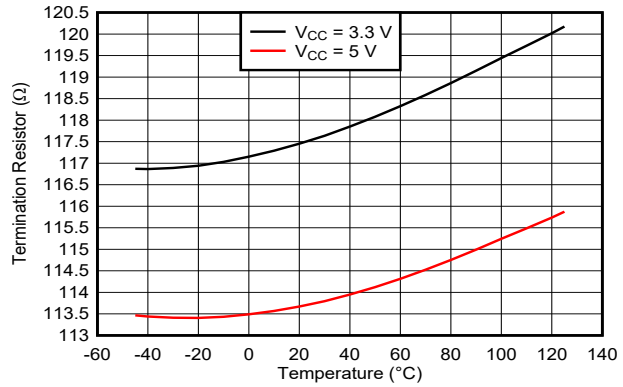
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DTEN}	Driver terminal Termination resistor turn-on time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, DIR = GND, V_{R2R1} = 2 V, V_{R1} = 0 V; See 図 6-10		1000	2200	ns
t_{DTZ}	Driver terminal Termination resistor turn-off time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, DIR = GND, V_{R2R1} = 2 V, V_{R1} = 0 V; See 図 6-10		2000	7200	ns
t_{RTEN}	Receiver terminal Termination resistor turn-on time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, V_{R3R4} = 2 V, V_{R4} = 0 V; See 図 6-10		1000	2200	ns
t_{RTZ}	Receiver terminal Termination resistor turn-off time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, V_{R3R4} = 2 V, V_{R4} = 0 V; See 図 6-10		2000	7200	ns

5.14 Switching Characteristics_Loopback mode

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted.

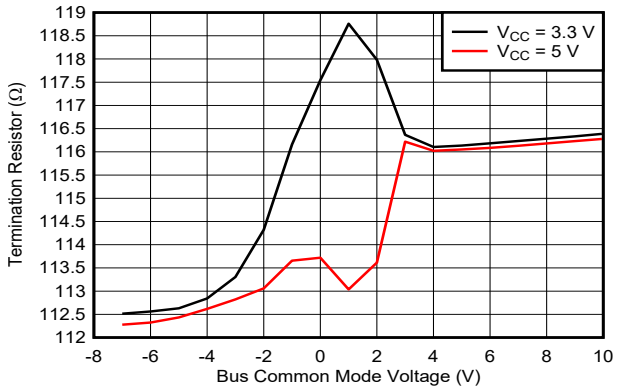
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LB\_RS232\_rising}$	Delay from Logic input rising edge to logic output rising edge in RS-232 Loopback mode	MODE1, MODE0 = GND; SLR = GND, Delay from 50% of L3/L4 rising edge to 50% L2/L1 rising edge, $\overline{SHDN}$ = Vio, TERM_TX and TERM_RX float, Load capacitance on output buffers = 15 pF, R_L on all 2 driver outputs = 3kΩ, -40 °C ≤ T_A ≤ 85 °C		410	920	ns
		MODE1, MODE0 = GND; SLR = Vio, Delay from 50% of L3/L4 rising edge to 50% L2/L1 rising edge, $\overline{SHDN}$ = Vio, TERM_TX and TERM_RX float, Load capacitance on output buffers = 15 pF, R_L on all 2 driver outputs = 3kΩ, -40 °C ≤ T_A ≤ 85 °C		640	1100	ns
$t_{LB\_RS232\_falling}$	Delay from Logic input falling edge to logic output falling edge in RS-232 Loopback mode	MODE1, MODE0 = GND; SLR = GND, Delay from 50% of L3/L4 falling edge to 50% L2/L1 falling edge, $\overline{SHDN}$ = Vio, TERM_TX and TERM_RX float, Load capacitance on output buffers = 15 pF, R_L on all 2 driver outputs = 3kΩ, -40 °C ≤ T_A ≤ 85 °C		570	760	ns
		MODE1, MODE0 = GND; SLR = Vio, Delay from 50% of L3/L4 falling edge to 50% L2/L1 falling edge, $\overline{SHDN}$ = Vio, TERM_TX and TERM_RX float, Load capacitance on output buffers = 15 pF, R_L on all 2 driver outputs = 3kΩ, -40 °C ≤ T_A ≤ 85 °C		600	1460	ns
$t_{SKEW\_RS232\_LB}$	Pulse skew from logic input to logic output in RS232 loopback mode	$\lvert t_{LB\_RS232\_rising} - t_{LB\_RS232\_falling} \rvert$, SLR = Vio, -40 °C ≤ T_A ≤ 85 °C		100	860	ns
		$\lvert t_{LB\_RS232\_rising} - t_{LB\_RS232\_falling} \rvert$, SLR = GND, -40 °C ≤ T_A ≤ 85 °C		70	250	ns

5.15 Typical Characteristics



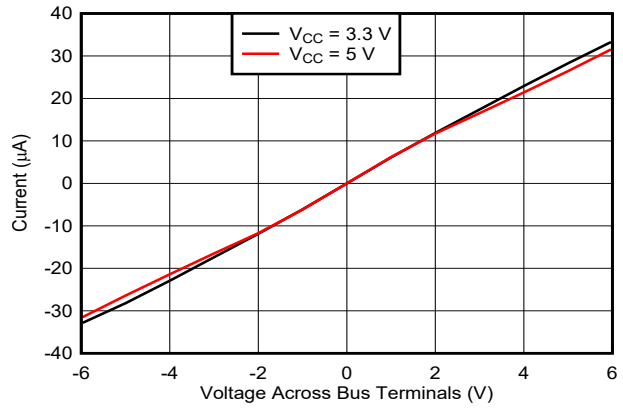
RS-485 Full Duplex mode V(R3-R4) = 2V

図 5-1. RS-485 Termination Resistor vs Temperature



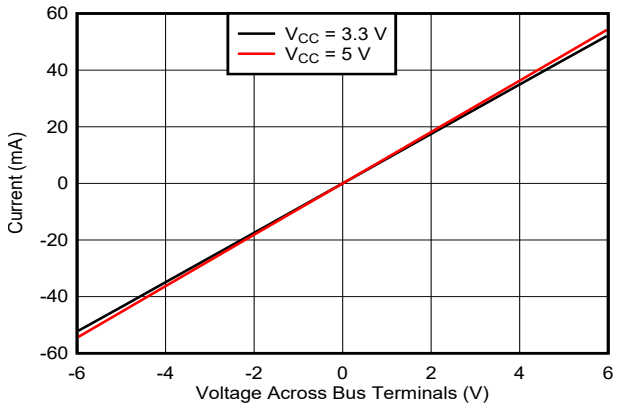
RS-485 Full Duplex mode V(R3-R4) = 2V

図 5-2. Termination Resistor vs Bus Common Mode Voltage



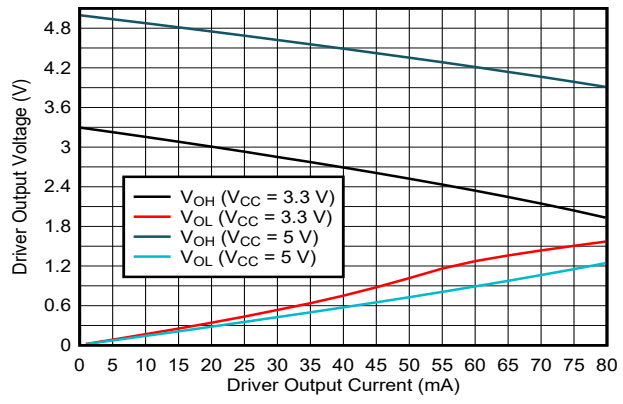
TERM_TX = GND DIR = GND T_A = 25°C

図 5-3. Voltage vs Current across R2-R1 Bus Pins with Termination OFF



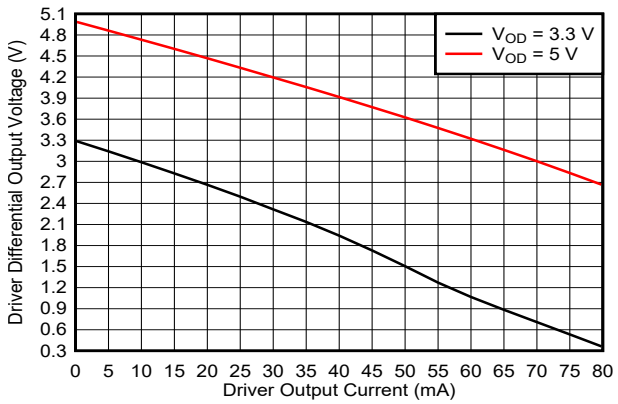
TERM_TX = V_{IO} DIR = GND T_A = 25°C

図 5-4. Voltage vs Current across R2-R1 Bus Pins with Termination ON



DIR = V_{IO} T_A = 25°C

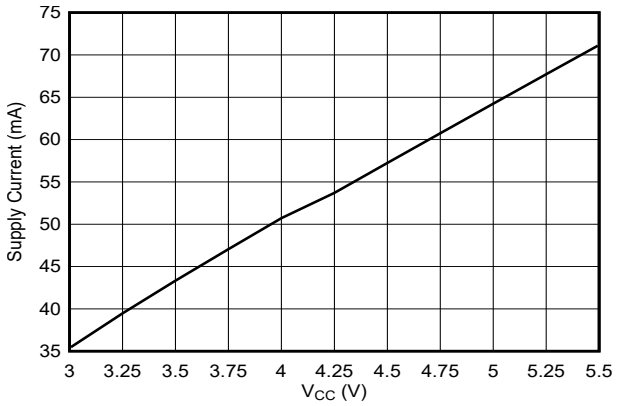
図 5-5. RS-485 Driver Output Voltage vs Driver Output Current



DIR = V_{IO} T_A = 25°C

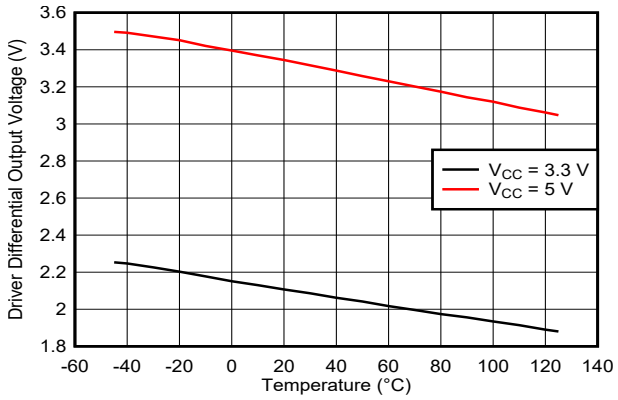
図 5-6. RS-485 Driver Differential Output Voltage vs Driver Output Current

5.15 Typical Characteristics (continued)



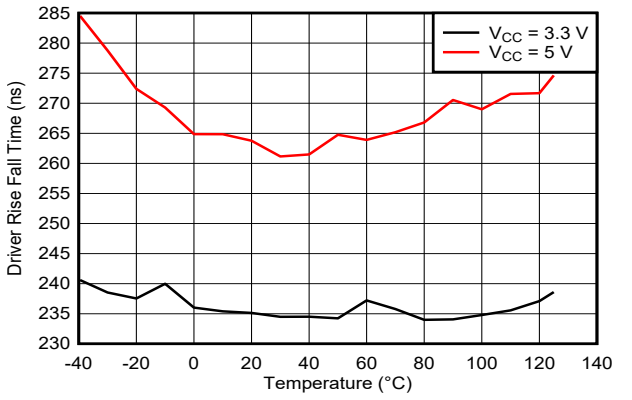
T_A = 25°C R_L = 54Ω DIR = L3 = V_{IO}
RS-485 Full Duplex mode

図 5-7. RS-485 Supply Current vs Supply Voltage



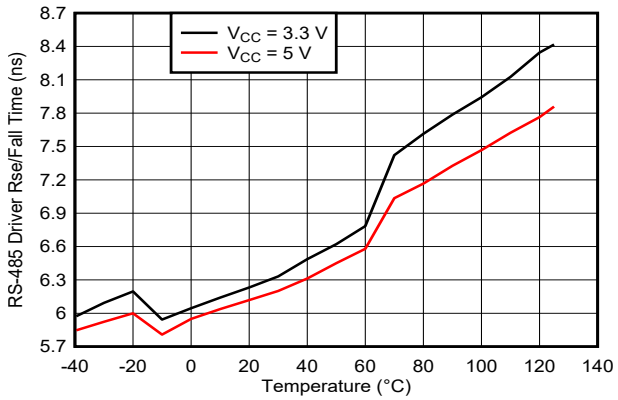
DIR = L3 = V_{IO} R_L = 54Ω
RS-485 Full Duplex mode

図 5-8. RS-485 Driver Differential Output Voltage vs Temperature



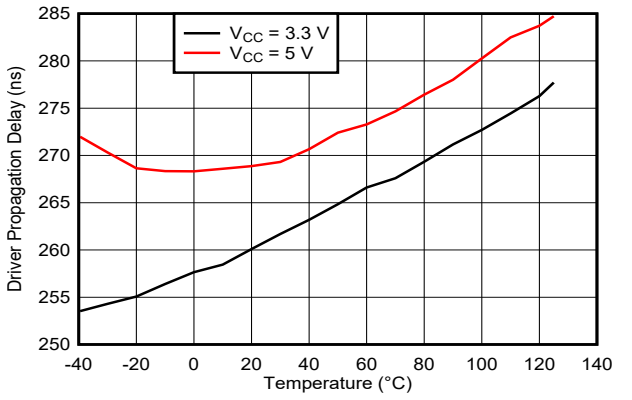
Bus Load = 54Ω ||50 pF SLR = V_{IO} DIR = V_{IO}

図 5-9. RS-485 500kbps Driver Rise or Fall Time vs Temperature



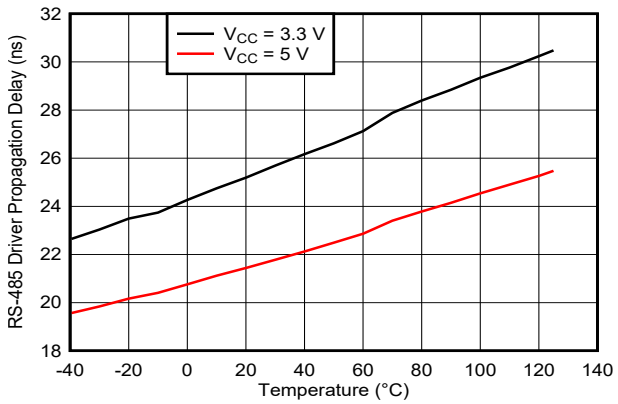
Bus Load = 54Ω || 50pF SLR = GND DIR = V_{IO}

図 5-10. RS-485 20Mbps Driver Rise or Fall Time vs Temperature



Bus Load = 54Ω ||50 pF SLR = V_{IO} DIR = V_{IO}

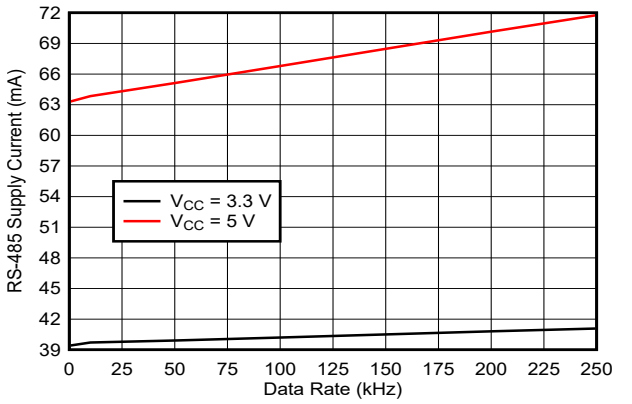
図 5-11. RS-485 500kbps Driver Propagation Delay vs Temperature



Bus Load = 54Ω || 50pF SLR = GND DIR = V_{IO}

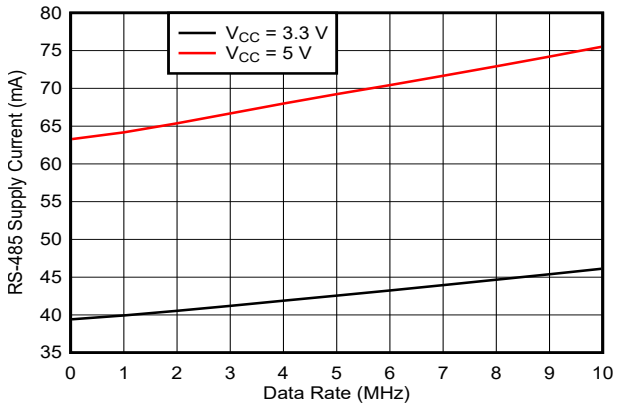
図 5-12. RS-485 20Mbps Driver Propagation Delay vs Temperature

5.15 Typical Characteristics (continued)



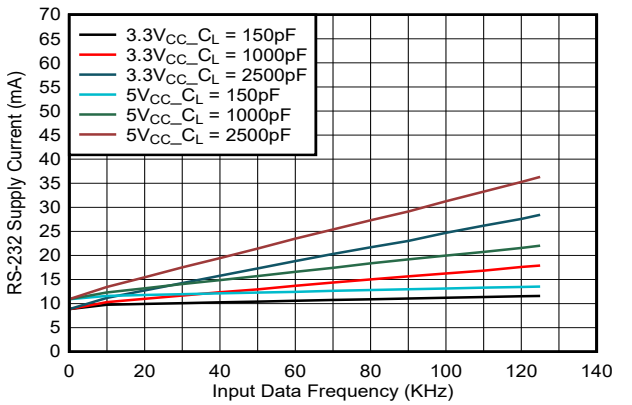
T_A = 25°C R_L = 54Ω DIR = V_{IO}

図 5-13. RS-485 500kbps Supply Current vs Signaling Rate



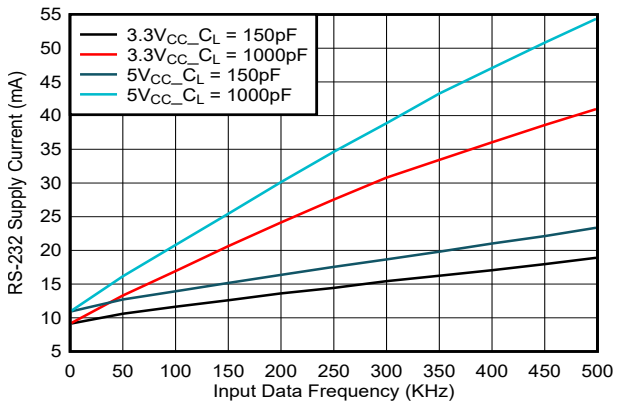
T_A = 25°C R_L = 54Ω DIR = V_{IO}

図 5-14. RS-485 20Mbps Supply Current vs Signaling Rate



T_A = 25°C SLR = V_{IO}
Both drivers loaded with 5kΩ ; device in RS-232 2T2R mode
L4 = static L3 toggling

図 5-15. RS-232 Supply Current vs Signaling Rate for 250 kbps Mode



T_A = 25°C SLR = GND
Both drivers loaded with 5kΩ ; device in RS-232 2T2R mode
L4 = static L3 toggling

図 5-16. RS-232 Supply Current vs Signaling Rate for 1 Mbps Mode

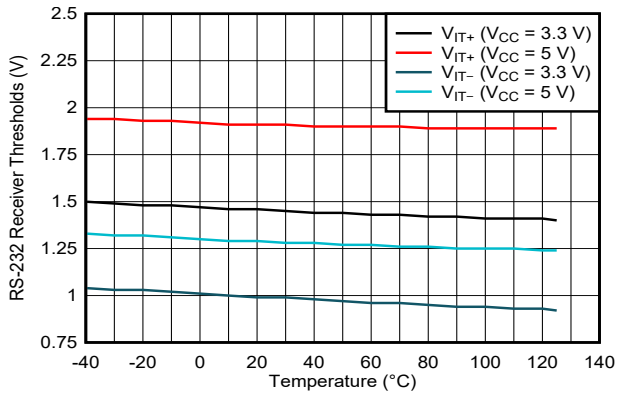


図 5-17. RS-232 Receiver Thresholds vs Temperature

6 Parameter Measurement Information

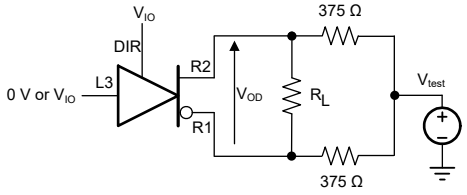


図 6-1. Measurement of RS-485 Driver Differential Output Voltage With Common-Mode Load

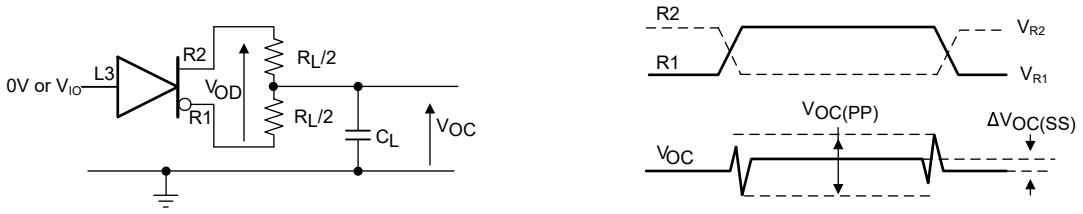


図 6-2. Measurement of RS-485 Driver Differential and Common-Mode Output With RS-485 Load

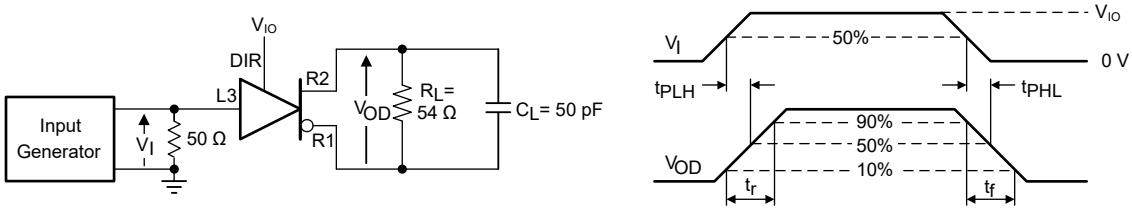


図 6-3. Measurement of RS-485 Driver Differential Output Rise and Fall Times and Propagation Delays

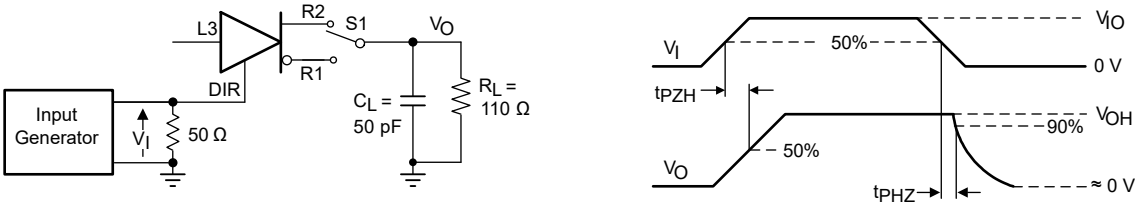


図 6-4. Measurement of RS-485 Driver Enable and Disable Times With Active High Output and Pull-Down Load

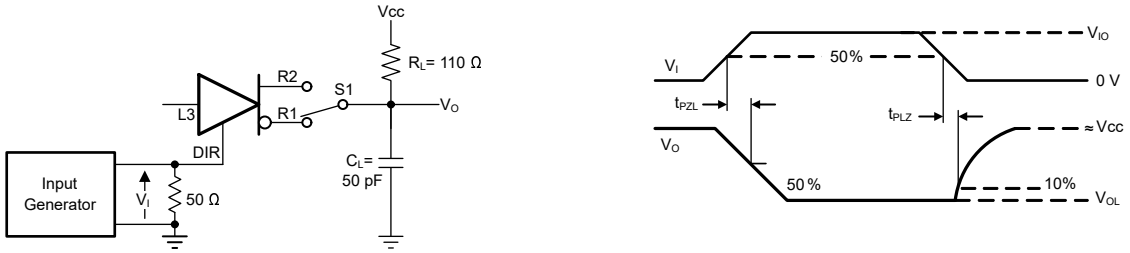


図 6-5. Measurement of RS-485 Driver Enable and Disable Times With Active Low Output and Pull-up Load

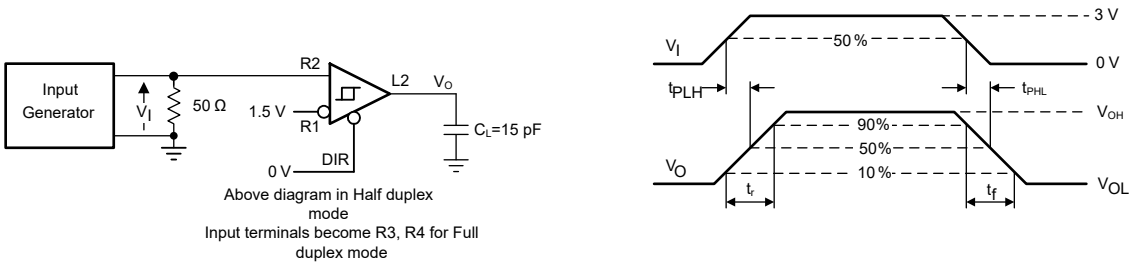


図 6-6. Measurement of RS-485 Receiver Output Rise and Fall Times and Propagation Delays

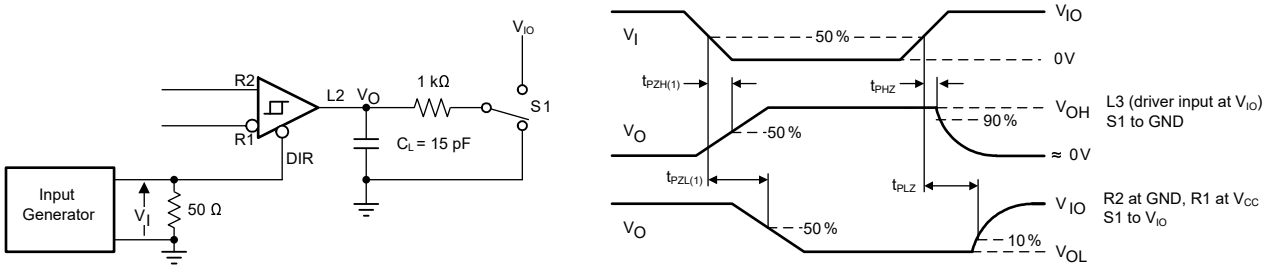


図 6-7. Measurement of RS-485 Receiver Enable/Disable Times in Half Duplex Mode

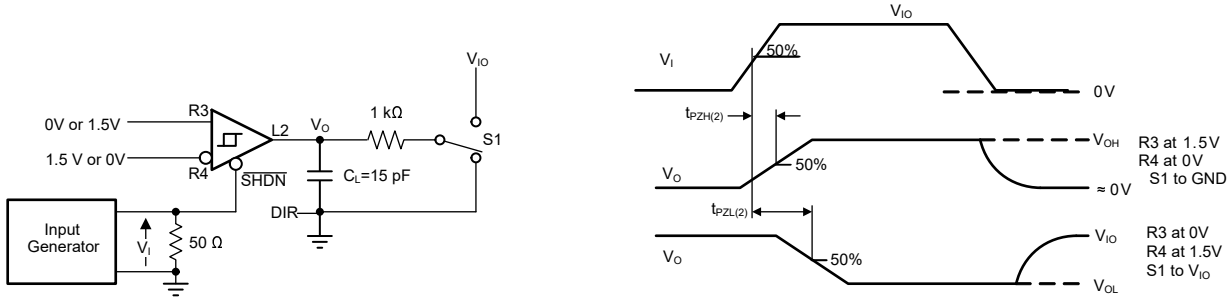


図 6-8. Measurement of RS-485 Receiver Enable Time from Shutdown with TX Disabled: Full duplex Mode

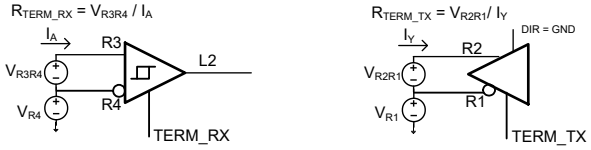


図 6-9. Termination Resistor Measurement

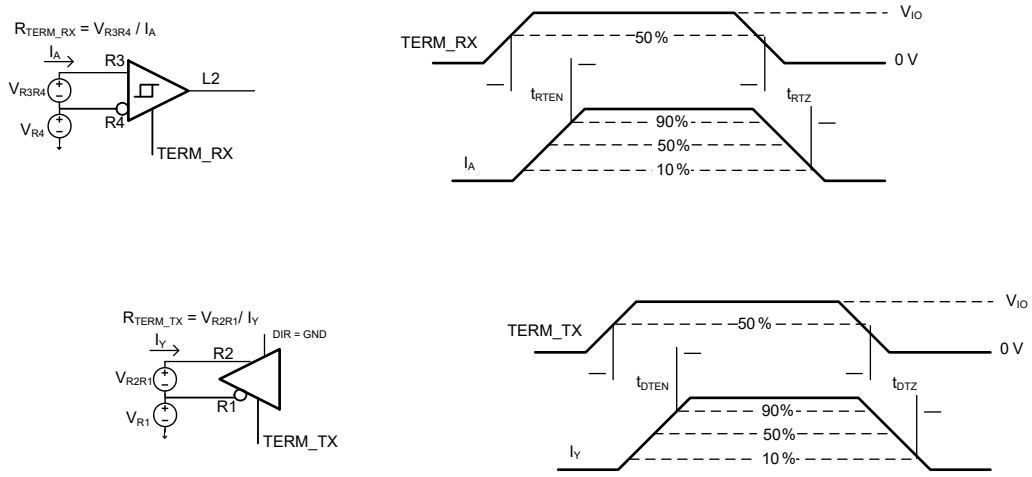


図 6-10. Termination Resistor Switching Measurement

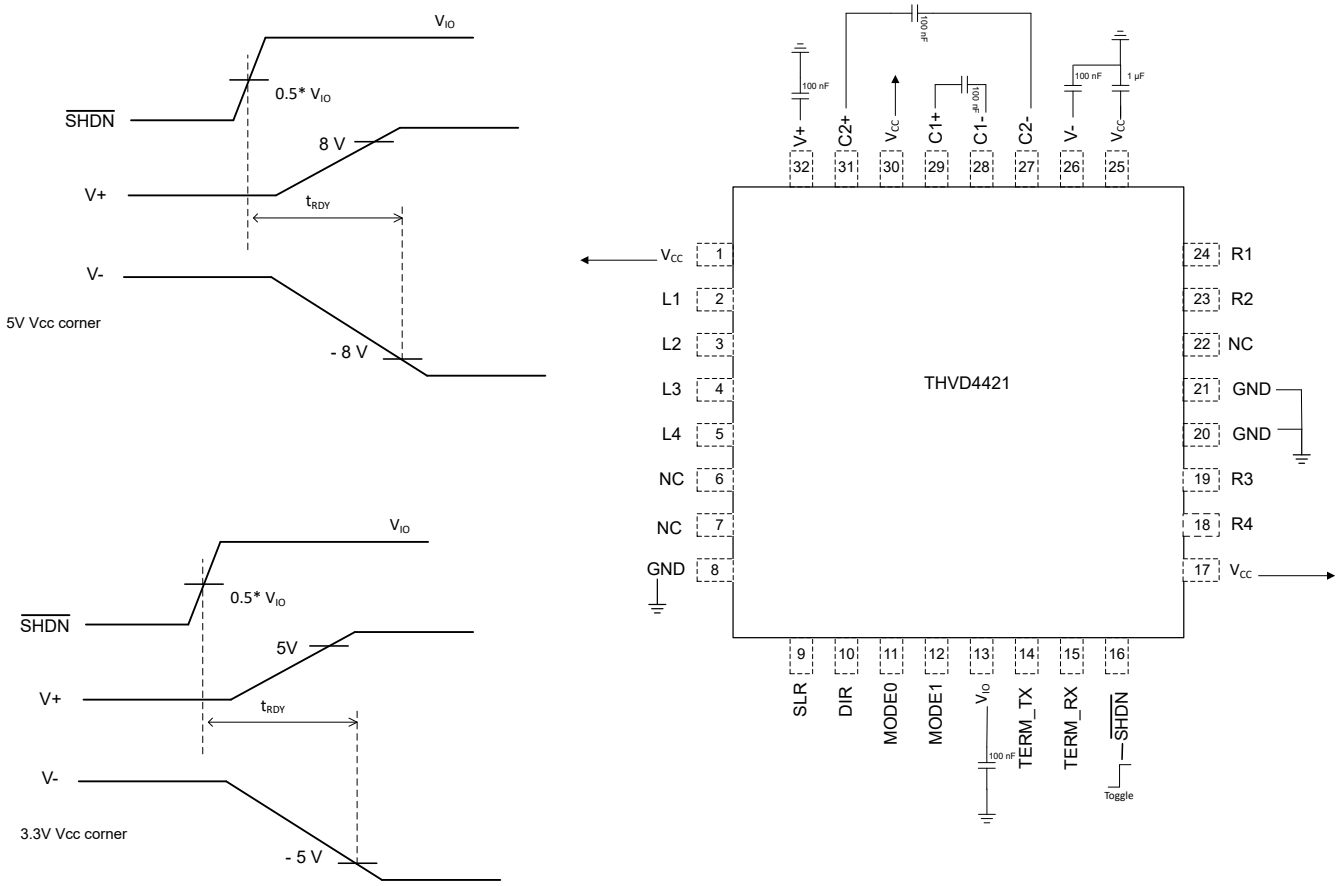


図 6-11. Time from Shutdown to RS-232 Ready

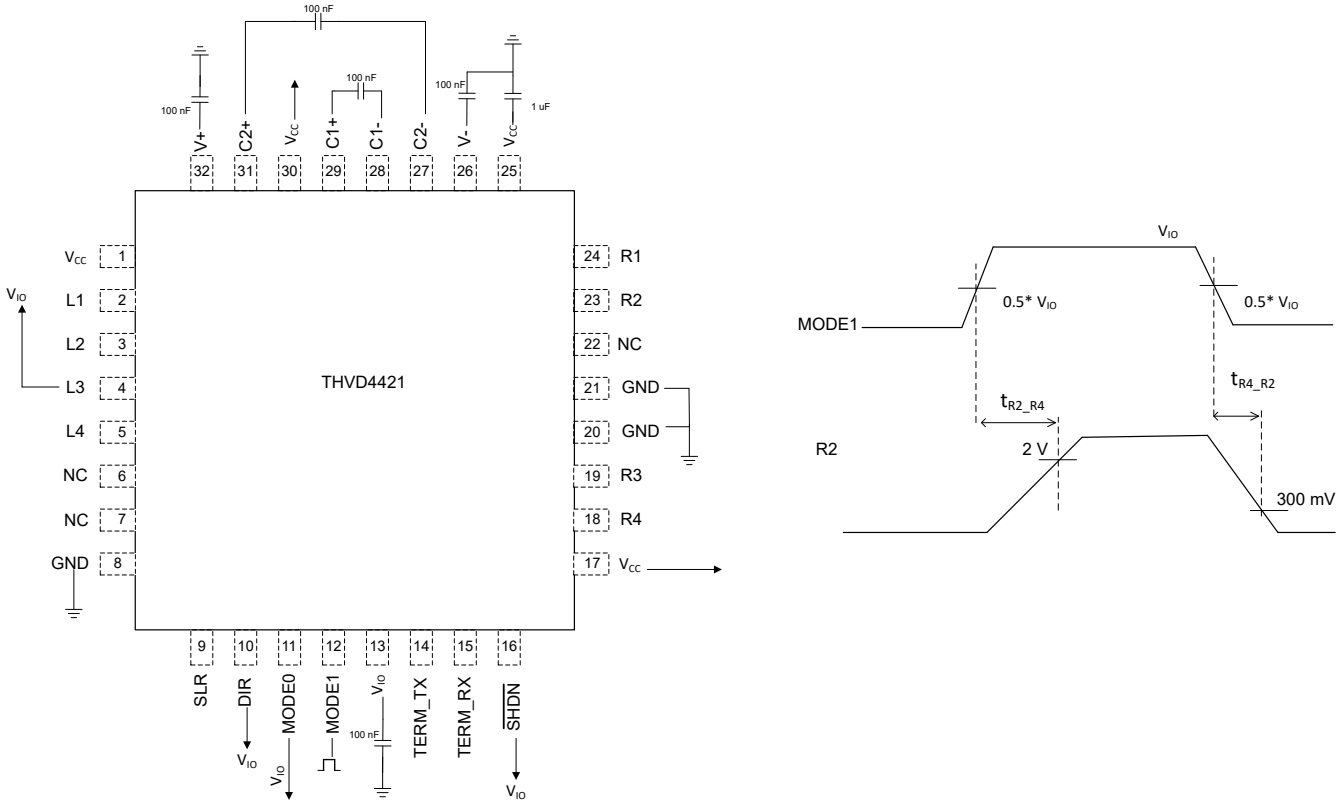


図 6-12. Time to Switch from RS-232 2T2R Mode to RS-485 Full Duplex Mode and Back

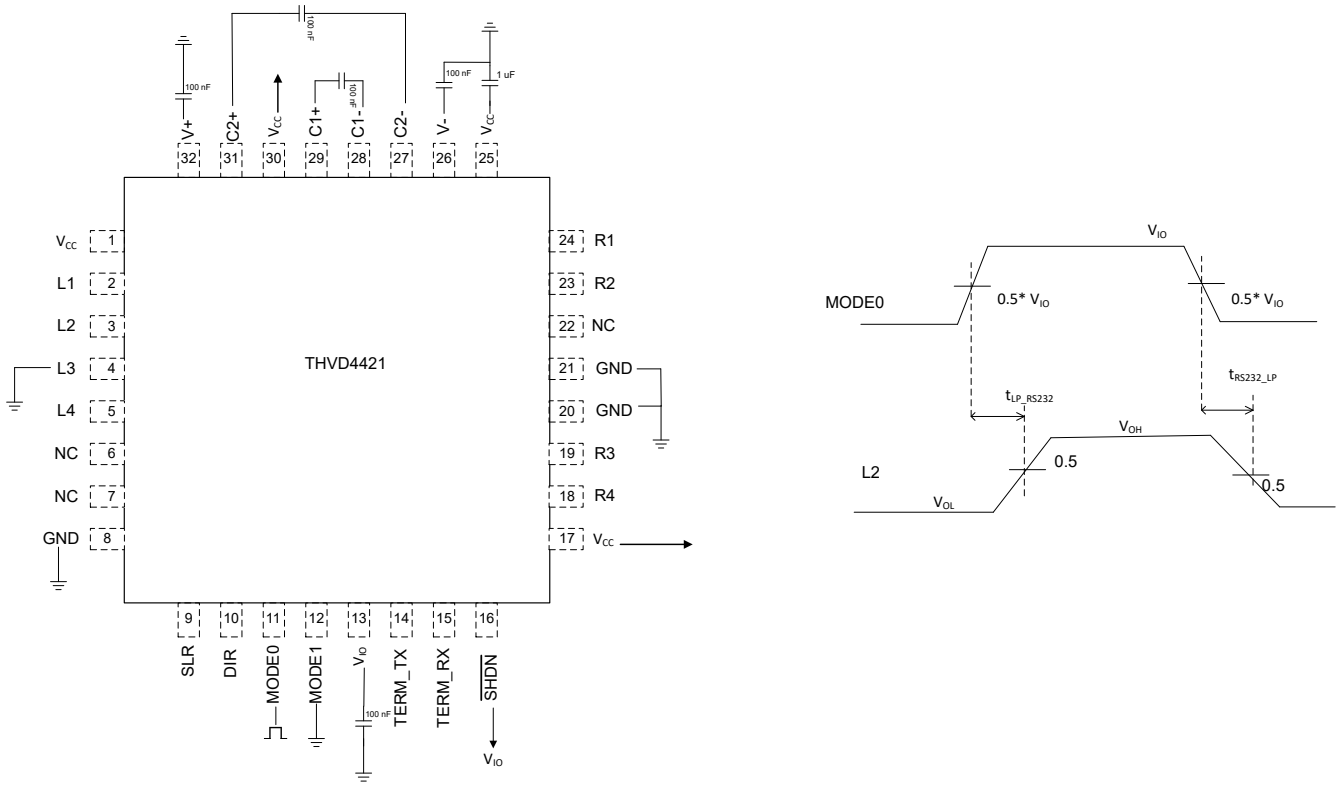


図 6-13. Time to Switch from RS-232 Loopback to Normal RS-232 2T2R Mode and Back

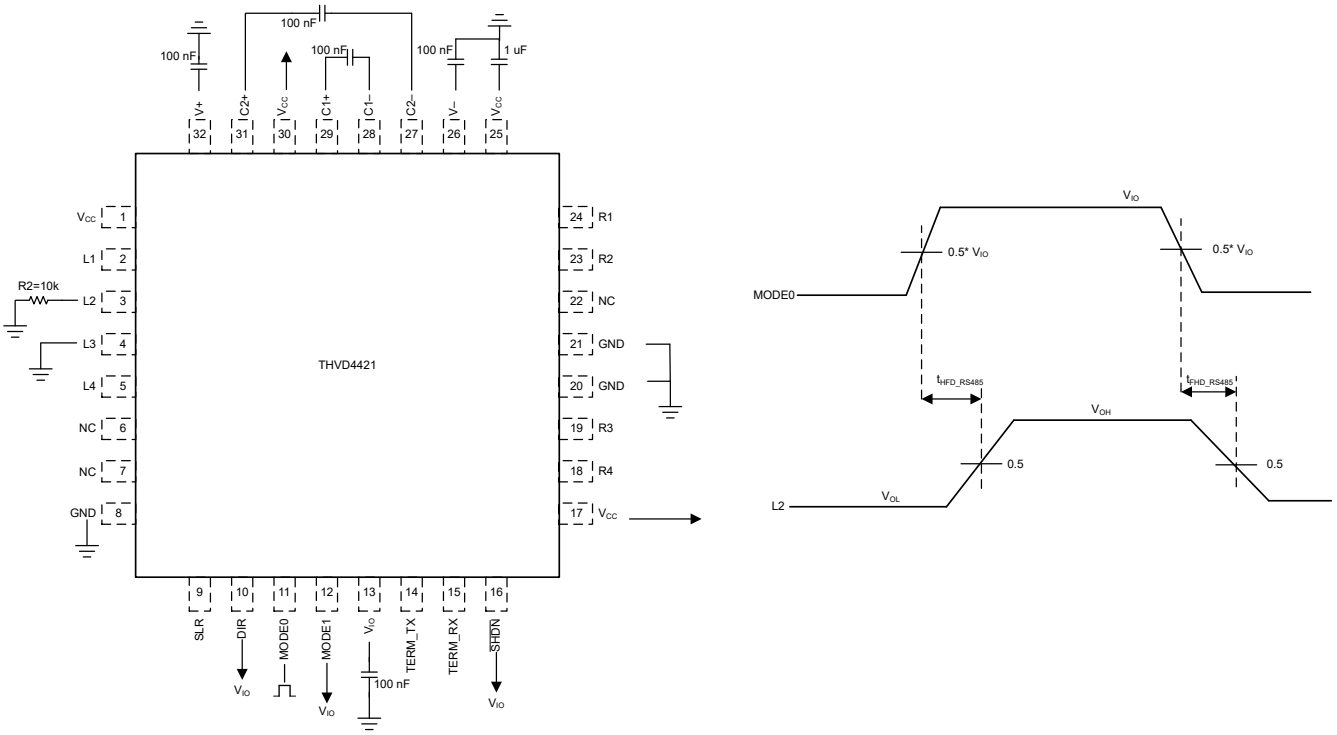
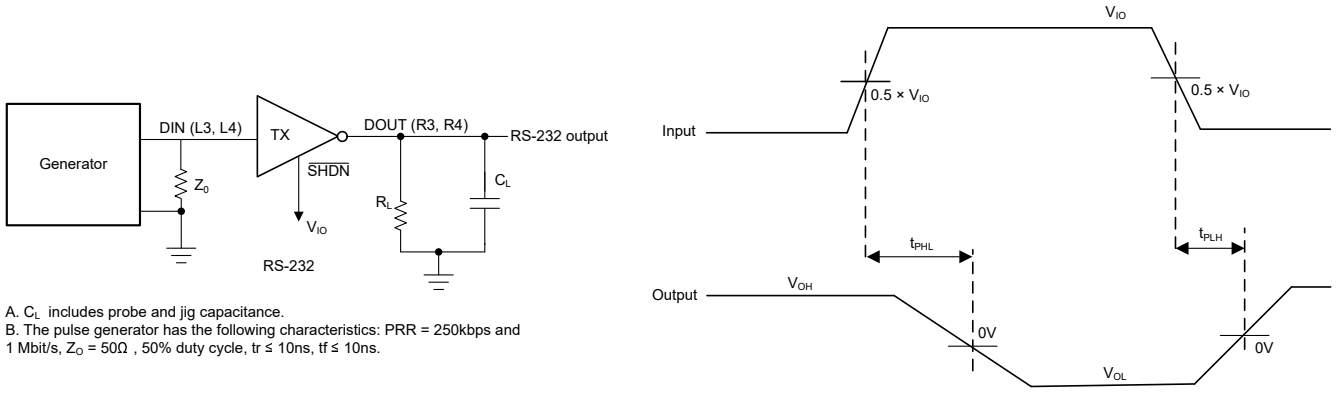
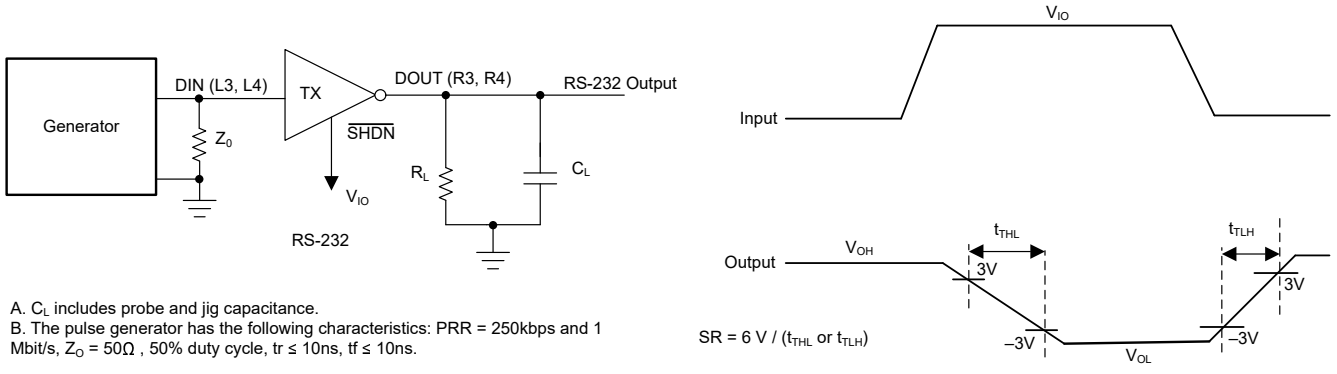


図 6-14. Time to Switch from RS-485 Full Duplex to Half Duplex and Back



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250kbps and 1 Mbit/s, Z_O = 50Ω , 50% duty cycle, tr ≤ 10ns, tf ≤ 10ns.

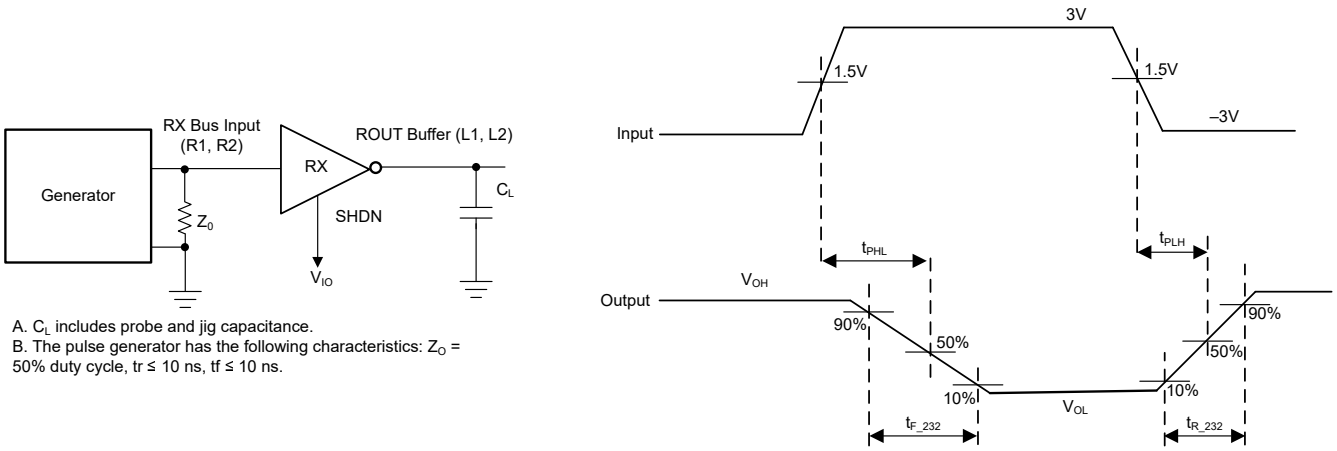
図 6-15. RS-232 Driver Prop Delay, Pulse Skew



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250kbps and 1 Mbit/s, Z_O = 50Ω , 50% duty cycle, tr ≤ 10ns, tf ≤ 10ns.

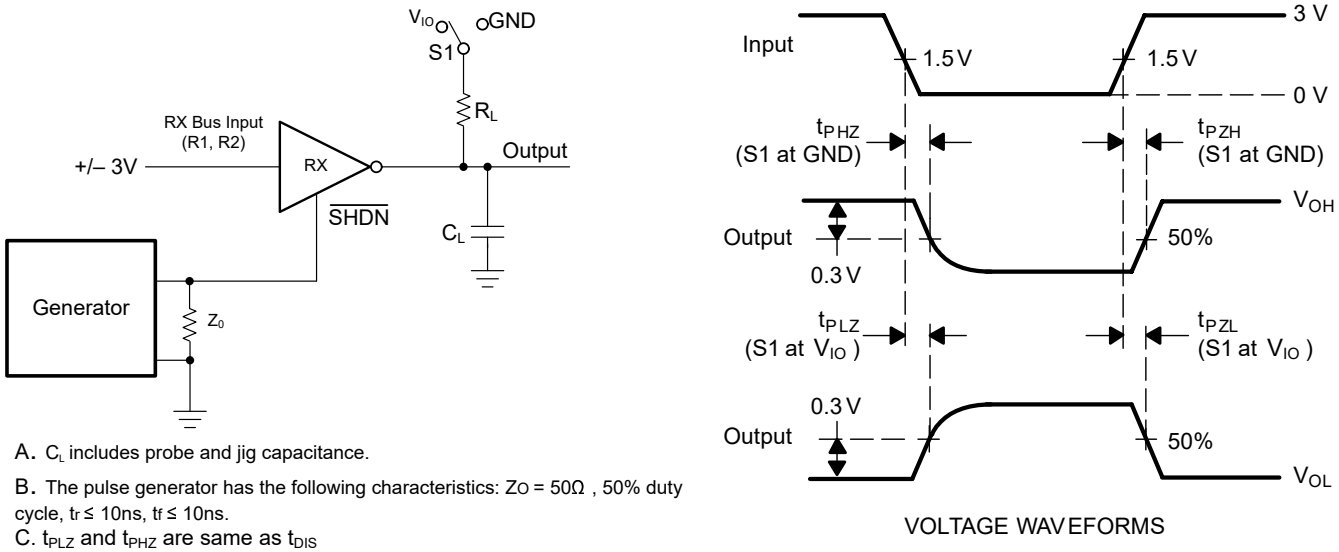
SR = 6 V / (t_{THL} or t_{TLH})

図 6-16. RS-232 Driver Slew Rate



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

図 6-17. RS-232 Receiver Propagation Delay, Pulse Skew



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50Ω , 50% duty cycle, tr ≤ 10ns, tf ≤ 10ns.
C. t_{PLZ} and t_{PHZ} are same as t_{DIS}
D. t_{PZL} and t_{PZH} are same as t_{EN}

図 6-18. RS-232 Receiver Enable and Disable Time

7 Detailed Description

7.1 Overview

THVD4421 is a highly integrated and robust multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layers. The device has two transmitters and two receivers to enable 2T2R RS-232 port. Device also integrates one transmitter and one receiver to enable half and full duplex RS-485 port. The MODE selection pins enable shared bus and logic pins for the protocols to share a common single connector.

The device has SLR pin which allows it to be used for two different maximum speed settings for RS-232 and for RS-485. This is beneficial as customers can qualify one device and use it in two separate end-applications. The devices also have flexible I/O supply pin V_{IO} which enables digital interface voltage range, from 1.65V to 5.5V, different from bus voltage supply 3V to 5.5V.

7.2 Functional Block Diagrams

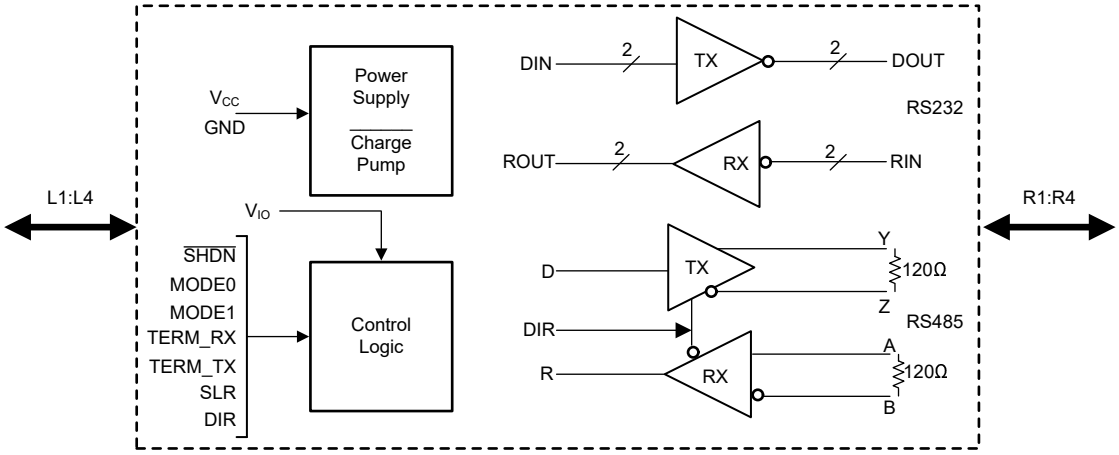


図 7-1. THVD4421 Block Diagram

7.3 Feature Description

7.3.1 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect all the transceiver bus pins (driver and receiver) against electrostatic discharges (ESD) according to IEC 61000-4-2 up to ±8kV for contact discharge and ±15kV (air-discharge) for all operating modes. Bus lines in RS-485 mode can also withstand electrical fast transients (EFT) according to IEC 61000-4-4 for up to ±4kV.

7.3.2 Protection Features

The THVD4421 bus pins are protected against any DC supply shorts in the range of -16V to +16V. In the RS-485 mode, the short circuit current is limited to ±250mA in order to comply with the TIA/EIA-485A standard. In RS-232 mode, current limiting of ±60mA is applicable for scenarios where bus pins can short to ground.

The device also features thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation on-chip.

Supply undervoltage protection is present on both V_{CC} and V_{IO} supplies. This maintains the bus output and receiver logic output in known driven state when both the supplies are above their rising undervoltage thresholds. 表 7-1 describes the device behavior in various scenarios of supply levels.

表 7-1. Supply Function Table

V_{CC}	V_{IO}	Driver Output	Receiver Output
> $UV_{VCC(rising)}$	> $UV_{VIO(rising)}$	For RS-485 mode, determined by DIR and L3 inputs; For RS-232 mode, determined by L3, L4 inputs; For shutdown mode, Hi-Z	For RS-485 mode, determined by DIR and (R1-R2) or (R3-R4) inputs. For RS-232 mode, determined by R1, R2 inputs. For shutdown mode, Hi-Z
< $UV_{VCC(falling)}$	> $UV_{VIO(rising)}$	High impedance	Undetermined
> $UV_{VCC(rising)}$	< $UV_{VIO(falling)}$	High impedance	High impedance
< $UV_{VCC(falling)}$	< $UV_{VIO(falling)}$	High impedance	High impedance

7.3.3 Receiver Fail-Safe Operation

The RS-485 differential receiver of the THVD4421 is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200mV, and must output a low when V_{ID} is more negative than –200mV. The receiver parameters which determine the failsafe performance are V_{TH+}, $V_{TH–}$, and V_{HYS} (the separation between V_{TH+} and $V_{TH–}$). As shown in the Receiver Function table, differential signals more negative than –200mV always causes a low receiver output, and differential signals more positive than 200mV always causes a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{TH+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{TH+}.

7.3.4 Low-Power Shutdown Mode

Driving the $\overline{SHDN}$ pin low puts the device into the shutdown mode. This is the lowest power mode of the device and current consumption is 10µA typical. All the blocks are disabled in this mode.

7.3.5 On-chip Switchable Termination Resistor

THVD4421 has 2 termination resistors of nominal 120Ω, one across R1/R2 and another across R3/R4 in RS-485 mode. Both termination resistors are enabled or disabled using pins as described in 表 7-2. Both the termination resistors can be enabled or disabled independent of the state of driver or receiver. Termination is OFF in RS-232 loopback, RS-232 2T2R, RS-485 loopback, unpowered and thermal shutdown modes.

表 7-2. On-chip Termination Function Table

Signal state	Device mode	Function	Comments
TERM_TX = V_{IO}	Full duplex mode	120Ω enabled between R1 and R2	Termination between R1/R2 is disabled by default
TERM_TX = GND or floating	Full duplex mode	120Ω disabled between R1 and R2	
TERM_RX = V_{IO}	Full duplex mode	120Ω enabled between R3 and R4	Termination between R3/R4 is disabled by default
TERM_RX = GND or floating	Full duplex mode	120Ω disabled between R3 and R4	
TERM_RX = X, TERM_TX = V_{IO}	Half duplex mode	120Ω enabled between R1 and R2	In half duplex mode, TERM_RX is don't care and TERM_TX has higher priority
TERM_RX = X, TERM_TX = GND	Half duplex mode	120Ω disabled between R1 and R2	

On-chip 120Ω termination resistor is designed to have minimum variation with temperature and across common mode voltage on bus pins. Also, the termination block offers a resistive load to the bus, and does not alter the magnitude or phase of the bus signals from DC to 20Mbps signaling.

7.3.6 Operational Data Rate

THVD4421 can be used in slow speed or fast speed RS-485 and RS-232 applications by configuring slew rate control (SLR) pin. 表 7-3 describes slew rate control function.

表 7-3. Slew Rate Control Function Table

Signal state	Driver	Receiver	Comment
SLR = V_{IO}	Maximum speed of operation for RS-485 = 500kbps. Maximum speed of operation in RS-232 mode is 250kbps	Maximum speed of operation for RS-485 = 500kbps. Maximum speed of operation in RS-232 mode is 250kbps	Active high slew rate limiting applied on driver output. In this configuration, glitch filter in receiver path for RS-485 is enabled
SLR = GND or floating	Maximum speed of operation for RS-485= 20Mbps. Maximum speed of operation in RS-232 mode is 1Mbps	Maximum speed of operation for RS-485 = 20Mbps. Maximum speed of operation in RS-232 mode is 1Mbps	Slew rate limiting on driver output disabled.

For RS-485 half and full duplex modes, receiver path in the slow speed mode (500kbps) provides additional noise filtering. To attenuate high frequency noise pulses from the bus which can be wrongly interpreted as valid data, SLR = V_{IO} enables a low pass filter to filter out pulses with frequency higher than typical 800kHz.

7.3.7 Diagnostic Loopback

THVD4421 provides complete diagnostic loopback mode for RS-232. This mode internally shorts bus outputs to bus inputs. So, if data is toggled from logic input, data reaches bus and is reflected back on logic buffer output. This enables MCU to detect bus side short (due to connector and cable) by comparing logic input and logic output.

In RS-232 loopback mode, L3 reflects on L2/R2/R3; L4 reflects on L1/R4/R1; enabling to detect short to ground on all bus pins from R1 through R4. RS-232 loopback mode is optimized for -40°C to 85°C ambient temperature. RS-232 diagnostic loopback can be performed on a node even with another node connected via cable, but listening node is not allowed to transmit anything on the RS232 lines while loopback is ongoing.

7.3.8 Integrated Charge Pump for RS-232

THVD4421 has integrated high-efficiency and low-noise charge pump to generate large output voltages for RS-232 signals. Charge pump consists of a voltage doubler and an inverter to regulate the voltage to nominal ±5.5 V or ±9.5 V for 3.3 V or 5 V V_{CC} operation respectively. Charge pump needs four external ceramic capacitors (2 flying capacitors and 2 storage capacitors) and allows for single supply operation for RS-232. For a generic description of RS-232 charge pump operation, please refer to the blog: How the RS-232 transceiver's regulated charge-pump circuitry works.

7.4 Device Functional Modes

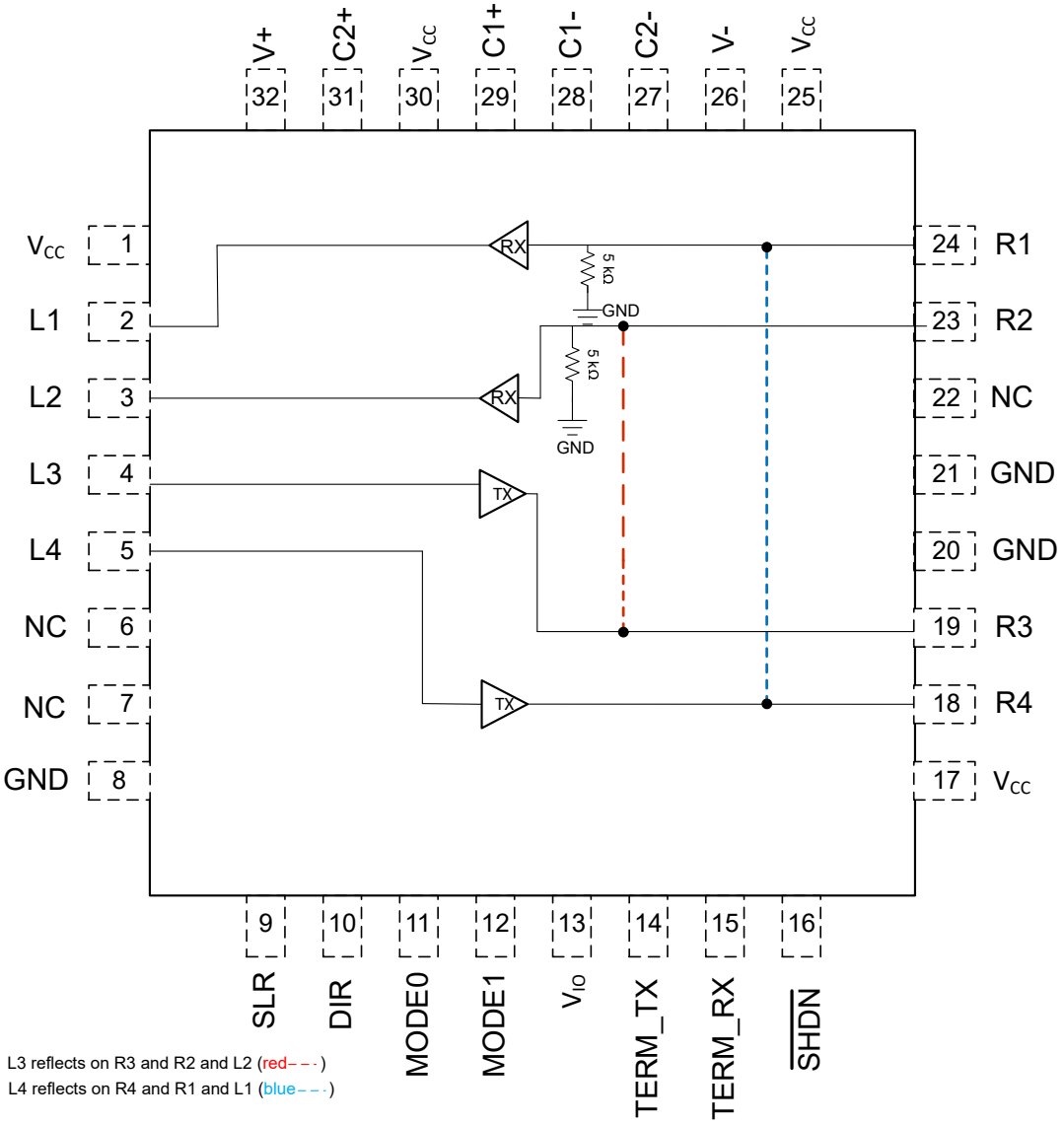


図 7-2. RS-232 Loopback mode

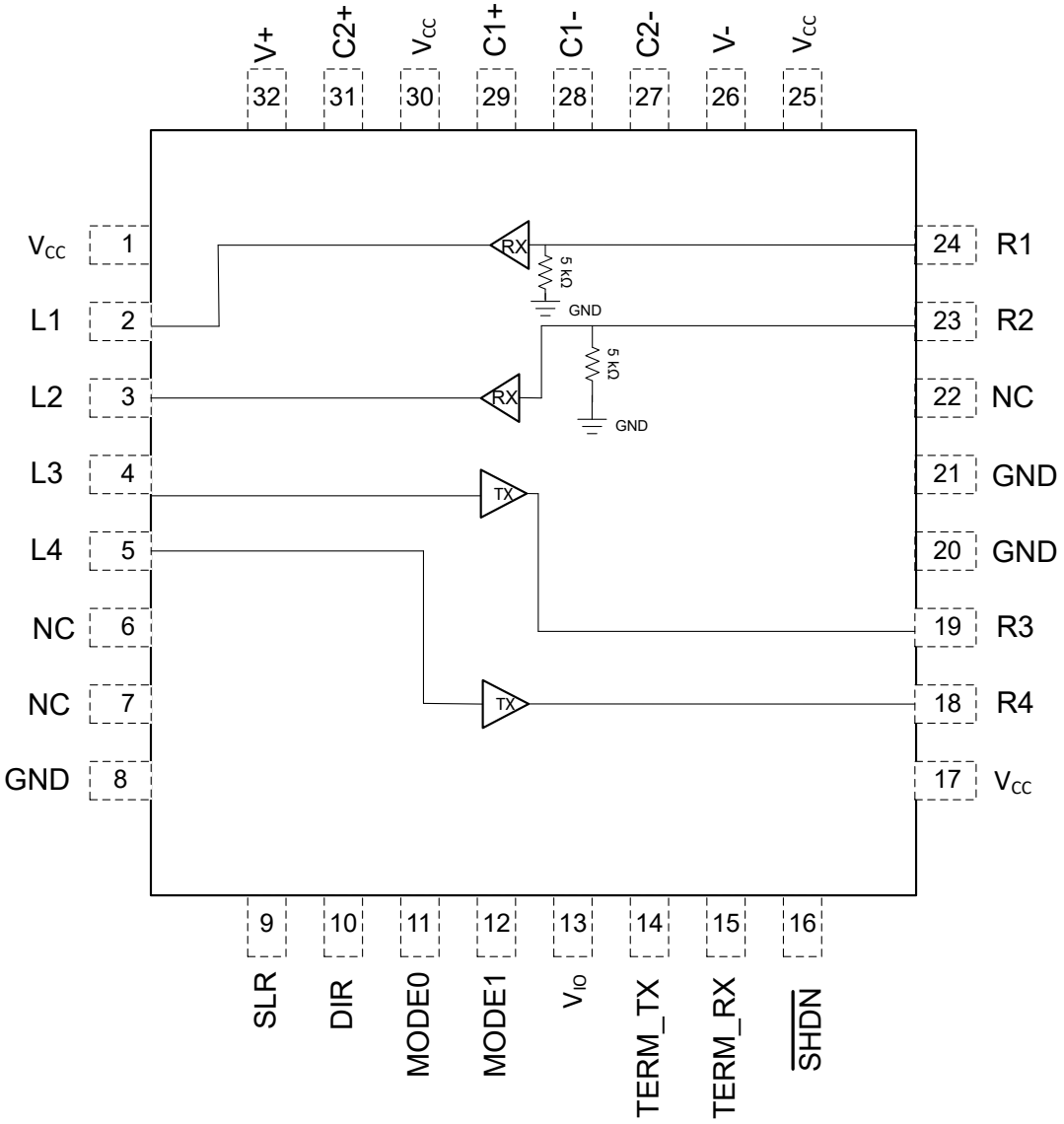


図 7-3. RS-232 2T2R Mode

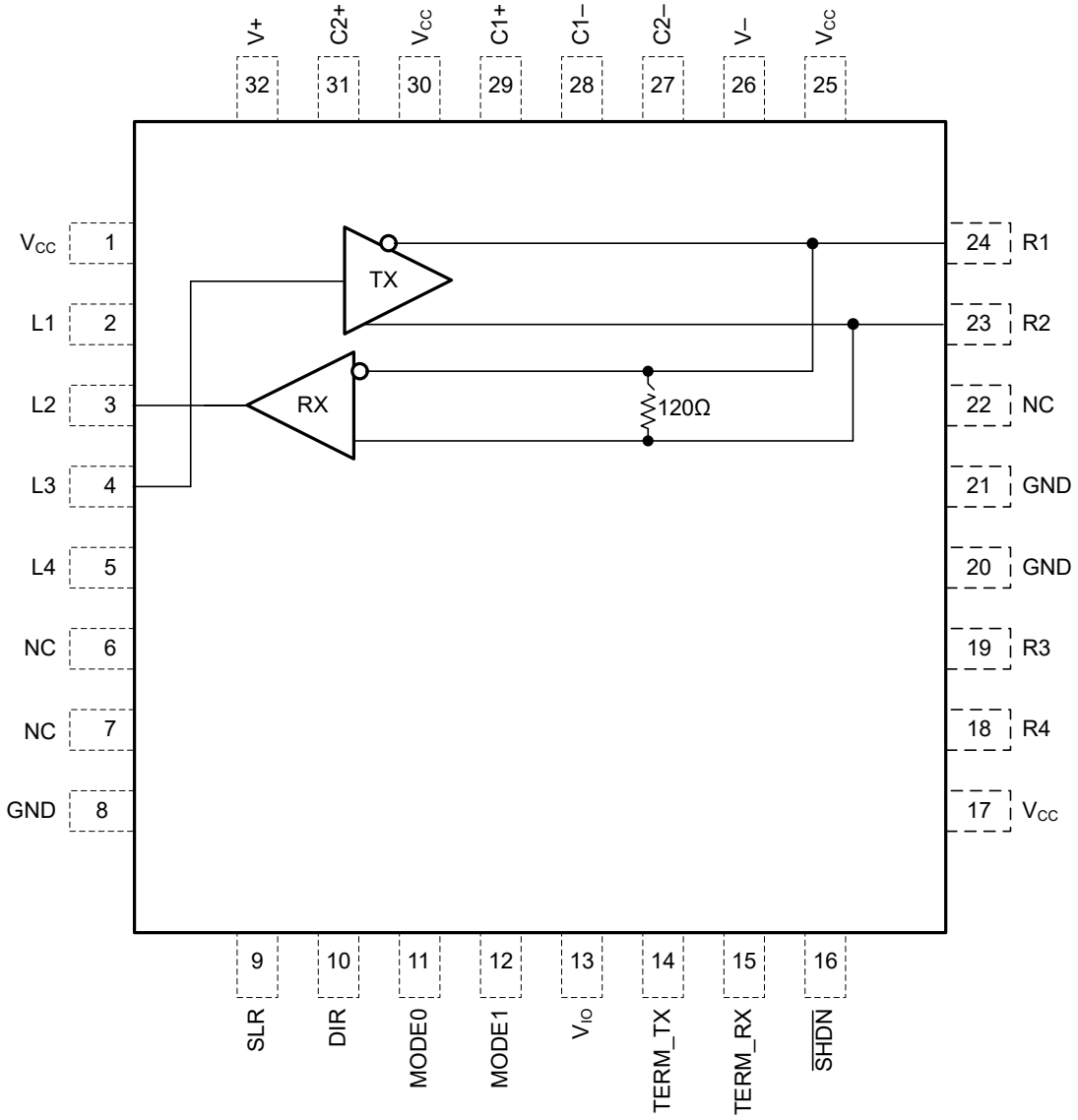


図 7-4. RS-485 Half Duplex Mode

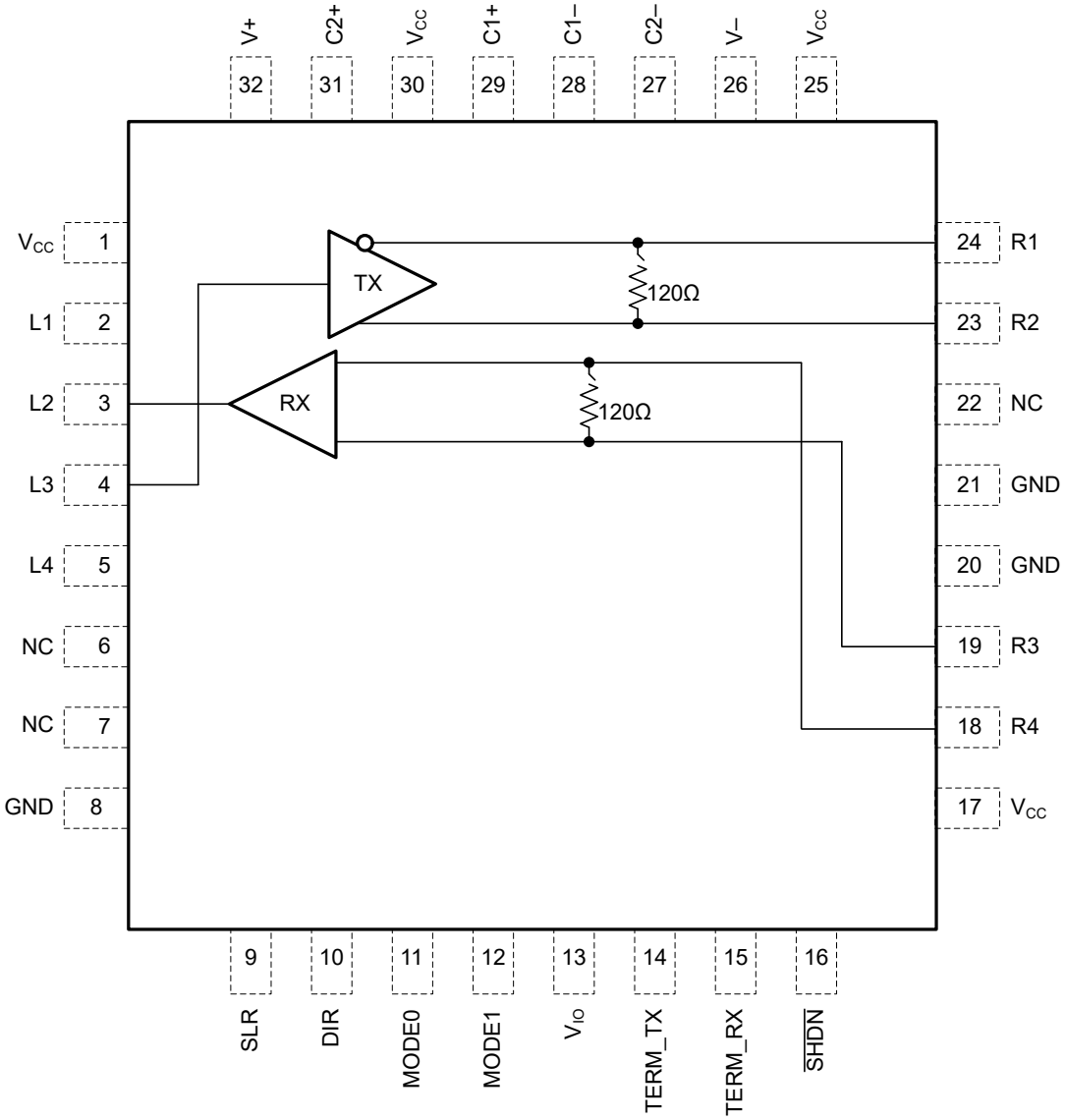


図 7-5. RS-485 Full Duplex Mode

7.4.1 RS-485 Functionality

When the driver enable pin, DIR, is logic high, the differential outputs R2 and R1 follow the logic states at data input L3. A logic high at L3 causes R2 to turn high and R1 to turn low. If the differential output voltage defined as $V_{OD} = V_{R2} – V_{R1}$ is positive. When L3 is low, the output states reverse: R1 turns high, R2 becomes low, and V_{OD} is negative.

When DIR is low, both outputs turn high-impedance. In this condition, the logic state at L3 is irrelevant. The DIR pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The L3 pin has an internal pull-up resistor to V_{IO}; thus, when left open while the driver is enabled, output R2 turns high and R1 turns low.

表 7-4. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
L3	DIR	R2	R1	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	High impedance	High impedance	Driver disabled
X	OPEN	High impedance	High impedance	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

表 7-4 is valid for both half duplex and full duplex modes, and is independent of state of TERM_TX, TERM_RX and SLR pins.

In full duplex mode, if $\overline{SHDN}$ is high, receiver is always enabled. In half duplex mode, receiver is enabled is DIR = Low/floating and disabled if DIR = V_{IO}. When the differential input voltage defined as $V_{ID} = V_{R2} – V_{R1}$ or $V_{R3} – V_{R4}$ is higher than the positive input threshold, V_{TH+}, the receiver output, L2, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, L2, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

In half duplex mode, when DIR is high, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 7-5 is valid irrespective of state of TERM_TX, TERM_RX and SLR pins. Other logic output L1 remains high in RS-485 mode.

表 7-5. Receiver Function Table

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_{R2} – V_{R1}$(Half duplex mode) or $V_{R3} – V_{R4}$(Full duplex mode)	L2	
$V_{TH+} < V_{ID}$	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	Receive valid bus low
X	High impedance for DIR = V_{IO} in Half duplex mode	Receiver disabled in half duplex mode for DIR = V_{IO}
Open-circuit bus	H	Fail-safe high output
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

7.4.2 RS-232 Functionality

In RS-232 mode, only way to disable driver is to go in shutdown mode by pulling $\overline{SHDN}$ pin low. A logic high at inputs for driver L3, L4 causes driver outputs R3, R4 to be driven low towards negative charge pump output V-. A logic low at inputs for driver L3, L4 causes driver outputs R3, R4 to be driven high towards positive charge pump output V+. If logic inputs are left floating, due to the pull-up resistors on driver logic inputs, the driver outputs are driven low towards V-.

表 7-6. Driver Function Table

INPUT	ENABLE	OUTPUTS	FUNCTION
L3, L4	$\overline{SHDN}$	R3, R4	
H	H	Low (driven towards V-)	Normal operation with inverting logic
L	H	H (Driven towards V+)	Normal operation with inverting logic
X	L	High impedance	TX and RX are disabled in shutdown mode
Open	H	Low (driven towards V-)	Since pull-up on logic input pin, output driven low by default

表 7-6 is valid irrespective of the state of SLR pin.

For the RS-232 receiver, if the receiver bus inputs are above rising threshold V_{IT+}, corresponding received logic output goes low. Also, if receiver bus inputs are below falling threshold V_{IT-}, corresponding received logic output goes high.

表 7-7. Receiver Function Table

RS-232 BUS INPUT	LOGIC OUTPUT	FUNCTION
V_{IRx} (voltage on R1, R2)	L1, L2	
$V_{IT+} < V_{IRx}$	L	Normal operation with inverting logic
$V_{IT-} < V_{IRx} < V_{IT+}$	?	Indeterminate bus state
$V_{IRx} < V_{IT-}$	H	Normal operation with inverting logic
X	High impedance for $\overline{SHDN}$ = GND	Receiver disabled in shutdown mode
Open-circuit bus	H	Fail-safe high output

表 7-7 is valid irrespective of the state of SLR pin.

7.4.3 Mode Control

表 7-8. MODE Control Function Table

MODE1	MODE0	Operating mode	Function
L	L	RS-232 loopback, charge pump is ON, V+/V- are regulated	L3 reflects on L2/R2/R3; L4 reflects on L1/R4/R1
L	H	RS-232 2T2R mode, charge pump is ON, V+/V- are regulated	2T2R mode; L3, L4 are Logic inputs for RS232 driver; L1, L2 are Logic outputs
H	L	RS-485 half duplex mode (charge pump is off)	L2 is RX Logic output; L3 is Driver Logic input; R1 R2 are Bus inverting and non-inverting terminals respectively
H	H	RS-485 full duplex mode (charge pump is off)	R1R2 are inverting and non-inverting driver terminals; R3R4 are non-inverting and inverting receiver terminals.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

THVD4421 is a highly integrated multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layer and is used for asynchronous data transmissions. MODE pins allow for the configuration of different operating modes. Device allows point-to-point RS-232 communication port and multipoint RS-485 communication port over common connector. The device also features integrated 120Ω switchable termination resistor on RS-485 bus lines which enables same device to be used for middle nodes or end nodes in an RS-485 network. When the device is configured in RS-232 mode, RS-485 circuits and 120Ω termination are disabled and do not interfere in RS-232 communication. For RS-232 communication, charge pump and 5kΩ resistor to ground on receiver bus pins is integrated in the device. This 5kΩ resistor and charge pump is automatically disabled in RS-485 mode. Slew rate limiting pin is provided so that same device can be used in slow speed or fast speed RS-485 and RS-232 applications. When ultra-low power consumption is needed, device can be put in shutdown mode using $\overline{SHDN}$ pin. All these features make the device completely flexible and suitable for various application needs. Integration of termination resistor saves significant PCB area compared to discrete implementation.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

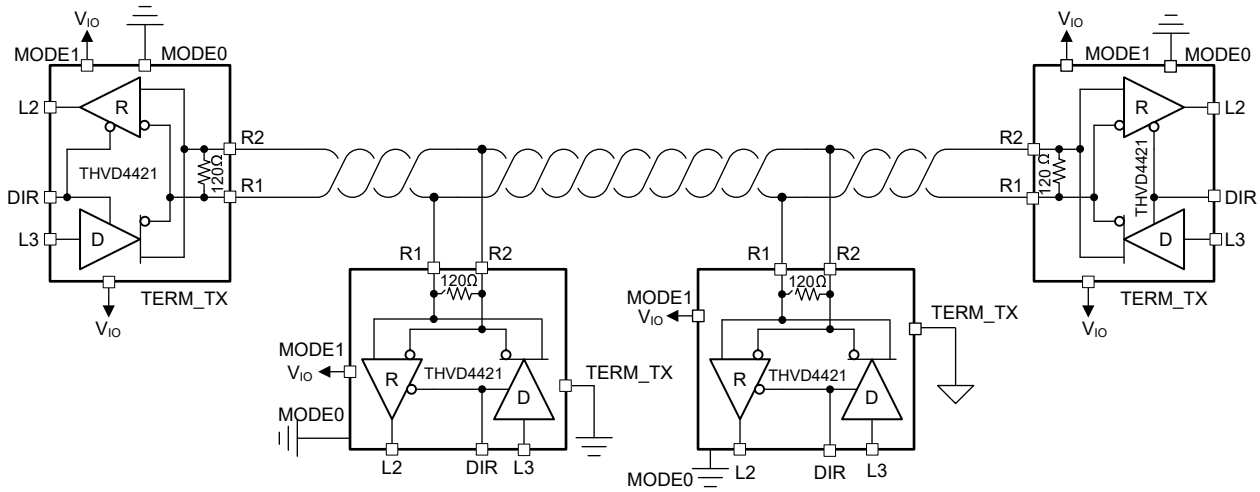


図 8-1. Typical RS-485 Network With Half-Duplex Transceivers

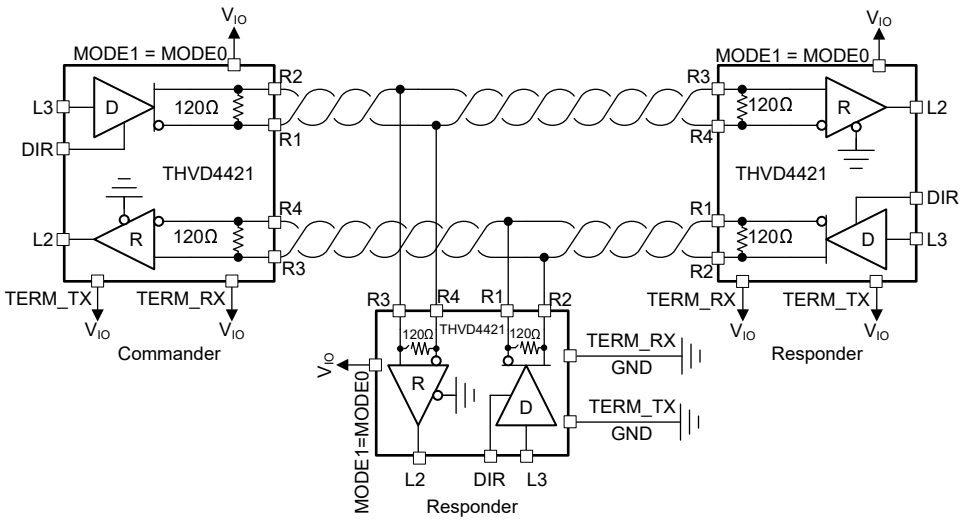


図 8-2. Typical RS-485 Network With Full-Duplex Transceivers

THVD4421 can be used in both networks (half and full duplex) and at all nodes (end node or middle nodes) since device has the configurability based on MODE1, MODE0 pins and TERM_TX, TERM_RX pins.

THVD4421 also consists of two line drivers, two line receivers and dual charge pump circuit to enable RS-232 serial communication port. This device provides the electrical interface between an asynchronous communication controller and the serial-port connector.

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes. RS-232 is more suitable for debug or configuration point to point applications.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

Even higher data rates are achievable (that is, 50Mbps for the THVD24xxV) when the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

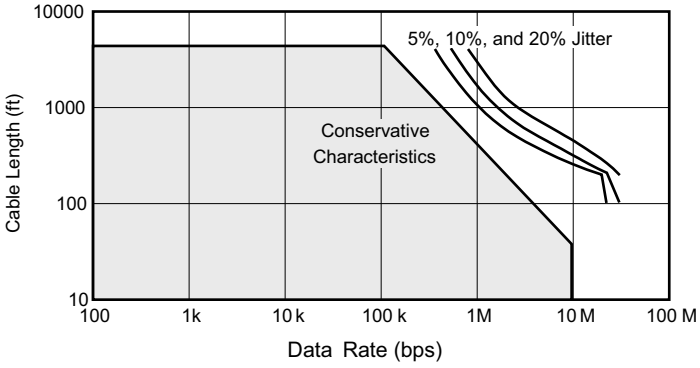


図 8-3. Cable Length vs Data Rate Characteristic

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the THVD4421 device in RS-485 half and full duplex mode consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible for a limited common mode range of - 7V to 12V.

8.2.2 Detailed Design Procedure

図 8-4 suggests an application schematic for THVD4421. Device has all logic pins on one side and bus side pins on other side to enable a flow-through layout in end application.

All V_{CC} power pins should have 1µF decoupling capacitor close to the respective device pins. RS-232 charge pump is designed such that 100nF charge pump capacitors work for both 3.3V and 5V operating V_{CC} supply.

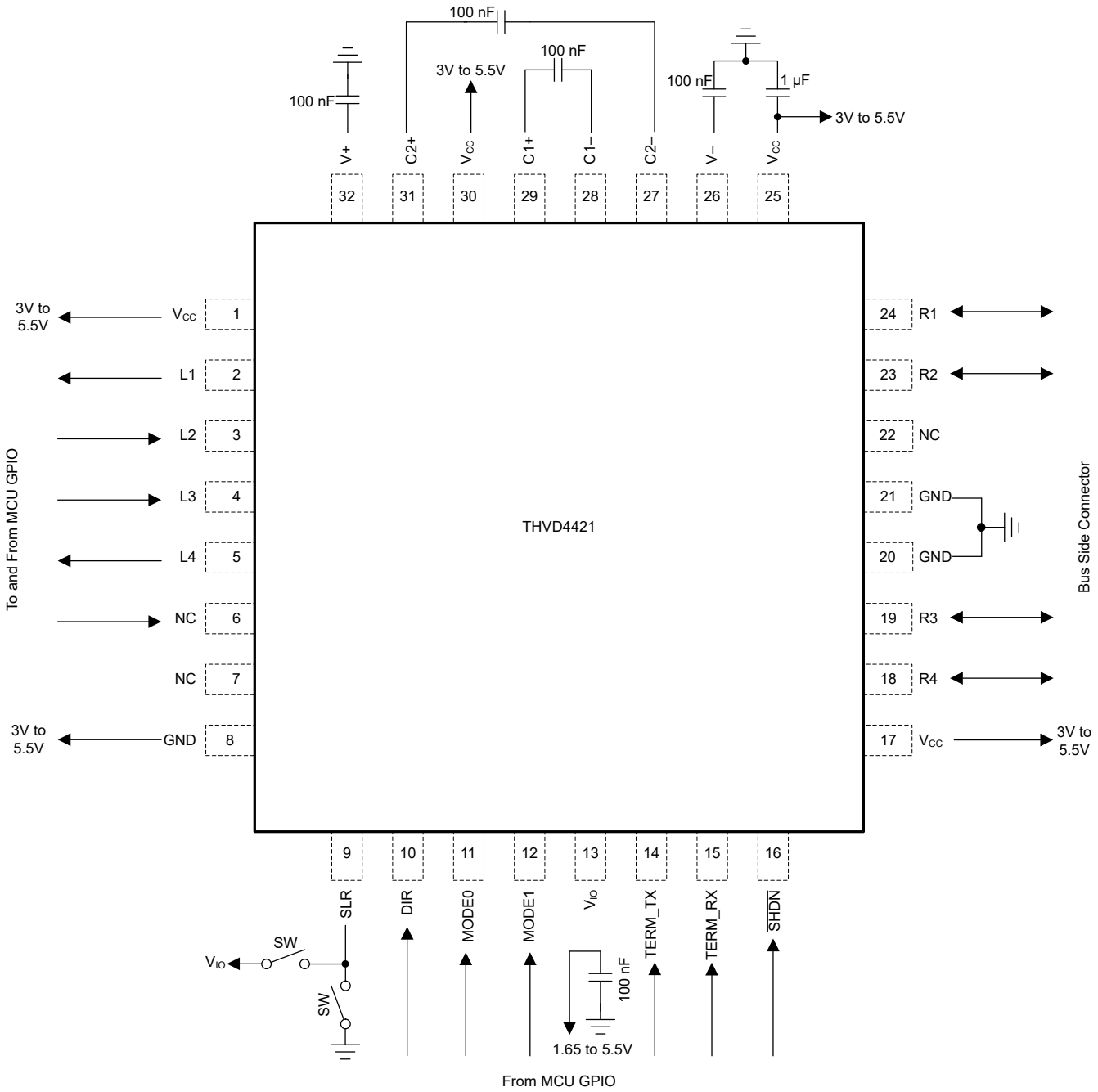
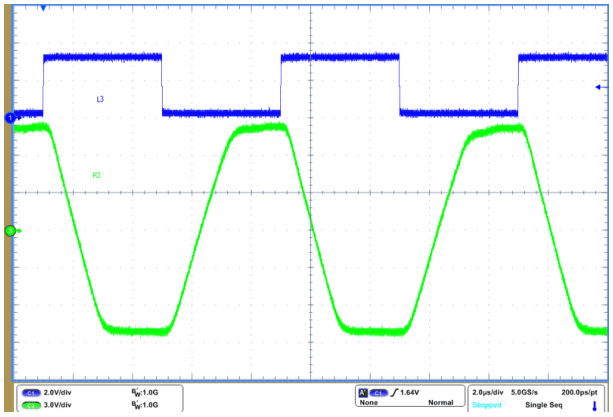


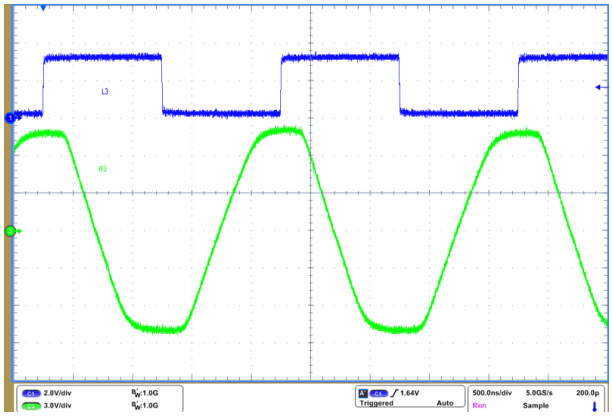
図 8-4. Typical application diagram for THVD4421

8.2.3 Application Curves



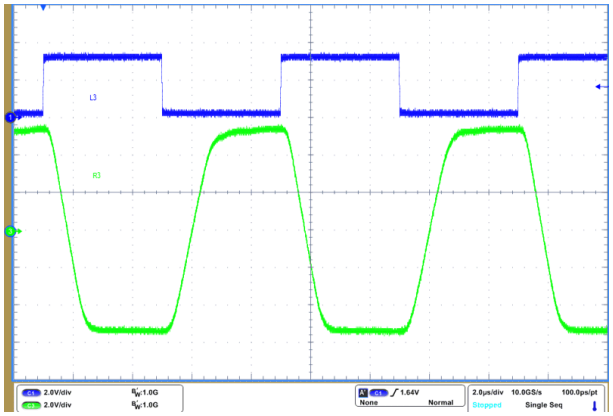
V_{CC} = 5V Bus Load = 5kΩ||2.5nF
250kbps SLR = V_{IO}

図 8-5. RS-232 Driver Waveform at 250kbps and V_{CC} = 5V



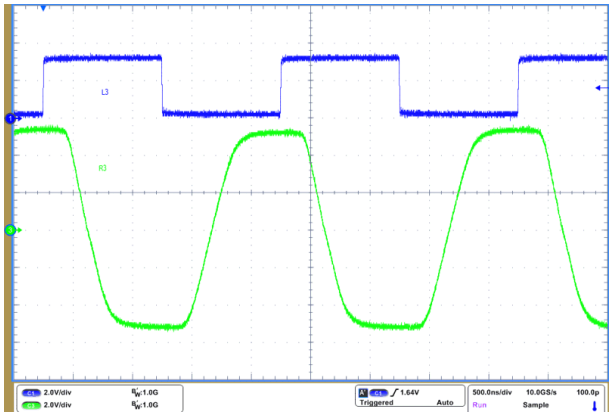
V_{CC} = 5V Bus Load = 5kΩ||1nF
1Mbps SLR = GND

図 8-6. RS-232 Driver Waveform at 1Mbps and V_{CC} = 5 V



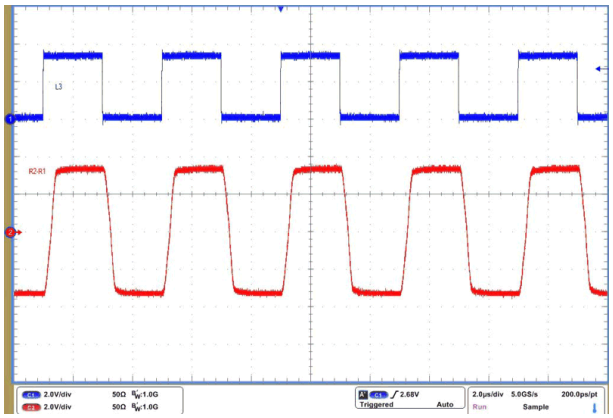
V_{CC} = 3.3V Bus Load = 5kΩ||2.5nF
250kbps SLR = V_{IO}

図 8-7. RS-232 Driver Waveform at 250kbps and V_{CC} = 3.3 V



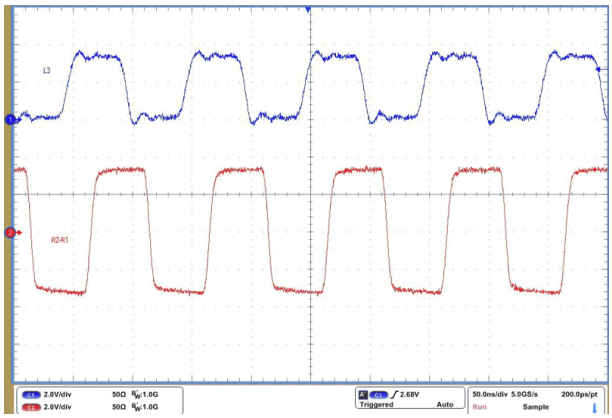
V_{CC} = 3.3V R_L = 5kΩ||1nF
1kbps SLR = GND

図 8-8. RS-232 Driver Waveform at 1Mbps and V_{CC} = 3.3 V



V_{CC} = 5V Bus Load = 54Ω||50pF
SLR = V_{IO} Square wave at 500kbps

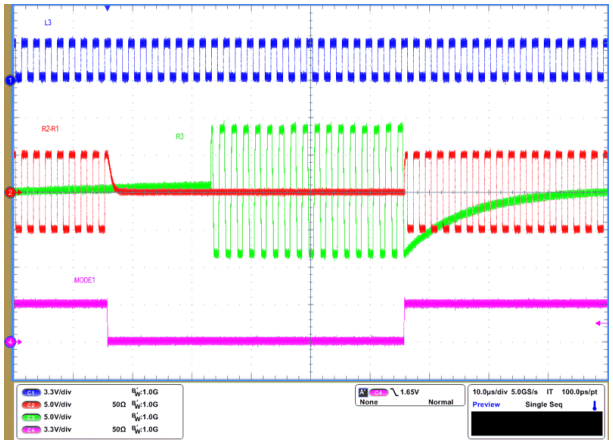
図 8-9. RS-485 Driver Waveform at 500 kbps and V_{CC} = 5 V



V_{CC} = 5V Bus Load = 54Ω||50pF
SLR = GND Square wave at 20kbps

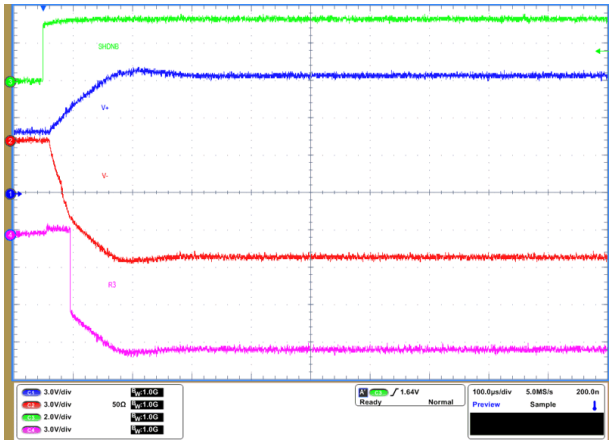
図 8-10. RS-485 Driver Waveform at 20 Mbps and V_{CC} = 5V

8.2.3 Application Curves (continued)



V_{CC} = 5V L3 = 1 Mbps square wave
SLR = GND MODE1 toggled at 10khz

図 8-11. RS-232 to RS-485 Mode Switching Waveform



V_{CC} = 5V L3 = GND
SHDN toggled

図 8-12. Mode Switching Waveform From Shutdown to RS-232 Mode

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a ceramic capacitor located as close to the supply pins as possible. Recommended bypass capacitor for V_{CC} is 1µF, for V_{IO} is 100nF, for V+, V- charge pump voltage supplies is 100nF. Besides this, two charge pump flying capacitors of 100 nF each are needed between C1+, C1- terminals and between C2+, C2- terminals. For V_{CC} = 3.3V ±10%, V+ and V- voltages are regulated to +5.5V and -5.5 V typically. If an application needs larger RS-232 output voltages, V_{CC} = 5V ± 10% is recommended because V+ and V- are regulated to ±9.5V.

8.4 Layout

8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. THVD4421 has integrated IEC ESD and EFT protection. So, if the application does not need IEC Surge protection, external transient protection may not needed. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the external protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply decoupling capacitors as close as possible to the V_{CC}, V_{IO}, V+, V- pins of transceiver.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Optionally, use 1kΩ to 10kΩ pull-up and pull-down resistors for control lines to limit noise currents in these lines during transient events.

8.4.2 Layout Example

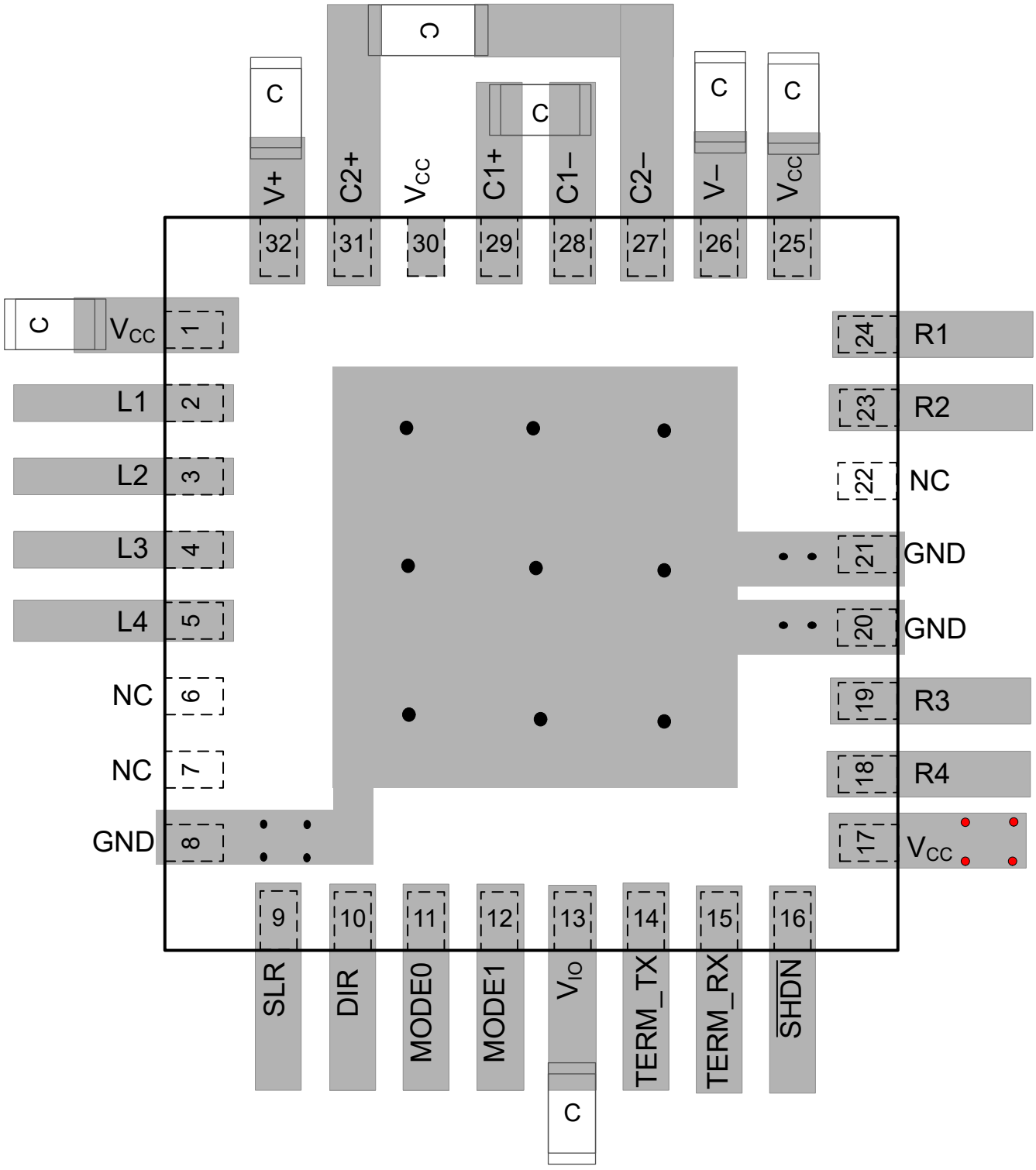


図 8-13. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

表 10-1.

DATE	REVISON	NOTES
April 2024	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD4421RHBR	ACTIVE	VQFN	RHB	32	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	THVD 4421	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

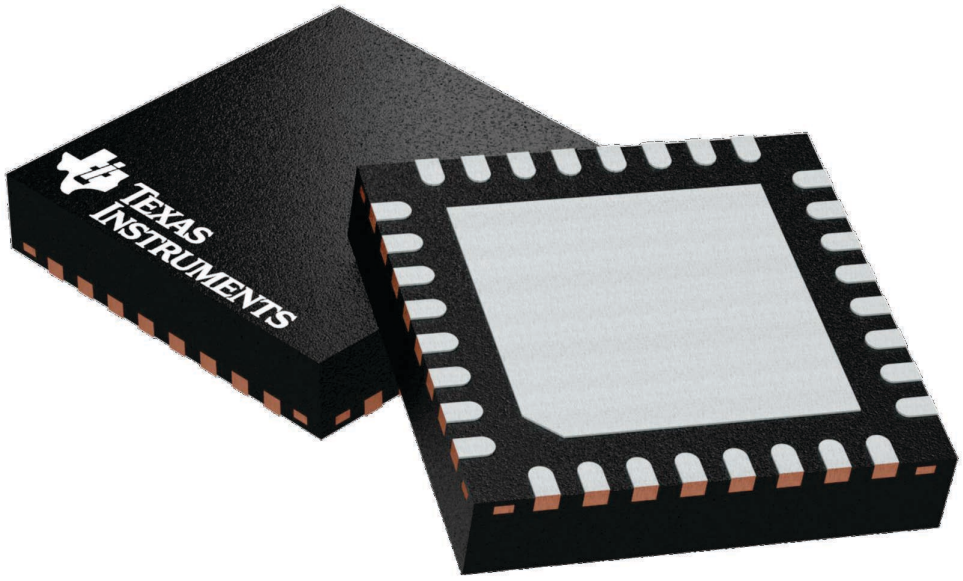
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

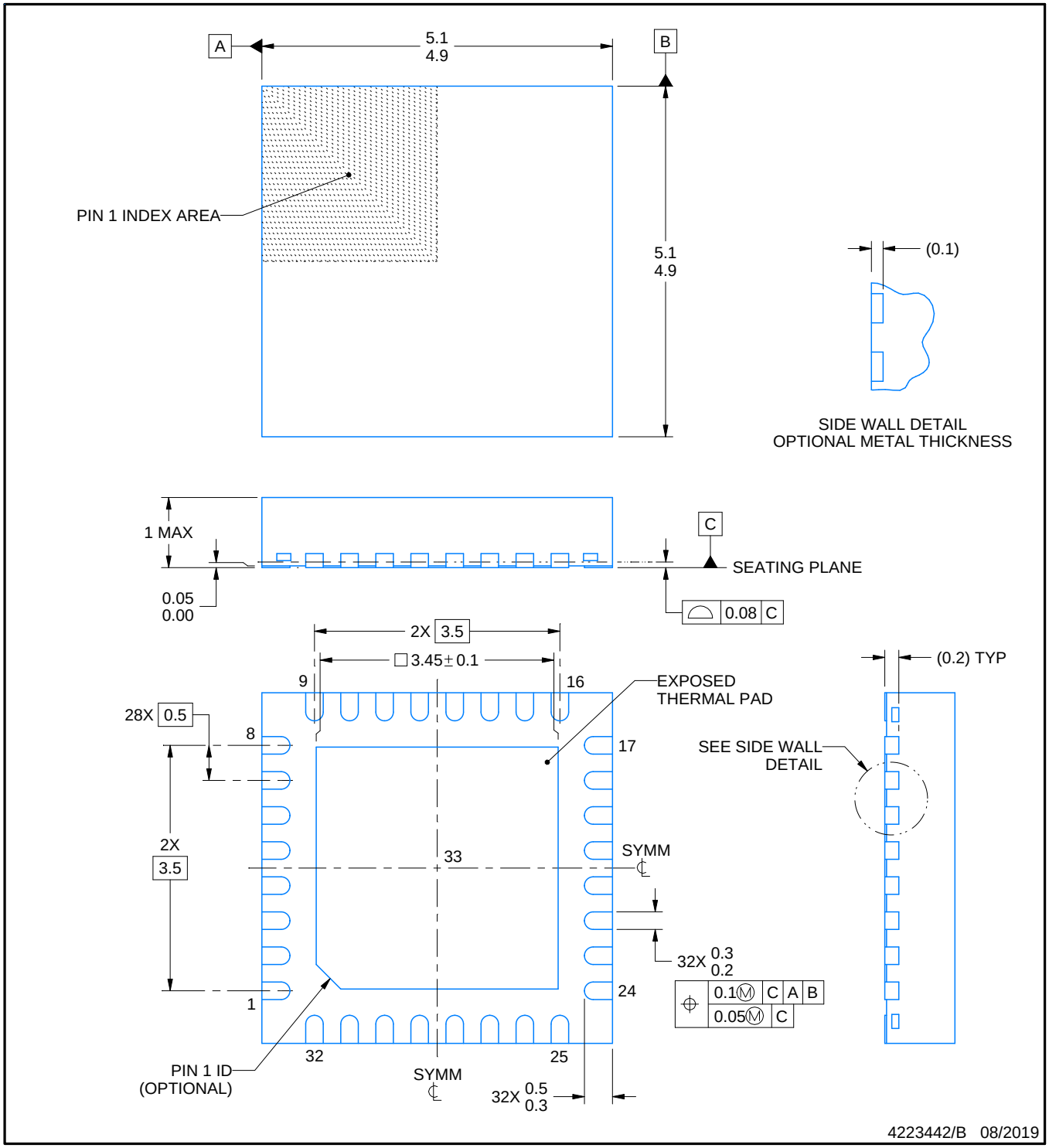
4224745/A

RHB0032E

PACKAGE OUTLINE

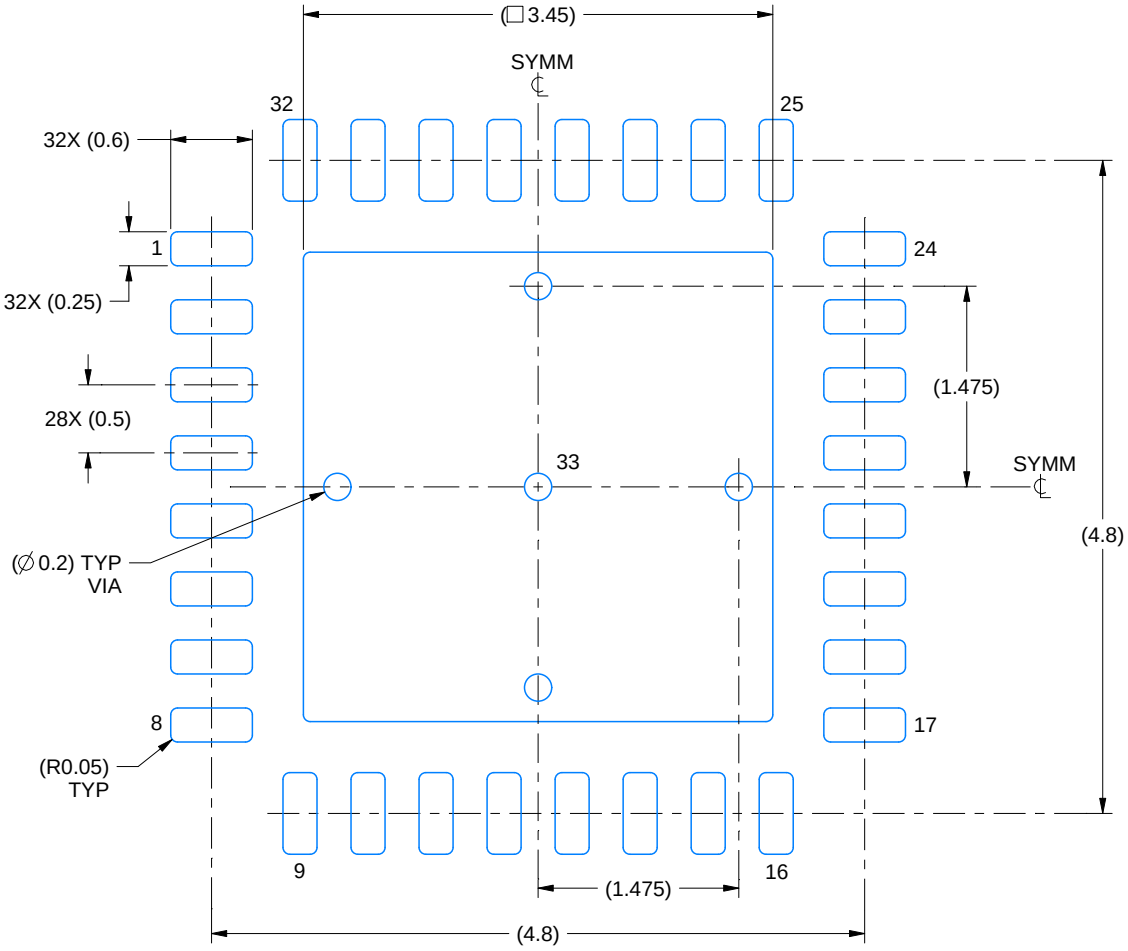
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

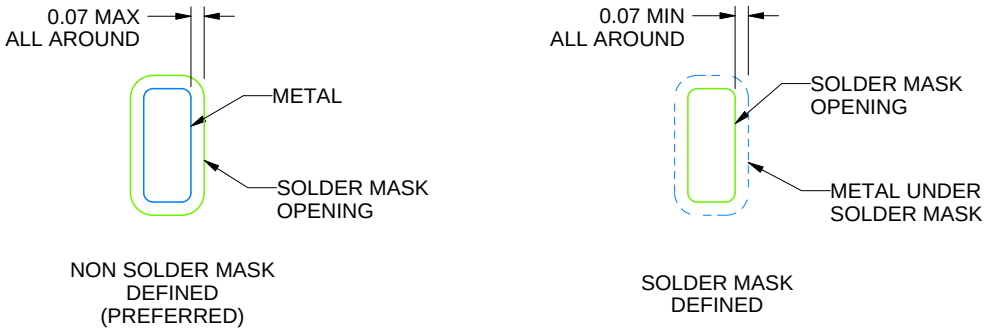


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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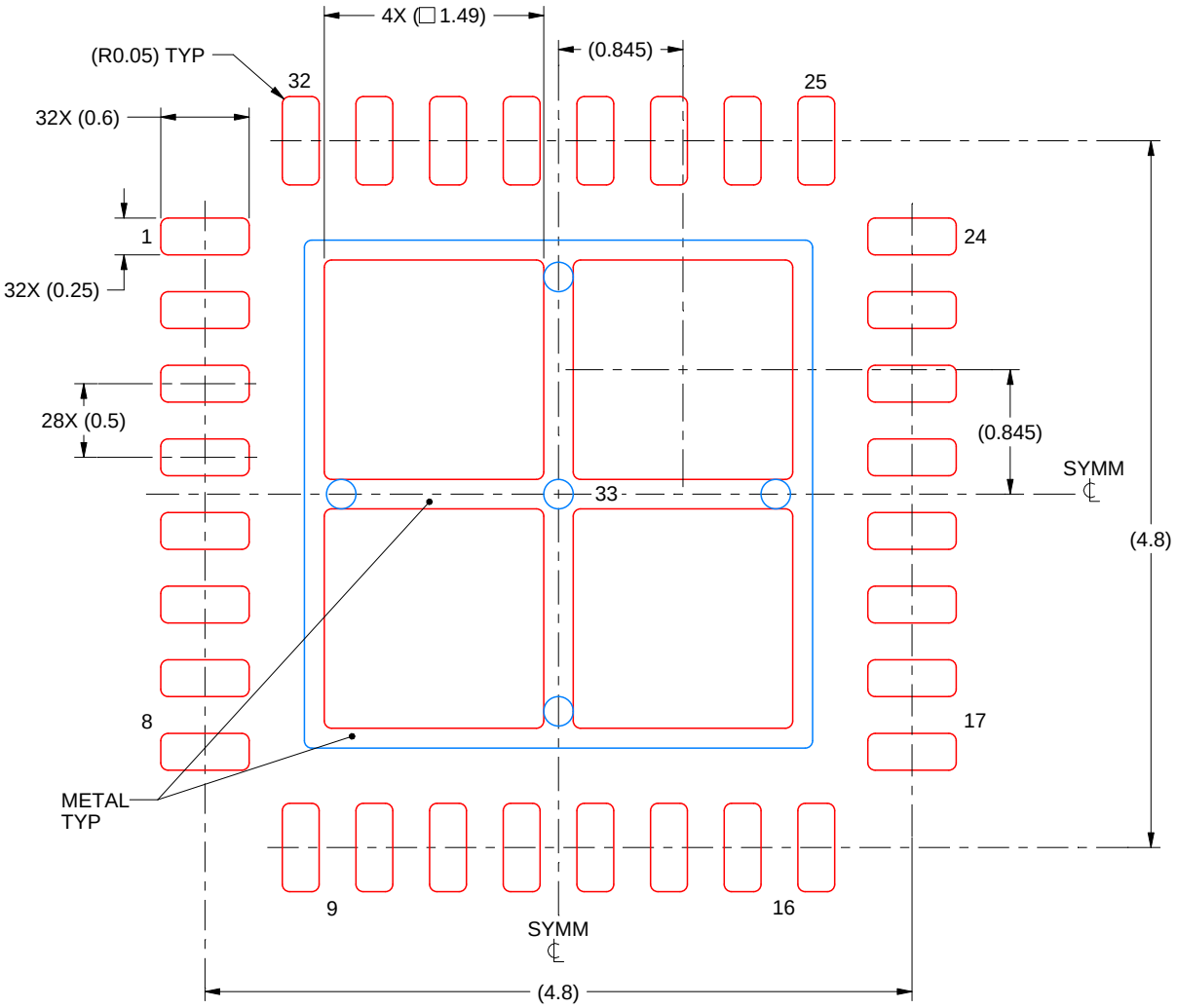
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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