TLIN2021A-Q1 故障保護 LIN トランシーバ、抑止およびウェイク付き

1 特長

- 車載アプリケーション用に AEC-Q100 (グレード 1) 認定済み
- LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2A、ISO 17987–4 電気的物理層 (EPL) 仕様に準拠
- SAE J2602-1 に準拠した車載用途向け LIN ネットワーク
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 12V および 24V アプリケーションに対応
- 広い入力電圧範囲
  - V_{SUP} 範囲:4.5V～45V
- 最高 20kbps の LIN 送信データ・レート
- 最高 100kbps の LIN 送信データ・レート
- 動作モード通常、スタンバイ、スリープ
- ソース認識による低消費電力モードからのウェイクアップをサポート
  - LIN バスからのリモート・ウェイクアップ
  - WAKE ピンによるローカル・ウェイクアップ
  - EN によるローカル・ウェイクアップ
- 45kΩ の LIN プルアップ抵抗を内蔵
- INH ピンを使用してシステム・レベルの電力を制御
- 電源オン / オフ時の LIN バスと RXD 出力のグリッチを防止
- 保護機能:±60V の LIN バス・フォルト耐性、58V の負荷ダンプ対応、V_{SUP} の低電圧保護、TXD ドミナント状態タイムアウト、サーマル・シャットダウン、電源なしノードまたはグランド切断に対するシステム・レベルのフェイルセーフ
- 接合部温度:-40℃～150℃
- 8 ピンの SOIC、ウェッタブル・フランク付きの VSON、SOT23 パッケージで供給

2 アプリケーション

- ボディ・エレクトロニクス / 照明
- 車載インフォテインメントおよびクラスタ
- ハイブリッド電気自動車およびパワー・トレイン・システム
- 産業用輸送

3 概要

TLIN2021A-Q1 は、ローカル相互接続ネットワーク (LIN) 物理層トランシーバです。LIN とは、車載用車内ネットワークをサポートする低速のユニバーサル非同期レシーバ・トランスミッタ (UART) 通信プロトコルです。

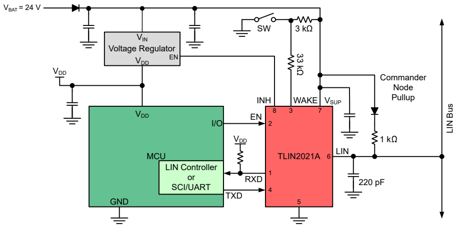
TLIN2021A-Q1 のトランスミッタは最大 20kbps のデータ・レートをサポートしています。本トランシーバは、TXD ピン経由で LIN バスの状態を制御し、オープン・ドレインの RXD 出力ピンでバスの状態を報告します。このデバイスは、電磁気放射 (EME) を低減するために電流制限付き波形整形ドライバを備えています。

TLIN2021A-Q1 は、広い入力電圧動作範囲によって 12V および 24V アプリケーションに対応するように設計されています。このデバイスは低消費電力スリープ・モードと、wake over LIN、WAKE ピン、EN ピンによる低消費電力モードからのウェークアップをサポートしています。このデバイスを使用すると、ノードに存在する可能性がある各種電源を本デバイスの INH 出力ピンで選択的に有効にすることで、バッテリの消費電流をシステム・レベルで低減できます。

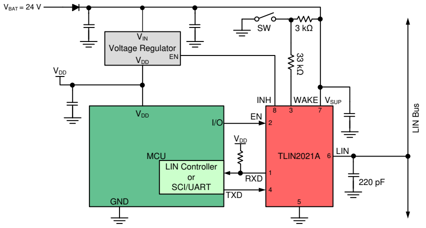
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TLIN2021A	SOIC (D) (8)(2)	4.90mm × 3.91mm
	VSON (DRB) (8)	3.00mm × 3.00mm
	SOT23 (DDF) (8)(2)	2.90mm × 1.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) 製品プレビュー



コマンダ・ノードの概略回路図



レスポンダ・ノードの概略回路図

English Data Sheet: SLLSFK7

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2021) to Revision A (April 2022) **Page**

- 回路図の画像の後にある注を削除.................... 1
- Changed the WAKE I_{IL} parameter description from "Ligh-level input leakage current" to "Low-level input leakage current".................... 6

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5 概要 (続き)

TLIN2021A-Q1 には LIN レスポンダ・ノード・アプリケーション用の抵抗、ESD 保護、フォルト保護が内蔵されているため、アプリケーションの外付け部品数を減らせます。このデバイスでは、グランドのシフトまたは電源電圧の切断が発生しても、電流が LIN 経由で電源入力に逆流することはありません。

TLIN2021A-Q1 は、低電圧検出、サーマル・シャットダウン保護、グランド喪失保護機能も内蔵しています。フォルト条件が発生した場合、トランスミッタは即座にオフになり、フォルト条件が解消するまでオフに維持されます。

6 Pin Configuration and Functions

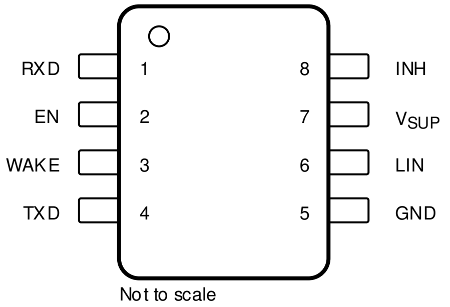


図 6-1. D Package, 8-Pin (SOIC), and DDF Package, 8-Pin (SOT23) Top View

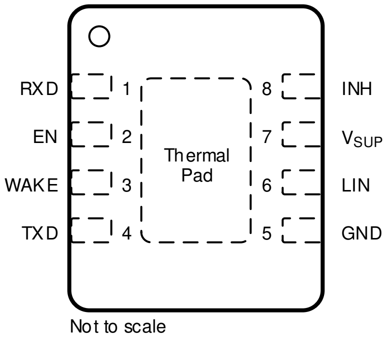


図 6-2. DRB Package, 8-Pin (VSON), Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
RXD	1	Digital	LIN receive data output, open-drain
EN	2	Digital	Sleep mode control input, integrated pull-down
WAKE	3	High Voltage	Local wake-up input, high voltage
TXD	4	Digital	LIN transmit data input, integrated pulled down - active low after a local wake-up event
GND	5	GND	Ground connection
LIN	6	Bus IO	LIN bus input/output line
V_{SUP}	7	Supply	High-voltage supply from the battery
INH	8	High Voltage	Inhibit output to control system voltage regulators and supplies, high voltage
Thermal Pad	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

7 Specification

7.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO 17987)	–0.3	60	V
V_{LIN}	LIN Bus input voltage (ISO 17987)	–60	60	V
V_{WAKE}	WAKE pin input voltage	–0.3	60	V
V_{INH}	INH pin output voltage	–0.3	60 and $V_O \leq V_{SUP}+0.3$	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_O	Digital pin output current		8	mA
$I_{O(INH)}$	Inhibit output current		4	mA
$I_{O(WAKE)}$	WAKE output current due to ground shift ($V_{WAKE} \leq V_{GND}$) – 0.3 V thus current out of the WAKE pin must be limited		3	mA
T_J	Junction Temp	–55	165	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM) classification level 3B: V_{SUP}, INH, and WAKE with respect to ground		±8000	V
		Human body model (HBM) classification level 3B: LIN with respect to ground		±10000	
		Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings - IEC Specification

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	LIN, V_{SUP}, WAKE terminal to GND(1)	IEC 62228-2 per ISO 10605 Contact discharge R = 330 Ω, C = 150 pF (IEC 61000-4-2)	±8000	V
		LIN terminal to GND(1)	IEC 62228-2 per ISO 10605 Indirect contact discharge R = 330 Ω, C = 150 pF (IEC 61000-4-2)	±8000	

7.3 ESD Ratings - IEC Specification (continued)

				VALUE	UNIT
V_{TRAN}	Non-synchronous transient injection	LIN, V_{SUP}, WAKE terminal to GND(1)	IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 1	-100	V
			IEC 62215-3 24 V electrical systems (3) Pulse 1	-450	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems 24 V electrical systems (3) Pulse 2	75	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3a	-150	
			IEC 62215-3 24 V electrical systems (3) Pulse 3a	-225	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3b	150	
			IEC 62215-3 24 V electrical systems (3) Pulse 3b	225	
	Direct capacitor coupling	LIN terminal to GND(2)	SAE J2962-1 per ISO 7637-3 DCC - Slow transient pulse	±30	

(1) Results given here are specific to the IEC 62228-2 Integrated circuits – EMC evaluation of transceivers – Part 2: LIN transceivers. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(2) Results given here are specific to the SAE J2962-1 Communication Transceivers Qualification Requirements - LIN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(3) Verified during characterization

7.4 Thermal Information

THERMAL METRIC(1)		TLIN2021A-Q1			UNIT
		D (SOIC)	DRB (VSON)	DDF(SOT)	
		8 PINS	8 Pins	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.2	54.4	120.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	61.1	60.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.6	26.8	42.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.7	2.3	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	68.9	26.7	41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	10.8	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Recommended Operating Conditions

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply Voltage	4.5		45	V
V_{LIN}	LIN Bus input voltage	0		45	V
V_{LOGIC}	Logic Pin Voltage	0		5.25	V
T_J	Operating virtual junction temperature range	-40		150	°C
T_{SDR}	Thermal shutdown rising	160			°C
T_{SDF}	Thermal shutdown falling			150	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

7.6 Power Supply Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
V_{SUP}	Operational supply voltage	Device is operational beyond the LIN defined nominal supply voltage range See Figure 8-1 See Figure 8-2	4.5		45	V
	Nominal supply voltage	Normal and standby modes(1) See Figure 8-1 See Figure 8-2	4.5		45	V
		Sleep mode	4.5		45	V
I_{SUP}	Supply current Bus dominant	Normal mode EN = V_{CC}, R_{LIN} ≥ 500 Ω, C_{LIN} ≤ 10 nF, INH = WAKE = V_{SUP}		1.8	7.5	mA
		Standby mode EN = 0 V, R_{LIN} ≥ 500 Ω, C_{LIN} ≤ 10 nF, INH =WAKE = V_{SUP}		1	2.1	mA
	Supply current Bus recessive	Normal mode EN = V_{CC}, INH = WAKE = V_{SUP}		400	850	µA
		Standby mode EN = 0 V, INH = WAKE = V_{SUP}		20	55	µA
	Supply current Sleep mode	4.5 V < V_{SUP} ≤ 27 V, T_J = 125℃ EN = 0 V, LIN = WAKE = V_{SUP}, TXD and RXD floating		12	20	µA
		27 V < V_{SUP} ≤ 45 V, T_J = 125℃ EN = 0 V, LIN = WAKE = V_{SUP}, TXD and RXD floating			26	µA
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp up		4.15	4.45	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp down	3.5	4		V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.13		V

(1) Normal mode ramp V_{SUP} while LIN signal is a 10 kHz square wave with 50% duty cycle and 36 V swing.

7.7 Electrical Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD Output Terminal						
V_{OL}	Low-level voltage	Based upon external pull-up to V_{CC} (4)			0.6	V
I_{OL}	Low-level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	–5		5	µA
TXD Input Terminal						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			V
I_{LKG}	Low-level input leakage current	TXD = 0 V	–5		5	µA
$I_{TXD(WAKE)}$	Local wake-up source recognition TXD	Standby mode after a local wake-up event V_{LIN} = V_{SUP}, WAKE = 0 V or V_{SUP}, TXD = 1 V	1.3		8	mA
R_{TXD}	Internal pull-down resistor value		125	350	800	kΩ
EN Input Terminal						
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{IH}	High-level input voltage		2		5.25	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low-level input current	EN = 0 V	–5		5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
LIN Terminal (Referenced to V_{SUP})						

7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	LIN recessive high-level output voltage(3)	TXD = V_{CC}, I_O = 0 mA 7 V ≤ V_{SUP} ≤ 45 V	0.85			V_{SUP}
V_{OH}	LIN recessive high-level output voltage(1) (2)	TXD = V_{CC}, I_O = 0 mA 7 V ≤ V_{SUP} ≤ 18 V	0.8			V_{SUP}
V_{OH}	LIN recessive high-level output voltage(3)	TXD = V_{CC}, I_O = 0 mA 4.5 V ≤ V_{SUP} ≤ 7 V	3			V
V_{OL}	LIN dominant low-level output voltage(3)	TXD = 0 V 7 V ≤ V_{SUP} ≤ 45 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage(1) (2)	TXD = 0 V 7 V ≤ V_{SUP} ≤ 18 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage(3)	TXD = 0 V 4.5 V ≤ V_{SUP} ≤ 7 V			1.2	V
V_{BUSdom}	Low-level input voltage(3)	LIN dominant (including LIN dominant for wake up) See Figure 8-3 See Figure 8-4			0.4	V_{SUP}
V_{BUSrec}	High-level input voltage(3)	LIN recessive See Figure 8-3 See Figure 8-4	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage(1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltge(1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.4		0.53	V_{SUP}
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5%(3)	TXD & RXD open 4.5 V ≤ V_{LIN} ≤ 60 V	–0.3		60	V
V_{BUS_CNT}	Receiver center threshold(3)	$V_{BUS\_CNT} = (V_{BUSrec} + V_{BUSdom})/2$ See Figure 8-3 See Figure 8-4	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO 17987)	$V_{HYS} = V_{BUSrec} - V_{BUSdom}$ See Figure 8-3 See Figure 8-4			0.175	V_{SUP}
V_{HYS}	Hysteresis voltage (SAE J2602)	$V_{HYS} = V_{IH} - V_{IL}$ See Figure 8-3 See Figure 8-4	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN termination pull-up path	I_{SERIAL_DIODE} = 10 µA	0.4	0.7	1.0	V
$I_{BUS(LIM)}$	Limiting current	TXD = 0 V, V_{LIN} = 36 V, R_{Meas} = 480 Ω V_{SUP} = 36 V, V_{BUSdom} < 10.224 V	75	120	300	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant	Driver off/recessive, LIN = 0 V V_{SUP} = 24 V See Figure 8-6	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive	Driver off/recessive, LIN ≥ V_{SUP} 4.5 V ≤ V_{SUP} ≤ 45 V See Figure 8-7			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive	Driver off/recessive, LIN = V_{SUP} See Figure 8-7	–5		5	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground	GND_{Device} = V_{SUP} = 24 V R_{Meas} = 1 kΩ 0 V < V_{LIN} < 36 V	–1.5		1.5	mA
$I_{leak\ gnd(dom)}$	Leakage current, loss of ground(5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = dominant	–1		1	mA
$I_{leak\ gnd(rec)}$	Leakage current, loss of ground(5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = recessive	–100		100	µA

7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply	V_{SUP} = GND 0 V ≤ V_{LIN} ≤ 36 V			5	μA
I_{RSLEEP}	Pull-up current source to V_{SUP} sleep mode	V_{SUP} = 27 V, LIN = GND	–20		–1.5	μA
R_{PU}	Pull-up resistor to V_{SUP}	Normal and standby modes	20	45	60	kΩ
C_{LIN}	Capacitance of the LIN pin	V_{SUP} = 14 V			25	pF
INH Output Terminal						
ΔV_H	High level voltage drop INH with respect to V_{SUP}	I_{INH} = - 0.5 mA		0.5	1	V
$I_{LKG(INH)}$	Leakage current sleep mode	INH = 0 V	–0.5		0.5	μA
WAKE Input Terminal						
V_{IH}	High-level input voltage	Standby and sleep mode	V_{SUP} – 1.8			V
V_{IL}	Low-level input voltage	Standby and sleep mode			V_{SUP} – 3.85	V
I_{IH}	High-level input leakage current	WAKE = V_{SUP} - 1 V	–25	–12.5		μA
I_{IL}	Low-level input leakage current	WAKE = 1 V		15	25	μA
t_{WAKE}	WAKE hold time	Wake up time from sleep mode	5		50	μs
Duty Cycle Characteristics						
$D1_{12V}$	Duty cycle 1(3) ISO 17987 Param 27	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 μs D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.396			
$D1_{12V}$	Duty cycle 1(3) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 50 μs D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.396			
$D1_{12V}$	Duty cycle 1(1) (2) (6)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 μs D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.396			
$D2_{12V}$	Duty cycle 2(3) ISO 17987 Param 28	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 μs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.581	
$D2_{12V}$	Duty cycle 2(3) (6)	$TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 4.5 V to 7 V, t_{BIT} = 50 μs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.581	
$D2_{12V}$	Duty cycle 2(1) (2) (6)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 μs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.581	
$D3_{12V}$	Duty cycle 3(3) ISO 17987 Param 29	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 μs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.417			
$D3_{12V}$	Duty cycle 3(3) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP} $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 μs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.417			

7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D3_{12V}$	Duty cycle 3(1) (2) (6)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.417			
$D4_{12V}$	Duty cycle 4(3) ISO 17987 Param 30	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.59	
$D4_{12V}$	Duty cycle 4(3) (6)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 µs D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.59	
$D4_{12V}$	Duty cycle 4(1) (2) (6)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.59	
$D1_{24V}$	Duty cycle 1 ISO 17987 Param 72	$TH_{REC(MAX)}$ = 0.710 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.554 x V_{SUP}, V_{SUP} = 15 V to 36 V, t_{BIT} = 50 µs D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.330			
$D2_{24V}$	Duty cycle 2 ISO 17987 Param 73	$TH_{REC(MIN)}$ = 0.446 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.302 x V_{SUP}, V_{SUP} = 15.6 V to 36 V, t_{BIT} = 50 µs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.642	
$D3_{24V}$	Duty cycle 3 ISO 17987 Param 74	$TH_{REC(MAX)}$ = 0.744 x V_{SUP} $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} V_{SUP} = 7 V to 36 V, t_{BIT} = 96 µs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.386			
$D3_{24V}$	Duty cycle 3 (6)	$TH_{REC(MAX)}$ = 0.645 x V_{SUP} $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 µs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9	0.386			
$D4_{24V}$	Duty cycle 2 (6) ISO 17987 Param 75	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4.5 V to 36 V, t_{BIT} = 96 µs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See Figure 8-8 and Figure 8-9			0.591	
$D1_{LB}$	Duty cycle 1 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 52 µs	0.396			
$D2_{LB}$	Duty cycle 2 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 52 µs			0.581	
$D3_{LB}$	Duty cycle 3 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 96 µs	0.396			
D_{4LB}	Duty cycle 4 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 96 µs			0.581	
$T_{r\text{-}d\ max\_D1}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Recessive to dominant	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{REC(MAX)\_D1}$ - $t_{DOM(MIN)\_D1}$			10.8	µs
$T_{d\text{-}r\ max\_D2}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Dominant to recessive	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{DOM(MAX)\_D2}$ - $t_{REC(MIN)\_D2}$			8.4	µs

7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{r\text{-}d\ max\_D3}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Recessive to dominant	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{REC(MAX)\_D3}$ - $t_{DOM(MIN)\_D3}$			15.9	µs
$T_{d\text{-}r\ max\_D4}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Dominant to recessive	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{DOM(MAX)\_D4}$ - $t_{REC(MIN)\_D4}$			17.28	µs
$T_{r\text{-}d\ max\_low}$	Low battery transmitter propagation delay timings for the duty cycle(1) (2) (6) Recessive to dominant	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5.5 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{REC(MAX)\_low}$ - $t_{DOM(MIN)\_low}$			10.8	µs
$T_{d\text{-}r\ max\_low}$	Low battery transmitter propagation delay timings for the duty cycle(1) (2) (6) Dominant to recessive	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 6.1 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{DOM(MAX)\_low}$ - $t_{REC(MIN)\_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
(2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
(4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage.
(5) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}
(6) Specified by design

7.8 AC Switching Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdr}	Receiver rising propagation delay time ISO 17987 Param 31	4.5 V ≤ VSUP < 5.5 V, R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See Figure 8-10 and Figure 8-11			6	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31				6	µs
t_{rx_pdr}	Receiver rising propagation delay time ISO 17987 Param 31	5.5 V ≤ VSUP, R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See Figure 8-10 and Figure 8-11			5	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31				5	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time ISO 17987 Param 32	Rising edge with respect to falling edge $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr}$), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See Figure 8-10 and Figure 8-11	–2		2	µs
t_{LINBUS}	Minimum dominant time on LIN bus for wake-up	See Figure 8-14, Figure 9-2 and Figure 9-3	25	65	150	µs
t_{CLEAR}	Time to clear false wake-up prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 9-3	8	25	50	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin See Figure 8-12	2		15	µs
t_{NOMINT}	Normal mode initialization time(1)	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby to normal mode. See Figure 8-12			45	µs
t_{PWR}	Power-up time	Time it takes for valid data on RXD upon power-up			1.5	ms
t_{TXD_DTO}	Dominant state time out		20	50	80	ms

(1) The transition time from sleep mode to normal mode includes both t_{MODE_CHANGE} and t_{NOMINT}.

7.9 Typical Curves

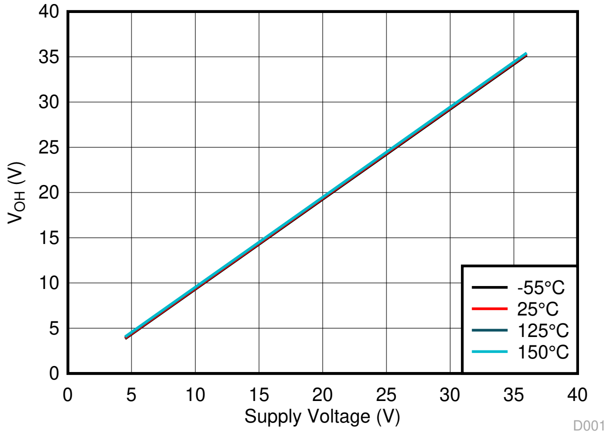


図 7-1. VOH vs VSUP vs Temperature

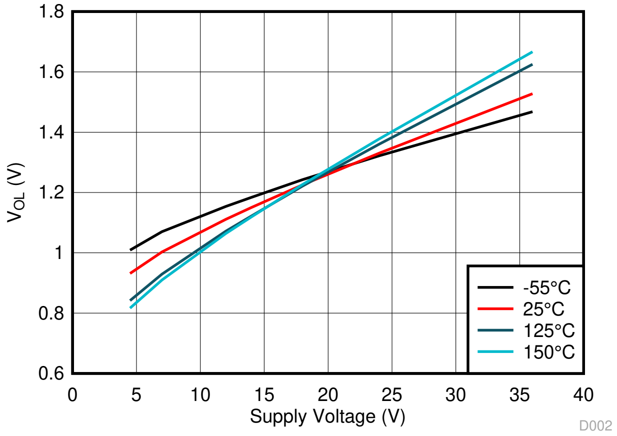


図 7-2. VOL vs VSUP vs Temperature

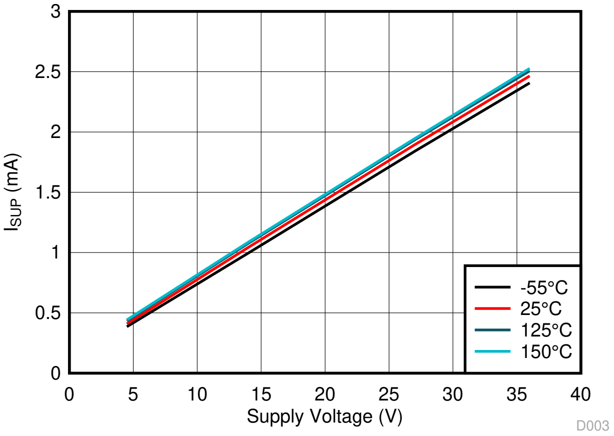


図 7-3. ISUP (DOM) vs VSUP vs Temperature

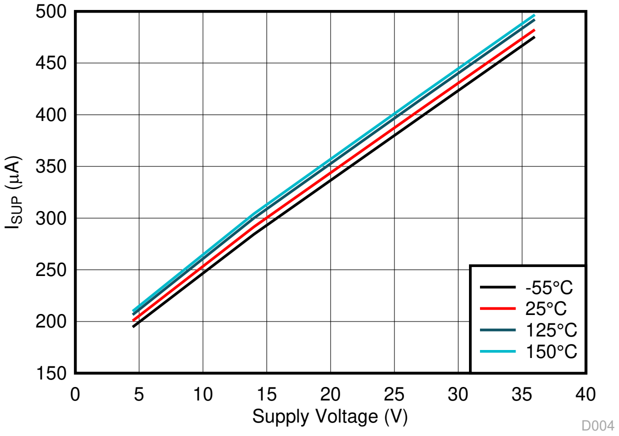


図 7-4. ISUP (REC) vs VSUP vs Temperature

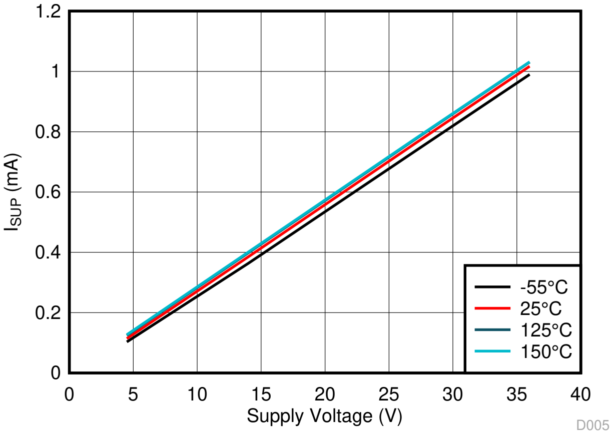


図 7-5. ISUP(STBY_DOM) vs VSUP vs Temperature

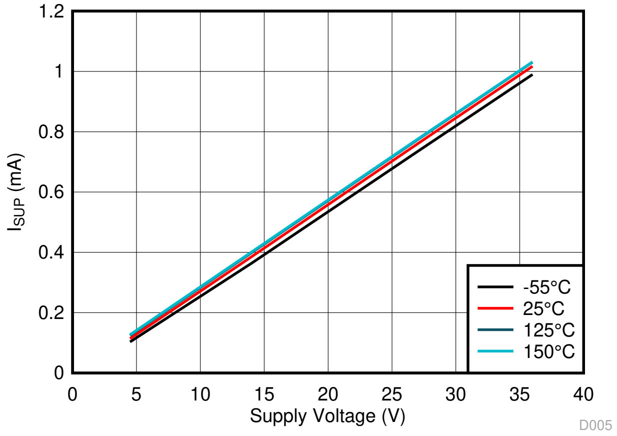


図 7-6. ISUP(STBY_REC) vs VSUP vs Temperature

7.9 Typical Curves (continued)

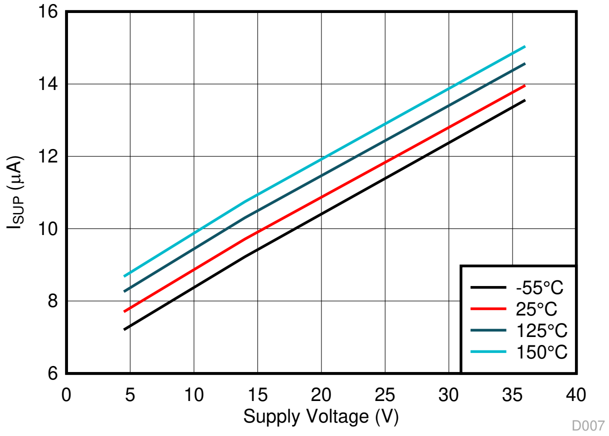


図 7-7. ISUP(SLP) vs VSUP vs Temperature

8 Parameter Measurement Information

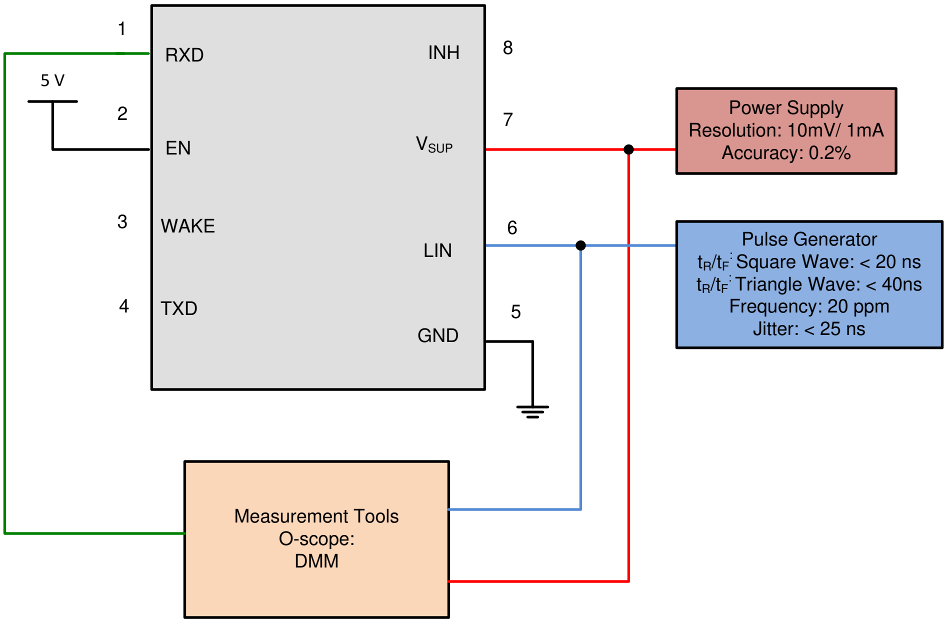


図 8-1. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

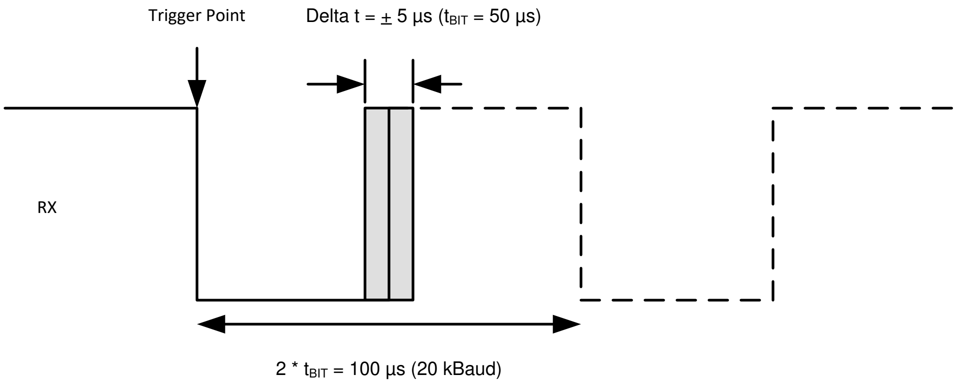


図 8-2. RX Response: Operating Voltage Range

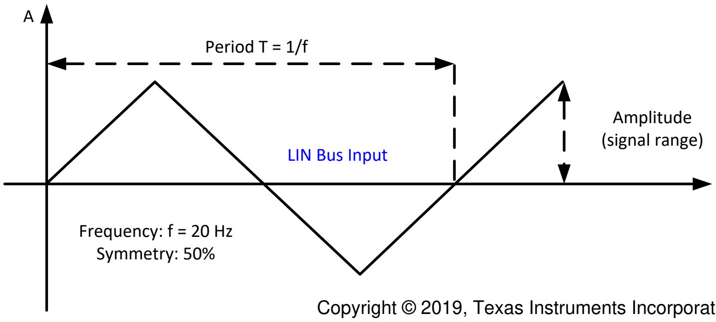


図 8-3. LIN Bus Input Signal

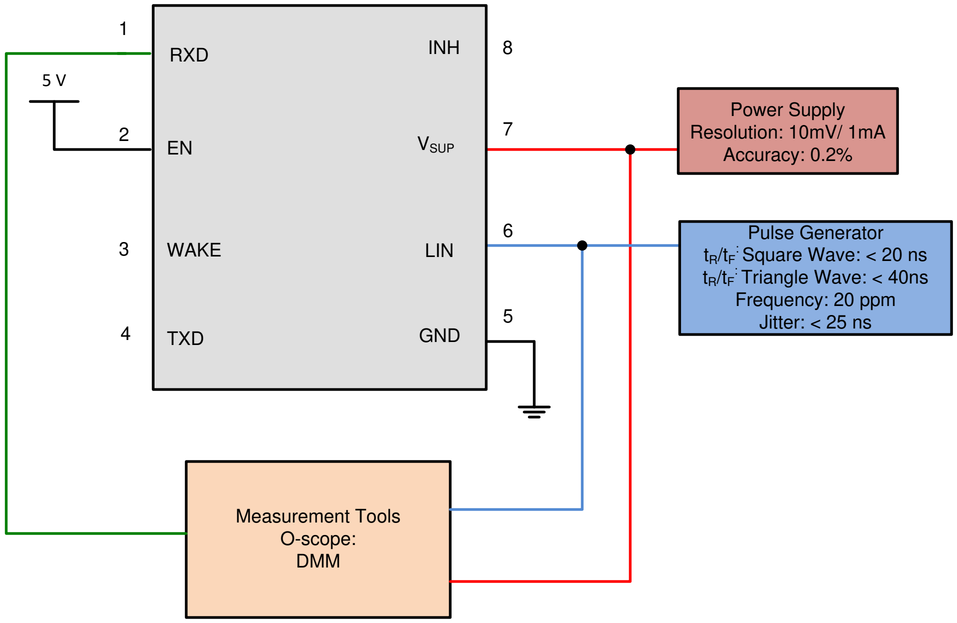


図 8-4. LIN Receiver Test with RX access Param 17, 18, 19, 20

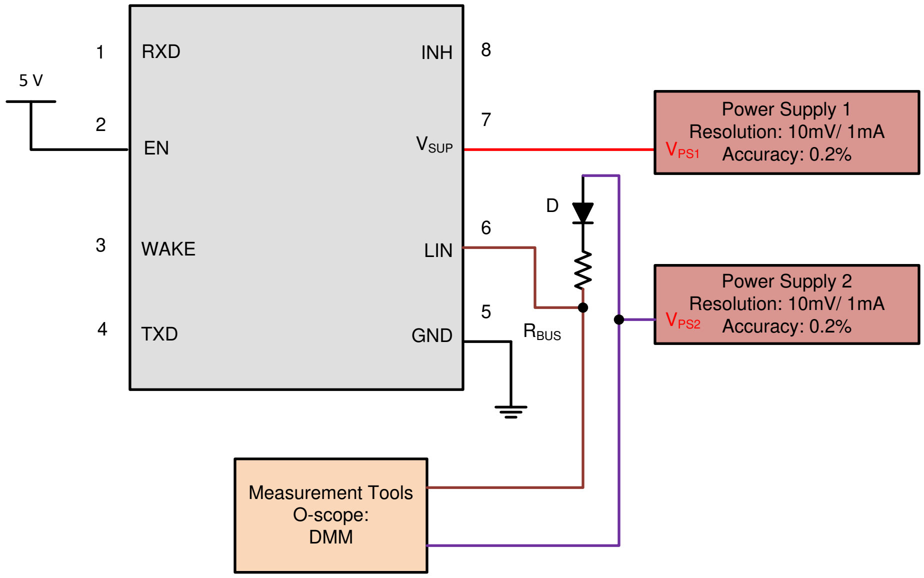


図 8-5. $V_{SUP\_NON\_OP}$ Param 11

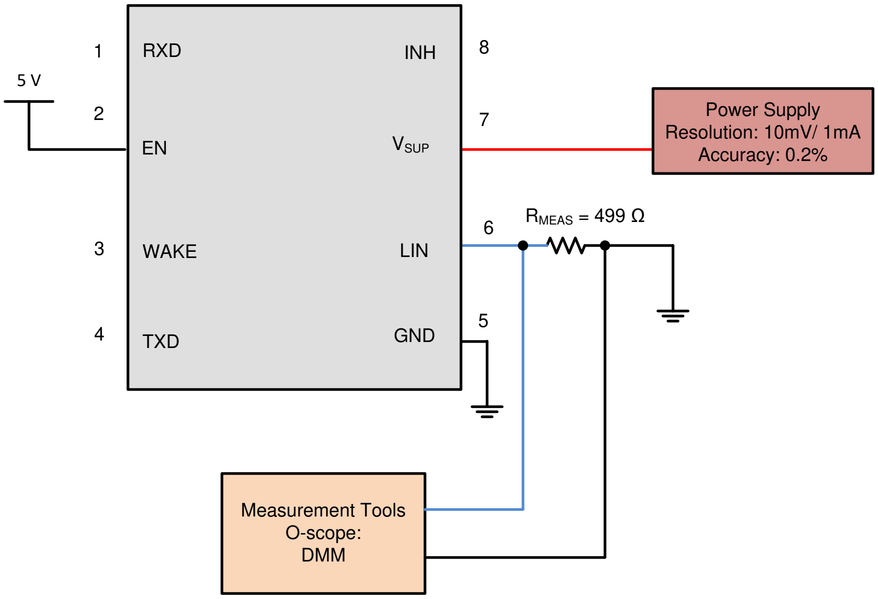
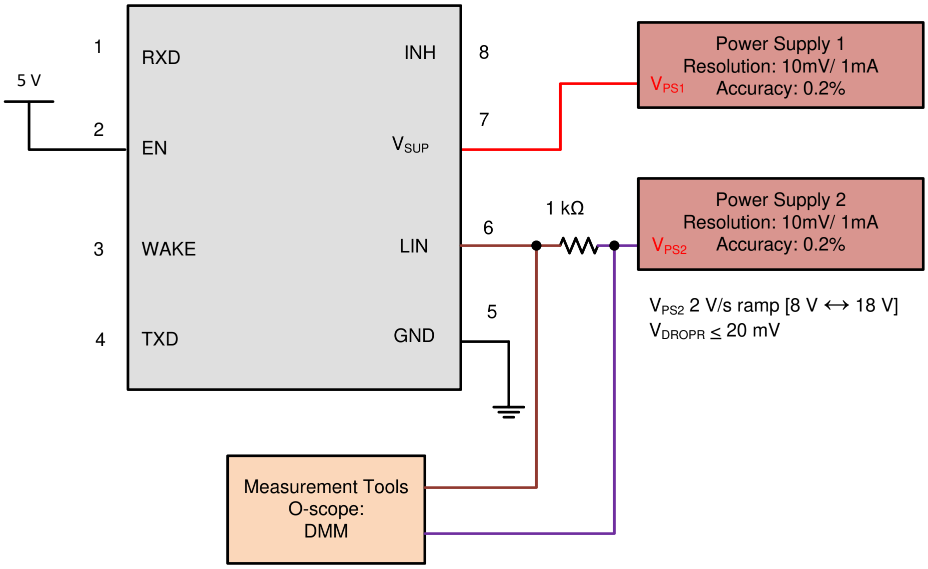


図 8-6. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State V_{BUS} = 0 V, Param 13



V_{PS2} 2 V/s ramp [8 V ↔ 18 V]
$V_{DROPR} \leq$ 20 mV

図 8-7. Test Circuit for $I_{BUS\_PAS\_rec}$ Param 14

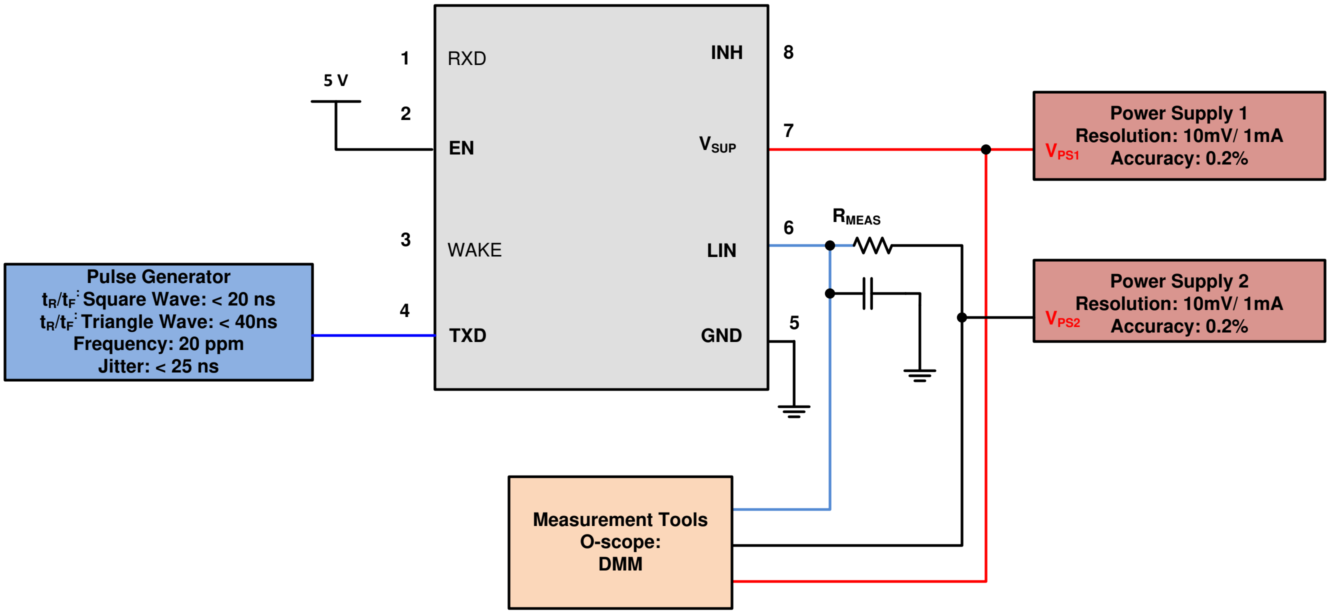


図 8-8. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30

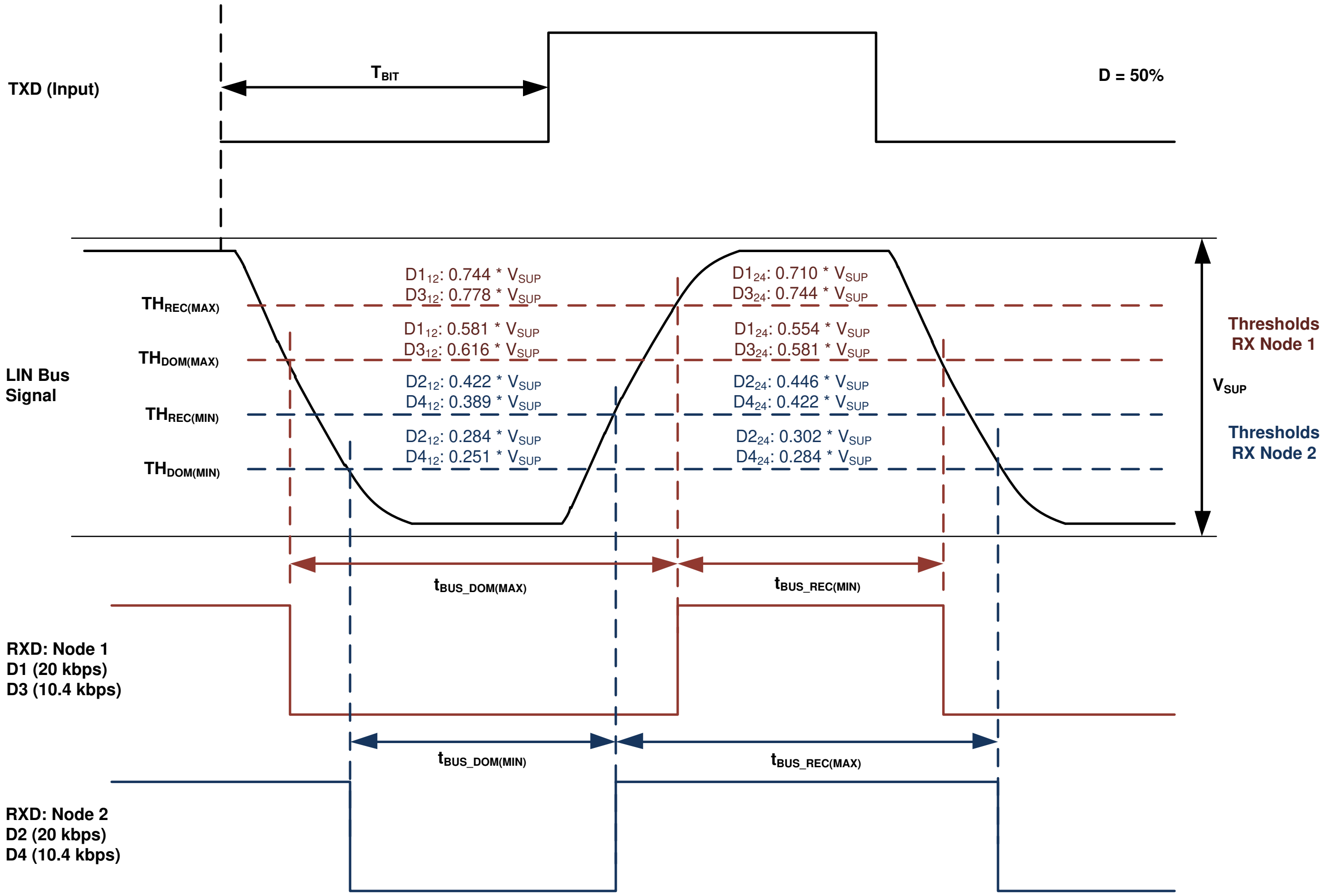


図 8-9. Definition of Bus Timing Parameters

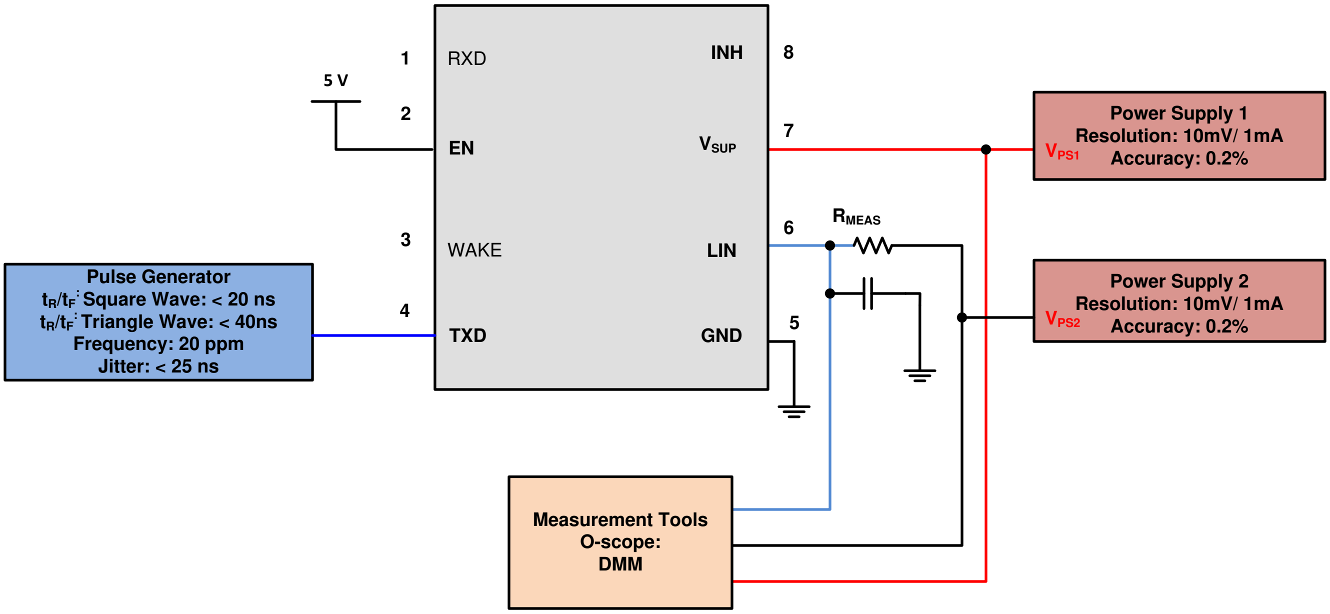


図 8-10. Propagation Delay Test Circuit; Param 31, 32

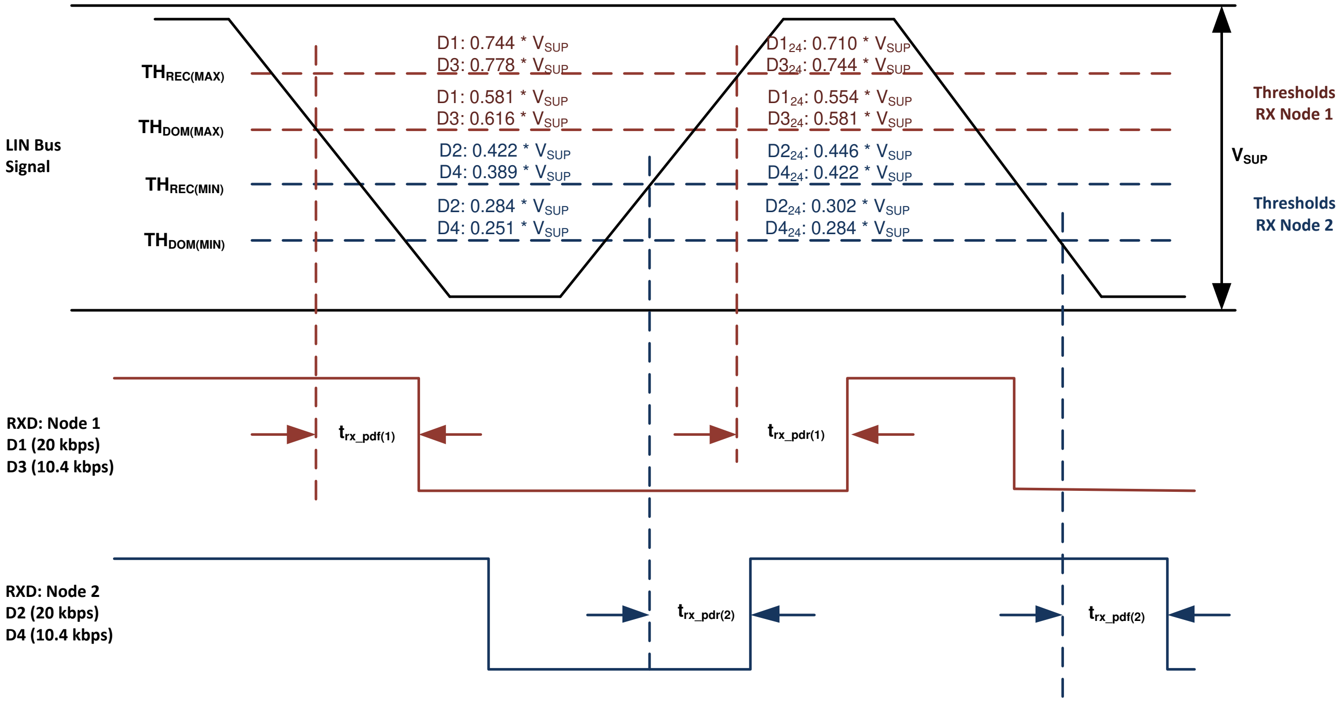


図 8-11. Propagation Delay

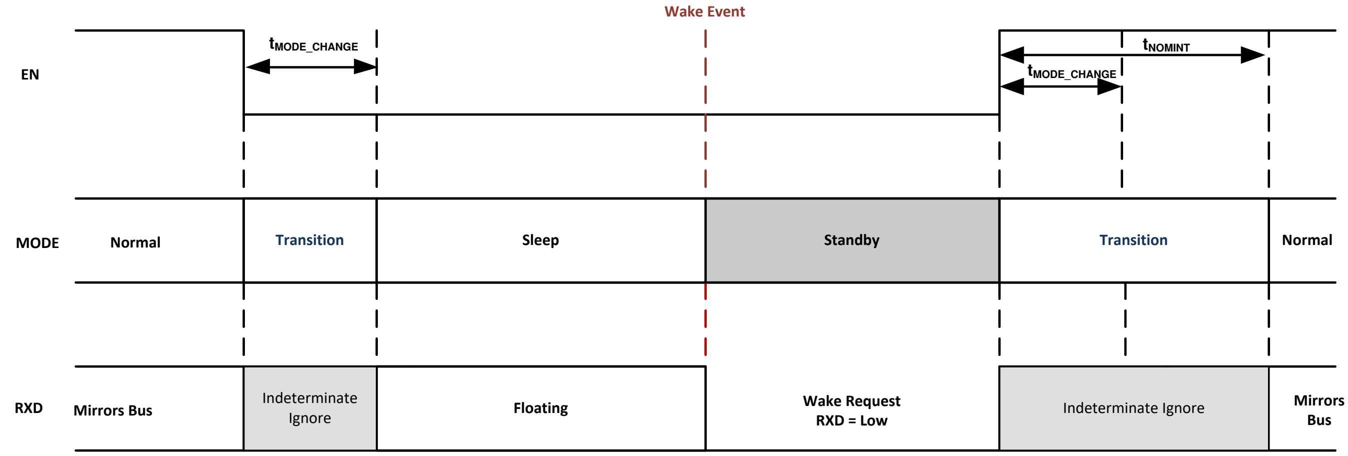


図 8-12. Mode Transitions

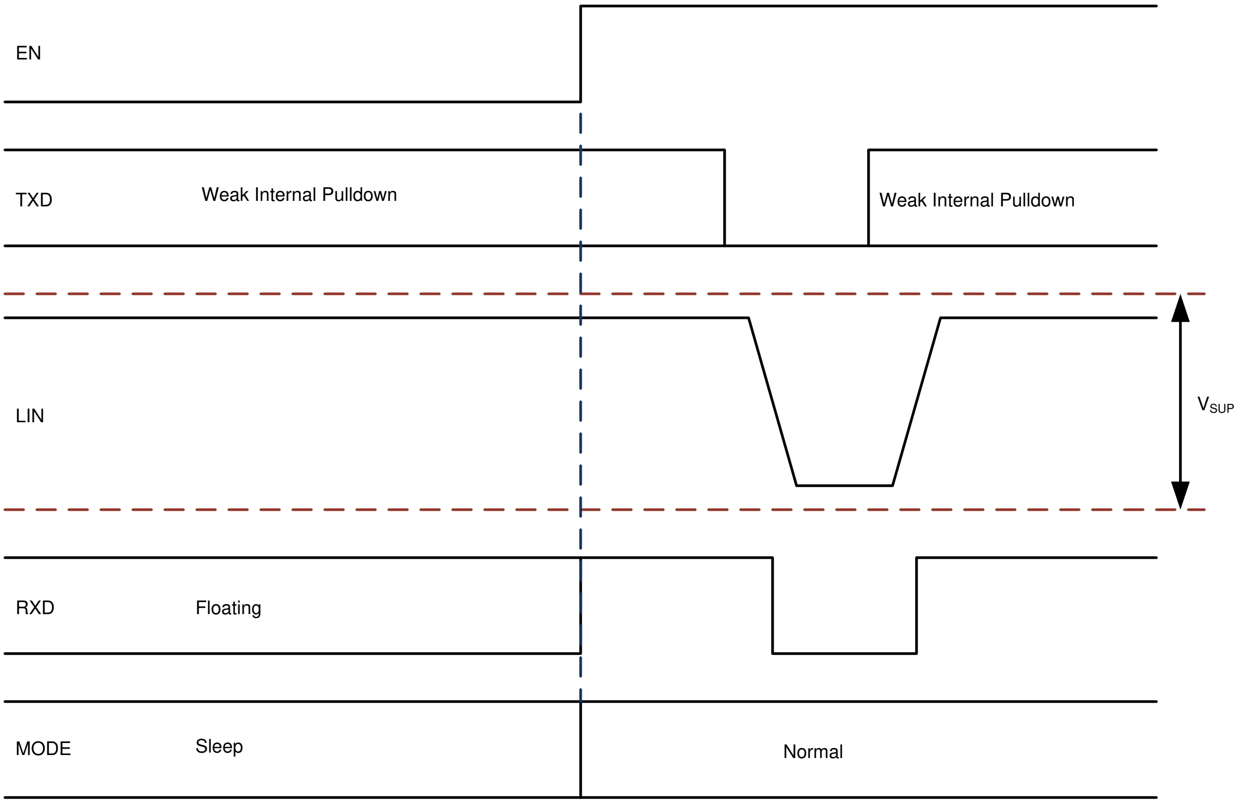


図 8-13. Wake-up Through EN

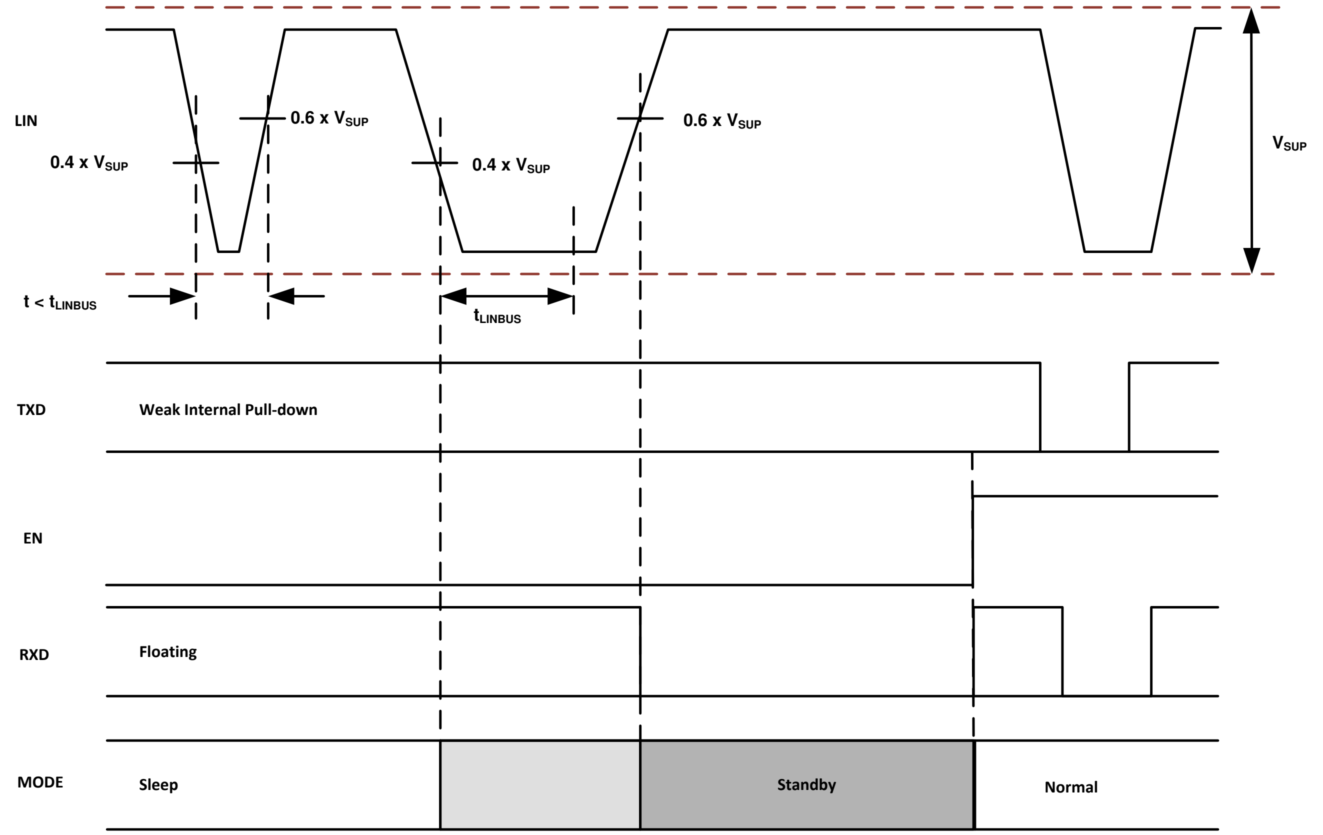


図 8-14. Wake-up through LIN

9 Detailed Description

9.1 Overview

The TLIN2021A-Q1 is a local interconnect network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602-1, SAE J2602-2, ISO 17987–4, and ISO 17987–7 standards. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol focused on automotive in-vehicle networking.

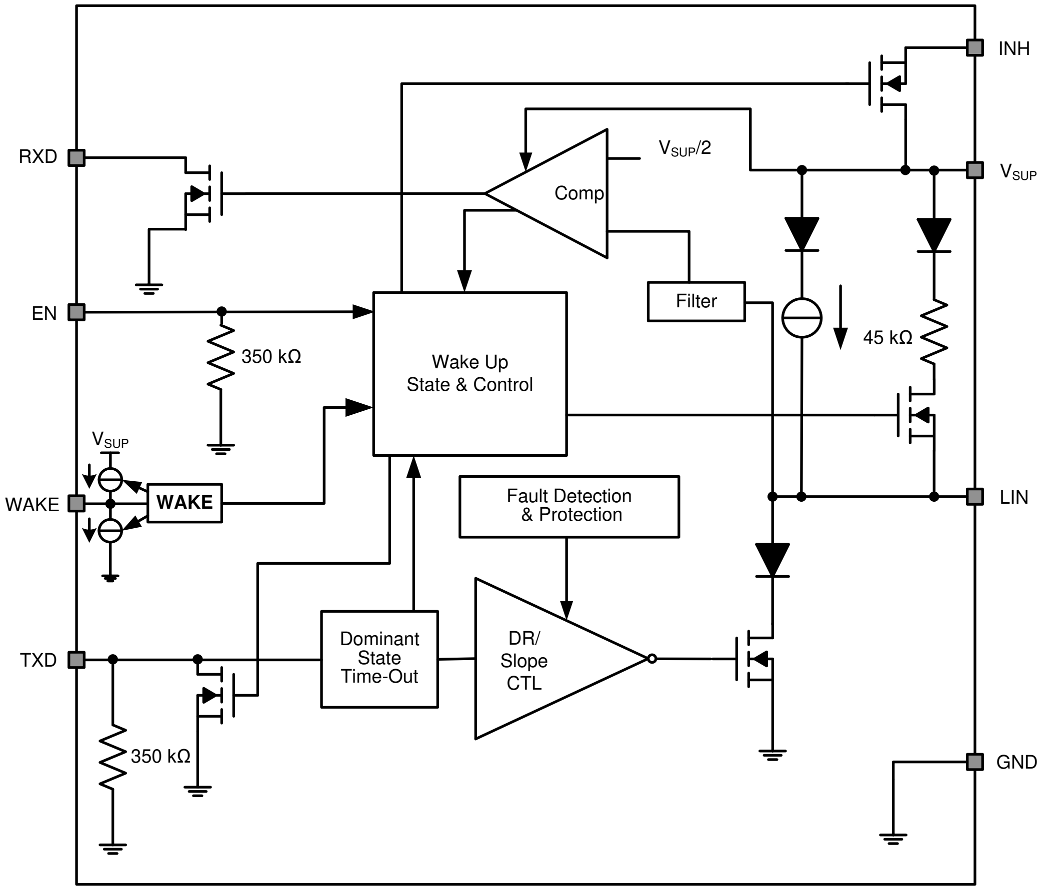
The device transmitter supports data rates from 2.4-kbps to 20-kbps and the receiver supports data rates up to 100-kbps for end-of-line programming. The device controls the state of the LIN bus through the TXD pin and reports the state of the bus through its open-drain RXD output pin. The LIN protocol data stream on the TXD input is converted by the device into a LIN bus signal using an optimized electromagnetic emissions current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microcontroller through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the transceivers internal pull-up resistor (45-kΩ) and a series diode. No external pull-up components are required for responder node applications. Commander node applications require an external pull-up resistor (1-kΩ) as well as a series diode per the LIN specification.

The device is designed to support 12-V and 24-V applications with a wide input voltage operating range and also supports low-power sleep mode. The device supports wake-up from low-power mode through wake over LIN, the WAKE pin, or the EN pin. The device allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a node through the INH output pin.

The TLIN2021A-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input.

The TLIN2021A-Q1 also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection. In the event of a fault condition, the transmitter is immediately switched off and remains off until the fault condition is removed.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LIN

This high voltage input/output pin is the single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 60-V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

9.3.1.1 LIN Transmitter Characteristics

The LIN transmitter has thresholds and AC switching parameters according to the LIN specification. The transmitter is a low-side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used in a commander node application per the LIN specification.

9.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates, > 100 kbps, than supported by LIN or SAEJ2602 specifications. This allows the TLIN2021A-Q1 to be used for high-speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1-kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification.

図 9-1 shows a commander node configuration and how the voltage levels are defined

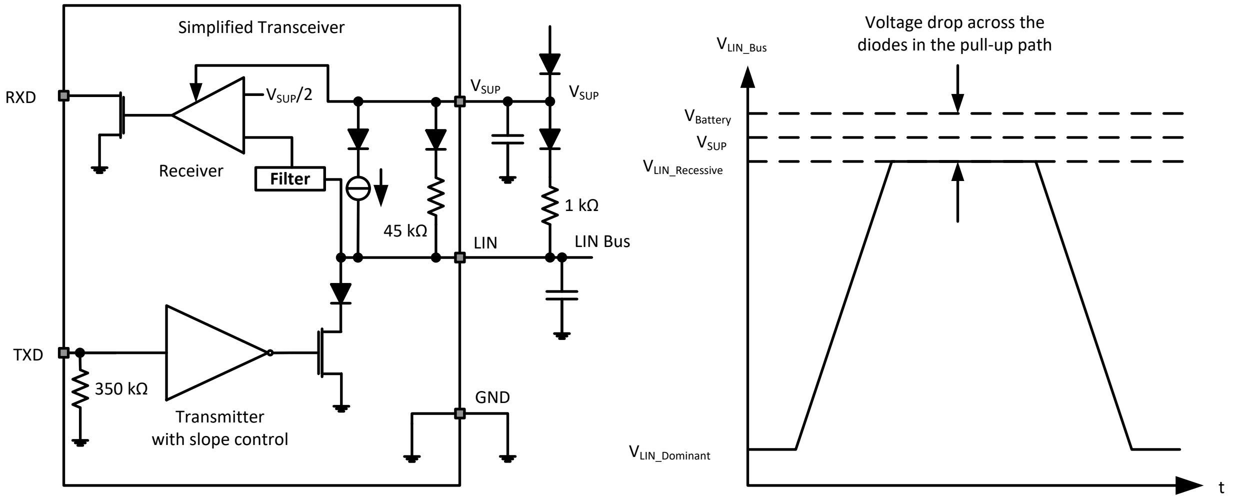


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図 9-1. Commander Node Configuration with Voltage Levels

9.3.2 TXD

TXD is the interface to the MCU LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground) and when TXD is high the LIN output is recessive (near V_{SUP}), see 図 9-1.

The TXD input structure is compatible with 3.3-V and 5-V microcontrollers and integrates a weak pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state time-out timer. When a change of state on the WAKE pin initiates a local wake-up event, the TXD pin is pulled hard to ground indicating a local wake-up event. The hard pull to ground is released upon the rising edge on the EN pin. If an external pull-up resistor is added to the TXD pin to the microcontroller's IO voltage then TXD is pulled high to indicate a remote wake-up event.

9.3.3 RXD

RXD is the interface to the MCU’s LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3-V and 5-V microcontrollers. If the microcontroller's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontroller's IO supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake-up request.

9.3.4 V_{SUP}

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode, see 図 9-1. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake-up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

9.3.7 WAKE

The WAKE pin is a high-voltage input used for the local wake-up (LWU) function. This function is explained further in セクション 9.4.4.1 section. The pin is defaulted to bidirectional edge trigger, meaning it recognizes a local wake-up (LWU) on a rising or falling edge of WAKE pin transition.

9.3.8 INH

The TLIN2021A-Q1 inhibit, INH, output pin can be used to control the enable of system power-management devices allowing for a significant reduction in battery quiescent current consumption while the application is in sleep mode. The INH pin has two states: driven high and high impedance. When the INH pin is driven high, the terminal shows V_{SUP} minus a diode voltage drop. In the high impedance state the output is left floating. The INH pin is high in the normal and standby modes and is low when in sleep mode. A 100 kΩ load can be added to the INH output to ensure a fast transition time from the driven high state to the low state and to also force the pin low when left floating.

The INH terminal should be considered a high-voltage logic terminal and not a power output. Thus should be used to drive the EN terminal of the systems power-management device and not used as a switch for the power-management supply itself. This terminal is not reverse battery protected and thus should not be connected outside the system module.

9.3.9 Local Faults

The TLIN2021A-Q1 has several protection features that are described as follows.

9.3.10 TXD Dominant Time-Out (DTO)

While the LIN driver is in active mode a TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit, t_{TXD_DTO}, expires the LIN driver is disabled releasing the bus line to the recessive level. This keeps the bus free for communication between other nodes on the network. The LIN driver is re-activated on the next dominant to recessive transition on the TXD terminal, thus clearing the dominant time-out. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, and the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. If EN pin is high at power-up, the TLIN2021A-Q1 enters normal mode. With the internal TXD connected low, the DTO timer starts. To avoid a t_{TXD_DTO} fault, a recessive signal should be put onto the TXD pin before the t_{TXD_DTO} timer expires, or the device should be into sleep mode by connecting EN pin low.

9.3.11 Bus Stuck Dominant System Fault: False Wake-Up Lockout

The TLIN2021A-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus clears the bus stuck dominant fault, preventing excessive current use, see 図 9-2 and 図 9-3.

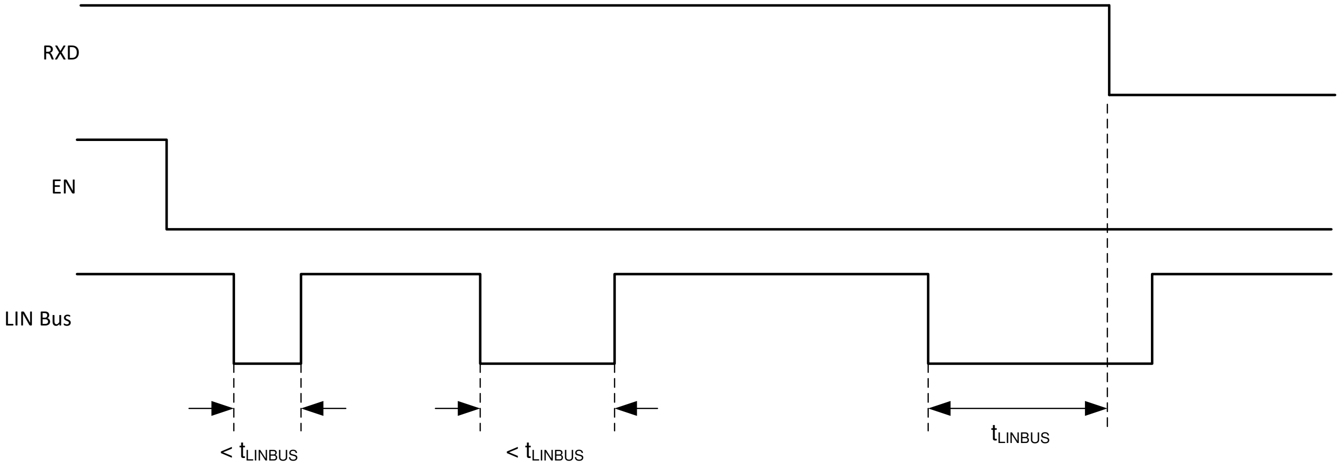

図 9-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake-up

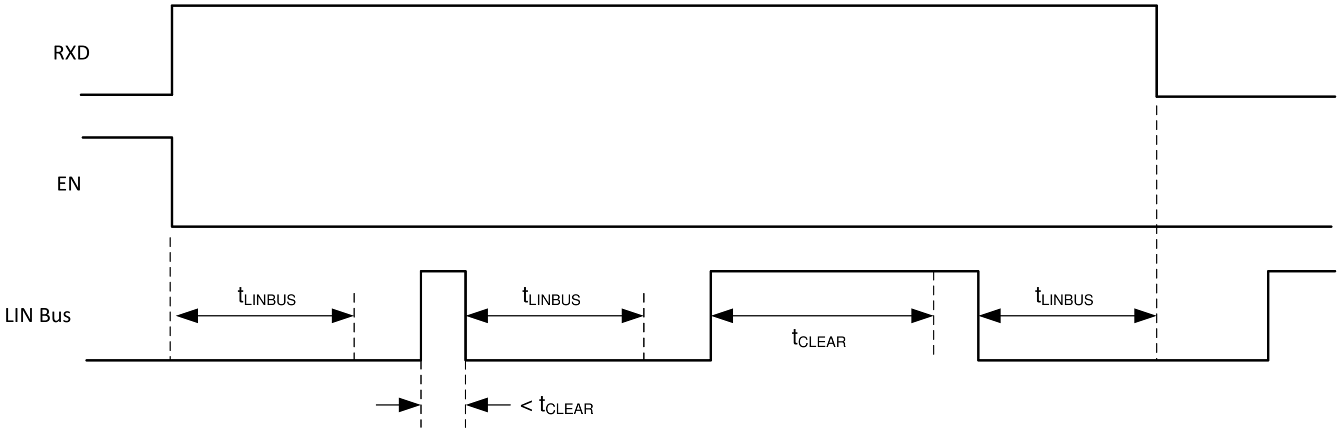

図 9-3. Bus Fault: Entering Sleep Mode With Bus Stuck Dominant Fault, Clearing, and Wake-up

9.3.12 Thermal Shutdown

The TLIN2021A-Q1 transmitter is protected by limiting the current. If the junction temperature, T_J, of the device exceeds the thermal shutdown threshold, $T_J > T_{SDR}$, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

9.3.13 Under Voltage on V_{SUP}

The device contains a power on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

9.3.14 Unpowered Device

In automotive applications, some LIN nodes in a system can be unpowered, ignition supplied, while others in the network remains powered by the battery. The device has extremely low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

9.4 Device Functional Modes

The TLIN2021A-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections describe these modes and how the device transitions between the different modes. 図 9-4 graphically shows the relationship while 表 9-1 shows the state of pins.

表 9-1. Operating Modes

MODE	EN	TXD	RXD	INH	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Weak pull-down	Floating	Floating	Weak current pull-up	Off	
Standby	Low	Weak pull-down if LIN bus wake-up; Strong pull-down if a local wake-up event (WAKE pin)	Low	High	45-kΩ	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	High: recessive state Low: dominant state	LIN Bus Data	High	45-kΩ	On	LIN transmission up to 20 kbps

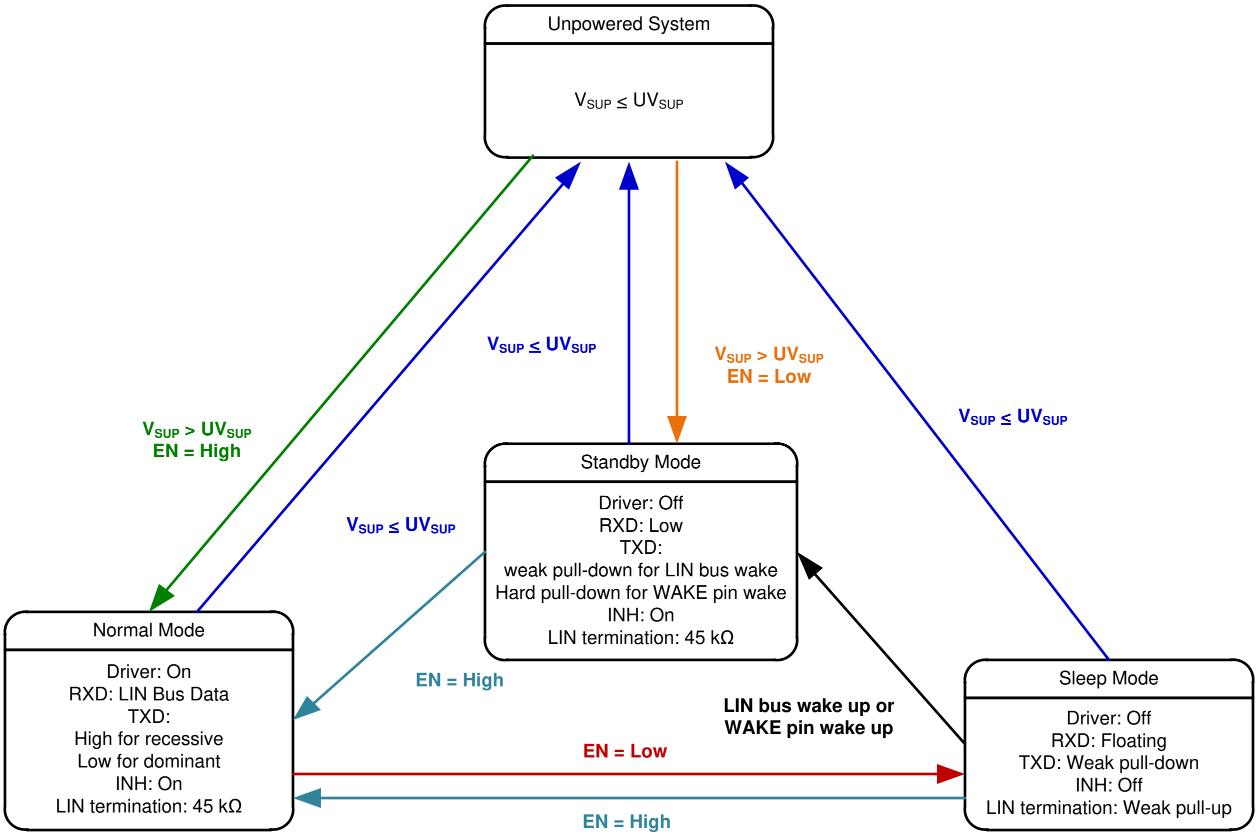

図 9-4. Operating State Diagram

9.4.1 Normal Mode

The EN pin controls the mode of the device. If the EN pin is high at power-up the device powers up in normal mode, if the EN is low at power-up the device powers up in standby mode. In normal mode the receiver and transmitter fully operational. The LIN transmitter transmits data from the LIN controller to the LIN bus up to the LIN specified maximum data rate of 20-kbps. The LIN receiver detects the data stream on the LIN bus up to data rates of 100-kbps and outputs the data on RXD output for the LIN controller. Upon an EN pin transition from low to high the TLIN2021A-Q1 transitions from sleep mode to normal mode in $t \geq t_{NOMINT}$.

9.4.2 Sleep Mode

Sleep mode is the lowest power mode of the TLIN2021A-Q1 and is only entered from normal mode when the EN pin transitions from high to low for $t > t_{MODE\_CHANGE}$. In sleep mode, the LIN driver and receiver are switched off, the LIN bus is weakly pulled up, and the transceiver cannot send or receive data. The INH pin is switched to a floating output in sleep mode causing any system power elements controlled by the INH pin to be switched off thus reducing the system power consumption. While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off to minimize power loss if LIN is short circuited to ground.
- A weak current pull-up is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input, WAKE pin and LIN wake-up receiver are active.

The TLIN2021A-Q1 supports three methods for wake-up from sleep mode:

- Wake-up over the LIN bus via the LIN wake-up receiver.
- Local wake-up via the WAKE pin.
- Local wake-up via the EN pin. The EN pin must be set high for $t > t_{NOMINT}$ in order for the device to wake-up.

9.4.3 Standby Mode

Standby mode is entered whenever a wake-up event occurs through LIN bus or the WAKE pin while the device is in sleep mode. In standby mode, the LIN bus responder termination circuit, 45-kΩ, is on. When a wake-up event occurs and the TLIN2021A-Q1 enters standby mode the RXD pin is driven low signaling the wake-up event to the LIN controller.

The TLIN2021A-Q1 exits standby mode and transitions to normal mode when the EN pin is set high for longer than t_{MODE_CHANGE} where the normal LIN transmitter and receiver are fully operational and bi-directional communication is possible.

9.4.4 Wake-Up Events

There are three ways to wake-up the TLIN2021A-Q1 from sleep mode:

- Remote wake-up initiated by the falling edge of a recessive-to-dominant state transition on the LIN bus where the dominant state is held longer than t_{LINBUS} filter time. After the t_{LINBUS} filter time has been met a rising edge on the LIN bus going from dominant-to-recessive initiates a remote wake-up event. The pattern and t_{LINBUS} filter time used for the LIN wake-up prevents noise and bus stuck dominant faults from causing false wake requests.
- A local wake-up event due to the EN pin being set high for $t > t_{MODE\_CHANGE}$.
- A local wake-up event due to a change in voltage level on the WAKE pin for $t > t_{WAKE}$

9.4.4.1 Local Wake-Up (LWU) via WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage input which can be used for local wake-up (LWU) requests via a voltage transition. A LWU event is triggered on either a low-to-high or high-to-low transition since it has bi-directional input thresholds. The WAKE pin could be used with a switch to V_{SUP} or to ground. If the terminal is unused it should be pulled to V_{SUP} or ground to avoid unwanted parasitic wake-up events. When a LWU event takes place the TXD pin is pulled hard to GND letting the LIN controller know that the wake-up event was due to the WAKE pin and not a wake over LIN event.

The LWU circuitry is active in standby mode and sleep mode. If a valid LWU event occurs in standby mode, the device remains in standby mode and drive the RXD output low. If a valid LWU event occurs in sleep mode, the device transitions to standby mode and drives the RXD output low. The LWU circuitry is not active in normal mode. To minimize system-level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of $t_{WAKE(MIN)}$. A constant high level on WAKE has an internal pull-up to V_{SUP}, and a constant low level on WAKE has an internal pull-down to GND.

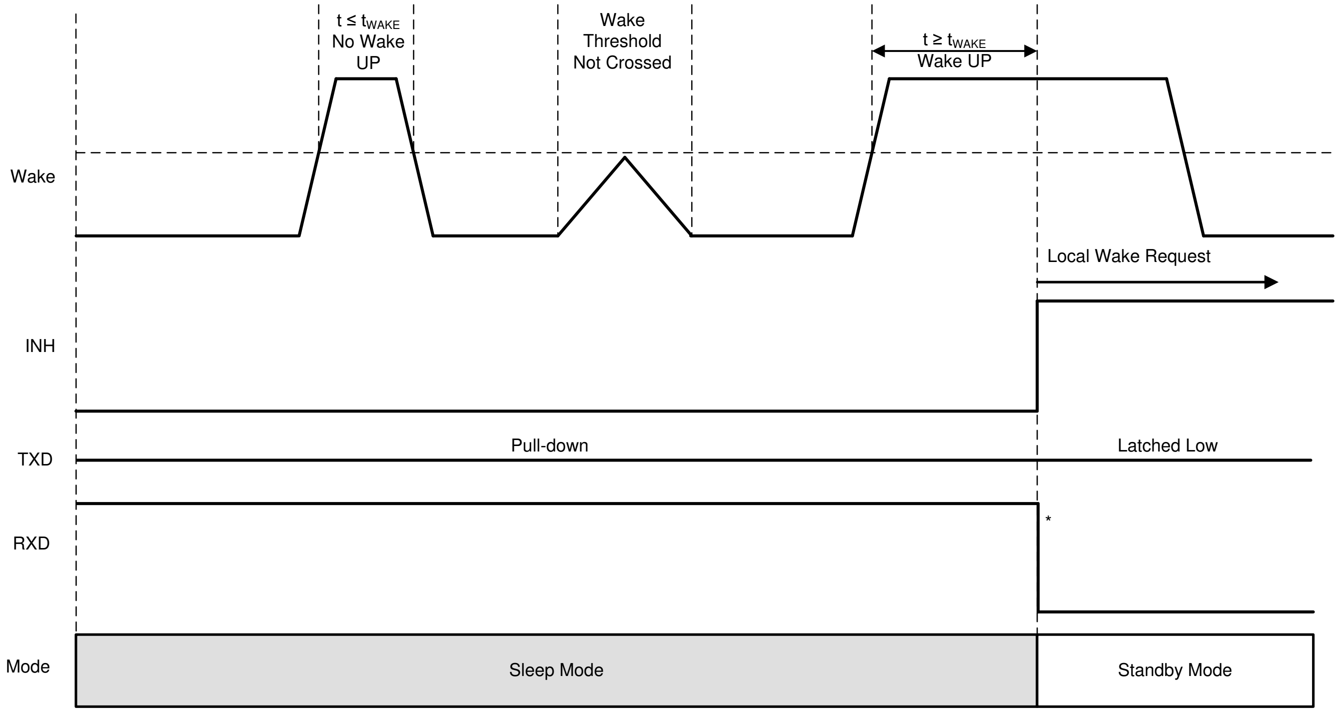

図 9-5. Local Wake-Up – Rising Edge

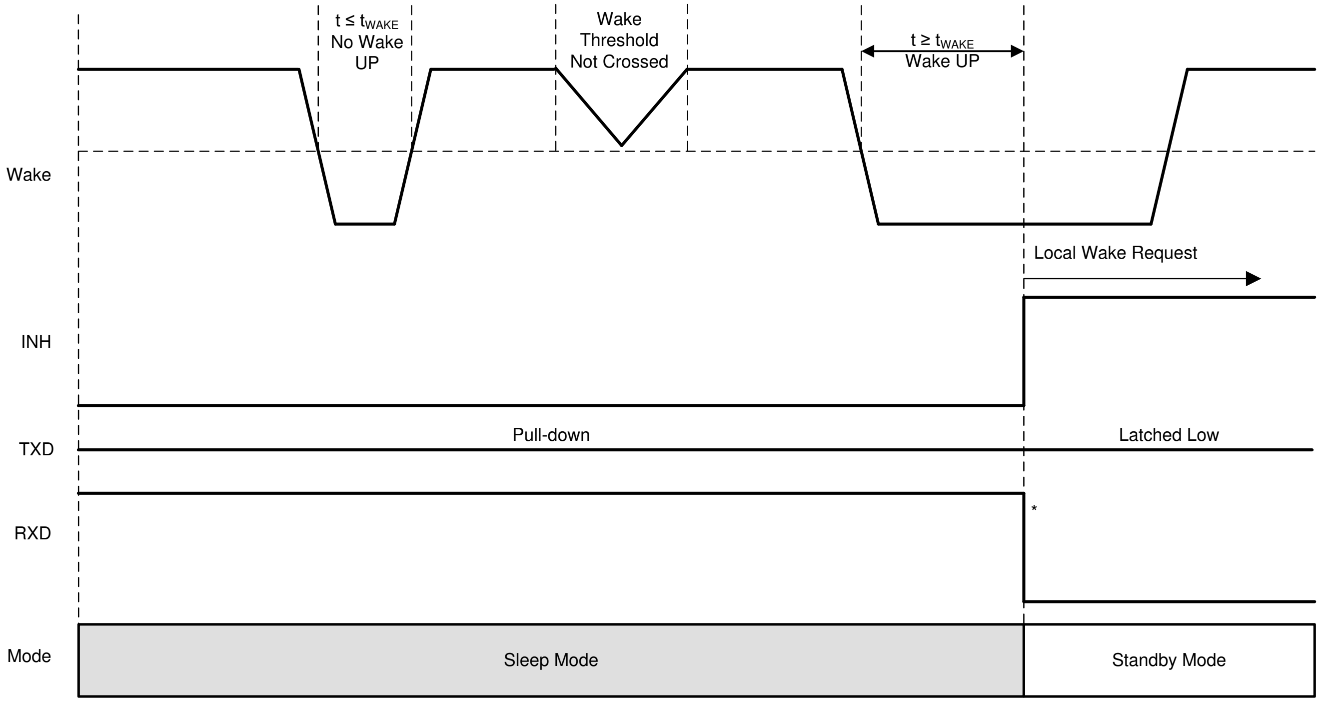

図 9-6. Local Wake-Up – Falling Edge

9.4.4.2 Wake-Up Request (RXD)

When the TLIN2021A-Q1 encounters a wake-up event from the WAKE pin or the LIN bus, the RXD output is driven low until EN is asserted high, the device enters normal mode. Once the device enters normal mode, the wake-up event is cleared, and the RXD output is released. The RXD output is fully operational and reflects the receiver output from the LIN bus.

10 Application Information Disclaimer

Note

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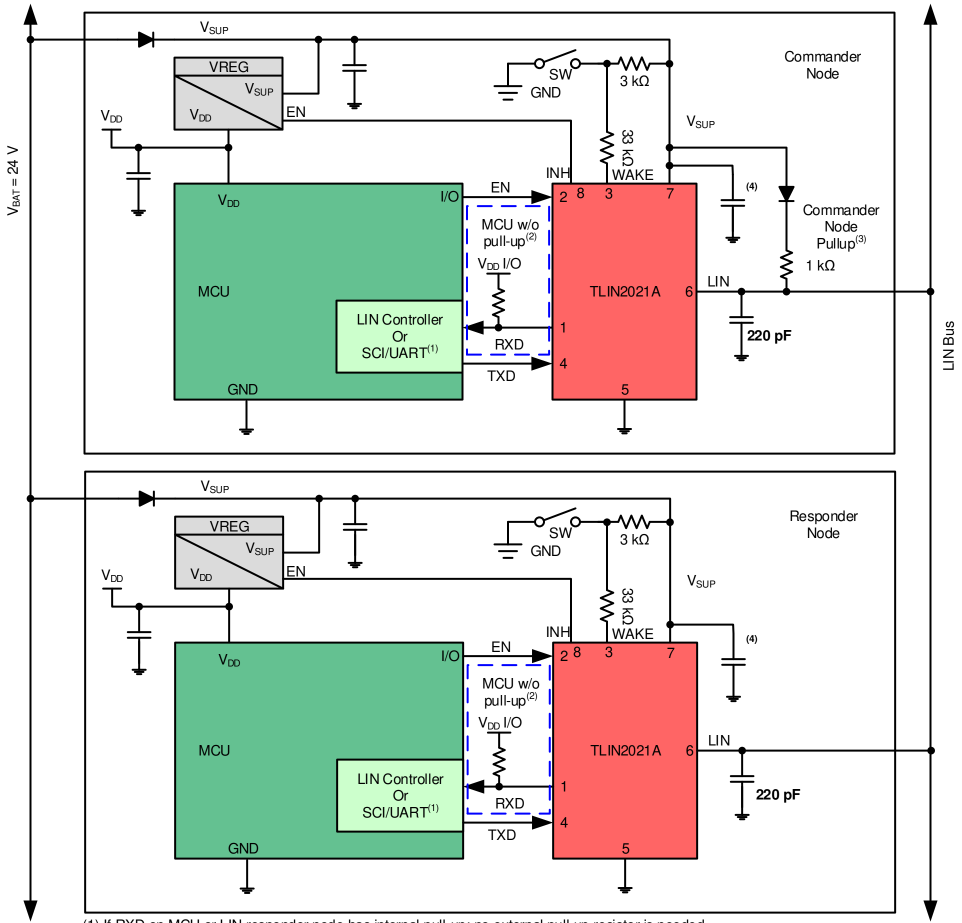
10.1 Application Information

The TLIN2021A-Q1 can be used in both a responder node application and a commander node application in a LIN network.

10.2 Typical Application

The device integrates a 45-kΩ pull-up resistor and series diode for responder node applications. For commander node applications, an external 1-kΩ pull-up resistor with series blocking diode can be used. 図 10-1 shows the device being used in both commander node and responder node applications.



(1) If RXD on MCU or LIN responder node has internal pull-up; no external pull-up resistor is needed.
(2) If RXD on MCU or LIN responder node does not have an internal pull-up requires external pull-up resistor.
(3) Commander node applications require and external 1 kΩ pull-up resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

図 10-1. Typical LIN Bus

10.2.1 Design Requirements

The RXD output structure is an open-drain output stage which allows the TLIN2021A-Q1 to be used with 3.3-V and 5-V controllers. If the RXD pin of the controller does not have an integrated pull-up, an external pull-up resistor to the controller's IO voltage is required. The external pull-up resistor value should be between 1-kΩ to 10-kΩ. The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

10.2.2 Detailed Design Procedures

10.2.2.1 Normal Mode Application Note

When using the TLIN2021A-Q1 in systems which are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE} has been met. This is shown in 図 8-12

10.2.2.2 TXD Dominant State Time-Out Application Note

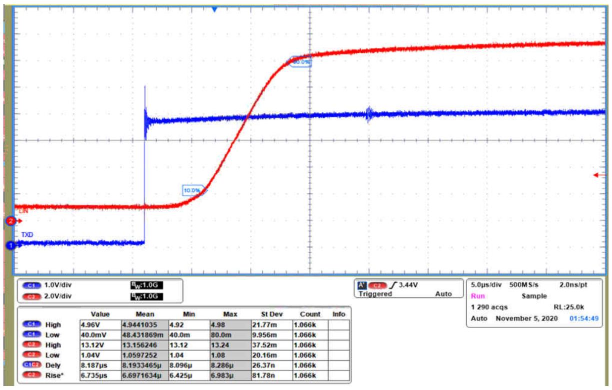
The maximum dominant TXD time allowed by the TXD dominant state time-out limits the minimum possible data rate of the device. The LIN protocol has different constraints for commander node and responder node applications thus there are different maximum consecutive dominant bits for each application case thus different minimum data rates.

10.2.2.3 Standby Mode Application Note

If the TLIN2021A-Q1 detects an under voltage on V_{SUP} the RXD pin transitions low signaling to the controller that the TLIN2021A-Q1 is in standby mode. The transceiver should be returned to sleep mode for the lowest power state.

10.2.3 Application Curves

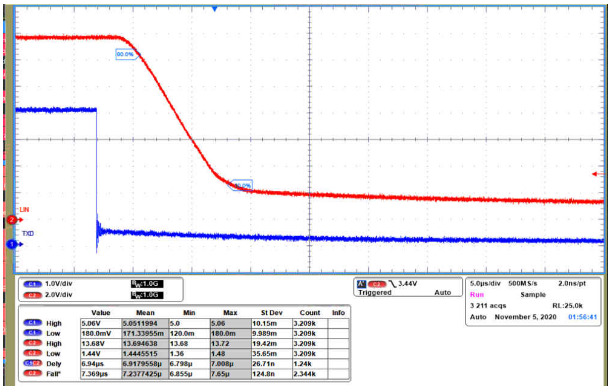
図 10-2 and 図 10-3 show the propagation delay from the TXD pin to the LIN pin for the dominant to recessive and recessive to dominant edges. Device was configured in commander mode with external pull-up resistor (1 kΩ) and 680 pF bus capacitance.



5.0µs/div 500MS/s 2.0ns/pt
Run Sample
1 290 acqs RL:25.0k
Auto November 5, 2020 01:54:49

	Value	Mean	Min	Max	St Dev	Count	Info
C1 High	4.96V	4.9441035	4.92	4.98	21.77m	1.066k	
C1 Low	40.0mV	48.431869m	40.0m	80.0m	9.956m	1.066k	
C2 High	13.12V	13.156246	13.12	13.24	37.52m	1.066k	
C2 Low	1.04V	1.0597252	1.04	1.08	20.16m	1.066k	
C1C2 Dely	8.187µs	8.1933465µ	8.096µ	8.286µ	26.37n	1.066k	
C2 Rise*	6.735µs	6.6971634µ	6.425µ	6.983µ	81.78n	1.066k	

図 10-2. Dominant To Recessive Propagation Delay



5.0µs/div 500MS/s 2.0ns/pt
Run Sample
3 211 acqs RL:25.0k
Auto November 5, 2020 01:56:41

	Value	Mean	Min	Max	St Dev	Count	Info
C1 High	5.06V	5.0511994	5.0	5.06	10.15m	3.209k	
C1 Low	180.0mV	171.33955m	120.0m	180.0m	9.989m	3.209k	
C2 High	13.68V	13.694638	13.68	13.72	19.42m	3.209k	
C2 Low	1.44V	1.4445515	1.36	1.48	35.65m	3.209k	
C1C2 Dely	6.94µs	6.9179558µ	6.798µ	7.008µ	26.71n	1.24k	
C2 Fall*	7.369µs	7.2377425µ	6.855µ	7.65µ	124.8n	2.344k	

図 10-3. Recessive to Dominant Propagation Delay

11 Power Supply Recommendations

The TLIN2021A-Q1 was designed to operate directly from a car battery, or any other DC supply ranging from 4.5-V to 45-V. The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements. Device has been designed and tested to support supply ramp rates equal to or slower than 0.5 V/μs.

12 Layout

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1(RXD):** The RXD pin is an open-drain output and requires and external pull-up resistor in the range of 1-kΩ and 10-kΩ to function properly. If the controller paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the supply voltage for the controller.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in low-power sleep mode. If this feature is not used, the pin should be connected to the supply voltage for the controller through a series resistor using a pull-up value between 1-kΩ and 10-kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (WAKE):** SW1 is oriented in a low-side configuration which is used to implement a local WAKE event. The series resistor R5 is needed for protection against over current conditions as it limits the current into the WAKE pin when the ECU has lost its ground connection. The pull-up resistor R4 is required to provide sufficient current during stimulation of a WAKE event. In this layout example R4 is set to 3-kΩ and R5 is set to 33-kΩ.
- **Pin 4 (TXD):** The TXD pin is the transmit input signal to the device from the controller. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to help filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** The LIN pin connects to the TLIN2021A-Q1 to the LIN bus. For responder node applications a 220 pF capacitor to ground is implemented. For commander node applications an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin, see Typical LIN Bus.
- **Pin 7 (V_{SUP}):** This is the supply pin for the device. A 100-nF capacitor should be placed close to the V_{SUP} supply pin for local power supply decoupling.
- **Pin 8 (INH):**The INH pin is used for system power-management. A 100-kΩ load can be added to the INH output to ensure a fast transition time from the driven high state to the low state and to also force the pin low when left floating.

Note

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

12.2 Layout Example

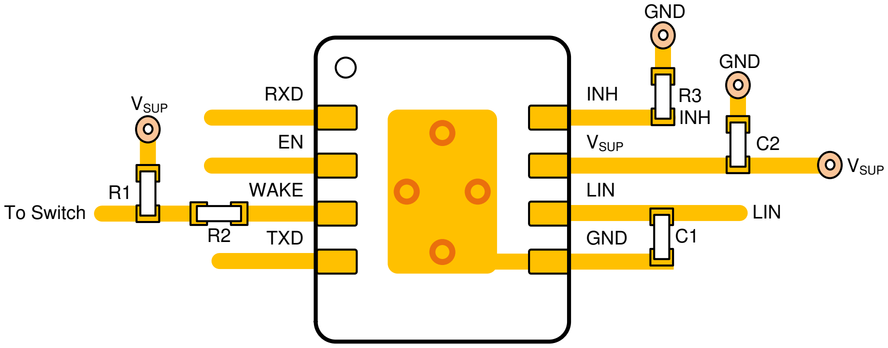


図 12-1. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN2021ADDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JJF
TLIN2021ADDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JJF
TLIN2021ADRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL021A
TLIN2021ADRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL021A
TLIN2021ADRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2021A
TLIN2021ADRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2021A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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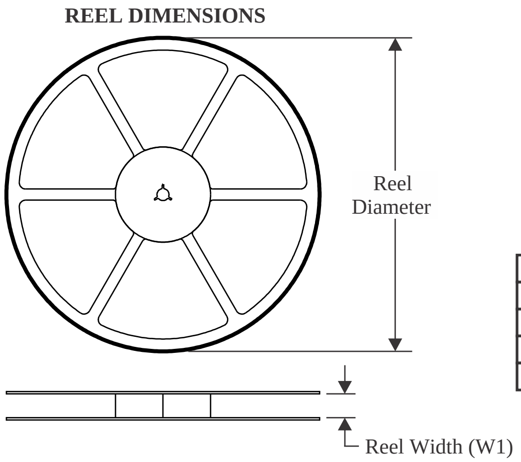
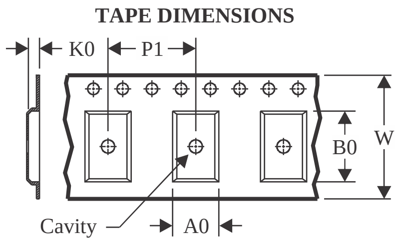
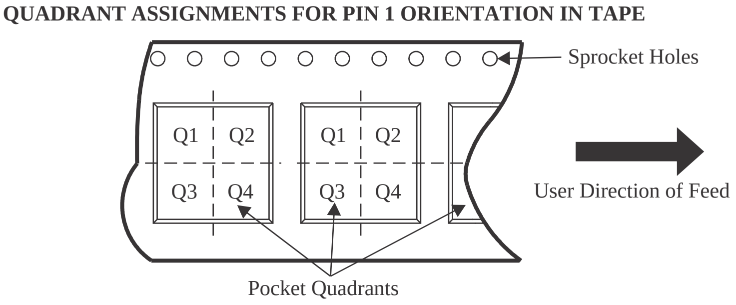
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





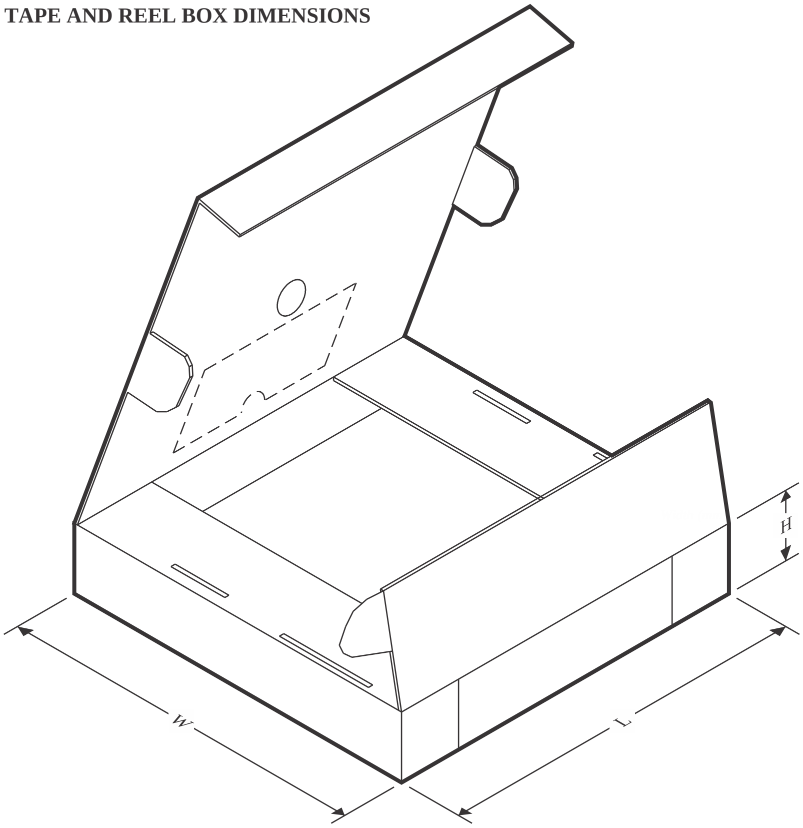
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN2021ADDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLIN2021ADRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TLIN2021ADRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN2021ADDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLIN2021ADRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN2021ADRQ1	SOIC	D	8	2500	353.0	353.0	32.0

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

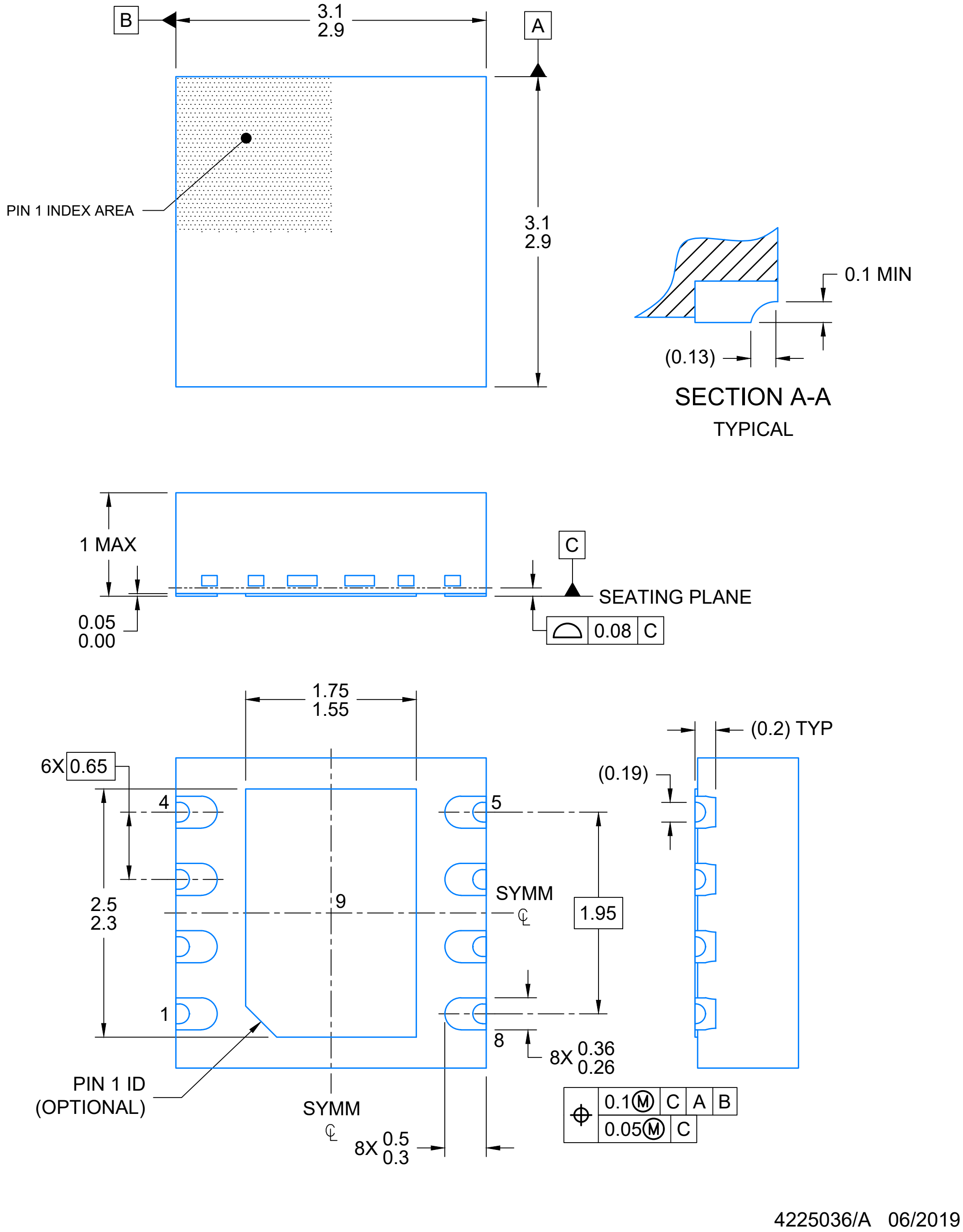
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRB0008J

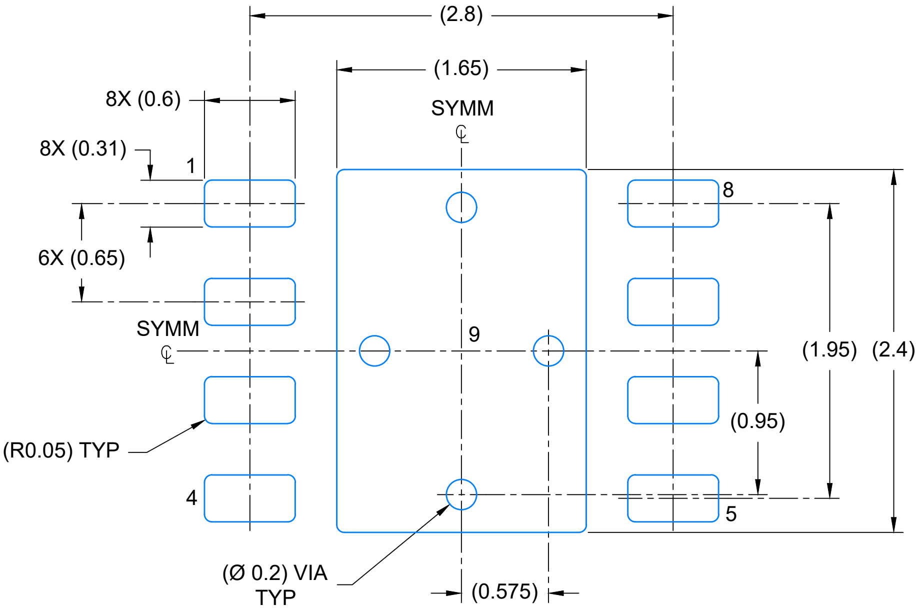
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

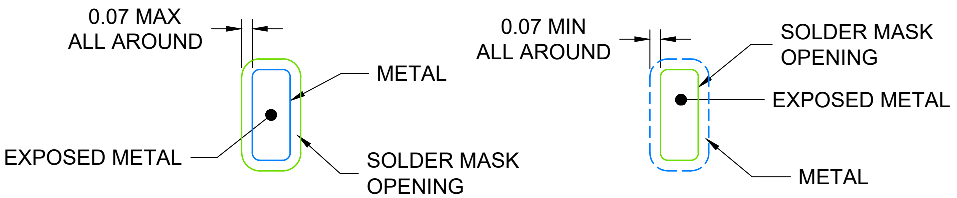


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

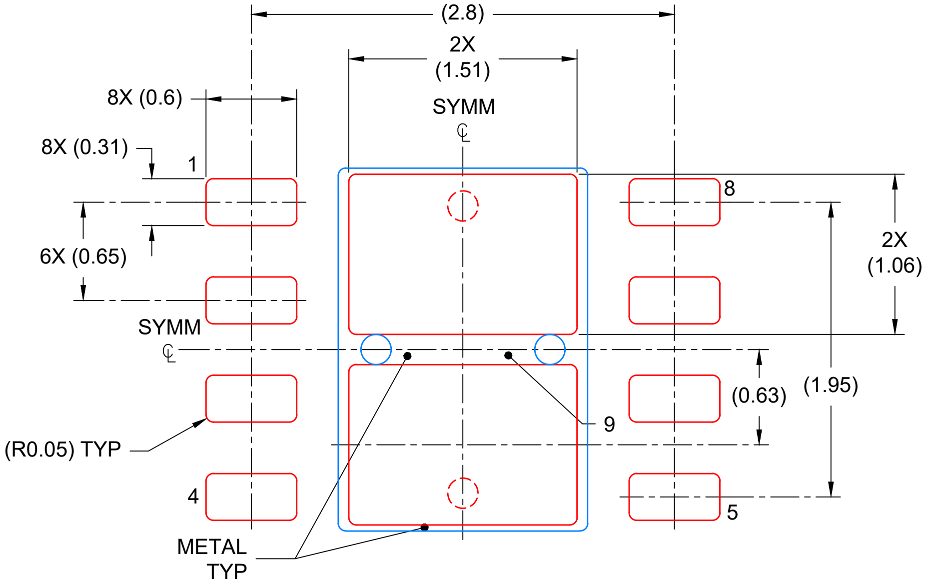
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

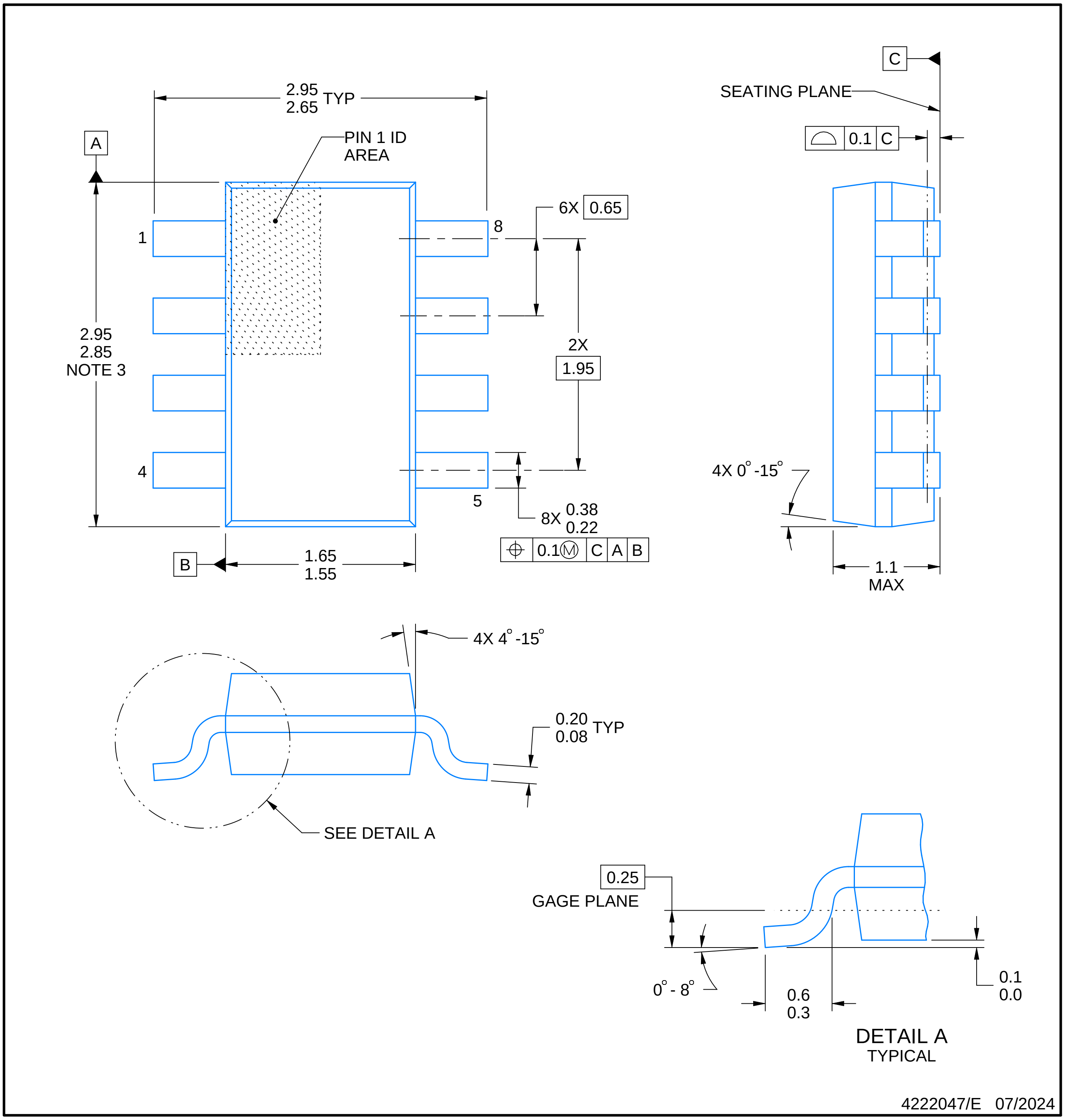
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

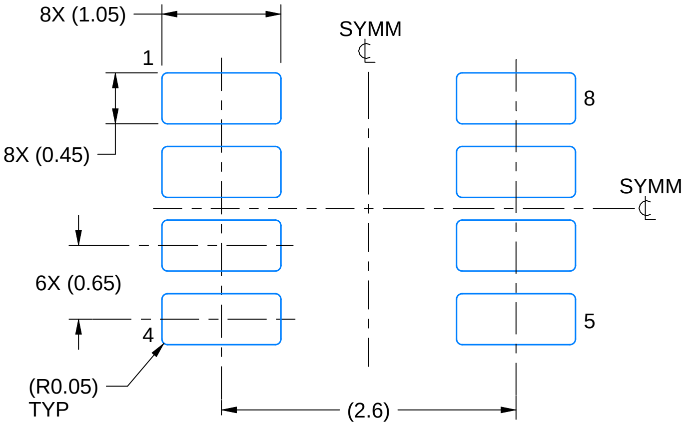
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

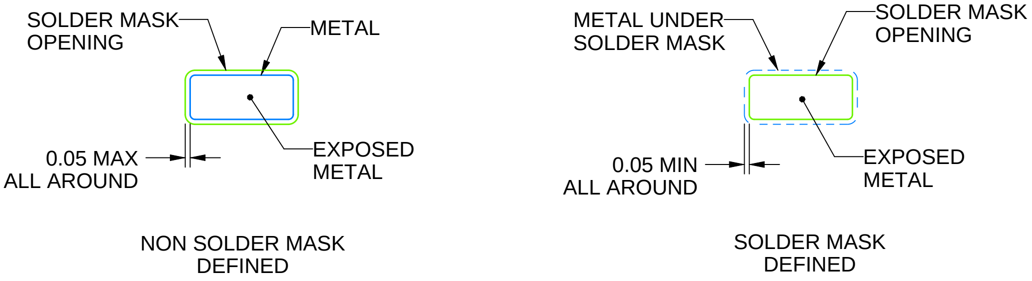


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



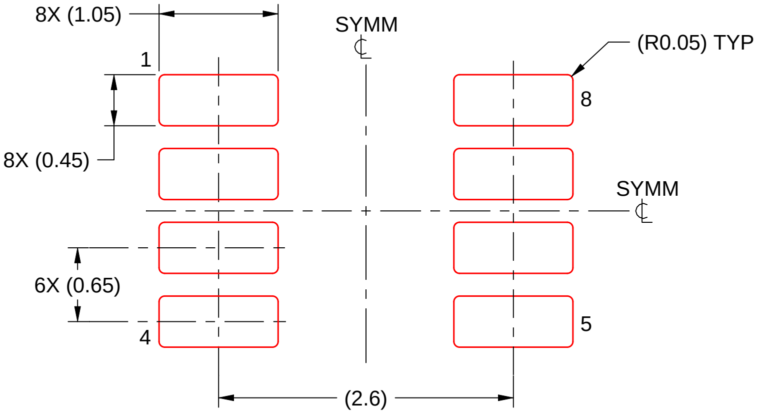
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

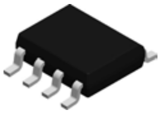


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

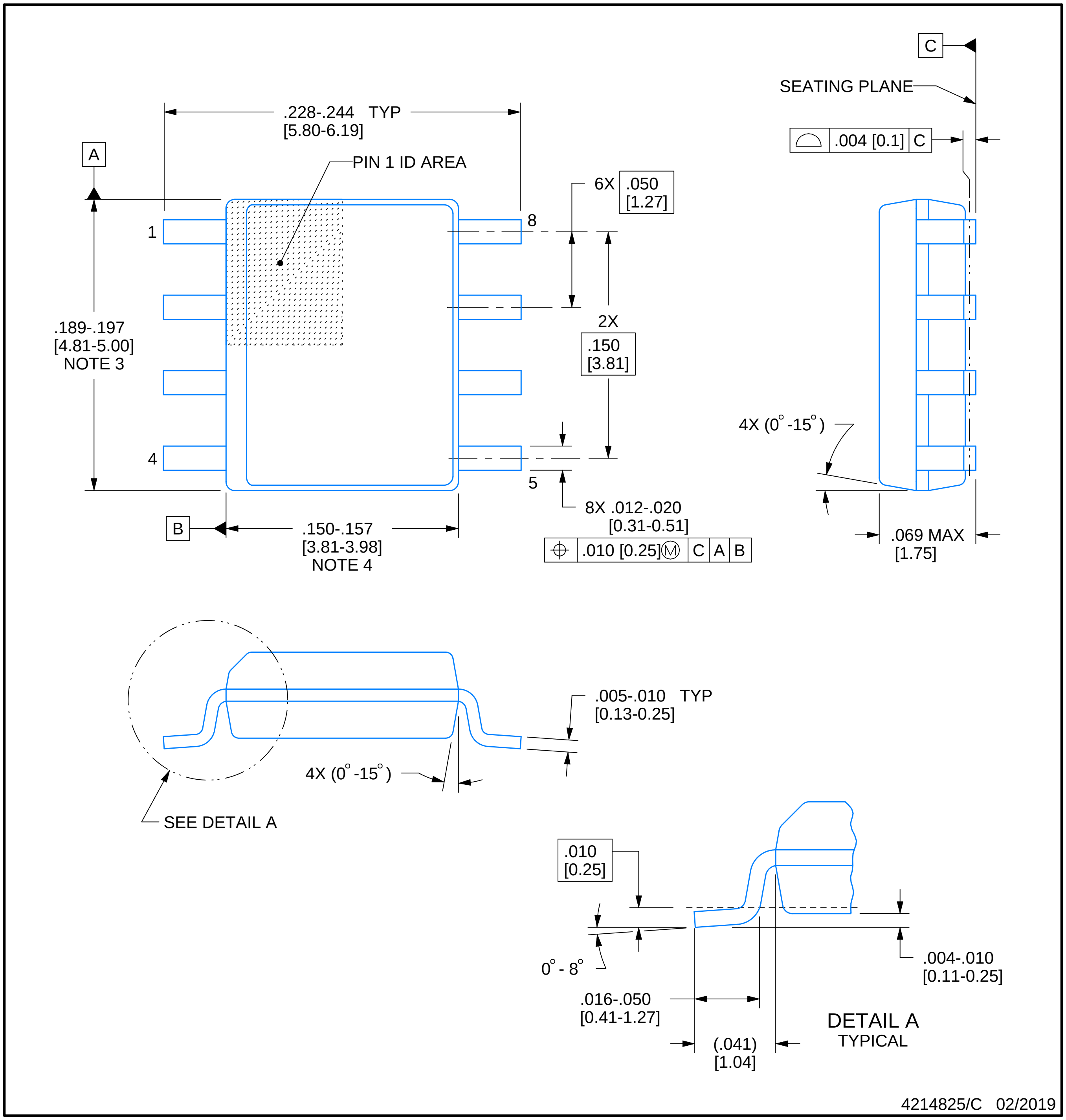
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

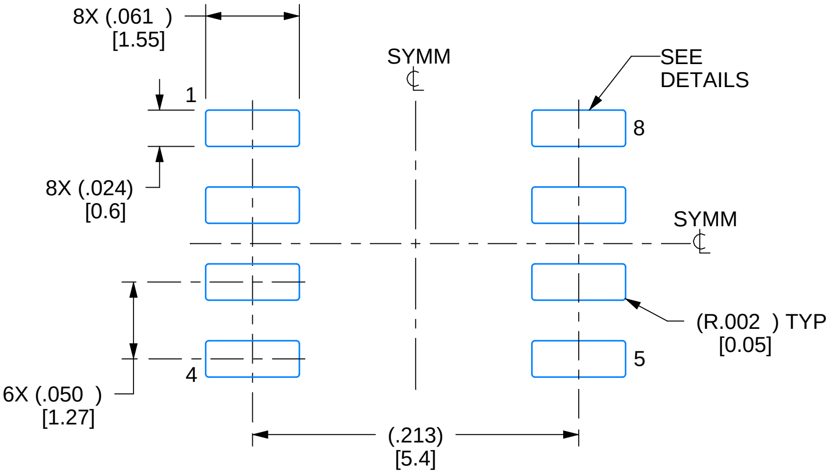
SMALL OUTLINE INTEGRATED CIRCUIT



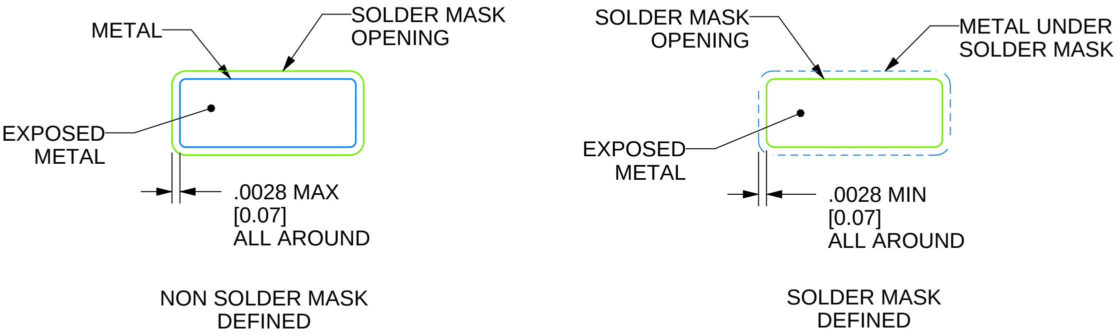
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



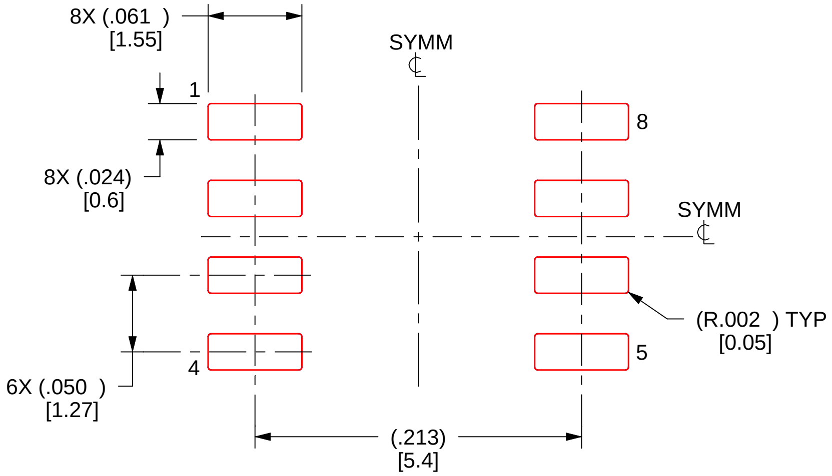
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月