参考資料

TEXAS INSTRUMENTS

TLV07

JAJSDQ3A – JULY 2017 – REVISED AUGUST 2017

TLV07 36V高精度レール・ツー・レール出力オペアンプ

1 特長

- 低オフセット電圧: 100µV (最大値)
- レール・ツー・レール出力
- 低ノイズ: 19nV/√Hz
- ユニティ・ゲイン安定
- RFIフィルタ付きの入力
- 入力範囲は負の電源電圧にも対応
- レール・ツー・レール出力
- ゲイン帯域幅: 1MHz
- 低い静止電流: 930µA
- 完全な工業用温度範囲: –40℃～+125℃
- 業界標準の8ピンSOICパッケージで供給

2 アプリケーション

- バッテリ・テスタ
- 電源モジュールのトラッキング・アンプ
- 商業施設の電源
- トランスデューサ・アンプ
- 温度測定
- ひずみゲージ・アンプ

3 概要

TLV07は、36V単電源、低ノイズの高精度オペアンプで、TIのレーザ・トリム・オペアンプ技術を使用して製造されています。各アンプの入力オフセット電圧は製造時にトリムされ、100µV (最大値)の低オフセット電圧を実現します。

TLV07は、レール・ツー・レール出力、低オフセット電圧(最大±100µV)、1MHzの帯域幅を含む、卓越したDC精度とAC性能を提供します。TLV07は、最大200pFの容量性負荷に対してG = 1で安定します。入力は負のレールより100mV下、および正のレールから2V以内で動作できます。この広い入力電圧範囲と120dBという高CMRRを兼ね備えたTLV07は、非反転構成での動作に適しています。

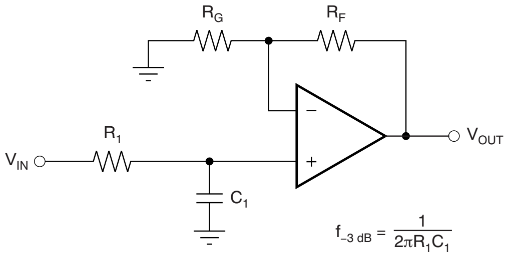
TLV07オペアンプは、-40℃～+125℃での動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLV07	SOIC (8)	4.90mm×3.91mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

単極ローパス・フィルタ、ゲイン付き



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

目次

4 改訂履歴

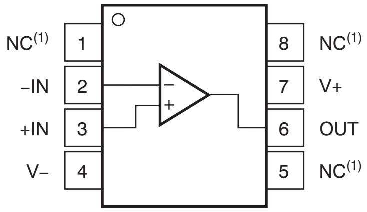
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年7月発行のものから更新 **Page**

- 生産データを用いたデータシートの初期リリース 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



(1) NC- no internal connection

Pin Functions: TLV07

NAME	NO.	I/O	DESCRIPTION
–IN	2	I	Negative (inverting) input
+IN	3	I	Positive (non-inverting) input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.[1]

	MIN	MAX	UNIT
Supply voltage	–20	20	V
Single supply voltage		40	V
Signal input pin voltage	(V–) – 0.5	(V+) + 0.5	V
Signal input pin current	–10	10	mA
Output short-circuit current[2]	Continuous		
Operating ambient temperature, T_A	–40	125	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V_S = V+ – V–)	2.7	36	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information: TLV07

THERMAL METRIC		TLV07 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

6.5 Electrical Characteristics

at T_A = 25°C, V+ = +15 V, V- = -15 V, $V_{CM} = V_{OUT} = V_S / 2$, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			50	±100	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		±0.9		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 36 V		0.3		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±40		pA
		T_A = –40°C to 125°C		±3		nA
I_{OS}	Input offset current			±4		pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2.7		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		19		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) - 0.1 V < V_{CM} < (V+) – 2 V	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			1		MHz
SR	Slew rate	G = 1		0.4		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step		20		µs
		To 0.01% (12-bit), V_S = ±18 V G = 1 10-V step		28		µs
OUTPUT						
V_O	Voltage output swing from rail	R_L = 10 kΩ		120		mV
I_{SC}	Short-circuit current			17		mA
R_O	Open-loop output resistance	f = 1 MHz I_O = 0 A		900		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 A		930	1800	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–40		125	°C

6.6 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

表 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	図 1
Offset Voltage Drift Distribution	図 2
Offset Voltage vs Temperature	図 3
Offset Voltage vs Common-Mode Voltage	図 4
Offset Voltage vs Power Supply	図 5
I_B and I_{OS} vs Common-Mode Voltage	図 6
Input Bias Current vs Temperature	図 7
Output Voltage Swing vs Output Current (Maximum Supply)	図 8
CMRR and PSRR vs Frequency (Referred-to-Input)	図 9
CMRR vs Temperature	図 10
PSRR vs Temperature	図 11
0.1-Hz to 10-Hz Noise	図 12
Input Voltage Noise Spectral Density vs Frequency	図 13
THD+N Ratio vs Frequency	図 14
THD+N vs Output Amplitude	図 15
Quiescent Current vs Temperature	図 16
Quiescent Current vs Supply Voltage	図 17
Open-Loop Gain and Phase vs Frequency	図 18
Closed-Loop Gain vs Frequency	図 19
Open-Loop Gain vs Temperature	図 20
Open-Loop Output Impedance vs Frequency	図 21
No Phase Reversal	図 22
Positive Overload Recovery	図 23
Negative Overload Recovery	図 24
Small-Signal Step Response	図 25, 図 26
Large-Signal Step Response	図 27, 図 28
Large-Signal Settling Time	図 29
Short-Circuit Current vs Temperature	図 30
Maximum Output Voltage vs Frequency	図 31
EMIRR IN+ vs Frequency	図 32

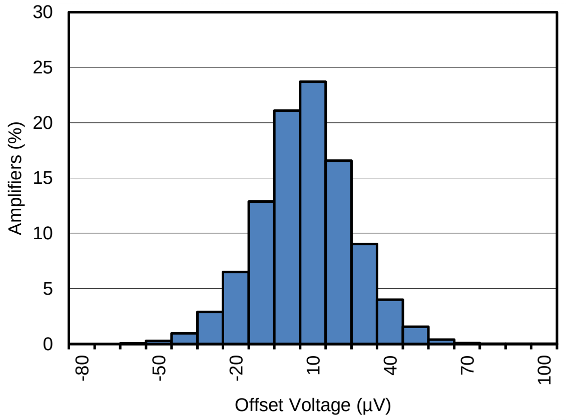


図 1. Input Offset Voltage Distribution

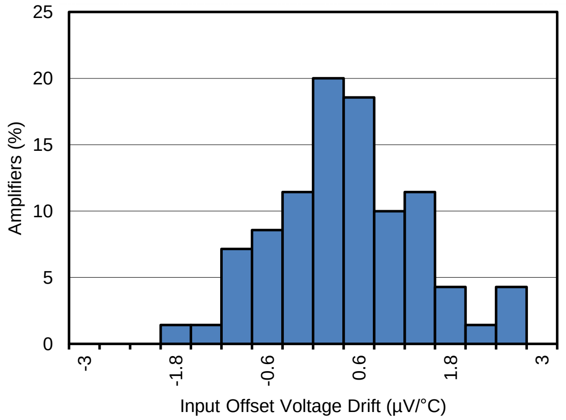


図 2. Input Offset Voltage Drift Distribution

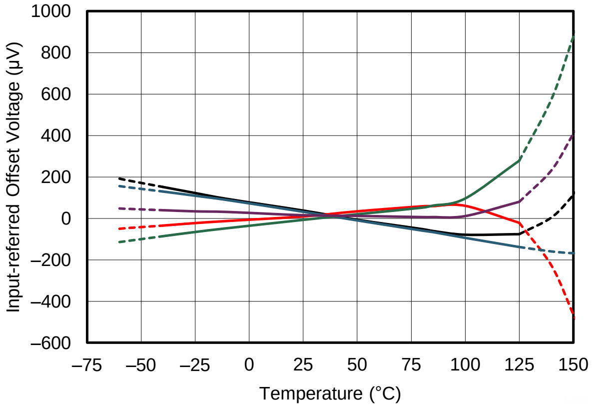


図 3. Input Offset Voltage vs Temperature

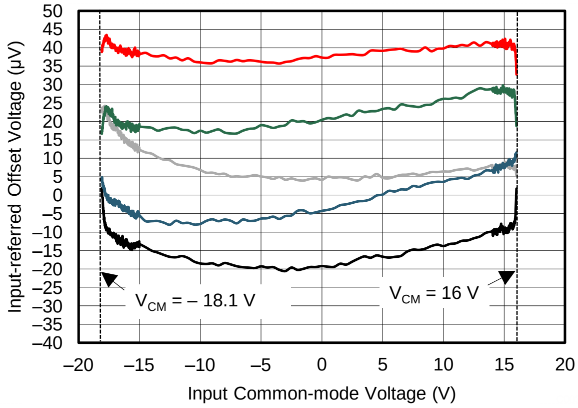


図 4. Input Offset Voltage vs Common-Mode Voltage

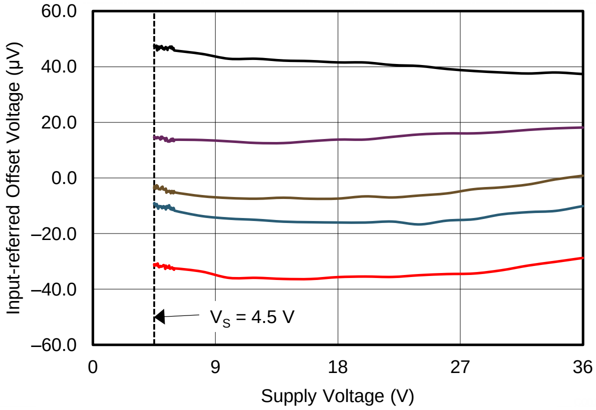


図 5. Offset Voltage vs Power Supply

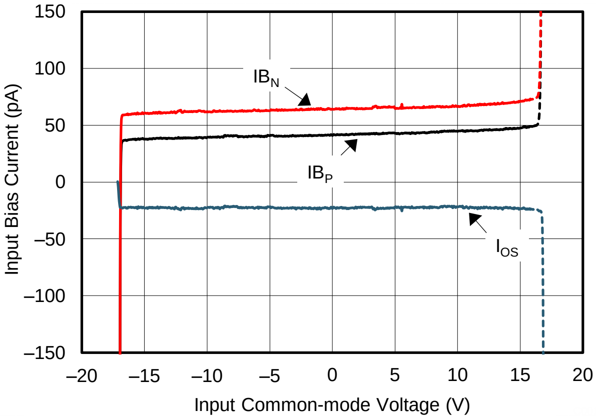


図 6. I_B and I_{OS} vs Common Mode Voltage

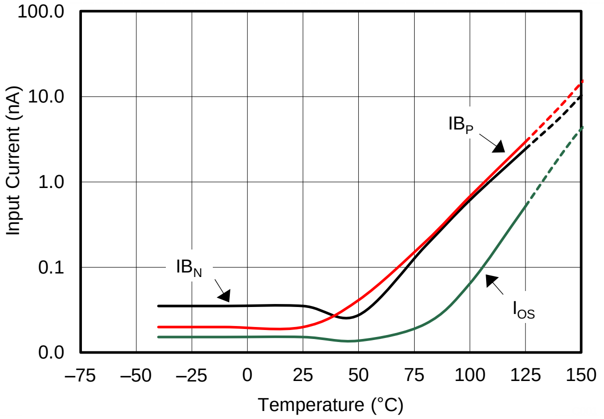


図 7. Input Bias Current vs Temperature

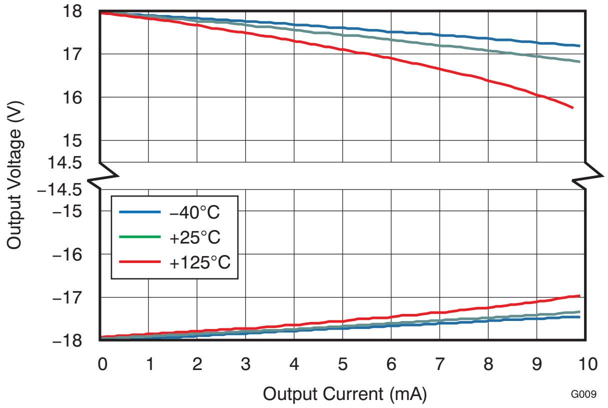


図 8. Output Voltage Swing vs Output Current (Maximum Supply)

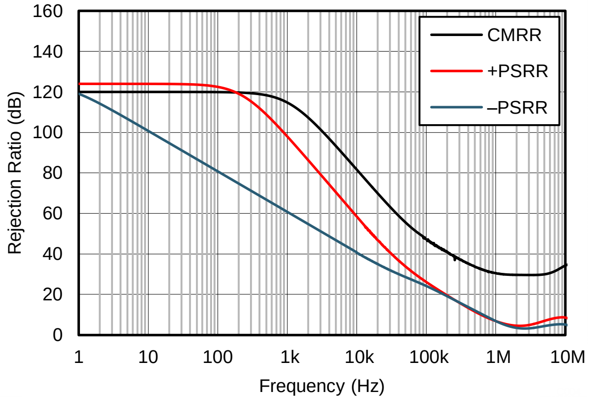


図 9. CMRR and PSRR vs Frequency

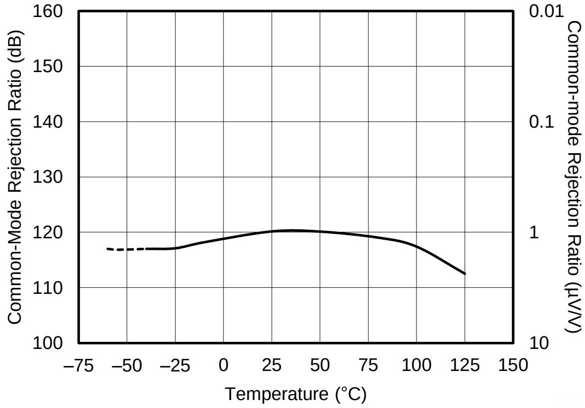


図 10. CMRR vs Temperature

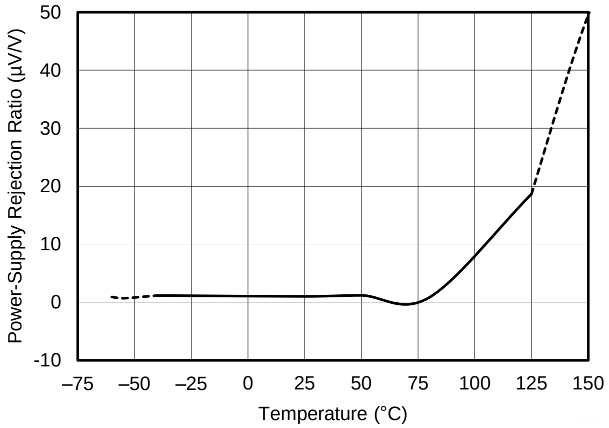


図 11. PSRR vs Temperature

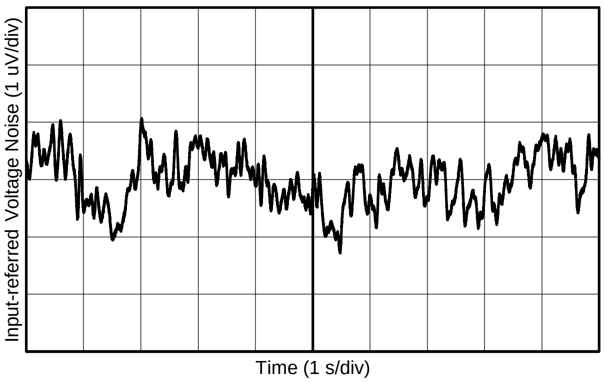


図 12. 0.1-Hz to 10-Hz Noise

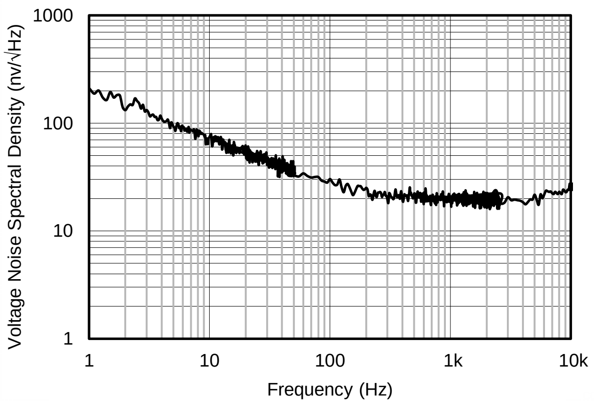


図 13. Input Voltage Noise Spectral Density vs Frequency

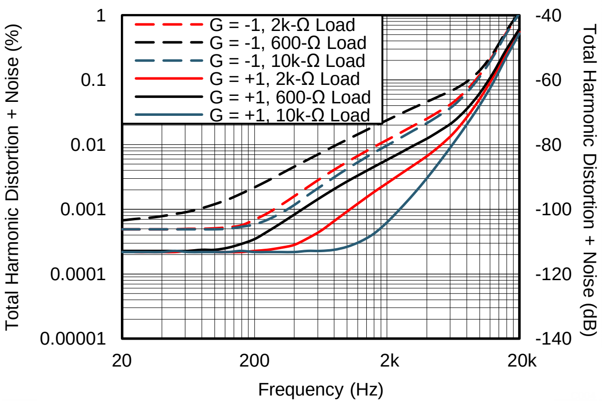


図 14. THD + N Ratio vs Frequency

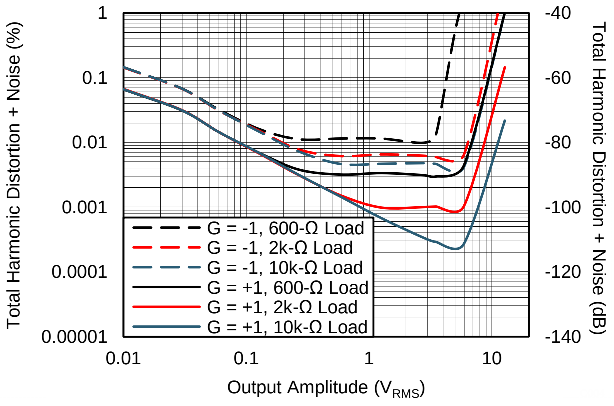


図 15. THD + N vs Output Amplitude

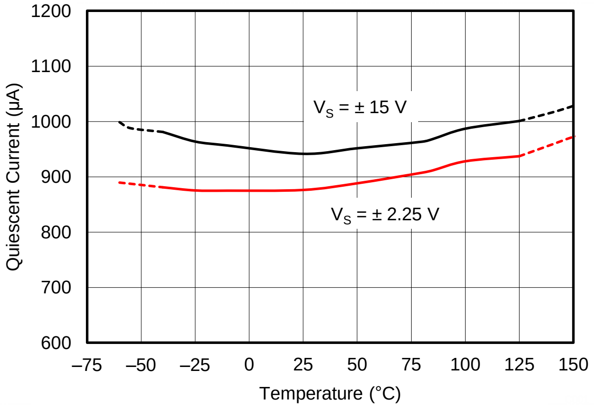


図 16. Quiescent Current vs Temperature

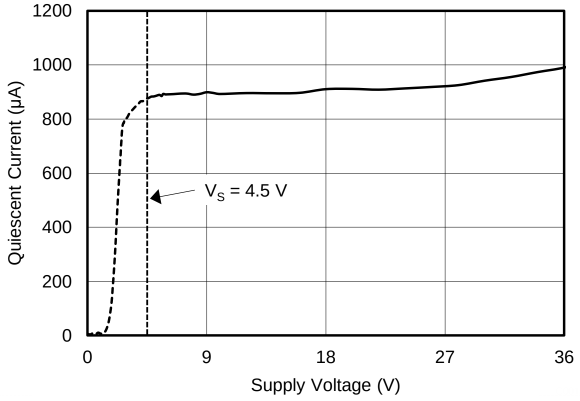


図 17. Quiescent Current vs Supply Voltage

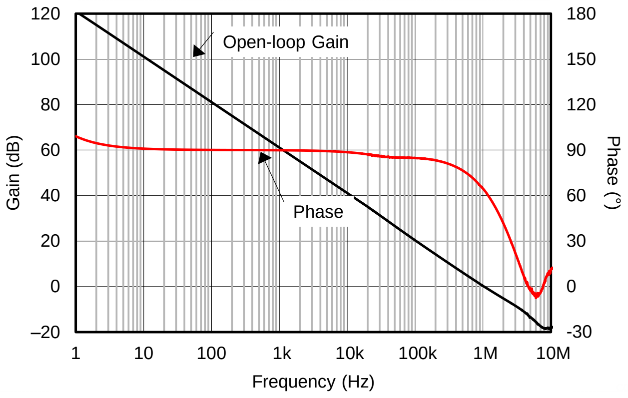


図 18. Open-Loop Gain and Phase vs Frequency

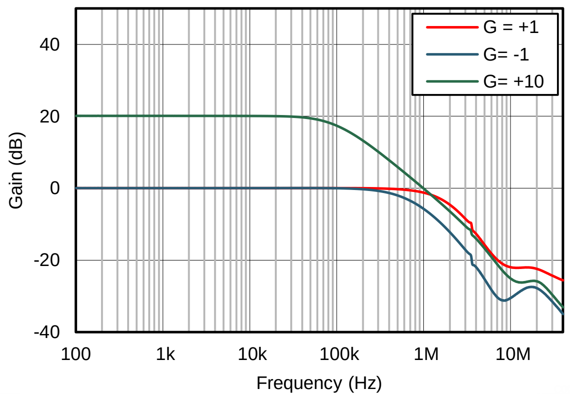


図 19. Closed-Loop Gain vs Frequency

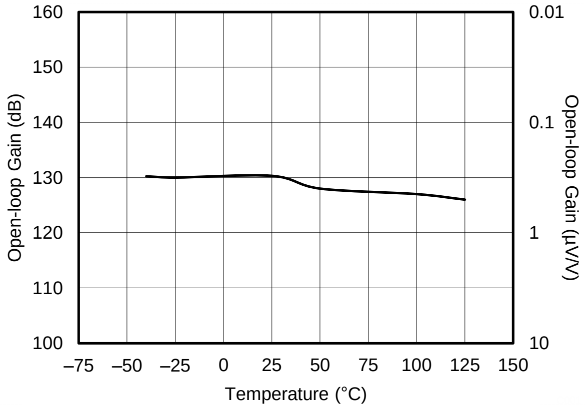


図 20. Open-Loop Gain vs Temperature

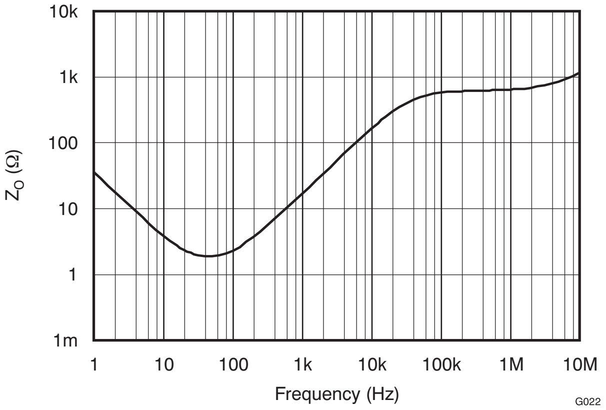


図 21. Open-Loop Output Impedance vs Frequency

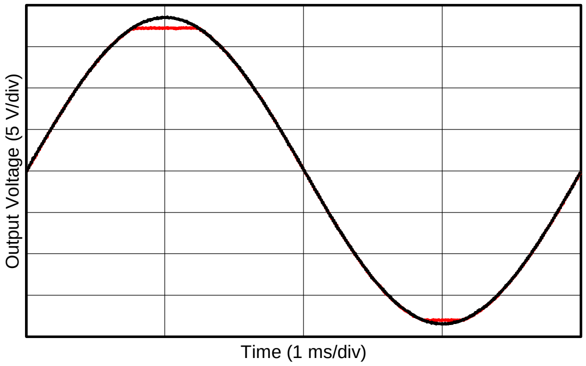


図 22. No Phase Reversal

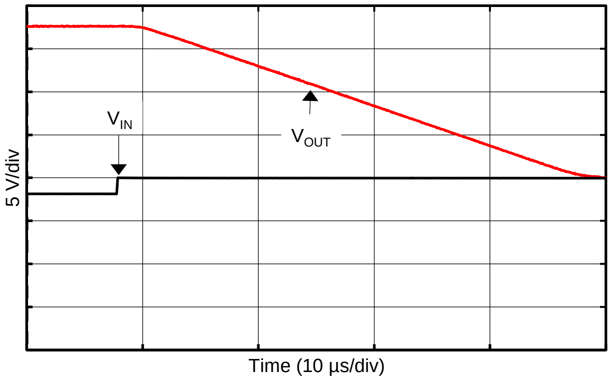


図 23. Positive Overload Recovery

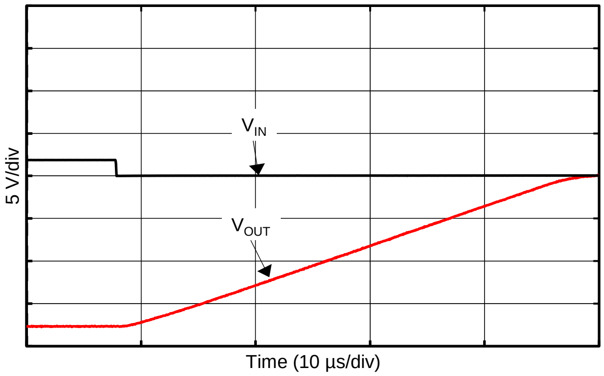
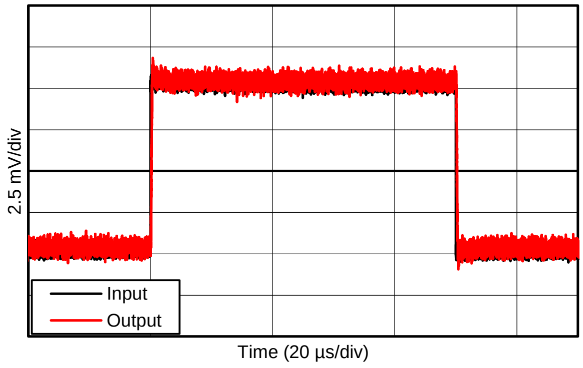
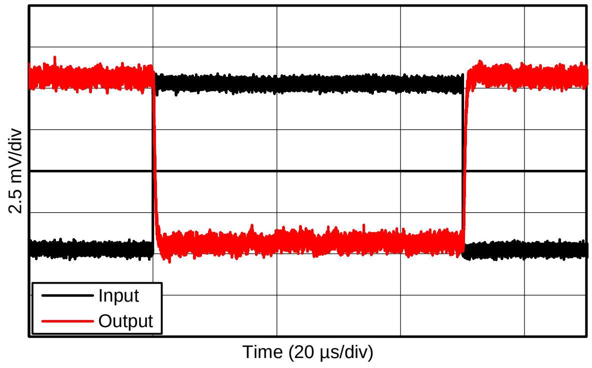


図 24. Negative Overload Recovery



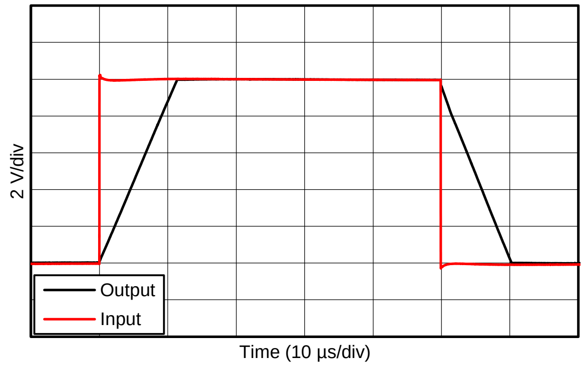
G = +1 V/V

図 25. Small-Signal Step Response



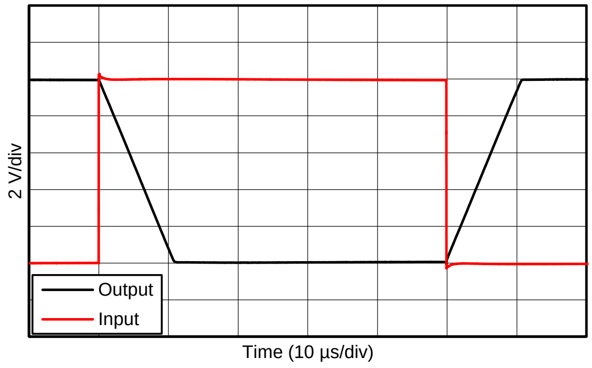
G = –1 V/V

図 26. Small-Signal Step Response



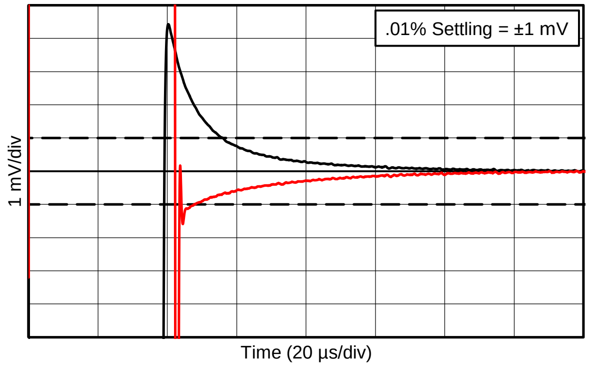
G = +1 V/V

図 27. Large-Signal Step Response



G = –1 V/V

図 28. Large-Signal Step Response



10-V positive step

図 29. Large-Signal Settling Time

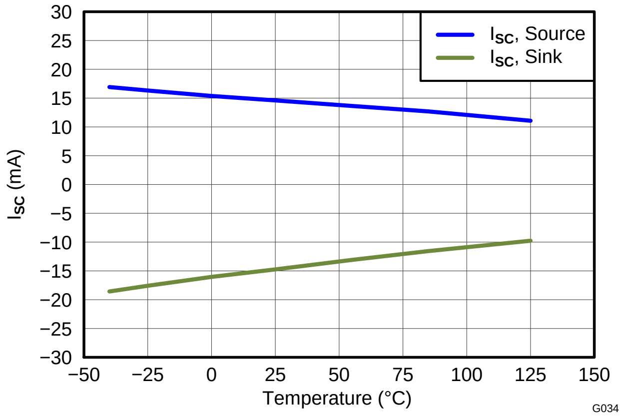


図 30. Short-Circuit Current vs Temperature

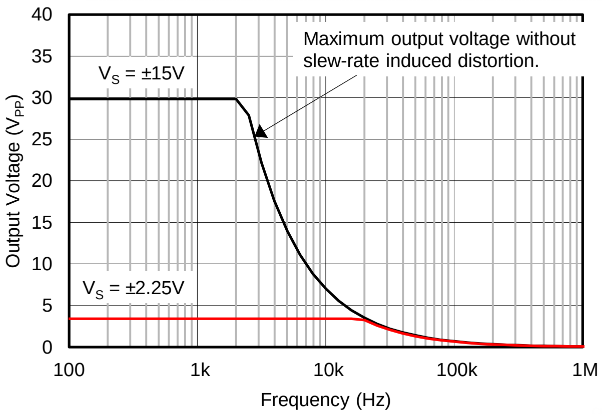


図 31. Maximum Output Voltage vs Frequency

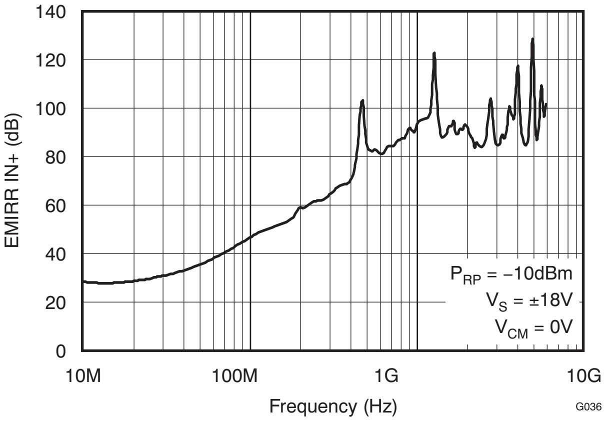


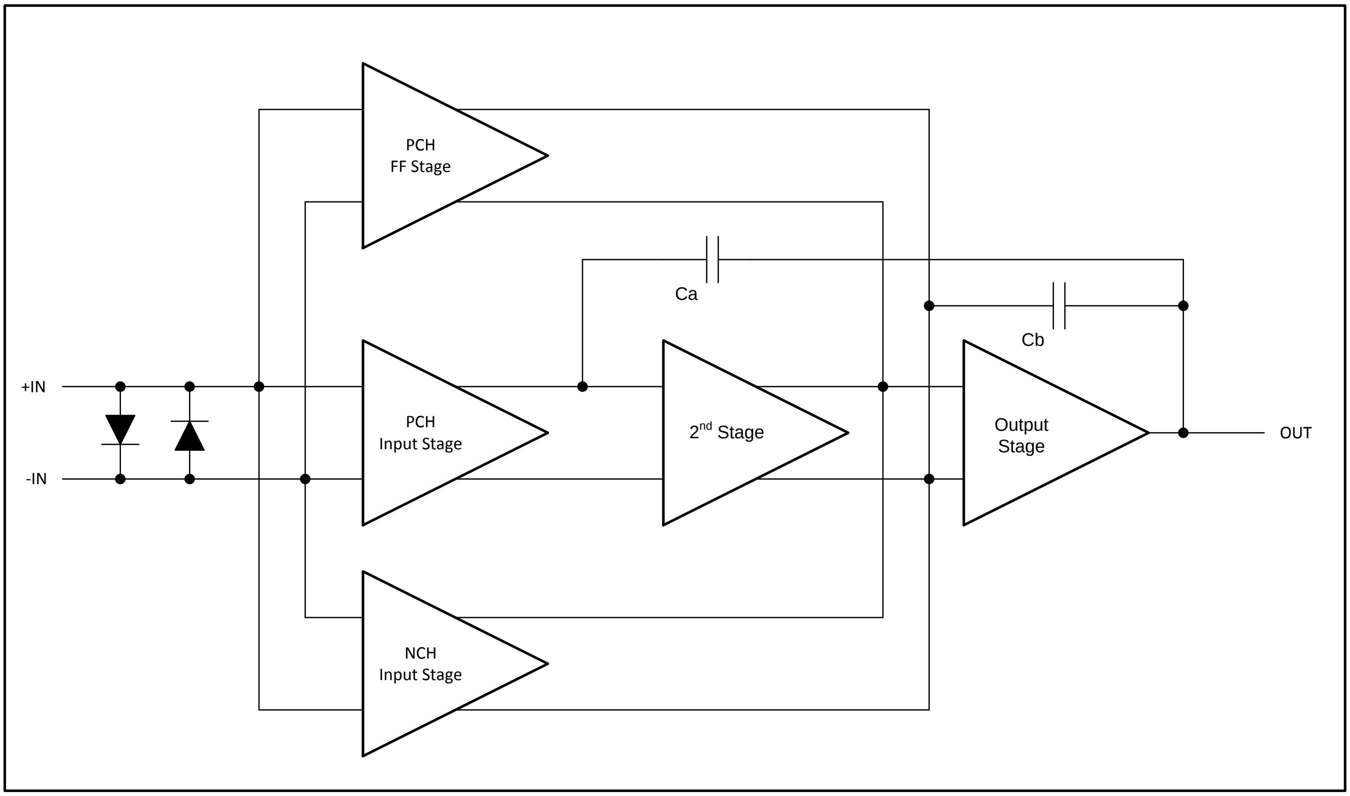
図 32. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The TLV07 operational amplifier provides high overall performance, making the device suitable for many general-purpose applications. The excellent offset drift of only 0.9 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and $A_{OL.}$

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The TLV07 op amp is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in *Typical Characteristics.*

7.3.2 Phase-Reversal Protection

The TLV07 has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input drives beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input drives beyond the specified common-mode voltage range, which causes the output to reverse into the opposite rail. The input of the TLV07 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 図 33.

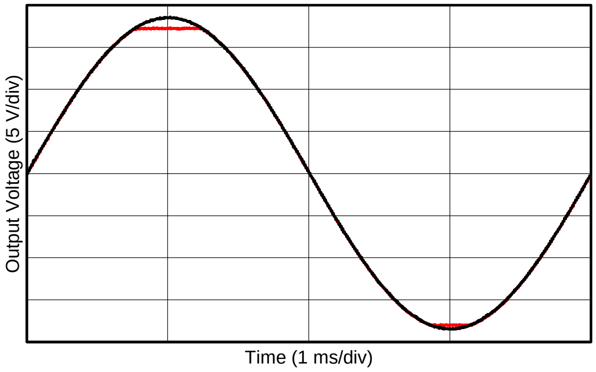


図 33. No Phase Reversal

7.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. The questions typically focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Internal electrostatic discharge (ESD) protection is built into the circuits to protect the circuits from accidental ESD events before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance of the circuitry to an electrical overstress event is helpful. 図 34 shows the ESD circuits contained in the TLV07 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at the power-supply ESD cell, an absorption device, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)

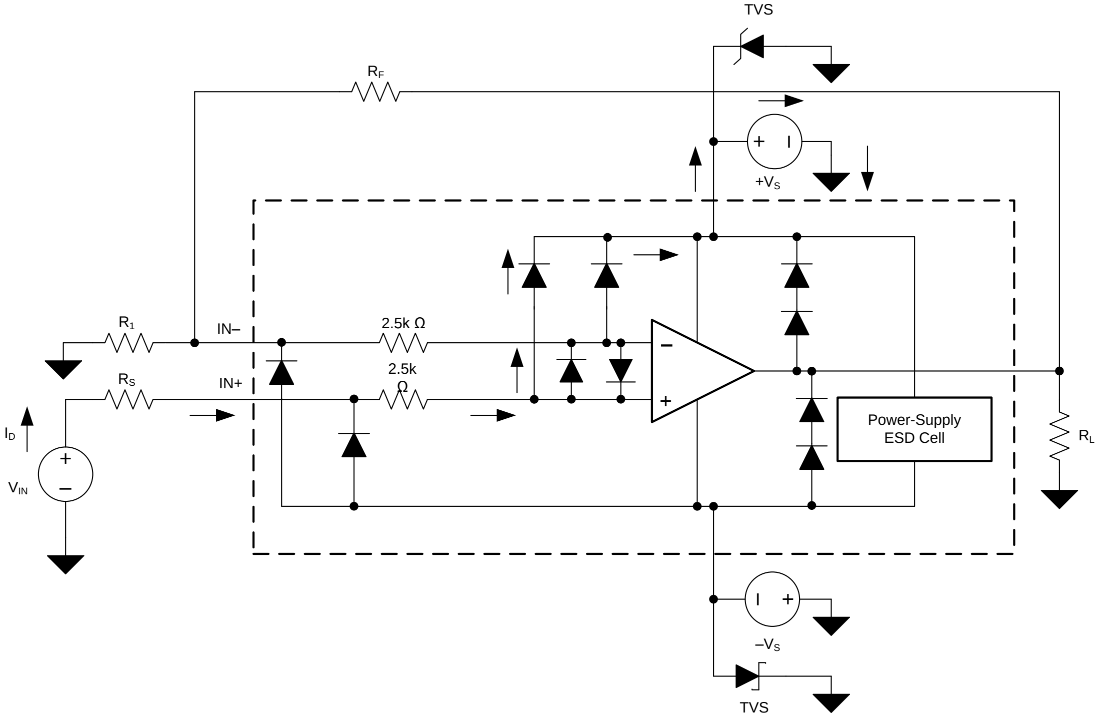


図 34. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLV07, but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see 図 34), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 34 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} sources current to the operational amplifier and becomes the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (continued)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. This question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 図 34. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The TLV07 input pins are protected from excessive differential voltage with back-to-back diodes; see 図 34. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, use an input series resistor to limit the input signal current.

7.4 Device Functional Modes

7.4.1 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices must have time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. As a result, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV07 is approximately 2 µs.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV07 op amp provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Follow the additional recommendations in *Layout Guidelines* to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier, potentially causing instability. Add an isolation resistor between the amplifier output and the capacitive load to stabilize the amplifier. *Typical Application* shows the design process for selecting this resistor.

8.2 Typical Application

This circuit can drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

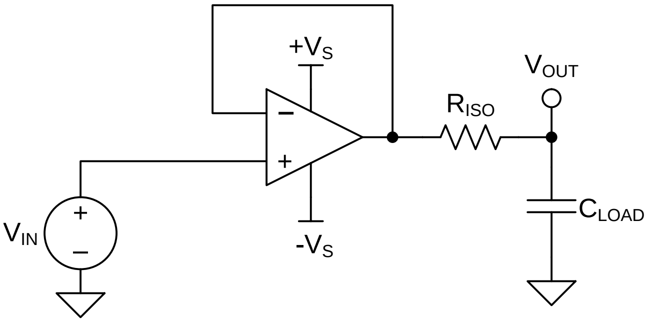


図 35. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

図 35 shows a unity-gain buffer driving a capacitive load. 式 1 shows the transfer function for the circuit in 図 35. 図 35 does not show the open-loop output resistance of the op amp (R_O).

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function shown in 式 1 has a pole and a zero. ($R_O + R_{ISO}$) and C_{LOAD} determine the frequency of the pole (f_p). The R_{ISO} and C_{LOAD} components determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade.

Typical Application (continued)

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R $_O$. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. These measurements then calculate phase margin. 表 2 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the TLV07, see *Capacitive Load Drive Solution Using an Isolation Resistor*

表 2. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.3 Application Curve

The values of R_{ISO} that yield phase margins of 45° and 60° for various capacitive loads are determined using the described methodology 図 36 shows the results.

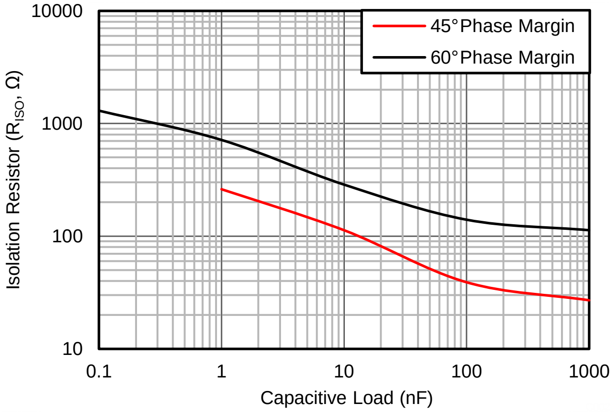


図 36. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

9 Power Supply Recommendations

The TLV07 is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

> **注意**
>
> Supply voltages larger than 40 V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 38, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

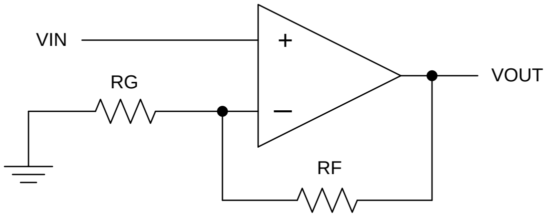


図 37. Schematic Representation of a Non-inverting Amplifier

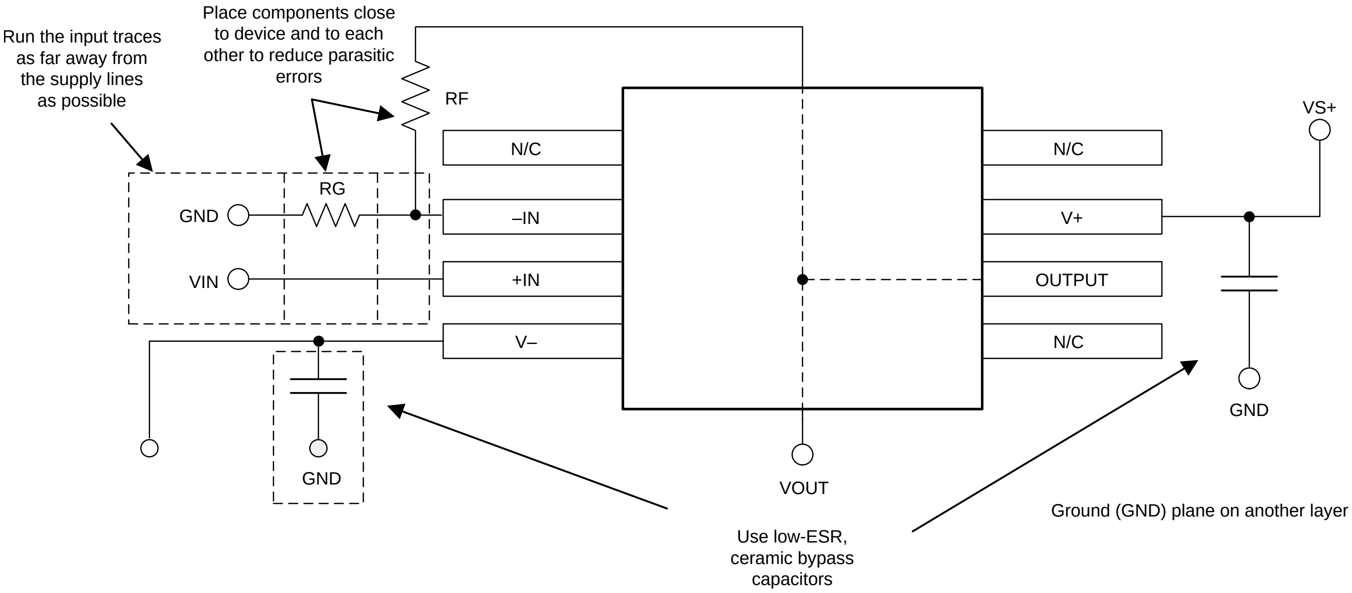


図 38. Operational Amplifier Board Layout for a Noninverting Configuration

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 開発サポート

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DIPアダプタ評価モジュール・ツールを使用すると、小さな表面実装ICのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU(SOIC-8)、PW(TSSOP-8)、DGK(MSOP-8)、DBV(SOT23-6、SOT23-5、およびSOT23-3)、DCK(SC70-6およびSC70-5)、およびDRL(SOT563-6)のTIパッケージに対応しています。DIPアダプタ評価モジュールは、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

11.1.2.3 ユニバーサル・オペアンプ評価モジュール

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のデバイス・パッケージ・タイプ向け回路のプロトタイプ作成を容易にします。この評価モジュール基板は、多くの異なる回路を簡単かつ迅速に構築できるように設計されています。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、SOT-23のすべてのパッケージがサポートされています。

注

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デバイス・サポート (continued)

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11.2 ドキュメントのサポート

11.2.1 関連資料

参照資料については、以下をご覧ください(www.ti.comからダウンロードできます)。

- *『フィードバック・プロットによるオペアンプAC性能の定義』*
- *『絶縁抵抗の使用による容量性負荷駆動のソリューション』*

11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV07IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV07	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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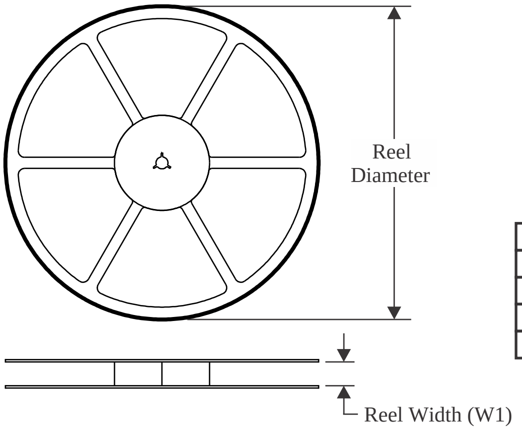
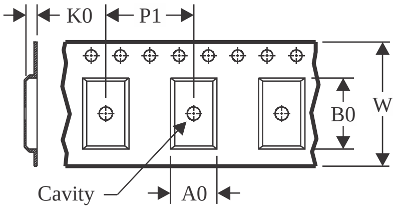
TAPE AND REEL INFORMATION

REEL DIMENSIONS

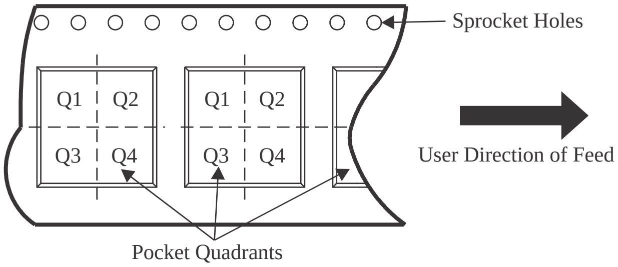


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

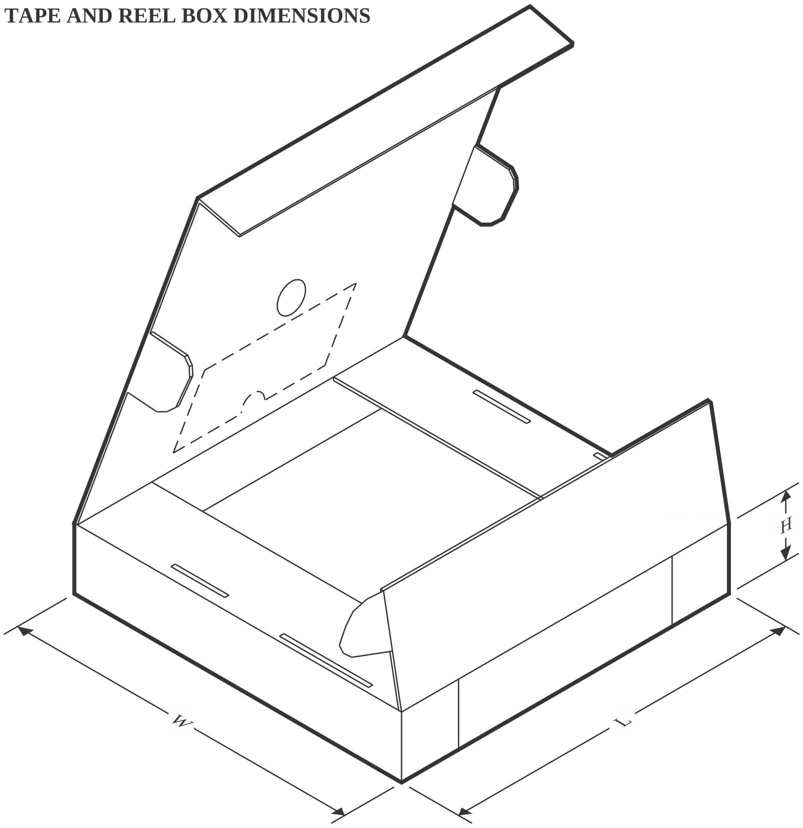
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

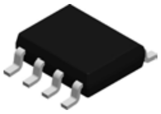
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV07IDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV07IDR	SOIC	D	8	2500	353.0	353.0	32.0

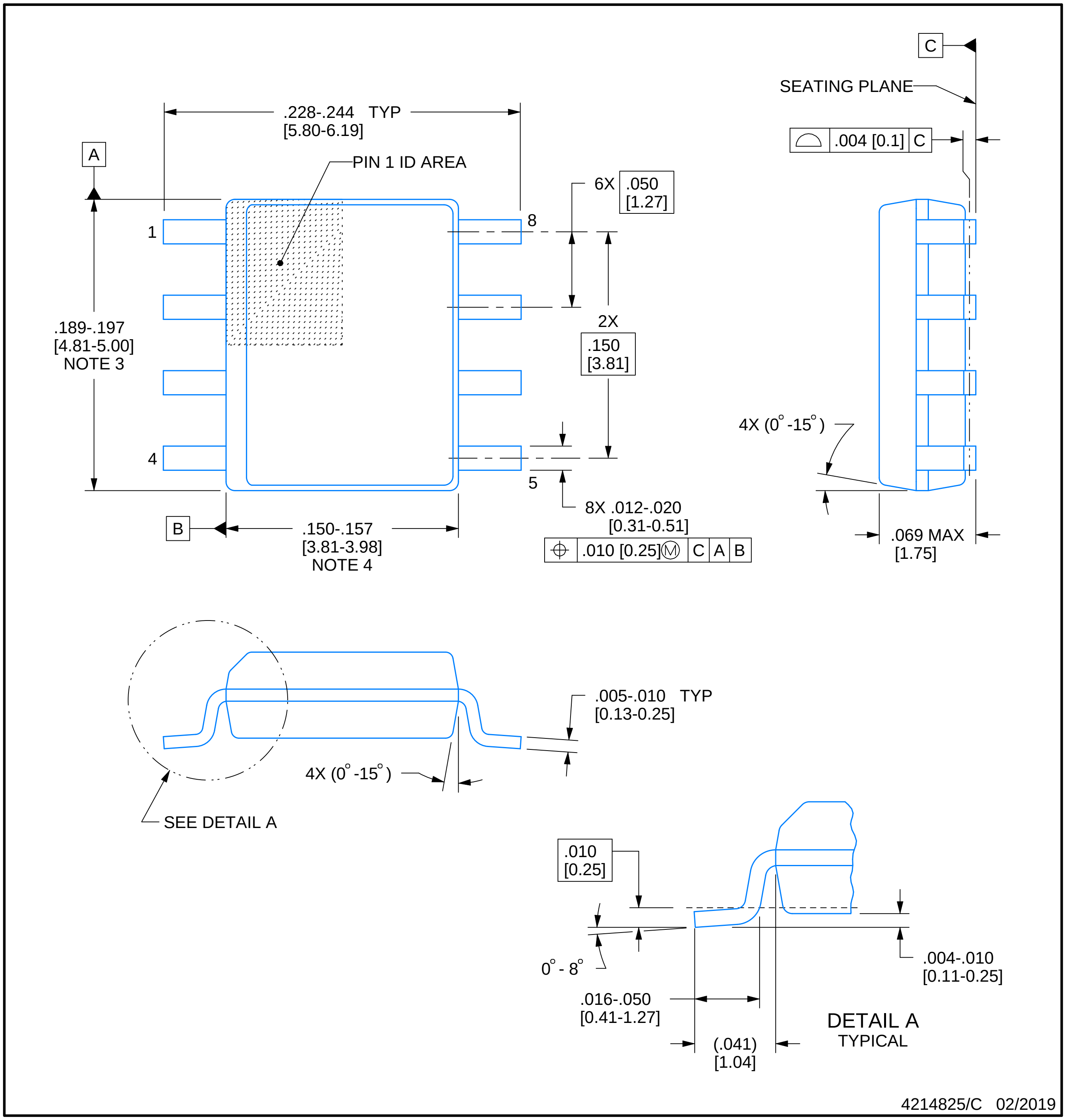


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

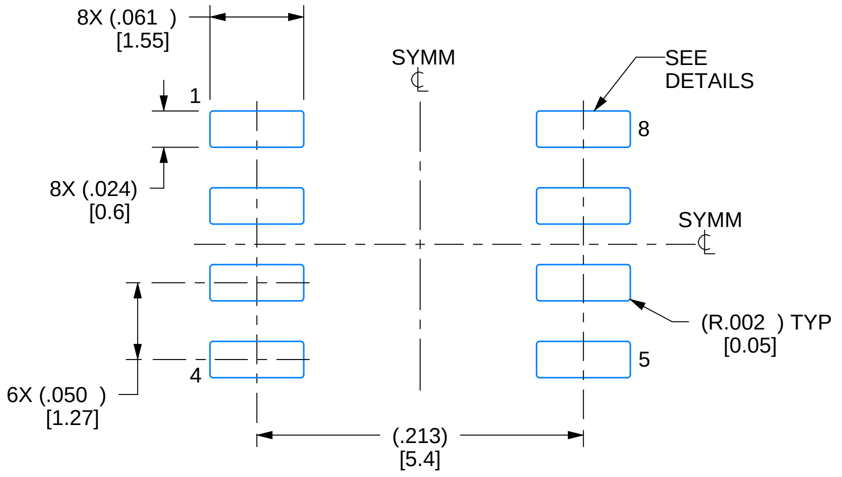
SMALL OUTLINE INTEGRATED CIRCUIT



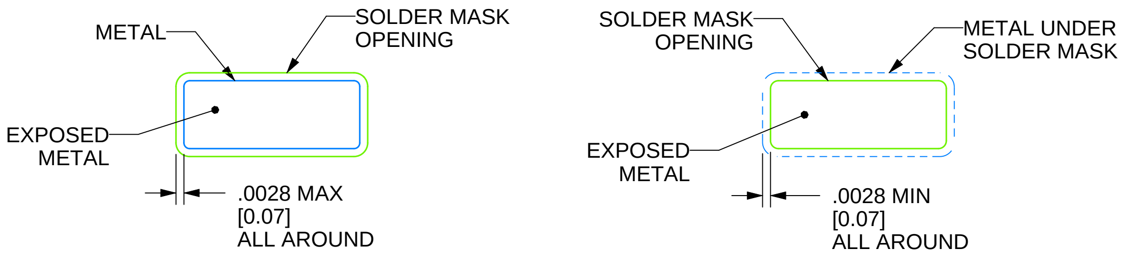
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



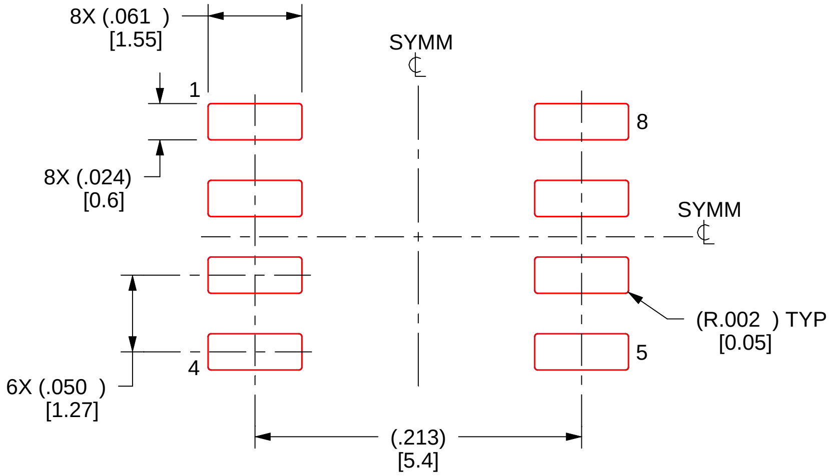
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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