TLV2401-Q1, TLV2402-Q1 16-V, Ultra-Low Power, 880-nA, RRIO Operational Amplifiers With Reverse Battery Protection

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C T_A
- Nano-power operation: 880 nA/channel
- Input common-mode range exceeds the rails: –0.1 V to V_{CC} + 5 V
- Reverse battery protection up to 18 V
- Rail-to-rail input or output
- Gain bandwidth product: 5.5 kHz
- Wide supply voltage range: 2.5 V to 16 V
- Industry standard packaging
  - 5-pin SOT-23 (TLV2401-Q1)
  - 8-pin MSOP (TLV2402-Q1)

2 Applications

- Hybrid, electric, and power train systems
- DC/DC converter
- On-board charger (OBC) and wireless charger
- Fuel cell and gasoline engine
- Inverter and motor control
- Telematics control unit

3 Description

The TLV240x-Q1 (TLV2401-Q1 and TLV2402-Q1) is a family of high voltage (16-V) nano-power operational amplifiers (op amps). The TLV240x-Q1 has an impressively low quiescent current of just 880 nA (typical) and is ideal for battery-powered or "always-on" applications, such as electric vehicle monitoring and protection applications. Reverse battery protection guards the amplifier from an overcurrent condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega-Ω resistors making them ideal for portable, long active-life applications. DC accuracy is ensured with a low typical offset voltage of 390 µV, CMRR of 120 dB and minimum open loop gain of 130 V/mV at 2.7 V.

The supply voltage extends from 2.5 V to 16 V, with electrical characteristics specified at 2.7 V, 5 V, and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micro-power microcontrollers including TI's MSP430 and MSP432.

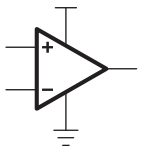
The single channel TLV2401-Q1 is available in a 5-pin SOT-23 package, and the dual channel TLV2402-Q1 is available in an 8-pin VSSOP. Both packages are fully specified from –40°C to 125°C.

Device Information(1)

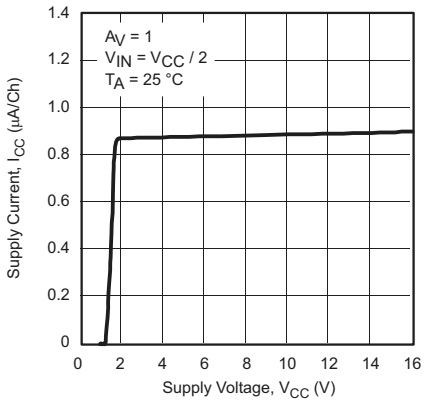
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV2401-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
TLV2402-Q1	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Operational Amplifier



Supply Current vs Supply Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2011) to Revision A	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging*, and *Orderable Information* section.	1
• Removed TLV2404-Q1 information from the data sheet	1
• Changed TLV2401-Q1 information from *Preview* to *Active*	1

5 Pin Configuration and Functions

TLV2401-Q1 DBV Package
5-Pin SOT-23
Top View

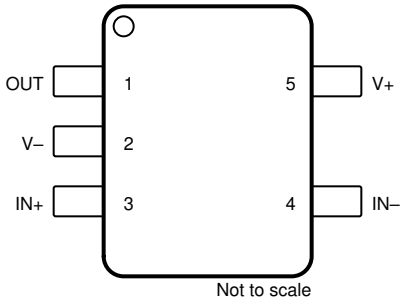


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (high) supply
V–	2	—	Negative (low) supply or ground (for single-supply operation)

TLV2402-Q1 DGK Package
8-Pin VSSOP
Top View

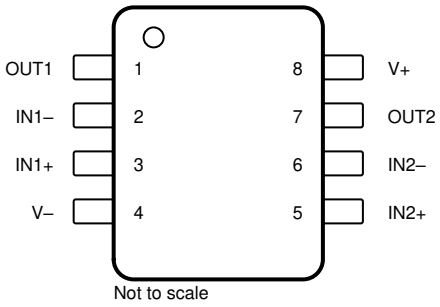


Table 2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (high) supply
V–	4	—	Negative (low) supply or ground (for single-supply operation)

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	17	V
Input pins	Differential voltage(2)	–20	20	V
	Current(2)	–10	10	mA
Output short-circuit(3)		Continuous		
Operating ambient temperature, T_A		–40	125	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Machine-model (MM)	±200	
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Single supply	2.5	16	V
		Split supply	±1.25	±8	V
V_I	Input voltage range		(V–) – 0.1	(V+) + 5	V
T_A	Specified temperature		–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC[1]		TLV2401-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	324.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information for Dual Channel

THERMAL METRIC[1]		TLV2402-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	259.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 500 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	R_S = 50 Ω				390	±1950	µV
				T_A = –40°C to 125°C			±2800	
dV_{OS}/dT	Input offset voltage drift	R_S = 50 Ω		T_A = –40°C to 125°C		±3		µV/°C
PSRR	Power supply rejection ratio	No load	V_{CC} = 2.7 V to 5 V	TLV2401-Q1		±1	±15	µV/V
				TLV2402-Q1		±1	±10	
				T_A = –40°C to 125°C			±70	
			V_{CC} = 5 V to 15 V			±1	±10	
				TLV2401-Q1, T_A = –40°C to 125°C			±35	
				TLV2402-Q1, T_A = –40°C to 125°C			±14	
INPUT BIAS CURRENT								
I_B	Input bias current	TLV2401-Q1	R_S = 50 Ω			±100	±1000	pA
				T_A = –40°C to 125°C			±4000	
		TLV2402-Q1				±100	±300	
				T_A = –40°C to 125°C			±900	
I_{OS}	Input offset current	TLV2401-Q1	R_S = 50 Ω			±25	±1000	pA
				T_A = –40°C to 125°C			±1500	
		TLV2402-Q1				±25	±250	
				T_A = –40°C to 125°C			±400	
NOISE								
e_N	Input voltage noise density	f = 10 Hz				800		nV/√Hz
		f = 100 Hz				500		
i_N	Input current noise	f = 1 kHz				8		fA/√Hz
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range				(V–) – 0.1		(V+) + 5	V
CMRR	Common-mode rejection ratio	TLV2401-Q1	V_S = 2.7 V, (V–) < V_{CM} < (V+), R_S = 50 Ω		56	100		dB
				T_A = –40°C to 125°C	54			
			V_S = 5 V, (V–) < V_{CM} < (V+), R_S = 50 Ω		62	106		
				T_A = –40°C to 125°C	58			
			V_S = 15 V, (V–) < V_{CM} < (V+), R_S = 50 Ω		71	112		
				T_A = –40°C to 125°C	68			
		TLV2402-Q1	V_S = 2.7 V, (V–) < V_{CM} < (V+), R_S = 50 Ω		60	120		
				T_A = –40°C to 125°C	56			
			V_S = 5 V, (V–) < V_{CM} < (V+), R_S = 50 Ω		65	120		
				T_A = –40°C to 125°C	58			
			V_S = 15 V, (V–) < V_{CM} < (V+), R_S = 50 Ω		73	120		
				T_A = –40°C to 125°C	73			
INPUT CAPACITANCE								
R_{ID}	Differential input resistance					300		MΩ
C_{ICM}	Common-mode input capacitance					3		pF

Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 500 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	TLV2401-Q1	V_S = 2.7 V, $V_{O(pp)}$ = 1 V		91	112		dB
				T_A = –40°C to 125°C	72			
			V_S = 5 V, $V_{O(pp)}$ = 1 V(1)		100	120		
				T_A = –40°C to 125°C	94			
			V_S = 15 V, $V_{O(pp)}$ = 6 V(1)		106	125		
				T_A = –40°C to 125°C	98			
		TLV2402-Q1	V_S = 2.7 V, $V_{O(pp)}$ = 1 V		102	112		
				T_A = –40°C to 125°C	81			
			V_S = 5 V, $V_{O(pp)}$ = 1 V		109	120		
				T_A = –40°C to 125°C	91			
			V_S = 15 V, $V_{O(pp)}$ = 6 V		120	125		
				T_A = –40°C to 125°C	96			
FREQUENCY RESPONSE								
GBW	Gain-bandwidth product	R_L = 500 kΩ, C_L = 100 pF				5.5		kHz
SR	Slew rate					2.5		V/ms
t_S	Settling time	V_S = 2.7 V or 5 V, V_{STEP} = 1 V, G = –1, C_L = 100 pF, R_L = 100 kΩ		To 0.1%		1.84		ms
		V_S = 15 V, V_{STEP} = 1 V, G = –1, C_L = 100 pF, R_L = 100 kΩ		To 0.1%		6.1		
				To 0.01%		32		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF				60		°
	Gain margin					15		dB
OUTPUT								
V_{OH}	High-level output voltage	V_{CM} = V_{CC} / 2, I_{OH} = –2 µA	V_{CC} = 2.7 V		2.65	2.68		V
				T_A = –40°C to 125°C	2.63			
			V_{CC} = 5 V(1)		4.95	4.98		
				T_A = –40°C to 125°C	4.93			
			V_{CC} = 15 V(1)		14.95	14.98		
				T_A = –40°C to 125°C	14.93			
		V_{CM} = V_{CC} / 2, I_{OH} = –50 µA	V_{CC} = 2.7 V		2.62	2.65		
				T_A = –40°C to 125°C	2.6			
			V_{CC} = 5 V(1)		4.92	4.95		
				T_A = –40°C to 125°C	4.9			
			V_{CC} = 15 V(1)		14.92	14.95		
				T_A = –40°C to 125°C	14.9			
V_{OL}	Low-level output voltage	V_{CM} = V_{CC} / 2, I_{OL} = 2 µA(1)				90	150	mV
				T_A = –40°C to 125°C			180	
		V_{CM} = V_{CC} / 2, I_{OL} = 50 µA(1)				180	230	
				T_A = –40°C to 125°C			260	
I_{SC}	Short-circuit current	V_O = 0.5 V from rail				±200		µA

(1) Assured by design and characterization only. This condition applies for TLV2401-Q1 only.

Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 500 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
POWER SUPPLY								
I_Q	Quiescent current per amplifier	TLV2401-Q1	V_{CC} = 2.7 V or 5 V, I_O = 0 A			880	1050	nA
				T_A = –40°C to 125°C			1400	
			V_{CC} = 15 V, I_O = 0 A			900	1050	
				T_A = –40°C to 125°C			1550	
		TLV2402-Q1	V_{CC} = 2.7 V or 5 V, I_O = 0 A			880	990	
				T_A = –40°C to 125°C			1300	
			V_{CC} = 15 V, I_O = 0 A			900	1050	
				T_A = –40°C to 125°C			1400	
	Reverse supply current	V_{CC} = –18 V, V_{IN} = 0 V, R_L = ∞				50		nA

6.7 Typical Characteristics

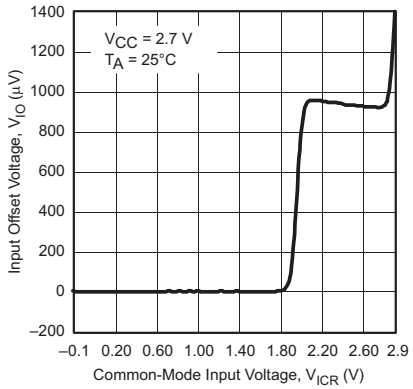


Figure 1. Input Offset Voltage vs Common-Mode Input Voltage

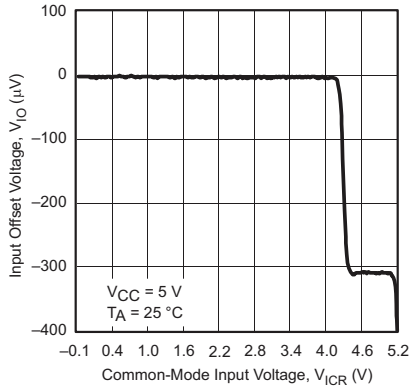


Figure 2. Input Offset Voltage vs Common-Mode Input Voltage

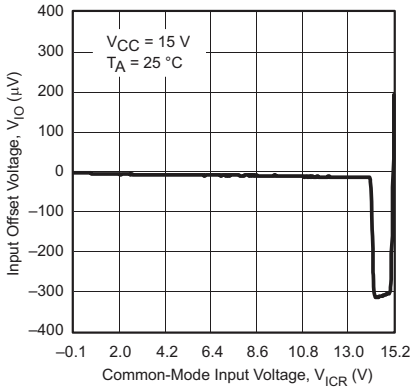


Figure 3. Input Offset Voltage vs Common-Mode Input Voltage

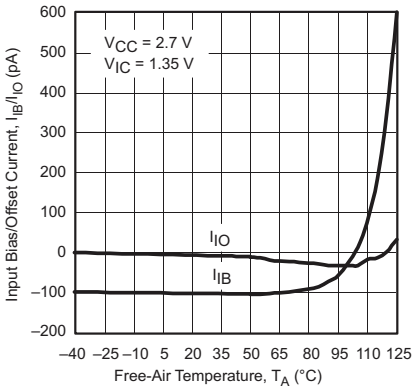


Figure 4. Input Bias and Offset Current vs Free-Air Temperature

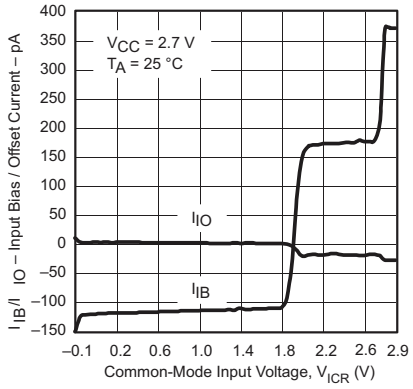


Figure 5. Input Bias and Offset Current vs Common-Mode Voltage

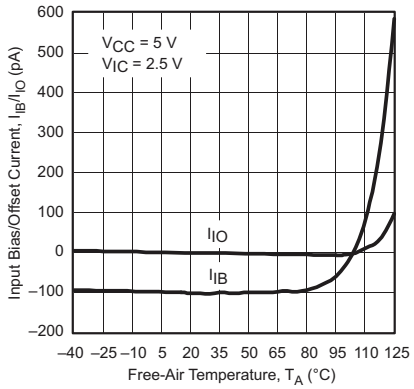


Figure 6. Input Bias and Offset Current vs Free-Air Temperature

Typical Characteristics (continued)

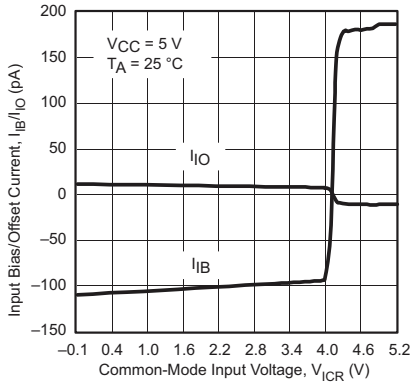


Figure 7. Input Bias and Offset Current vs Common-Mode Voltage

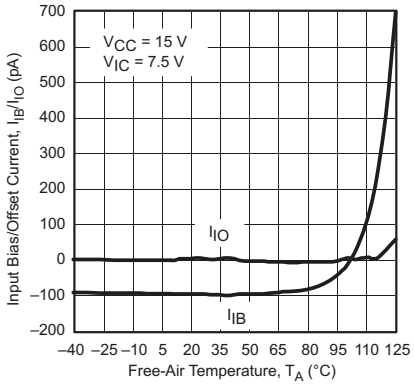


Figure 8. Input Bias and Offset Current vs Free-Air Temperature

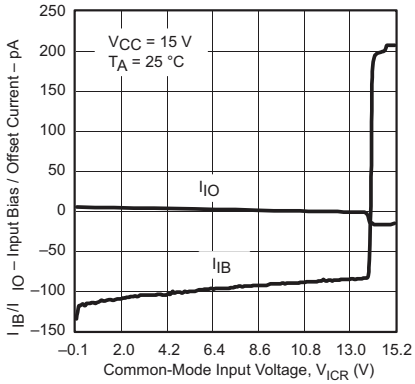


Figure 9. Input Bias and Offset Current vs Common-Mode Input Voltage

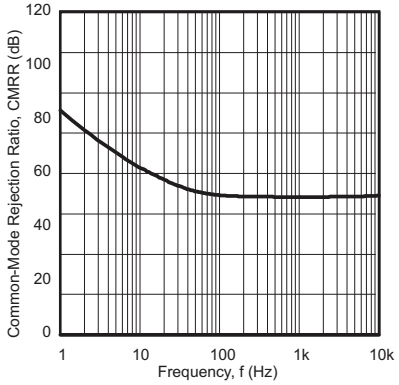


Figure 10. Common-Mode Rejection Ratio vs Frequency

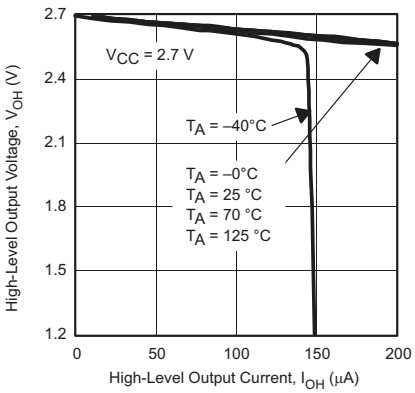


Figure 11. High-Level Output Voltage vs High-Level Output Current

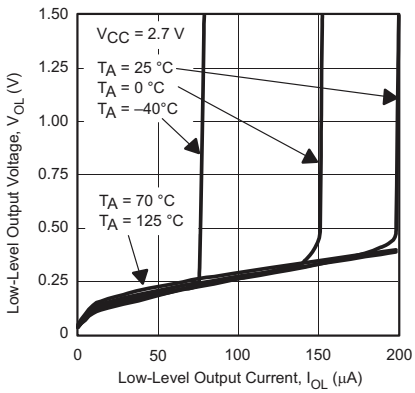


Figure 12. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

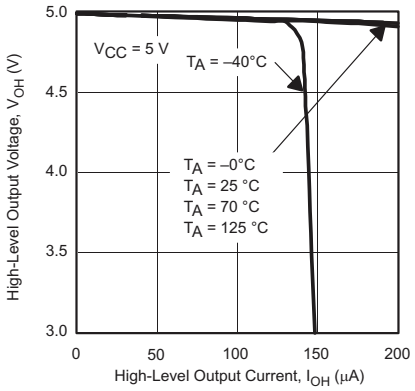


Figure 13. High-Level Output Voltage vs High-Level Output Current

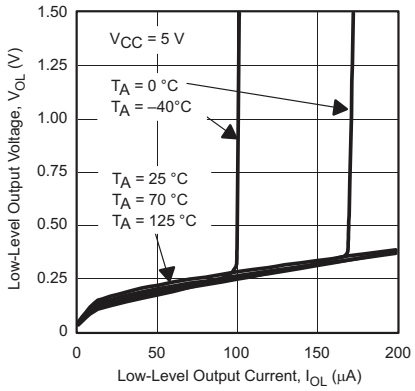


Figure 14. Low-Level Output Voltage vs Low-Level Output Current

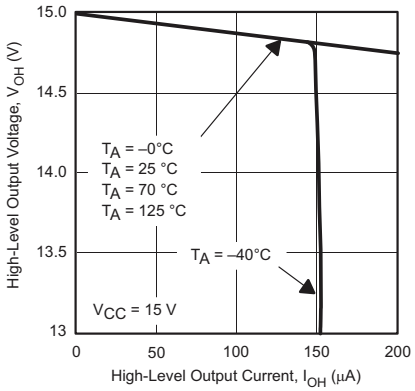


Figure 15. High-Level Output Voltage vs High-Level Output Current

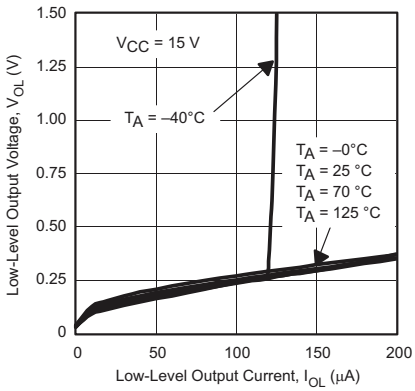


Figure 16. Low-Level Output Voltage vs Low-Level Output Current

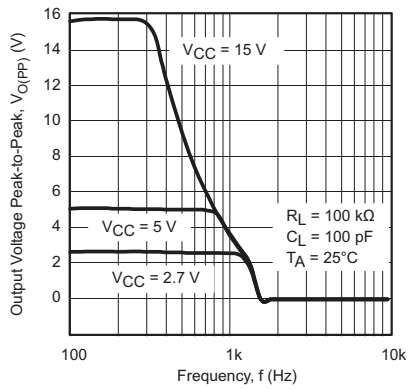


Figure 17. Output Voltage Peak-to-Peak vs Frequency

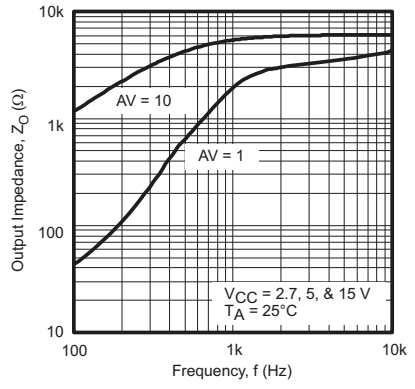


Figure 18. Output Impedance vs Frequency

Typical Characteristics (continued)

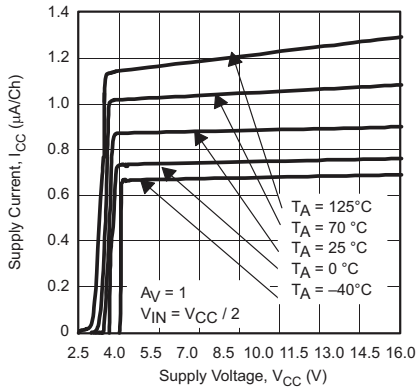


Figure 19. Supply Current vs Supply Voltage

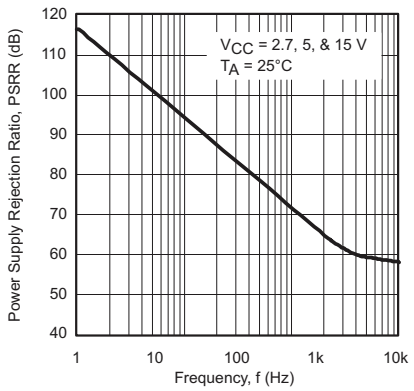


Figure 20. Power Supply Rejection Ratio vs Frequency

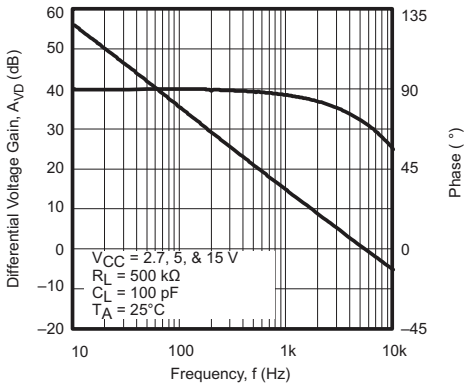


Figure 21. Differential Voltage Gain and Phase vs Frequency

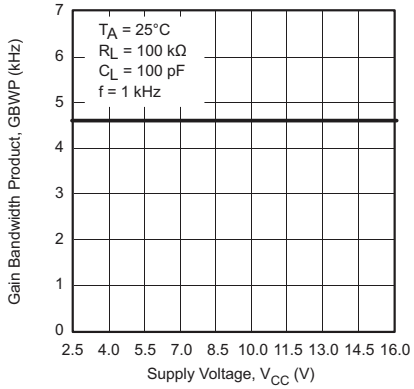


Figure 22. Gain Bandwidth Product vs Supply Voltage

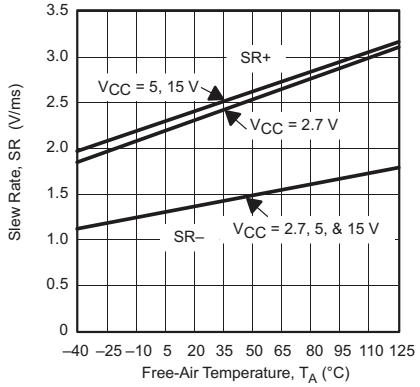


Figure 23. Slew Rate vs Free-Air Temperature

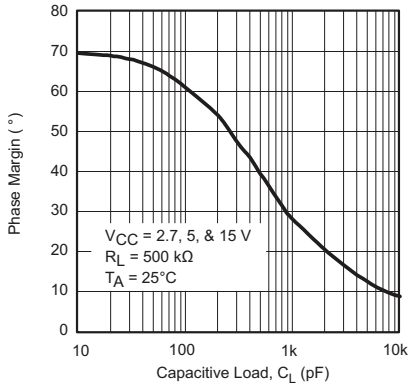


Figure 24. Phase Margin vs Capacitive Load

Typical Characteristics (continued)

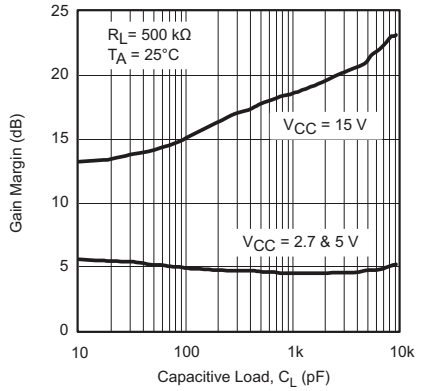


Figure 25. Gain Margin vs Capacitive Load

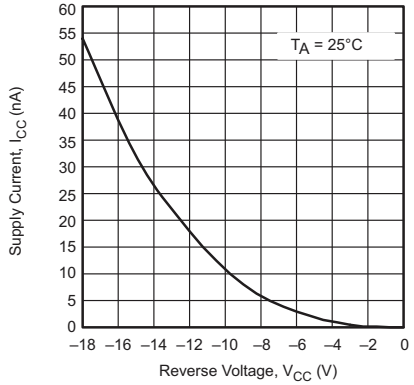


Figure 26. Supply Current vs Reverse Voltage

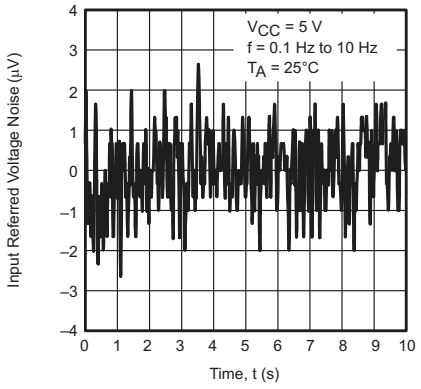


Figure 27. 0.1 Hz to 10 Hz Voltage Noise

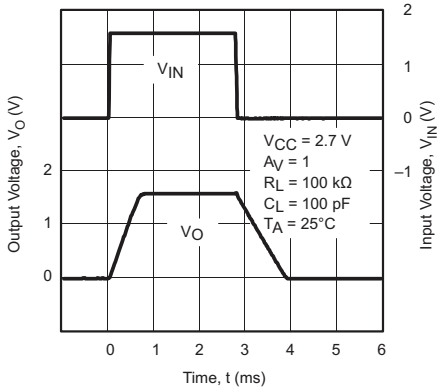


Figure 28. Large Signal Follower Pulse Response

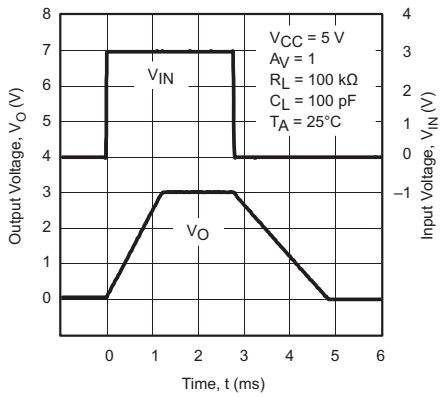


Figure 29. Large Signal Follower Pulse Response

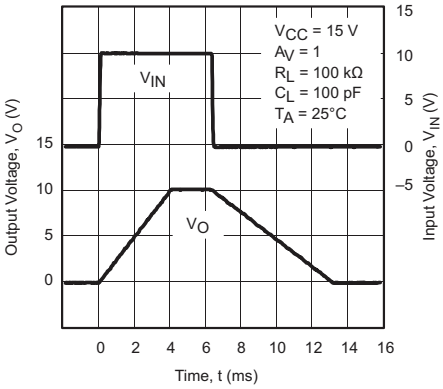


Figure 30. Large Signal Follower Pulse Response

Typical Characteristics (continued)

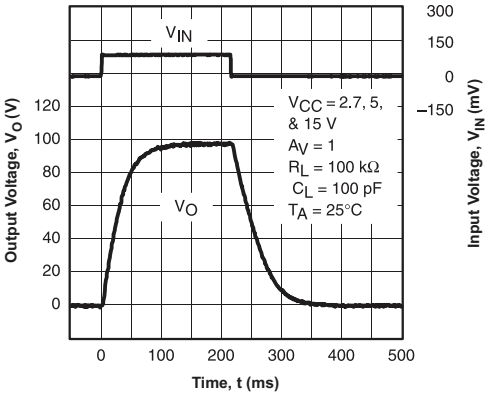


Figure 31. Small Signal Follower Pulse Response

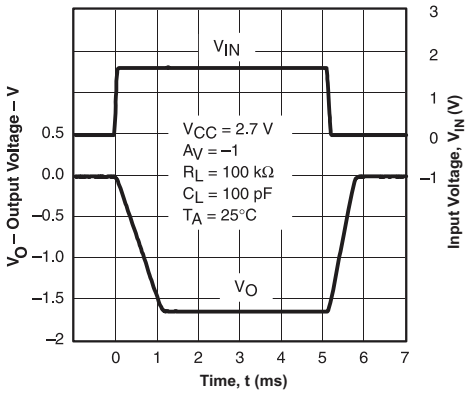


Figure 32. Large Signal Follower Pulse Response

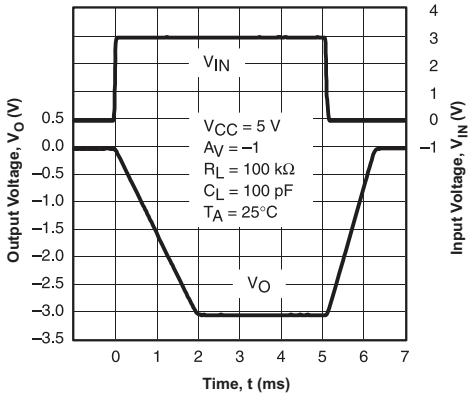


Figure 33. Large Signal Follower Pulse Response

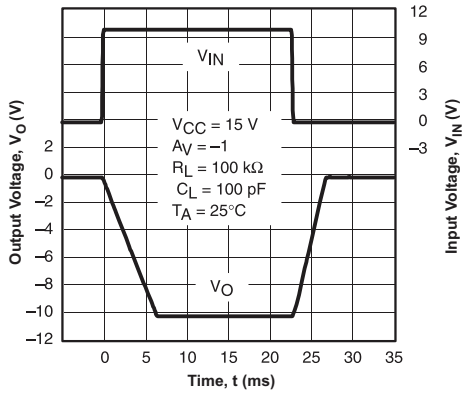


Figure 34. Large Signal Follower Pulse Response

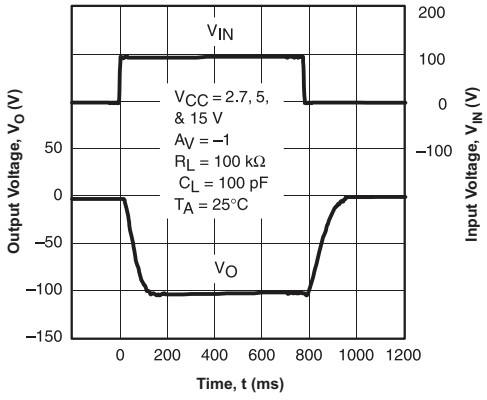


Figure 35. Small Signal Follower Pulse Response

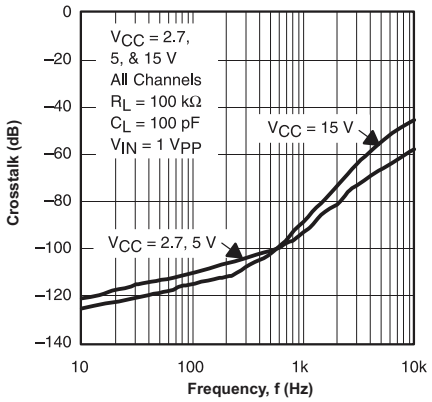


Figure 36. Crosstalk

7 Detailed Description

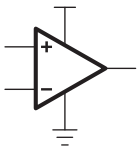
7.1 Overview

The TLV240x-Q1 (TLV2401-Q1 and TLV2402-Q1) is a family of high voltage (16-V) general purpose operational amplifiers (op amps). The TLV240x-Q1 has an impressively low quiescent current of just 880 nA (typ) and is ideal for battery-powered or "always-on" applications, such as electric vehicle monitoring and protection applications. Reverse battery protection guards the amplifier from an overcurrent condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega-Ω resistors making them ideal for portable, long active-life applications. DC accuracy is ensured with a low typical offset voltage as low as 390 µV, CMRR of 120 dB and minimum open loop gain of 130 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micro-power microcontrollers including TI's MSP430 and MSP432.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reverse Battery Protection

The TLV240x-Q1 are protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of 6 Schottky diodes; and therefore, increases as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure turns on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

7.3.1.1 Common-Mode Input Range

The TLV240x-Q1 has rail-to-rail input and outputs. For common-mode inputs from –0.1 V to V_{CC} – 0.8 V a PNP differential pair provides the gain.

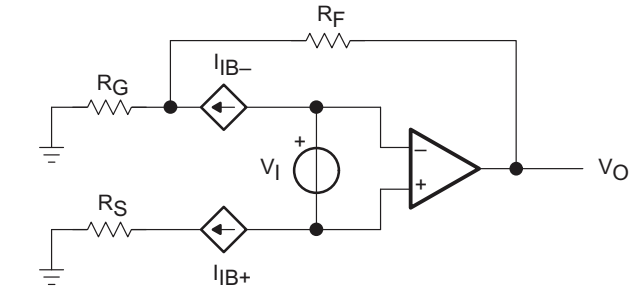
For inputs between V_{CC} – 0.8 V and V_{CC}, two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails, because as the inputs go above V_{CC}, the NPNs switch from functioning as transistors to functioning as diodes. This leads to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC}.

The TLV240x-Q1 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain is observed with the ultimate possibility of phase inversion.

Feature Description (continued)

7.3.2 Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 37. Output Offset Voltage Model

7.4 Device Functional Modes

The TLV240x-Q1 has a single functional mode. The devices are powered on as long as the power supply voltage is between 2.5 V (±1.25 V) and 16 V (±8 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required to maximize accuracy. A low-pass filter using different topologies can offer circuit designers the flexibility to design their circuit optimally.

8.2 Typical Application

The simplest way to accomplish this a low-pass filter is to place an RC filter at the non-inverting terminal of the amplifier (see Figure 38). If even more attenuation is needed, a multiple pole filter is required. The Figure 39 can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

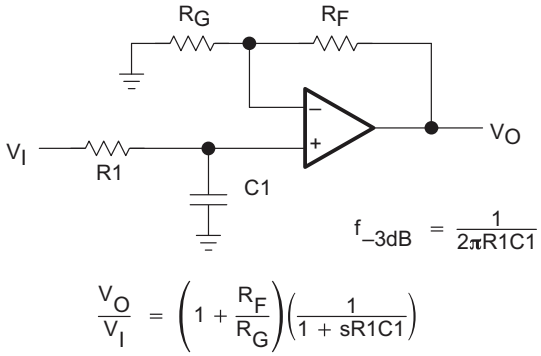


Figure 38. Single-Pole Low-Pass Filter

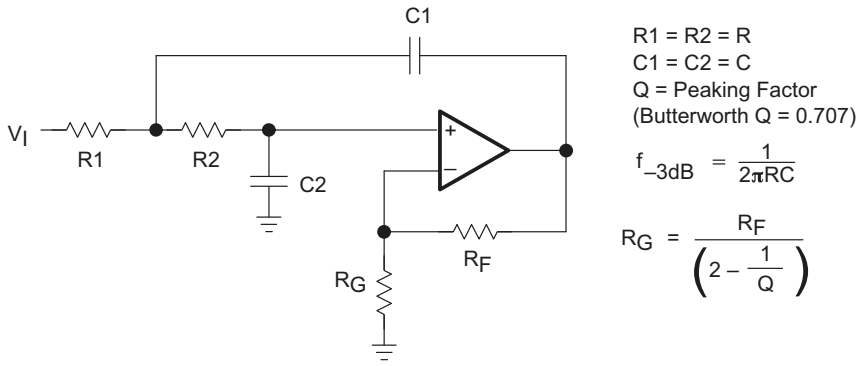


Figure 39. 2-Pole Low-Pass Sallen-Key Filter

8.2.1 Design Requirements

The design requirements for this circuit are:

- Supply voltage: 5 V
- Low quiescent current: ≤ 5-µA typical
- –3-dB bandwidth: 100 Hz
- Gain at 0 Hz: 2

Typical Application (continued)

8.2.2 Detailed Design Procedure

Considering the equations shown in Figure 39, we can derive that $R_F = R_G$ if the gain must equal 2 at DC. To minimize power dissipation of the system, we can set $R_F = R_G = 1\ M\Omega$. With a supply voltage of 5 V, this will give a worst-possible feedback current of about 2.5 µA.

To set the –3-dB pole at 100 Hz, we can calculate that the ratio R1 × C1 must equal ≈ 1.6×10^{-4}. With this in mind, we can set R1 = 100 kΩ and C1 = 1.6 pF.

With these values, we have achieved all of our design goals for the circuit.

8.2.3 Application Curve

The frequency response of the filter circuit is shown below.

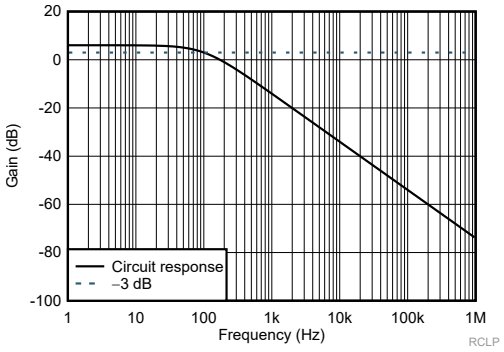


Figure 40. RC Low Pass Filter Frequency Response

9 Power Supply Recommendations

The TLV240x-Q1 is specified for operation from 2.5 V to 16 V (±1.25 V to ±8 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 16 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the .

10 Layout

10.1 Layout Guidelines

To achieve the levels of high performance of the TLV240x-Q1, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-mF tantalum capacitor in parallel with a 0.1-mF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-mF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-mF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 in between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

10.2 Layout Example

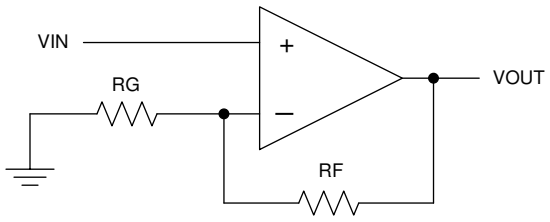


Figure 41. Schematic Representation

Layout Example (continued)

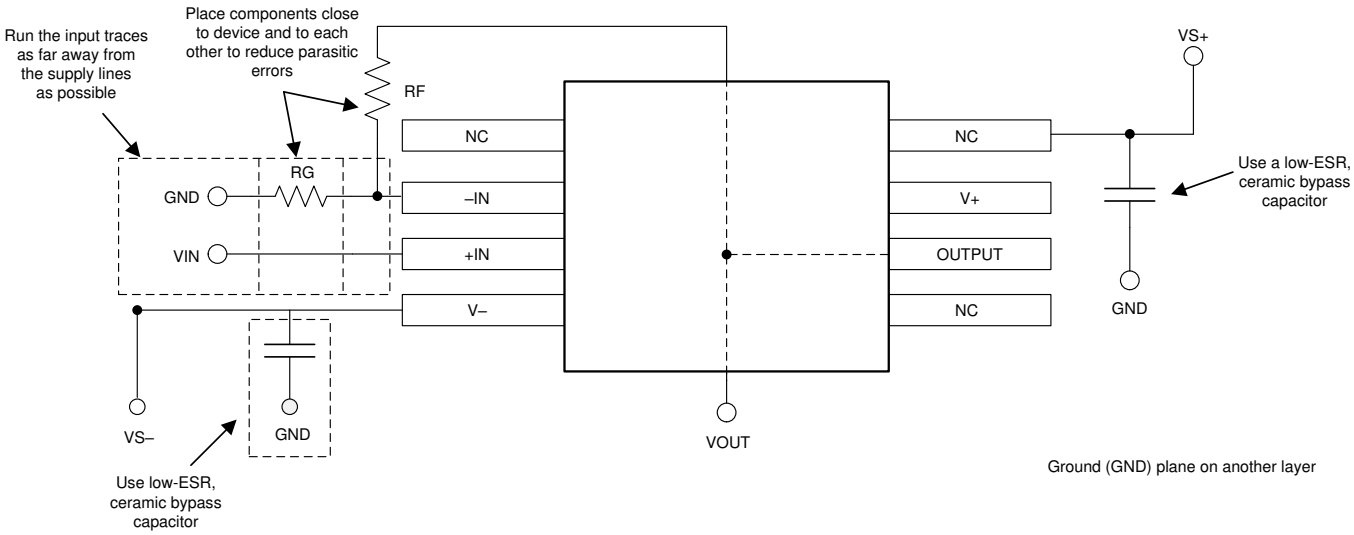


Figure 42. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV2401-Q1	Click here	Click here	Click here	Click here	Click here
TLV2402-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2401QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1WU9
TLV2401QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1WU9
TLV2402QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWX
TLV2402QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWX

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV2401-Q1, TLV2402-Q1 :

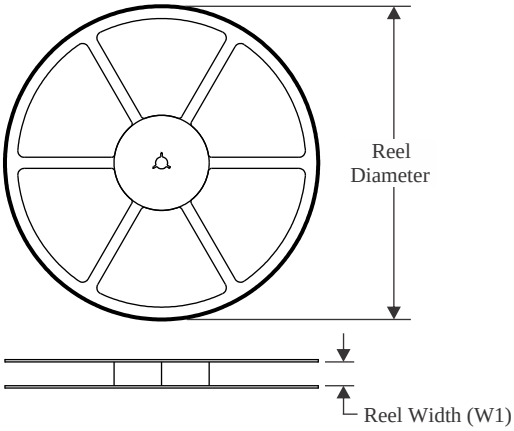
- Catalog : TLV2401, TLV2402

NOTE: Qualified Version Definitions:

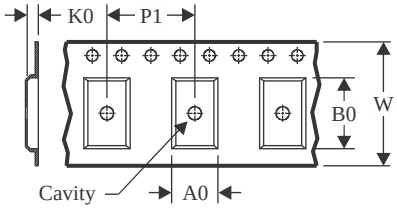
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

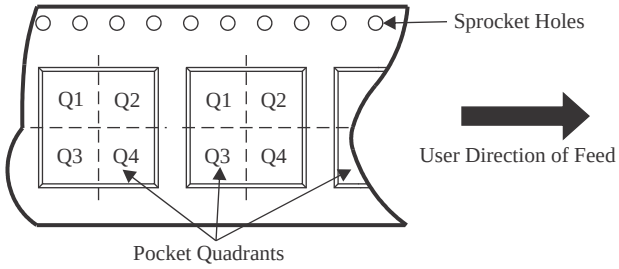


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

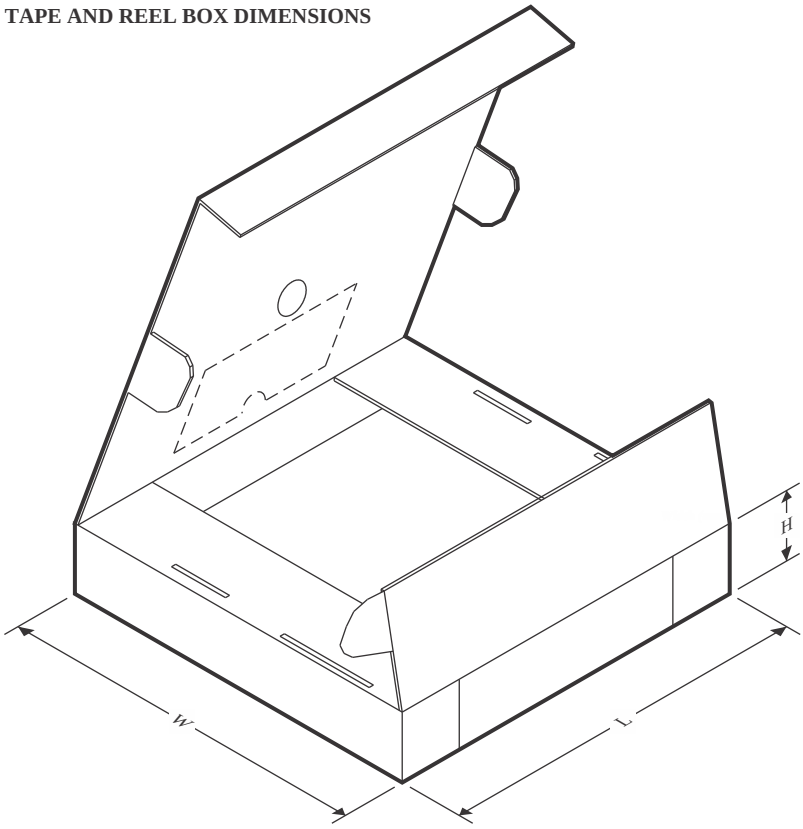
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2401QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2402QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

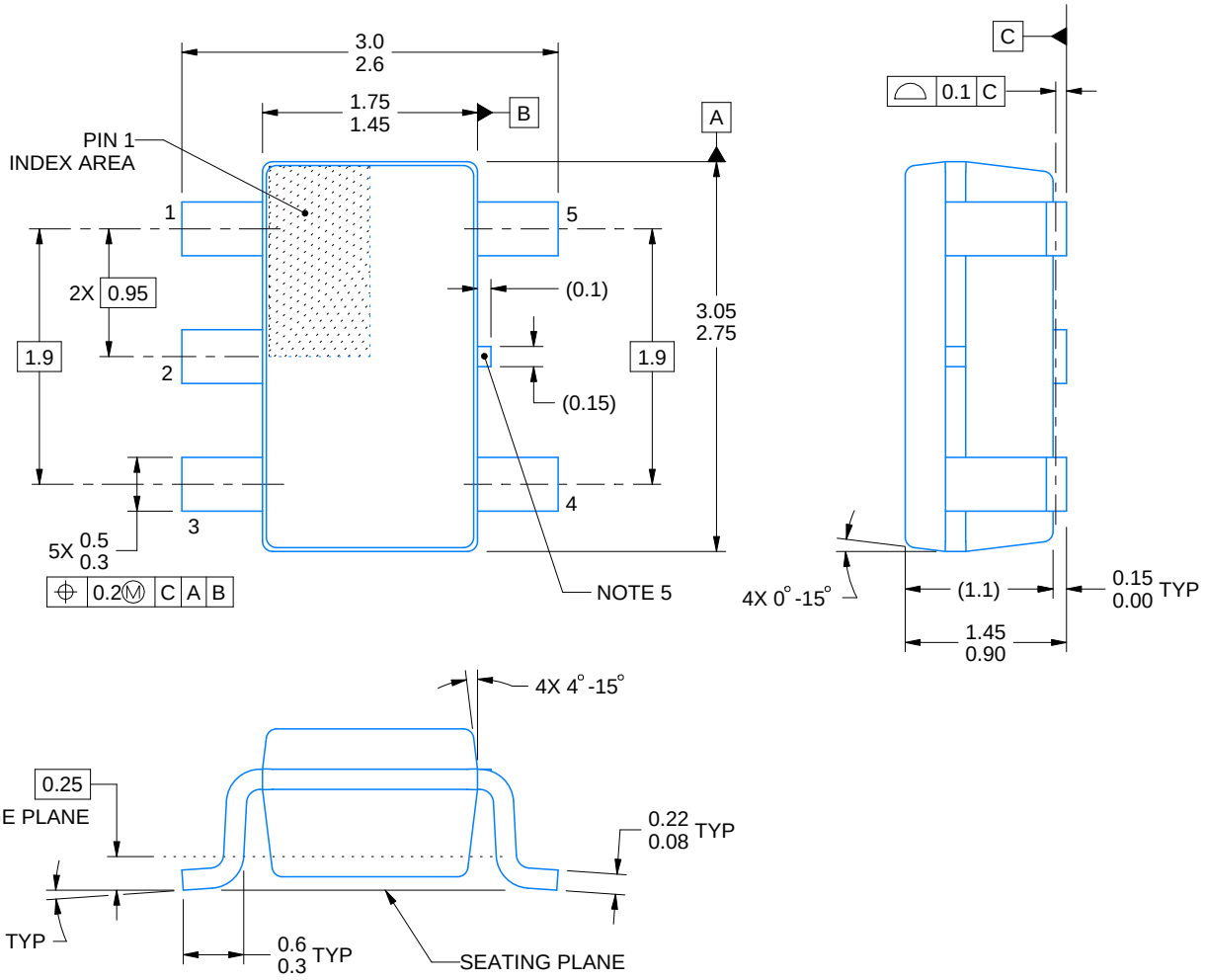
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2401QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2402QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

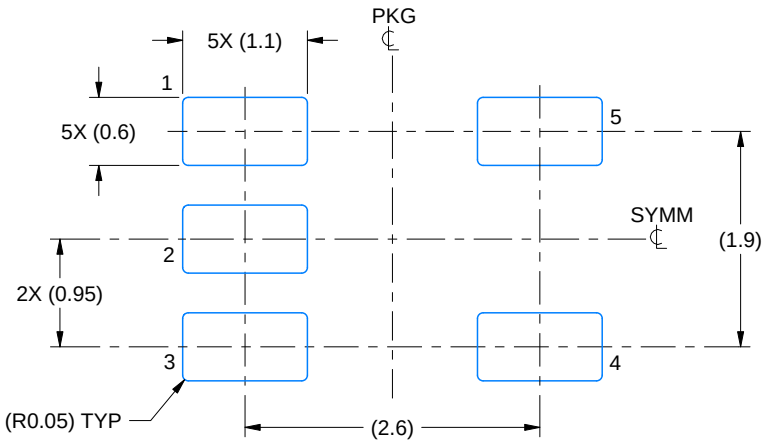
SMALL OUTLINE TRANSISTOR



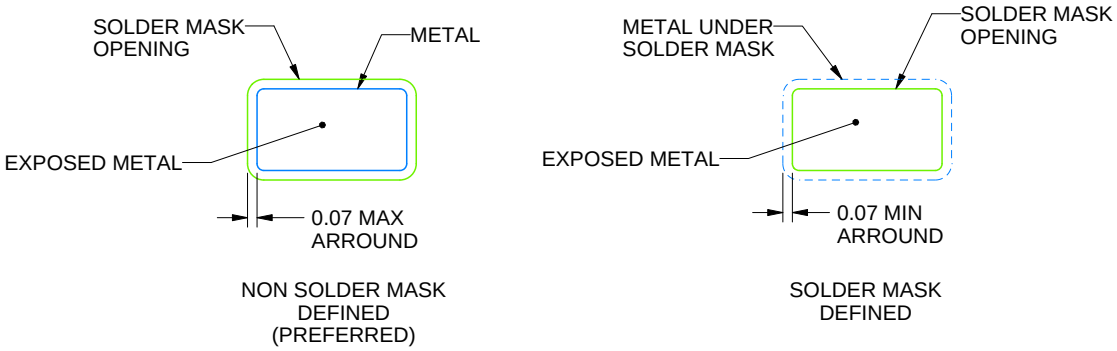
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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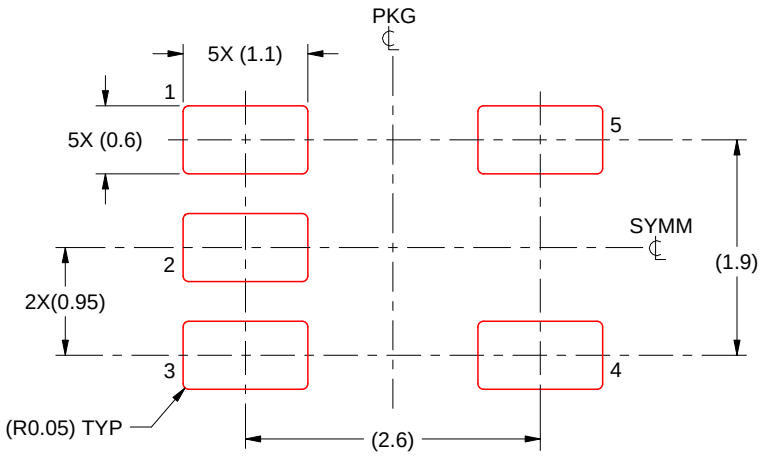
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

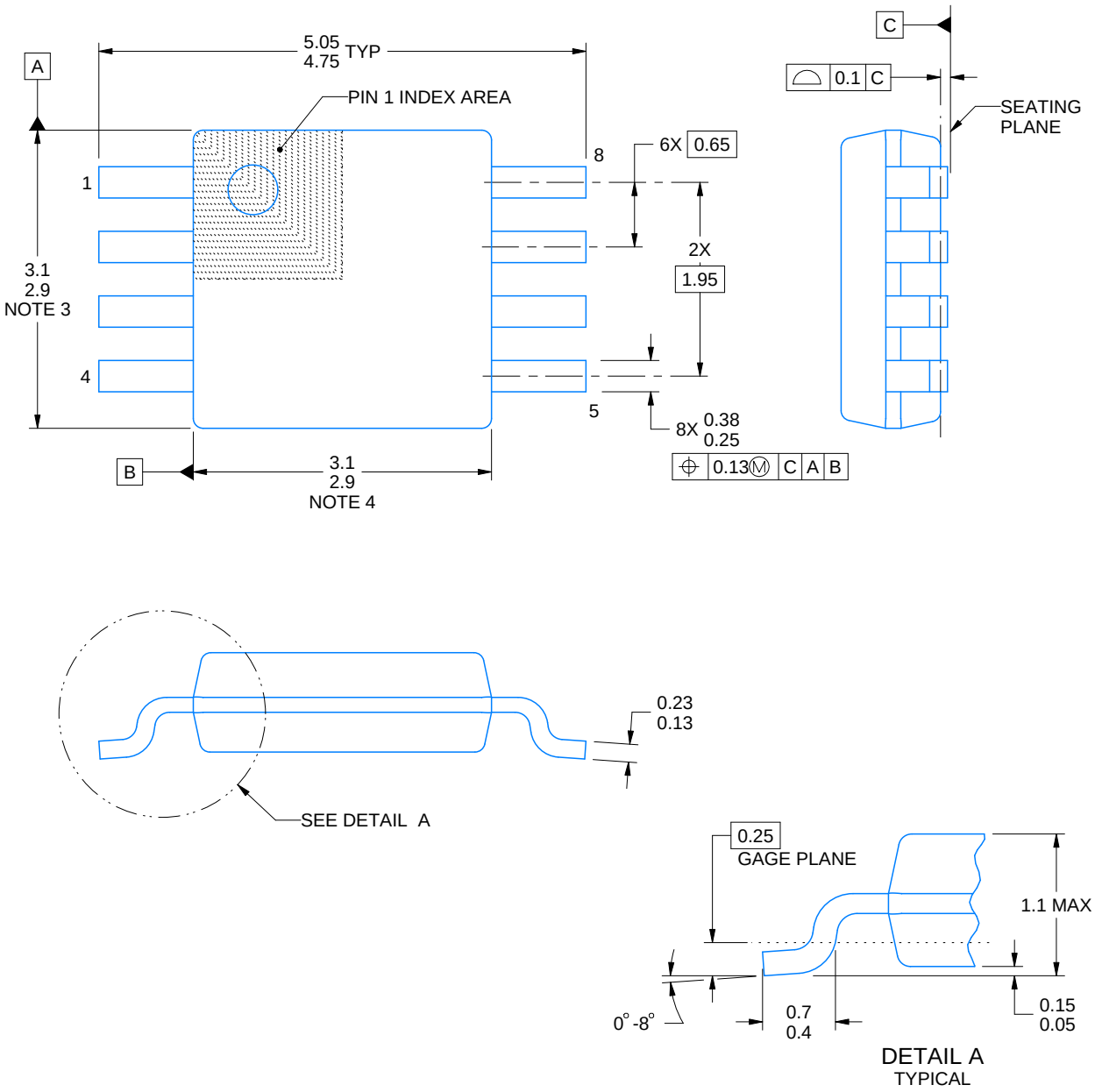
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

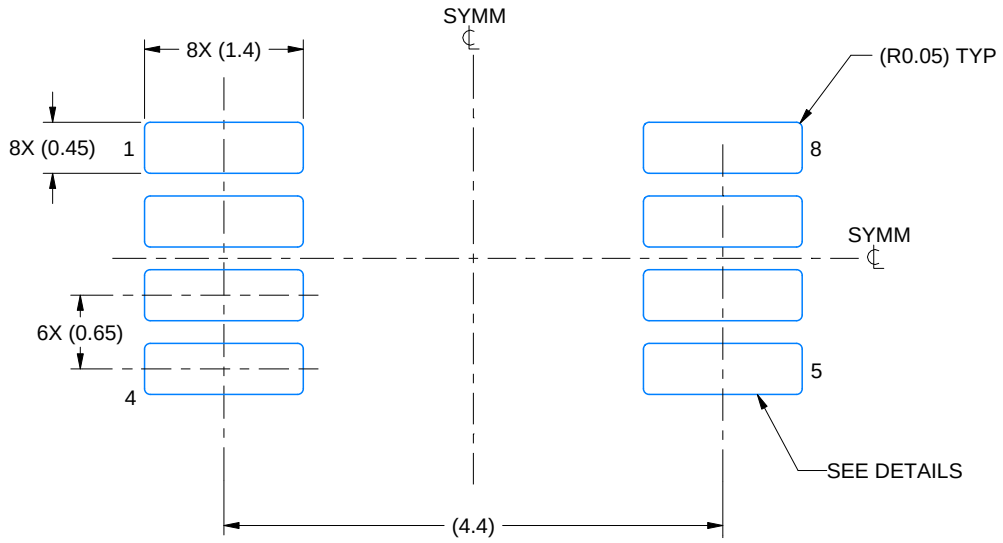
SMALL OUTLINE PACKAGE



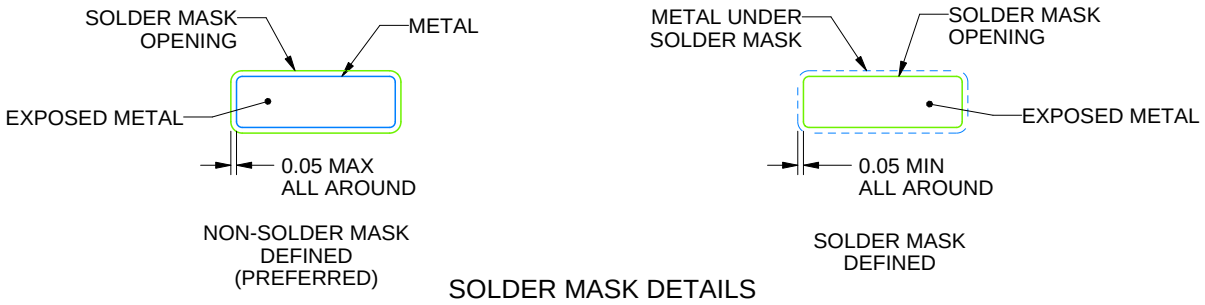
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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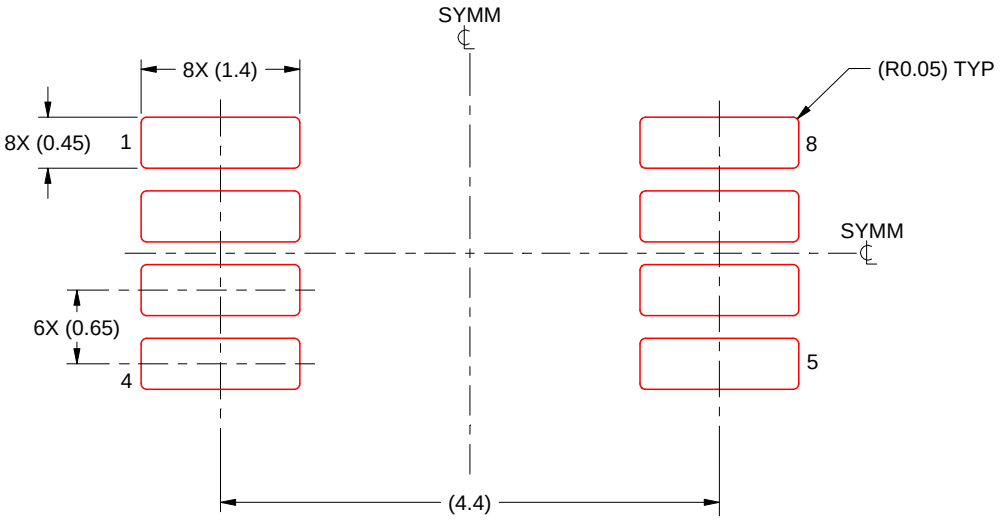
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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