# TLVx888 低ノイズ、ゼロ ドリフト、広帯域幅、マルチプレクサ対応オペアンプ

## 1 特長

- 高い DC 精度:
  - ゼロドリフト: 0.01µV/°C
  - 低いオフセット電圧:3µV
  - 高 PSRR:150 dB
  - 高い CMRR:150 dB
- 優れた AC 性能:
  - ゲイン帯域幅:14MHz
  - スルーレート:40V/µs
  - 低ノイズ:7.5nV/√Hz
- 負レールへの入力、レール ツー レール出力
- 低い静止電流:1.5mA
- RFI および EMI フィルタ付き入力
- 電源電圧範囲:4.5V～36V
- 温度:-40°C ～ +125°C

## 2 アプリケーション

- PC 電源およびゲーム機
- 商用 DC/DC
- 流量トランスミッタ
- 圧力トランスミッタ
- 商用バッテリ チャージャ
- 電気メータ

## 3 概要

TLV888、TLV2888、TLV4888 (TLVx888) は、広帯域幅、低ノイズのゼロドリフトのオペアンプです。これらのオペアンプのオフセット電圧は、わずか 15µV (最大値) であり、温度範囲全体でのオフセット電圧ドリフトは、わずか 0.1µV/°C (最大値) です。

TLVx888 は広いゲイン帯域幅と非常に高いスルー レートにより、非常に短いセトリング時間を特長としています。独自の MUX 対応入力アーキテクチャを使用することで、マルチチャネル システムではセトリング タイムがさらに短縮されます。

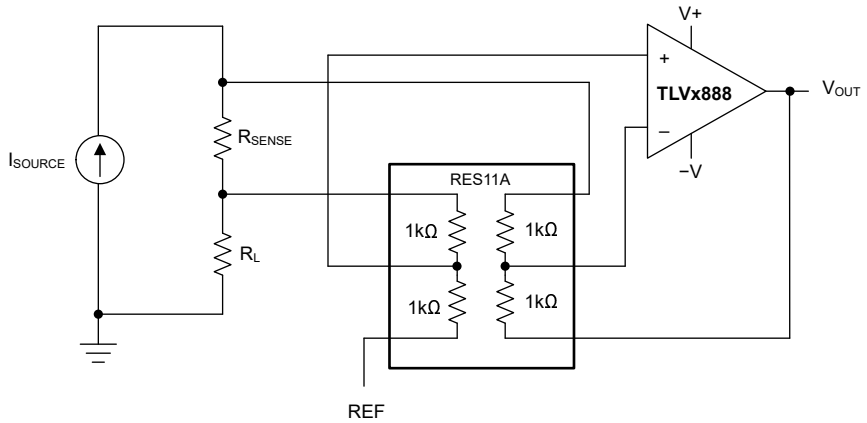
高精度、高速セトリング、低ノイズを兼ね備えた TLVx888 は、信号測定、高精度計測機器、データ アクイジションなど広範なアプリケーションに最適です。

TLVx888 は、業界標準のパッケージとマイクロサイズのパッケージで利用可能、スペースの制約が厳しいアプリケーションに適しています。これらのデバイスの動作範囲は、–40°C ～ +125°C に指定されています。

**製品情報**

| 部品番号 | チャネル数 | パッケージ (1) |
|---|---|---|
| TLV888(2) | シングル | D (SOIC、8) |
| | | DBV (SOT-23、5) |
| | | DRL (SOT、5) |
| TLV2888 | デュアル | D (SOIC、8) |
| | | DDF (SOT-23、8)(2) |
| | | DGK (VSSOP-8)(2) |
| | | DSG (WSON-8)(2) |
| TLV4888(2) | クワッド | D (SOIC、14) |
| | | PW (TSSOP-14) |

(1) 詳細については、セクション 10 を参照してください。
(2) プレビュー情報 (事前情報ではありません)。




**ハイサイド電流シャント モニタ アプリケーション**

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## 4 Pin Configuration and Functions

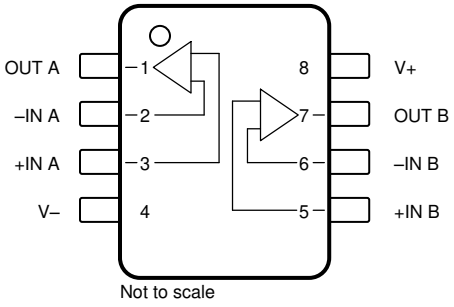



**図 4-1. TLV2888: D Package, 8-Pin SOIC (Top View)**

**表 4-1. Pin Functions: TLV2888**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | Input | Inverting input channel A |
| –IN B | 6 | Input | Inverting input channel B |
| +IN A | 3 | Input | Noninverting input channel A |
| +IN B | 5 | Input | Noninverting input channel B |
| OUT A | 1 | Output | Output channel A |
| OUT B | 7 | Output | Output channel B |
| V– | 4 | Power | Negative supply |
| V+ | 8 | Power | Positive supply |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage | | | 40 | V |
| | Signal input voltage | Common-mode | (V–) – 0.5 | (V+) + 0.5 | V |
| | | Differential | | (V+) – (V–) | |
| | Current | | | ±10 | mA |
| | Output short circuit(2) | | Continuous | | |
| $T_A$ | Operating temperature | | –55 | 150 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±250 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_S$ | Supply voltage, (V+) – (V–) | Single supply | 4.5 | | 36 | V |
| | | Dual supply | ±2.25 | | ±18 | |
| $T_A$ | Operating temperature | | –40 | | 125 | °C |

## 5.4 Thermal Information: TLV2888

| THERMAL METRIC(1) | | TLV2888 D (SOIC) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 148 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 88 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 91 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 37 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 91 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics

at $T_A$ = 25°C, $V_S$ = 4.5V to 36V, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage(1) | | | | ±3 | ±15 | µV |
| | | $T_A$ = –40°C to +125°C | | | | ±20 | |
| $dV_{OS}/dT$ | Input offset voltage drift(1) | $T_A$ = –40°C to +125°C | | | ±0.01 | ±0.05 | µV/°C |
| PSRR | Power-supply rejection ratio(1) | $T_A$ = –40°C to +125°C | | | ±0.03 | ±0.5 | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current(1) | | | | ±50 | ±350 | pA |
| | | $T_A$ = –40°C to +125°C | | | | ±7 | nA |
| $I_{OS}$ | Input offset current(1) | | | | ±100 | ±600 | pA |
| | | $T_A$ = –40°C to +125°C | | | | ±3 | nA |
| **NOISE** | | | | | | | |
| $E_n$ | Input voltage noise | f = 0.1Hz to 10Hz | | | 0.180 | | $µV_{PP}$ |
| $e_n$ | Input voltage noise density | f = 10Hz | | | 7.6 | | $nV/\sqrt{Hz}$ |
| | | f = 100Hz | | | 7.6 | | |
| | | f = 1kHz | | | 7.5 | | |
| $i_n$ | Input current noise density | f = 1kHz | | | 175 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage | | | (V–) – 0.1 | | (V+) – 1.7 | V |
| CMRR | Common-mode rejection ratio | (V–) – 0.1V ≤ $V_{CM}$ ≤ (V+) – 1.7V | $V_S$ = ±2.25V | 118 | 135 | | dB |
| | | | $V_S$ = ±18V | 140 | 150 | | |
| | | (V–) – 0.1V ≤ $V_{CM}$ ≤ (V+) – 1.7V, $T_A$ = –40°C to +125°C | $V_S$ = ±2.25V | 118 | 130 | | |
| | | | $V_S$ = ±18V | 140 | 150 | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $z_{id}$ | Differential input impedance | | | | 100 \|\| 1.6 | | MΩ \|\| pF |
| $z_{ic}$ | Common-mode input impedance | | | | 1 \|\| 1.9 | | TΩ \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = ±15V, (V–) + 0.6V < $V_O$ < (V+) – 0.6V, $R_{LOAD}$ = 10kΩ | | 130 | 148 | | dB |
| | | | $T_A$ = –40°C to +125°C | 130 | | | |
| | | $V_S$ = ±15V, (V–) + 1V < $V_O$ < (V+) – 1V, $R_{LOAD}$ = 2kΩ | | 130 | 144 | | |
| | | | $T_A$ = –40°C to +125°C | 130 | | | |

## 5.5 Electrical Characteristics (続き)

at $T_A$ = 25°C, $V_S$ = 4.5V to 36V, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_{LOAD}$ = 10kΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | | | | 14 | | MHz |
| SR | Slew rate | Gain = 1, 10V step | | | 40 | | V/µs |
| THD+N | Total harmonic distortion + noise | Gain = 1, f = 1kHz, $V_{OUT}$ = 4$V_{RMS}$ | | | 0.00012% | | |
| | Crosstalk | f = 100kHz | | | 110 | | dB |
| $t_S$ | Settling time | $V_S$ = ±18V, gain = 1, 10V step | To 0.1% | | 1 | | µs |
| | | | To 0.01% | | 15 | | |
| $t_{OR}$ | Overload recovery time | $V_{IN}$ × gain = $V_S$ = ±18V | | | 460 | | ns |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing from rail | Positive rail, $V_S$ = 30V | No load | | 26 | 30 | mV |
| | | | $R_{LOAD}$ = 10kΩ | | 122 | 150 | |
| | | | $R_{LOAD}$ = 2kΩ | | 500 | 575 | |
| | | Negative rail, $V_S$ = 30V | No load | | 20 | 25 | |
| | | | $R_{LOAD}$ = 10kΩ | | 120 | 135 | |
| | | | $R_{LOAD}$ = 2kΩ | | 515 | 575 | |
| | | $R_{LOAD}$ = 10kΩ, $T_A$ = –40°C to +125°C, both rails(1) | | | | 225 | |
| $I_{SC}$ | Short-circuit current | | | | ±42 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | | See *Typical Characteristics* | | pF |
| $Z_O$ | Open-loop output impedance | f = 1MHz | | | 220 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $V_S$ = ±2.25V ($V_S$ = 4.5V), $I_O$ = 0A | | | 1.5 | 1.8 | mA |
| | | | $T_A$ = –40°C to +125°C(1) | | 1.5 | 1.9 | |
| | | $V_S$ = ±18V ($V_S$ = 36V), $I_O$ = 0A | | | 1.5 | 1.8 | |
| | | | $T_A$ = –40°C to +125°C(1) | | 1.5 | 1.9 | |

(1) Specification established from device population bench system measurements across multiple lots.

## 5.6 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, and $R_L$ = 10kΩ (unless otherwise noted)

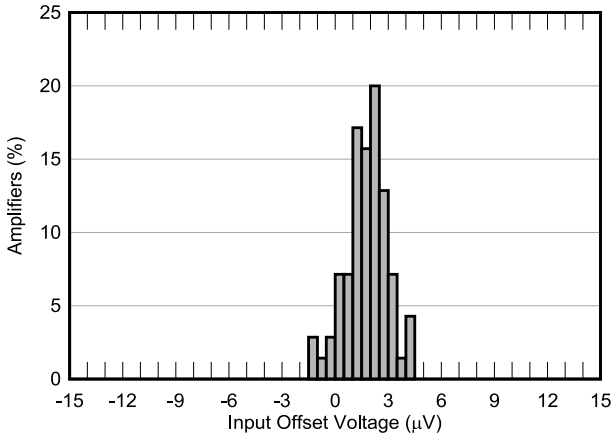



**図 5-1. Offset Voltage Distribution**

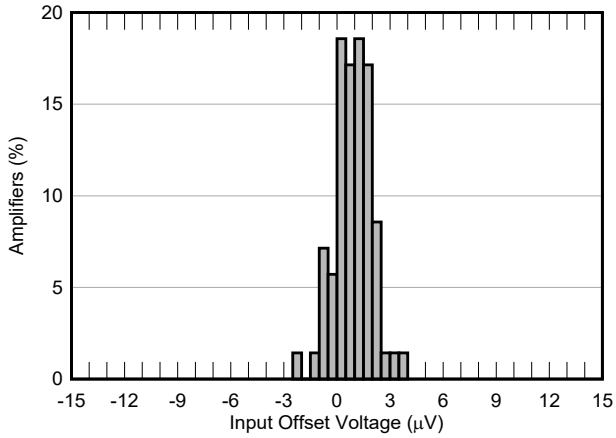



**図 5-2. Offset Voltage Distribution**

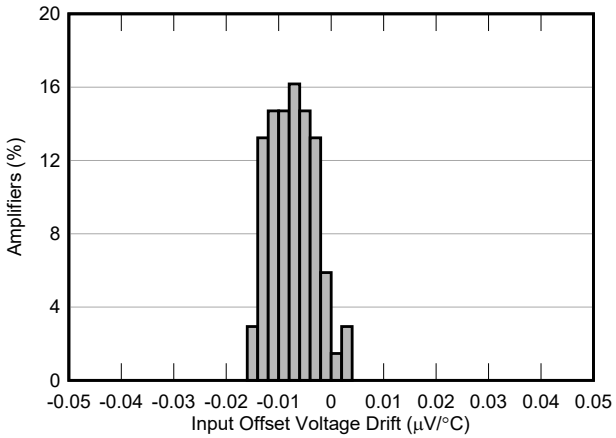



**図 5-3. Offset Voltage Drift**

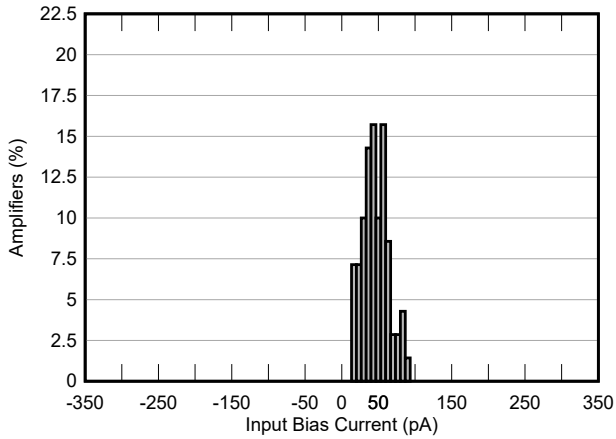



**図 5-4. Input Bias Current Distribution, $I_{BN}$**

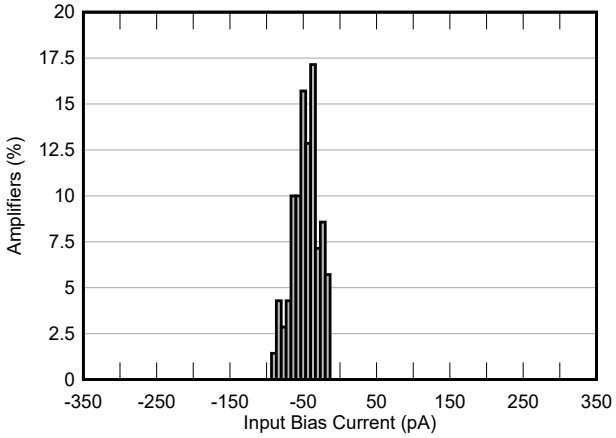



**図 5-5. Input Bias Current Distribution, $I_{BP}$**

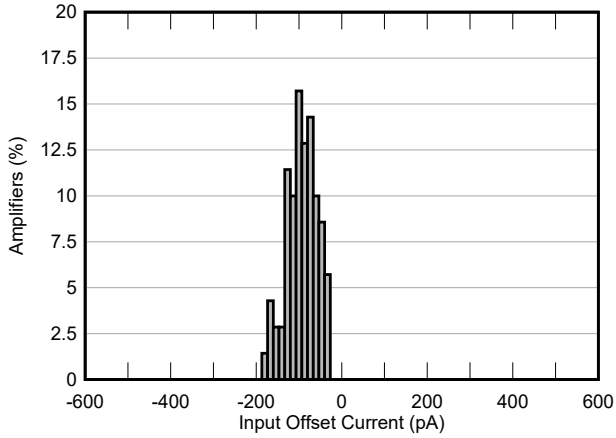



**図 5-6. Input Offset Current Distribution**

## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, and $R_L$ = 10kΩ (unless otherwise noted)

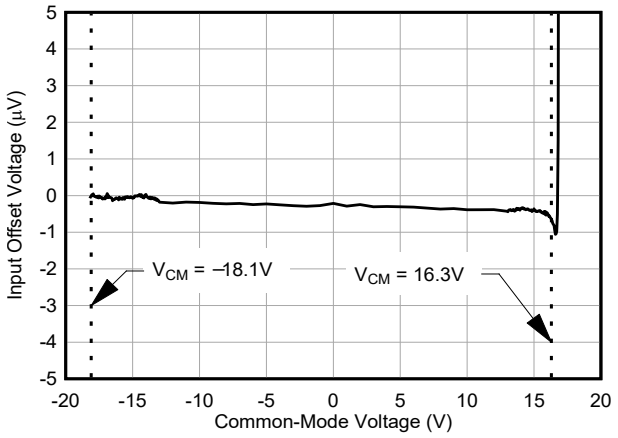



**図 5-7. Offset Voltage vs Common-Mode Voltage**

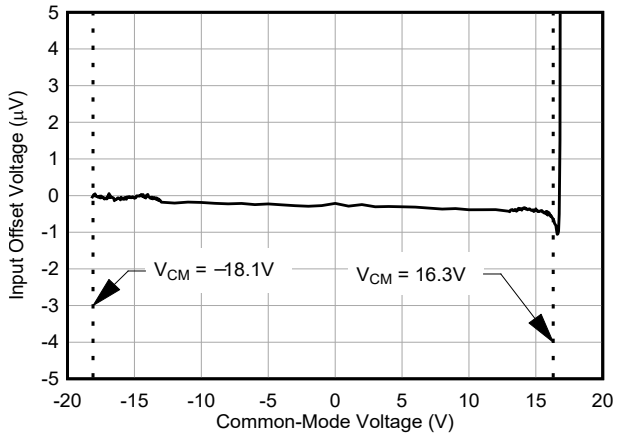



**図 5-8. Offset Voltage vs Common-Mode Voltage**

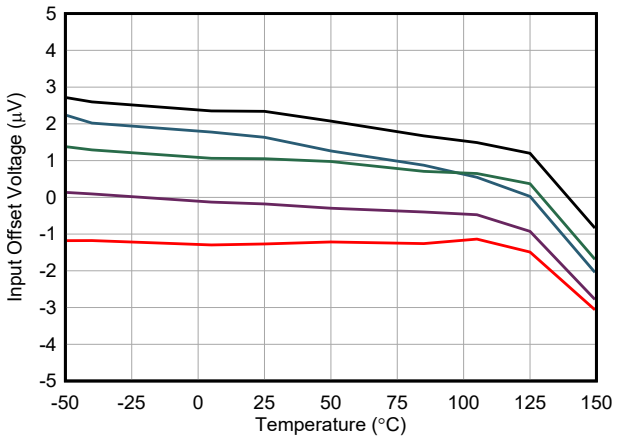



**図 5-9. Offset Voltage vs Temperature**

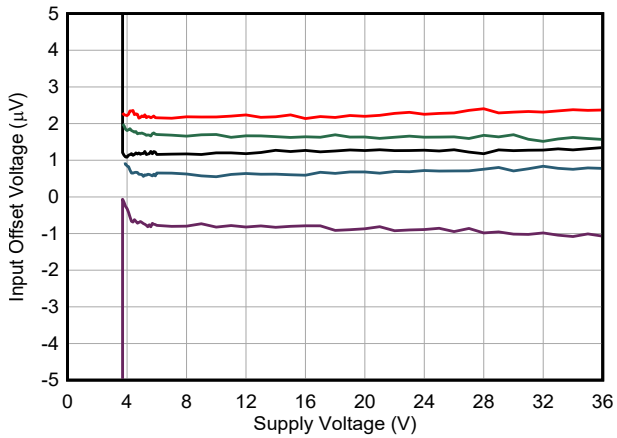



**図 5-10. Offset Voltage vs Supply Voltage**

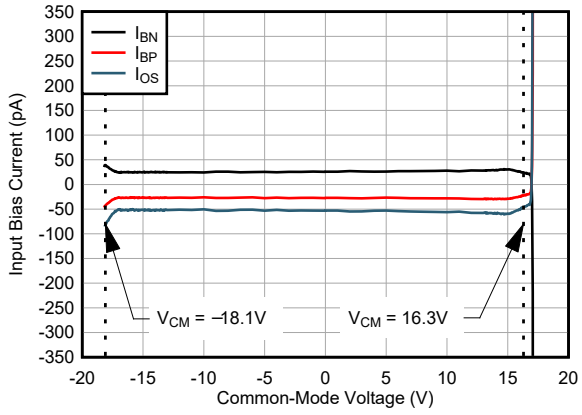



**図 5-11. Input Bias Current vs Common-Mode Voltage**

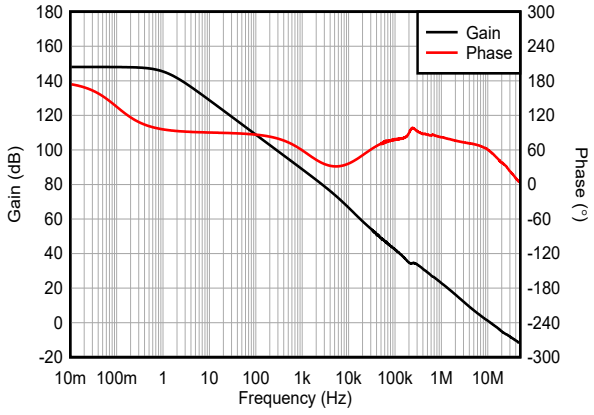



**図 5-12. Open-Loop Gain and Phase vs Frequency**

## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, and $R_L$ = 10kΩ (unless otherwise noted)

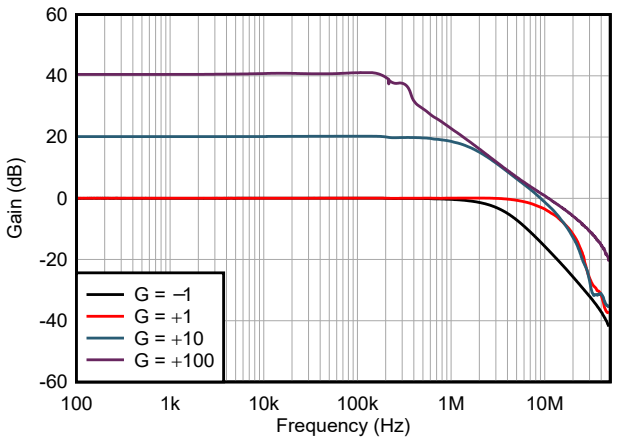



図 5-13. Closed-Loop Gain vs Frequency

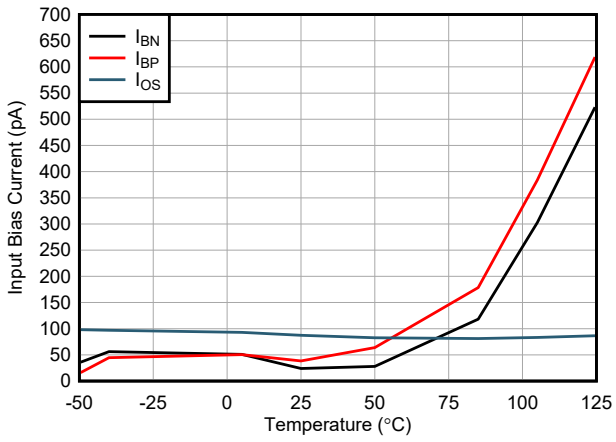



図 5-14. Input Bias Current and Offset Current vs Temperature

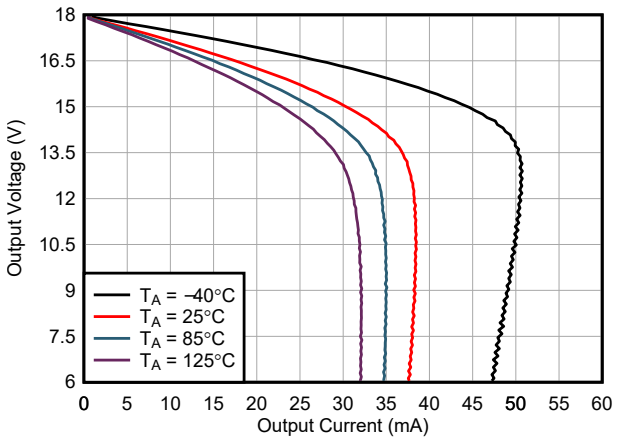



図 5-15. Output Voltage Swing vs Output Current (Sourcing)

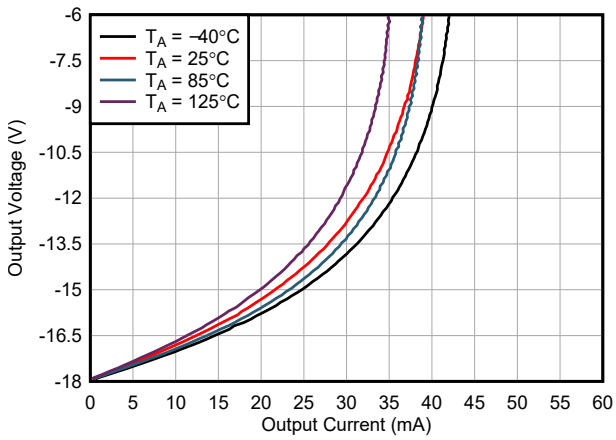



図 5-16. Output Voltage Swing vs Output Current (Sinking)

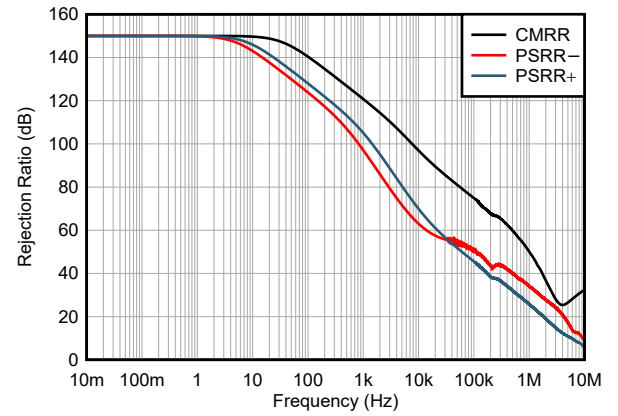



図 5-17. CMRR and PSRR vs Frequency

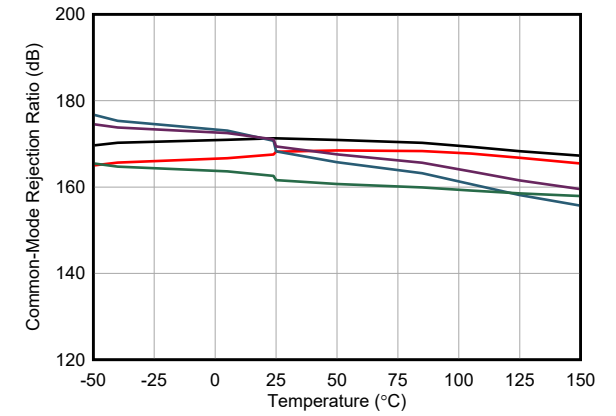



図 5-18. CMRR vs Temperature

## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, and $R_L$ = 10kΩ (unless otherwise noted)

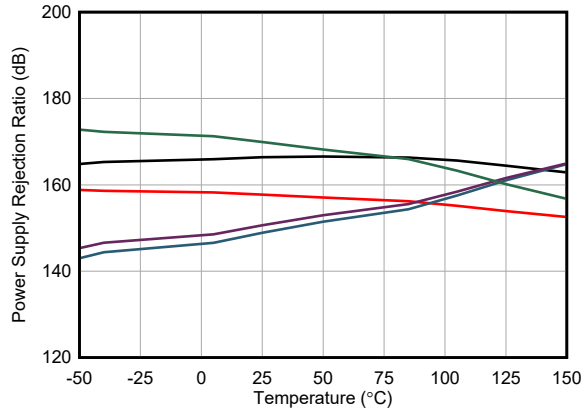



図 5-19. PSRR vs Temperature

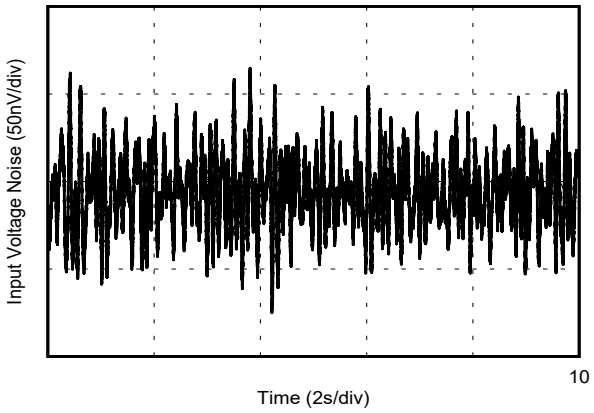



図 5-20. 0.1Hz to 10Hz Voltage Noise

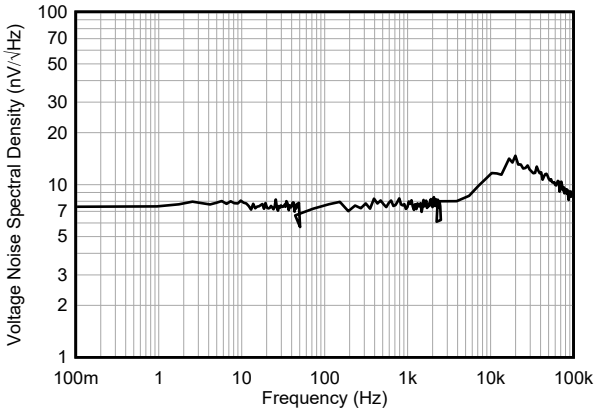



図 5-21. Input Voltage Noise Spectral Density vs Frequency

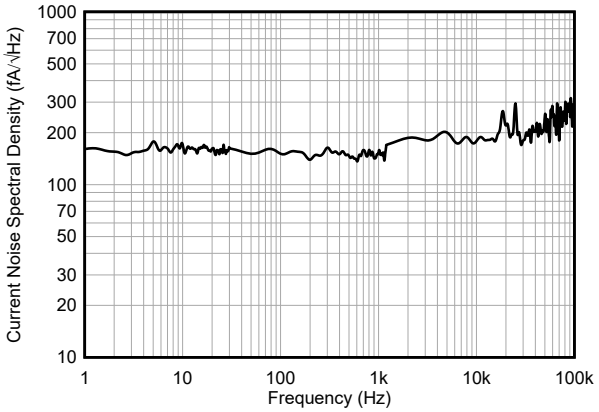



図 5-22. Input Current Noise Spectral Density vs Frequency

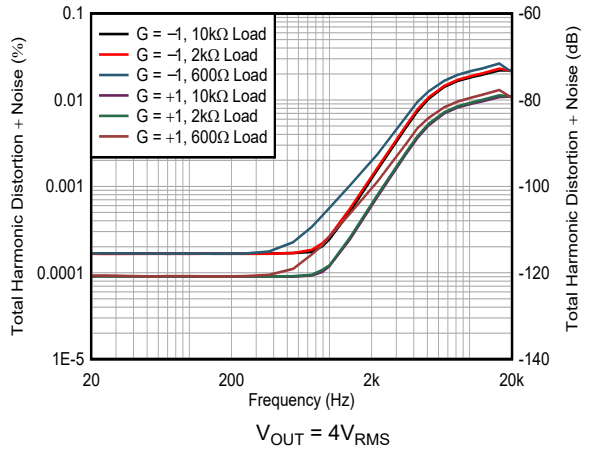



図 5-23. THD+N vs Frequency

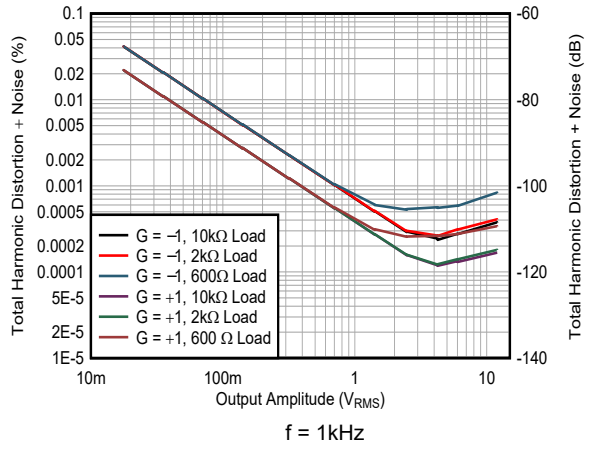
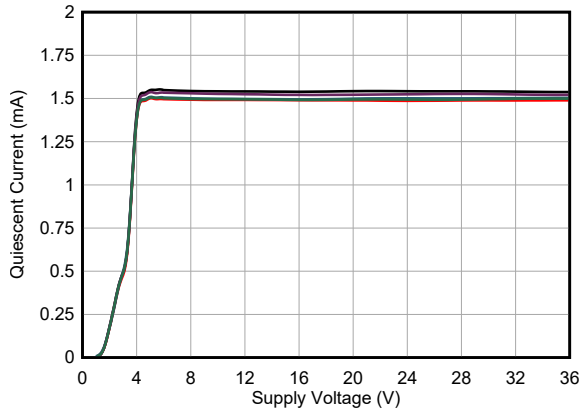



図 5-24. THD+N vs Output Amplitude

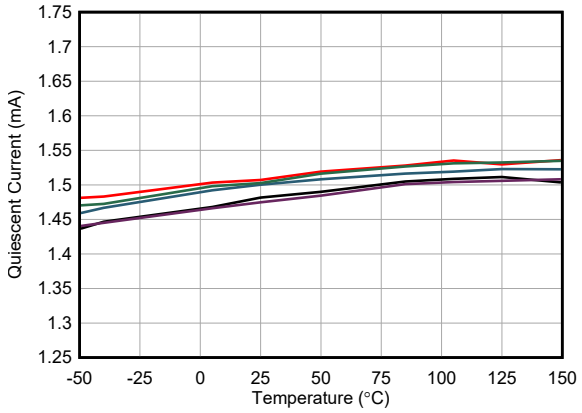
## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, and $R_L$ = 10kΩ (unless otherwise noted)




5 typical units

**図 5-25. Quiescent Current vs Supply Voltage**




5 typical units

**図 5-26. Quiescent Current vs Temperature**

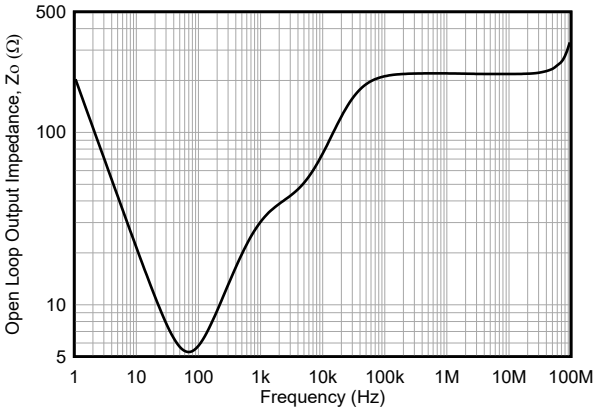
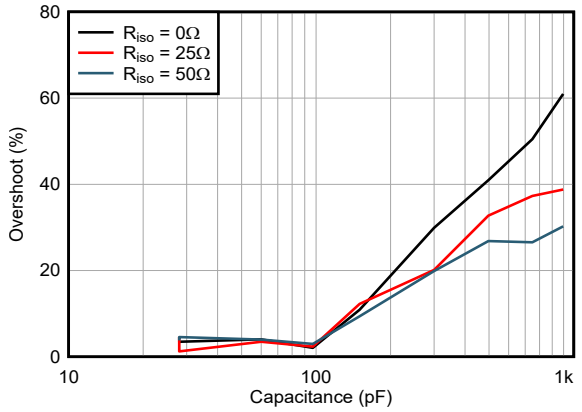
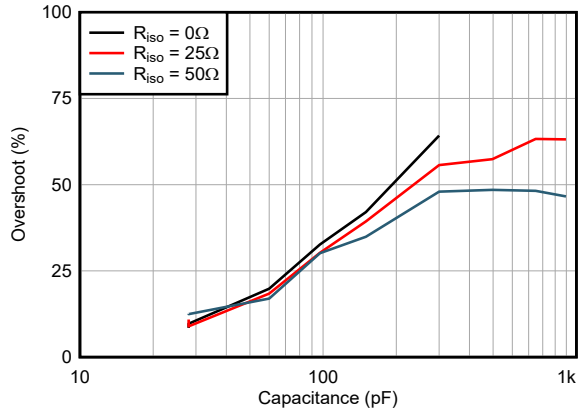



**図 5-27. Open-Loop Output Impedance vs Frequency**




Gain = –1, 10mV step

**図 5-28. Small-Signal Overshoot vs Capacitive Load**




Gain = 1, 10mV step

**図 5-29. Small-Signal Overshoot vs Capacitive Load**

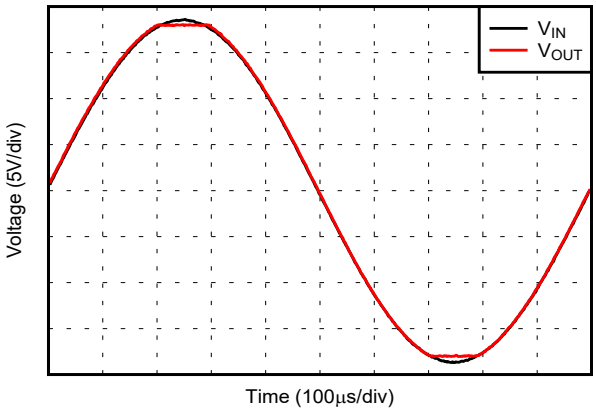



**図 5-30. No Phase Reversal**

## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, and $R_L$ = 10kΩ (unless otherwise noted)

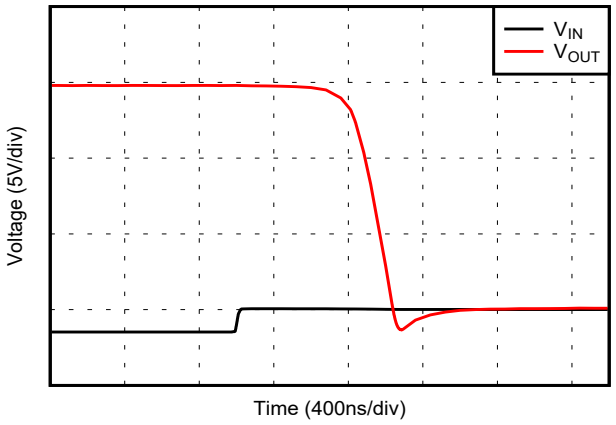



**図 5-31. Positive Overload Recovery**

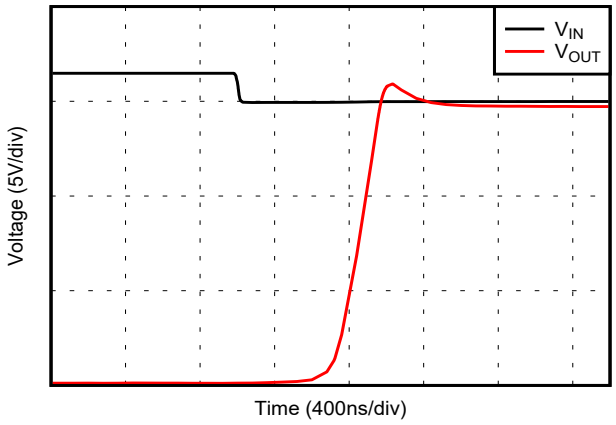
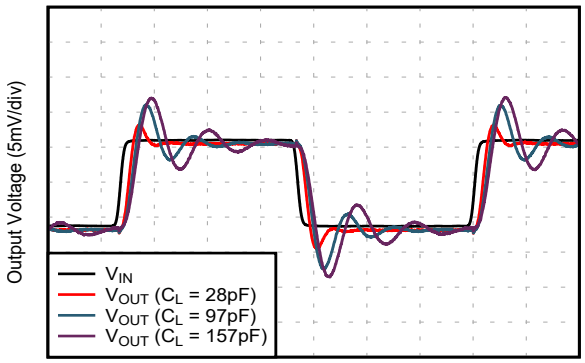
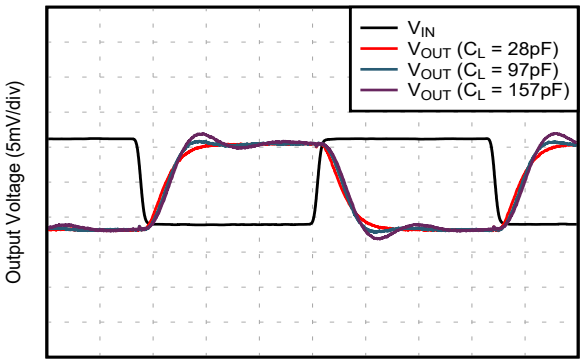



**図 5-32. Negative Overload Recovery**



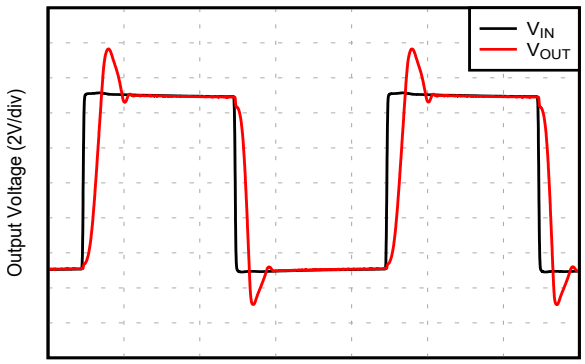

Gain = 1, 10mV step

**図 5-33. Small-Signal Step Response**



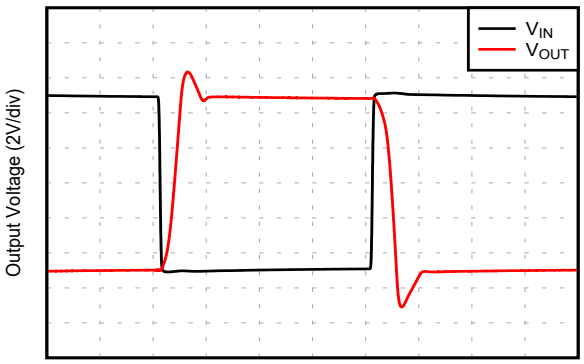

Gain = –1, 10mV step

**図 5-34. Small-Signal Step Response**




Gain = 1, 10V step

**図 5-35. Large-Signal Step Response**




Gain = –1, 10V step

**図 5-36. Large-Signal Step Response**

## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±18V, $V_{CM}$ = $V_S$ / 2, and $R_L$ = 10kΩ (unless otherwise noted)

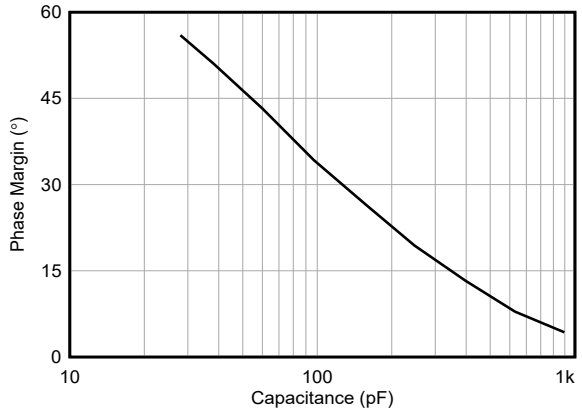
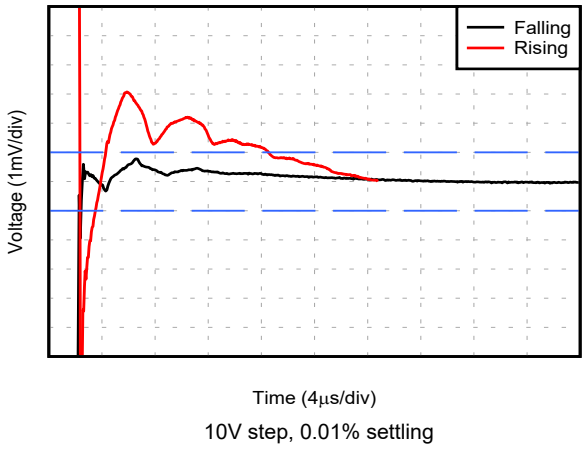



図 5-37. Phase Margin vs Capacitive Load




10V step, 0.01% settling

図 5-38. Settling Time

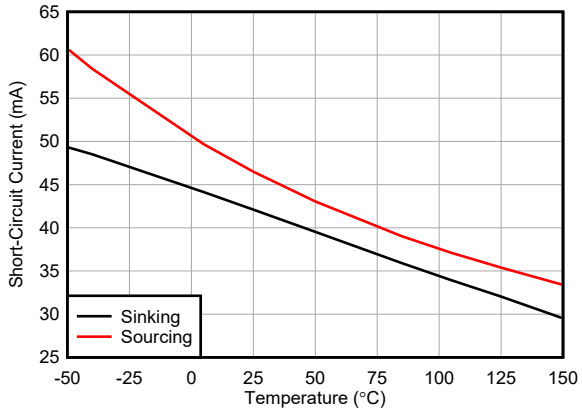



図 5-39. Short Circuit Current vs Temperature

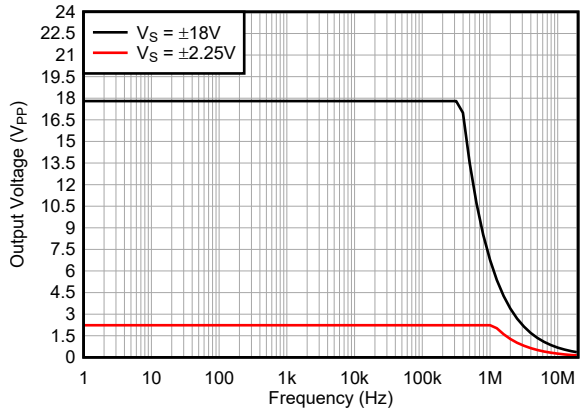



図 5-40. Maximum Output Voltage vs Frequency

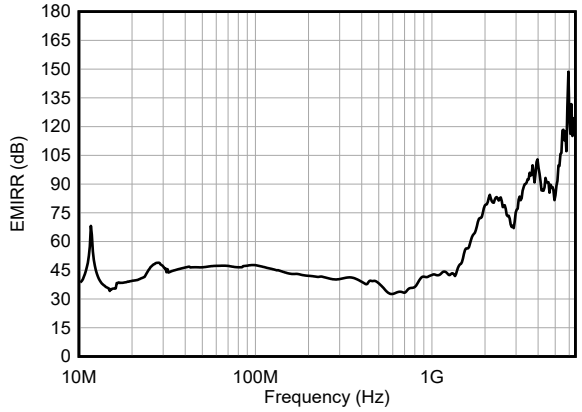



図 5-41. EMIRR vs Frequency

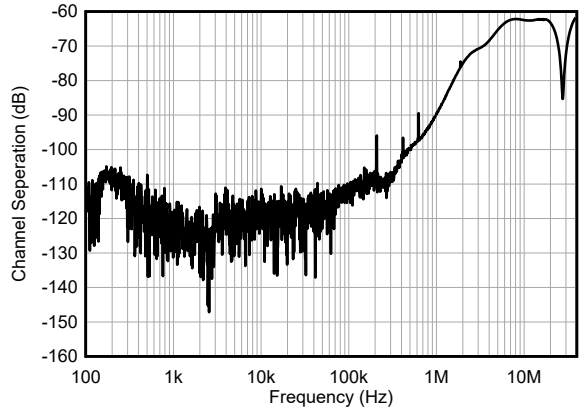



図 5-42. Channel Separation

# 6 Detailed Description

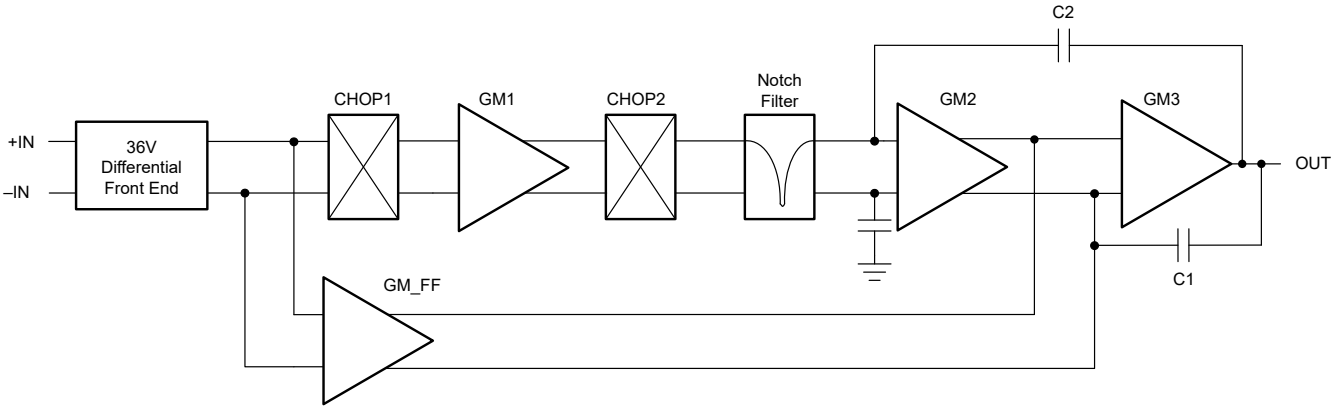
## 6.1 Overview

The TLVx888 operational amplifiers combine precision offset and drift with excellent overall performance, making the device a great choice for a wide variety of precision applications. The precision offset drift of only 0.01µV/°C provides stability over the entire operating temperature range of –40°C to +125°C. In addition, this device offers excellent linear performance with high CMRR, PSRR, and $A_{OL}$. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate. For details and a layout example, see セクション 7.4.

The TLVx888 is part of a family of zero-drift, MUX-friendly operational amplifiers. This device operates from 4.5V to 36V, is unity-gain stable, and is designed for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise, zero flicker noise, and outstanding distortion performance when operating at less than the chopper frequency.

The following section shows a representation of the proprietary TLVx888 architecture.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

The TLVx888 operational amplifiers use a proprietary, periodic autocalibration technique to provide extremely low input offset voltage and input offset voltage drift over time and temperature. The devices have several integrated features to help maintain a high level of precision through a variety of applications. These include a phase-reversal protection, EMI rejection, electrical overstress protection, and MUX-friendly inputs.

Several design techniques and considerations to maintain the specified performance of the TLVx888 are detailed in the *Optimizing Chopper Amplifier Accuracy* and *Op Amp Offset Voltage and Bias Current Limitations* application notes.

### *6.3.1 Input Common-Mode Range*

The TLVx888 are specified for operation from 4.5V to 36V (±2.25V to ±18V). The TLVx888 provide a wide input common-mode voltage ($V_{CM}$) range that includes the negative rail making them an excellent choice for single supply operation. The input common-mode voltage to the positive rail is limited to (V+) − 1.7V. Limit the input common mode voltage to (V–) – 0.1V ≤ $V_{CM}$ ≤ (V+) – 1.7V to maintain specified performance.

### 6.3.2 Phase-Reversal Protection

The TLVx888 have internal phase-reversal protection. Some op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLVx888 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. 図 6-1 shows this performance.

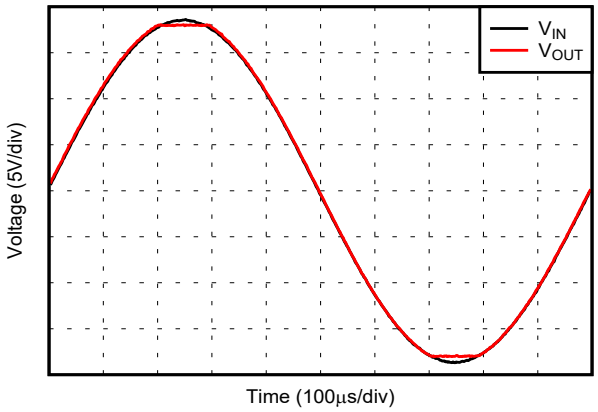



**図 6-1. No Phase Reversal**

### 6.3.3 Chopping Transients

Zero-drift amplifiers such as the TLVx888 use a switching architecture on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying; however, the pulses can be coupled to the output of the amplifier through the feedback network. Use low value resistors to minimize the input transient effects at the output of the amplifier. Use a low-pass filter, such as an RC network, to minimize any additional noise attributed to the transients. The chopping frequency of the TLVx888 is typically 200kHz.

### 6.3.4 EMI Rejection

The TLVx888 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLVx888 benefits from these design improvements.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects, as there is insufficient amplifier loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

### 6.3.5 Electrical Overstress

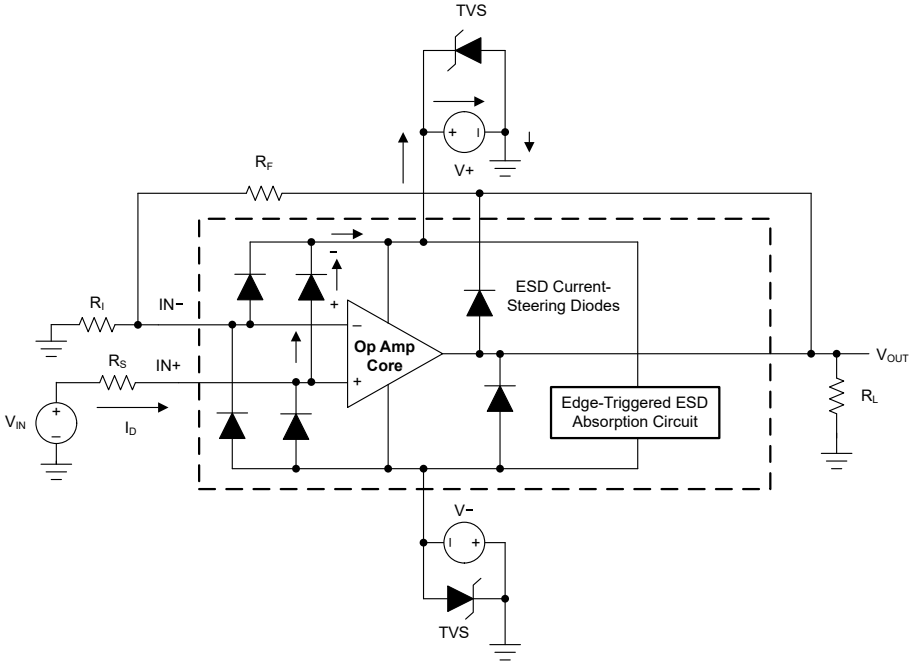
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 図 6-2 shows an illustration of the ESD circuits contained in the TLVx888 (shows as the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the op amp. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger or threshold voltage that is greater than the normal operating voltage of the TLVx888, but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

図 6-2 shows that when the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive, and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits are biased on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.




Notes: $V_{IN}$ = (V+) + 500mV.
TVS: V+ < $V_{TVSBR\ (min)}$ < 40V, where $V_{TVSBR\ (min)}$ is the minimum specified value for the TVS breakdown voltage.

Suggested value for $R_S$ is approximately 5kΩ in an overvoltage condition.

**図 6-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

図 6-2 shows a specific example where the input voltage ($V_{IN}$) exceeds the positive supply voltage (V+) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher $V_{IN}$. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, $V_{IN}$ can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current-steering diodes. This state is not a normal biasing condition for the amplifier and can result in specification degradation or abnormal operation. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external transient voltage suppressor (TVS) diodes to the supply pins; see also 図 6-2. The breakdown voltage must be selected such that the diode does not turn on during normal operation. However, the breakdown voltage must be low enough so that the TVS diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

### *6.3.6 MUX-Friendly Inputs*

The TLVx888 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature antiparallel diodes that protect input transistors from large $V_{GS}$ voltages that can exceed the semiconductor process maximum and permanently damage the device. Large $V_{GS}$ voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator.

The TLVx888 solves these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This input architecture addresses many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials. 図 6-3 shows a typical application where MUX-Friendly inputs can improve settling time performance. The TLVx888 offers outstanding settling performance as a result of these design innovations and built-in slew-rate boost and wide bandwidth. The TLVx888 can also be used as a comparator. Differential and common-mode input ranges still apply.

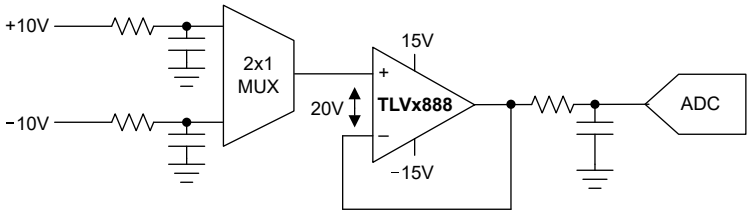



**図 6-3. Multiplexed Application**

## 6.4 Device Functional Modes

The TLVx888 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The recommended power supply voltage for the TLVx888 is 36V (±18V).

# 7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The TLVx888 operational amplifier combines precision offset and drift with excellent overall performance, making the device an excellent choice for many precision applications. The precision offset drift of only 0.01µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and $A_{OL}$ dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate.

### *7.1.1 Basic Noise Calculations*

Low-noise circuit design requires careful analysis of all noise sources. In many cases, external noise sources can dominate; consider the effect of source resistance on overall op-amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is usually fixed; consequently, select op amp and the feedback resistors that minimize the respective contributions to the total noise.

図 7-1 shows the noninverting op-amp circuit configurations with gain. 図 7-2 shows the inverting op-amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the low current noise of the TLVx888 means that the current noise contribution can be ignored.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

For additional resources on noise calculations, visit *TI Precision Labs*.

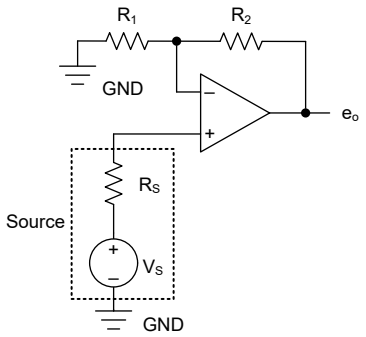



**図 7-1. Noise Calculation in Noninverting Gain Configurations**

$$E_o = e_o\sqrt{BW_N}\ [V_{RMS}] \quad (1)$$

$$e_o = \left(1 + \frac{R_2}{R_1}\right)\sqrt{{e_S}^2 + {e_N}^2 + \left(e_{R_1||R_2}\right)^2 + \left(i_N R_S\right)^2 + \left(i_N \frac{R_1 R_2}{R_1 + R_2}\right)^2}\left[\frac{V}{\sqrt{Hz}}\right] \quad (2)$$

$$e_S = \sqrt{4k_B T(K) R_S}\left[\frac{V}{\sqrt{Hz}}\right] \quad (3)$$

$$e_{R_1||R_2} = \sqrt{4k_B T(K)\left(\frac{R_1 R_2}{R_1 + R_2}\right)}\left[\frac{V}{\sqrt{Hz}}\right] \quad (4)$$

$$k_B = 1.38065 \times 10^{-23}\left[\frac{J}{K}\right] \quad (5)$$

$$T(K) = 2.37.15 + T(°C)\ [K] \quad (6)$$

where

- $e_n$ is the voltage noise spectral density of the amplifier. For the TLVx888, $e_n$ = 7.5nV/√Hz at 1kHz)
- $e_o$ is the total noise density
- $e_S$ is the thermal noise of $R_S$
- $e_{R_1 \,||\, R_2}$ is the thermal noise of $R_1$ || $R_2$
- $k_B$ is the Boltzmann constant
- T(K) is the temperature in kelvins

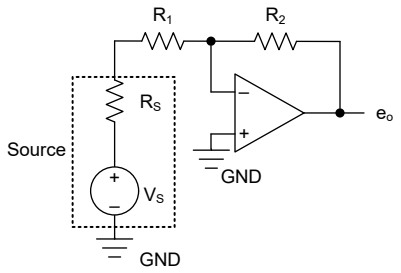



**図 7-2. Noise Calculation in Inverting Gain Configurations**

$$E_o = e_o\sqrt{BW_N}\,[V_{RMS}] \tag{7}$$

$$e_o = \left(1 + \frac{R_2}{R_S + R_1}\right)\sqrt{{e_N}^2 + \left(e_{R_1 + R_S||R_2}\right)^2 + \left(i_N\frac{(R_S + R_1)R_2}{R_S + R_1 + R_2}\right)^2}\left[\frac{V}{\sqrt{Hz}}\right] \tag{8}$$

$$e_{R_1 + R_S||R_2} = \sqrt{4k_B T(K)\left(\frac{(R_S + R_1)R_2}{R_S + R_1 + R_2}\right)}\left[\frac{V}{\sqrt{Hz}}\right] \tag{9}$$

$$k_B = 1.38065 \times 10^{-23}\left[\frac{J}{K}\right] \tag{10}$$

$$T(K) = 2.37.15 + T(°C)\,[K] \tag{11}$$

where

- See

- $e_n$ is the voltage noise spectral density of the amplifier. For the TLVx888, $e_n$ = 7.5nV/√Hz at 1kHz)
- $e_o$ is the total noise density
- $e_S$ is the thermal noise of $R_S$
- $e_{(R_1 + R_S)\,||\,R_2}$ is the thermal noise of ($R_1$ + $R_S$) || $R_2$
- $k_B$ is the Boltzmann constant
- T(K) is the temperature in kelvins

## 7.2 Typical Applications

### 7.2.1 High-Side Current Sensing

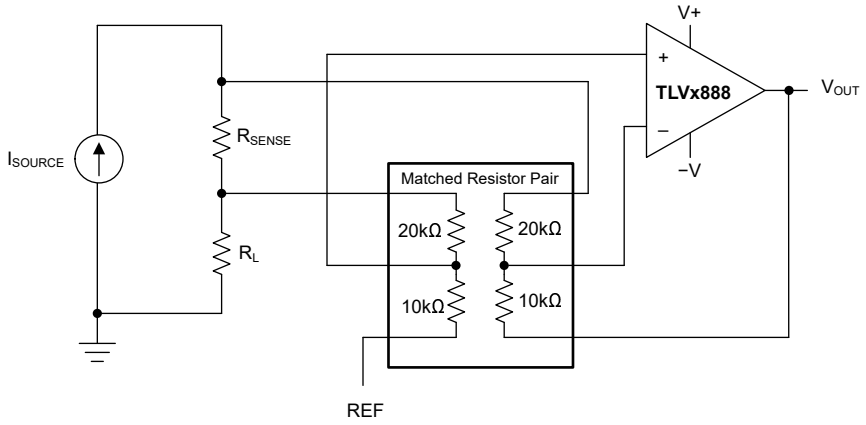



**図 7-3. High-Side Current Monitor**

#### 7.2.1.1 Design Requirements

A common systems requirement is to monitor the current being delivered to a load. Monitoring confirms that normal current levels are being maintained, and also provides an alert if an overcurrent condition occurs.

Fortunately, a relatively simple current monitor circuit can be achieved using a precision op amp, such as the TLVx888. This device has exceptional precision and wide gain bandwidth product to accommodate for very high gain configurations.

The TLVx888 is configured as a difference amplifier with a predetermined gain. The difference amplifier inputs are connected across a sense resistor through which the load current flows. The sense resistor can be connected to the high side or low side of the circuit through which the load current flows. Commonly, high-side current sensing is applied. 図 7-3 shows an applicable TLVx888 configuration. Low-side current sensing can be applied as well if the sense resistor can be placed between the load and ground.

Use the following parameters for this design example:

- Dual supply: ±15V
- Linear output voltage range: 0V to 5V
- Load current, $I_L$: 1mA to 100mA

The following design details and equations can be used to reconfigure this design for different output voltage ranges and current loads.

#### 7.2.1.2 Detailed Design Procedure

Designing a high-side current monitor circuit is straightforward, provided that the amplifier electrical characteristics are carefully considered so that linear operation is maintained. Other additional characteristics, such as the input voltage range of the analog to digital converter (ADC) that follows the current monitor stage, must also be considered when configuring the system.

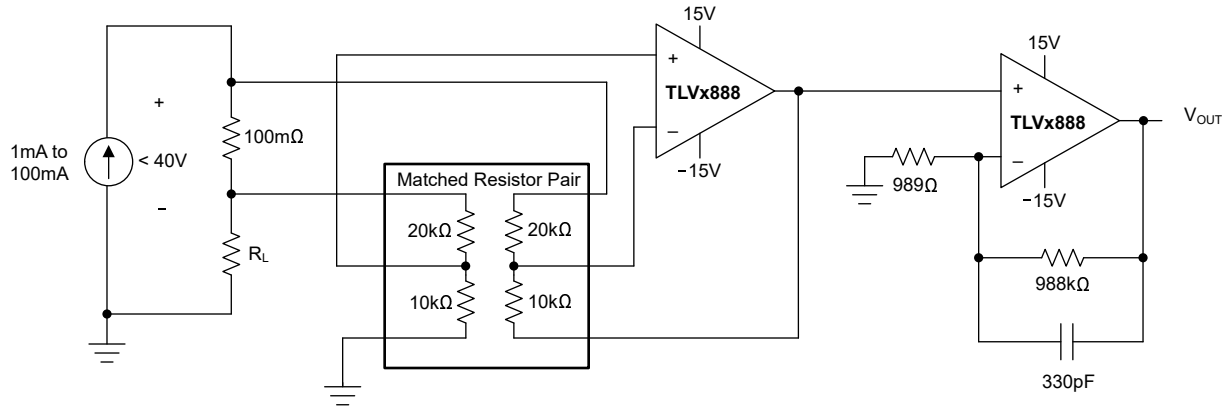



**図 7-4. High Side Current Sense With Gain Stage**

For example, consider the design of a TLVx888 high-side current monitor with an output voltage range set to be compatible with the input of an ADC with a full-scale input range of 0V to 5V. Although the TLVx888 is specified as a rail-to-rail output amplifier, the linear output operating range (like all amplifiers) does not quite extend all the way to the supply rails. This linear operating range must be considered.

In this design example, the TLVx888 is powered by ±15V; therefore, the device is easily capable of providing the 0V to 5V swing; or even more, if the ADC has a wider input range.

The best measure of an op-amp linear output voltage range comes from the open-loop voltage gain ($A_{OL}$) specification listed in the *Electrical Characteristics* table. The $A_{OL}$ test conditions specify a linear swing range from 600mV from each supply rail ($R_L$ = 10kΩ).

A nominal load current ($I_L$) of 100mA is used in this example. In most applications, however, the ability to monitor current levels far less than 100mA is useful.

Selection of current sense resistor $R_S$ comes down to how much voltage drop can be tolerated at maximum current and the permissible power loss or dissipation. A good compromise for a 100mA sense application is an $R_S$ of 100mΩ. That value results in a power dissipation of 1mW, and a 10mV drop at 100mA.

Next, determine the gain of the TLVx888 difference amplifier circuit. The maximum current of 100mA flowing through a 100mΩ sense resistor results in 100mV across the resistor. The gain of the difference amplifier is limited by the required input common-mode voltage. A gain of 1/2, for example, provides a 1/3 attenuation of the high side voltage seen by the circuit. The attenuation is enough to keep the input common-mode within the range of the TLVx888, (V+) − 1.7V.

The differential voltage that is applied across the TLVx888 difference amplifier circuit inputs is attenuated by the difference amplifier and a gain stage is needed for proper scaling. Conveniently, the second channel of the TLV2888 can used. The ultra-low offset and wide-bandwidth enable very high gain configurations. In this example, a gain of 1000V/V provides the necessary scaling for a 0V to 5V output.

The TLVx888 output voltage is intentionally limited to 5V. However, because of the ±15V supply, the output voltage can be much higher to allow for a higher voltage data converter with a wider dynamic range.

The TLVx888 output, as well as other CMOS output amplifiers, often swing closer to 0V (in single supply configurations) than the linear output parameters suggest. The voltage output swing, $V_O$ (see the *Electrical Characteristics* table), is not an indication of the linear output range, but rather how close the output can move

towards the supply rail. In that region, the amplifier output approaches saturation, and the amplifier ceases to operate linearly. Thus, in the current-monitor application, the current-measurement capability can continue to much less than the 600mV output level. However, keep in mind that the linearity errors are becoming large.

Lastly, some notes about maximizing the high-side current monitor performance:

1. All resistor values are critical for accurate gain results. Match resistor pairs of [R1 and R3] and [R2 and R4] as closely as possible to minimize common-mode mismatch error. Use a 0.1% tolerance, or better. Often, selecting two adjacent resistors on a reel provides close matching compared to random selection. The *RES21A* provides an even more elegant circuit design with better performance than discrete 0.1% resistors.
2. Keep the closed-loop gain, G, of the difference amplifier set to a reasonable value to reduce gain error and maximize bandwidth. The high bandwidth of TLVx888 enables very high gain configurations.
3. Although current monitoring is often used for monitoring dc supply currents, ac current can also be monitored. Special attention to the −3dB cutoff frequency of the circuit is warranted.

For more information about amplifier-based, high-side current monitors, see the *TI Analog Engineer's Circuit Cookbook: Amplifiers*.

#### 7.2.1.3 Application Curve

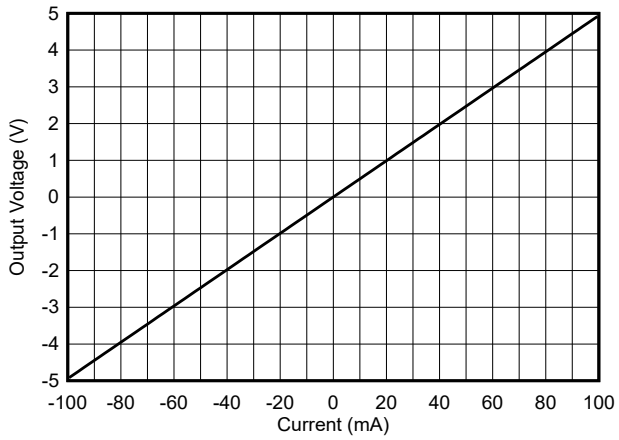



**図 7-5. Current Sense Measurement Results**

### 7.2.2 Programmable Current Source

図 7-6 shows the basic configuration for a precision current source using the TLVx888. The circuit provides a configurable current source to a floating load. 図 7-6 uses a digital-to-analog converter (DAC) to set the current level. For example, a 5V full-scale voltage at the input of the amplifier provides a 100mA current source.

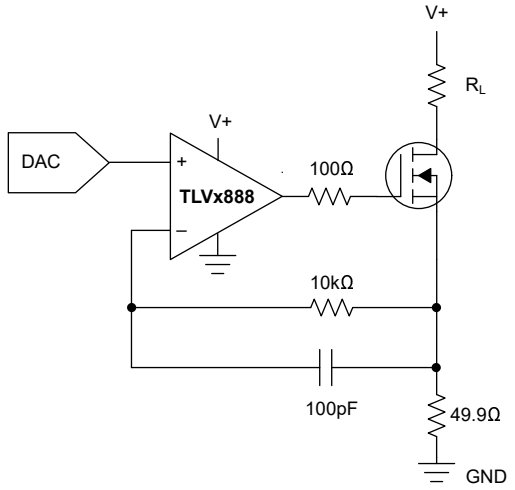



**図 7-6. Programmable, Precision Current Source**

### 7.2.3 Programmable Current Source For A Grounded Load

図 7-7 shows the TLVx888 configured as a programmable current source for a ground referenced load. To achieve single supply operation, a two stage design is employed. The first stage sets a reference current, and the second stage acts as a current mirror with gain. The TLVx888 are used to regulate the current sourced from the transistors in both stages.

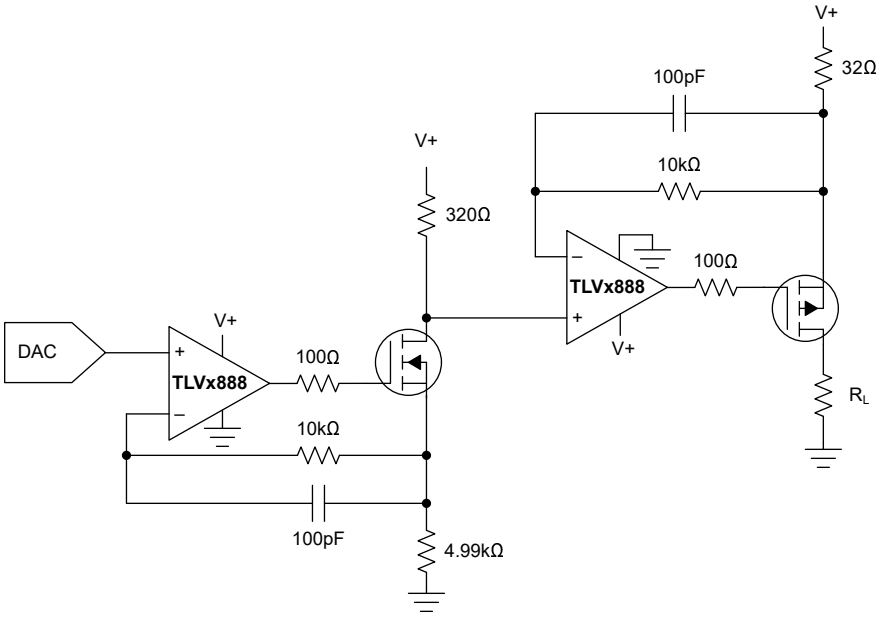



**図 7-7. Single Supply Programmable Current Source For A Ground Referenced Load**

## 7.3 Power Supply Recommendations

The TLVx888 are specified for operation from 4.5V to 36V (±2.25V to ±18V). The TLVx888 operates on both single and dual supplies. The TLVx888 do not require symmetrical supplies; the op amps only require a minimum voltage of 4.5V to operate.

> **注意**
>
> Supply voltages larger than 40V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *セクション 7.4*.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

For best operational performance of the device, use good PCB layout practices:

- For the lowest offset voltage, avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Also:
  - Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
  - Thermally isolate components from power supplies or other heat sources.
  - Shield operational amplifier and input circuitry from air currents, such as cooling fans.
- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see the *The PCB is a component of op amp design* analog application journal.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be separated, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As 図 7-9 shows, keep the feedback resistor (R3) and gain resistor (R4) close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Short traces to the inverting input help to minimize parasitic capacitance on the inverting input. Always remember that the input traces are the most sensitive part of the circuit.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

### 7.4.2 Layout Example

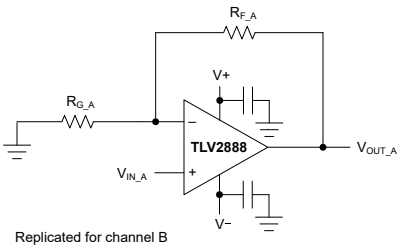



**図 7-8. Schematic Representation**

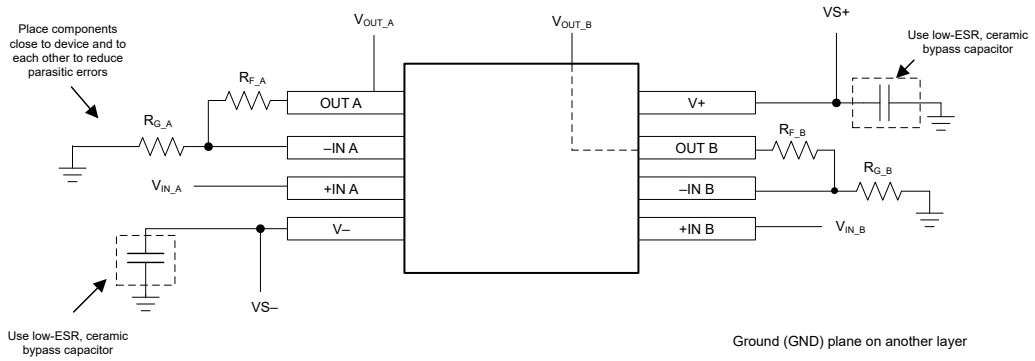



**図 7-9. Operational Amplifier Board Layout for Noninverting Amplifier Configuration**

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

#### 8.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

#### 8.1.1.2 TINA-TI™シミュレーション ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション プログラムです。TINA-TI シミュレーション ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ モデルとアクティブ モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション ソフトウェアは設計およびシミュレーション ツール Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな形式で処理できる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック スタート ツールを作成できます。

**注**

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア フォルダから、無償の TINA-TI シミュレーション ソフトウェアをダウンロードしてください。

## 8.2 Documentation Support

### *8.2.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *Zero-drift Amplifiers: Features and Benefits* application brief
- Texas Instruments, *The PCB is a component of op amp design* application note
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters* application note
- Texas Instruments, *Op Amp Performance Analysis*
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application note
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application note
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application note
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* application note
- Texas Instruments, *TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter*

## 8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 8.4 サポート・リソース

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リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|---|---|---|
| December 2024 | * | Initial Release |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2888DR | ACTIVE | SOIC | D | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL2888 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

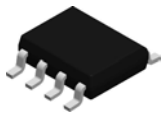
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

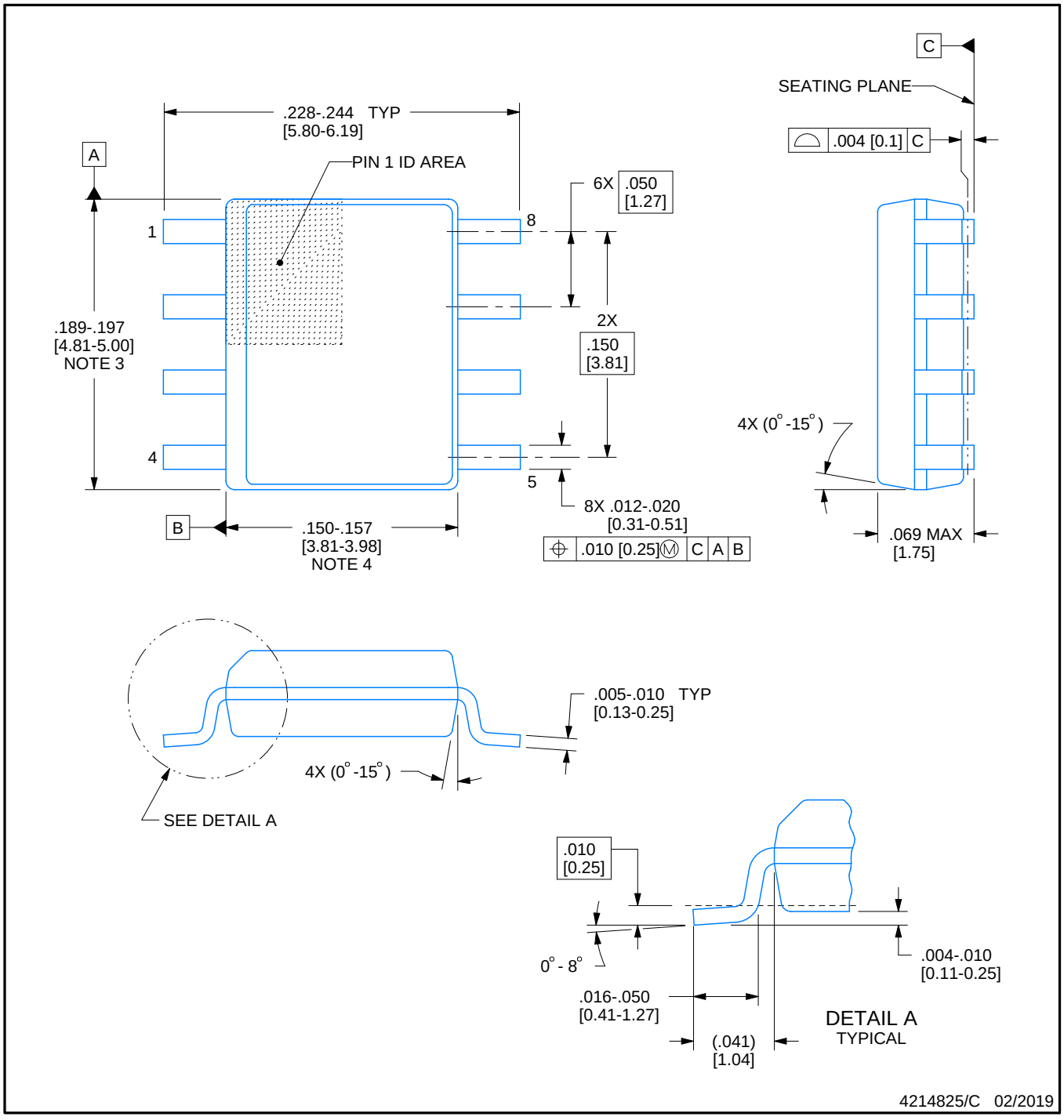


# PACKAGE OUTLINE

## D0008A

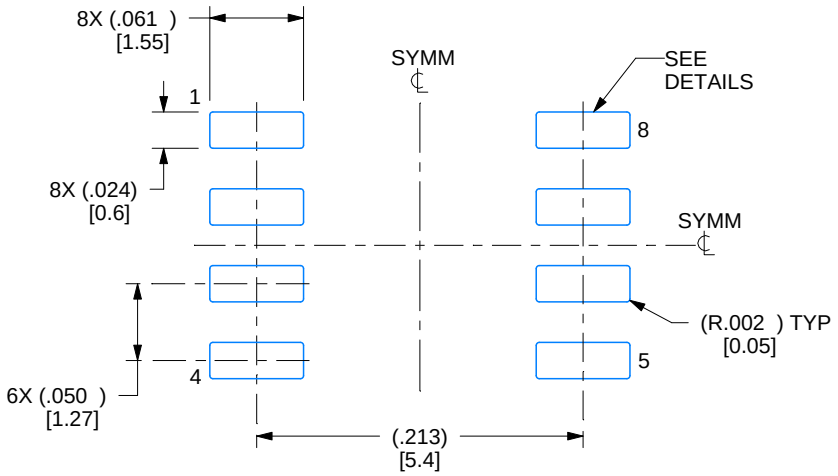
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

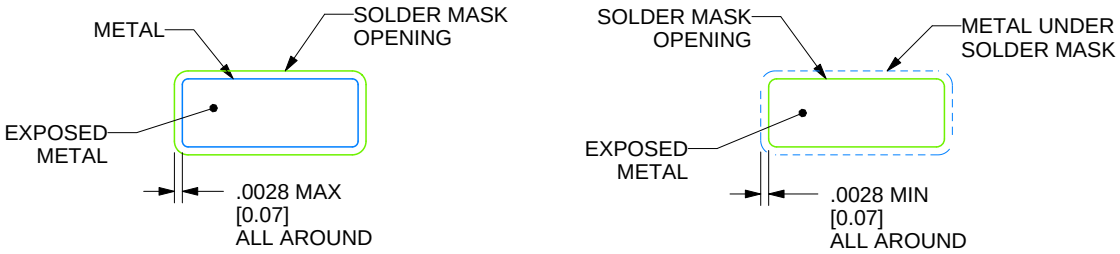



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

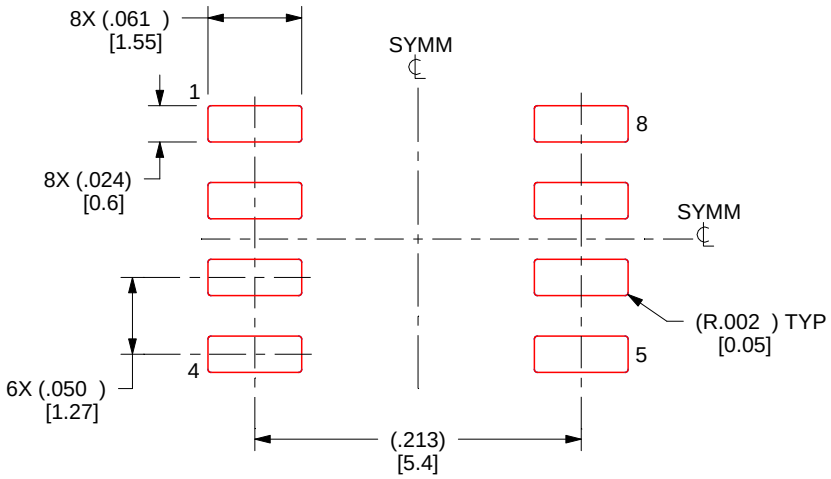
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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