TLV3011-Q1、TLV3012-Q1、TLV3011B-Q1、TLV3012B-Q1 1.24V 基準電圧内蔵低消費電力コンパレータ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～+125℃
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C3
- 低い静止電流:3.1µA (最大値、「B」バージョン)
- 内蔵基準電圧:1.242 V
- 入力同相範囲:レールの 200mV 外まで
- 基準電圧の初期精度:1.5%
- 内蔵ヒステリシス機能:6mV (標準値)
- フェイルセーフ入力 (「B」バージョン)
- パワーオン リセット (「B」バージョン)
- オープンドレイン出力オプション (TLV3011x-Q1)
- プッシュプル出力オプション (TLV3012x-Q1)
- 迅速な応答時間:2µS (「B」バージョン)
- 低い電源電圧:1.65V～5.5V (「B」バージョン)

2 アプリケーション

- 車線離脱警報
- クラスタ
- 有料道路支払い用タグ
- アセットトラッキング
- バッテリ管理システム

3 概要

TLV3011-Q1 は低消費電力オープン ドレイン出力のコンパレータです。TLV3012-Q1 はプッシュプル出力のコンパレータです。どちらのデバイスも、不確定なオンチップ基準電圧を採用しており、静止電流が 5µA (最大値)、電源レールを上回る 200mV 入力同相範囲、1.8V ～ 5.5V の単一電源で動作します。内蔵 1.242V シリーズ基準電圧は、100ppm/℃ (最大値) の低ドリフトを実現し、最大 10nF の容量性負荷で安定しており、最大 0.5mA (標準値) の出力電流を提供できます。

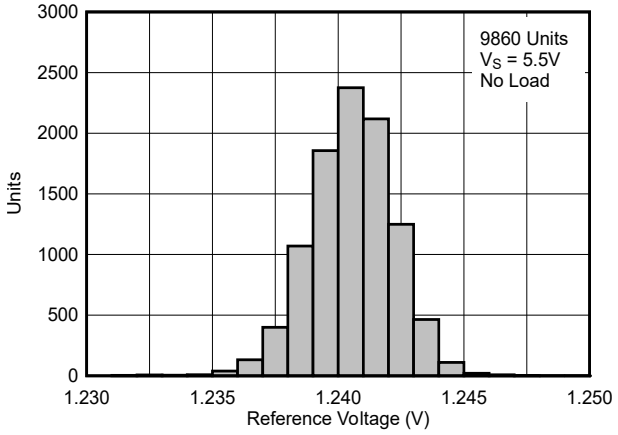
TLV3011B-Q1 および TLV3012B-Q1 の「B」バージョンには、パワー オン リセット (POR)、フェイルセーフ入力、最小電源電圧は 1.65V と低く、最大静止電流は 3.1µA です。

このファミリは、省スペース設計向けの超小型 SOT23-6 パッケージと、基板面積をさらに節約できる SC-70 パッケージで供給されます。どちらのバージョンも、動作温度範囲の仕様は -40℃～+125℃です。

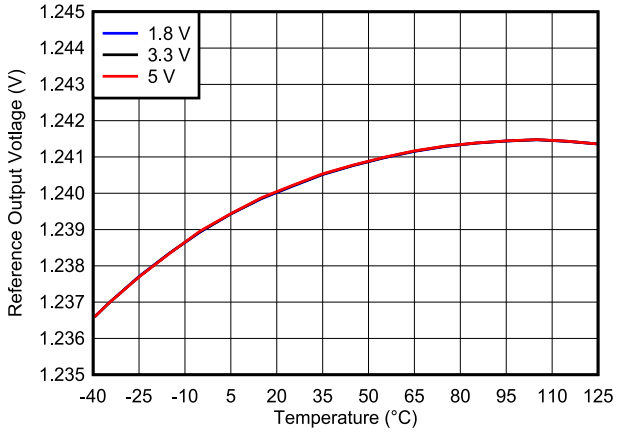
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TLV3011A-Q1、TLV3012A-Q1、TLV3011B-Q1、TLV3012B-Q1	DBV (SOT-23、6)	2.9mm × 2.8mm
	DCK (SC-70、6)	2mm × 2.1mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



TLV3012B-Q1 の基準電圧の分布



TLV3012B-Q1 の基準電圧と温度との関係

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4 Pin Configuration and Functions

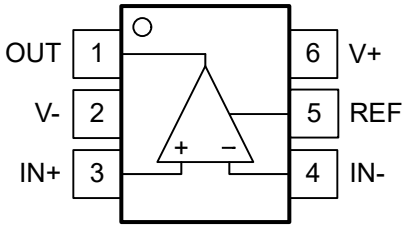


図 4-1. DCK, DBV Package
6-Pin SC-70, SOT-23
Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT	O	Comparator Output
2	V–	-	Negative (lowest) power supply
3	IN+	I	Non-inverting comparator input
4	IN–	I	Inverting comparator input
5	REF	O	Reference Output
6	V+	-	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.5	7	V
Input pins (IN+, IN–) from (V–)(2)	–0.5	7	V
Output (OUT) (Open-Drain) from (V–)(3)	–0.5	7	V
Output (OUT) (Push-Pull) from (V–)	–0.5	(V+) + 0.5	V
Output short circuit current(4)		10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to (V–). Inputs (IN+, IN–) can be greater than (V+) as long as within the –0.5V to 7V range. Inputs beyond –0.3V must be current-limited to less than –10mA, while inputs beyond 7V must be externally voltage clamped.
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as the output is within the –0.5V to 7V range
(4) Short-circuit to (V–) or (V+).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information

THERMAL METRIC(1)		DCK (SC-70)	DBV (SOT-23)	UNIT
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.8	162.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.5	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.9	21.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.0	41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		1.8	5.5	V
Supply voltage: V_S = (V+) – (V–)	B-Versions	1.65	5.5	V
Input voltage range from (V–)		–0.2	(V+) + 0.2	V
Output voltage range from (V–) for open drain		–0.2	(V+)	V
Output voltage range from (V–) for open drain	B-Versions	–0.2	5.5	V
Ambient temperature, T_A		–40	125	°C

5.5 Electrical Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = (V–)	–6	±0.3	6	mV
V_{OS}	Input offset voltage	V_{CM} = (V–) T_A = –40°C to +125°C	–9		9	mV
dV_{IO}/dT	Input offset voltage drift	V_{CM} = (V–) T_A = –40°C to +125°C		±12		µV/°C
PSRR	power supply rejection ratio	V_{CM} = (V–) V_S = 1.8V to 5.5V T_A = –40°C to +125°C		100	1000	µV/V
PSRR	power supply rejection ratio (B-Versions)	V_{CM} = (V–) V_S = 1.65V to 5.5V T_A = –40°C to +125°C		100	1000	µV/V
V_{HYS}	Input hysteresis voltage	T_A = –40°C to +125°C	2	6	8	mV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S /2	–10(1)	±4.5	10(1)	pA
I_{OS}	Input offset current	V_{CM} = V_S /2	–10(1)	±1	10(1)	pA
INPUT COMMON MODE RANGE						
$V_{CM-Range}$	Common-mode voltage range	V_S = 1.8V to 5.5V	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common mode rejection ratio	V_{CM} = (V–) + 1.5V to (V+) + 0.2V V_S = 5.5V	60	74		dB
CMRR	Common mode rejection ratio	V_{CM} = (V–) - 0.2V to (V+) + 0.2V V_S = 5.5V	54	62		dB
R_{CM}	Input Common Mode Resistance			10^{13}		Ω
C_{IC}	Input Common Mode Capacitance			2		pF
INPUT IMPEDANCE						
R_{DM}	Input Differential Mode Resistance			10^{13}		Ω
C_{ID}	Input Differential Mode Capacitance			4		pF
OUTPUT						
V_{OL}	Voltage swing from (V–)	V_S = 5V I_{SINK} = 5mA T_A = –40°C to +125°C		160	200	mV
V_{OH}	Voltage swing from (V+) (for Push-Pull only)	V_S = 5V I_{SOURCE} = 5mA T_A = –40°C to +125°C		90	200	mV
VOLTAGE REFERENCE						
V_{OUT}	Reference Voltage		1.223	1.242	1.260	V
	Accuracy			±0.25%	±1.5%	
dV_{OUT}/d_T	Temperature Drift	T_A = –40°C to +125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load Regulation, Sourcing	0mA < I_{SOURCE} ≤ 0.5mA		0.36	1(1)	mV/mA

5.5 Electrical Characteristics (続き)

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Load Regulation, Sinking	0mA < I_{SINK} ≤ 0.5mA		6.6		mV/mA
ILOAD	Output Current			0.5		mA
dV_{OUT}/dV_S	Line Regulation	1.8V ≤ V_S ≤ 5.5V		10	100(1)	µV/V
dV_{OUT}/dV_S	Line Regulation (B-Versions)	1.65V ≤ V_S ≤ 5.5V		10	100(1)	µV/V
V_{noise}	Noise	f = 0.1Hz to 10Hz		0.2		mV_{PP}
POWER SUPPLY						
I_Q	Quiescent current per comparator	Output is logic high		2.8	5	µA
I_Q	Quiescent current per comparator	Output is logic high T_A = –40°C to +125°C			7	µA
I_Q	Quiescent current per comparator (B-Versions)	Output is logic high		2.4	3.1	µA
I_Q	Quiescent current per comparator (B-Versions)	Output is logic high T_A = –40°C to +125°C			3.6	µA

(1) Verified by characterization

5.6 Switching Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-LH}	Propagation delay time, low-to-high	f = 10kHz, V_{STEP} = 1V, V_{OD} = 10mV, C_L = 10pF		12		µs
T_{PD-LH}	Propagation delay time, low-to-high	f = 10kHz, V_{STEP} = 1V, V_{OD} = 100mV, C_L = 10pF		6		µs
T_{PD-LH}	Propagation delay time, low-to-high (push-pull output, B-Version)	f = 10kHz, V_{STEP} = 200mV, V_{OD} = 100mV, C_L = 10pF		2	4	µs
T_{PD-HL}	Propagation delay time, high-to-low	f = 10kHz, V_{STEP} = 1V, V_{OD} = 10mV, C_L = 10pF		13.5		µs
T_{PD-HL}	Propagation delay time, high-to-low	f = 10kHz, V_{STEP} = 1V, V_{OD} = 100mV, C_L = 10pF		6.5		µs
T_{PD-HL}	Propagation delay time, high-to-low (B-Versions)	f = 10kHz, V_{STEP} = 200mV, V_{OD} = 100mV, C_L = 10pF		2	4	µs
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	C_L = 10pF		100		ns
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output (B-Versions)	C_L = 10pF		10		ns
T_{RISE}	Output Rise Time, 20% to 80%, open-drain output	R_L = 10kΩ, C_L = 10pF		200		ns
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 10pF		100		ns
T_{FALL}	Output Fall Time, 80% to 20% (B-Versions)	C_L = 10pF		10		ns
T_{FALL}	Output Fall Time, 80% to 20%, open-drain output	R_L = 10kΩ, C_L = 10pF		200		ns
T_{FALL}	Output Fall Time, 80% to 20%, open-drain output (B-Versions)	R_L = 10kΩ, C_L = 10pF		10		ns
t_{ON}	Power on-time (B-Versions)			1.9		ms

6 Typical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

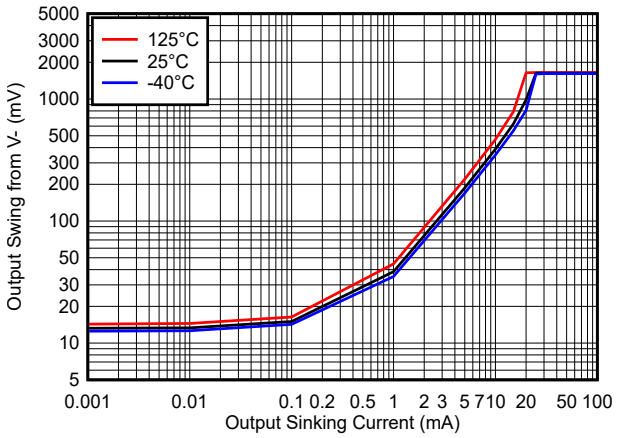


図 6-1. Output Swing vs. Output Sinking Current - 1.8V

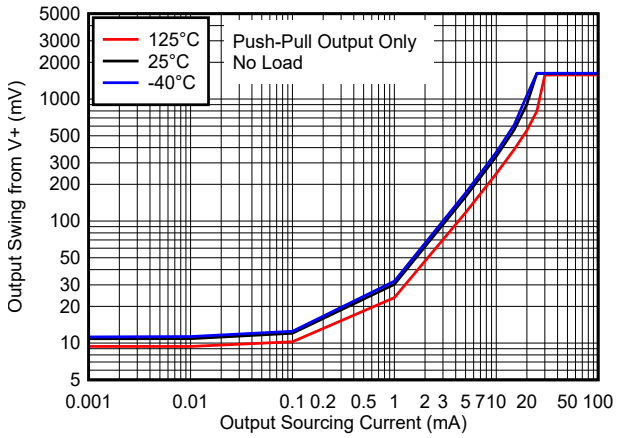


図 6-2. Output Swing vs. Output Sourcing Current - 1.8V

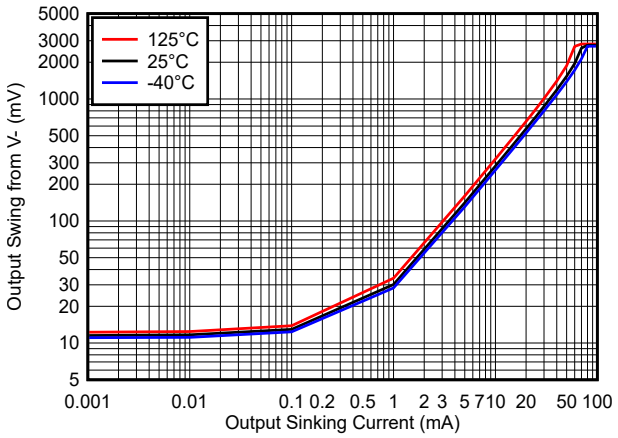


図 6-3. Output Swing vs. Output Sinking Current - 3.3V

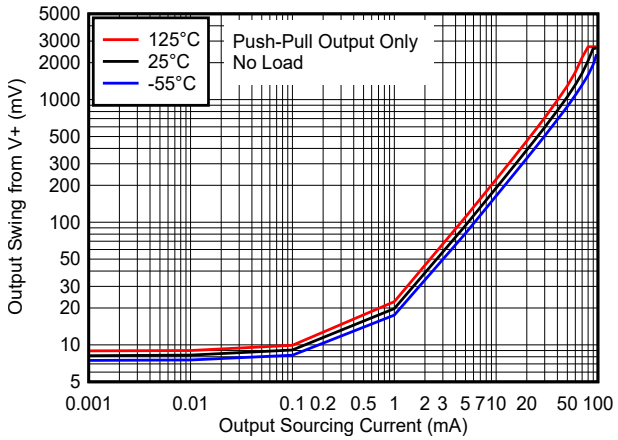


図 6-4. Output Swing vs. Output Sourcing Current - 3.3V

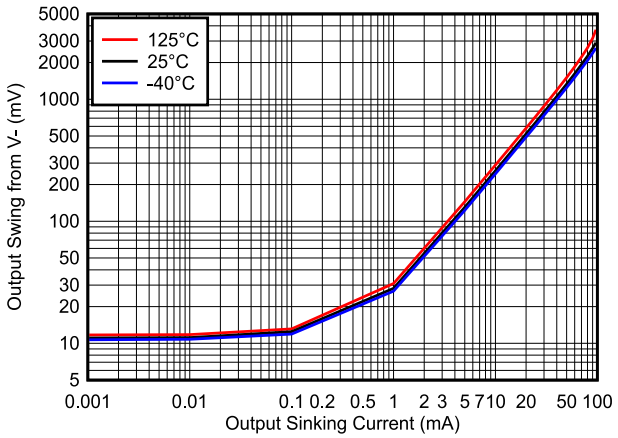


図 6-5. Output Swing vs. Output Sinking Current - 5V

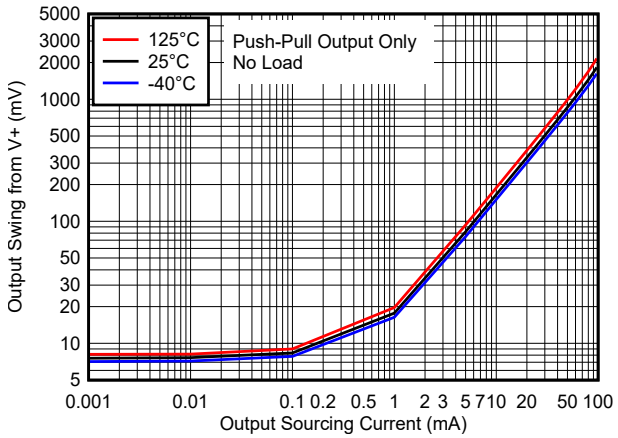


図 6-6. Output Swing vs. Output Sourcing Current - 5V

6 Typical Characteristics (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

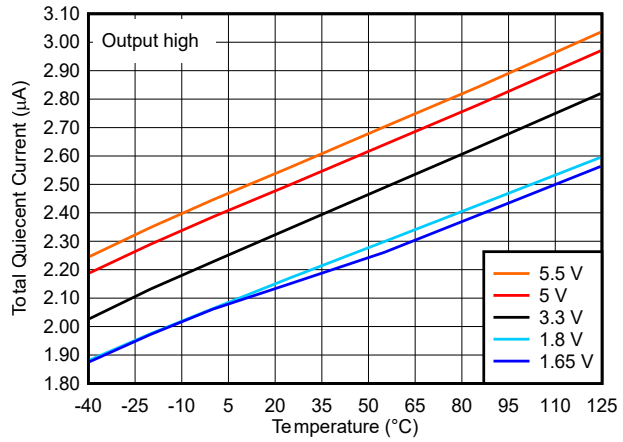


図 6-7. Supply Current vs. Temperature

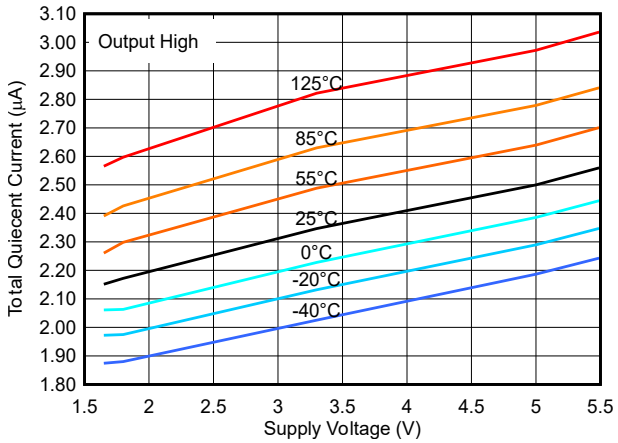


図 6-8. Supply Current vs. Supply Voltage

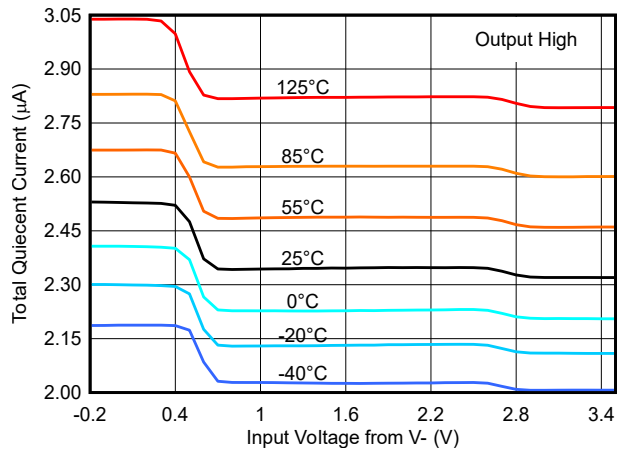


図 6-9. Supply Current vs. Common Mode - 3.3V

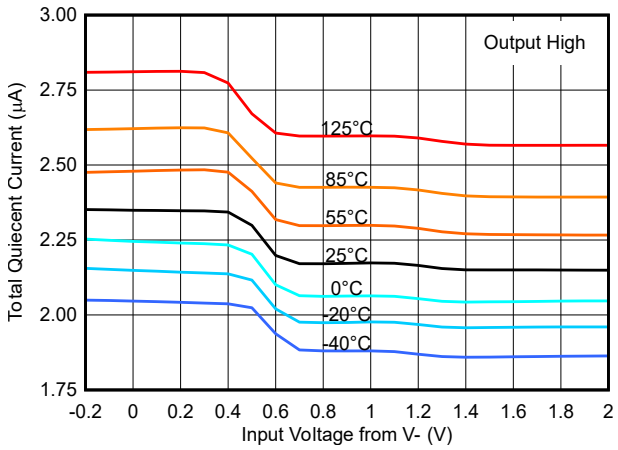


図 6-10. Supply Current vs. Common Mode - 1.8V

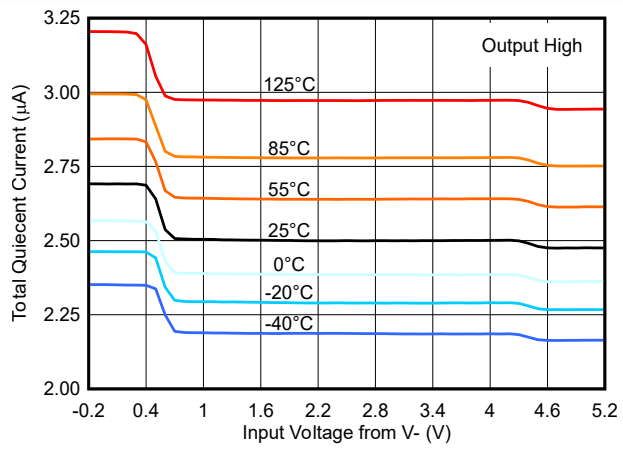


図 6-11. Supply Current vs. Common Mode - 5V

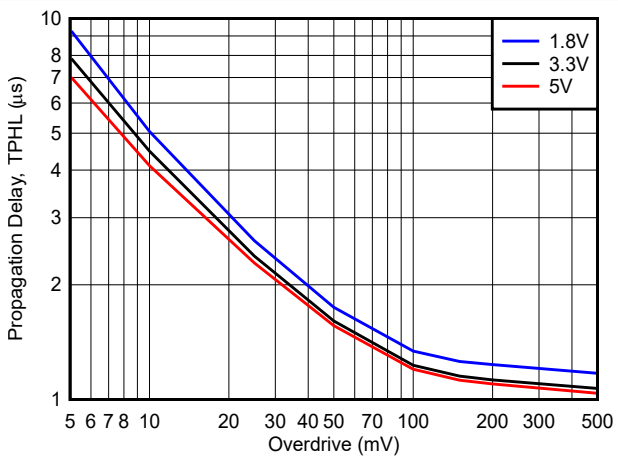


図 6-12. High to Low Propagation Delay vs. Overdrive

6 Typical Characteristics (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

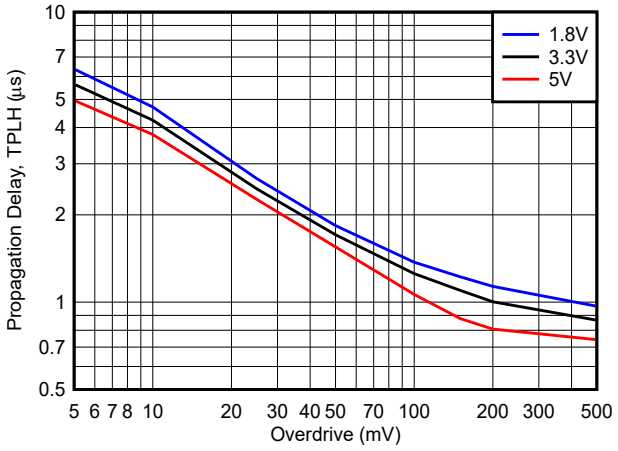


図 6-13. Low to High Propagation Delay vs. Overdrive

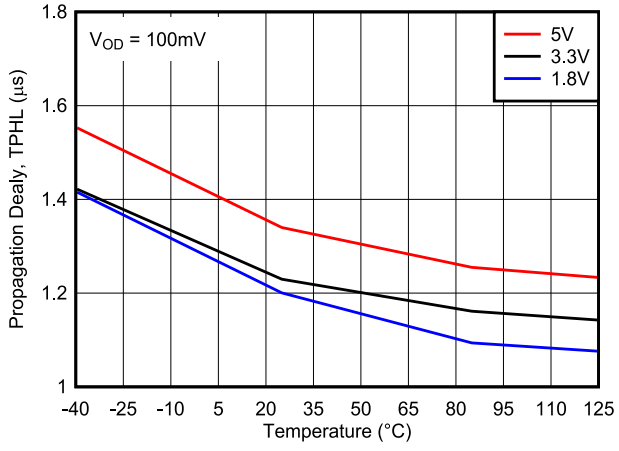


図 6-14. High to Low Propagation Delay vs. Temperature

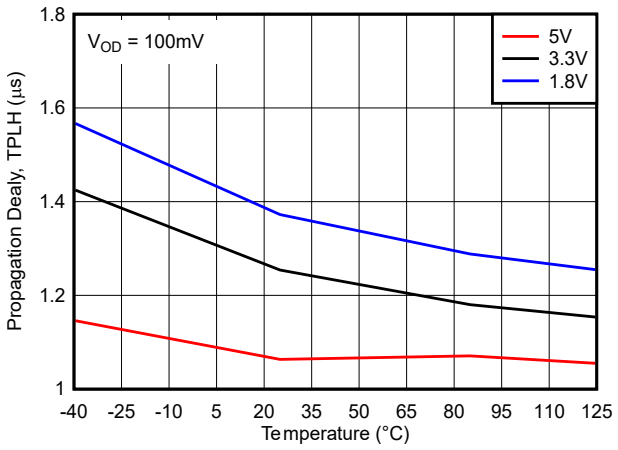


図 6-15. Low to High Propagation Delay vs. Temperature

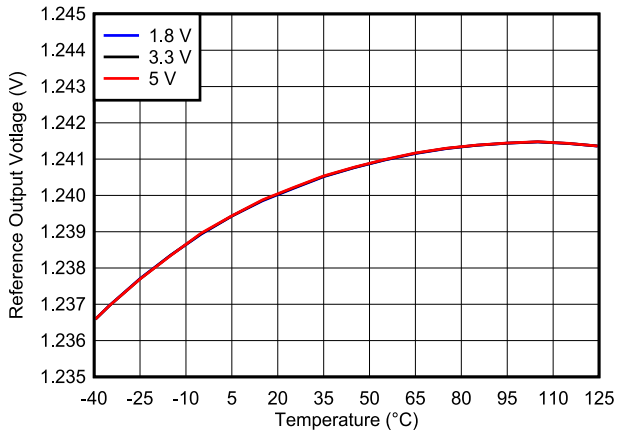


図 6-16. Reference Voltage vs. Temperature

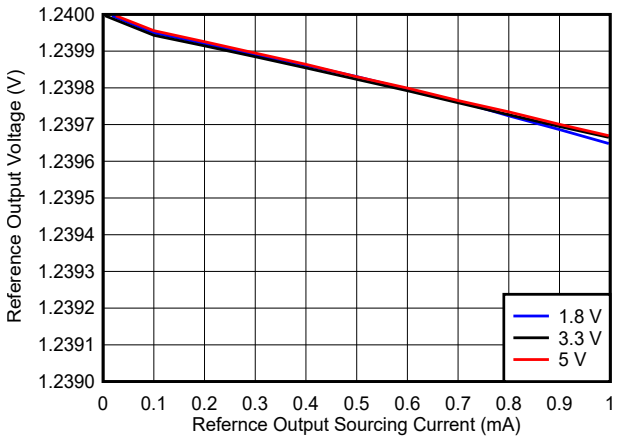


図 6-17. Reference Voltage vs. Reference Output Sourcing Current

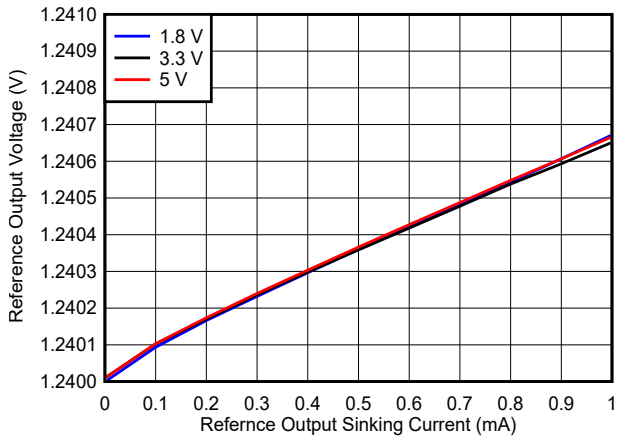


図 6-18. Reference Voltage vs. Reference Output Sinking Current

6 Typical Characteristics (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

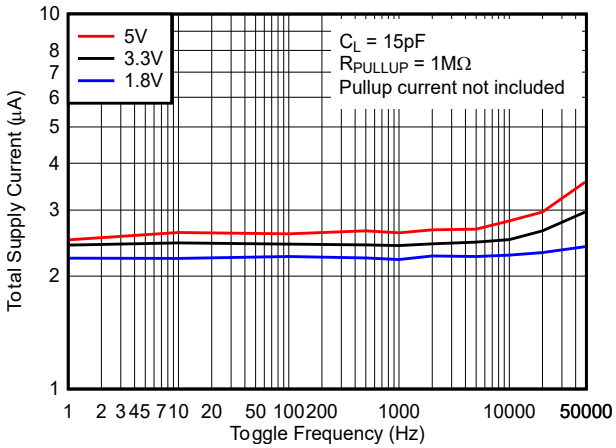


図 6-19. Supply Current vs. Toggle Frequency - Open Drain Output

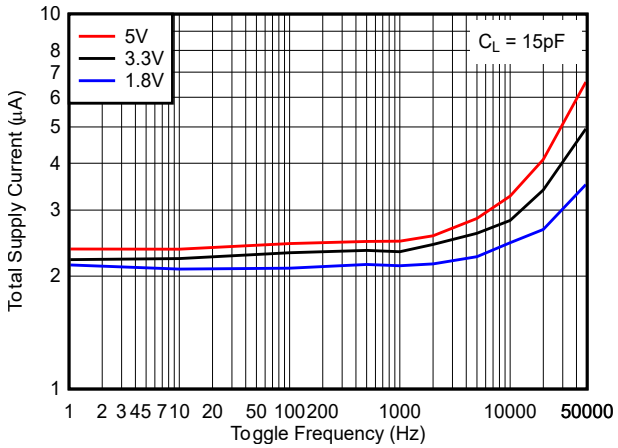


図 6-20. Supply Current vs. Toggle Frequency - Push-Pull Output

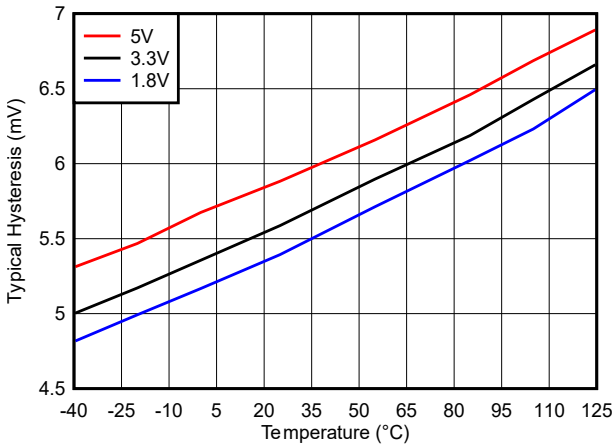


図 6-21. Hysteresis Voltage vs. Temperature

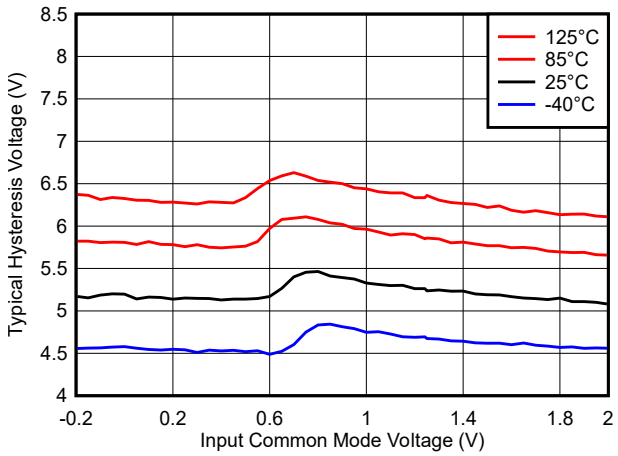


図 6-22. Hysteresis Voltage vs. Common Mode, 1.8V

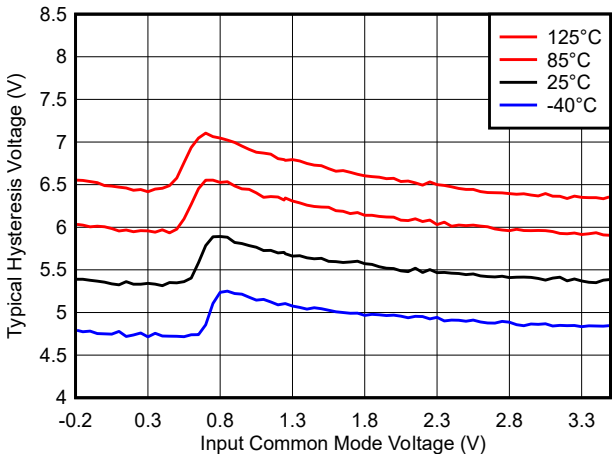


図 6-23. Hysteresis Voltage vs. Common Mode, 3.3V

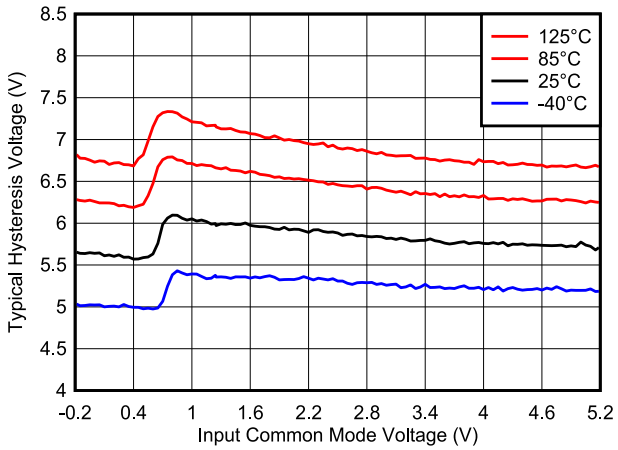


図 6-24. Hysteresis Voltage vs. Common Mode, 5V

6 Typical Characteristics (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

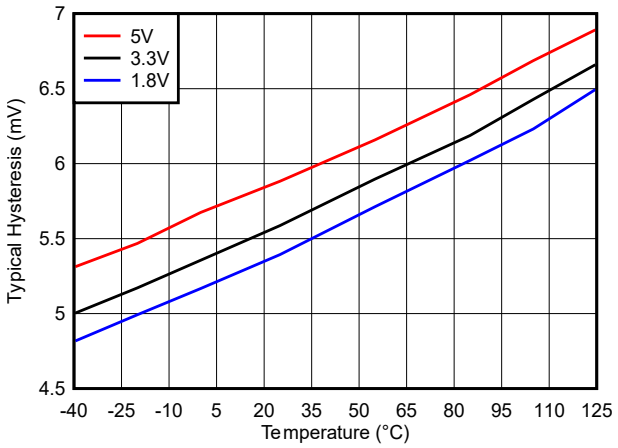


図 6-25. Hysteresis Voltage vs. Supply Voltage

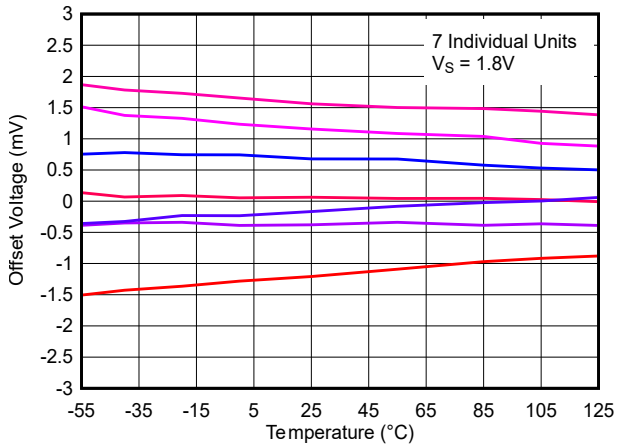


図 6-26. Offset Voltage vs. Temperature, 1.8V

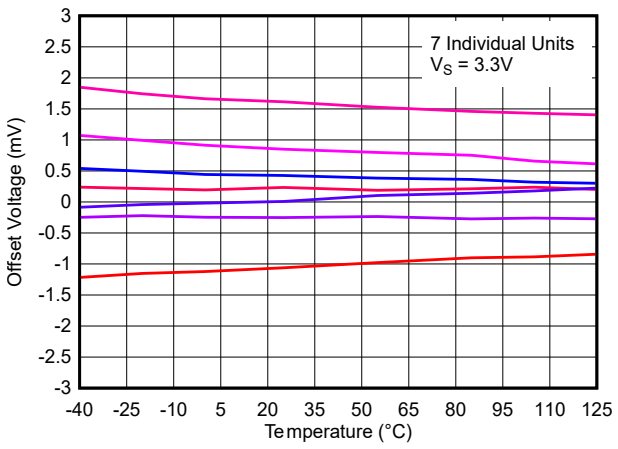


図 6-27. Offset Voltage vs. Temperature, 3.3V

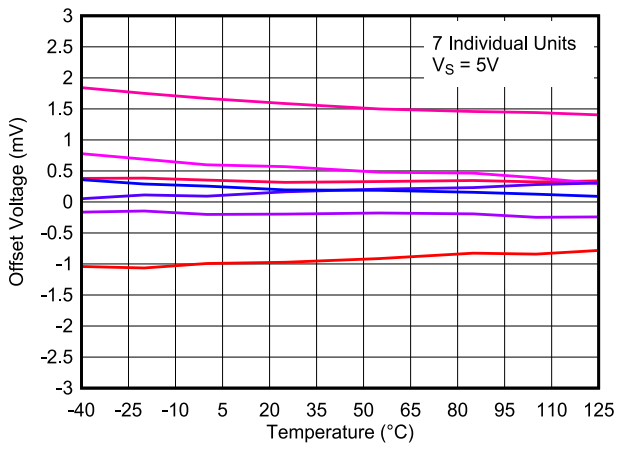


図 6-28. Offset Voltage vs. Temperature, 5V

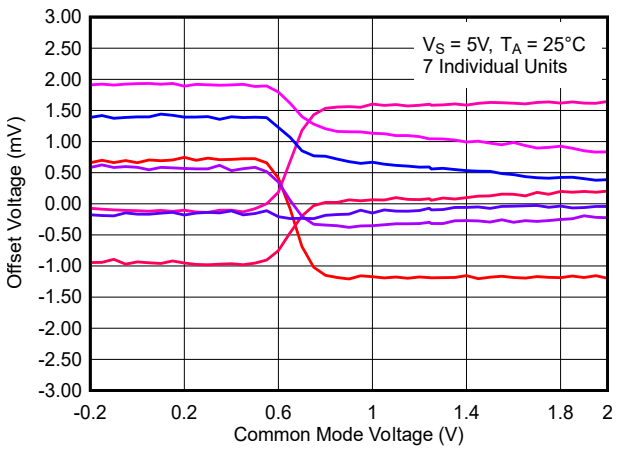


図 6-29. Offset Voltage vs. Common Mode Voltage, 1.8V

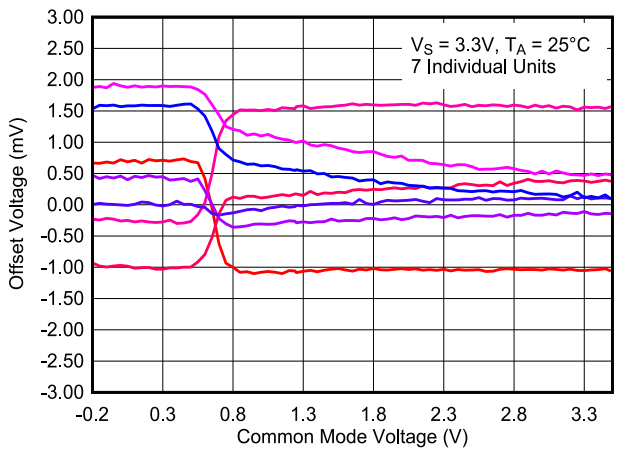


図 6-30. Offset Voltage vs. Common Mode Voltage, 3.3V

6 Typical Characteristics (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

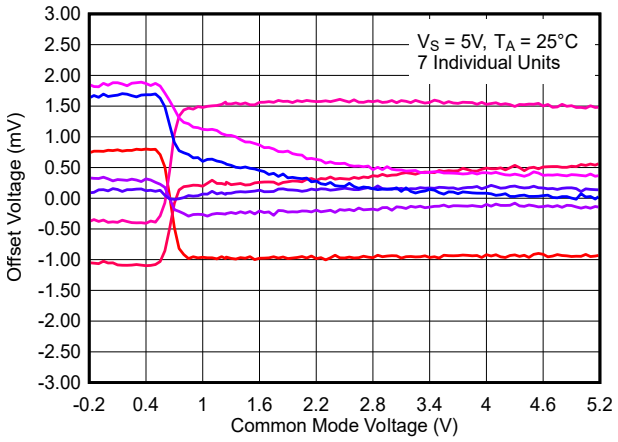


図 6-31. Offset Voltage vs. Common Mode Voltage, 5V

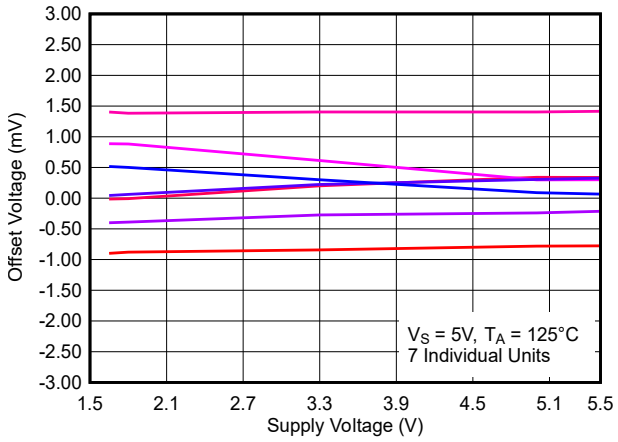


図 6-32. Offset Voltage vs. Supply Voltage, 125°C

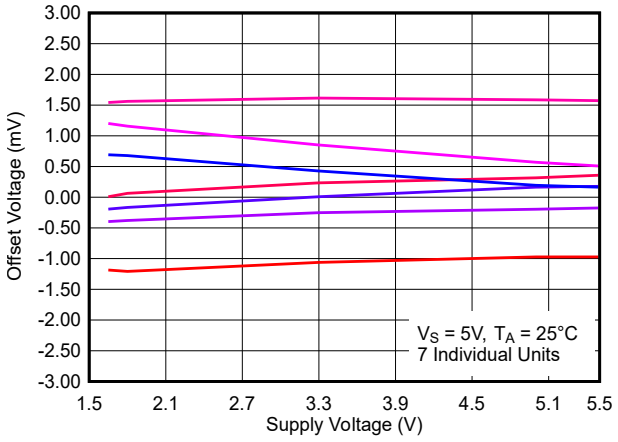


図 6-33. Offset Voltage vs. Supply Voltage, 25°C

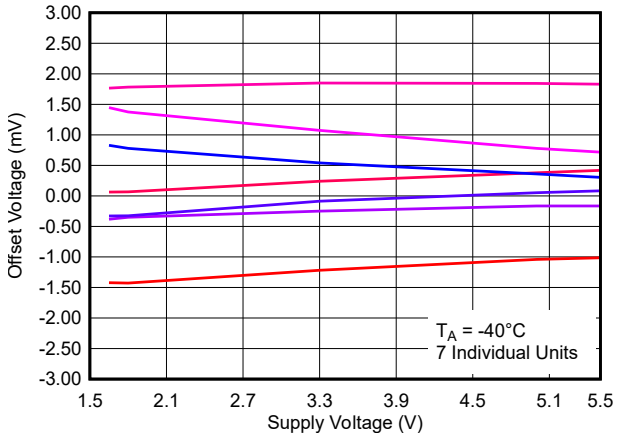


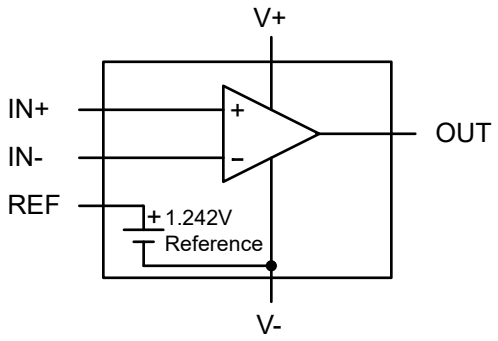
図 6-34. Offset Voltage vs. Supply Voltage, -40°C

7 Detailed Description

7.1 Overview

The TLV301x-Q1 is a MicroPower comparator with an integrated reference that is well suited for compact, low-current, precision voltage detection applications. With a high-accuracy, internal reference of 1.242V and low quiescent current, the TLV301x-Q1 enables power conscious systems to monitor and respond quickly to fault conditions. Throughout this data sheet, rev "B" is only specified when there is a difference.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV301x-Q1 is comprised of a rail-to-rail input comparator with open-drain or push-pull output options and a voltage reference that is externally available.

7.4 Device Functional Modes

The TLV301x-Q1 requires an operating voltage between 1.8V and 5.5V for the comparator output to reflect the voltage applied to the inputs. Similarly, the reference output (REF) is valid over the same operating voltage range. The "B" versions add power on reset, fail-safe inputs and a 1.65V minimum supply voltage.

7.4.1 Open Drain Output (TLV3011-Q1 and TLV3011B-Q1)

The TLV3011-Q1 features an Open-Drain (sinking only) output that allows multiple devices to be driven by a single pull-up resistor to accomplish an OR function, making the TLV3011-Q1 useful for logic applications. The value of the pull-up resistor and supply voltage used affects current consumption due to additional current drawn when the output is in a low state. This effect can be seen in the typical curve Quiescent Current vs Output Switching Frequency.

For the TLV3011-Q1, the pull-up voltage must be less than, or equal to, the V+ supply voltage ($V_{PULLUP} \leq V+$).

The TLV3011B-Q1 output can be pulled-up to any voltage up to 5.5V, regardless of the supply voltage.

7.4.2 Push-Pull Output (TLV3012-Q1 and TLV3012B-Q1)

The TLV3012-Q1 has a "Push-Pull" output capable of both sinking and sourcing current. The push-pull output stage is an excellent choice for reduced power budget applications by eliminating the need for a pull-up resistor and features no shoot-through current. Do not tie push-pull outputs together.

7.4.3 Voltage Reference

The integrated 1.242V voltage reference offers low 100ppm/°C (maximum) drift provided on a seporate output pin that allows use of external dividers or to provide a reference voltage for other external circuitry. The reference is stable with up to a 10nF capacitive load and can sink or source up to 500µA (typical) of output current.

7.4.4 Internal Hysteresis

The TLV301x-Q1 and TLV301xB-Q1 have typically 6mV of built-in hysteresis. External hysteresis can still be added as explained in the section Adding External Hysteresis.

7.4.5 TLV3011B-Q1 and TLV3012B-Q1 Fail-Safe inputs

The TLV3011B-Q1 and TLV3012B-Q1 inputs are Fail-Safe up to 5.5V independent of V+ voltage. Fail-Safe is defined as maintaining the same high input impedance when V+ is unpowered or within the recommended operating ranges.

The Fail-Safe inputs can be any value between 0V and 5.5V, even while V+ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains the value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state is correct.

The following is a summary of the TLV3011B-Q1 and TLV3012B-Q1 device input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output state is **indeterminate** (random). *Do not* operate in this region.

Because the inputs do not have upper ESD diode clamps to V+, input voltages must be externally clamped to below 5.5V if the source can possibly exceed 5.5V. A current limiting resistor in series with the input is also recommend in case of input transients.

7.4.6 TLV3011B-Q1 and TLV3012B-Q1 Power On Reset

The TLV3011B-Q1 and TLV3012B-Q1 have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 1.9ms after the minimum supply voltage threshold is crossed, or immediately when the supply voltage drops below minimum supply. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}). This delay is long enough to allow the reference output to stabilize with up to a 10nF capacitive load.

During the POR period (t_{on}), the outputs are as follows:

- The open drain output TLV3011B-Q1 is high (Hi-Z).
- The push-pull output TLV3012B-Q1 is low (sinking).

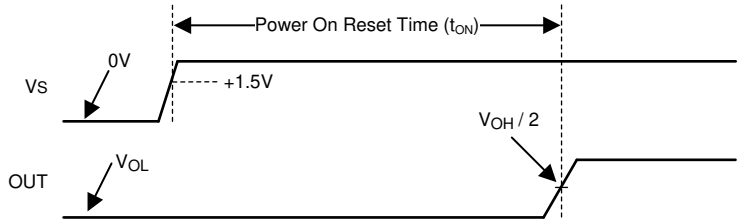


図 7-1. Power-On Reset Example Timing Diagram for Push-Pull Output

Note the nature of an open collector output is that that the output rises with the pull-up voltage during the HI-Z POR period.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV301x-Q1 and TLV301xB-Q1 comparator family with on-chip 1.242V series reference with the choice of either open-drain or push-pull output stages.

A typical supply current of 2.4µA and small packaging combined with 1.65V supply requirements make the TLV301xB-Q1 devices an excellent choice for battery and portable designs.

Shown below are the typical connections for the TLV3012-Q1 device.

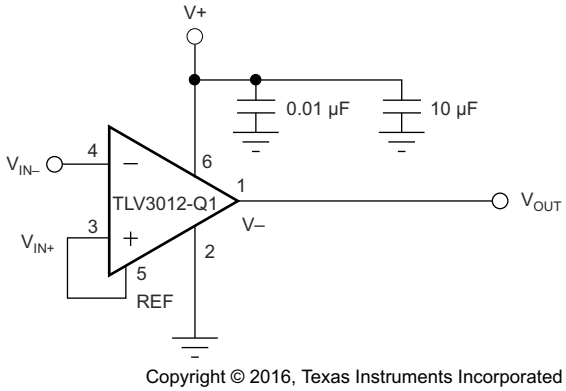


図 8-1. Basic Connections

8.1.1 Adding External Hysteresis

For noisy input signals, the comparator output can display multiple switching as input signals move through the switching threshold. The typical hysteresis of the TLV301x-Q1 family is 6 mV (±3mV). To increase the overall hysteresis, external hysteresis can be added by connecting a small amount of feedback to the positive input. This external hysteresis adds to the internal hysteresis. Shown below is a typical topology used to introduce external hysteresis.

$$V_{HYST} = \frac{V+ \times R1}{R1 + R2} \quad (1)$$

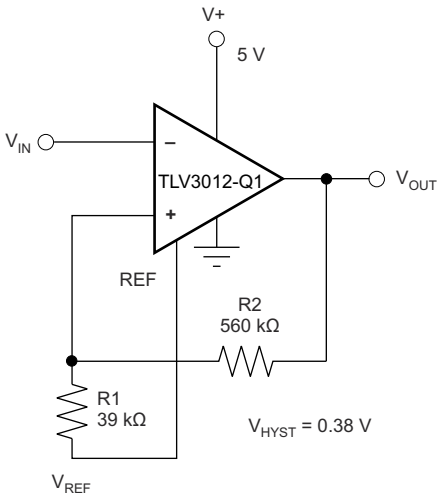


図 8-2. Adding External Hysteresis

The V_{HYST} voltage sets the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

8.2 Typical Application

8.2.1 Under-Voltage Detection

Under-voltage detection is frequently required to alert the system that a battery voltage has dropped below the usable voltage level. Figure 23 shows a simple under-voltage detection circuit using the TLV3012-Q1 which is configured as a non-inverting comparator with the integrated 1.242V reference is externally connected to the inverting input pin (IN-).

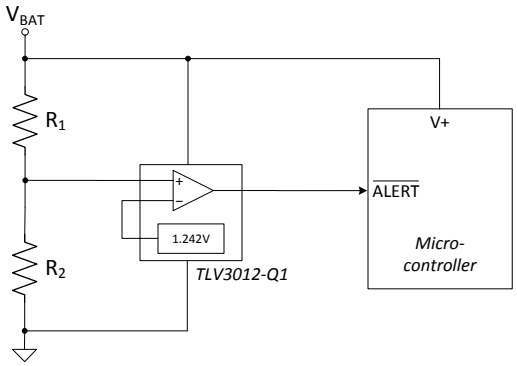


図 8-3. Under-Voltage Detection

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Operate from power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} is less than 2.0V.

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown above. Connect (V+) to V_{BAT} which also powers the microcontroller. Resistors R_1 and R_2 create the under-voltage alert level of 2.0V. When the battery voltage sags down to 2.0V, the resistor divider voltage crosses V_{REF}, the 1.242V reference threshold of the TLV3012-Q1. This causes the comparator

output to transition from a logic high to a logic low. The push-pull output of the TLV3012-Q1 is selected since the comparator operating voltage is shared with the microcontroller which is receiving the under-voltage alert signal.

式 2 is derived from the analysis of 図 8-3.

$$V_{REF} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \tag{2}$$

where

- R_1 and R_2 are the resistor values for the resistor divider connected to IN+
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{REF} is the falling edge threshold where the comparator output changes state from high to low

Rearranging the equation and solving for R_1 yields this result.

$$R_1 = \frac{(V_{BAT} - V_{REF})}{V_{REF}} \times R_2 \tag{3}$$

For the specific undervoltage detection of 2.0V using the TLV3012-Q1, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.242)}{1.242} \times 1M = 610\ k\Omega \tag{4}$$

where

- R_2 is set to 1MΩ
- V_{BAT} is set to 2.0V
- V_{REF} is set to1.242V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at least 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

8.2.1.3 Application Curve

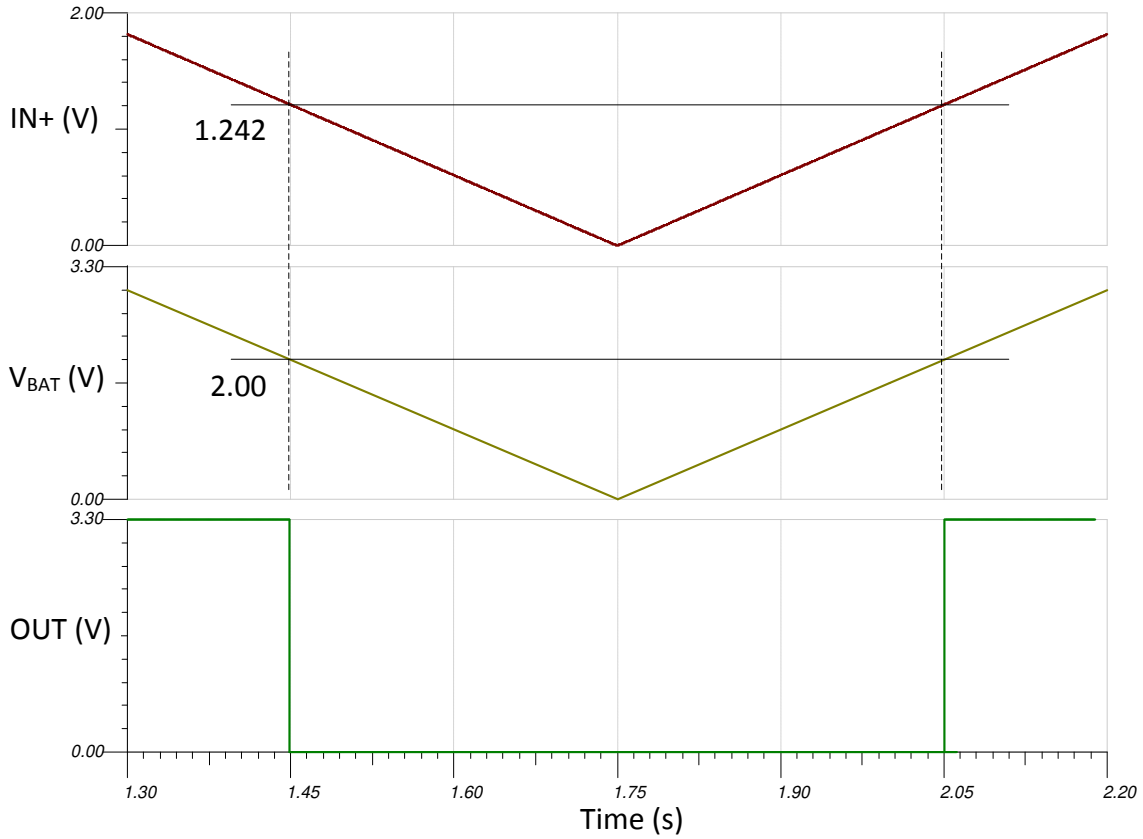


図 8-4.

8.3 System Examples

8.3.1 Power-On Reset

The reset circuit shown below provides a time-delayed release of reset to the MSP430™ microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by the internal voltage reference. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state, releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit does not increase current consumption, because no current flows through the RC circuit after the supply has stabilized.

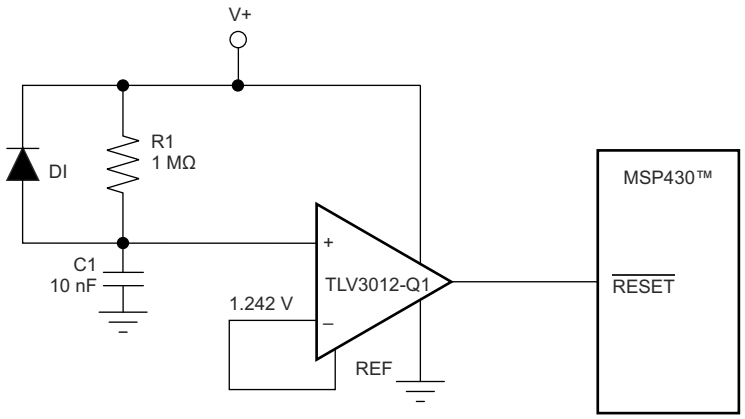


図 8-5. TLV3012-Q1 Configured as Power-Up Reset Circuit for the MSP430™ Microcontroller

The reset delay needed depends on the power-up characteristics of the system power supply. R_1 and C_1 are selected to allow enough time for the power supply to stabilize. D_1 provides rapid reset if power is lost. In this example, the $R_1 \times C_1$ time constant is 10 ms.

8.3.2 Relaxation Oscillator

Shown below, the TLV3012-Q1 device can be configured as a relaxation oscillator to provide a simple and inexpensive clock output. The capacitor is charged at a rate of T = 0.69RC and discharges at a rate of 0.69RC. Therefore, the period is T = 1.38RC. R_1 can be a different value than R_2.

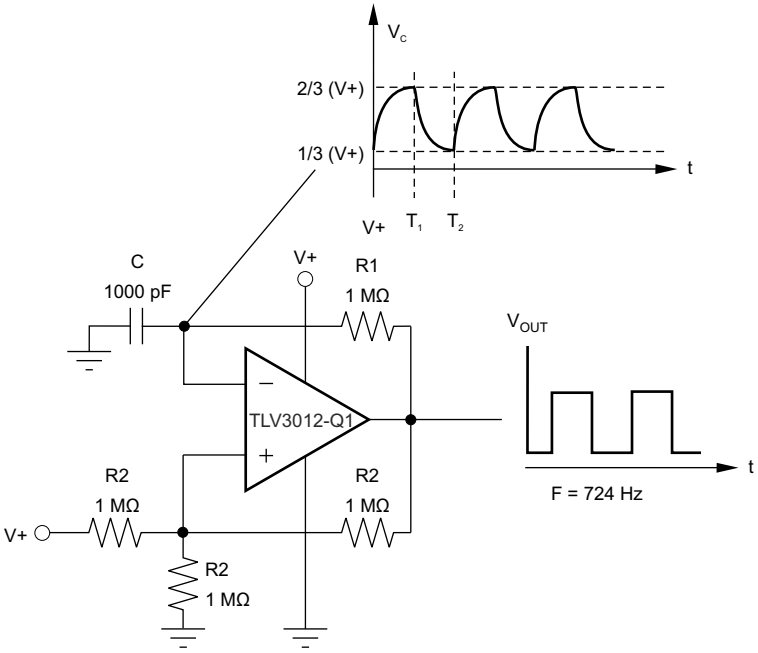


図 8-6. TLV3012-Q1 Configured as Relaxation Oscillator

8.4 Power Supply Recommendations

The TLV3012-Q1 has a recommended operating voltage range (V_S) of 1.8V to 5.5V. V_S is defined as (V+) – (V-). Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5V and 0V and bipolar supply voltages of +2.5V and –2.5V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, realize that the reference (REF) and logic low level of the comparator output is referenced to (V-). Output capacitive loading and output toggle rate causes the average supply current to rise over the quiescent current in the EC Table.

8.5 Layout

8.5.1 Layout Guidelines

To minimize supply noise, power supplies must be capacitively decoupled by a 0.1µF ceramic capacitor. Comparators are sensitive to input noise and precautions such as proper grounding (use of ground plane), supply bypassing, and guarding of high-impedance nodes minimize the effects of noise and help specified performance.

8.5.2 Layout Example

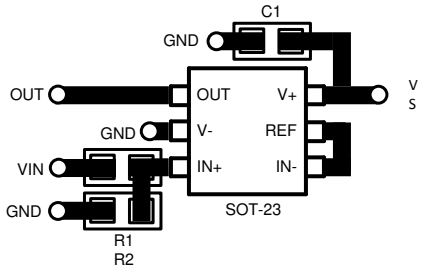


図 8-7. Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (April 2023) to Revision D (January 2025)	Page
• *TLV3012-Q1 DCK パッケージのみの絶対最大値表*を削除しました（1 つの表に結合）	1
• *TLV3012-Q1 DCK パッケージのみの熱に関する情報表*を削除しました（1 つの表に結合）	1
• *TLV3012-Q1 DCK パッケージのみの電気的特性表*を削除しました（1 つの表に結合）	1
• *TLV3012-Q1 DCK パッケージのみのスイッチング特性表*を削除しました（1 つの表に結合）	1
• *TLV3012-Q1 DCK パッケージのみの代表的特性*の曲線を削除しました	1
• フロント ページにある*製品情報表*のタイトルを*パッケージ情報*に変更	1
• Updated Supply Current Graphs	8

Changes from Revision B (August 2022) to Revision C (April 2023)	Page
• 先頭ページのテキストと表に TLV3011B-Q1 と TLV3012B-Q1 を追加。	1

Changes from Revision A (June 2019) to Revision B (August 2022)	Page
• DBV パッケージと DCK パッケージの両方に TLV3011-Q1 を追加	1
• SOT-23 (DBV) に TLV3012-Q1 を追加	1

- DBV パッケージの新しい表を追加 1
- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1

Changes from Revision * (March 2011) to Revision A (June 2019) **Page**

- HBM と CDM の ESD 定格および分類レベルを追加。AEC-Q100 デバイスの温度グレードも追加 1
- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- データシートから TLV3011-Q1 デバイスを削除し、TLV3012-Q1 の部品番号から A を削除 1
- Deleted the *Package Ordering Information* section 3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3011AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q7F	Samples
TLV3011AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1M6	Samples
TLV3011BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31IF	Samples
TLV3011BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1O6	Samples
TLV3012AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q8F	Samples
TLV3012AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPF	Samples
TLV3012BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31JF	Samples
TLV3012BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1O7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV3011-Q1, TLV3011B-Q1, TLV3012-Q1, TLV3012B-Q1 :

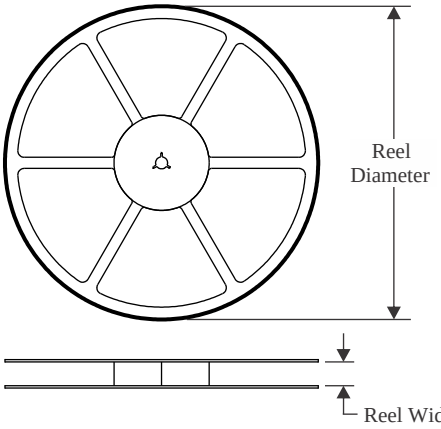
- Catalog : TLV3011, TLV3011B, TLV3012, TLV3012B
- Enhanced Product : TLV3011-EP, TLV3012-EP

NOTE: Qualified Version Definitions:

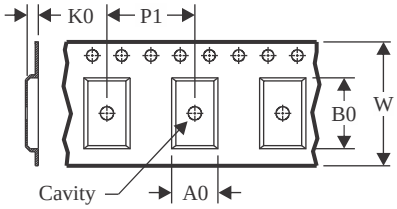
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

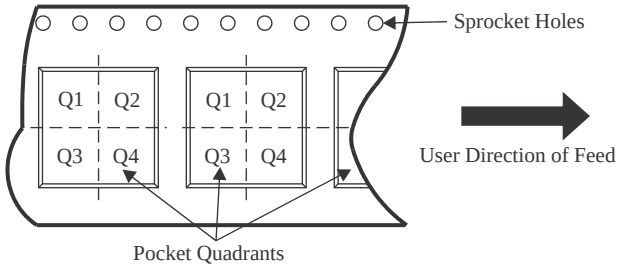


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

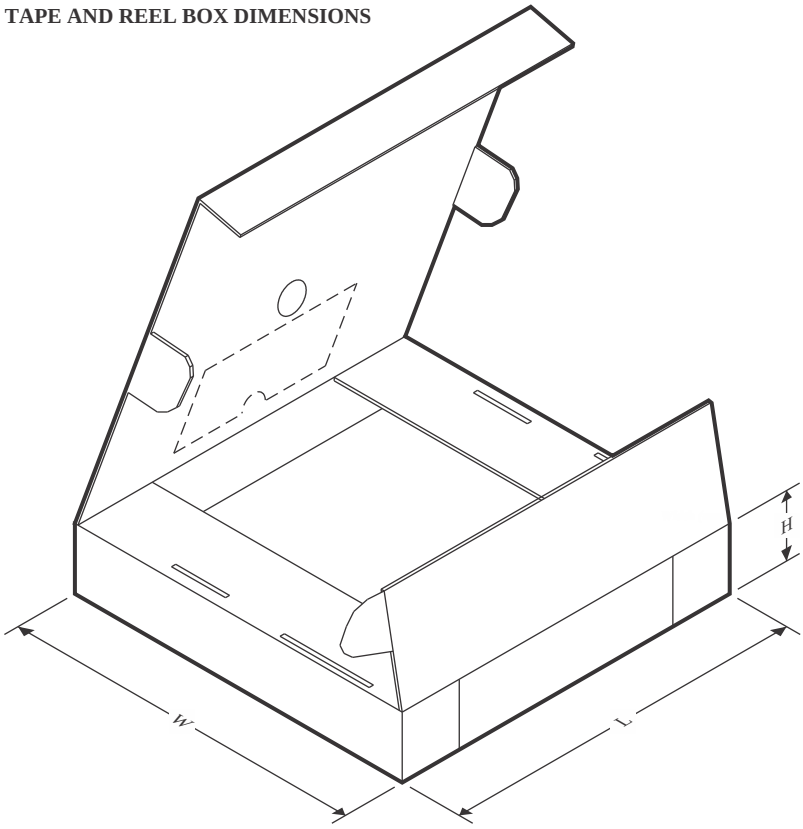
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3011AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3011AQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3011BQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3011BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3012AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3012AQDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV3012AQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3012BQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3012BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

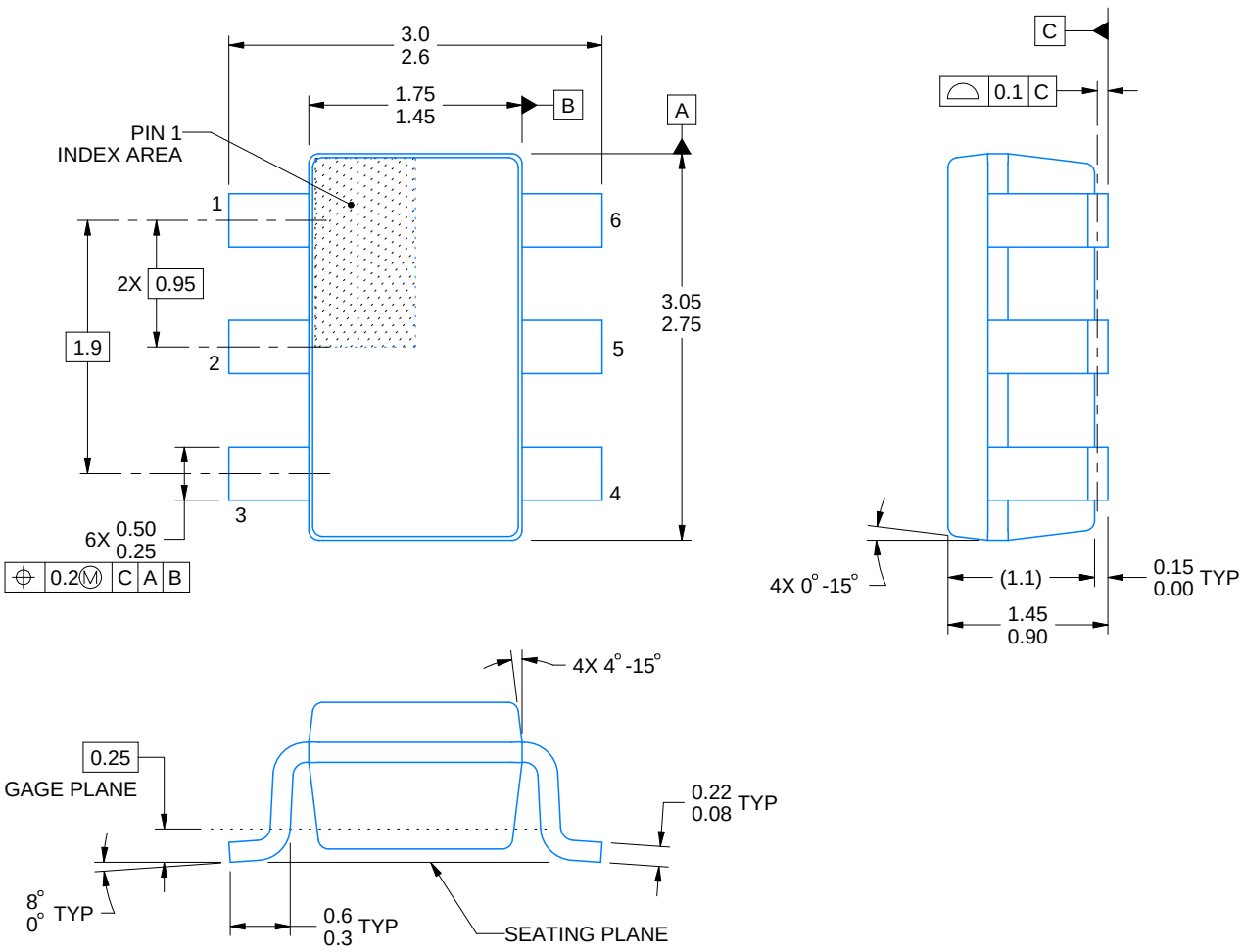
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3011AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3011AQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3011BQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3011BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3012AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3012AQDCKRQ1	SC70	DCK	6	3000	200.0	183.0	25.0
TLV3012AQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3012BQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3012BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

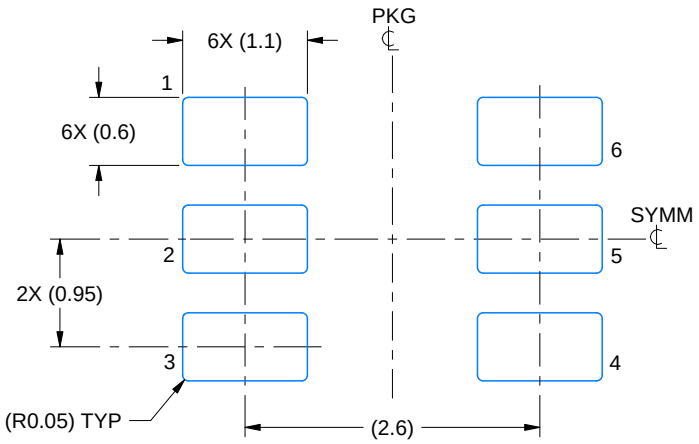
SMALL OUTLINE TRANSISTOR



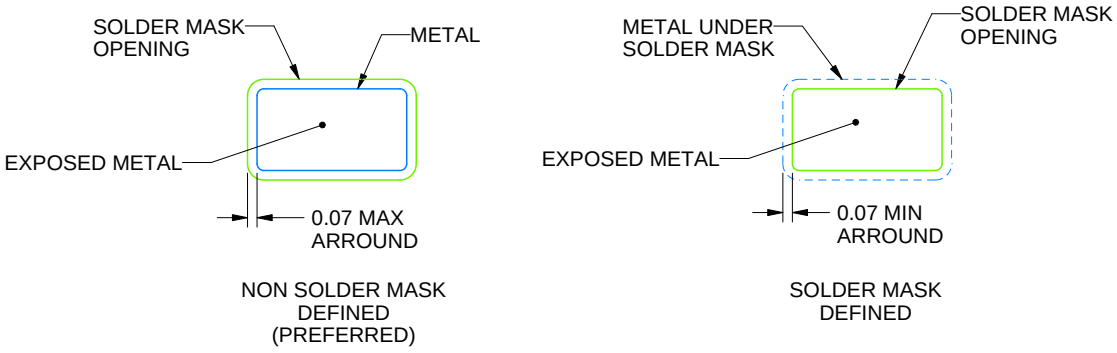
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

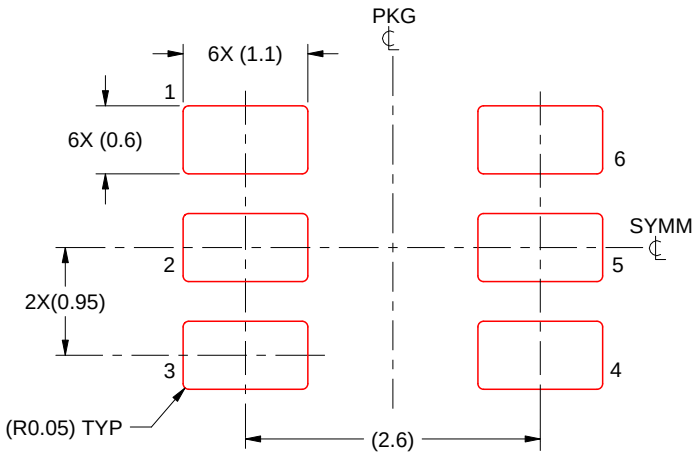


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

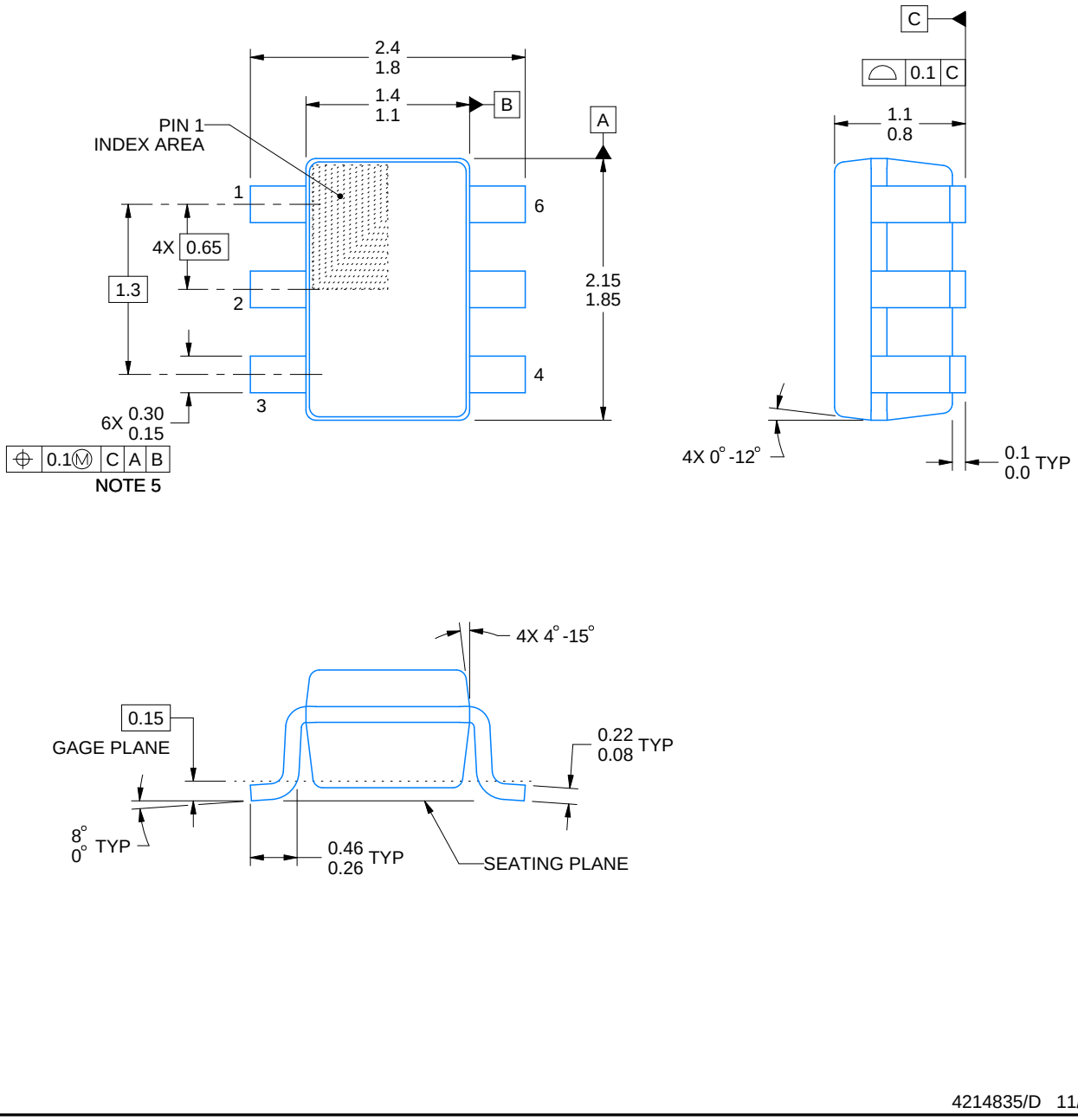
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

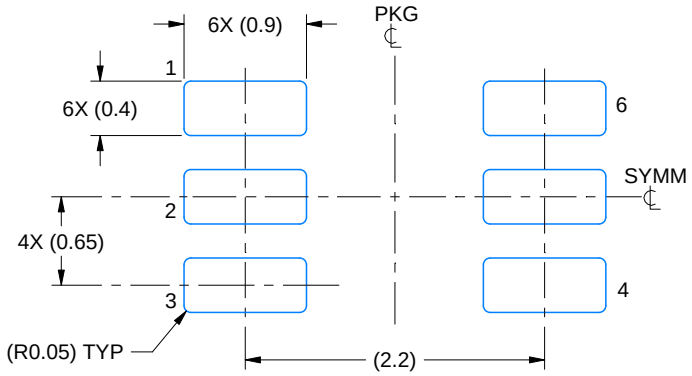
SMALL OUTLINE TRANSISTOR



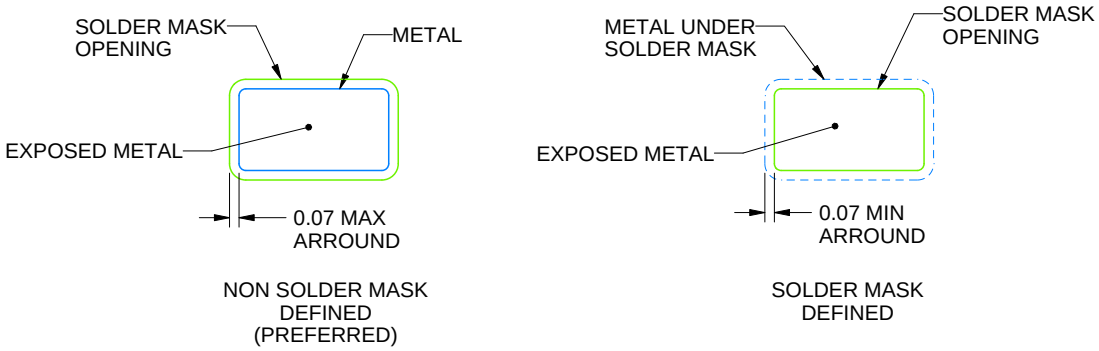
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

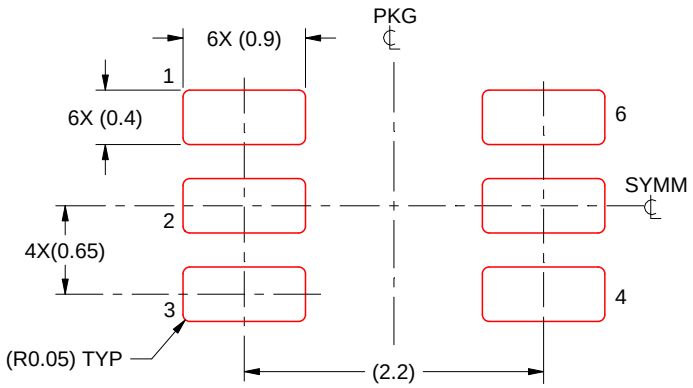


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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