TLV320AIC3106 低消費電力ステレオ・オーディオ・コーデック、ポータブル・オーディオ / 携帯電話用

1 特長

- ステレオ・オーディオ DAC:
  - 信号対雑音比:102dBA
  - 16、20、24、32 ビットのデータ
  - 8kHz~96kHz のサンプル・レートに対応
  - 3D、バス、トレブル、EQ、ディエンファシスのエフェクト
  - 柔軟な省電力モードと性能が利用可能
- ステレオ・オーディオ ADC:
  - 信号対雑音比:92dBA
  - 8kHz~96kHz のサンプル・レートに対応
  - 録音時にデジタル信号処理とノイズ・フィルタリングが利用可能
- 10 本のオーディオ入力ピン:
  - シングルエンドまたは完全差動構成にプログラム可能
  - 3 ステート機能によるフローティング入力構成
- 7 つのオーディオ出力ドライバ:
  - ステレオの完全差動またはシングルエンド・ヘッドフォン・ドライバ
  - 完全差動ステレオ・ライン出力
  - 完全差動モノラル出力
- 低消費電力:15mW (ステレオ、48kHz 再生、3.3V アナログ電源)
- 超低消費電力モード、パッシブ・アナログ・バイパス付
- 入出力アナログ・ゲインをプログラム可能
- 録音時の自動ゲイン制御 (AGC)
- プログラム可能なマイクロフォン・バイアス・レベル
- プログラム可能な PLL による柔軟なクロック生成
- SPI または I²C を選択可能な制御バス
- オーディオ・シリアル・データ・バスは I²S、左揃えおよび右揃え、DSP、TDM モードをサポート
- 代替シリアル PCM 、I²S データ・バスにより Bluetooth™ モジュールへ簡単に接続可能
- デジタル・マイクとアナログ・マイクの同時サポートが利用可能
- 包括的なモジュール型電源制御
- 電源:
  - アナログ:2.7V~3.6V
  - デジタル・コア:1.65V~1.95V
  - デジタル I/O:1.1V~3.6V
- パッケージ:5.00mm × 5.00mm 80 ピン VFBGA、7.00mm × 7.00mm 48 ピン VQFN

2 アプリケーション

- デジタル・カメラ
- スマートフォン

3 概要

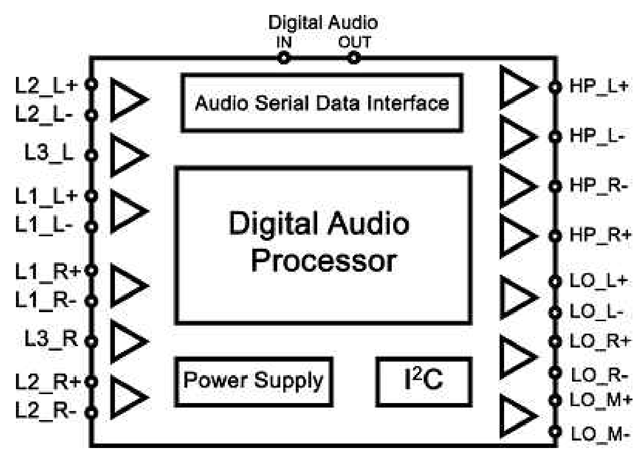
TLV320AIC3106 は、ステレオ・ヘッドホン・アンプを内蔵した低消費電力ステレオ・オーディオ・コーデックであり、シングル・エンドまたは完全差動構成でプログラマブルな複数の入力と出力を備えています。レジスタ・ベースの包括的な電源制御機能が搭載されており、3.3V のアナログ電源から 15mW のステレオ 48kHz DAC 再生が可能なため、携帯用のバッテリ駆動オーディオおよびテレフォニー・アプリケーションに最適です。

TLV320AIC3106 の録音パスには、内蔵マイクロフォン・バイアス、デジタル制御のステレオ・マイク・プリアンプ、自動ゲイン制御 (AGC) が含まれており、複数のアナログ入力の間に MIX および MUX 機能があります。録音時にプログラム可能なフィルタを使用できるため、デジタルカメラの光学ズーム中に発生する可聴ノイズを除去できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TLV320AIC3106	BGA MICROSTAR JUNIOR (80)	5.00mm × 5.00mm
	VQFN (48)	7.00mm × 7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (December 2014) to Revision G (July 2021) **Page**

- *文書全体にわたって表、図、相互参照の採番方法を更新*....1
- ドキュメント全体を通して QFN を VQFN に変更....1
- *アプリケーションセクションにリンクを追加*....1

Changes from Revision E (December 2008) to Revision F (December 2014) **Page**

- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクションを追加。. 1

5 概要 (続き)

再生パスには MIX および MUX 機能があり、ステレオ DAC および選択した入力から、プログラム可能なボリューム制御を介して各種の出力が可能です。

TLV320AIC3106 には、4 つの大電力出力ドライバと 3 つの完全差動出力ドライバが内蔵されています。大電力出力ドライバは、AC カップリング・コンデンサを使用した最大 4 チャネルのシングルエンド 16Ω ヘッドホン、あるいはコンデンサレス出力構成のステレオ 16Ω ヘッドホンなど、さまざまな負荷構成を駆動できます。

ステレオ・オーディオ DAC は 8kHz ~ 96kHz のサンプリング・レートをサポートし、DAC パスにプログラマブル・デジタル・フィルタを備えており、3D、低音、高音、ミッドレンジ・エフェクト、スピーカ・イコライゼーション、32kHz、44.1kHz、48kHz の各レートでのディエンファシスを実現します。ステレオ・オーディオ ADC は、8kHz ~ 96kHz のサンプリング・レートをサポートし、前段にプログラマブル・ゲイン・アンプまたは AGC が搭載され、低レベルのマイク入力に対して最大 59.5dB のアナログ・ゲインを実現します。TLV320AIC3106 は、アタック (8ms～1,408ms) とディケイ (0.05 秒 ~ 22.4 秒) の両方に対して非常に広範囲にわたるプログラマビリティを実現します。AGC 範囲が広いので、AGC を多くの種類のアプリケーションに合わせてチューニングできます。

アナログ信号処理とデジタル信号処理のどちらも必要ないバッテリ節約アプリケーションでは、デバイスを特別なアナログ信号パススルー・モードに設定できます。このモードでは、パススルー動作中にほとんどのデバイスがパワーダウンするため、消費電力が大幅に削減されます。

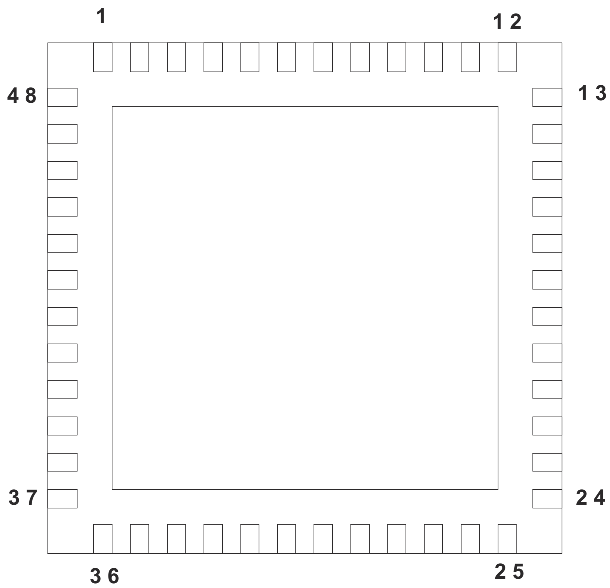
シリアル制御バスは SPI または I^2C プロトコルをサポートし、シリアル・オーディオ・データ・バスは I^2S、左 / 右揃え、DSP または TDM モードにプログラムできます。高度にプログラム可能な PLL が内蔵されており、柔軟なクロック生成ができ、512kHz～50MHz の広い範囲の MCLK から標準的なオーディオ速度のすべてをサポートしています。これには最も一般的な 12MHz、13MHz、16MHz、19.2MHz、19.68MHz のシステム・クロックが含まれるように特に注意を払っています。

TLV320AIC3106 は、2.7V~3.6V のアナログ電源、1.65V~1.95V のデジタル・コア電源、1.1V~3.6V のデジタル I/O 電源で動作します。このデバイスは 5mm × 5mm、80 ボールの MicroStar Junior™ BGA パッケージと、7mm × 7mm、48 ピンの QFN パッケージで供給されます。

6 Device Comparison Table

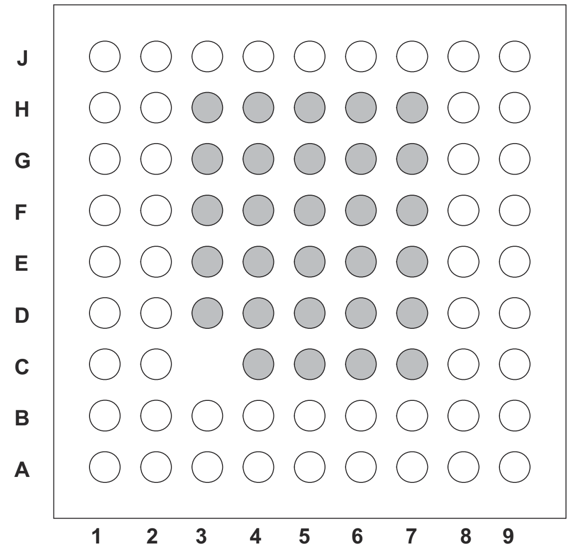
DEVICE NAME	DESCRIPTION
TLV320AIC3106	Low-Power Stereo CODEC with 10 Inputs, 7 Outputs, Speaker/HP Amp and Enhanced Digital Effects.
TLV320AIC3101	Same as TLV320AIC3106, but with 6 inputs, 6 outputs and Speaker/HP Amp.
TLV320AIC3104	Same as TLV320AIC3106, but with 6 inputs and 6 outputs.
TLV320AIC3105	Same as TLV320AIC3106, but with 6 Single-ended inputs and 6 outputs.
TLV320AIC3107	Same as TLV320AIC3106, but with 7 Inputs, 6 Outputs and Integrated Mono Class-D Amplifier.

7 Pin Configuration and Functions



Solder the VQFN thermal pad to the ground plane (DRVSS).

図 7-1. RGZ Package, 48-Pin VQFN, Bottom View



The shaded balls are not connected to the die, but are electrically connected to each other. Is recommended to solder them to analog ground in order to enhance the thermal performance of the device.

図 7-2. ZQE Package, 80-Ball BGA Microstar Junior, Bottom View

表 7-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	VQFN	BGA BALL		
MICBIAS	13	A2	O	Microphone bias voltage output
MIC3R	14	A1	I	MIC3 input (right or multifunction)
AVSS_ADC	15	C2,D2	–	Analog ADC ground supply, 0 V
DRVDD	16,17	B1,C1	–	ADC analog and output driver voltage supply, 2.7 V–3.6 V
HPLOUT	18	D1	O	High-power output driver (left +)
HPLCOM	19	E1	O	High-power output driver (left – or multifunctional)
DRVSS	20,21	E2,F2	–	Analog output driver ground supply, 0 V
HPRCOM	22	F1	O	High-power output driver (right – or multifunctional)
HPROUT	23	G1	O	High-power output driver (right +)
DRVDD	24	H1	–	ADC analog and output driver voltage supply, 2.7 V–3.6 V
AVDD_DAC	25	J1	–	Analog DAC voltage supply, 2.7 V–3.6 V
AVSS_DAC	26	G2,H2	–	Analog DAC ground supply, 0 V
MONO_LOP	27	J2	O	Mono line output (+)
MONO_LOM	28	J3	O	Mono line output (–)
LEFT_LOP	29	J4	O	Left line output (+)
LEFT_LOM	30	J5	O	Left line output (–)
RIGHT_LOP	31	J6	O	Right line output (+)
RIGHT_LOM	32	J7	O	Right line output (–)
$\overline{\text{RESET}}$	33	H8	I	Reset
GPIO2	34	J8	I/O	General-purpose input/output #2 (input/output)/digital microphone data input/PLL clock input/audio serial data bus bit clock input/output

表 7-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	VQFN	BGA BALL		
GPIO1	35	J9	I/O	General-purpose input/output #1 (input/output)/PLL/clock mux output/short circuit interrupt/AGC noise flag/digital microphone clock audio serial data bus word clock input/output
DVDD	36	H9	–	Digital core voltage supply, 1.65 V–1.95 V
MCLK	37	G8	I	Master clock input
BCLK	38	G9	I	Audio serial data bus bit clock (input/output)
WCLK	39	F9	I	Audio serial data bus word clock (input/output)
DIN	40	E9	I	Audio serial data bus data input (input)
DOUT	41	F8	O	Audio serial data bus data output (output)
DVSS	42	D9	–	Digital core / I/O ground supply, 0V
SELECT	43	E8	I	Control mode select pin (1 = SPI, 0 = I^2C)
IOVDD	44	C9	–	I/O voltage supply, 1.1 V–3.6 V
MFP0	45	B8	I	Multifunction pin #0 – SPI chip select / GPI / I^2C address pin #0
MFP1	46	B9	I	Multifunction pin #1 – SPI serial clock / GPI / I^2C address pin #1S
MFP2	47	A8	I	Multifunction pin #2 – SPI MISO slave serial data output / GPOI
MFP3	48	A9	I	Multifunction pin #3 – SPI MOSI slave serial data input/GPI/audio serial data bus data input
SCL	1	C8	I/O	I^2C serial clock/GPIO
SDA	2	D8	I/O	I^2C serial data input/output/GPIO
NC	–	A7	–	Not connected
LINE1LP	3	A6	I	MIC1 or Line1 analog input (left + or multifunction)
LINE1LM	4	A5	I	MIC1 or Line1 analog input (left – or multifunction)
LINE1RP	5	B7	I	MIC1 or Line1 analog input (right + or multifunction)
LINE1RM	6	B6	I	MIC1 or Line1 analog input (right – or multifunction)
LINE2LP	7	A4	I	MIC2 or Line2 analog input (left + or multifunction)
LINE2LM	8	B5	I	MIC2 or Line2 analog input (left – or multifunction)
LINE2RP	9	B4	I	MIC2 or Line2 analog input (right + or multifunction)
LINE2RM	10	A3	I	MIC2 or Line2 analog input (right – or multifunction)
MIC3L	11	B3	I	MIC3 input (left or multifunction)
MICDET	12	B2	I	Microphone detect
NC	–	C4-C7, D3-D7, E3-E7, F3-F7, G3-G7, H3-H7	–	Not connected

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX.	UNIT
Input voltage	AVDD_DAC to AVSS_DAC, DRVDD to DRVSS, AVSS_ADC	–0.3	3.9	V
	AVDD to DRVSS	–0.3	3.9	V
	IOVDD to DVSS	–0.3	3.9	V
	DVDD to DVSS	–0.3	2.5	V
	AVDD_DAC to DRVDD	–0.1	0.1	V
Digital input voltage	to DVSS	–0.3	IOVDD + 0.3	V
Analog input voltage	to AVSS_ADC	–0.3	AVDD + 0.3	V
Operating temperature		–40	t85	°C
Junction temperature, T_J			105	°C
Storage temperature, T_{stg}		–65	105	°C
Power dissipation		$(T_J$ Max – $T_A) / R_{\theta JA}$		

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ESD complicance tested to EIA/JESD22-A114-B and passed.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1900	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD_DAC, DRVDD[(1)]	Analog supply voltage	2.7	3.3	3.6	V
DVDD[(1)]	Digital core supply voltage	1.65	1.8	1.95	V
IOVDD[(1)]	Digital I/O supply voltage	1.1	1.8	3.6	V
V_I	Analog full-scale 0-dB input voltage (DRVDD1 = 3.3 V)		0.707		V_{RMS}
	Stereo line output load resistance	10			kΩ
	Stereo headphone output load resistance	16			Ω
	Digital output load capacitance		10		pF
T_A	Operating free-air temperature	–40		85	°C

(1) Analog voltage values are with respect to AVSS_ADC, AVSS_DAC, DRVSS; digital voltage values are with respect to DVSS.

8.4 Thermal Information

THERMAL METRIC[1]		RGZ 48 PINS	ZQE 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.1	54.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.7	25.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.9	31.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.4	31.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

at 25°C, AVDD_DAC, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC						
	Input signal level (0-dB)	Single-ended input		0.707		V_{RMS}
	Signal-to-noise ratio, A-weighted[1] [2]	f_S = 48 ksps, 0-dB PGA gain, inputs ac-shorted to ground	80	92		dB
	Dynamic range [2]	f_S = 48 ksps, 0-dB PGA gain, –60 dB full-scale input signal		91		dB
THD	Total harmonic distortion	f_S = 48 ksps, 0-dB PGA gain, –2dB full-scale, 1-kHz input signal		–88	–70	dB
PSRR	Power supply rejection ratio	217-Hz signal applied to DRVDD		49		dB
		1-kHz signal applied to DRVDD		46		
	Gain error	f_S = 48 ksps, 0-dB PGA gain, –2dB full-scale, 1-kHz input signal		0.84		dB
	Input channel separation	1-kHz, –2-dB full-scale signal, MIC3L to MIC3R		–86		dB
		1-kHz, –2-dB full-scale signal, MIC2L to MIC2R		–98		
		1-kHz, –2-dB full-scale signal, MIC1L to MIC1R		–75		
	ADC programmable gain amplifier maximum gain	1-kHz input tone		59.5		dB
	ADC programmable gain amplifier step size			0.5		dB
	Input resistance	MIC1L/MIC1R inputs routed to single ADC Input mix attenuation = 0 dB		20		kΩ
		MIC1L/MIC1R inputs routed to single ADC, input mix attenuation = 12 dB		80		
		MIC2L/MIC2R inputs routed to single ADC Input mix attenuation = 0 dB		20		
		MIC2L/MIC2R inputs routed to single ADC, input mix attenuation = 12 dB		80		
		MIC3L/MIC3R inputs routed to single ADC Input mix attenuation = 0 dB		20		
		MIC3L/MIC3R inputs routed to single ADC, input mix attenuation = 12 dB		80		
	Input level control minimum attenuation setting			0		dB
	Input level control maximum attenuation setting			12		dB
	Input signal level	Differential Input		1.414		V_{RMS}
	Signal-to-noise ratio, A-weighted[1] [2]	f_S = 48 ksps, 0-dB PGA gain, inputs ac-shorted to ground, differential mode		92		dB
THD	Total harmonic distortion	f_S = 48 ksps, 0-dB PGA gain, –2-dB full-scale 1-kHz input signal, differential mode		–91		dB

8.5 Electrical Characteristics (continued)

at 25°C, AVDD_DAC, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48-kHz, 16-bit audio data (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG PASS THROUGH MODE						
	Input to output switch resistance, (rds_{ON})	MIC1/LINE1 to LINE_OUT		330		Ω
		MIC2/LINE2 to LINE_OUT		330		
ADC DIGITAL DECIMATION FILTER, f_S = 48 kHz						
	Filter gain from 0 to 0.39 f_S			±0.1		dB
	Filter gain at 0.4125 f_S			–0.25		dB
	Filter gain at 0.45 f_S			–3		dB
	Filter gain at 0.5 f_S			–17.5		dB
	Filter gain from 0.55 f_S to 64 f_S			–75		dB
	Filter group delay			17/f_S		s
MICROPHONE BIAS						
	Bias voltage	Programmable setting = 2.0		2.0		V
		Programmable setting = 2.5	2.3	2.5	2.7	
		Programmable setting = DRVDD		DRVDD		
	Current sourcing	Programmable setting = 2.5V		4		mA
AUDIO DAC – Differential Line output, load = 10 kΩ						
	Full-scale output voltage	0-dB input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V		1.414		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted[(3)]	No input signal, output volume control = 0 dB, output common mode setting = 1.35 V, f_S = 48 kHz	90	102		dB
	Dynamic range, A-weighted	–60 dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		99		dB
THD	Total harmonic distortion	0-dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		–94	–75	dB
	Power-supply rejection ratio	217-Hz signal applied to DRVDD, AVDD_DAC		77		dB
		1-kHz signal applied to DRVDD, AVDD_DAC		73		
	DAC channel separation	0-dB full-scale input signal between left and right Lineout		123		dB
	DAC gain error	0-dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		–0.4		dB
AUDIO DAC – SINGLE ENDED LINE OUTPUT, Load = 10 kΩ						
	Full-scale output voltage	0-dB input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V		0.707		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted	No input signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		97		dB
THD	Total harmonic distortion	0-dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		84		dB
	DAC gain error	0-dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		0.55		dB
AUDIO DAC – SINGLE ENDED HEADPHONE OUTPUT, Load = 16 Ω						
	Full-scale output voltage	0-dB input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V		0.707		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted	No input signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		95		dB
		No input signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz, 50% DAC current boost mode		96		dB
	Dynamic range, A-weighted	–60-dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		92		dB
THD	Total harmonic distortion	0-dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		–80	–65	dB
PSRR	Power-supply rejection ratio	217-Hz signal applied to DRVDD, AVDD_DAC		41		dB
		1-kHz signal applied to DRVDD, AVDD_DAC		44		
	DAC channel separation	0-dB full-scale input signal between left and right Lineout		84		dB
	DAC gain error	0-dB 1-kHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V, f_S = 48 kHz		–0.5		dB

8.5 Electrical Characteristics (continued)

at 25°C, AVDD_DAC, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO DAC – LINEOUT AND HEADPHONE OUT DRIVERS							
	Output common mode	First option			1.35		V
		Second option			1.5		
		Third option			1.65		
		Fourth option			1.8		
	Output volume control max setting				9		dB
	Output volume control step size				1		dB
DAC DIGITAL INTERPOLATION – FILTER f_S = 48 ksps							
	Pass band			0		0.45 f_S	Hz
	Pass-band ripple				±0.06		dB
	Transition band			0.45 f_S		0.55 f_S	Hz
	Stop band			0.55 f_S		7.5 f_S	Hz
	Stop-band attenuation				65		dB
	Group delay				21/f_S		s
DIGITAL I/O							
V_{IL}	Input low level			–0.3		0.3 × IOVDD	V
V_{IH}	Input high level(4)	IOVDD > 1.6 V		0.7 × IOVDD			V
		IOVDD < 1.6 V		1.1			
V_{OL}	Output low level					0.1 × IOVDD	V
V_{OH}	Output high level			0.8 × IOVDD			V
POWER CONSUMPTION, DRVDD, AVDD_DAC = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V							
	Current consumption	IDRVDD+IAVDD_DAC	RESET held low		0.1		µA
		IDVDD			0.2		
		IDRVDD+IAVDD_DAC	Mono ADC record, f_S = 8 kSPS, I²S slave, AGC off, no signal		2.1		mA
		IDVDD			0.5		
		IDRVDD+IAVDD_DAC			4.1		mA
		IDVDD			0.6		
		IDRVDD+IAVDD_DAC	Stereo ADC record, f_S = 48 kSPS, I²S slave, AGC off, no signal		4.3		mA
		IDVDD			2.5		
		IDRVDD+IAVDD_DAC	Stereo DAC playback to line out, analog mixer bypassed, f_S = 48 kSPS, I²S slave		3.5		mA
		IDVDD			2.3		
		IDRVDD+IAVDD_DAC	Stereo DAC playback to line out, f_S = 48 kSPS, I²S slave, no signal		4.9		mA
		IDVDD			2.3		
		IDRVDD+IAVDD_DAC	Stereo DAC playback to stereo single-ended headphone, f_S = 48 kSPS, I²S slave, no signal		6.7		mA
		IDVDD			2.3		
		IDRVDD+IAVDD_DAC	Stereo line in to stereo line out, no signal		3.1		mA
		IDVDD			0		
		IDRVDD+IAVDD_DAC	Extra power when PLL enabled		1.4		mA
		IDVDD			0.9		
		IDRVDD+IAVDD_DAC	All blocks powered down, headset detection enabled		28		µA
		IDVDD			2		

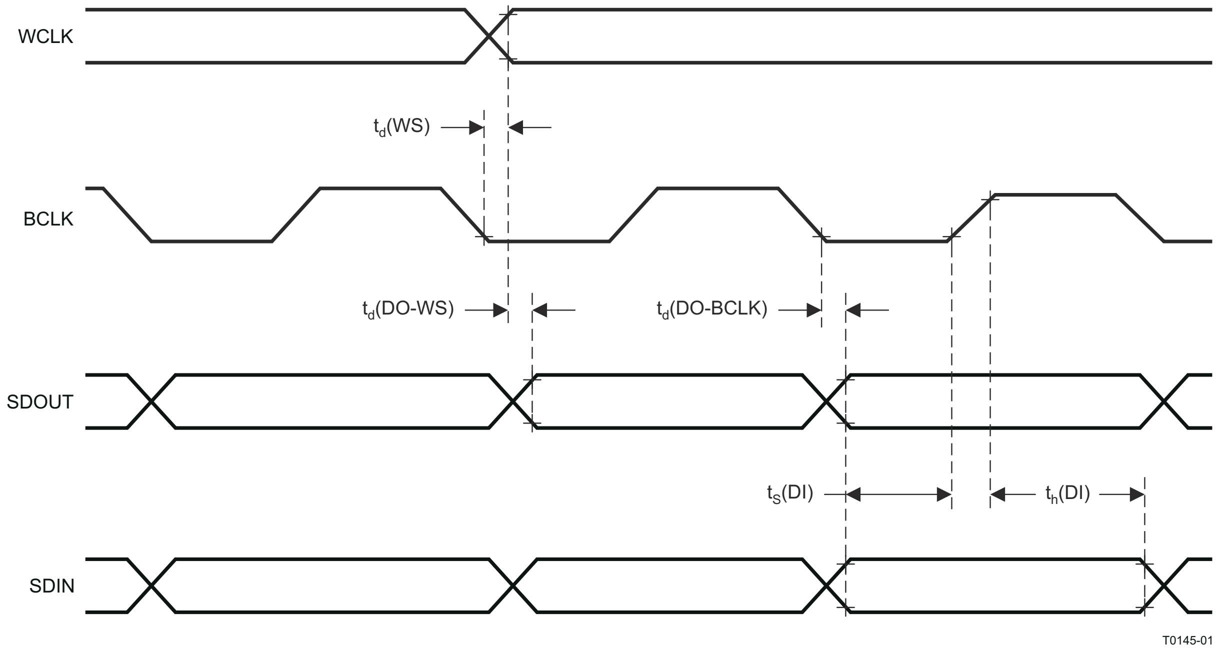
(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the *Electrical Characteristics*. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) Unless otherwise noted, all measurements use output common-mode voltage setting of 1.35 V, 0-dB output level control gain, 16-Ω single-ended load.
(4) When IOVDD < 1.6 V, minimum V_{IH} is 1.1 V.

8.6 Timing Requirements: Audio Data Serial Interface[1]

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
I^2S/LJF/RJF Timing in Master Mode						
t_d(WS)	ADWS/WCLK delay time		50		15	ns
t_d(DO-WS)	ADWS/WCLK to DOUT delay time		50		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns
DSP Timing in Master Mode						
t_d(WS)	ADWS/WCLK delay time		50		15	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns
I^2S/LJF/RJF Timing in Slave Mode						
t_H(BCLK)	BCLK high period	70		35		ns
t_L(BCLK)	BCLK low period	70		35		ns
t_s(WS)	ADWS/WCLK setup time	10		6		ns
t_h(WS)	ADWS/WCLK hold time	10		6		ns
t_d(DO-WS)	ADWS/WCLK to DOUT delay time (for LJF Mode only)		50		35	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		20	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns
DSP Timing in Slave Mode						
t_H(BCLK)	BCLK high period	70		35		ns
t_L(BCLK)	BCLK low period	70		35		ns
t_s(WS)	ADWS/WCLK setup time	10		8		ns
t_h(WS)	ADWS/WCLK hold time	10		8		ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		20	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

(1) All timing specifications are measured at characterization but not tested at final test.

8.7 Timing Diagrams



All specifications at 25°C, DVDD = 1.8 V.

図 8-1. I²S, LJF, RJF Timing in Master Mode

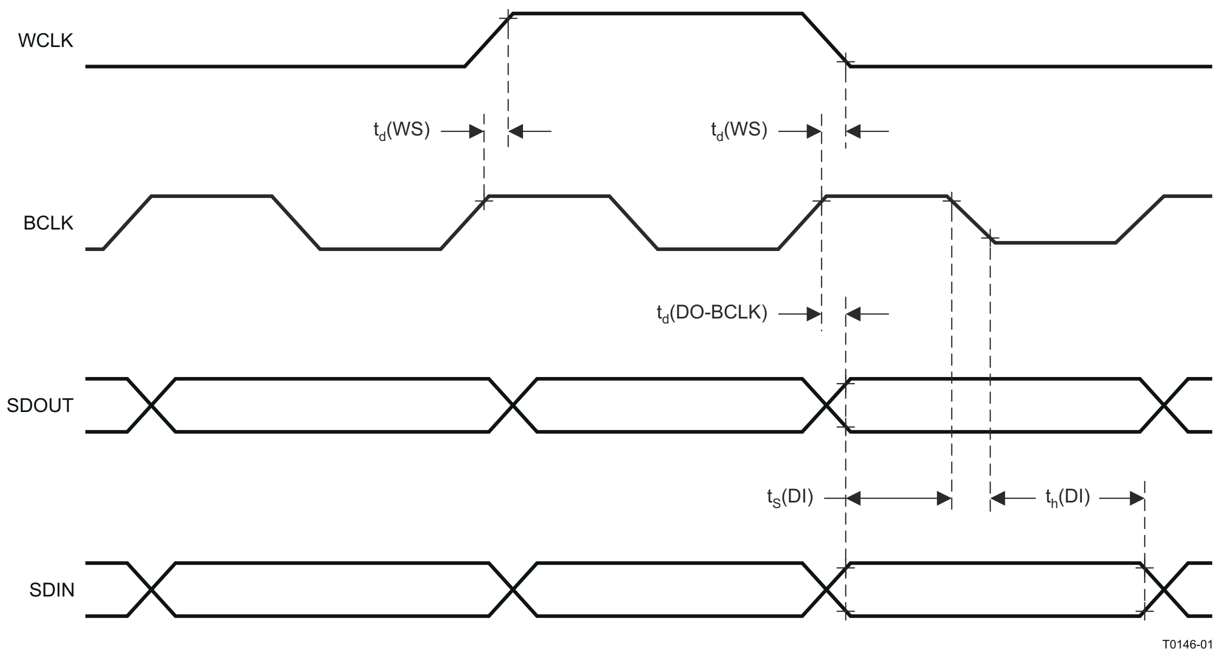


図 8-2. DSP Timing in Master Mode

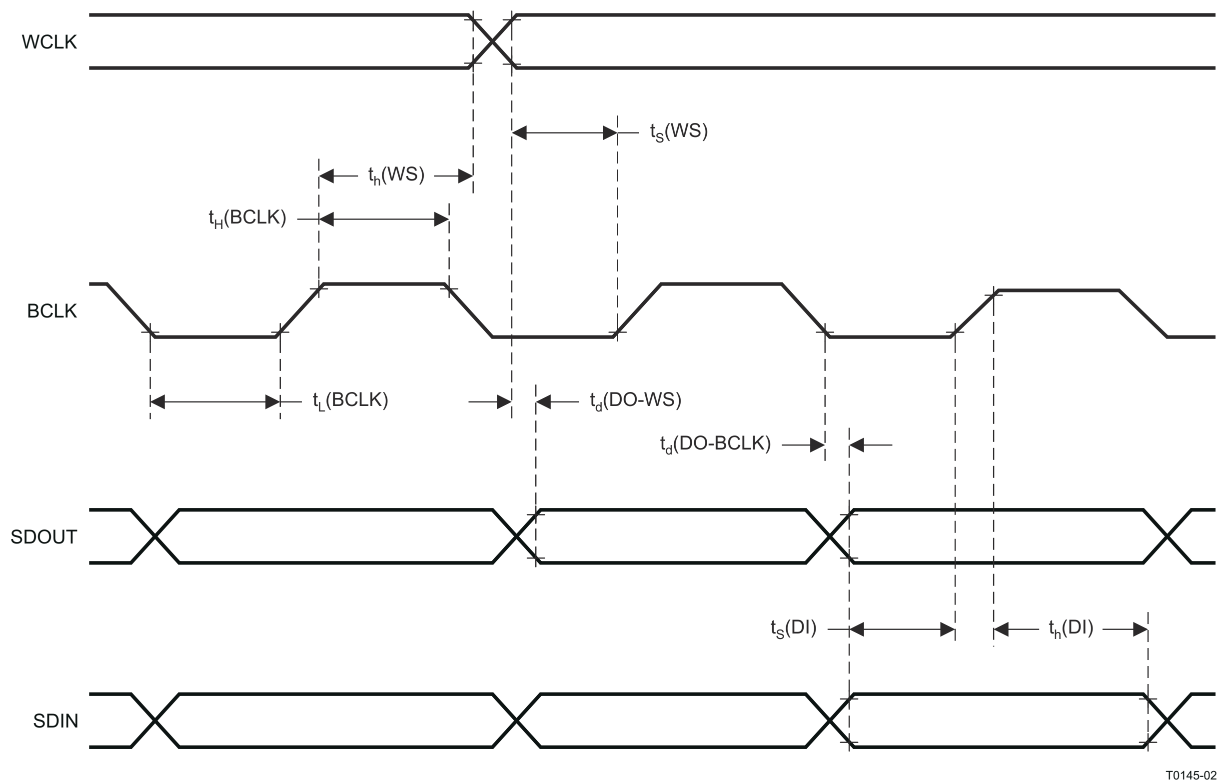


図 8-3. I^2S, LJF, RJF Timing in Slave Mode

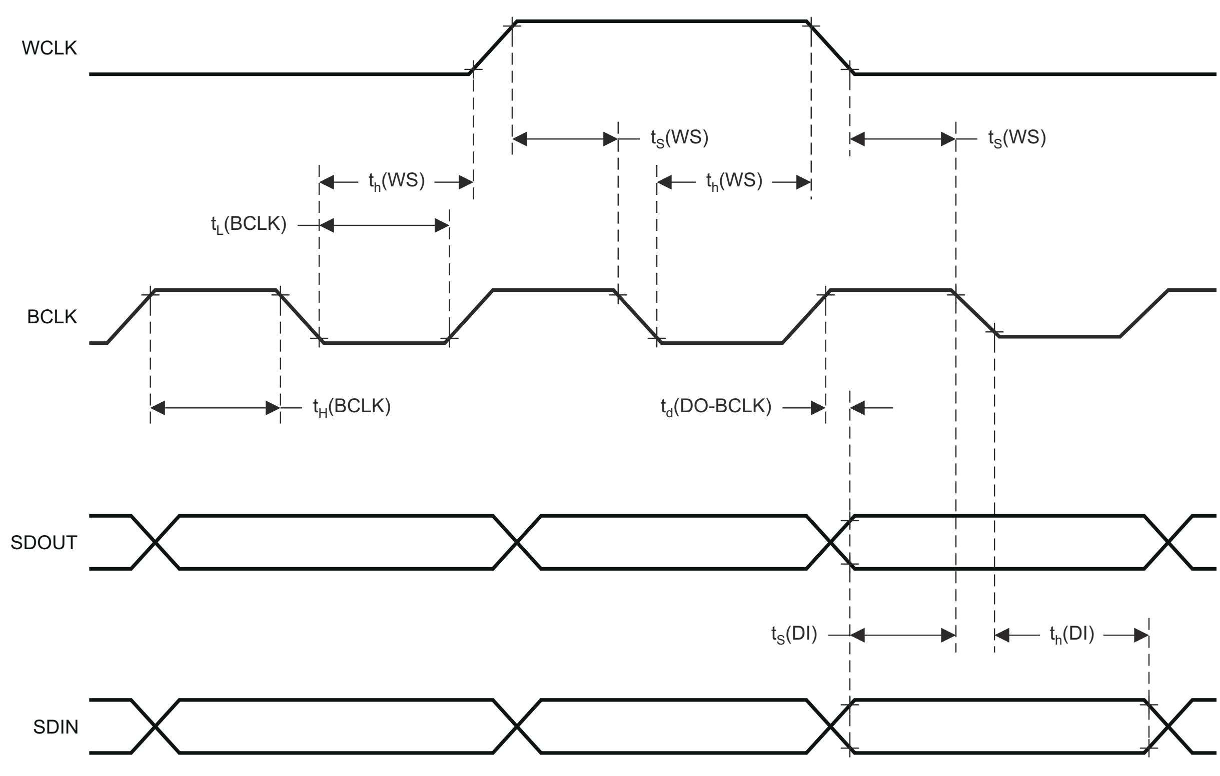


図 8-4. DSP Timing in Slave Mode

8.8 Typical Characteristics

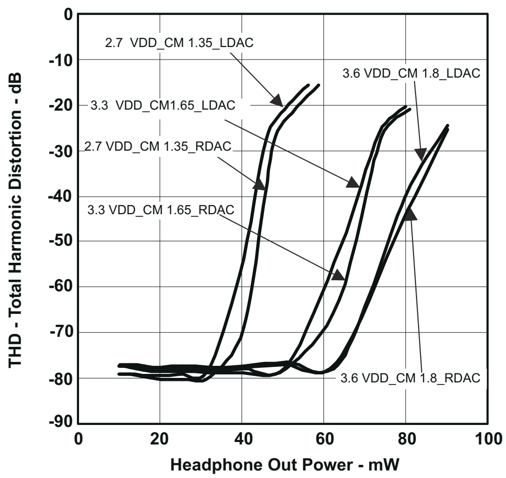


図 8-5. Total Harmonic Distortion vs Headphone Out Power

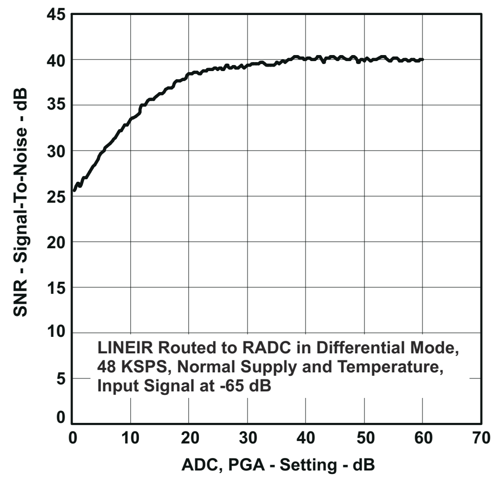


図 8-6. Signal-To-Noise Ratio vs ADC PGA Setting

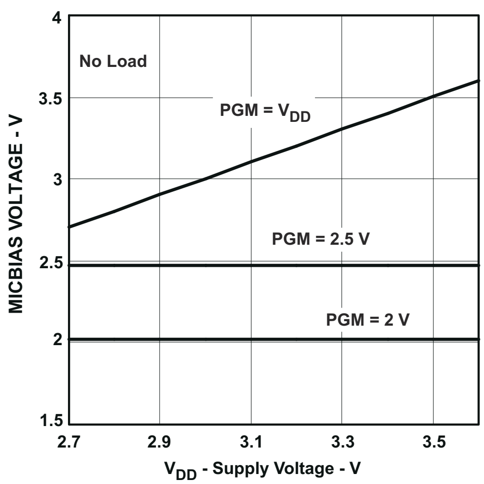


図 8-7. MICBIAS Voltage vs Supply Voltage

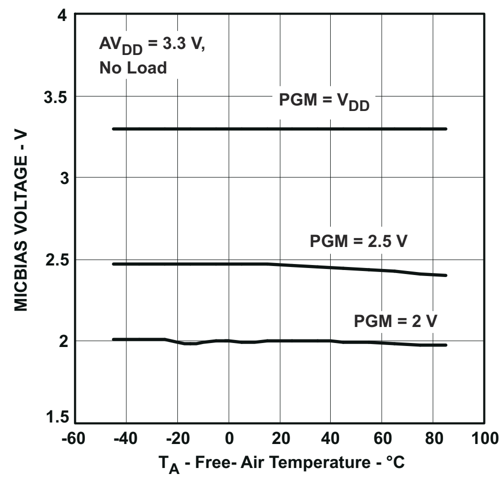


図 8-8. MICBIAS Voltage vs Free-Air Temperature

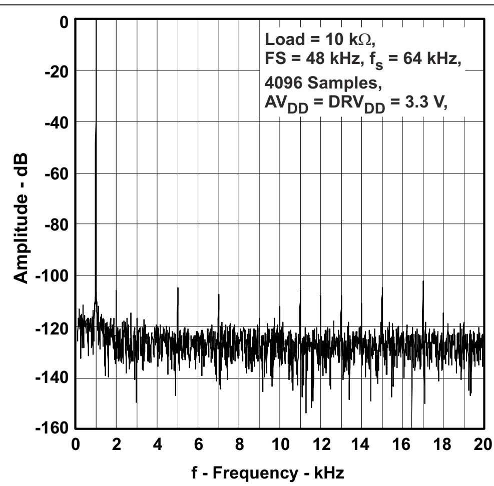


図 8-9. Left DAC FFT

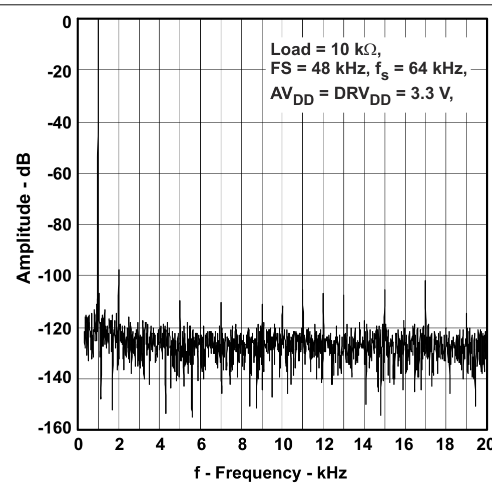


図 8-10. Right DAC FFT

8.8 Typical Characteristics (continued)

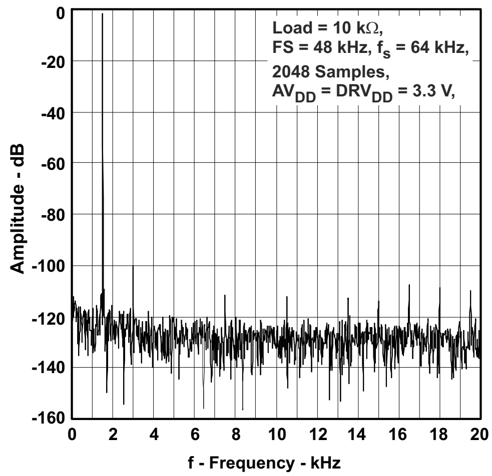


図 8-11. Left ADC FFT

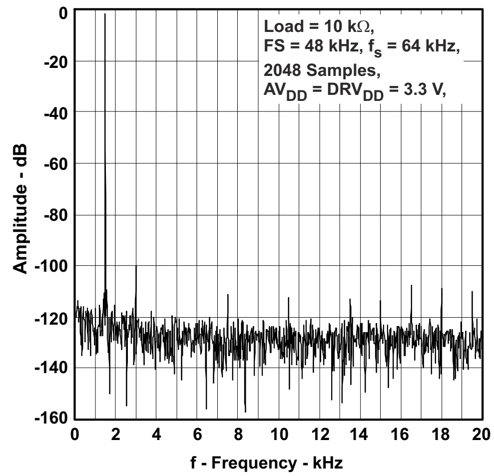


図 8-12. Right ADC FFT

9 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

10 Detailed Description

10.1 Overview

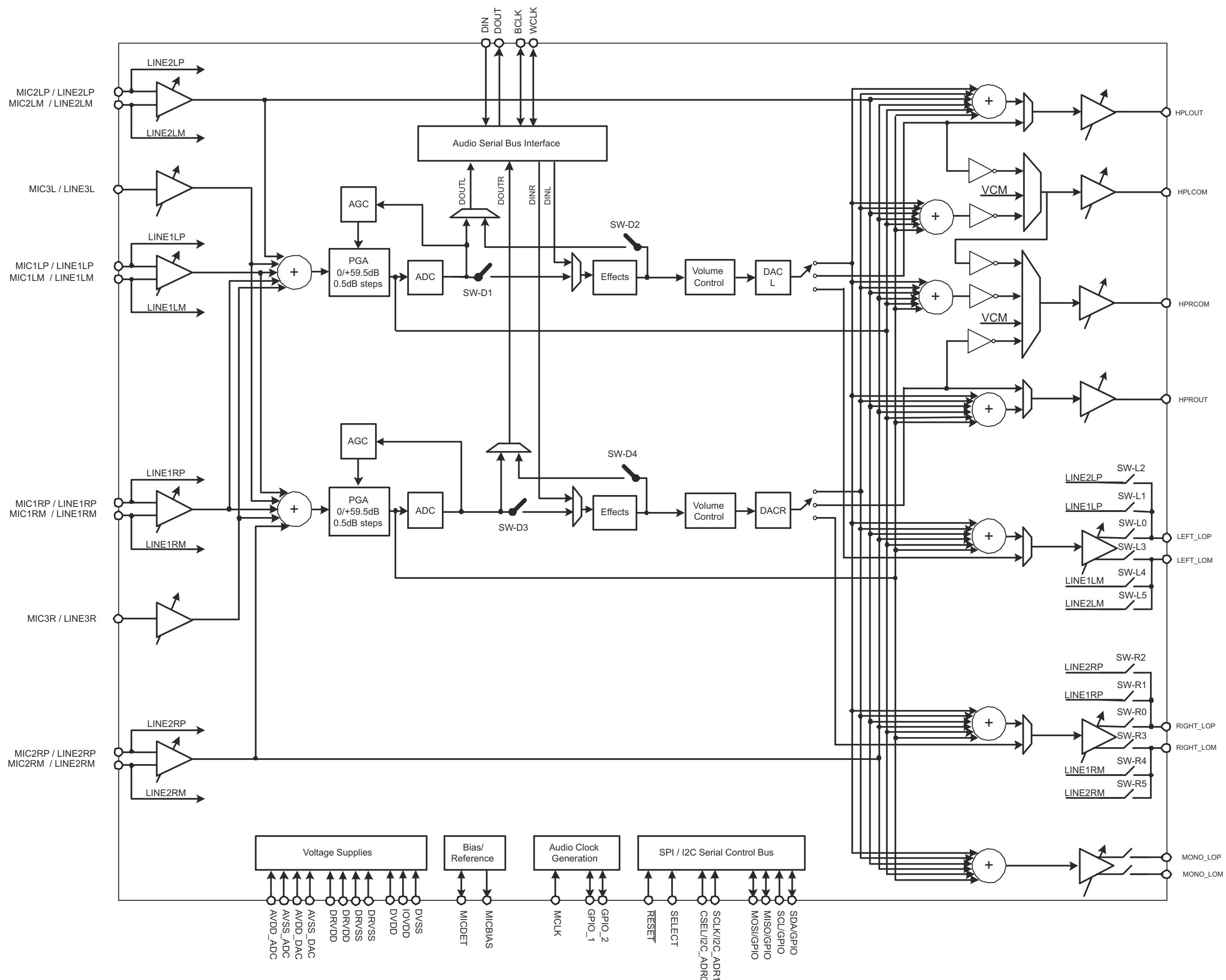
The TLV320AIC3106 is a highly flexible, low power, stereo audio codec with extensive feature integration, intended for applications in smartphones, PDAs, and portable computing, communication, and entertainment applications. Available in a 5x5mm 80-ball BGA (with 51 balls actually used) and 7x7mm 48-lead QFN, the product integrates a host of features to reduce cost, board space, and power consumption in space-constrained, battery-powered, portable applications.

The TLV320AIC3106 consists of the following blocks:

- Stereo audio multi-bit delta-sigma DAC (8 kHz–96 kHz)
- Stereo audio multi-bit delta-sigma ADC (8 kHz–96 kHz)
- Programmable digital audio effects processing (3-D, bass, treble, mid-range, EQ, notch filter, de-emphasis)
- Six audio inputs
- Four high-power audio output drivers (headphone drive capability)
- Three fully differential line output drivers
- Fully programmable PLL
- Headphone/headset jack detection with interrupt

Communication to the TLV320AIC3106 for control is pin-selectable (using the SELECT pin) as either SPI or I^2C. The SPI interface requires that the Slave Select signal (MFP0) be driven low to communicate with the TLV320AIC3106. Data is then shifted into or out of the TLV320AIC3106 under control of the host microprocessor, which also provides the serial data clock. The I^2C interface supports both standard and fast communication modes, and also enables cascading of up to four multiple codecs on the same I^2C bus through the use of two pins for addressing (MFP0, MFP1).

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Hardware Reset

The TLV320AIC3106 requires a hardware reset after power-up for proper operation. After all power supplies are at their specified values, the $\overline{\text{RESET}}$ pin must be driven low for at least 10 ns. If this reset sequence is not performed, the TLV320AIC3106 may not respond properly to register reads/writes.

10.3.2 Digital Audio Data Serial Interface

Audio data is transferred between the host processor and the TLV320AIC3106 via the digital audio data serial interface, or *audio bus*. The audio bus on this device is very flexible, including left or right justified data options, support for I^{2}S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The data serial interface uses two sets of pins for communication between external devices, with the particular pin used controlled through register programming. This configuration is illustrated in 図 10-1.

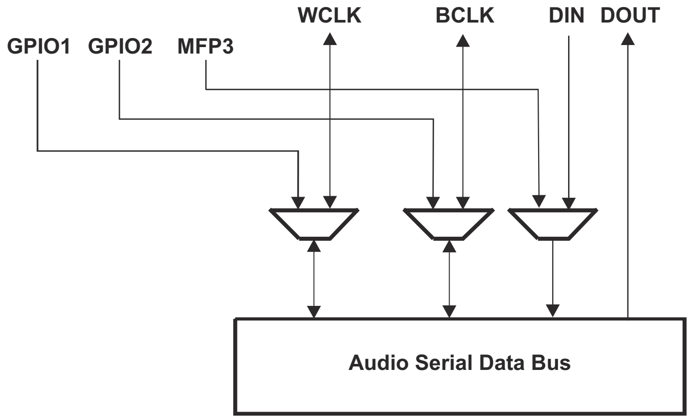
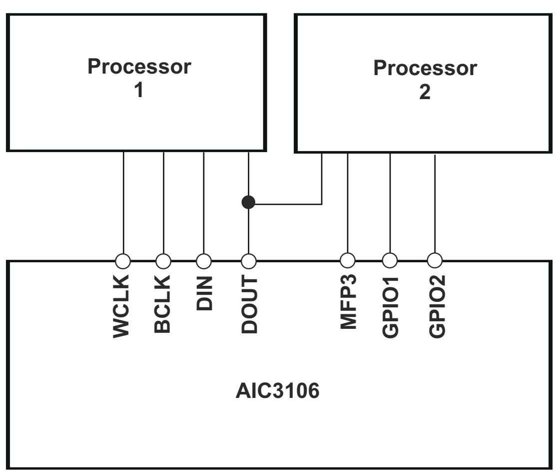


図 10-1. Alternate Audio Bus Mulitplexing Function

In cases where MFP3 is needed for a secondary device digital input, the TLV320AIC3106 must be used in I^{2}C mode (when in SPI mode, MFP3 is used as the SPI bus MOSI pin and thus cannot be used here as an alternate digital input source).

This mux capability allows the TLV320AIC3106 to communicate with two separate devices with independent I^{2}S/PCM buses. An example of such an application is a cellphone containing a Bluetooth transceiver with PCM/I^{2}S interface, as shown in 図 10-2. The applications processor can be connected to the WCLK, BCLK, DIN, DOUT pins on the TLV320AIC3106, while a Bluetooth device with PCM interface can be connected to the GPIO1, GPIO2, MFP3, and DOUT pins on the TLV320AIC3106. By programming the registers via I^{2}C control, the applications processor can determine which device is communicating with the TLV320AIC3106. This is attractive in cases where the TLV320AIC3106 can be configured to communicate data with the Bluetooth device, then the applications processor can be put into a low power sleep mode, while voice/audio transmission still occurs between the Bluetooth device and the TLV320AIC3106.



Possible Processor Types:
Application Processor, Multimedia Processor,
Compressed Audio Decoder, Wireless Modem,
Bluetooth Module, Additional Audio/Voice Codec

図 10-2. TLV320AIC3106 Connected to Multiple Audio Devices

The audio bus of the TLV320AIC3106 can be configured for left or right justified, I^{2}S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. In addition, the word clock (WCLK or GPIO1) and bit clock (BCLK or GPIO2) can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors

The word clock (WCLK or GPIO1) is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock (BCLK or GPIO2) is used to clock in and out the digital audio data across the serial bus. When in Master mode, this signal can be programmed in two further modes: continuous transfer mode, and 256-clock mode. In continuous transfer mode, only the minimal number of bit clocks needed to transfer the audio data are generated, so in general the number of bit clocks per frame will be two times the data width. For example, if data width is chosen as 16 bits, then 32 bit clocks will be generated per frame. If the bit clock signal in master mode will be used by a PLL in another device, it is recommended that the 16-bit or 32-bit data width selections be used. These cases result in a low jitter bit clock signal being generated, having frequencies of 32 × f_S or 64 × f_S. In the cases of 20-bit and 24-bt data width in master mode, the bit clocks generated in each frame will not all be of equal period, due to the device not having a clean 40 × f_S or 48 × f_S clock signal readily available. The average frequency of the bit clock signal is still accurate in these cases (being 40 × f_S or 48 × f_S), but the resulting clock signal has higher jitter than in the 16-bit and 32-bit cases.

In 256-clock mode, a constant 256 bit clocks per frame are generated, independent of the data width chosen. The TLV320AIC3106 further includes programmability to 3-state the DOUT line during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data will begin, time-division multiplexing (TDM) can be accomplished, resulting in multiple codecs able to use a single audio serial data bus.

When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface will be put into a 3-state output condition.

10.3.2.1 Right-Justified Mode

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

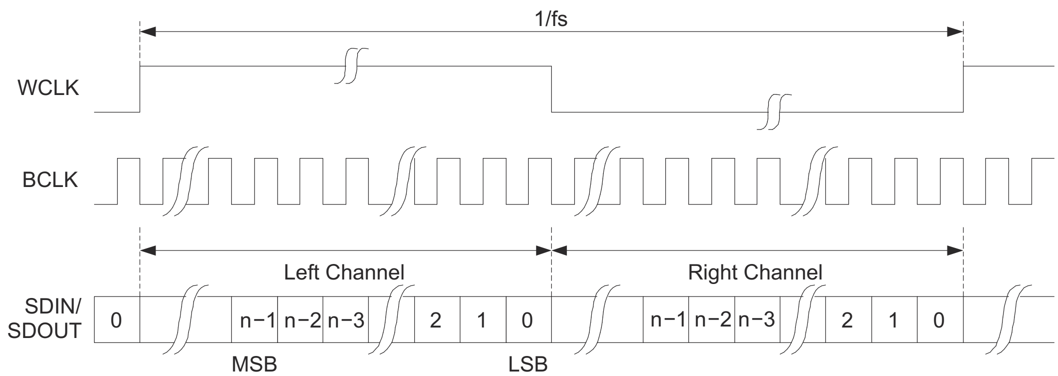


図 10-3. Right-Justified Serial Bus Mode Operation

10.3.2.2 Left-Justified Mode

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

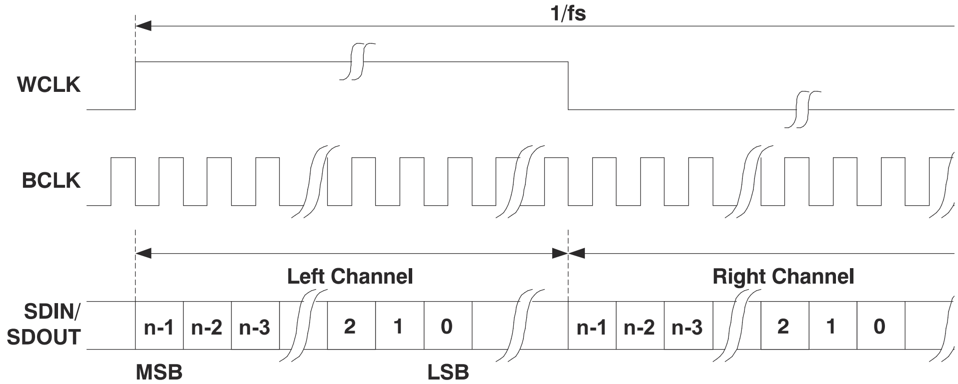


図 10-4. Left-Justified Serial Data Bus Mode Operation

10.3.2.3 I²S Mode

In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

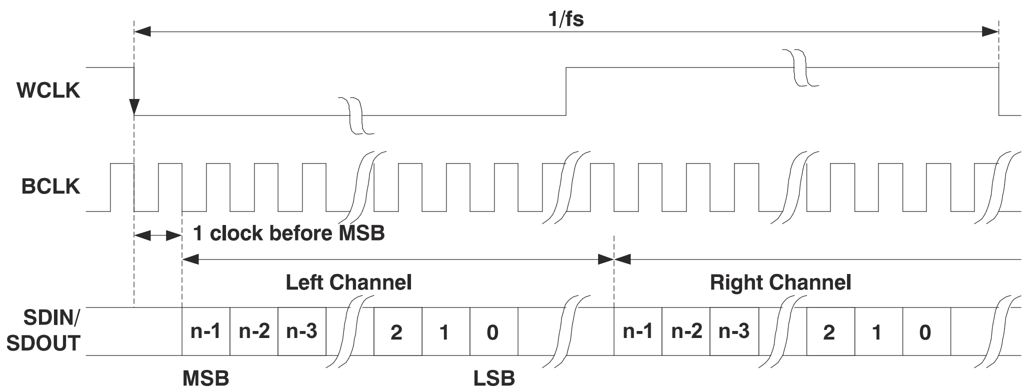


図 10-5. I²S Serial Data Bus Mode Operation

10.3.2.4 DSP Mode

In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

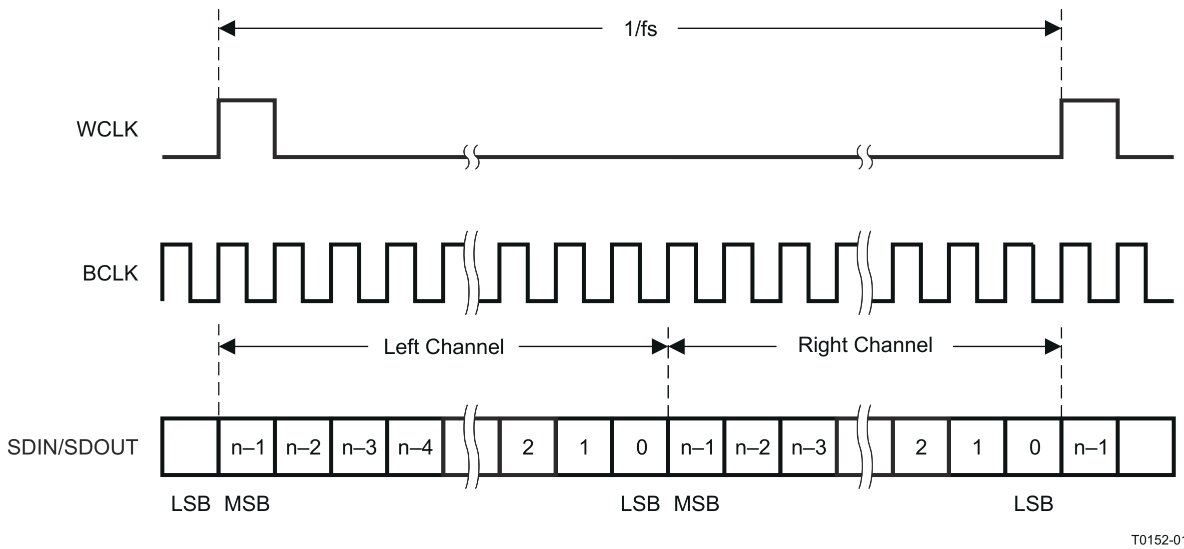


図 10-6. DSP Serial Bus Mode Operation

10.3.2.5 TDM Data Transfer

Time-division multiplexed data transfer can be realized in any of the above transfer modes if the 256-clock bit clock mode is selected, although it is recommended to be used in either left-justified mode or DSP mode. By changing the programmable offset, the bit clock in each frame where the data begins can be changed, and the serial data output driver (DOUT) can also be programmed to 3-state during all bit clocks except when valid data is being put onto the bus. This allows other codecs to be programmed with different offsets and to drive their data onto the same DOUT line, just in a different slot. For incoming data, the codec simply ignores data on the bus except where it is expected based on the programmed offset.

Note that the location of the data when an offset is programmed is different, depending on what transfer mode is selected. In DSP mode, both left and right channels of data are transferred immediately adjacent to each other in the frame. This differs from left-justified mode, where the left and right channel data will always be a half-frame apart in each frame. In this case, as the offset is programmed from zero to some higher value, both the left and right channel data move across the frame, but still stay a full half-frame apart from each other. This is depicted in 図 10-7 for the two cases.

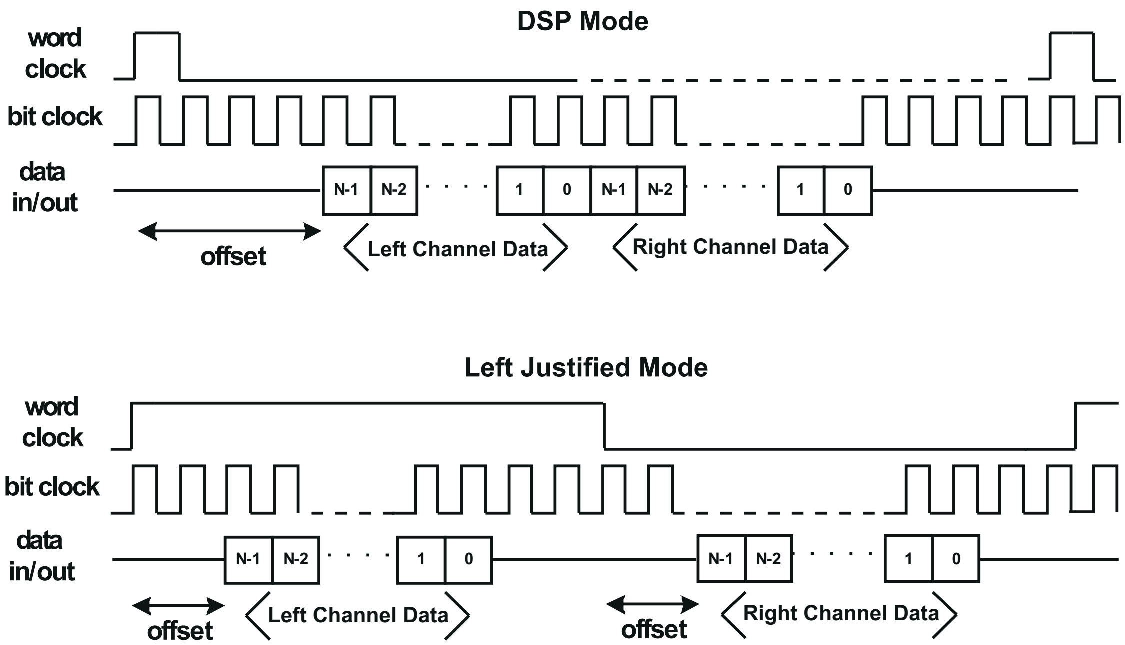


図 10-7. DSP Mode and Left Justified Modes, Showing the Effect of a Programmed Data Word Offset

10.3.3 Audio Data Converters

The TLV320AIC3106 supports the following standard audio sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz. The converters can also operate at different sampling rates in various combinations, which are described further below.

The data converters are based on the concept of an $f_{S(ref)}$ rate that is used internal to the part, and it is related to the actual sampling rates of the converters through a series of ratios. For typical sampling rates, $f_{S(ref)}$ will be either 44.1 kHz or 48 kHz, although it can realistically be set over a wider range of rates up to 53 kHz, with additional restrictions applying if the PLL is used. This concept is used to set the sampling rates of the ADC and DAC, and also to enable high quality playback of low sampling rate data, without high frequency audible noise being generated.

The sampling rate of the ADC and DAC can be set to $f_{S(ref)}$/NDAC or 2×$f_{S(ref)}$/NDAC, with NDAC being 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, or 6.

While only one $f_{S(ref)}$ can be used at a time in the part, the ADC and DAC sampling rates can differ from each other by using different NADC and NDAC divider ratios for each. For example, with $f_{S(ref)}$=44.1-kHz, the DAC sampling rate can be set to 44.1-kHz by using NDAC=1, while the ADC sampling rate can be set to 8.018-kHz by using NADC=5.5.

When the ADCs and DACs are operating at different sampling rates, an additional word clock is required, to provide information regarding where data begins for the ADC versus the DAC. In this case, the standard bit clock signal (which can be supplied through the BCLK pin or through GPIO2) is used to transfer both ADC and DAC data, the standard word clock signal is used to identify the start of the DAC data, and a separate ADC word clock signal (denoted ADWK) is used. This clock can be supplied or generated from GPIO1 at the same time the DAC word clock is supplied or generated from WCLK.

10.3.3.1 Audio Clock Generation

The audio converters in the TLV320AIC3106 need an internal audio master clock at a frequency of 256 × $f_{S(ref)}$, which can be obtained in a variety of manners from an external clock signal applied to the device.

A more detailed diagram of the audio clock section of the TLV320AIC3106 is shown in 図 10-8.

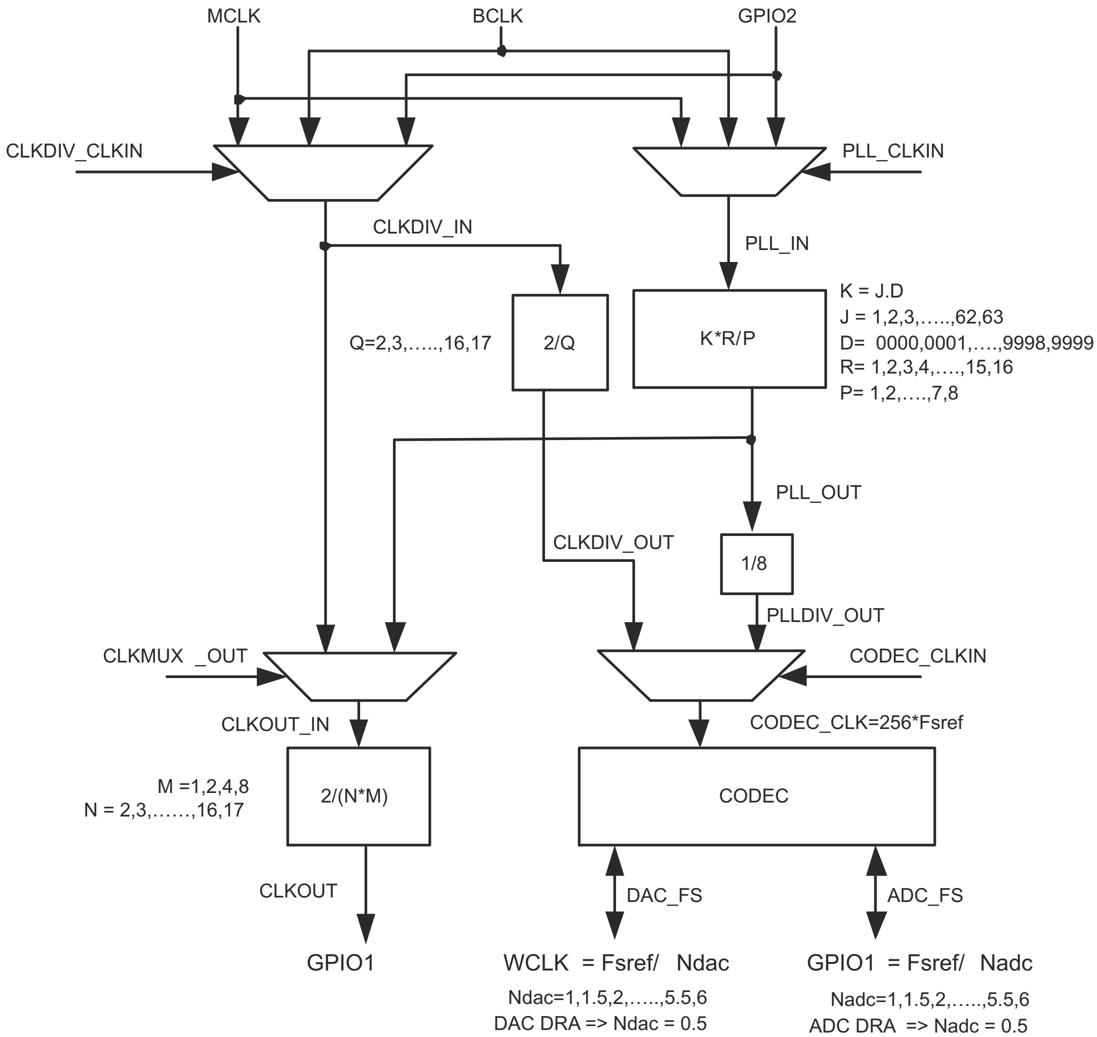


図 10-8. Audio Clock Generation Processing

The part can accept an MCLK input from 512 kHz to 50 MHz, which can then be passed through either a programmable divider or a PLL, to get the proper internal audio master clock needed by the part. The BCLK or GPIO2 inputs can also be used to generate the internal audio master clock.

This design also allows the PLL to be used for an entirely separate purpose in a system, if the audio codec is not powered up. The user can supply a separate clock to GPIO2, route this through the PLL, with the resulting output clock driven out GPIO1, for use by other devices in the system

A primary concern is proper operation of the codec at various sample rates with the limited MCLK frequencies available in the system. This device includes a highly programmable PLL to accommodate such situations easily. The integrated PLL can generate audio clocks from a wide variety of possible MCLK inputs, with particular focus paid to the standard MCLK rates already widely used.

When the PLL is disabled:

$$f_{S(ref)} = CLKDIV\_IN / (128 \times Q) \quad (1)$$

where:

- Q = 2, 3, …, 17

CLKDIV_IN can be MCLK, BCLK, or GPIO2, selected by register 102, bits D7-D6.

Note

When NDAC = 1.5, 2.5, 3.5, 4.5, or 5.5, odd values of Q are not allowed. In this mode, MCLK can be as high as 50 MHz, and $f_{S(ref)}$ should fall within 39 kHz to 53 kHz.

When the PLL is enabled:

$$f_{S(ref)} = (PLLCLK\_IN \times K \times R) / (2048 \times P) \quad (2)$$

where

- P = 1, 2, 3,…, 8
- R = 1, 2, …, 16
- K = J.D
- J = 1, 2, 3, …, 63
- D = 0000, 0001, 0002, 0003, …, 9998, 9999
- PLLCLK_IN can be MCLK or BCLK, selected by Page 0, register 102, bits D5-D4

P, R, J, and D are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

Examples:

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied to meet specified performance:

2 MHz ≤ (PLLCLK_IN / P) ≤ 20 MHz
80 MHz ≤ (PLLCLK _IN × K × R / P) ≤ 110 MHz
4 ≤ J ≤ 55

When the PLL is enabled and D≠0000, the following conditions must be satisfied to meet specified performance:

10 MHz ≤ PLLCLK _IN / P ≤ 20 MHz
80 MHz ≤ PLLCLK _IN × K × R / P ≤ 110 MHz
4 ≤ J ≤ 11
R = 1

Example:

MCLK = 12 MHz and $f_{S(ref)}$ = 44.1 kHz
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example:

MCLK = 12 MHz and $f_{S(ref)}$ = 48 kHz
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

表 10-1 lists several example cases of typical MCLK rates and how to program the PLL to achieve $f_{S(ref)}$ = 44.1 kHz or 48 kHz.

表 10-1. Typical MCLK Rates

$f_{S(ref)}$ = 44.1 kHz						
MCLK (MHz)	**P**	**R**	**J**	**D**	**ACHIEVED $f_{S(ref)}$**	**% ERROR**
2.8224	1	1	32	0	44100.00	0.0000
5.6448	1	1	16	0	44100.00	0.0000
12.0	1	1	7	5264	44100.00	0.0000
13.0	1	1	6	9474	44099.71	–0.0007
16.0	1	1	5	6448	44100.00	0.0000
19.2	1	1	4	7040	44100.00	0.0000
19.68	1	1	4	5893	44100.30	0.0007
48.0	4	1	7	5264	44100.00	0.0000
$f_{S(ref)}$ = 48 kHz						
MCLK (MHz)	P	R	J	D	ACHIEVED $f_{S(ref)}$	% ERROR
2.048	1	1	48	0	48000.00	0.0000
3.072	1	1	32	0	48000.00	0.0000
4.096	1	1	24	0	48000.00	0.0000
6.144	1	1	16	0	48000.00	0.0000
8.192	1	1	12	0	48000.00	0.0000
12.0	1	1	8	1920	48000.00	0.0000
13.0	1	1	7	5618	47999.71	–0.0006
16.0	1	1	6	1440	48000.00	0.0000
19.2	1	1	5	1200	48000.00	0.0000
19.68	1	1	4	9951	47999.79	–0.0004
48.0	4	1	8	1920	48000.00	0.0000

The TLV320AIC3106 can also output a separate clock on the GPIO1 pin. If the PLL is being used for the audio data converter clock, the M and N settings can be used to provide a divided version of the PLL output. If the PLL is not being used for the audio data converter clock, the PLL can still be enabled to provide a completely independent clock output on GPIO1. The formula for the GPIO1 clock output when PLL is enabled and CLKMUX_OUT is 0 is:

$$\text{GPIO1} = (\text{PLLCLK\_IN} \times 2 \times K \times R) / (M \times N \times P) \quad (3)$$

When CLKMUX_OUT is 1, regardless of whether PLL is enabled or disabled, the input to the clock output divider can be selected as MCLK, BCLK, or GPIO2. Is this case, the formula for the GPIO1 clock is:

$$\text{GPIO1} = (\text{CLKDIV\_IN} \times 2) / (M \times N) \quad (4)$$

where:

- M = 1, 2, 4, 8
- N = 2, 3, …, 17
- CLKDIV_IN can be BCLK, MCLK, or GPIO2, selected by page 0, register 102, bits D7-D6

10.3.3.2 Stereo Audio ADC

The TLV320AIC3106 includes a stereo audio ADC, which uses a delta-sigma modulator with 128-times oversampling in single-rate mode, followed by a digital decimation filter. The ADC supports sampling rates from 8 kHz to 48 kHz in single-rate mode, and up to 96 kHz in dual-rate mode. Whenever the ADC or DAC is in operation, the device requires that an audio master clock be provided and appropriate audio clock generation be set up within the device.

In order to provide optimal system power dissipation, the stereo ADC can be powered one channel at a time, to support the case where only mono record capability is required. In addition, both channels can be fully powered or entirely powered down.

The integrated digital decimation filter removes high-frequency content and downsamples the audio data from an initial sampling rate of 128 f_S to the final output sampling rate of f_S. The decimation filter provides a linear phase output response with a group delay of 17/f_S. The –3-dB bandwidth of the decimation filter extends to 0.45 f_S and scales with the sample rate (f_S). The filter has minimum 75-dB attenuation over the stop band from 0.55 f_S to 64 f_S. Independent digital high-pass filters are also included with each ADC channel, with a corner frequency that can be independently set.

Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog antialiasing filtering are very relaxed. The TLV320AIC3106 integrates a second-order analog antialiasing filter with 20-dB attenuation at 1 MHz. This filter, combined with the digital decimation filter, provides sufficient antialiasing filtering without requiring additional external components.

The ADC is preceded by a programmable gain amplifier (PGA), which allows analog gain control from 0 dB to 59.5 dB in steps of 0.5 dB. The PGA gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register programming (see page 0, registers 19 and 22). This soft-stepping ensures that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and on power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag is set whenever the gain applied by PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming a register bit. When soft stepping is enabled, the audio master clock must be applied to the part after the ADC power-down register is written to ensure the soft-stepping to mute has completed. When the ADC power-down flag is no longer set, the audio master clock can be shut down.

10.3.3.2.1 Stereo Audio ADC High-Pass Filter

Often in audio applications it is desirable to remove the dc offset from the converted audio data stream. The TLV320AIC3106 has a programmable first-order high-pass filter which can be used for this purpose. The digital filter coefficients are in 16-bit format and therefore use two 8-bit registers for each of the three coefficients, N0, N1, and D1. The transfer function of the digital high-pass filter is of the form:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32,768 - D1 \times z^{-1}} \tag{5}$$

Programming the left channel is done by writing to page 1, registers 65–70, and the right channel is programmed by writing to page 1, registers 71–76. After the coefficients have been loaded, these ADC high-pass filter coefficients can be selected by writing to page 0, register 107, bits D7–D6, and the high-pass filter can be enabled by writing to page 0, register 12, bits D7–D4.

10.3.3.2.2 Automatic Gain Control (AGC)

An automatic gain control (AGC) circuit is included with the ADC and can be used to maintain nominally constant output signal amplitude when recording speech signals (it can be fully disabled if not desired). This circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable settings, including target gain, attack and decay time constants, noise threshold, and maximum PGA gain applicable that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal.

Note that completely independent AGC circuitry is included with each ADC channel with entirely independent control over the algorithm from one channel to the next. This is attractive in cases where two microphones are used in a system, but may have different placement in the end equipment and require different dynamic performance for optimal system operation.

10.3.3.2.2.1 Target Level

The target level represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320AIC3106 allows programming of eight different target levels, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Since the device reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.

10.3.3.2.2.2 Attack Time

The Attack time determines how quickly the AGC circuitry reduces the PGA gain when the input signal is too loud. It can be varied from 7 ms to 1,408 ms. The extended Right Channel Attack time can be programmed by writing to Page 0, Registers 103, and Left Channel is programmed by writing to Page 0, Register 105.

10.3.3.2.2.3 Decay Time

The decay time determines how quickly the PGA gain is increased when the input signal is too low. It can be varied in the range from 0.05 s to 22.4 s. The extended Right Channel Decay time can be programmed by writing to Page 0, Registers 104, and Left Channel is programmed by writing to Page 0, Register 106.

The actual AGC decay time maximum is based on a counter length, so the maximum decay time will scale with the clock set up that is used. 表 10-2 shows the relationship of the NADC ratio to the maximum time available for the AGC decay. In practice, these maximum times are extremely long for audio applications and should not limit any practical AGC decay time that is needed by the system.

表 10-2. AGC Decay Time Restriction

NADC RATIO	MAXIMUM DECAY TIME (seconds)
1.0	4.0
1.5	5.6
2.0	8.0
2.5	9.6
3.0	11.2
3.5	11.2
4.0	16.0
4.5	16.0
5.0	19.2
5.5	22.4
6.0	22.4

10.3.3.2.2.4 Noise Gate Threshold

The noise gate threshold determines the level below which if the input speech average value falls, AGC considers it as a silence and hence brings down the gain to 0 dB in steps of 0.5 dB every FS and sets the noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This ensures that noise does not get gained up in the absence of speech. Noise threshold level in the AGC algorithm is programmable from –30 dB to –90 dB relative to full scale. A disable noise gate feature is also available. This operation includes programmable debounce and hysteresis functionality to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. When the noise threshold flag is set, the status of gain applied by the AGC and the saturation flag should be ignored.

10.3.3.2.2.5 Maximum PGA Gain Applicable

Maximum PGA gain applicable allows the user to restrict the maximum PGA gain that can be applied by the AGC algorithm. This can be used for limiting PGA gain in situations where environmental noise is greater than programmed noise threshold. It can be programmed from 0 dB to 59.5 dB in steps of 0.5 dB.

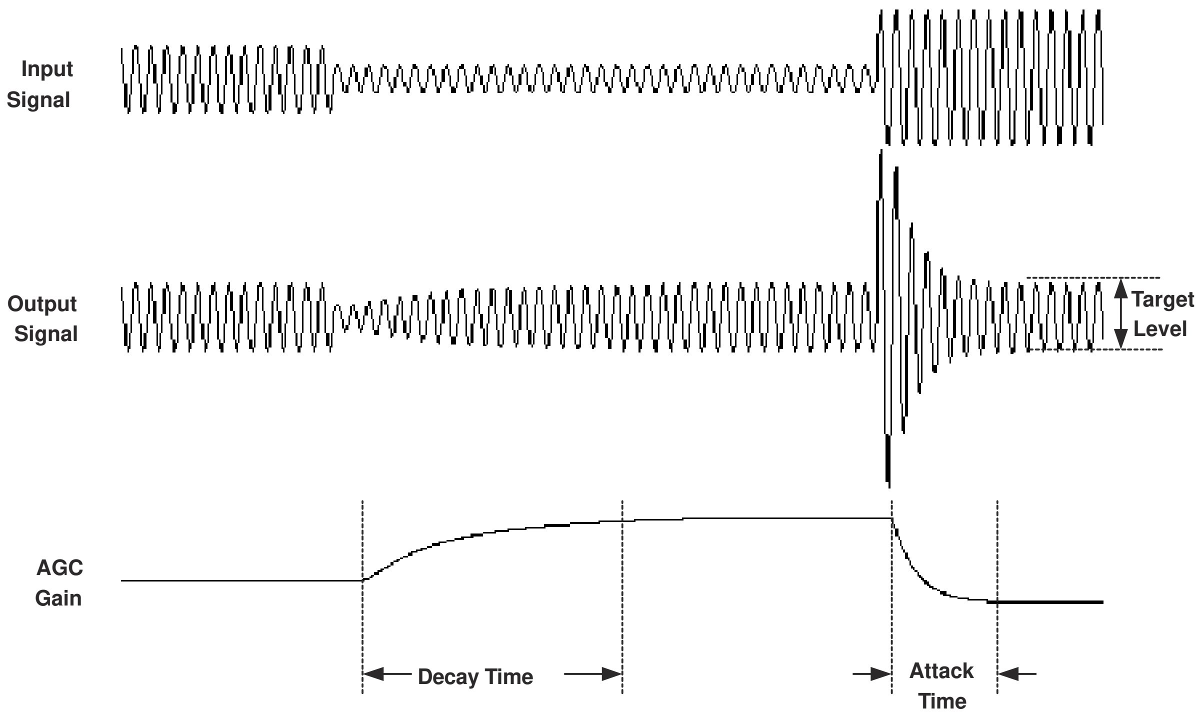


図 10-9. Typical Operation of the AGC Algorithm During Speech Recording

Note that the time constants here are correct when the ADC is not in double-rate audio mode. The time constants are achieved using the $f_{S(ref)}$ value programmed in the control registers. However, if the $f_{S(ref)}$ is set in the registers to, for example, 48 kHz, but the actual audio clock or PLL programming actually results in a different $f_{S(ref)}$ in practice, then the time constants would not be correct.

The actual AGC decay time maximum is based on a counter length, so the maximum decay time scales with the clock set up that is used. 表 10-2 shows the relationship of the NADC ratio to the maximum time available for the AGC decay. In practice, these maximum times are extremely long for audio applications and should not limit any practical AGC decay time that is needed by the system.

10.3.3.3 Stereo Audio DAC

The TLV320AIC3106 includes a stereo audio DAC supporting sampling rates from 8 kHz to 96 kHz. Each channel of the stereo audio DAC consists of a digital audio processing block, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20 kHz. This is realized by keeping the upsampled rate constant at 128 × $f_{S(ref)}$ and changing the oversampling ratio as the input sample rate is changed. For an $f_{S(ref)}$ of 48 kHz, the digital delta-sigma modulator always operates at a rate of 6.144 MHz. This ensures that quantization noise generated within the delta-sigma modulator stays low within the frequency band below 20 kHz at all sample rates. Similarly, for an $f_{S(ref)}$ rate of 44.1 kHz, the digital delta-sigma modulator always operates at a rate of 5.6448 MHz.

The following restrictions apply in the case when the PLL is powered down and double-rate audio mode is enabled in the DAC.

Allowed Q values = 4, 8, 9, 12, 16

Q values where equivalent $f_{S(ref)}$ can be achieved by turning on PLL

Q = 5, 6, 7 (set P = 5 / 6 / 7 and K = 16.0 and PLL enabled)

Q = 10, 14 (set P = 5, 7 and K = 8.0 and PLL enabled)

10.3.3.3.1 Digital Audio Processing for Playback

The DAC channel consists of optional filters for de-emphasis and bass, treble, midrange level adjustment, speaker equalization, and 3-D effects processing. The de-emphasis function is implemented by a programmable digital filter block with fully programmable coefficients (see Page-1/Reg-21-26 for left channel, Page-1/Reg-47-52 for right channel). If de-emphasis is not required in a particular application, this programmable filter block can be used for some other purpose. The de-emphasis filter transfer function is given by:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32768 - D1 \times z^{-1}} \tag{6}$$

where the N0, N1, and D1 coefficients are fully programmable individually for each channel. The coefficients that should be loaded to implement standard de-emphasis filters are given in 表 10-3.

表 10-3. De-Emphasis Coefficients for Common Audio Sampling Rates

SAMPLING FREQUENCY	N0	N1	D1
32-kHz	16950	–1220	17037
44.1-kHz	15091	–2877	20555
48-kHz(1)	14677	–3283	21374

(1) The 48-kHz coefficients listed in 表 10-3 are used as defaults.

In addition to the de-emphasis filter block, the DAC digital effects processing includes a fourth order digital IIR filter with programmable coefficients (one set per channel). This filter is implemented as cascade of two biquad sections with frequency response given by:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right) \tag{7}$$

The N and D coefficients are fully programmable, and the entire filter can be enabled or bypassed. The structure of the filtering when configured for independent channel processing is shown below in 図 10-10, with LB1 corresponding to the first left-channel biquad filter using coefficients N0, N1, N2, D1, and D2. LB2 similarly corresponds to the second left-channel biquad filter using coefficients N3, N4, N5, D4, and D5. The RB1 and RB2 filters refer to the first and second right-channel biquad filters, respectively.

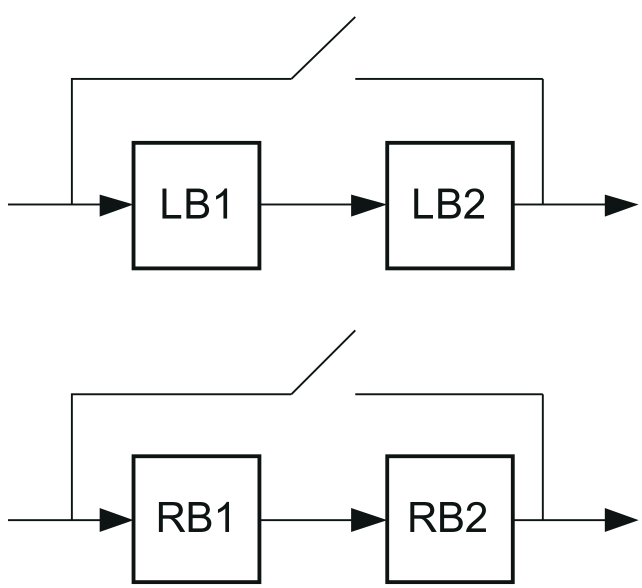


図 10-10. Structure of the Digital Effects Processing for Independent Channel Processing

The coefficients for this filter implement a variety of sound effects, with bass-boost or treble boost being the most commonly used in portable audio applications. The default N and D coefficients in the part are given in 表 10-4 and implement a shelving filter with 0-dB gain from DC to approximately 150 Hz, at which point it rolls off to a 3-dB attenuation for higher frequency signals, thus giving a 3-dB boost to signals below 150 Hz. The N and D coefficients are represented by 16-bit two's complement numbers with values ranging from –32768 to 32767.

表 10-4. Default Digital Effects Processing Filter Coefficients, When in Independent Channel Processing Configuration

Coefficients				
N0 = N3	D1 = D4	N1 = N4	D2 = D5	N2 = N5
27,619	32,131	–27,034	–31,506	26,461

The digital processing also includes capability to implement 3-D processing algorithms by providing means to process the mono mix of the stereo input, and then combine this with the individual channel signals for stereo output playback. The architecture of this processing mode, and the programmable filters available for use in the system, is shown in 図 10-11. Note that the programmable attenuation block provides a method of adjusting the level of 3-D effect introduced into the final stereo output. This combined with the fully programmable biquad filters in the system enables the user to fully optimize the audio effects for a particular system and provide extensive differentiation from other systems using the same device.

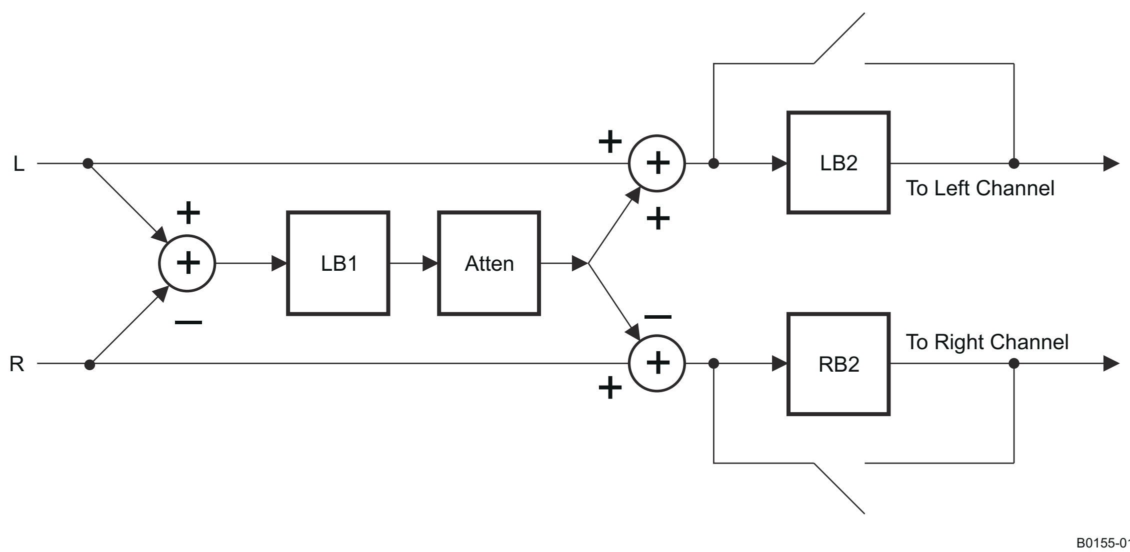


図 10-11. Architecture of the Digital Audio Processing When 3-D Effects are Enabled

It is recommended that the digital effects filters should be disabled while the filter coefficients are being modified. While new coefficients are being written to the device over the control port, it is possible that a filter using partially updated coefficients may actually implement an unstable system and lead to oscillation or objectionable audio output. By disabling the filters, changing the coefficients, and then re-enabling the filters, these types of effects can be entirely avoided.

10.3.3.3.2 Digital Interpolation Filter

The digital interpolation filter upsamples the output of the digital audio processing block by the required oversampling ratio before data is provided to the digital delta-sigma modulator and analog reconstruction filter stages. The filter provides a linear phase output with a group delay of $21/f_S$. In addition, programmable digital interpolation filtering is included to provide enhanced image filtering and reduce signal images caused by the upsampling process that are below 20 kHz. For example, upsampling an 8-kHz signal produces signal images at multiples of 8-kHz (i.e., 8 kHz, 16 kHz, 24 kHz, etc.). The images at 8 kHz and 16 kHz are below 20 kHz and still audible to the listener; therefore, they must be filtered heavily to maintain a good quality output. The interpolation filter is designed to maintain at least 65-dB rejection of images that land below 7.455 f_S. In order to utilize the programmable interpolation capability, the $f_{S(ref)}$ should be programmed to a higher rate (restricted to be in the range of 39 kHz to 53 kHz when the PLL is in use), and the actual f_S is set using the NDAC divider. For example, if f_S = 8 kHz is required, then $f_{S(ref)}$ can be set to 48 kHz, and the DAC f_S set to $f_{S(ref)}/6$. This ensures that all images of the 8-kHz data are sufficiently attenuated well beyond a 20-kHz audible frequency range.

10.3.3.3.3 Delta-Sigma Audio DAC

The stereo audio DAC incorporates a third order multi-bit delta-sigma modulator followed by an analog reconstruction filter. The DAC provides high-resolution, low-noise performance, using oversampling and noise shaping techniques. The analog reconstruction filter design consists of a 6-tap analog FIR filter followed by a continuous time RC filter. The analog FIR operates at a rate of 128 × $f_{S(ref)}$ (6.144 MHz when $f_{S(ref)}$ = 48 kHz, 5.6448 MHz when $f_{S(ref)}$ = 44.1 kHz). Note that the DAC analog performance may be degraded by excessive clock jitter on the MCLK input. Therefore, care must be taken to keep jitter on this clock to a minimum.

10.3.3.3.4 Audio DAC Digital Volume Control

The audio DAC includes a digital volume control block which implements a programmable digital gain. The volume level can be varied from 0 dB to –63.5 dB in 0.5-dB steps, in addition to a mute bit, independently for each channel. The volume level of both channels can also be changed simultaneously by the master volume control. Gain changes are implemented with a soft-stepping algorithm, which only changes the actual volume by one step per input sample, either up or down, until the desired volume is reached. The rate of soft-stepping can be slowed to one step per two input samples through a register bit.

Because of soft-stepping, the host does not know when the DAC has been actually muted. This may be important if the host wishes to mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the device provides a flag back to the host via a read-only register bit that alerts the host when the part has completed the soft-stepping and the actual volume has reached the desired volume level. The soft-stepping feature can be disabled through register programming. If soft-stepping is enabled, the MCLK signal should be kept applied to the device until the DAC power-down flag is set. When this flag is set, the internal soft-stepping process and power down sequence is complete, and the MCLK can then be stopped if desired.

The TLV320AIC3106 also includes functionality to detect when the user switches on or off the de-emphasis or digital audio processing functions, to first (1) soft-mute the DAC volume control, (2) change the operation of the digital effects processing, and (3) soft-unmute the part. This avoids any possible pop/clicks in the audio output due to instantaneous changes in the filtering. A similar algorithm is used when first powering up or down the DAC. The circuit begins operation at power up with the volume control muted, then soft-steps it up to the desired volume level. At power down, the logic first soft-steps the volume down to a mute level, then powers down the circuitry.

10.3.3.3.5 Increasing DAC Dynamic Range

The TLV320AIC3106 allows trading off dynamic range with power consumption. The DAC dynamic range can be increased by writing to Page 0, Register 109 bits D7-D6. The lowest DAC current setting is the default, and the dynamic range is displayed in the datasheet table. Increasing the current can increase the DAC dynamic range by up to 1.5dB.

10.3.3.3.6 Analog Output Common-Mode Adjustment

The output common-mode voltage and output range of the analog output are determined by an internal bandgap reference, in contrast to other codecs that may use a divided version of the supply. This scheme is used to reduce the coupling of noise that may be on the supply (such as 217-Hz noise in a GSM cellphone) into the audio signal path.

However, due to the possible wide variation in analog supply range (2.7 V – 3.6 V), an output common-mode voltage setting of 1.35 V, which would be used for a 2.7 V supply case, will be overly conservative if the supply is actually much larger, such as 3.3 V or 3.6 V. In order to optimize device operation, the TLV320AIC3106 includes a programmable output common-mode level, which can be set by register programming to a level most appropriate to the actual supply range used by a particular customer. The output common-mode level can be varied among four different values, ranging from 1.35 V (most appropriate for low supply ranges, near 2.7 V) to 1.8 V (most appropriate for high supply ranges, near 3.6 V). Note that there is also some limitation on the range of DVDD voltage as well in determining which setting is most appropriate.

表 10-5. Appropriate Settings

CM SETTING	RECOMMENDED AVDD_DAC, DRVDD	RECOMMENDED DVDD
1.35	2.7 V – 3.6 V	1.65 V – 1.95 V
1.50	3.0 V – 3.6 V	1.65 V – 1.95 V
1.65 V	3.3 V – 3.6 V	1.8 V – 1.95 V
1.8 V	3.6 V	1.95 V

10.3.3.3.7 Audio DAC Power Control

The stereo DAC can be fully powered up or down, and in addition, the analog circuitry in each DAC channel can be powered up or down independently. This provides power savings when only a mono playback stream is needed.

10.3.4 Audio Analog Inputs

The TLV320AIC3106 includes ten analog audio input pins, which can be configured as up to four fully-differential pair plus one single-ended pair of audio inputs, or up to six single-ended audio inputs. . These pins connect through series resistors and switches to the virtual ground terminals of two fully differential opamps (one per ADC/PGA channel). By selecting to turn on only one set of switches per opamp at a time, the inputs can be effectively muxed to each ADC PGA channel.

By selecting to turn on multiple sets of switches per opamp at a time, mixing can also be achieved. Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal opamps, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, the user should take adequate precautions to avoid such a saturation case from occurring. In general, the mixed signal should not exceed 2 V_{pp} (single-ended) or 4 V_{pp} (differential).

In most mixing applications, there is also a general need to adjust the levels of the individual signals being mixed. For example, if a soft signal and a large signal are to be mixed and played together, the soft signal generally should be amplified to a level comparable to the large signal before mixing. In order to accommodate this need, the TLV320AIC3106 includes input level control on each of the individual inputs before they are mixed or muxed into the ADC PGAs, with gain programmable from 0 dB to –12 dB in 1.5 dB steps. Note that this input level control is not intended to be a volume control, but instead used occasionally for level setting. Soft-stepping of the input level control settings is implemented in this device, with the speed and functionality following the settings used by the ADC PGA for soft-stepping.

The TLV320AIC3106 supports the ability to mix up to three fully-differential analog inputs into each ADC PGA channel. 図 10-12 shows the mixing configuration for the left channel, which can mix the signals LINE1LP-LINE1LM, LINE2LP-LINE2LM, and LINE1RP-LINE1RM.

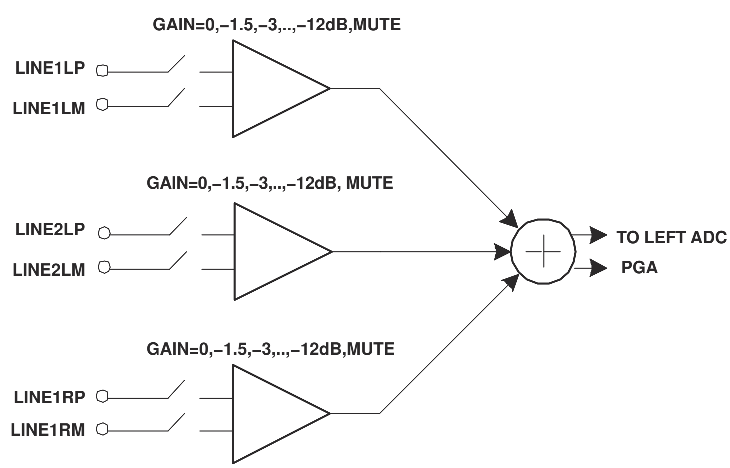


図 10-12. Left Channel Fully-Differential Analog Input Mixing Configuration

Three fully-differential analog inputs can similarly be mixed into the right ADC PGA as well, consisting of LINE1RP-LINE1RM, LINE2RP-LINE2RM, and LINE1LP-LINE1LM. Note that it is not necessary to mix all three fully-differential signals if this is not desired – unnecessary inputs can simply be muted using the input level control registers.

Inputs can also be selected as single-ended instead of fully-differential, and mixing or muxing into the ADC PGAs is also possible in this mode. It is not possible, however, for an input pair to be selected as fully-differential for connection to one ADC PGA and simultaneously selected as single-ended for connection to the other ADC PGA channel. However, it is possible for an input to be selected or mixed into both left and right channel PGAs, as long as it has the same configuration for both channels (either both single-ended or both fully-differential).

図 10-13 shows the single-ended mixing configuration for the left channel ADC PGA, which enables mixing of the signals LINE1LP, LINE2LP, LINE1RP, MIC3L, and MIC3R. The right channel ADC PGA mix is similar, enabling mixing of the signals LINE1RP, LINE2RP, LINE1LP, MIC3L, and MIC3R.

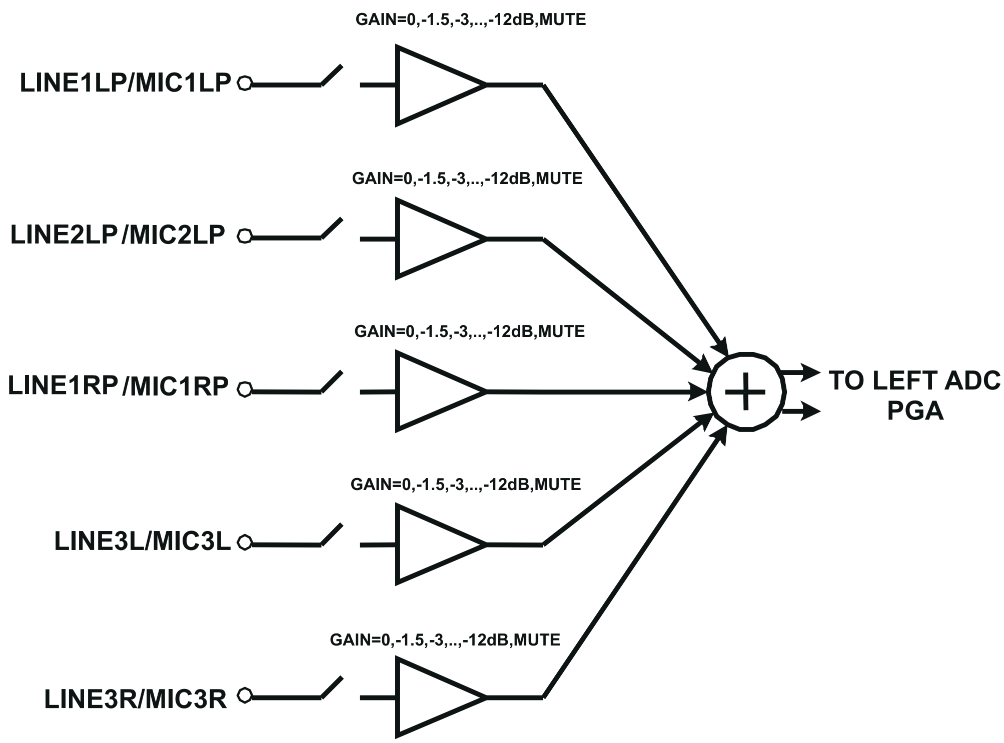


図 10-13. Left Channel Single-Ended Analog Input Mixing Configuration

10.3.5 Analog Fully Differential Line Output Drivers

The TLV320AIC3106 has two fully differential line output drivers, each capable of driving a 10-kΩ differential load. The output stage design leading to the fully differential line output drivers is shown in 図 10-14 and 図 10-15. This design includes extensive capability to adjust signal levels independently before any mixing occurs, beyond that already provided by the PGA gain and the DAC digital volume control.

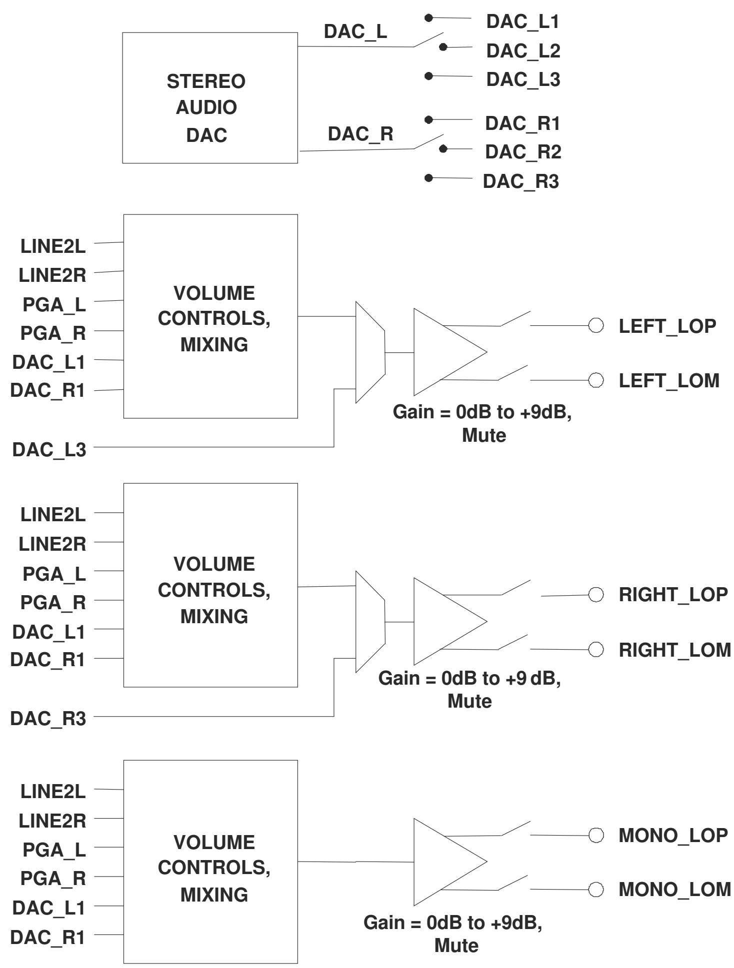


図 10-14. Architecture of the Output Stage Leading to the Fully Differential Line Output Drivers

The LINE2L/R signals refer to the signals that travel through the analog input bypass path to the output stage. The PGA_L/R signals refer to the outputs of the ADC PGA stages that are similarly passed around the ADC to the output stage. Note that since both left and right channel signals are routed to all output drivers, a mono mix of any of the stereo signals can easily be obtained by setting the volume controls of both left and right channel signals to –6 dB and mixing them. Undesired signals can also be disconnected from the mix as well through register control.

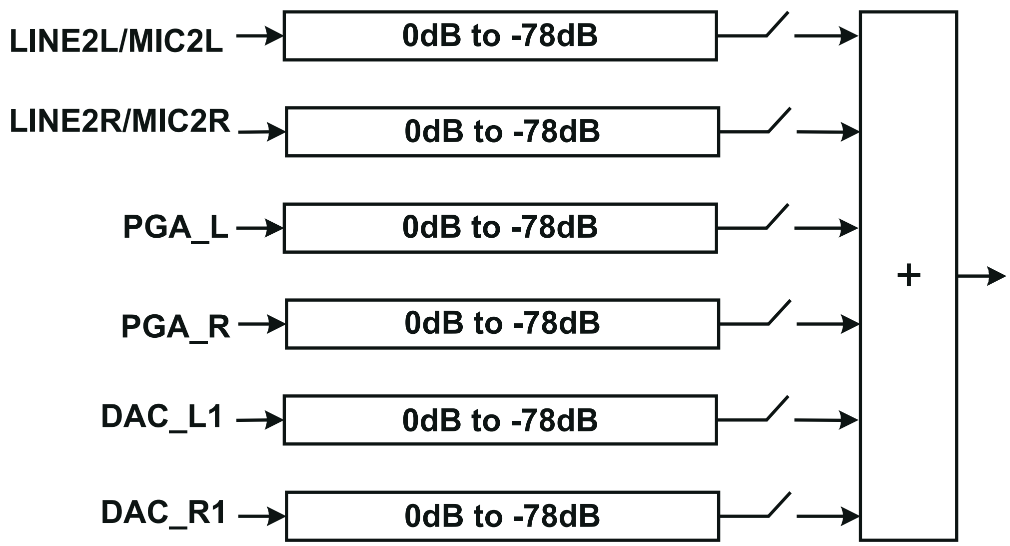


図 10-15. Detail of the Volume Control and Mixing Function Shown in 図 10-10 and 図 10-25

The DAC_L/R signals are the outputs of the stereo audio DAC, which can be steered by register control based on the requirements of the system. If mixing of the DAC audio with other signals is not required, and the DAC output is only needed at the stereo line outputs, then it is recommended to use the routing through path DAC_L3/R3 to the fully differential stereo line outputs. This results not only in higher quality output performance, but also in lower power operation, since the analog volume controls and mixing blocks ahead of these drivers can be powered down.

If instead the DAC analog output must be routed to multiple output drivers simultaneously (such as to LEFT_LOP/M, RIGHT_LOP/M, and MONO_LOP/M) or must be mixed with other analog signals, then the DAC outputs should be switched through the DAC_L1/R1 path. This option provides the maximum flexibility for routing of the DAC analog signals to the output drivers

The TLV320AIC3106 includes an output level control on each output driver with limited gain adjustment from 0 dB to 9 dB. The output driver circuitry in this device are designed to provide a low distortion output while playing fullscale stereo DAC signals at a 0dB gain setting. However, a higher amplitude output can be obtained at the cost of increased signal distortion at the output. This output level control allows the user to make this tradeoff based on the requirements of the end equipment. Note that this output level control is not intended to be used as a standard output volume control. It is expected to be used only sparingly for level setting, that is, adjustment of the fullscale output range of the device.

The PGA_L/R signals refer to the outputs of the ADC PGA stages that are similarly passed around the ADC to the output stage. Note that because both left- and right-channel signals are routed to all output drivers, a mono mix of any of the stereo signals can easily be obtained by setting the volume controls of both left- and right-channel signals to –6 dB and mixing them. Undesired signals can also be disconnected from the mix as well through register control.

10.3.6 Analog High Power Output Drivers

The TLV320AIC3106 includes four high power output drivers with extensive flexibility in their usage. These output drivers are individually capable of driving 30 mW each into a 16-Ω load in single-ended configuration, and they can be used in pairs connected in bridge-terminated load (BTL) configuration between two driver outputs.

The high power output drivers can be configured in a variety of ways, including:

1. driving up to two fully differential output signals
2. driving up to four single-ended output signals
3. driving two single-ended output signals, with one or two of the remaining drivers driving a fixed VCM level, for a pseudo-differential stereo output

The output stage architecture leading to the high power output drivers is shown in 図 10-16, with the volume control and mixing blocks being effectively identical to that shown in 図 10-15. Note that each of these drivers have a output level control block like those included with the line output drivers, allowing gain adjustment up to +9dB on the output signal. As in the previous case, this output level adjustment is not intended to be used as a standard volume control, but instead is included for additional fullscale output signal level control.

Two of the output drivers, HPROUT and HPLOUT, include a direct connection path for the stereo DAC outputs to be passed directly to the output drivers and bypass the analog volume controls and mixing networks, using the DAC_L2/R2 path. As in the line output case, this functionality provides the highest quality DAC playback performance with reduced power dissipation, but can only be utilized if the DAC output does not need to route to multiple output drivers simultaneously, and if mixing of the DAC output with other analog signals is not needed.

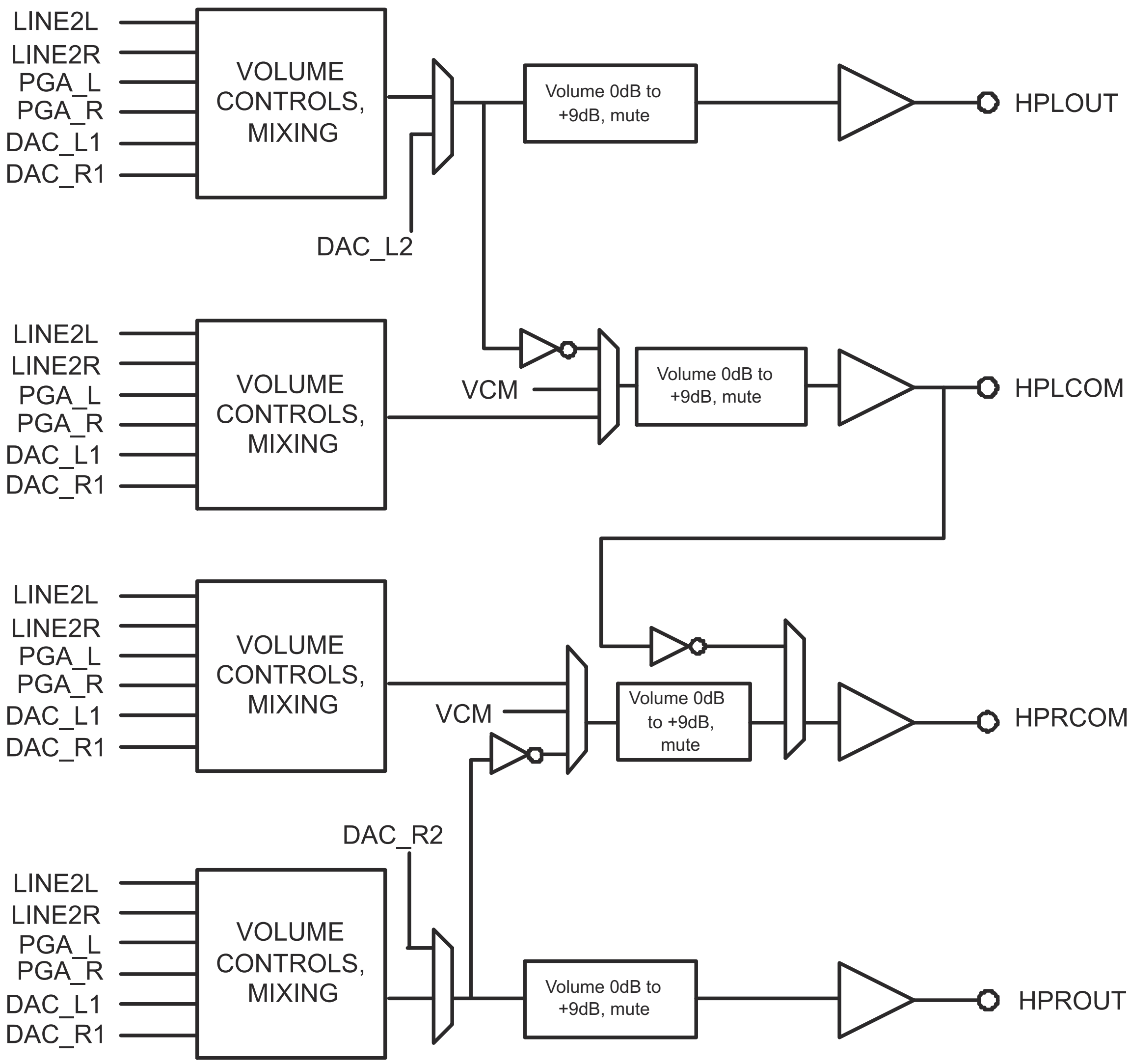


図 10-16. Architecture of the Output Stage Leading to the High Power Output Drivers

The high power output drivers include additional circuitry to avoid artifacts on the audio output during power-on and power-off transient conditions. The user should first program the type of output configuration being used in Page-0/Reg-14, to allow the device to select the optimal power-up scheme to avoid output artifacts. The power-up delay time for the high power output drivers is also programmable over a wide range of time delays, from instantaneous up to 4-sec, using Page-0/Reg-42.

When these output drivers are powered down, they can be placed into a variety of output conditions based on register programming. If lowest power operation is desired, then the outputs can be placed into a 3-state condition, and all power to the output stage is removed. However, this generally results in the output nodes drifting to rest near the upper or lower analog supply, due to small leakage currents at the pins. This then results in a longer delay requirement to avoid output artifacts during driver power-on. In order to reduce this required power-on delay, the TLV320AIC3106 includes an option for the output pins of the drivers to be weakly driven to the VCM level they would normally rest at when powered with no signal applied. This output VCM level is determined by an internal bandgap voltage reference, and thus results in extra power dissipation when the drivers are in powerdown. However, this option provides the fastest method for transitioning the drivers from powerdown to full power operation without any output artifact introduced.

The device includes a further option that falls between the other two – while it requires less power drawn while the output drivers are in powerdown, it also takes a slightly longer delay to power-up without artifact than if the bandgap reference is kept alive. In this alternate mode, the powered-down output driver pin is weakly driven to a voltage of approximately half the DRVDD1/2 supply level using an internal voltage divider. This voltage will not match the actual VCM of a fully powered driver, but due to the output voltage being close to its final value, a much shorter power-up delay time setting can be used and still avoid any audible output artifacts. These output voltage options are controlled in Page-0/Reg-42.

The high power output drivers can also be programmed to power up first with the output level control in a highly attenuated state, then the output driver will automatically slowly reduce the output attenuation to reach the desired output level setting programmed. This capability is enabled by default but can be enabled in Page-0/Reg-40.

10.3.7 Input Impedance and VCM Control

The TLV320AIC3106 includes several programmable settings to control analog input pins, particularly when they are not selected for connection to an ADC PGA. The default option allows unselected inputs to be put into a 3-state condition, such that the input impedance seen looking into the device is extremely high. Note, however, that the pins on the device do include protection diode circuits connected to AVDD and AVSS. Thus, if any voltage is driven onto a pin approximately one diode drop (~0.6 V) above AVDD or one diode drop below AVSS, these protection diodes will begin conducting current, resulting in an effective impedance that no longer appears as a 3-state condition.

Another programmable option for unselected analog inputs is to weakly hold them at the common-mode input voltage of the ADC PGA (which is determined by an internal bandgap voltage reference). This is useful to keep the ac-coupling capacitors connected to analog inputs biased up at a normal DC level, thus avoiding the need for them to charge up suddenly when the input is changed from being unselected to selected for connection to an ADC PGA. This option is controlled in Page-0/Reg-20 and 23. The user should ensure this option is disabled when an input is selected for connection to an ADC PGA or selected for the analog input bypass path, since it can corrupt the recorded input signal if left operational when an input is selected.

In most cases, the analog input pins on the TLV320AIC3106 should be ac-coupled to analog input sources, the only exception to this generally being if an ADC is being used for DC voltage measurement. The ac-coupling capacitor will cause a highpass filter pole to be inserted into the analog signal path, so the size of the capacitor must be chosen to move that filter pole sufficiently low in frequency to cause minimal effect on the processed analog signal. The input impedance of the analog inputs when selected for connection to an ADC PGA varies with the setting of the input level control, starting at approximately 20 kΩ with an input level control setting of 0-dB, and increasing to approximately 80-kΩ when the input level control is set at –12 dB. For example, using a 0.1 µF ac-coupling capacitor at an analog input results in a highpass filter pole of 80 Hz when the 0 dB input level control setting is selected.

10.3.8 General-Purpose I/O

TLV320AIC3106 has two dedicated pins for general-purpose I/O. These pins can be used to read status of external signals through register read when configured as general-purpose input. When configured as general-purpose output , these pins can also drive logic high or low. Besides these standard GPIO functions, these pins can also be used in a variety of ways, such as output for internal clocks and interrupt signals. The TLV320AIC3106 generates a variety of interrupts of use to the host processor such interrupts on jack detection, button press, short-circuit detection, and AGC noise detection. All these interrupts can be routed individually to the GPIO pins or can be combined by a logical OR. In case of a combined interrupt, the user can read an internal status register to find the actual cause of interrupt. When configured as interrupt, the TLV320AIC3106 also offers the flexibility of generating a single pulse or a train of pulses until the interrupt status register is read by the user.

10.3.9 Digital Microphone Connectivity

The TLV320AIC3106 includes support for connection of a digital microphone to the device by routing the digital signal directly into the ADC digital decimation filter, where it is filtered, downsampled, and provided to the host processor over the audio data serial bus.

When digital microphone mode is enabled, the TLV320AIC3106 provides an oversampling clock output for use by the digital microphone to transmit its data. The TLV320AIC3106 includes the capability to latch the data on either the rising, falling, or both edges of this supplied clock, enabling support for stereo digital microphones.

In this mode, the oversampling ratio of the digital mic modulator can be programmed as 128, 64 or 32 times the ADC sample rate, ADCFS. The GPIO1 pin will output the serial oversampling clock at the programmed rate. TLV320AIC3106 latches the data input on GPIO2 as the Left and Right channel digital microphone data. For the Left channel input, GPIO2 will be sampled on the rising edge of the clock, and for the Right channel input, GPIO2 will be sampled on the falling edge of the clock. If a single digital mic channel is needed then the corresponding ADC channel should be powered up, and the unused channel should be powered down. When digital microphone mode is enabled, neither ADC can be used for digitizing analog inputs.

Configuring the digital microphone configuration set up is done by writing to Page 0, Register 107, bits D5-D4, and Register 25, bits D5-D4.

10.3.10 Micbias Generation

The TLV320AIC3106 includes a programmable microphone bias output voltage (MICBIAS), capable of providing output voltages of 2.0 V or 2.5 V (both derived from the on-chip bandgap voltage) with 4-mA output current drive. In addition, the MICBIAS may be programmed to be switched to AVDD directly through an on-chip switch, or it can be powered down completely when not needed, for power savings. This function is controlled by register programming in Page-0/Reg-25.

10.3.11 Short Circuit Output Protection

The TLV320AIC3106 includes programmable short-circuit protection for the high power output drivers, for maximum flexibility in a given application. By default, if these output drivers are shorted, they will automatically limit the maximum amount of current that can be sourced to or sunk from a load, thereby protecting the device from an over-current condition. In this mode, the user can read Page-0/Reg-95 to determine whether the part is in short-circuit protection or not, and then decide whether to program the device to power down the output drivers. However, the device includes further capability to automatically power down an output driver whenever it does into short-circuit protection, without requiring intervention from the user. In this case, the output driver will stay in a power down condition until the user specifically programs it to power down and then power back up again, to clear the short-circuit flag.

10.3.12 Jack/Headset Detection

The TLV320AIC3106 includes extensive capability to monitor a headphone, microphone, or headset jack, determine if a plug has been inserted into the jack, and then determine what type of headset/headphone is wired to the plug. 図 10-17 shows one configuration of the device that enables detection and determination of headset type when a pseudo-differential (capless) stereo headphone output configuration is used. The registers used for this function are page 0, registers 14, 96, 97, and 13. The type of headset detected can be read back from page 0, register 13. Note that for best results, it is recommended to select a MICBIAS value as high as possible, and to program the output driver common-mode level at a 1.35-V or 1.5-V level.

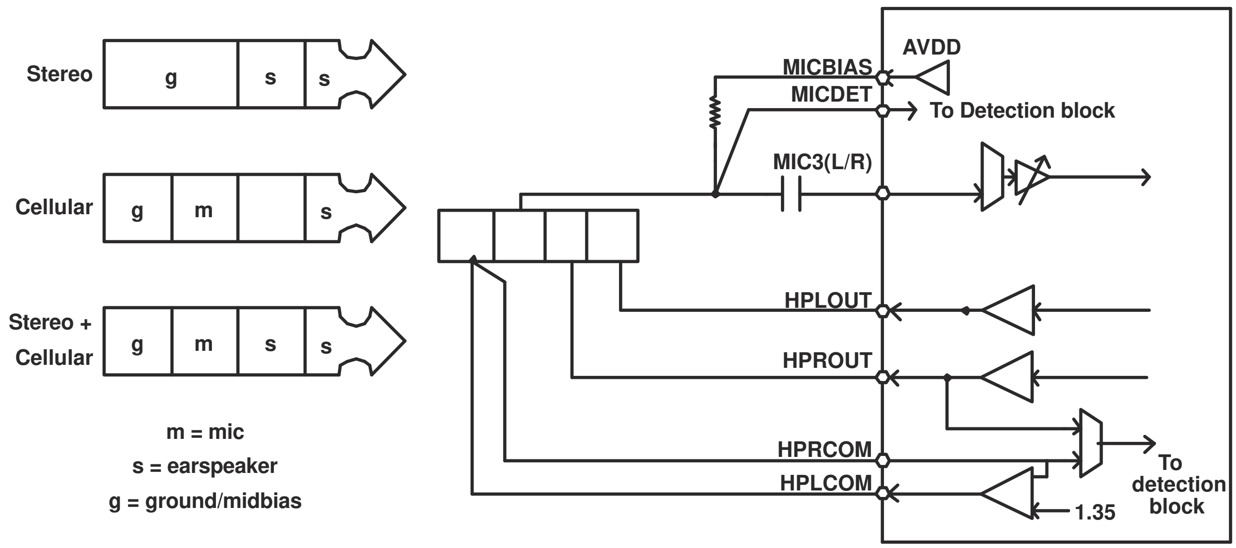


図 10-17. Configuration of Device for Jack Detection Using a Pseudo-Differential (Capless) Headphone Output Connection

A modified output configuration used when the output drivers are ac-coupled is shown in 図 10-18. Note that in this mode, the device cannot accurately determine if the inserted headphone is a mono or stereo headphone.

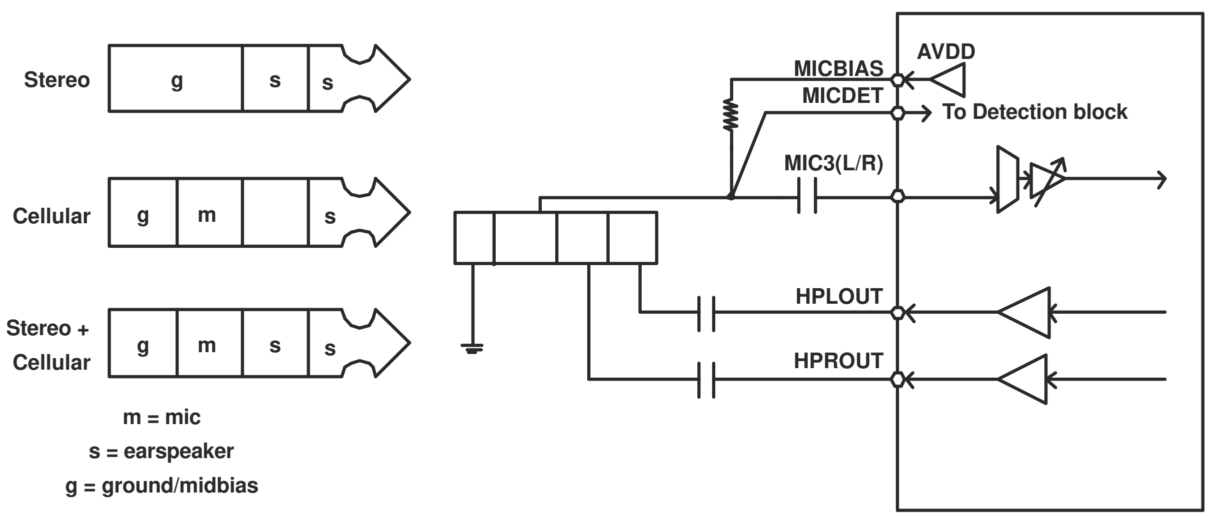


図 10-18. Configuration of Device for Jack Detection Using an AC-Coupled Stereo Headphone Output Connection

An output configuration for the case of the outputs driving fully differential stereo headphones is shown in 図 10-19. In this mode, there is a requirement on the jack side that either HPLCOM or HPLOUT get shorted to ground if the plug is removed, which can be implemented using a spring terminal in a jack. For this mode to function properly, short-circuit detection should be enabled and configured to power down the drivers if a short-circuit is detected. The registers that control this functionality are in page 0, register 38, bits D2–D1.

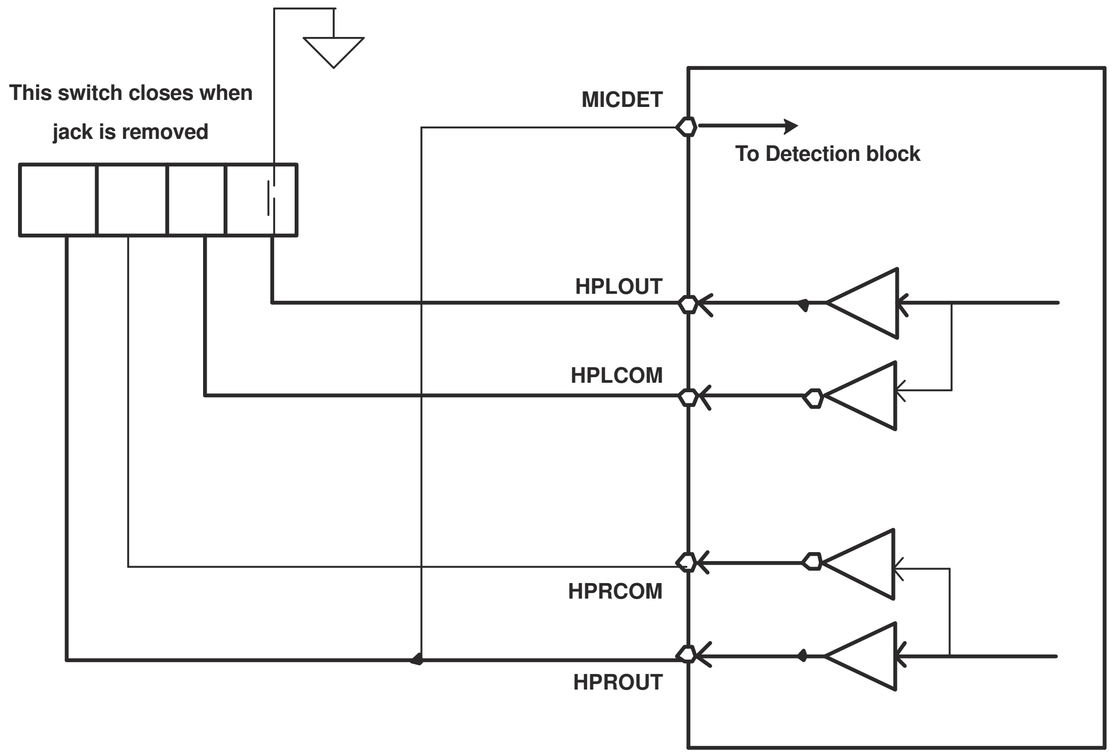


図 10-19. Configuration of Device for Jack Detection Using a Fully Differential Stereo Headphone Output Connection

10.4 Device Functional Modes

10.4.1 Bypass Path Mode

The TLV320AIC3106 is a versatile device designed for low-power applications. In some cases, only a few features of the device are required. For these applications, the unused stages of the device must be powered down to save power and an alternate route should be used. This is called a bypass path. The bypass path modes let the device to save power by turning off unused stages, like ADC, DAC and PGA.

10.4.1.1 Analog Input Bypass Path Functionality

The TLV320AIC3106 includes the additional ability to route some analog input signals past the integrated data converters, for mixing with other analog signals and then direct connection to the output drivers. This capability is useful in a cellphone, for example, when a separate FM radio device provides a stereo analog output signal that needs to be routed to headphones. The TLV320AIC3106 supports this in a low power mode by providing a direct analog path through the device to the output drivers, while all ADCs and DACs can be completely powered down to save power.

For fully-differential inputs, the TLV320AIC3106 provides the ability to pass the signals LINE2LP-LINE2LM and LINE2RP-LINE2RM to the output stage directly. If in single-ended configuration, the device can pass the signal LINE2LP and LINE2RP to the output stage directly.

10.4.1.2 ADC PGA Signal Bypass Path Functionality

In addition to the input bypass path described above, the TLV320AIC3106 also includes the ability to route the ADC PGA output signals past the ADC, for mixing with other analog signals and then direct connection to the output drivers. These bypass functions are described in more detail in the sections on output mixing and output driver configurations.

10.4.1.3 Passive Analog Bypass During Powerdown

Programming the TLV320AIC3106 to Passive Analog bypass occurs by configuring the output stage switches for pass through. This is done by opening switches SW-L0, SW-L3, SW-R0, SW-R3 and closing either SW-L1 or

SW-L2 and SW-R1 or SW-R2. See 図 10-20 Passive Analog Bypass Mode Configuration. Programming this mode is done by writing to Page 0, Register 108.

Connecting MIC1LP/LINE1LP input signal to the LEFT_LOP pin is done by closing SW-L1 and opening SW-L0, this action is done by writing a “1” to Page 0, Register 108, Bit D0. Connecting MIC2LP/LINE2LP input signal to the LEFT_LOP pin is done by closing SW-L2 and opening SW-L0, this action is done by writing a “1” to Page 0, Register 108, Bit D2. Connecting MIC1LM/LINE1LM input signal to the LEFT_LOM pin is done by closing SW-L4 and opening SW-L3, this action is done by writing a “1” to Page 0, Register 108, Bit D1. Connecting MIC2LM/LINE2LM input signal to the LEFT_LOM pin is done by closing SW-L5 and opening SW-L3, this action is done by writing a “1” to Page 0, Register 108, Bit D3.

Connecting MIC1RP/LINE1RP input signal to the RIGHT_LOP pin is done by closing SW-R1 and opening SW-R0, this action is done by writing a “1” to Page 0, Register 108, Bit D4. Connecting MIC2RP/LINE2RP input signal to the RIGHT_LOP pin is done by closing SW-R2 and opening SW-R0, this action is done by writing a “1” to Page 0, Register 108, Bit D6. Connecting MIC1RM/LINE1RM input signal to the RIGHT_LOM pin is done by closing SW-R4 and opening SW-R3, this action is done by writing a “1” to Page 0, Register 108, Bit D5. Connecting MIC2RM/LINE2RM input signal to the RIGHT_LOM pin is done by closing SW-R5 and opening SW-R3, this action is done by writing a “1” to Page 0, Register 108, Bit D7. A diagram of the passive analog bypass mode configuration can be seen in 図 10-20.

In general, connecting two switches to the same output pin should be avoided, as this error will short two input signals together, and would like cause distortion of the signal as the two signal are in contention, and poor frequency response would also likely occur.

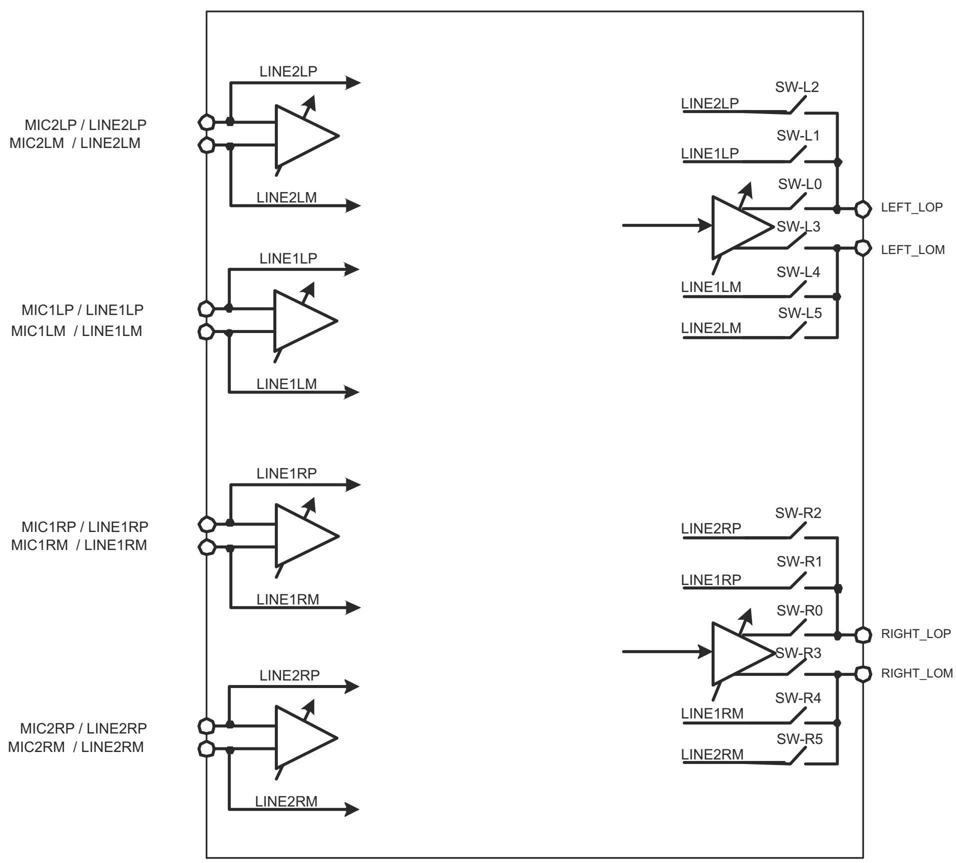


図 10-20. Passive Analog Bypass Mode Configuration

10.4.2 Digital Audio Processing for Record Path

In applications where record *only* is selected, and DAC is powered down, the playback path signal processing blocks can be used in the ADC record path. These filtering blocks can support high pass, low pass, band pass or notch filtering. In this mode, the record only path has switches SW-D1 through SW-D4 closed, and reroutes the ADC output data through the digital signal processing blocks. Since the DAC's Digital Signal Processing blocks are being re-used, naturally the addresses of these digital filter coefficients are the same as for the DAC digital processing and are located on Page 1, Registers 1-52. This record only mode is enabled by powering down both DACs by writing to Page 0, Register 37, bits D7-D6 (D7=D6="0"). Next, enable the digital filter pathway for the ADC by writing a "1" to Page 0, Register 107, bit D3. (Note, this pathway is only enabled if *both* DACs are powered down.) This record only path can be seen in 図 10-21.

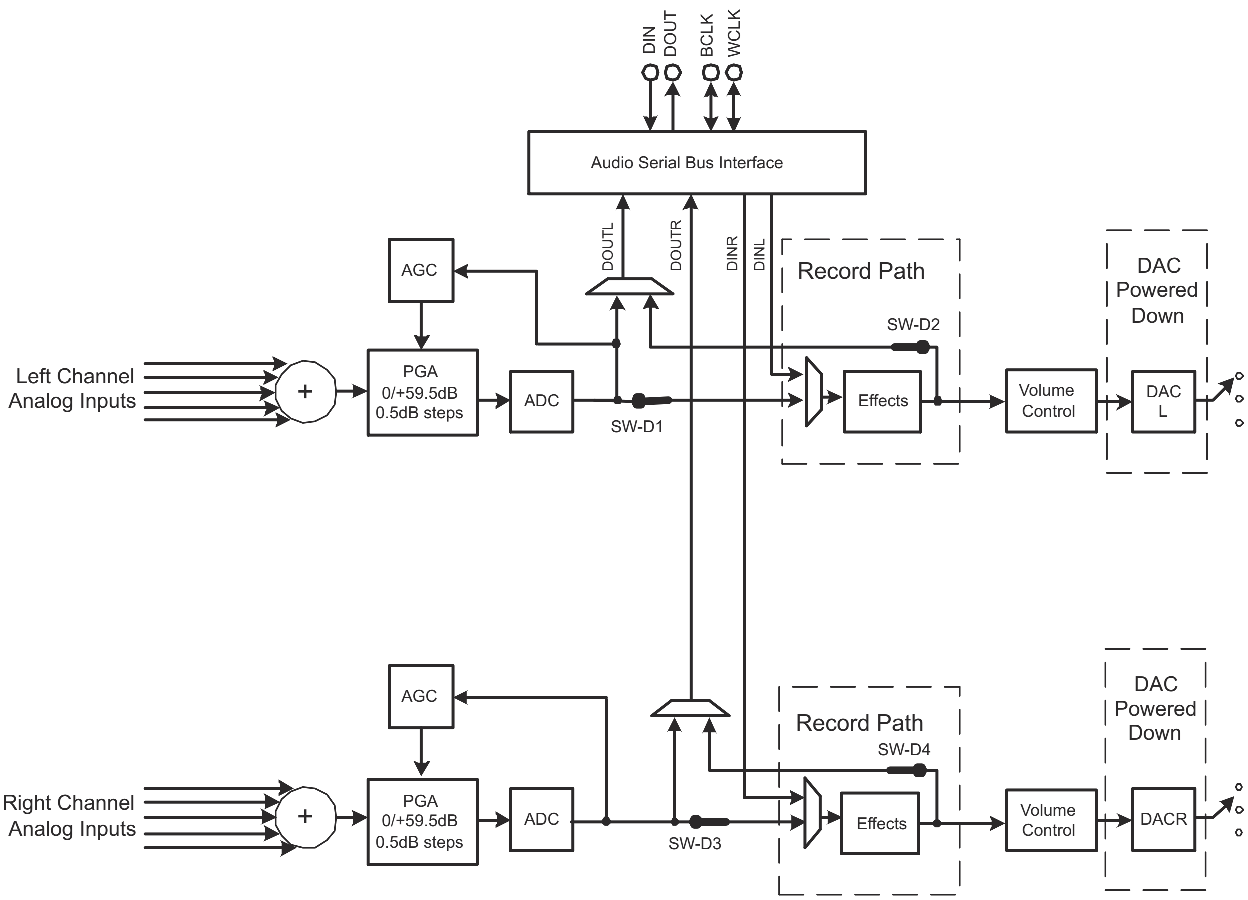


図 10-21. Record *Only* Mode With Digital Processing Path Enabled

10.5 Programming

10.5.1 Digital Control Serial Interface

The TLV320AIC3106 control interface supports SPI or I^{2}C communication protocols, with the protocol selectable using the SELECT pin. For SPI, SELECT should be tied high; for I^{2}C, SELECT should be tied low. It is not recommended to change the state of SELECT during device operation.

10.5.1.1 SPI Control Mode

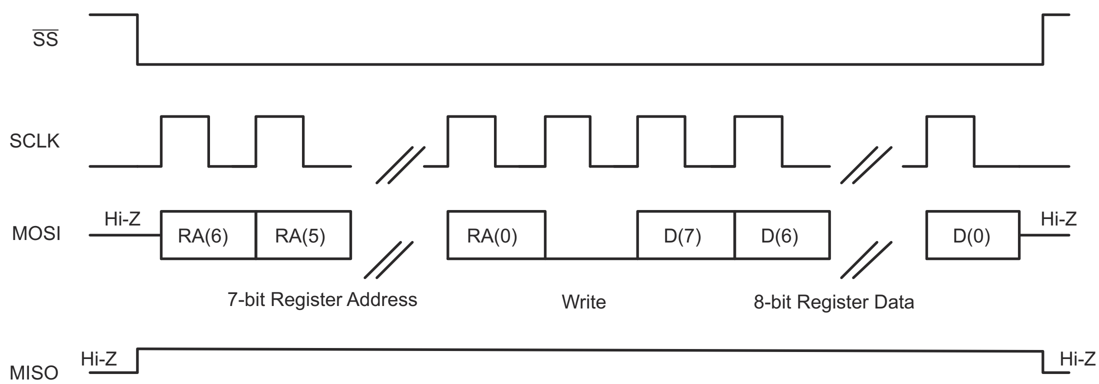


図 10-22. SPI Write

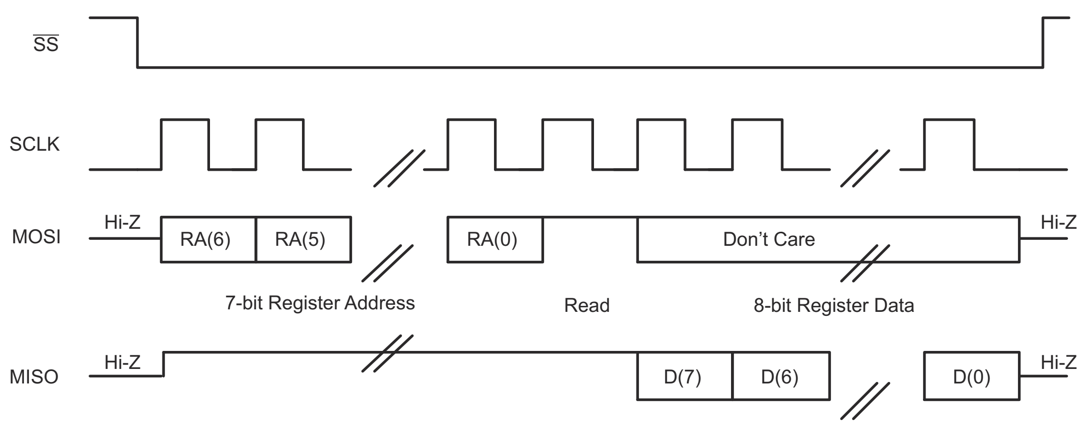


図 10-23. SPI Read

In the SPI control mode, the TLV320AIC3106 uses the pins MFP0=SSB, MFP1=SCLK, MFP2=MISO, MFP3=MOSI as a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3106) depend on a master to start and synchronize transmissions.

A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

The TLV320AIC3106 interface is designed so that with a clock phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its MISO pin on the first serial clock edge. The SSB pin can remain low between transmissions; however, the TLV320AIC3106 only interprets the first 8 bits transmitted after the falling edge of SSB as a command byte, and the next 8 bits as a data byte only if writing to a register. Reserved register bits should be written to their default values.

10.5.1.1.1 SPI Communication Protocol

The TLV320AIC3106 is entirely controlled by registers. Reading and writing these registers is accomplished by the use of an 8-bit command, which is sent to the MOSI pin of the part prior to the data for that register. The command is constructed as shown in 表 10-6. The first 7 bits specify the register address which is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction of data flow on the serial bus. In the case of a register write, the R/W bit should be set to 0. A second byte of data is sent to the MOSI pin and contains the data to be written to the register.

Reading of registers is accomplished in similar fashion. The 8-bit command word sends the 7-bit register address, followed by R/W bit = 1 to signify a register read is occurring,. The 8-bit register data is then clocked out of the part on the MISO pin during the second 8 SCLK clocks in the frame.

表 10-6. Command Word

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	R/ $\overline{W}$

10.5.1.1.2 Limitation on Register Writing

When writing registers in SPI mode related to the audio output drivers mux, mix, gain configuration, etc., do not use the auto-increment mode. In addition, between two successive writes to these registers, the host should keep MFP0 (SPI chip select) high for at least 6.25us, to ensure that the register writes have occurred properly.

10.5.1.1.3 Continuous Read / Write Operation

The TLV320AIC3106 includes the ability to read/write registers continuously, without needing to provide an address for every register accessed. In SPI mode, a continuous write is executed by transitioning MFP0 (SPI chip select) low to start the frame, sending the first 8-bit command word to read/write a particular register, and then sending multiple bytes of register data, intended for the addressed register and those following. A continuous read is done similarly, with multiple bytes read in from the addressed register and the following registers on the page. When the MFP0 (SPI chip select) pin is transitioned high again, the frame ends, as does the continuous read/write operation. A new frame must begin again with a new command word, to start the next bus transaction.

Note that this continuous read/write operation does not continue past a page boundary. The user should not attempt to read/write past the end of a page, since this may result in undesirable operation.

10.5.1.2 I²C Control Interface

The TLV320AIC3106 supports the I²C control protocol when the SELECT pin is tied low, using 7-bit addressing and capable of both standard and fast modes. For I2C fast mode, note that the minimum timing for each of $t_{HD\text{-}STA}$, $t_{SU\text{-}STA}$, and $t_{SU\text{-}STO}$ is 0.9 us, as seen in 図 10-24. When in I²C control mode, the TLV320AIC3106 can be configured for one of four different addresses, using the multifunction pins MFP0 and MFP1, which control the two LSBs of the device address. The 5 MSBs of the device address are fixed as 00110 and cannot be changed, while the two LSBs are given by MFP1:MFP0. This results in four possible device addresses:

表 10-7. I^2C Slave Device Addresses for MFP1, MFP0 Settings

MFP1	MFP0	Device Address
0	0	0011000
0	1	0011001
1	0	0011010
1	1	0011011

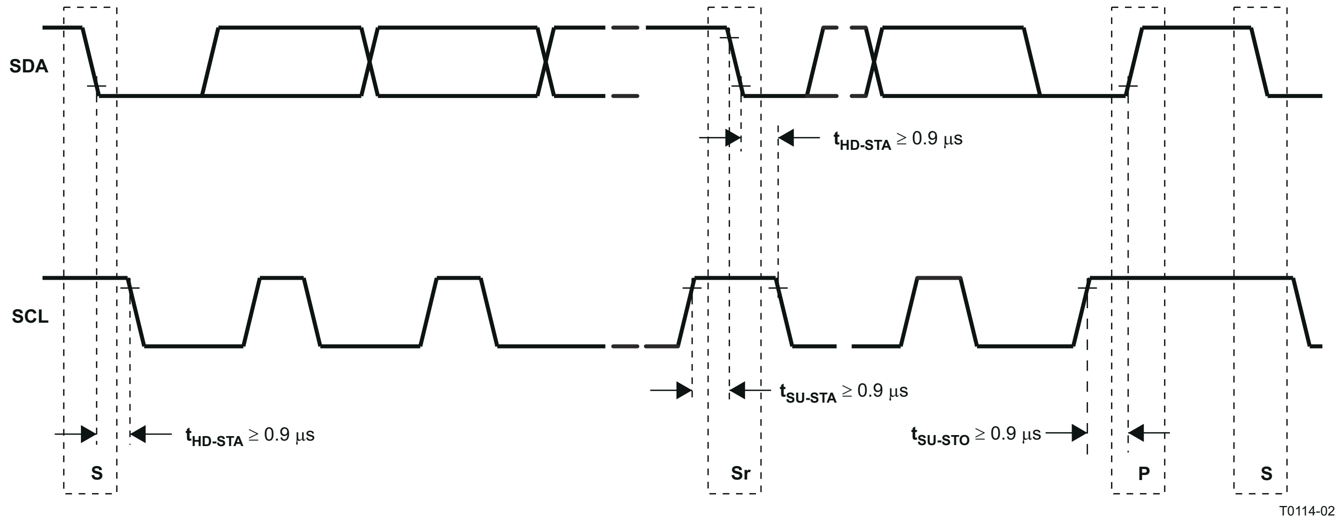


図 10-24. I^2C Interface Timing

I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the TLV320AIC3106 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero; a HIGH indicates the bit is one). Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receivers shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. Under normal circumstances the master drives the clock line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication. They do this by causing a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit.

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC3106 also responds to and acknowledges a General Call, which consists of the master issuing a command with a slave address byte of 00H.

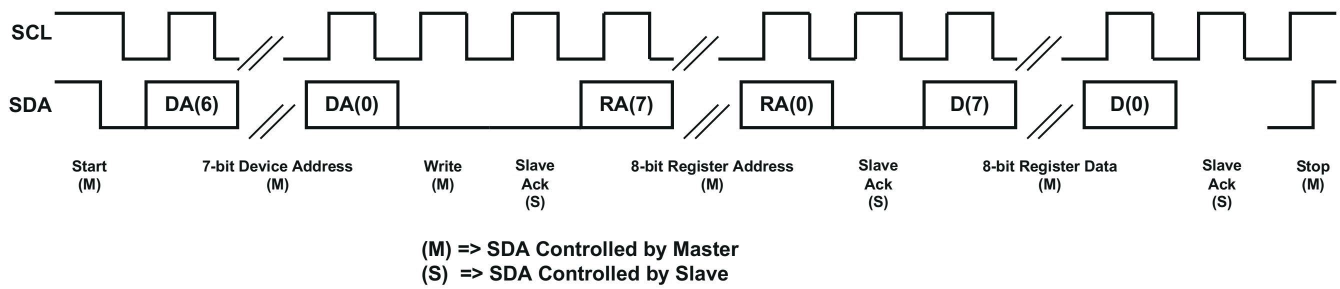


図 10-25. I2C Write

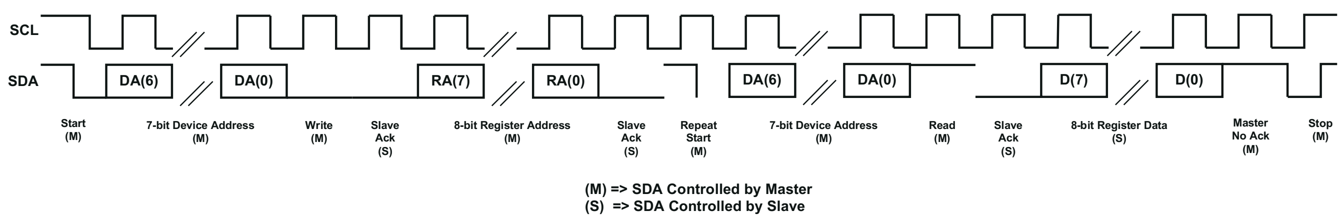


図 10-26. I2C Read

In the case of an I2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I2C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues an ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next 8 clocks the data of the next incremental register.

10.5.1.2.1 I2C BUS Debug in a Glitched System

Occasionally, some systems may encounter noise or glitches on the I2C bus. In the unlikely event that this affects bus performance, then it can be useful to use the I2C Debug register. This feature terminates the I2C bus error allowing this I2C device and system to resume communications. The I2C bus error detector is enabled by default. The TLV320AIC3106 I2C error detector status can be read from Page 0, Register 107, bit D0. If desired, the detector can be disabled by writing to Page 0, Register 107, bit D2.

10.6 Register Maps

The register map of the TLV320AIC3106 actually consists of multiple pages of registers, with each page containing 128 registers. The register at address zero on each page is used as a page-control register, and writing to this register determines the active page for the device. All subsequent read/write operations will access the page that is active at the time, unless a register write is performed to change the active page. Only two pages of registers are implemented in this product, with the active page defaulting to page 0 upon device reset.

For example, at device reset, the active page defaults to page 0, and thus all register read/write operations for addresses 1 to 127 will access registers in page 0. If registers on page 1 must be accessed, the user must write the 8-bit sequence 0x01 to register 0, the page control register, to change the active page from page 0 to page 1. After this write, it is recommended the user also read back the page control register, to safely ensure the change in page control has occurred properly. Future read/write operations to addresses 1 to 127 will now access registers in page 1. When page 0 registers must be accessed again, the user writes the 8-bit sequence 0x00 to register 0, the page control register, to change the active page back to page 0. After a recommended read of the page control register, all further read/write operations to addresses 1 to 127 will now access page 0 registers again.

The control registers for the TLV320AIC3106 are described in detail below. All registers are 8 bit in width, with D7 referring to the most significant bit of each register, and D0 referring to the least significant bit.

表 10-8. Page 0 / Register 0: Page Select Register

BIT(1)	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	X	0000 000	Reserved, write only zeros to these register bits
D0	R/W	0	Page Select Bit Writing zero to this bit sets Page-0 as the active page for following register accesses. Writing a one to this bit sets Page-1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read/writes.

(1) When resetting registers related to routing and volume controls of output drivers, it is recommended to reset them by writing directly to the registers instead of using software reset.

表 10-9. Page 0 / Register 1: Software Reset Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	W	0	Software Reset Bit 0 : Don't Care 1 : Self clearing software reset
D6–D0	W	000 0000	Reserved; don't write

表 10-10. Page 0 / Register 2: Codec Sample Rate Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	ADC Sample Rate Select 0000: ADC $f_S = f_{S(ref)}/1$ 0001: ADC $f_S = f_{S(ref)}/1.5$ 0010: ADC $f_S = f_{S(ref)}/2$ 0011: ADC $f_S = f_{S(ref)}/2.5$ 0100: ADC $f_S = f_{S(ref)}/3$ 0101: ADC $f_S = f_{S(ref)}/3.5$ 0110: ADC $f_S = f_{S(ref)}/4$ 0111: ADC $f_S = f_{S(ref)}/4.5$ 1000: ADC $f_S = f_{S(ref)}/5$ 1001: ADC $f_S = f_{S(ref)}/5.5$ 1010: ADC $f_S = f_{S(ref)}/6$ 1011–1111: Reserved, do not write these sequences.

表 10-10. Page 0 / Register 2: Codec Sample Rate Select Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D0	R/W	0000	DAC Sample Rate Select 0000 : DAC $f_S = f_{S(ref)}/1$ 0001 : DAC $f_S = f_{S(ref)}/1.5$ 0010 : DAC $f_S = f_{S(ref)}/2$ 0011 : DAC $f_S = f_{S(ref)}/2.5$ 0100 : DAC $f_S = f_{S(ref)}/3$ 0101 : DAC $f_S = f_{S(ref)}/3.5$ 0110 : DAC $f_S = f_{S(ref)}/4$ 0111 : DAC $f_S = f_{S(ref)}/4.5$ 1000 : DAC $f_S = f_{S(ref)}/5$ 1001: DAC $f_S = f_{S(ref)}/5.5$ 1010: DAC $f_S = f_{S(ref)} / 6$ 1011–1111 : Reserved, do not write these sequences.

表 10-11. Page 0 / Register 3: PLL Programming Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Control Bit 0: PLL is disabled 1: PLL is enabled
D6–D3	R/W	0010	PLL Q Value 0000: Q = 16 0001 : Q = 17 0010 : Q = 2 0011 : Q = 3 0100 : Q = 4 … 1110: Q = 14 1111: Q = 15
D2–D0	R/W	000	PLL P Value 000: P = 8 001: P = 1 010: P = 2 011: P = 3 100: P = 4 101: P = 5 110: P = 6 111: P = 7

表 10-12. Page 0 / Register 4: PLL Programming Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 01	PLL J Value 0000 00: Reserved, do not write this sequence 0000 01: J = 1 0000 10: J = 2 0000 11: J = 3 … 1111 10: J = 62 1111 11: J = 63
D1–D0	R/W	00	Reserved, write only zeros to these bits

表 10-13. Page 0 / Register 5: PLL Programming Register C[(1)]

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	PLL D value – Eight most significant bits of a 14-bit unsigned integer valid values for D are from zero to 9999, represented by a 14-bit integer located in Page-0/Reg-5-6. Values should not be written into these registers that would result in a D value outside the valid range.

(1) Note that whenever the D value is changed, register 5 should be written, immediately followed by register 6. Even if only the MSB or LSB of the value changes, both registers should be written.

表 10-14. Page 0 / Register 6: PLL Programming Register D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 0000	PLL D value – Six least significant bits of a 14-bit unsigned integer valid values for D are from zero to 9999, represented by a 14-bit integer located in Page-0/Reg-5-6. Values should not be written into these registers that would result in a D value outside the valid range.
D1–D0	R	00	Reserved, write only zeros to these bits.

表 10-15. Page 0 / Register 7: Codec Datapath Setup Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	$f_{S(ref)}$ setting This register setting controls timers related to the AGC time constants. 0: $f_{S(ref)}$ = 48 kHz 1: $f_{S(ref)}$ = 44.1 kHz
D6	R/W	0	ADC Dual rate control 0: ADC dual rate mode is disabled 1: ADC dual rate mode is enabled Note: ADC Dual Rate Mode must match DAC Dual Rate Mode
D5	R/W	0	DAC Dual Rate Control 0: DAC dual rate mode is disabled 1: DAC dual rate mode is enabled
D4–D3	R/W	00	Left DAC Datapath Control 00: Left DAC datapath is off (muted) 01: Left DAC datapath plays left channel input data 10: Left DAC datapath plays right channel input data 11: Left DAC datapath plays mono mix of left and right channel input data
D2–D1	R/W	00	Right DAC Datapath Control 00: Right DAC datapath is off (muted) 01: Right DAC datapath plays right channel input data 10: Right DAC datapath plays left channel input data 11: Right DAC datapath plays mono mix of left and right channel input data
D0	R/W	0	Reserved. Only write zero to this register.

表 10-16. Page 0 / Register 8: Audio Serial Data Interface Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Bit Clock Directional Control 0: BCLK (or GPIO2 if programmed as BCLK) is an input (slave mode) 1: BCLK (or GPIO2 if programmed as BCLK) is an output (master mode)
D6	R/W	0	Word Clock Directional Control 0: WCLK (or GPIO1 if programmed as WCLK) is an input (slave mode) 1: WCLK (or GPIO1 if programmed as WCLK) is an output (master mode)
D5	R/W	0	Serial Output Data Driver (DOUT) 3-State Control 0: Do not place DOUT in high-impedance state when valid data is not being sent 1: Place DOUT in high-impedance state when valid data is not being sent
D4	R/W	0	Bit/ Word Clock Drive Control 0: BCLK (or GPIO2 if programmed as BCLK) / WCLK (or GPIO1 if programmed as WCLK) will not continue to be transmitted when running in master mode if codec is powered down 1: BCLK (or GPIO2 if programmed as BCLK) / WCLK (or GPIO1 if programmed as WCLK) continues to be transmitted when running in master mode, even if codec is powered down
D3	R/W	0	Reserved. Don't write to this register bit.
D2	R/W	0	3-D Effect Control 0: Disable 3-D digital effect processing 1: Enable 3-D digital effect processing
D1–D0	R/W	00	Digital Microphone Functionality Control 00: Digital microphone support is disabled 01: Digital microphone support is enabled with an oversampling rate of 128 10: Digital microphone support is enabled with an oversampling rate of 64 11: Digital microphone support is enabled with an oversampling rate of 32

表 10-17. Page 0 / Register 9: Audio Serial Data Interface Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Audio Serial Data Interface Transfer Mode 00: Serial data bus uses I^2S mode 01: Serial data bus uses DSP mode 10: Serial data bus uses right-justified mode 11: Serial data bus uses left-justified mode
D5–D4	R/W	00	Audio Serial Data Word Length Control 00: Audio data word length = 16 bits 01: Audio data word length = 20 bits 10: Audio data word length = 24 bits 11: Audio data word length = 32 bits
D3	R/W	0	Bit Clock Rate Control This register only has effect when bit clock is programmed as an output 0: Continuous-transfer mode used to determine master mode bit clock rate 1: 256-clock transfer mode used, resulting in 256 bit clocks per frame
D2	R/W	0	DAC Re-Sync 0: Don't Care 1: Re-sync stereo DAC with codec interface if the group delay changes by more than ±DACFS/4.
D1	R/W	0	ADC Re-Sync 0: Don't Care 1: Re-sync stereo ADC with codec interface if the group delay changes by more than ±ADCFS/4.
D0	R/W		Re-Sync Mute Behavior 0: Re-sync is done without soft-muting the channel. (ADC/DAC) 1: Re-sync is done by internally soft-muting the channel. (ADC/DAC)

表 10-18. Page 0 / Register 10: Audio Serial Data Interface Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Audio Serial Data Word Offset Control This register determines where valid data is placed or expected in each frame, by controlling the offset from beginning of the frame where valid data begins. The offset is measured from the rising edge of word clock when in DSP mode. 0000 0000: Data offset = 0 bit clocks 0000 0001: Data offset = 1 bit clock 0000 0010: Data offset = 2 bit clocks … Note: In continuous transfer mode the maximum offset is 17 for I^2S/LJF/RJF modes and 16 for DSP mode. In 256-clock mode, the maximum offset is 242 for I^2S/LJF/RJF and 241 for DSP modes. 1111 1110: Data offset = 254 bit clocks 1111 1111: Data offset = 255 bit clocks

表 10-19. Page 0 / Register 11: Audio Codec Overflow Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to 0 after it is read. 0: No overflow has occurred 1: An overflow has occurred
D6	R	0	Right ADC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to 0 after it is read. 0: No overflow has occurred 1: An overflow has occurred
D5	R	0	Left DAC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to 0 after it is read. 0: No overflow has occurred 1: An overflow has occurred
D4	R	0	Right DAC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to 0 after it is read. 0: No overflow has occurred 1: An overflow has occurred
D3–D0	R/W	0001	PLL R Value 0000: R = 16 0001 : R = 1 0010 : R = 2 0011 : R = 3 0100 : R = 4 … 1110: R = 14 1111: R = 15

表 10-20. Page 0 / Register 12: Audio Codec Digital Filter Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left ADC Highpass Filter Control 00: Left ADC highpass filter disabled 01: Left ADC highpass filter –3-dB frequency = 0.0045 × ADC f_S 10: Left ADC highpass filter –3-dB frequency = 0.0125 × ADC f_S 11: Left ADC highpass filter –3-dB frequency = 0.025 × ADC f_S
D5–D4	R/W	00	Right ADC Highpass Filter Control 00: Right ADC highpass filter disabled 01: Right ADC highpass filter –3-dB frequency = 0.0045 × ADC f_S 10: Right ADC highpass filter –3-dB frequency = 0.0125 × ADC f_S 11: Right ADC highpass filter –3-dB frequency = 0.025 × ADC f_S
D3	R/W	0	Left DAC Digital Effects Filter Control 0: Left DAC digital effects filter disabled (bypassed) 1: Left DAC digital effects filter enabled
D2	R/W	0	Left DAC De-emphasis Filter Control 0: Left DAC de-emphasis filter disabled (bypassed) 1: Left DAC de-emphasis filter enabled
D1	R/W	0	Right DAC Digital Effects Filter Control 0: Right DAC digital effects filter disabled (bypassed) 1: Right DAC digital effects filter enabled
D0	R/W	0	Right DAC De-emphasis Filter Control 0: Right DAC de-emphasis filter disabled (bypassed) 1: Right DAC de-emphasis filter enabled

表 10-21. Page 0 / Register 13: Headset / Button Press Detection Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Headset Detection Control 0: Headset detection disabled 1: Headset detection enabled
D6–D5	R	00	Headset Type Detection Results 00: No headset detected 01: Headset without microphone detected 10: Ignore (reserved) 11: Headset with microphone detected
D4–D2	R/W	000	Headset Glitch Suppression Debounce Control for Jack Detection 000: Debounce = 16 ms (sampled with 2-ms clock) 001: Debounce = 32 ms (sampled with 4-ms clock) 010: Debounce = 64 ms (sampled with 8-ms clock) 011: Debounce = 128 ms (sampled with 16-ms clock) 100: Debounce = 256 ms (sampled with 32-ms clock) 101: Debounce = 512 ms (sampled with 64-ms clock) 110: Reserved, do not write this bit sequence to these register bits. 111: Reserved, do not write this bit sequence to these register bits.
D1–D0	R/W	00	Headset Glitch Suppression Debounce Control for Button Press 00: Debounce = 0msec 01: Debounce = 8 ms (sampled with 1-ms clock) 10: Debounce = 16 ms (sampled with 2-ms clock) 11: Debounce = 32 ms (sampled with 4-ms clock)

表 10-22. Page 0 / Register 14: Headset / Button Press Detection Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Driver Capacitive Coupling 0: Programs high-power outputs for capless driver configuration 1: Programs high-power outputs for ac-coupled driver configuration
D6(1)	R/W	0	Stereo Output Driver Configuration A Note: do not set bits D6 and D3 both high at the same time. 0: A stereo fully differential output configuration is not being used 1: A stereo fully differential output configuration is being used
D5	R	0	Button Press Detection Flag This register is a sticky bit, and will stay set to 1 after a button press has been detected, until the register is read. Upon reading this register, the bit is reset to zero. 0: A button press has not been detected 1: A button press has been detected
D4	R	0	Headset Detection Flag 0: A headset has not been detected 1: A headset has been detected
D3(1)	R/W	0	Stereo Output Driver Configuration B Note: do not set bits D6 and D3 both high at the same time. 0: A stereo pseudodifferential output configuration is not being used 1: A stereo pseudodifferential output configuration is being used
D2–D0	R	000	Reserved. Write only zeros to these bits.

(1) Do not set D6 and D3 to 1 simultaneously

表 10-23. Page 0 / Register 15: Left ADC PGA Gain Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left ADC PGA Mute 0: The left ADC PGA is not muted 1: The left ADC PGA is muted
D6–D0	R/W	000 0000	Left ADC PGA Gain Setting 000 0000: Gain = 0 dB 000 0001: Gain = 0.5 dB 0000010: Gain = 1 dB … 111 0110: Gain = 59 dB 111 0111: Gain = 59.5 dB 111 1000: Gain = 59.5 dB … 111 1111: Gain = 59.5 dB

表 10-24. Page 0 / Register 16: Right ADC PGA Gain Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Right ADC PGA Mute 0: The right ADC PGA is not muted 1: The right ADC PGA is muted
D6–D0	R/W	000 0000	Right ADC PGA Gain Setting 000 0000: Gain = 0 dB 000 0001: Gain = 0.5 dB 000 0010: Gain = 1 dB … 111 0110: Gain = 59 dB 111 0111: Gain = 59.5 dB 111 1000: Gain = 59.5 dB … 111 1111: Gain = 59.5 dB

表 10-25. Page 0 / Register 17: MIC3L/R to Left ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	1111	MIC3L Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects MIC3L to the left ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: MIC3L is not connected to the left ADC PGA
D3–D0	R/W	1111	MIC3R Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects MIC3R to the left ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: MIC3R is not connected to the left ADC PGA

表 10-26. Page 0 / Register 18: MIC3L/R to Right ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	1111	MIC3L Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects MIC3L to the right ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: MIC3L is not connected to the right ADC PGA
D3–D0	R/W	1111	MIC3R Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects MIC3R to the right ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: MIC3R is not connected to right ADC PGA

表 10-27. Page 0 / Register 19: LINE1L to Left ADC Control Register

BIT	READ/WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE1L Single-Ended vs Fully Differential Control If LINE1L is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: LINE1L is configured in single-ended mode 1: LINE1L is configured in fully differential mode
D6–D3	R/W	1111	LINE1L Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects LINE1L to the left ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: LINE1L is not connected to the left ADC PGA
D2	R/W	0	Left ADC Channel Power Control 0: Left ADC channel is powered down 1: Left ADC channel is powered up
D1–D0	R/W	00	Left ADC PGA Soft-Stepping Control 00: Left ADC PGA soft-stepping at once per f_S 01: Left ADC PGA soft-stepping at once per two f_S 10–11: Left ADC PGA soft-stepping is disabled

表 10-28. Page 0 / Register 20: LINE2L to Left[(1)] ADC Control Register

BIT	READ/WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Single-Ended vs Fully Differential Control If LINE2L is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: LINE2L is configured in single-ended mode 1: LINE2L is configured in fully differential mode
D6–D3	R/W	1111	LINE2L Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects LINE2L to the left ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: LINE2L is not connected to the left ADC PGA
D2	R/W	0	Left ADC Channel Weak Common-Mode Bias Control 0: Left ADC channel unselected inputs are not biased weakly to the ADC common-mode voltage 1: Left ADC channel unselected inputs are biased weakly to the ADC common- mode voltage
D1–D0	R	00	Reserved. Write only zeros to these register bits

(1) LINE1R SEvsFD control is available for both left and right channels. However this setting must be same for both the channels.

表 10-29. Page 0 / Register 21: LINE1R to Left ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE1R Single-Ended vs Fully Differential Control If LINE1R is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: LINE1R is configured in single-ended mode 1: LINE1R is configured in fully differential mode
D6–D3	R/W	1111	LINE1R Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects LINE1R to the left ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: LINE1R is not connected to the left ADC PGA
D2–D0	R	000	Reserved. Write only zeros to these register bits.

表 10-30. Page 0 / Register 22: LINE1R to Right ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE1R Single-Ended vs Fully Differential Control If LINE1R is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: LINE1R is configured in single-ended mode 1: LINE1R is configured in fully differential mode
D6–D3	R/W	1111	LINE1R Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects LINE1R to the right ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: LINE1R is not connected to the right ADC PGA
D2	R/W	0	Right ADC Channel Power Control 0: Right ADC channel is powered down 1: Right ADC channel is powered up
D1–D0	R/W	00	Right ADC PGA Soft-Stepping Control 00: Right ADC PGA soft-stepping at once per f_S 01: Right ADC PGA soft-stepping at once per two f_S 10–11: Right ADC PGA soft-stepping is disabled

表 10-31. Page 0 / Register 23: LINE2R to Right ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Single-Ended vs Fully Differential Control If LINE2R is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: LINE2R is configured in single-ended mode 1: LINE2R is configured in fully differential mode

表 10-31. Page 0 / Register 23: LINE2R to Right ADC Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D3	R/W	1111	LINE2R Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects LINE2R to the right ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: LINE2R is not connected to the right ADC PGA
D2	R/W	0	Right ADC Channel Weak Common-Mode Bias Control 0: Right ADC channel unselected inputs are not biased weakly to the ADC common-mode voltage 1: Right ADC channel unselected inputs are biased weakly to the ADC common- mode voltage
D1–D0	R	00	Reserved. Write only zeros to these register bits

表 10-32. Page 0 / Register 24: LINE1L to Right ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE1L Single-Ended vs Fully Differential Control If LINE1L is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: LINE1L is configured in single-ended mode 1: LINE1L is configured in fully differential mode
D6–D3	R/W	1111	LINE1L Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects LINE1L to the right ADC PGA mix 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: LINE1L is not connected to the right ADC PGA
D2–D0	R	000	Reserved. Write only zeros to these register bits.

表 10-33. Page 0 / Register 25: MICBIAS Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	MICBIAS Level Control 00: MICBIAS output is powered down 01: MICBIAS output is powered to 2.0V 10: MICBIAS output is powered to 2.5V 11: MICBIAS output is connected to AVDD
D5–D4	R/W	00	Digital Microphone Control 00: If Digital MIC is enabled, both Left and Right Digital MICs are available 01: If Digital MIC is enabled, Left Digital MIC and Right ADC are available 10: If Digital MIC is enabled, Left ADC and Right Digital MIC are available 11: Reserved. Don't write to this sequence.
D3	R	0	Reserved. Don't write to this register bit.
D2–D0	R	XXX	Reserved. Write only zeros to these register bits.

表 10-34. Page 0 / Register 26: Left AGC Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left AGC Enable 0: Left AGC is disabled 1: Left AGC is enabled
D6–D4	R/W	000	Left AGC Target Level 000: Left AGC target level = –5.5 dB 001: Left AGC target level = –8 dB 010: Left AGC target level = –10 dB 011: Left AGC target level = –12 dB 100: Left AGC target level = –14 dB 101: Left AGC target level = –17 dB 110: Left AGC target level = –20 dB 111: Left AGC target level = –24 dB
D3–D2	R/W	00	Left AGC Attack Time These time constants[(1)] will not be accurate when double rate audio mode is enabled. 00: Left AGC attack time = 8 ms 01: Left AGC attack time = 11 ms 10: Left AGC attack time = 16 ms 11: Left AGC attack time = 20 ms
D1–D0	R/W	00	Left AGC Decay Time These time constants[(1)] will not be accurate when double rate audio mode is enabled. 00: Left AGC decay time = 100 ms 01: Left AGC decay time = 200 ms 10: Left AGC decay time = 400 ms 11: Left AGC decay time = 500 ms

(1) Time constants are valid when DRA is not enabled. The values would change if DRA is enabled.

表 10-35. Page 0 / Register 27: Left AGC Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	1111 111	Left AGC Maximum Gain Allowed 0000 000: Maximum gain = 0 dB 0000 001: Maximum gain = 0.5 dB 0000 010: Maximum gain = 1 dB … 1110 110: Maximum gain = 59 dB 1110 111–1111 111: Maximum gain = 59.5 dB
D0	R/W	0	Reserved. Write only zero to this register bit.

表 10-36. Page 0 / Register 28: Left AGC Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Noise Gate Hysteresis Level Control 00: Hysteresis = 1 dB 01: Hysteresis = 2 dB 10: Hysteresis = 3 dB 11: Hysteresis is disabled
D5–D1	R/W	00 000	Left AGC Noise Threshold Control 00 000: Left AGC Noise/Silence Detection disabled 00 001: Left AGC noise threshold = –30 dB 00 010: Left AGC noise threshold = –32 dB 00 011: Left AGC noise threshold = –34 dB … 11 101: Left AGC noise threshold = –86 dB 11 110: Left AGC noise threshold = –88 dB 11 111: Left AGC noise threshold = –90 dB
D0	R/W	0	Left AGC Clip Stepping Control 0: Left AGC clip stepping disabled 1: Left AGC clip stepping enabled

表 10-37. Page 0 / Register 29: Right AGC Control Register A

BIT	READ/WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right AGC Enable 0: Right AGC is disabled 1: Right AGC is enabled
D6–D4	R/W	000	Right AGC Target Level 000: Right AGC target level = –5.5 dB 001: Right AGC target level = –8 dB 010: Right AGC target level = –10 dB 011: Right AGC target level = –12 dB 100: Right AGC target level = –14 dB 101: Right AGC target level = –17 dB 110: Right AGC target level = –20 dB 111: Right AGC target level = –24 dB
D3–D2	R/W	00	Right AGC Attack Time These time constants will not be accurate when double rate audio mode is enabled. 00: Right AGC attack time = 8 ms 01: Right AGC attack time = 11 ms 10: Right AGC attack time = 16 ms 11: Right AGC attack time = 20 ms
D1–D0	R/W	00	Right AGC Decay Time These time constants will not be accurate when double rate audio mode is enabled. 00: Right AGC decay time = 100 ms 01: Right AGC decay time = 200 ms 10: Right AGC decay time = 400 ms 11: Right AGC decay time = 500 ms

表 10-38. Page 0 / Register 30: Right AGC Control Register B

BIT	READ/WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	1111 111	Right AGC Maximum Gain Allowed 0000 000: Maximum gain = 0 dB 0000 001: Maximum gain = 0.5 dB 0000 010: Maximum gain = 1 dB … 1110 110: Maximum gain = 59 dB 1110 111–1111 111: Maximum gain = 59.5 dB
D0	R/W	0	Reserved. Write only zero to this register bit.

表 10-39. Page 0 / Register 31: Right AGC Control Register C

BIT	READ/WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Noise Gate Hysteresis Level Control 00: Hysteresis = 1 dB 01: Hysteresis = 2 dB 10: Hysteresis = 3 dB 11: Hysteresis is disabled
D5–D1	R/W	00 000	Right AGC Noise Threshold Control 00 000: Right AGC Noise/Silence Detection disabled 00 001: Right AGC noise threshold = –30 dB 00 010: Right AGC noise threshold = –32 dB 00 011: Right AGC noise threshold = –34 dB … 11 101: Right AGC noise threshold = –86 dB 11 110: Right AGC noise threshold = –88 dB 11 111: Right AGC noise threshold = –90 dB
D0	R/W	0	Right AGC Clip Stepping Control 0: Right AGC clip stepping disabled 1: Right AGC clip stepping enabled

表 10-40. Page 0 / Register 32: Left AGC Gain Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel Gain Applied by AGC Algorithm 1110 1000: Gain = –12 dB 1110 1001: Gain = –11.5 dB 1110 1010: Gain = –11 dB … 0000 0000: Gain = 0 dB 0000 0001: Gain = 0.5 dB … 0111 0110: Gain = 59 dB 0111 0111: Gain = 59.5 dB

表 10-41. Page 0 / Register 33: Right AGC Gain Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel Gain Applied by AGC Algorithm 1110 1000: Gain = –12 dB 1110 1001: Gain = –11.5 dB 1110 1010: Gain = –11 dB … 0000 0000: Gain = 0 dB 0000 0001: Gain = 0.5 dB … 0111 0110: Gain = 59 dB 0111 0111: Gain = 59.5 dB

表 10-42. Page 0 / Register 34: Left AGC Noise Gate Debounce Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Left AGC Noise Detection Debounce Control These times(1) will not be accurate when double rate audio mode is enabled. 0000 0: Debounce = 0 ms 0000 1: Debounce = 0.5 ms 0001 0: Debounce = 1 ms 0001 1: Debounce = 2 ms 0010 0: Debounce = 4 ms 0010 1: Debounce = 8 ms 0011 0: Debounce = 16 ms 0011 1: Debounce = 32 ms 0100 0: Debounce = 64×1 = 64ms 0100 1: Debounce = 64×2 = 128ms 0101 0: Debounce = 64×3 = 192ms … 1111 0: Debounce = 64×23 = 1472ms 1111 1: Debounce = 64×24 = 1536ms
D2–D0	R/W	000	Left AGC Signal Detection Debounce Control These times(1) will not be accurate when double rate audio mode is enabled. 000: Debounce = 0 ms 001: Debounce = 0.5 ms 010: Debounce = 1 ms 011: Debounce = 2 ms 100: Debounce = 4 ms 101: Debounce = 8 ms 110: Debounce = 16 ms 111: Debounce = 32 ms

(1) Time constants are valid when DRA is not enabled. The values would change when DRA is enabled

表 10-43. Page 0 / Register 35: Right AGC Noise Gate Debounce Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Right AGC Noise Detection Debounce Control These times(1) will not be accurate when double rate audio mode is enabled. 0000 0: Debounce = 0 ms 0000 1: Debounce = 0.5 ms 0001 0: Debounce = 1 ms 0001 1: Debounce = 2 ms 0010 0: Debounce = 4 ms 0010 1: Debounce = 8 ms 0011 0: Debounce = 16 ms 0011 1: Debounce = 32 ms 0100 0: Debounce = 64 × 1 = 64 ms 0100 1: Debounce = 64 × 2 = 128 ms 0101 0: Debounce = 64 × 3 = 192 ms … 1111 0: Debounce = 64 × 23 = 1472 ms 1111 1: Debounce = 64 × 24 = 1536 ms
D2–D0	R/W	000	Right AGC Signal Detection Debounce Control These times(1) will not be accurate when double rate audio mode is enabled. 000: Debounce = 0 ms 001: Debounce = 0.5 ms 010: Debounce = 1 ms 011: Debounce = 2 ms 100: Debounce = 4 ms 101: Debounce = 8 ms 110: Debounce = 16 ms 111: Debounce = 32 ms

(1) Time constants are valid when DRA is not enabled. The values would change when DRA is enabled.

表 10-44. Page 0 / Register 36: ADC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC PGA Status 0: Applied gain and programmed gain are not the same 1: Applied gain = programmed gain
D6	R	0	Left ADC Power Status 0: Left ADC is in a power down state 1: Left ADC is in a power up state
D5	R	0	Left AGC Signal Detection Status 0: Signal power is greater than noise threshold 1: Signal power is less than noise threshold
D4	R	0	Left AGC Saturation Flag 0: Left AGC is not saturated 1: Left AGC gain applied = maximum allowed gain for left AGC
D3	R	0	Right ADC PGA Status 0: Applied gain and programmed gain are not the same 1: Applied gain = programmed gain
D2	R	0	Right ADC Power Status 0: Right ADC is in a power down state 1: Right ADC is in a power up state
D1	R	0	Right AGC Signal Detection Status 0: Signal power is greater than noise threshold 1: Signal power is less than noise threshold
D0	R	0	Right AGC Saturation Flag 0: Right AGC is not saturated 1: Right AGC gain applied = maximum allowed gain for right AGC

表 10-45. Page 0 / Register 37: AC Power and Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Power Control 0: Left DAC not powered up 1: Left DAC is powered up
D6	R/W	0	Right DAC Power Control 0: Right DAC not powered up 1: Right DAC is powered up
D5–D4	R/W	00	HPLCOM Output Driver Configuration Control 00: HPLCOM configured as differential of HPLOUT 01: HPLCOM configured as constant VCM output 10: HPLCOM configured as independent single-ended output 11: Reserved. Do not write this sequence to these register bits.
D3–D0	R	000	Reserved. Write only zeros to these register bits.

表 10-46. Page 0 / Register 38: High-Power Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only zeros to these register bits.
D5–D3	R/W	000	HPRCOM Output Driver Configuration Control 000: HPRCOM configured as differential of HPROUT 001: HPRCOM configured as constant VCM output 010: HPRCOM configured as independent single-ended output 011: HPRCOM configured as differential of HPLCOM 100: HPRCOM configured as external feedback with HPLCOM as constant VCM output 101–111: Reserved. Do not write these sequences to these register bits.
D2	R/W	0	Short Circuit Protection Control 0: Short circuit protection on all high power output drivers is disabled 1: Short circuit protection on all high power output drivers is enabled
D1	R/W	0	Short-Circuit Protection Mode Control 0: If short circuit protection enabled, it will limit the maximum current to the load 1: If short circuit protection enabled, it will power down the output driver automatically when a short is detected
D0	R	0	Reserved. Write only zero to this register bit.

表 10-47. Page 0 / Register 39: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to this register.

表 10-48. Page 0 / Register 40: High Power Output Stage Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Output Common-Mode Voltage Control 00: Output common-mode voltage = 1.35 V 01: Output common-mode voltage = 1.5 V 10: Output common-mode voltage = 1.65 V 11: Output common-mode voltage = 1.8 V
D5–D4	R/W	00	LINE2L Bypass Path Control 00: LINE2L bypass is disabled 01: LINE2L bypass uses LINE2LP single-ended 10: LINE2L bypass uses LINE2LM single-ended 11: LINE2L bypass uses LINE2LP/M differentially
D3–D2	R/W	00	LINE2R Bypass Path Control 00: LINE2R bypass is disabled 01: LINE2R bypass uses LINE2RP single-ended 10: LINE2R bypass uses LINE2RM single-ended 11: LINE2R bypass uses LINE2RP/M differentially

表 10-48. Page 0 / Register 40: High Power Output Stage Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1–D0	R/W	00	Output Volume Control Soft-Stepping 00: Output soft-stepping = one step per f_S 01: Output soft-stepping = one step per 2 f_S 10: Output soft-stepping disabled 11: Reserved. Do not write this sequence to these register bits.

表 10-49. Page 0 / Register 41: DAC Output Switching Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left DAC Output Switching Control 00: Left DAC output selects DAC_L1 path 01: Left DAC output selects DAC_L3 path to left line output driver 10: Left DAC output selects DAC_L2 path to left high power output drivers 11: Reserved. Do not write this sequence to these register bits.
D5–D4	R/W	00	Right DAC Output Switching Control 00: Right DAC output selects DAC_R1 path 01: Right DAC output selects DAC_R3 path to right line output driver 10: Right DAC output selects DAC_R2 path to right high power output drivers 11: Reserved. Do not write this sequence to these register bits.
D3–D2	R/W	00	Reserved. Write only zeros to these bits.
D1–D0	R/W	00	DAC Digital Volume Control Functionality 00: Left and right DAC channels have independent volume controls 01: Left DAC volume follows the right channel control register 10: Right DAC volume follows the left channel control register 11: Left and right DAC channels have independent volume controls (same as 00)

表 10-50. Page 0 / Register 42: Output Driver Pop Reduction Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Output Driver Power-On Delay Control 0000: Driver power-on time = 0 μs 0001: Driver power-on time = 10 μs 0010: Driver power-on time = 100 μs 0011: Driver power-on time = 1 ms 0100: Driver power-on time = 10 ms 0101: Driver power-on time = 50 ms 0110: Driver power-on time = 100 ms 0111: Driver power-on time = 200 ms 1000: Driver power-on time = 400 ms 1001: Driver power-on time = 800 ms 1010: Driver power-on time = 2 s 1011: Driver power-on time = 4 s 1100–1111: Reserved. Do not write these sequences to these register bits.
D3–D2	R/W	00	Driver Ramp-up Step Timing Control 00: Driver ramp-up step time = 0 ms 01: Driver ramp-up step time = 1 ms 10: Driver ramp-up step time = 2 ms 11: Driver ramp-up step time = 4 ms
D1	R/W	0	Weak Output Common-mode Voltage Control 0: Weakly driven output common-mode voltage is generated from resistor divider off the AVDD supply 1: Weakly driven output common-mode voltage is generated from bandgap reference
D0	R/W	0	Reserved. Write only zero to this register bit.

表 10-51. Page 0 / Register 43: Left DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left DAC Digital Mute 0: The left DAC channel is not muted 1: The left DAC channel is muted
D6–D0	R/W	000 0000	Left DAC Digital Volume Control Setting 000 0000: Gain = 0 dB 000 0001: Gain = –0.5 dB 000 0010: Gain = –1 dB … 111 1101: Gain = –62.5 dB 111 1110: Gain = –63 dB 111 1111: Gain = –63.5 dB

表 10-52. Page 0 / Register 44: Right DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Right DAC Digital Mute 0: The right DAC channel is not muted 1: The right DAC channel is muted
D6–D0	R/W	000 0000	Right DAC Digital Volume Control Setting 000 0000: Gain = 0 dB 000 0001: Gain = –0.5 dB 000 0010: Gain = –1 dB … 111 1101: Gain = –62.5 dB 111 1110: Gain = –63 dB 111 1111: Gain = –63.5 dB

10.6.1 Output Stage Volume Controls

A basic analog volume control with range from 0 dB to –78 dB and mute is replicated multiple times in the output stage network, connected to each of the analog signals that route to the output stage. In addition, to enable completely independent mixing operations to be performed for each output driver, each analog signal coming into the output stage may have up to seven separate volume controls. These volume controls all have approximately 0.5-dB step programmability over most of the gain range, with steps increasing slightly at the lowest attenuations. 表 10-53 lists the detailed gain versus programmed setting for this basic volume control.

表 10-53. Output Stage Volume Control Settings and Gains

GAIN SETTING	ANALOG GAIN (dB)	GAIN SETTING	ANALOG GAIN (dB)	GAIN SETTING	ANALOG GAIN (dB)	GAIN SETTING	ANALOG GAIN (dB)
0	0.0	30	–15.0	60	–30.1	90	–45.2
1	–0.5	31	–15.5	61	–30.6	91	–45.8
2	–1.0	32	–16.0	62	–31.1	92	–46.2
3	–1.5	33	–16.5	63	–31.6	93	–46.7
4	–2.0	34	–17.0	64	–32.1	94	–47.4
5	–2.5	35	–17.5	65	–32.6	95	–47.9
6	–3.0	36	–18.0	66	–33.1	96	–48.2
7	–3.5	37	–18.6	67	–33.6	97	–48.7
8	–4.0	38	–19.1	68	–34.1	98	–49.3
9	–4.5	39	–19.6	69	–34.6	99	–50.0
10	–5.0	40	–20.1	70	–35.1	100	–50.3
11	–5.5	41	–20.6	71	–35.7	101	–51.0
12	–6.0	42	–21.1	72	–36.1	102	–51.4
13	–6.5	43	–21.6	73	–36.7	103	–51.8
14	–7.0	44	–22.1	74	–37.1	104	–52.2
15	–7.5	45	–22.6	75	–37.7	105	–52.7
16	–8.0	46	–23.1	76	–38.2	106	–53.7
17	–8.5	47	–23.6	77	–38.7	107	–54.2
18	–9.0	48	–24.1	78	–39.2	108	–55.3
19	–9.5	49	–24.6	79	–39.7	109	–56.7
20	–10.0	50	–25.1	80	–40.2	110	–58.3
21	–10.5	51	–25.6	81	–40.7	111	–60.2
22	–11.0	52	–26.1	82	–41.2	112	–62.7
23	–11.5	53	–26.6	83	–41.7	113	–64.3
24	–12.0	54	–27.1	84	–42.2	114	–66.2
25	–12.5	55	–27.6	85	–42.7	115	–68.7
26	–13.0	56	–28.1	86	–43.2	116	–72.2
27	–13.5	57	–28.6	87	–43.8	117	–78.3
28	–14.0	58	–29.1	88	–44.3	118–127	Mute
29	–14.5	59	–29.6	89	–44.8		

表 10-54. Page 0 / Register 45: LINE2L to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Output Routing Control 0: LINE2L is not routed to HPLOUT 1: LINE2L is routed to HPLOUT
D6–D0	R/W	000 0000	LINE2L to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-55. Page 0 / Register 46: PGA_L to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPLOUT 1: PGA_L is routed to HPLOUT
D6–D0	R/W	000 0000	PGA_L to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-56. Page 0 / Register 47: DAC_L1 to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPLOUT 1: DAC_L1 is routed to HPLOUT
D6–D0	R/W	000 0000	DAC_L1 to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-57. Page 0 / Register 48: LINE2R to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Output Routing Control 0: LINE2R is not routed to HPLOUT 1: LINE2R is routed to HPLOUT
D6–D0	R/W	000 0000	LINE2R to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-58. Page 0 / Register 49: PGA_R to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPLOUT 1: PGA_R is routed to HPLOUT
D6–D0	R/W	000 0000	PGA_R to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-59. Page 0 / Register 50:DAC_R1 to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPLOUT 1: DAC_R1 is routed to HPLOUT
D6–D0	R/W	000 0000	DAC_R1 to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-60. Page 0 / Register 51: HPLOUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPLOUT Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLOUT Mute 0: HPLOUT is muted 1: HPLOUT is not muted
D2	R/W	1	HPLOUT Power Down Drive Control 0: HPLOUT is weakly driven to a common-mode when powered down 1: HPLOUT is high-impedance when powered down
D1	R	1	HPLOUT Volume Control Status 0: All programmed gains to HPLOUT have been applied 1: Not all programmed gains to HPLOUT have been applied yet
D0	R/W	0	HPLOUT Power Control 0: HPLOUT is not fully powered up 1: HPLOUT is fully powered up

表 10-61. Page 0 / Register 52: LINE2L to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Output Routing Control 0: LINE2L is not routed to HPLCOM 1: LINE2L is routed to HPLCOM
D6–D0	R/W	000 0000	LINE2L to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-62. Page 0 / Register 53: PGA_L to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPLCOM 1: PGA_L is routed to HPLCOM
D6–D0	R/W	000 0000	PGA_L to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-63. Page 0 / Register 54: DAC_L1 to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPLCOM 1: DAC_L1 is routed to HPLCOM
D6–D0	R/W	000 0000	DAC_L1 to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-64. Page 0 / Register 55: LINE2R to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Output Routing Control 0: LINE2R is not routed to HPLCOM 1: LINE2R is routed to HPLCOM
D6–D0	R/W	000 0000	LINE2R to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-65. Page 0 / Register 56: PGA_R to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPLCOM 1: PGA_R is routed to HPLCOM
D6–D0	R/W	000 0000	PGA_R to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-66. Page 0 / Register 57: DAC_R1 to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPLCOM 1: DAC_R1 is routed to HPLCOM
D6–D0	R/W	000 0000	DAC_R1 to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-67. Page 0 / Register 58: HPLCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPLCOM Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLCOM Mute 0: HPLCOM is muted 1: HPLCOM is not muted
D2	R/W	1	HPLCOM Power Down Drive Control 0: HPLCOM is weakly driven to a common-mode when powered down 1: HPLCOM is high-impedance when powered down.
D1	R	1	HPLCOM Volume Control Status 0: All programmed gains to HPLCOM have been applied 1: Not all programmed gains to HPLCOM have been applied yet
D0	R/W	0	HPLCOM Power Control 0: HPLCOM is not fully powered up 1: HPLCOM is fully powered up

表 10-68. Page 0 / Register 59: LINE2L to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Output Routing Control 0: LINE2L is not routed to HPROUT 1: LINE2L is routed to HPROUT
D6–D0	R/W	000 0000	LINE2L to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-69. Page 0 / Register 60: PGA_L to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPROUT 1: PGA_L is routed to HPROUT
D6–D0	R/W	000 0000	PGA_L to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-70. Page 0 / Register 61: DAC_L1 to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPROUT 1: DAC_L1 is routed to HPROUT
D6–D0	R/W	000 0000	DAC_L1 to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-71. Page 0 / Register 62: LINE2R to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Output Routing Control 0: LINE2R is not routed to HPROUT 1: LINE2R is routed to HPROUT
D6–D0	R/W	000 0000	LINE2R to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-72. Page 0 / Register 63: PGA_R to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPROUT 1: PGA_R is routed to HPROUT
D6–D0	R/W	000 0000	PGA_R to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-73. Page 0 / Register 64: DAC_R1 to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPROUT 1: DAC_R1 is routed to HPROUT
D6–D0	R/W	000 0000	DAC_R1 to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-74. Page 0 / Register 65: HPROUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPROUT Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPROUT Mute 0: HPROUT is muted 1: HPROUT is not muted
D2	R/W	1	HPROUT Power Down Drive Control 0: HPROUT is weakly driven to a common-mode when powered down 1: HPROUT is high-impedance when powered down
D1	R	1	HPROUT Volume Control Status 0: All programmed gains to HPROUT have been applied 1: Not all programmed gains to HPROUT have been applied yet
D0	R/W	0	HPROUT Power Control 0: HPROUT is not fully powered up 1: HPROUT is fully powered up

表 10-75. Page 0 / Register 66: LINE2L to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Output Routing Control 0: LINE2L is not routed to HPRCOM 1: LINE2L is routed to HPRCOM
D6–D0	R/W	000 0000	LINE2L to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-76. Page 0 / Register 67: PGA_L to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPRCOM 1: PGA_L is routed to HPRCOM
D6–D0	R/W	000 0000	PGA_L to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-77. Page 0 / Register 68: DAC_L1 to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPRCOM 1: DAC_L1 is routed to HPRCOM
D6–D0	R/W	000 0000	DAC_L1 to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-78. Page 0 / Register 69: LINE2R to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Output Routing Control 0: LINE2R is not routed to HPRCOM 1: LINE2R is routed to HPRCOM
D6–D0	R/W	000 0000	LINE2R to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-79. Page 0 / Register 70: PGA_R to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPRCOM 1: PGA_R is routed to HPRCOM
D6–D0	R/W	000 0000	PGA_R to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-80. Page 0 / Register 71: DAC_R1 to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPRCOM 1: DAC_R1 is routed to HPRCOM
D6–D0	R/W	000 0000	DAC_R1 to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-81. Page 0 / Register 72: HPRCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPRCOM Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPRCOM Mute 0: HPRCOM is muted 1: HPRCOM is not muted
D2	R/W	1	HPRCOM Power Down Drive Control 0: HPRCOM is weakly driven to a common-mode when powered down 1: HPRCOM is high-impedance when powered down
D1	R	1	HPRCOM Volume Control Status 0: All programmed gains to HPRCOM have been applied 1: Not all programmed gains to HPRCOM have been applied yet
D0	R/W	0	HPRCOM Power Control 0: HPRCOM is not fully powered up 1: HPRCOM is fully powered up

表 10-82. Page 0 / Register 73: LINE2L to MONO_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Output Routing Control 0: LINE2L is not routed to MONO_LOP/M 1: LINE2L is routed to MONO_LOP/M
D6–D0	R/W	000 0000	LINE2L to MONO_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-83. Page 0 / Register 74: PGA_L to MONO_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to MONO_LOP/M 1: PGA_L is routed to MONO_LOP/M
D6–D0	R/W	000 0000	PGA_L to MONO_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-84. Page 0 / Register 75: DAC_L1 to MONO_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to MONO_LOP/M 1: DAC_L1 is routed to MONO_LOP/M
D6–D0	R/W	000 0000	DAC_L1 to MONO_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-85. Page 0 / Register 76: LINE2R to MONO_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Output Routing Control 0: LINE2R is not routed to MONO_LOP/M 1: LINE2R is routed to MONO_LOP/M
D6–D0	R/W	000 0000	LINE2R to MONO_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-86. Page 0 / Register 77: PGA_R to MONO_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to MONO_LOP/M 1: PGA_R is routed to MONO_LOP/M
D6–D0	R/W	000 0000	PGA_R to MONO_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-87. Page 0 / Register 78: DAC_R1 to MONO_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to MONO_LOP/M 1: DAC_R1 is routed to MONO_LOP/M
D6–D0	R/W	000 0000	DAC_R1 to MONO_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-88. Page 0 / Register 79: MONO_LOP/M Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	MONO_LOP/M Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	MONO_LOP/M Mute 0: MONO_LOP/M is muted 1: MONO_LOP/M is not muted
D2	R	0	Reserved. Don't write to this register bit.
D1	R	1	MONO_LOP/M Volume Control Status 0: All programmed gains to MONO_LOP/M have been applied 1: Not all programmed gains to MONO_LOP/M have been applied yet
D0	R	0	MONO_LOP/M Power Status 0: MONO_LOP/M is not fully powered up 1: MONO_LOP/M is fully powered up

表 10-89. Page 0 / Register 80: LINE2L to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Output Routing Control 0: LINE2L is not routed to LEFT_LOP/M 1: LINE2L is routed to LEFT_LOP/M
D6–D0	R/W	000 0000	LINE2L to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-90. Page 0 / Register 81: PGA_L to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to LEFT_LOP/M 1: PGA_L is routed to LEFT_LOP/M
D6–D0	R/W	000 0000	PGA_L to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-91. Page 0 / Register 82: DAC_L1 to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to LEFT_LOP/M 1: DAC_L1 is routed to LEFT_LOP/M
D6–D0	R/W	000 0000	DAC_L1 to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-92. Page 0 / Register 83: LINE2R to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Output Routing Control 0: LINE2R is not routed to LEFT_LOP/M 1: LINE2R is routed to LEFT_LOP/M
D6–D0	R/W	000 0000	LINE2R to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-93. Page 0 / Register 84: PGA_R to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to LEFT_LOP/M 1: PGA_R is routed to LEFT_LOP/M
D6–D0	R/W	000 0000	PGA_R to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-94. Page 0 / Register 85: DAC_R1 to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to LEFT_LOP/M 1: DAC_R1 is routed to LEFT_LOP/M
D6–D0	R/W	000 0000	DAC_R1 to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-95. Page 0 / Register 86: LEFT_LOP/M Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	LEFT_LOP/M Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	LEFT_LOP/M Mute 0: LEFT_LOP/M is muted 1: LEFT_LOP/M is not muted
D2	R	0	Reserved. Don't write to this register bit.
D1	R	1	LEFT_LOP/M Volume Control Status 0: All programmed gains to LEFT_LOP/M have been applied 1: Not all programmed gains to LEFT_LOP/M have been applied yet
D0	R	0	LEFT_LOP/M Power Status 0: LEFT_LOP/M is not fully powered up 1: LEFT_LOP/M is fully powered up

表 10-96. Page 0 / Register 87: LINE2L to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2L Output Routing Control 0: LINE2L is not routed to RIGHT_LOP/M 1: LINE2L is routed to RIGHT_LOP/M
D6–D0	R/W	000 0000	LINE2L to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-97. Page 0 / Register 88: PGA_L to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to RIGHT_LOP/M 1: PGA_L is routed to RIGHT_LOP/M
D6–D0	R/W	000 0000	PGA_L to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-98. Page 0 / Register 89: DAC_L1 to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to RIGHT_LOP/M 1: DAC_L1 is routed to RIGHT_LOP/M
D6–D0	R/W	000 0000	DAC_L1 to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-99. Page 0 / Register 90: LINE2R to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2R Output Routing Control 0: LINE2R is not routed to RIGHT_LOP/M 1: LINE2R is routed to RIGHT_LOP/M
D6–D0	R/W	000 0000	LINE2R to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-100. Page 0 / Register 91: PGA_R to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to RIGHT_LOP/M 1: PGA_R is routed to RIGHT_LOP/M
D6–D0	R/W	000 0000	PGA_R to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-101. Page 0 / Register 92: DAC_R1 to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to RIGHT_LOP/M 1: DAC_R1 is routed to RIGHT_LOP/M
D6–D0	R/W	000 0000	DAC_R1 to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see 表 10-53

表 10-102. Page 0 / Register 93: RIGHT_LOP/M Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	RIGHT_LOP/M Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	RIGHT_LOP/M Mute 0: RIGHT_LOP/M is muted 1: RIGHT_LOP/M is not muted
D2	R	0	Reserved. Don't write to this register bit.
D1	R	1	RIGHT_LOP/M Volume Control Status 0: All programmed gains to RIGHT_LOP/M have been applied 1: Not all programmed gains to RIGHT_LOP/M have been applied yet
D0	R	0	RIGHT_LOP/M Power Status 0: RIGHT_LOP/M is not fully powered up 1: RIGHT_LOP/M is fully powered up

表 10-103. Page 0 / Register 94: Module Power Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Power Status 0: Left DAC not fully powered up 1: Left DAC fully powered up
D6	R	0	Right DAC Power Status 0: Right DAC not fully powered up 1: Right DAC fully powered up
D5	R	0	MONO_LOP/M Power Status 0: MONO_LOP/M output driver powered down 1: MONO_LOP/M output driver powered up
D4	R	0	LEFT_LOP/M Power Status 0: LEFT_LOP/M output driver powered down 1: LEFT_LOP/M output driver powered up
D3	R	0	RIGHT_LOP/M Power Status 0: RIGHT_LOP/M is not fully powered up 1: RIGHT_LOP/M is fully powered up
D2	R	0	HPLOUT Driver Power Status 0: HPLOUT Driver is not fully powered up 1: HPLOUT Driver is fully powered up
D1	R	0	HPROUT Driver Power Status 0: HPROUT Driver is not fully powered up 1: HPROUT Driver is fully powered up
D0	R	0	Reserved. Do not write to this register bit.

表 10-104. Page 0 / Register 95: Output Driver Short Circuit Detection Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short circuit detected at HPLOUT 1: Short circuit detected at HPLOUT
D6	R	0	HPROUT Short Circuit Detection Status 0: No short circuit detected at HPROUT 1: Short circuit detected at HPROUT
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short circuit detected at HPLCOM 1: Short circuit detected at HPLCOM

表 10-104. Page 0 / Register 95: Output Driver Short Circuit Detection Status Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short circuit detected at HPRCOM 1: Short circuit detected at HPRCOM
D3	R	0	HPLCOM Power Status 0: HPLCOM is not fully powered up 1: HPLCOM is fully powered up
D2	R	0	HPRCOM Power Status 0: HPRCOM is not fully powered up 1: HPRCOM is fully powered up
D1–D0	R	00	Reserved. Do not write to these register bits.

表 10-105. Page 0 / Register 96: Sticky Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short circuit detected at HPLOUT driver 1: Short circuit detected at HPLOUT driver
D6	R	0	HPROUT Short Circuit Detection Status 0: No short circuit detected at HPROUT driver 1: Short circuit detected at HPROUT driver
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short circuit detected at HPLCOM driver 1: Short circuit detected at HPLCOM driver
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short circuit detected at HPRCOM driver 1: Short circuit detected at HPRCOM driver
D3	R	0	Button Press Detection Status 0: No Headset Button Press detected 1: Headset Button Pressed
D2	R	0	Headset Detection Status 0: No Headset insertion/removal is detected 1: Headset insertion/removal is detected
D1	R	0	Left ADC AGC Noise Gate Status 0: Left ADC Signal Power Greater than Noise Threshold for Left AGC 1: Left ADC Signal Power Lower than Noise Threshold for Left AGC
D0	R	0	Right ADC AGC Noise Gate Status 0: Right ADC Signal Power Greater than Noise Threshold for Right AGC 1: Right ADC Signal Power Lower than Noise Threshold for Right AGC

表 10-106. Page 0 / Register 97: Real-Time Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short circuit detected at HPLOUT driver 1: Short circuit detected at HPLOUT driver
D6	R	0	HPROUT Short Circuit Detection Status 0: No short circuit detected at HPROUT driver 1: Short circuit detected at HPROUT driver
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short circuit detected at HPLCOM driver 1: Short circuit detected at HPLCOM driver
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short circuit detected at HPRCOM driver 1: Short circuit detected at HPRCOM driver

表 10-106. Page 0 / Register 97: Real-Time Interrupt Flags Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R	0	Button Press Detection Status[(1)] 0: No Headset Button Press detected 1: Headset Button Pressed
D2	R	0	Headset Detection Status 0: No Headset is detected 1: Headset is detected
D1	R	0	Left ADC AGC Noise Gate Status 0: Left ADC Signal Power Greater than Noise Threshold for Left AGC 1: Left ADC Signal Power Lower than Noise Threshold for Left AGC
D0	R	0	Right ADC AGC Noise Gate Status 0: Right ADC Signal Power Greater than Noise Threshold for Right AGC 1: Right ADC Signal Power Lower than Noise Threshold for Right AGC

(1) This bit is a sticky bit, cleared only when page 0, register 14 is read.

表 10-107. Page 0 / Register 98: GPIO1 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	GPIO1 Output Control 0000: GPIO1 is disabled 0001: GPIO1 used for audio serial data bus ADC word clock 0010: GPIO1 output = clock mux output divided by 1 (M=1) 0011: GPIO1 output = clock mux output divided by 2 (M=2) 0100: GPIO1 output = clock mux output divided by 4 (M=4) 0101: GPIO1 output = clock mux output divided by 8 (M=8) 0110: GPIO1 output = short circuit interrupt 0111: GPIO1 output = AGC noise interrupt 1000: GPIO1 = general purpose input 1001: GPIO1 = general purpose output 1010: GPIO1 output = digital microphone modulator clock 1011: GPIO1 = word clock for audio serial data bus (programmable as input or output) 1100: GPIO1 output = hook-switch/button press interrupt (interrupt polarity: active high, typical interrupt duration: button pressed time + clock resolution. Clock resolution depends upon debounce programmability. Typical interrupt delay from button: debounce duration + 0.5ms) 1101: GPIO1 output = jack/headset detection interrupt 1110: GPIO1 output = jack/headset detection interrupt OR button press interrupt 1111: GPIO1 output = jack/headset detection OR button press OR Short Circuit detection OR AGC Noise detection interrupt
D3	R/W	0	GPIO1 Clock Mux Output Control 0: GPIO1 clock mux output = PLL output 1: GPIO1 clock mux output = clock divider mux output
D2	R/W	0	GPIO1 Interrupt Duration Control 0: GPIO1 Interrupt occurs as a single active-high pulse of typical duration 2ms. 1: GPIO1 Interrupt occurs as continuous pulses until the Interrupt Flags register (register 96) is read by the host
D1	R	0	GPIO1 General Purpose Input Value 0: A logic-low level is input to GPIO1 1: A logic-high level is input to GPIO1
D0	R/W	0	GPIO1 General Purpose Output Value 0: GPIO1 outputs a logic-low level 1: GPIO1 outputs a logic-high level

表 10-108. Page 0 / Register 99: GPIO2 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	GPIO2 Output Control 0000: GPIO2 is disabled 0001: Reserved. Do not use. 0010: GPIO2 output = jack/headset detect interrupt (interrupt polarity: active high. Typical interrupt duration: 1.75 ms.) 0011: GPIO2 = general purpose input 0100: GPIO2 = general purpose output 0101–0111: GPIO2 input = digital microphone input, data sampled on clock rising and falling edges 1000: GPIO2 = bit clock for audio serial data bus (programmable as input or output) 1001: GPIO2 output = Headset detect OR button press interrupt 1010: GPIO2 output = Headset detect OR button press OR short-circuit detect OR AGC noise detect interrupt 1011: GPIO2 output = Short-circuit detect OR AGC noise detect interrupt 1100: GPIO2 output = Headset detect OR button press OR short-circuit detect interrupt 1101: GPIO2 output = Short-circuit detect interrupt 1110: GPIO2 output = AGC noise detect interrupt 1111: GPIO2 output = Button press / hookswitch interrupt
D3	R/W	0	GPIO2 General Purpose Output Value 0: GPIO1 outputs a logic-low level 1: GPIO1 outputs a logic-high level
D2	R	0	GPIO2 General Purpose Input Value 0: A logic-low level is input to GPIO2 1: A logic-high level is input to GPIO2
D1	R/W	0	GPIO2 Interrupt Duration Control 0: GPIO2 Interrupt occurs as a single active-high pulse of typical duration 2ms. 1: GPIO2 Interrupt occurs as continuous pulses until the Interrupt Flags register (register 96) is read by the host
D0	R	0	Reserved. Don’t write to this register bit.

表 10-109. Page 0 / Register 100: Additional GPIO Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	SDA Pin Control [(1)] The SDA pin hardware includes pulldown capability only (open-drain NMOS), so an external pullup resistor is required when using this pin, even in GPIO mode. 00: SDA pin is not used as general purpose I/O 01: SDA pin used as general purpose input 10: SDA pin used as general purpose output 11: Reserved. Do not write this sequence to these register bits.
D5	R/W	0	SDA General Purpose Output Control [(1)] 0: SDA driven to logic-low when used as general-purpose output 1: SDA driven to logic-high when used as general-purpose output (requires external pullup resistor)
D4	R	0	SDA General Purpose Input Value [(1)] 0: SDA detects a logic-low when used as general-purpose input 1: SDA is detects a logic-high when used as general purpose input
D3–D2	R/W	00	SCL Pin Control[(1)] The SCL pin hardware includes pulldown capability only (open-drain NMOS), so an external pullup resistor is required when using this pin, even in GPIO mode. 00: SCL pin is not used as general purpose I/O 01: SCL pin used as general purpose input 10: SCL pin used as general purpose output 11: Reserved. Do not write this sequence to these register bits.
D1	R/W	0	SCL General Purpose Output Control [(1)] 0: SCL driven to logic-low when used as general-purpose output 1: SCL driven to logic-high when used as general-purpose output (requires external pullup resistor)
D0	R	0	SCL General Purpose Input Value [(1)] 0: SCL detects a logic-low when used as general-purpose input 1: SCL detects a logic-high when used as general-purpose input

(1) The control bits in Register 100 are only valid in SPI Mode, when SELECT=1.

表 10-110. Page 0 / Register 101: Additional GPIO Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	I^2C Address Pin #0 Status (1) 0: MFP1 pin = I^2C address pin #0 = 0 at reset 1: MFP1 pin = I^2C address pin #0 = 1 at reset
D6	R	0	I^2C Address Pin #1 Status (1) 0: MFP0 pin = I^2C address pin #1 = 0 at reset 1: MFP0 pin = I^2C address pin #1 = 1 at reset
D5	R/W	0	MFP3 Pin General Purpose Input Control (1) 0: MFP3 pin usage as general purpose input is disabled 1: MFP3 pin usage as general purpose input is enabled
D4	R/W	0	MFP3 Pin Serial Data Bus Input Control (1) 0: MFP3 pin usage as audio serial data input pin is disabled (SDIN) 1: MFP3 pin usage as audio serial data input pin is enabled (MOSI)
D3	R	0	MFP3 General Purpose Input Value (1) 0: MFP3 detects a logic-low when used as general-purpose input 1: MFP3 detects a logic-high when used as general-purpose input
D2	R/W	0	MFP2 General Purpose Output Control (1) 0: MFP2 pin usage as general purpose output is disabled 1: MFP2 pin usage as general purpose output is enabled
D1	R/W	0	MFP2 General Purpose Output Control (1) 0: MFP2 pin drives a logic-low when used as a general-purpose output 1: MFP2 pin drives a logic-high when used as a general-purpose output
D0	R/W	0	CODEC_CLKIN Source Selection 0: CODEC_CLKIN uses PLLDIV_OUT 1: CODEC_CLKIN uses CLKDIV_OUT

(1) Bits D7–D1 in Register 101 are only valid in I^2C control Mode, when SELECT = 0.

表 10-111. Page 0 / Register 102: Clock Generation Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	CLKDIV_IN Source Selection 00: CLKDIV_IN uses MCLK 01: CLKDIV_IN uses GPIO2 10: CLKDIV_IN uses BCLK 11: Reserved. Do not use.
D5–D4	R/W	00	PLLCLK_IN Source Selection 00: PLLCLK_IN uses MCLK 01: PLLCLK_IN uses GPIO2 10: PLLCLK _IN uses BCLK 11: Reserved. Do not use.
D3–D0	R/W	0010	PLL Clock Divider N Value 0000: N=16 0001: N=17 0010: N=2 0011: N=3 … 1111: N=15

表 10-112. Page 0 / Register 103: Left AGC New Programmable Attack Time Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Attack Time Register Selection 0: Attack time for the left AGC is generated from register 26. 1: Attack time for the left AGC is generated from this register.

表 10-112. Page 0 / Register 103: Left AGC New Programmable Attack Time Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D5	R/W	00	Baseline AGC Attack time 00: Left AGC attack time = 7 ms 01: Left AGC Attack time = 8 ms 10: Left AGC Attack time = 10 ms 11: Left AGC Attack time = 11 ms
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC Attack time = 1 001: Multiplication factor for the baseline AGC Attack time = 2 010: Multiplication factor for the baseline AGC Attack time = 4 011: Multiplication factor for the baseline AGC Attack time = 8 100: Multiplication factor for the baseline AGC Attack time = 16 101: Multiplication factor for the baseline AGC Attack time = 32 110: Multiplication factor for the baseline AGC Attack time = 64 111: Multiplication factor for the baseline AGC Attack time = 128
D1–D0	R/W	00	Reserved. Write only zero to these register bits.

表 10-113. Page 0 / Register 104: Left AGC New Programmable Decay Time Register(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Decay Time Register Selection 0: Decay time for the Left AGC is generated from Register 26. 1: Decay time for the Left AGC is generated from this Register.
D6–D5	R/W	00	Baseline AGC Decay time 00: Left AGC Decay time = 50 ms 01: Left AGC Decay time = 150 ms 10: Left AGC Decay time = 250 ms 11: Left AGC Decay time = 350 ms
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC Decay time = 1 001: Multiplication factor for the baseline AGC Decay time = 2 010: Multiplication factor for the baseline AGC Decay time = 4 011: Multiplication factor for the baseline AGC Decay time = 8 100: Multiplication factor for the baseline AGC Decay time = 16 101: Multiplication factor for the baseline AGC Decay time = 32 110: Multiplication factor for the baseline AGC Decay time = 64 111: Multiplication factor for the baseline AGC Decay time = 128
D1–D0	R/W	00	Reserved. Write only zero to these register bits.

(1) Decay time is limited based on NADC ratio that is selected. For
NADC = 1, Max Decay time = 4 seconds
NADC = 1.5, Max Decay time = 5.6 seconds
NADC = 2, Max Decay time = 8 seconds
NADC = 2.5, Max Decay time = 9.6 seconds
NADC = 3 or 3.5, Max Decay time = 11.2 seconds
NADC = 4 or 4.5, Max Decay time = 16 seconds
NADC = 5, Max Decay time = 19.2 seconds
NADC = 5.5 or 6, Max Decay time = 22.4 seconds

表 10-114. Page 0 / Register 105: Right AGC New Programmable Attack Time Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Attack Time Register Selection 0: Attack time for the Right AGC is generated from Register 29. 1: Attack time for the Right AGC is generated from this Register.
D6–D5	R/W	00	Baseline AGC Attack time 00: Right AGC Attack time = 7 ms 01: Right AGC Attack time = 8 ms 10: Right AGC Attack time = 10 ms 11: Right AGC Attack time = 11 ms

表 10-114. Page 0 / Register 105: Right AGC New Programmable Attack Time Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC Attack time = 1 001: Multiplication factor for the baseline AGC Attack time = 2 010: Multiplication factor for the baseline AGC Attack time = 4 011: Multiplication factor for the baseline AGC Attack time = 8 100: Multiplication factor for the baseline AGC Attack time = 16 101: Multiplication factor for the baseline AGC Attack time = 32 110: Multiplication factor for the baseline AGC Attack time = 64 111: Multiplication factor for the baseline AGC Attack time = 128
D1–D0	R/W	00	Reserved. Write only zero to these register bits.

表 10-115. Page 0 / Register 106: Right AGC New Programmable Decay Time Register(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Decay Time Register Selection 0: Decay time for the right AGC is generated from register 29. 1: Decay time for the right AGC is generated from this register.
D6–D5	R/W	00	Baseline AGC Decay time 00: Right AGC Decay time = 50 ms 01: Right AGC Decay time = 150 ms 10: Right AGC Decay time = 250 ms 11: Right AGC Decay time = 350 ms
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC Decay time = 1 001: Multiplication factor for the baseline AGC Decay time = 2 010: Multiplication factor for the baseline AGC Decay time = 4 011: Multiplication factor for the baseline AGC Decay time = 8 100: Multiplication factor for the baseline AGC Decay time = 16 101: Multiplication factor for the baseline AGC Decay time = 32 110: Multiplication factor for the baseline AGC Decay time = 64 111: Multiplication factor for the baseline AGC Decay time = 128
D1–D0	R/W	00	Reserved. Write only zero to these register bits.

(1) Decay time is limited based on NADC ratio that is selected. For
NADC = 1, Max Decay time = 4 seconds
NADC = 1.5, Max Decay time = 5.6 seconds
NADC = 2, Max Decay time = 8 seconds
NADC = 2.5, Max Decay time = 9.6 seconds
NADC = 3 or 3.5, Max Decay time = 11.2 seconds
NADC = 4 or 4.5, Max Decay time = 16 seconds
NADC = 5, Max Decay time = 19.2 seconds
NADC = 5.5 or 6, Max Decay time = 22.4 seconds

表 10-116. Page 0 / Register 107: New Programmable ADC Digital Path and I^{2}C Bus Condition Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Channel High Pass Filter Coefficient Selection 0: Default Coefficients are used when ADC High Pass is enabled. 1: Programmable Coefficients are used when ADC High Pass is enabled.
D6	R/W	0	Right Channel High Pass Filter Coefficient Selection 0: Default Coefficients are used when ADC High Pass is enabled. 1: Programmable Coefficients are used when ADC High Pass is enabled.
D5–D4	R/W	00	ADC Decimation Filter configuration 00: Left and Right Digital Microphones are used 01: Left Digital Microphone and Right Analog Microphone are used 10: Left Analog Microphone and Right Digital Microphone are used 11: Left and Right Analog Microphones are used
D3	R/W	0	ADC Digital output to Programmable Filter Path Selection 0: No additional Programmable Filters other than the HPF are used for the ADC. 1: The Programmable Filter is connected to ADC output, if both DACs are powered down.

表 10-116. Page 0 / Register 107: New Programmable ADC Digital Path and I²C Bus Condition Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R/W	0	I²C Bus Condition Detector 0: Internal logic is enabled to detect an I²C bus error, and clears the bus error condition. 1: Internal logic is disabled to detect an I²C bus error.
D1	R	0	Reserved. Write only zero to these register bits.
D0	R	0	I²C Bus error detection status 0: I²C bus error is not detected 1: I²C bus error is detected. This bit is cleared by reading this register.

表 10-117. Page 0 / Register 108: Passive Analog Signal Bypass Selection During Powerdown Register(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINE2RM Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to RIGHT_LOM
D6	R/W	0	LINE2RP Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to RIGHT_LOP
D5	R/W	0	LINE1RM Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to RIGHT_LOM
D4	R/W	0	LINE1RP Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to RIGHT_LOP
D3	R/W	0	LINE2LM Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to LEFT_LOM
D2	R/W	0	LINE2LP Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to LEFT_LOP
D1	R/W	0	LINE1LM Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to LEFT_LOM
D0	R/W	0	LINE1LP Path Selection 0: Normal Signal Path 1: Signal is routed by a switch to LEFT_LOP

(1) Based on the setting above, if BOTH LINE1 and LINE2 inputs are routed to the output at the same time, then the two switches used for the connection short the two input signals together on the output pins. The shorting resistance between the two input pins is two times the bypass switch resistance (Rdson). In general this condition of shorting should be avoided, as higher drive currents are likely to occur on the circuitry that feeds these two input pins of this device.

表 10-118. Page 0 / Register 109: DAC Quiescent Current Adjustment Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	DAC Current Adjustment 00: Default 01: 50% increase in DAC reference current 10: Reserved 11: 100% increase in DAC reference current
D5–D0	R/W	00 0000	Reserved. Write only zero to these register bits.

表 10-119. Page 0 / Register 110–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

表 10-120. Page 1 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	X	0000 000	Reserved, write only zeros to these register bits
D0	R/W	0	Page Select Bit Writing zero to this bit sets Page-0 as the active page for following register accesses. Writing a one to this bit sets Page-1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read/writes. This register has the same functionality on page-0 and page-1.

表 10-121. Page 1 / Register 1:Left Channel Audio Effects Filter N0 Coefficient MSB Register(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Left Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

(1) When programming any coefficient value in Page 1, the MSB register should always be written first, immediately followed by the LSB register. Even if only the MSB or LSB of the coefficient changes, both registers should be written in this sequence.

表 10-122. Page 1 / Register 2:Left Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Left Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-123. Page 1 / Register 3:Left Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Left Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-124. Page 1 / Register 4: Left Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Left Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-125. Page 1 / Register 5: Left Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Left Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-126. Page 1 / Register 6: Left Channel Audio Effects Filter N2 Coefficient LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Left Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-127. Page 1 / Register 7: Left Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Left Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-128. Page 1 / Register 8: Left Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Left Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-129. Page 1 / Register 9: Left Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Left Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-130. Page 1 / Register 10: Left Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Left Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-131. Page 1 / Register 11: Left Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Left Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-132. Page 1 / Register 12: Left Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Left Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-133. Page 1 / Register 13: Left Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Left Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-134. Page 1 / Register 14: Left Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Left Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-135. Page 1 / Register 15: Left Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0100	Left Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-136. Page 1 / Register 16: Left Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Left Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-137. Page 1 / Register 17: Left Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Left Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-138. Page 1 / Register 18: Left Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Left Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-139. Page 1 / Register 19: Left Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0100	Left Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-140. Page 1 / Register 20: Left Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Left Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-141. Page 1 / Register 21: Left Channel De-Emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0011 1001	Left Channel De-Emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-142. Page 1 / Register 22: Left Channel De-Emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Left Channel De-Emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-143. Page 1 / Register 23: Left Channel De-Emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Left Channel De-Emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-144. Page 1 / Register 24: Left Channel De-Emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Left Channel De-Emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-145. Page 1 / Register 25: Left Channel De-Emphasis Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Left Channel De-Emphasis Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-146. Page 1 / Register 26: Left Channel De-Emphasis Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Left Channel De-Emphasis Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-147. Page 1 / Register 27: Right Channel Audio Effects Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Right Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-148. Page 1 / Register 28: Right Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Right Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-149. Page 1 / Register 29: Right Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Right Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-150. Page 1 / Register 30: Right Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Right Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-151. Page 1 / Register 31: Right Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Right Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-152. Page 1 / Register 32: Right Channel Audio Effects Filter N2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Right Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-153. Page 1 / Register 33: Right Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Right Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-154. Page 1 / Register 34: Right Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Right Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-155. Page 1 / Register 35: Right Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Right Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-156. Page 1 / Register 36: Right Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Right Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-157. Page 1 / Register 37: Right Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Right Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-158. Page 1 / Register 38: Right Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Right Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-159. Page 1 / Register 39: Right Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Right Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-160. Page 1 / Register 40: Right Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Right Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to +32767.

表 10-161. Page 1 / Register 41: Right Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	10000100	Right Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-162. Page 1 / Register 42: Right Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Right Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-163. Page 1 / Register 43: Right Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Right Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-164. Page 1 / Register 44: Right Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Right Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-165. Page 1 / Register 45: Right Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0100	Right Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-166. Page 1 / Register 46: Right Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Right Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-167. Page 1 / Register 47: Right Channel De-Emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	00112's complement 1001	Right Channel De-Emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-168. Page 1 / Register 48: Right Channel De-Emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Right Channel De-Emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-169. Page 1 / Register 49: Right Channel De-Emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Right Channel De-Emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-170. Page 1 / Register 50: Right Channel De-Emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Right Channel De-Emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-171. Page 1 / Register 51: Right Channel De-Emphasis Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Right Channel De-Emphasis Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-172. Page 1 / Register 52: Right Channel De-Emphasis Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Right Channel De-Emphasis Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-173. Page 1 / Register 53: 3-D Attenuation Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1111	3-D Attenuation Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-174. Page 1 / Register 54: 3-D Attenuation Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 1111	3-D Attenuation Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-175. Page 1 / Register 55–64: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

表 10-176. Page 1 / Register 65: Left Channel ADC High Pass Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0011 1001	Left Channel ADC High Pass Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-177. Page 1 / Register 66: Left Channel ADC High Pass Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Left Channel ADC High Pass Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-178. Page 1 / Register 67: Left Channel ADC High Pass Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Left Channel ADC High Pass Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-179. Page 1 / Register 68: Left Channel ADC High Pass Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Left Channel ADC High Pass Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-180. Page 1 / Register 69: Left Channel ADC High Pass Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Left Channel ADC High Pass Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-181. Page 1 / Register 70: Left Channel ADC High Pass Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Left Channel ADC High Pass Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-182. Page 1 / Register 71: Right Channel ADC High Pass Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0011 1001	Right Channel ADC High Pass Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-183. Page 1 / Register 72: Right Channel ADC High Pass Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Right Channel ADC High Pass Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-184. Page 1 / Register 73: Right Channel ADC High Pass Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Right Channel ADC High Pass Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-185. Page 1 / Register 74: Right Channel ADC High Pass Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Right Channel ADC High Pass Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-186. Page 1 / Register 75: Right Channel ADC High Pass Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Right Channel ADC High Pass Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-187. Page 1 / Register 76: Right Channel ADC High Pass Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Right Channel ADC High Pass Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32768 to 32767.

表 10-188. Page 1 / Registers 77–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

The TLV320AIC3106 is a highly integrated low-power stereo audio codec with integrated stereo headphone/line amplifier, as well as multiple inputs and outputs that are programmable in single-ended or fully differential configurations. All the features of the TLV320AIC3106 are accessed by programmable registers. External processor with SPI or I^{2}C protocol is required to control the device, the protocol is selectable with external pin configuration. It is good practice to perform a hardware reset after initial power up to ensure that all registers are in their default states. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 14-mW from a 3.3-V analog supply, making it ideal for portable battery-powered audio and telephony applications.

11.2 Typical Application

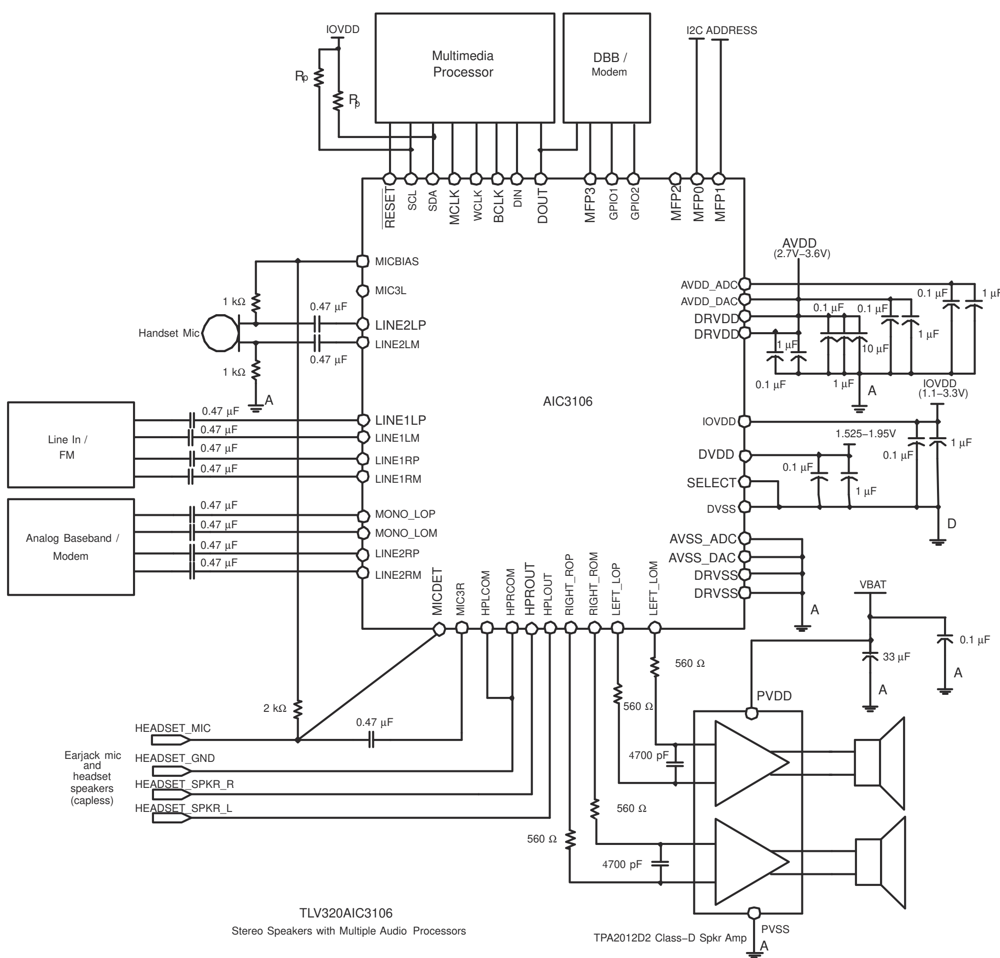


図 11-1. Typical Connections for Capless Headphone and External Speaker Amplifier

11.2.1 Design Requirements

For this design example, use the parameters shown in 表 11-1.

表 11-1. Design Parameters

PARAMETER	VALUE
Supply Voltage (AVDD, DRVDD)	3.3 V
Supply Voltage (DVDD, IOVDD)	1.8 V
Analog High-Power Output Driver load	16 Ω
Analog Fully Differential Line Output Driver load	10 kΩ

11.2.2 Detailed Design Procedure

Using the Typical Application Schematic as a guide, integrate the hardware into the system.

Following the recommended component placement, schematic layout and routing given in the *Layout Examples* section, integrate the device and its supporting components into the system PCB file.

- For questions and support go to the E2E forums (e2e.ti.com). If it is necessary to deviate from the recommended layout, visit the E2E forum to request a layout review.

As the TLV320AIC3106 can be controlled with I^2C or SPI protocol, the selection pin of the device should be connected properly.

Determining sample rate and Master clock frequency is required since powering up the device as all internal timing is derived from the master clock. See the *Audio Clock Generation* section in order to get more information of how to configure correctly the required clocks for the device.

As the TLV320AIC3106 is designed for low-power applications, when powered up, the device has several features powered down. A correct routing of the TLV320AIC3106 signals is achieved by a correct setting of the device registers, powering up the required stages of the device and configuring the internal switches to follow a desired route.

For more information of the device configuration and programming, see the TLV320AIC3106 technical documents section in ti.com (http://www.ti.com/product/TLV320AIC3106/technicaldocuments).

11.2.3 Application Curves

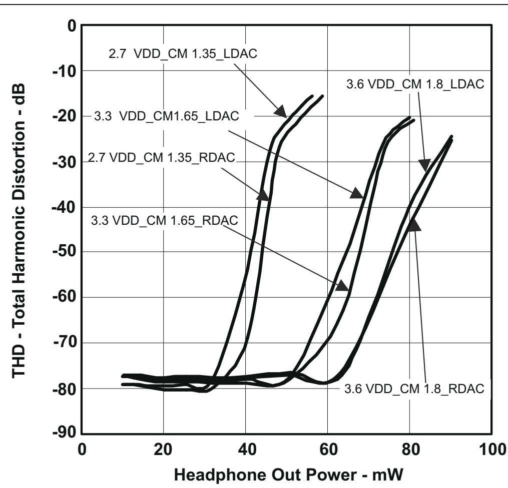


図 11-2. Total Harmonic Distortion vs Headphone Out Power

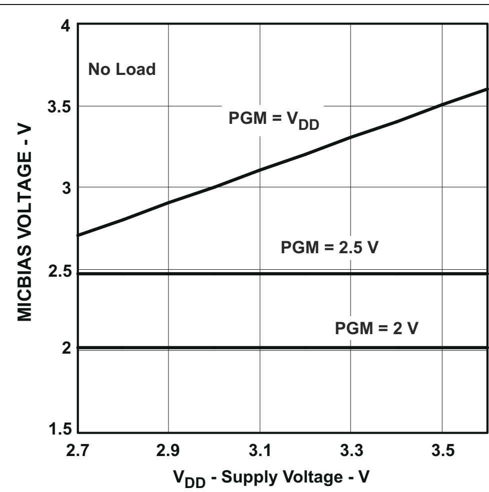


図 11-3. MICBIAS Voltage vs Supply Voltage

12 Power Supply Recommendations

The TLV320AIC3106 has been designed to be extremely tolerant of power supply sequencing. However, in some rare instances, unexpected conditions can be attributed to power supply sequencing. The following sequence provides the most robust operation.

IOVDD should be powered up first. The analog supplies, which include AVDD and DRVDD, should be powered up second. The digital supply DVDD should be powered up last. Keep $\overline{\text{RESET}}$ low until all supplies are stable. The analog supplies should be greater than or equal to DVDD at all times.

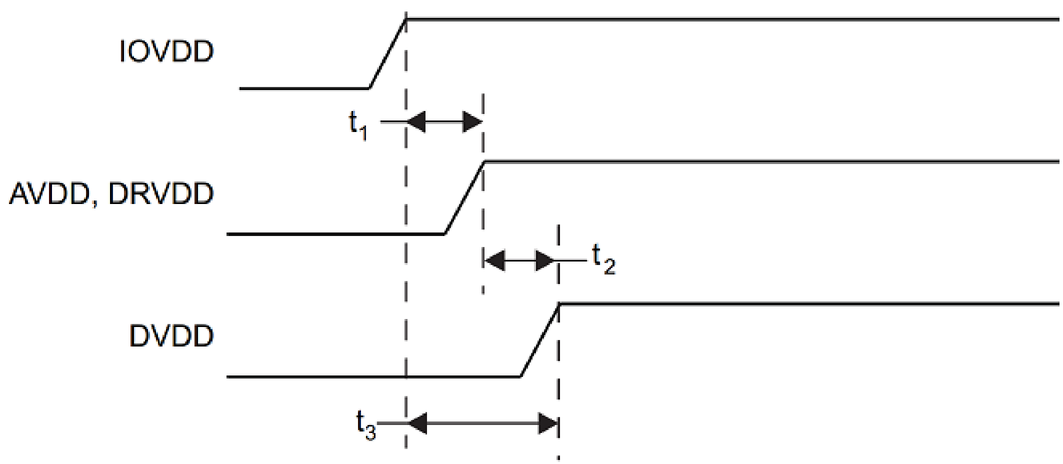


図 12-1. TLV320AIC3101 Power Supply Sequencing

表 12-1. TLV320AIC3101 Power Supply Sequencing

PARAMETER		MIN	MAX	UNIT
t_1	IOVDD to AVDD, DRVDD	0		ms
t_2	AVDD to DVDD	0	5	
t_3	IOVDD, to DVDD	0		

13 Layout

13.1 Layout Guidelines

PCB design is made considering the application, and the review is specific for each system requirements. However, general considerations can optimize the system performance.

- The TLV320AIC3106 thermal pad should be connected to analog output driver ground using multiple VIAS to minimize impedance between the device and ground.
- It is highly recommended to connect the NC central balls of the TLV320AIC3106IZQE to analog ground to enhance the device's thermal performance.
- Analog and digital grounds should be separated to prevent possible digital noise from affecting the analog performance of the board.
- The TLV320AIC3106 requires the decoupling capacitors to be placed as close as possible to the device power supply terminals.
- If possible, route the differential audio signals differentially on the PCB. This is recommended to get better noise immunity.

13.2 Layout Examples

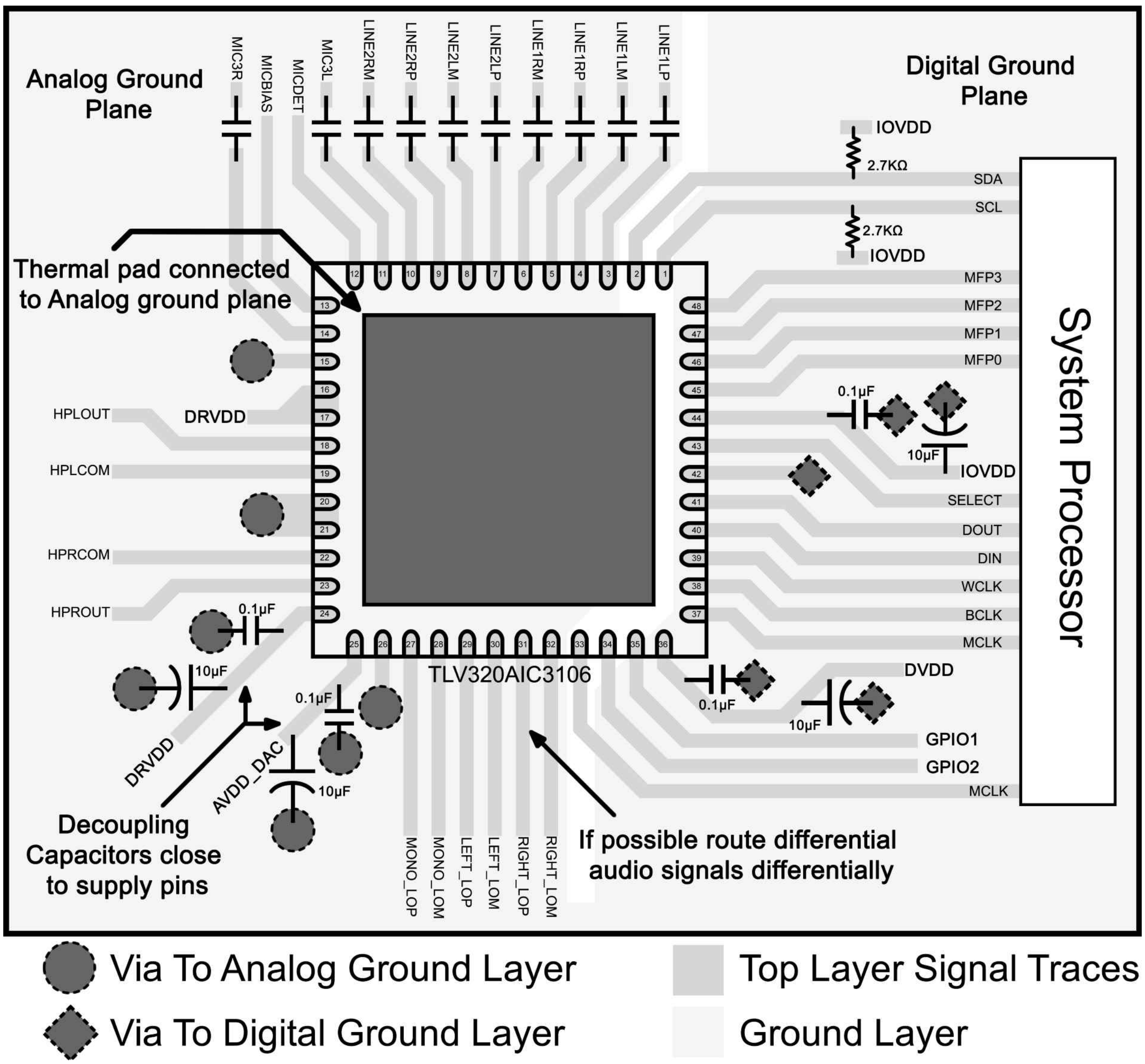


図 13-1. AIC3106 VQFN Layout Example

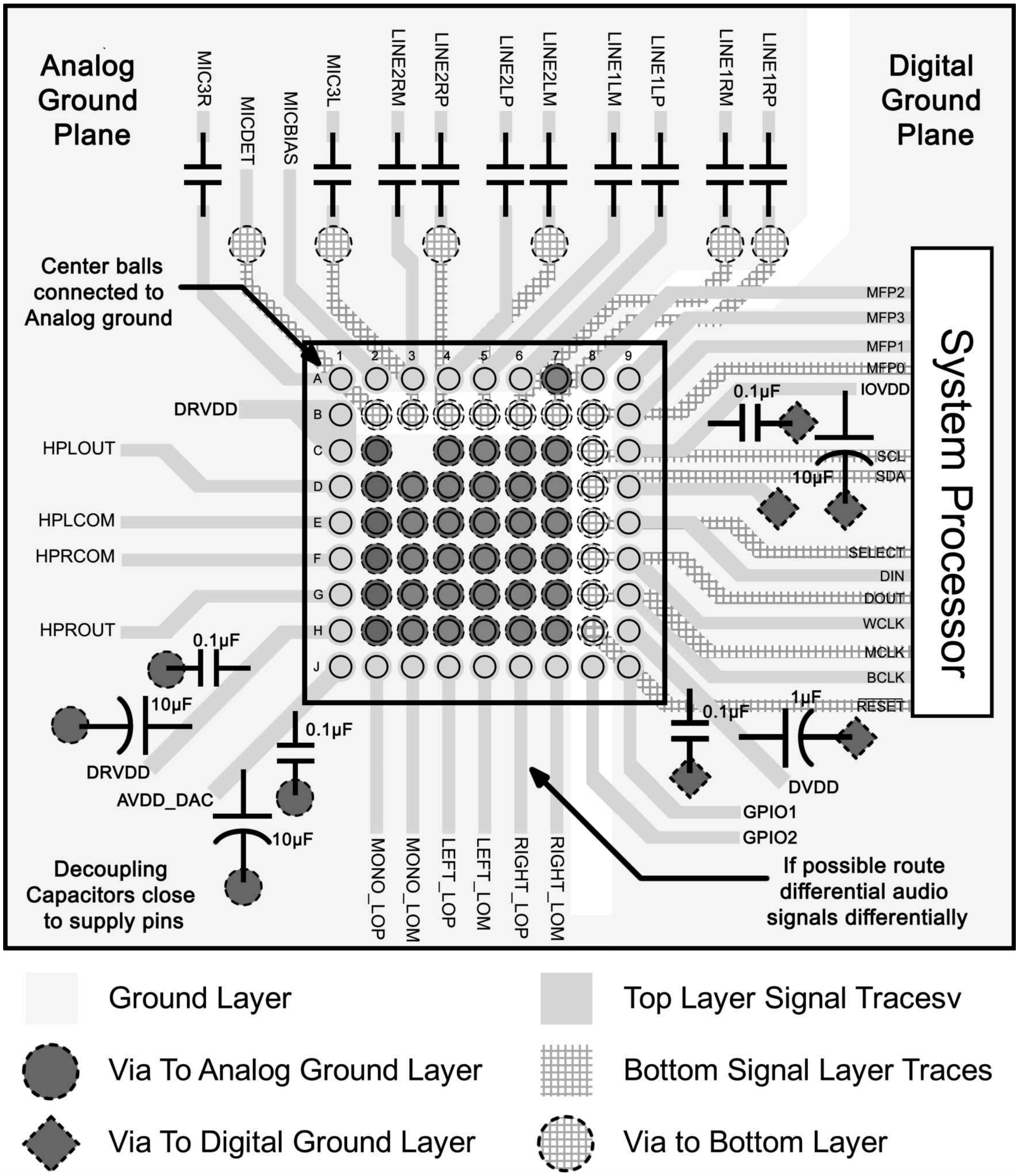


図 13-2. AIC3106 BGA Layout Example

14 Device and Documentation Support

14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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14.3 Trademarks

Bluetooth™ is a trademark of Bluetooth SIG, Inc.
MicroStar Junior™ and TI E2E™ are trademarks of Texas Instruments.
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14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320AIC3106IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AC3106I	Samples
TLV320AIC3106IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AC3106I	Samples
TLV320AIC3106IZXHR	ACTIVE	NFBGA	ZXH	80	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AC3106I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV320AIC3106 :

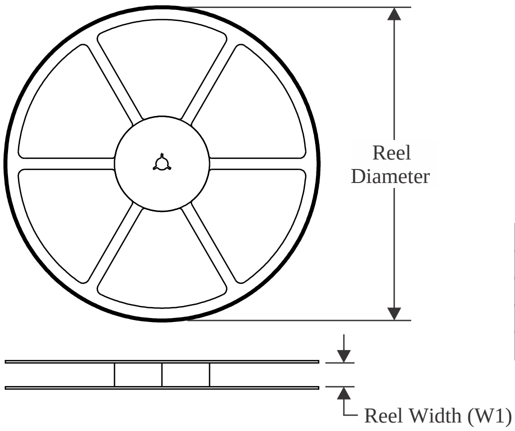
- Automotive : TLV320AIC3106-Q1

NOTE: Qualified Version Definitions:

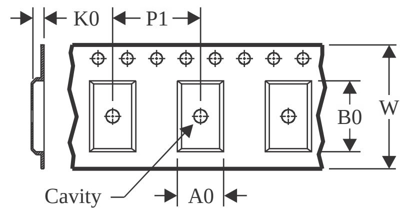
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

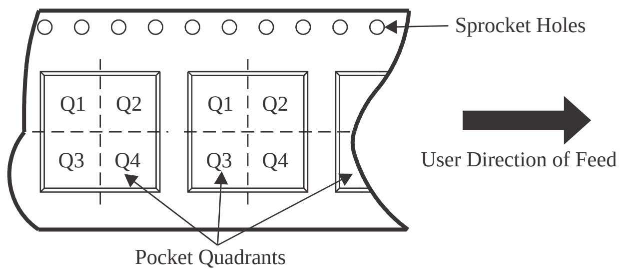


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

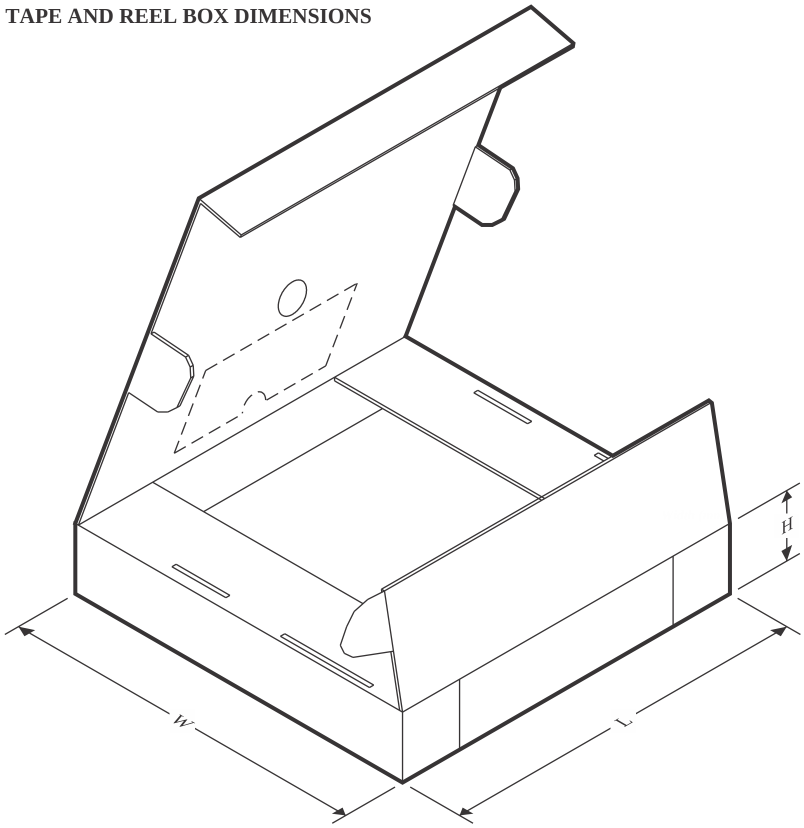
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3106IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TLV320AIC3106IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TLV320AIC3106IZXHR	NFBGA	ZXH	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

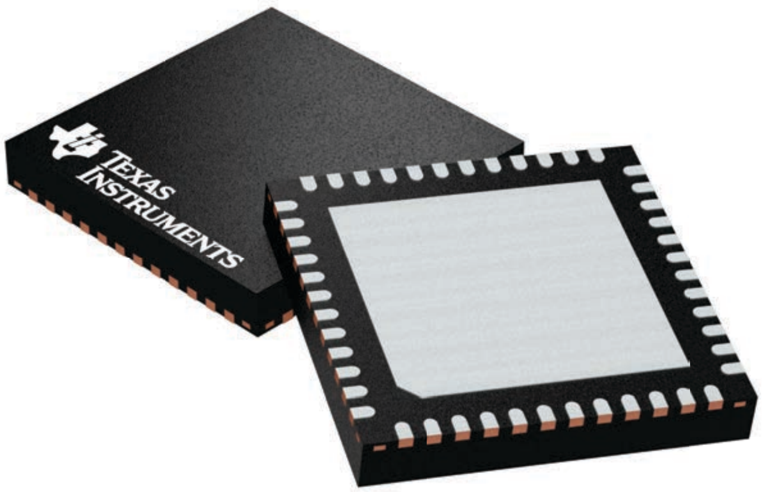
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3106IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TLV320AIC3106IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
TLV320AIC3106IZXHR	NFBGA	ZXH	80	2500	336.6	336.6	31.8

RGZ 48

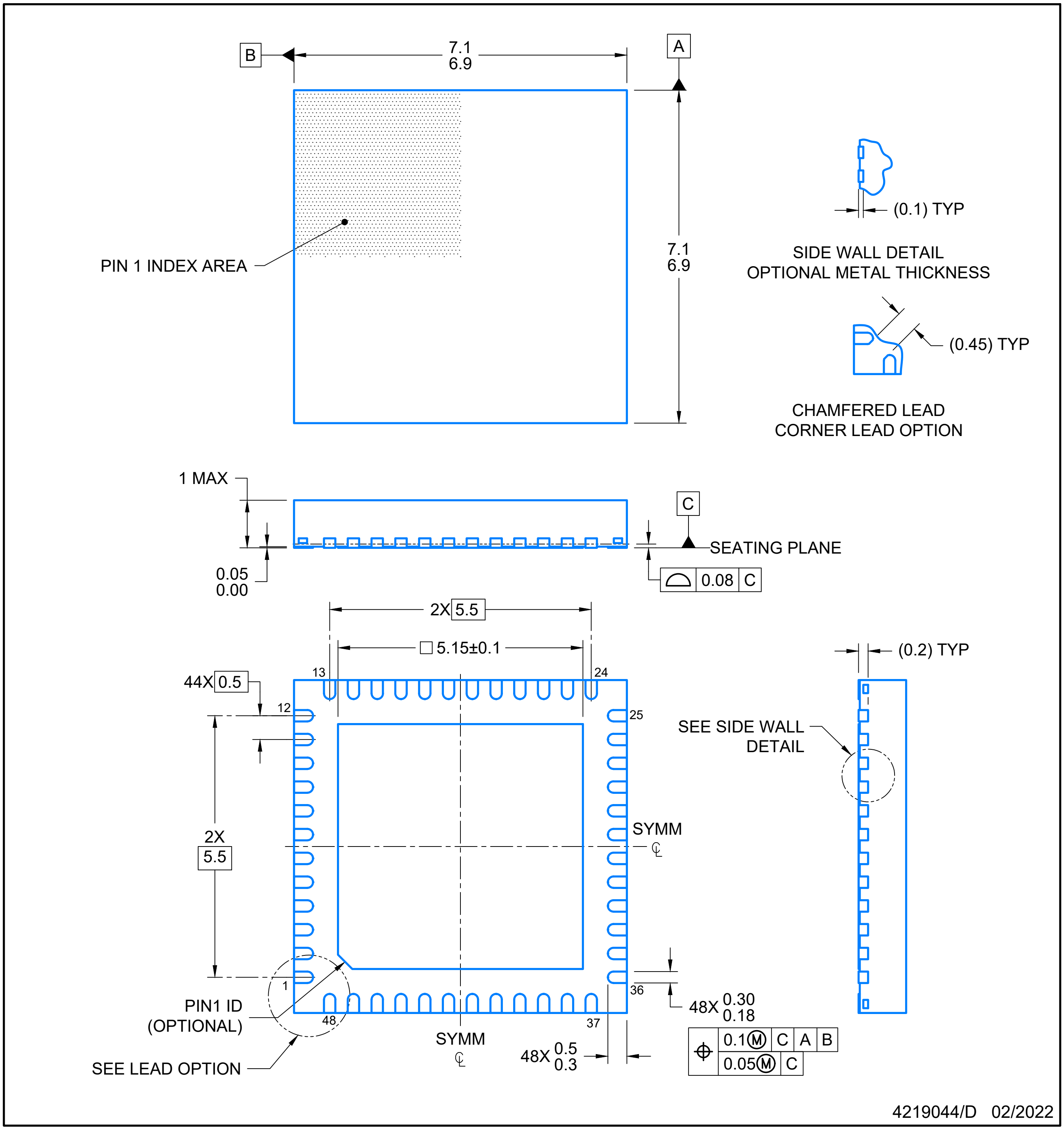
VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD

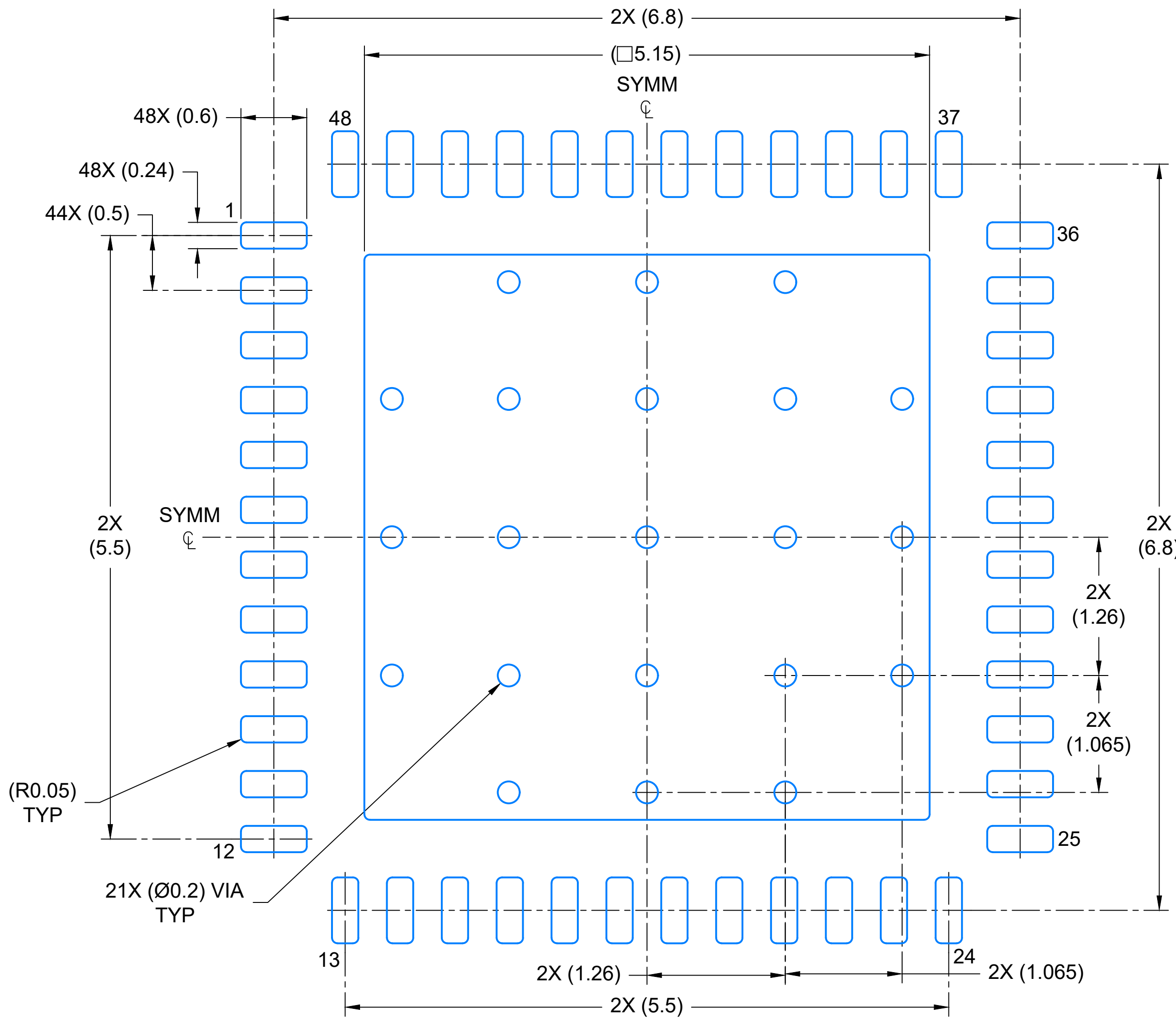


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

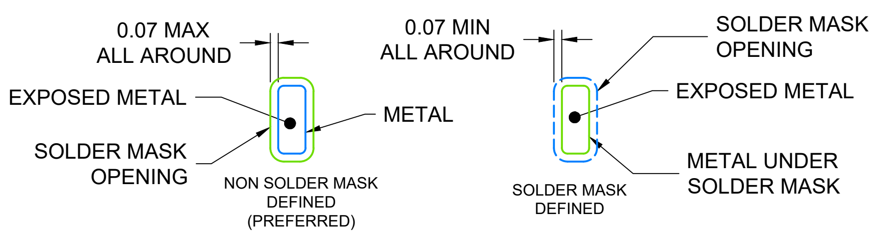


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X



SOLDER MASK DETAILS

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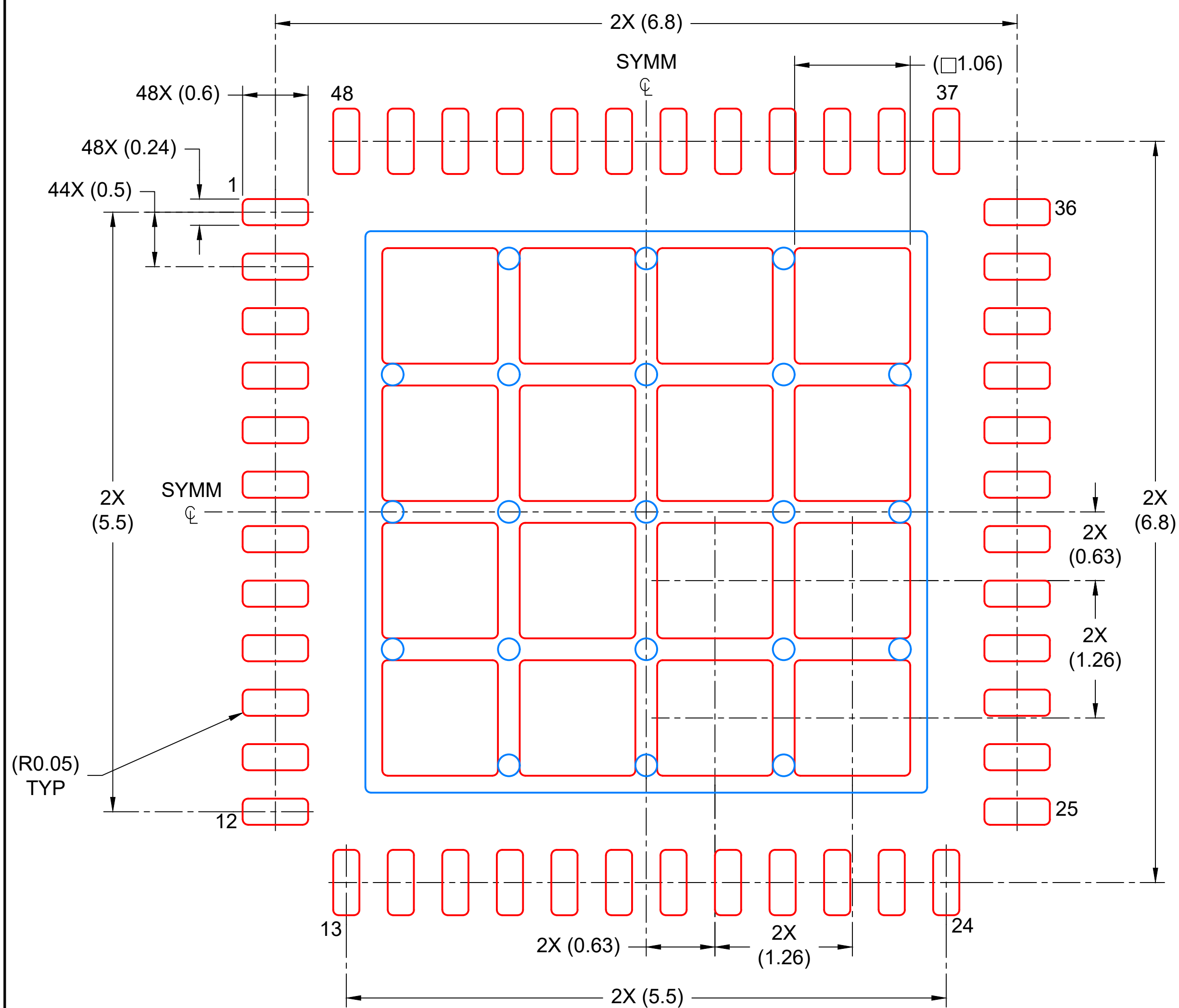
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

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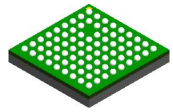
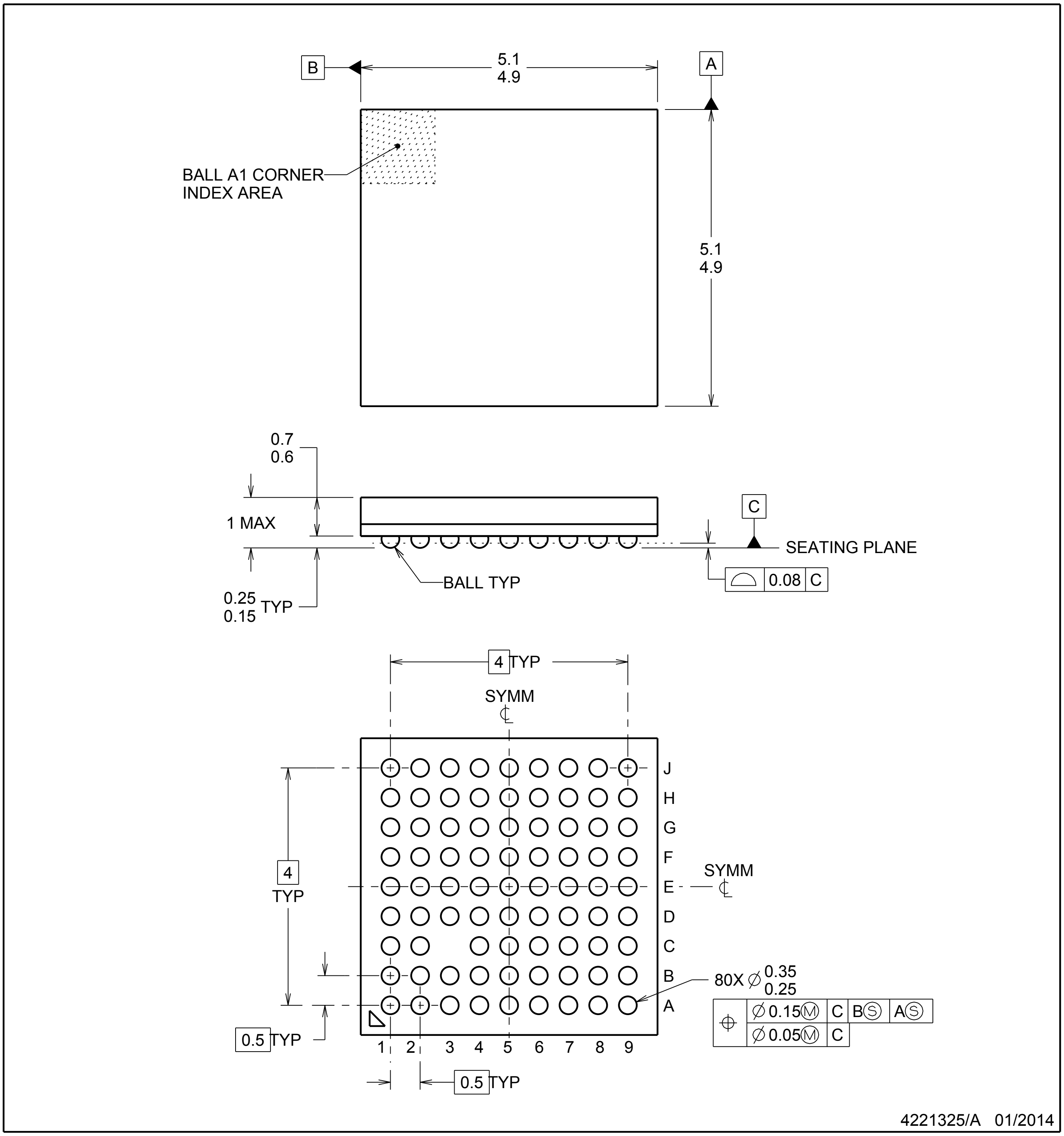
NOTES: (continued)

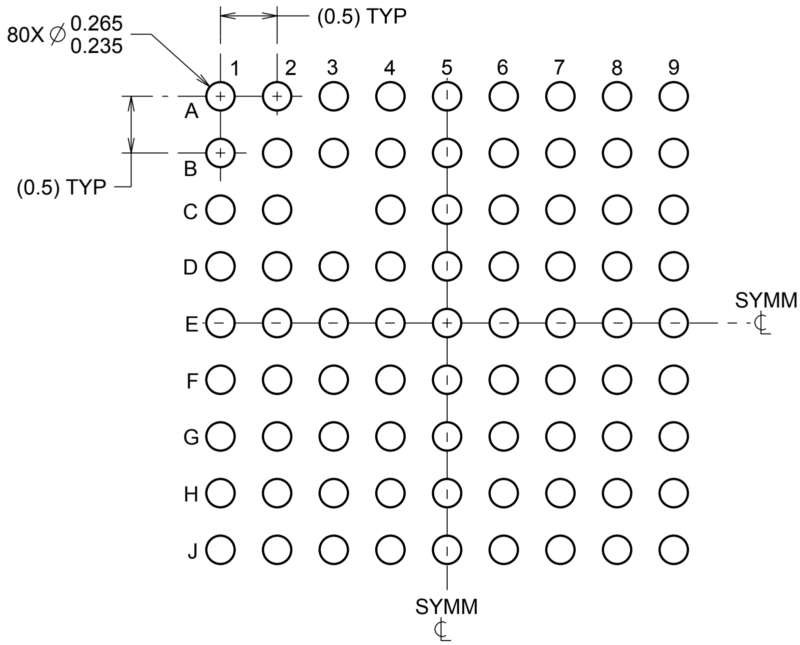
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



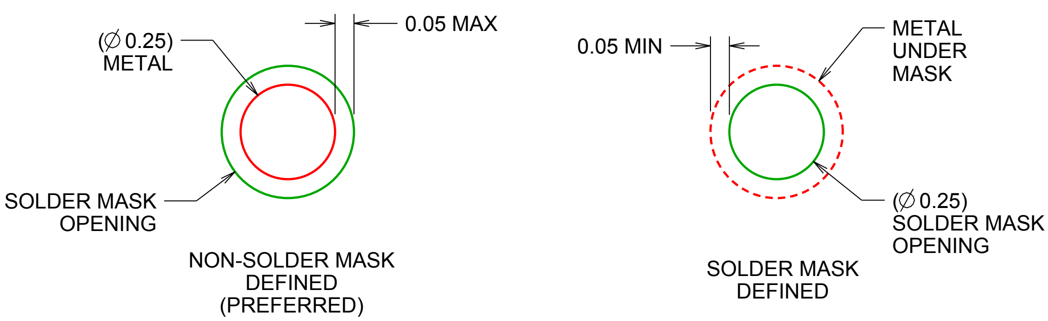


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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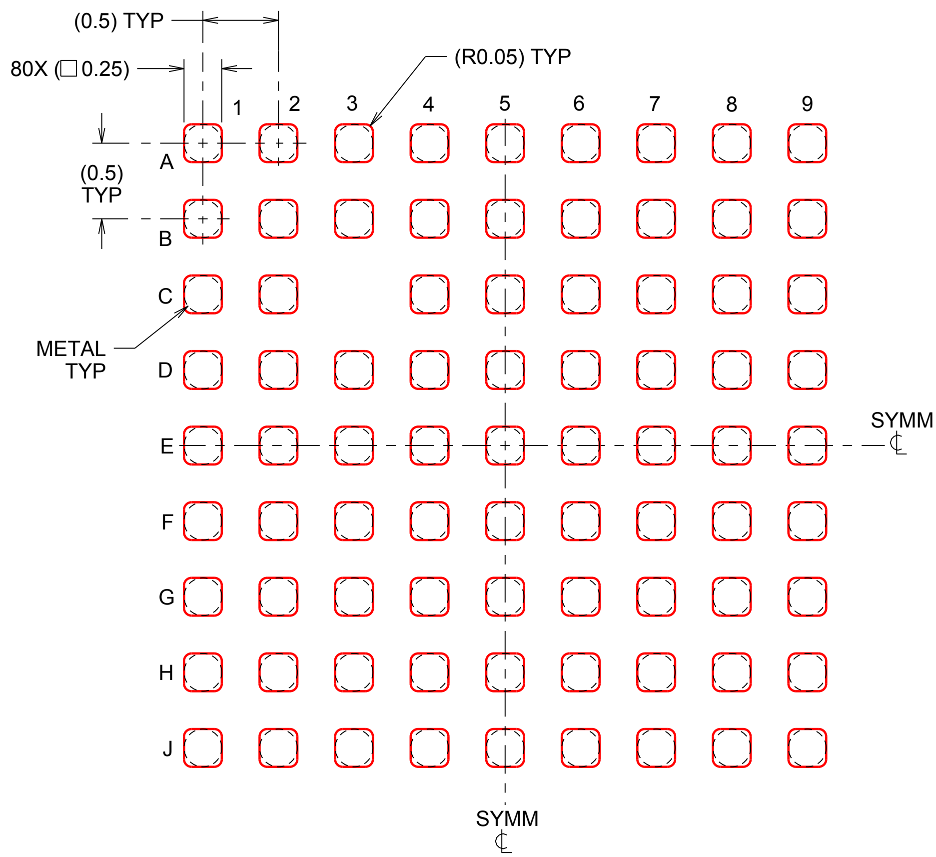
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

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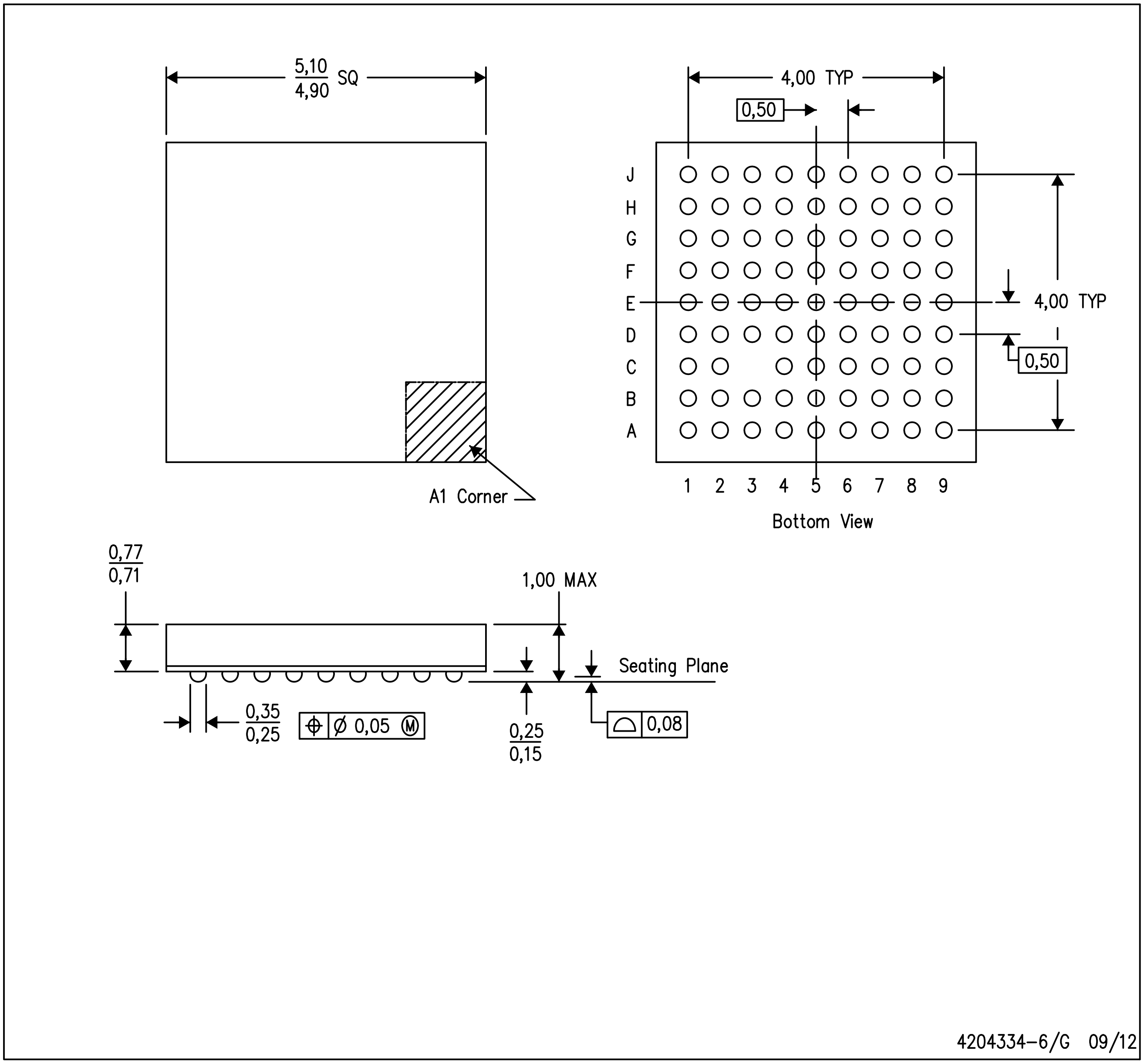
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ZQE (S-PBGA-N80) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-225
D. This is a Pb-free solder ball design.