TLV3511-Q1 レール ツー レール入力の 7ns 高速コンパレータ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～125℃
  - デバイス HBM ESD 分類レベル H1C
  - デバイス CDM ESD 分類レベル C6
- 伝搬遅延:7ns
- 高いトグル周波数:180MHz
- 幅広い電源電圧範囲:2.7V～5.5V
- 入力オフセット電圧:±1mV (標準値)
- 低い消費電流:1.1mA (チャネルあたり)
- 各レールから 300mV 拡張された入力電圧同相範囲
- 内部ヒステリシス:2 mV
- 既知の起動条件を提供するパワーオン リセット
- プッシュ プル出力

2 アプリケーション

- テレマティクス eCall
- 車載用ヘッド ユニット
- インストルメント クラスタ
- オンボード チャージャ (OBC) / ワイヤレス チャージャ

3 概要

TLV351x-Q1 は、プッシュプル出力を搭載した 5V シングルおよびデュアル チャネル コンパレータのファミリです。このファミリは速度と消費電力の組み合わせが非常に優れており、伝搬遅延は 7ns、電源電圧範囲は 2.7V～5.5V で、チャネルあたりの静止電流はわずか 1mA です。

すべてのデバイスに、パワーオン リセット (POR) 機能が搭載されています。これにより、出力が入力に応答する前、最小電源電圧に達するまでの間、出力が既知の状態 (出力 Low) であることが保証されるため、システムの電源オンおよび電源オフ時に誤った出力が発生することを防止できます。

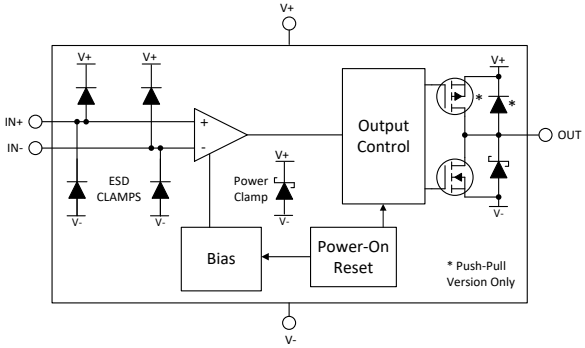
同様に、TLV351x-Q1 は標準のリード付きおよびリードレス パッケージで供給され、レール ツー レール入力、低オフセット電圧、大きな出力駆動電流などの特長があります。これらの特長と高速な応答時間により、本コンパレータは電流センシング、ゼロクロス検出、その他精度と速度が重要なさまざまなアプリケーションに最適です。

すべてのデバイスは、-40℃～125℃°C の拡張工業用温度範囲で仕様が規定されています。

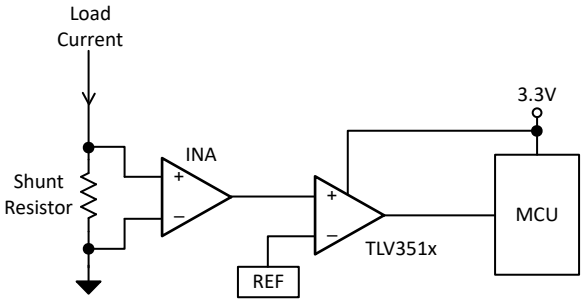
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TLV3511-Q1	SC-70 (5)	1.25mm × 2.00mm
	SOT-23 (5) (プレビュー)	1.60mm × 2.90mm
	SOT (5) (プレビュー)	1.2mm × 1.5mm
TLV3512-Q1	VSSOP (8) (プレビュー)	3.00mm × 3.00mm
	WSON (8) (プレビュー)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



ブロック図



ローサイド電流センシング

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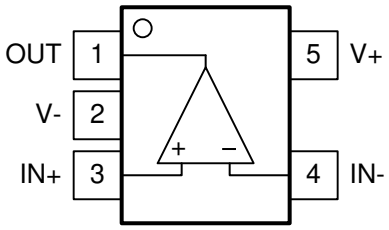
4 Pin Configuration and Functions

Pin Configurations: TLV3511 and TLV3512



DCK, DBV, DRL Packages
SC70, SOT-23-5, SOT
Top View
(Standard "north west" pinout)

表 4-1. Pin Functions: TLV3511-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage

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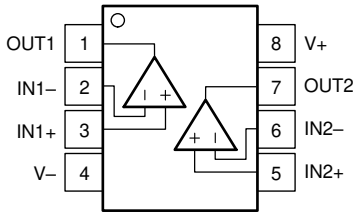

図 4-1. DGK Package
8-Pin VSSOP
Top View

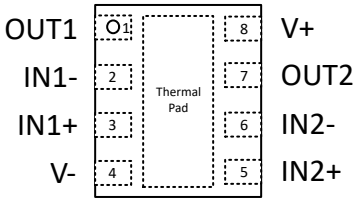

図 4-2. DSG Package
8-Pin WSON
Top View

Pin Functions: TLV3512-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2–	3	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	7	O	Output, channel 1
OUT2	6	O	Output, channel 2
V-	5	-	Negative (lowest) supply or ground
V+	8	-	Positive (highest) supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage V_S = (V+) - (V-)		6	V
Differential input voltage, VID	-6	6	V
Input pins (IN+, IN–) from (V-) (2)	– 0.5	(V+) + 0.5	V
Current into input pins (IN+, IN-)	-10	10	mA
Output (OUT) from (V-)	– 0.5	(V+) + 0.5	V
Output short-circuit current	-100	100	mA
Output short-circuit duration		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–) and (V+). Input signals that can swing more than 0.5V beyond the supply rails must be current-limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage V_S = (V+) - (V-)	2.7	5.5	V
Input voltage range	(V-) - 0.3	(V+) + 0.3	V
Ambient temperature, T_A	–40	125	°C

5.4 Thermal Information

THERMAL METRIC (1)		TLV3511		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	198.1	220.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.6	136.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.7	65.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.1	34.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.3	65.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

V_S = 2.7V to 5V, V_{CM} = V_S / 2; at T_A = 25°C (unless otherwise noted).
Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input Offset Voltage	V_S = 5V, V_{CM} = V_S / 2		±1	±5	mV
V_{IO}	Input Offset Voltage	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 125°C			±6	mV
V_{HYS}	Hysteresis	V_S = 5V, V_{CM} = V_S / 2		2.3		mV
V_{HYS}	Hysteresis	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 125°C			3.5	mV
V_{CM}	Common-mode voltage range		(V-) - 0.2		(V+) + 0.2	V
I_B	Input bias current	V_S = 5V, V_{CM} = V_S / 2			1	nA
I_B	Input bias current	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 125°C			10	nA
I_{OS}	Input offset current	V_S = 5V, V_{CM} = V_S / 2			1	nA
C_{IN}	Input capacitance			4		pF
CMRR	Common-mode rejection ratio	V_{CM} = V_{EE} - 0.2V to V_{CC} + 0.2V		80		dB
DC Output Characteristics						
V_{OH}	Voltage swing from (V+)	V_S = 5V, I_{Source} = 4mA		180	250	mV
V_{OH}	Voltage swing from (V+)	V_S = 5V, I_{Source} = 4mA, -40 to 125C			300	mV
V_{OL}	Voltage swing from (V-)	V_S = 5V, I_{Sink} = 4mA		180	250	mV
V_{OL}	Voltage swing from (V-)	V_S = 5V, I_{Sink} = 4mA, -40 to 125C			300	mV
I_{SC}	Short-circuit current	V_S = 5V, sourcing		84		mA
		V_S = 5V, sinking		94		
Power Supply						
I_Q	Supply current / Channel	V_S = 2.7V and 5V, no load, T_A = -40 to 125°C		1.1	2	mA
$V_{POR\ (postive)}$	Power-On Reset Voltage			2.2		V
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V, T_A = -40 to 125°C		93		dB

5.6 Switching Characteristics

For V_S = 2.7V to V_S = 5V, V_{CM} = V_S / 2; C_L = 15pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low	Midpoint of input to midpoint of output, V_{OD} = 10mV		12		ns
t_{PHL}	Propagation delay time, high to-low	Midpoint of input to midpoint of output, V_{OD} = 50mV		7	9	ns
t_{PLH}	Propagation delay time, low-to high	Midpoint of input to midpoint of output, V_{OD} = 10mV		12		ns
t_{PLH}	Propagation delay time, low-to high	Midpoint of input to midpoint of output, V_{OD} = 50mV		7	9	ns
PWin	Minimum input pulse width	Voverdrive = Vunderdrive = 50mV PWout = 90% of PWin		5		ns
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200mV_{PP} Sine Wave, When output high reaches 90% of V_{CC} - V_{EE} or output low reaches 10% of V_{CC} - V_{EE}		180		MHz
t_R	Rise time	Measured from 20% to 80%		1.5		ns
t_F	Fall time	Measured from 20% to 80%		1.5		ns
t_{ON}	Power-up time	During power on, (V+) must exceed 2.2V for 4µs before the output will reflect the input.		2.5		µs

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6 Detailed Description

6.1 Overview

The TLV351x-Q1 devices are high-speed comparators with push-pull outputs.

6.2 Functional Block Diagrams

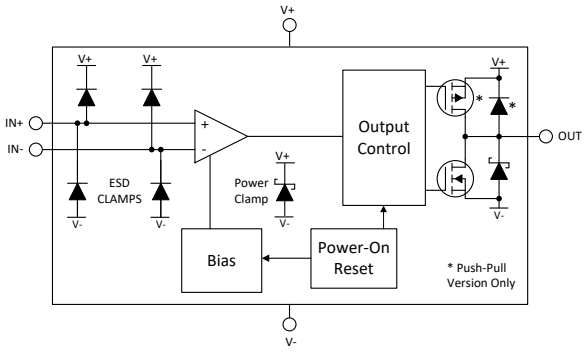

図 6-1. Block Diagram

6.3 Feature Description

The TLV351x-Q1 consumes 1mA per channel with 7ns of propagation delay. The TLV351x-Q1 detects fast voltage and current transients while maintaining low power consumption with single-ended, push-pull outputs.

6.4 Device Functional Modes

6.4.1 Inputs

The inputs incorporate internal ESD protection circuits to (V+) and (V-). Voltages on the inputs are limited to 0.3V beyond the rails.

When connecting to a low impedance source such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. Limit the current to 10mA or less. One form of series resistance is any resistive input dividers or networks.

6.4.1.1 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs can be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

6.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown below. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

  (typically 2mV for the TLV351x-Q1 family)

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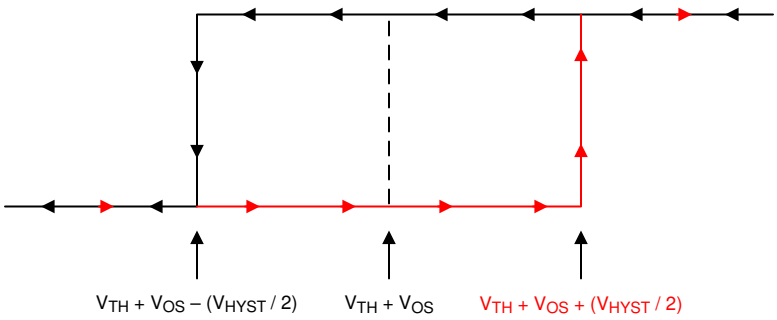

図 6-2. Hysteresis Transfer Curve

6.4.3 Outputs

The TLV351x-Q1 features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

6.4.4 ESD Protection

The inputs and outputs incorporate internal ESD protection circuits to (V+) and (V-).

Voltages on the inputs are limited to 0.3V beyond the rails. If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents in case the clamps conduct. Limit the current to 10mA or less.

6.4.5 Power-On Reset (POR)

The TLV351x-Q1 devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 2.5us after the V_{POR} of 2.2V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV351x-Q1 devices, the output is held low during the POR period (t_{on}) as shown below.

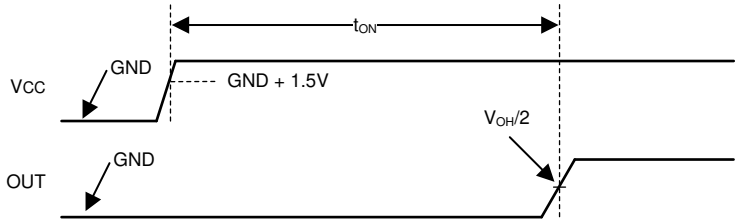

図 6-3. Power-On Reset Timing Diagram

6.5 Overview

The TLV351x-Q1 devices are high-speed comparators with push-pull outputs.

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7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Likewise, the table below summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in the figure below and is measured from the mid-point of the input to the midpoint of the output.

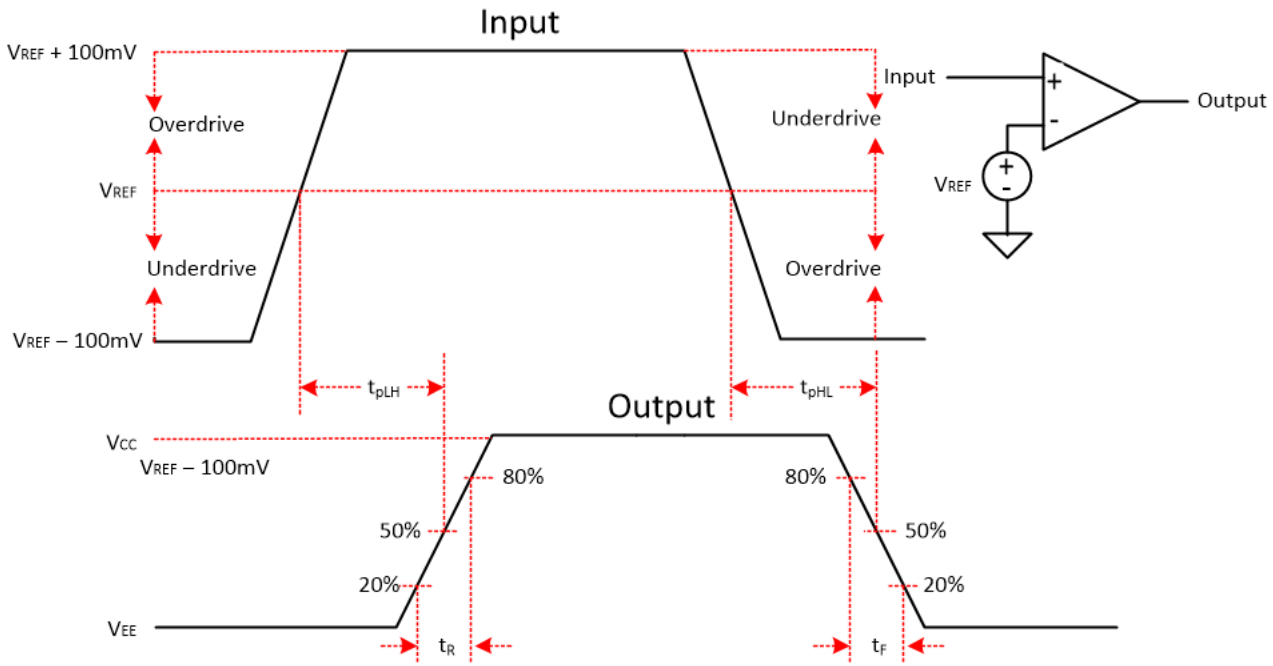

図 7-1. Comparator Timing Diagram

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7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the above example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration may produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV351x-Q1 only have a minimal amount of internal hysteresis of 2mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state.

The hysteresis transfer curve is shown below. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

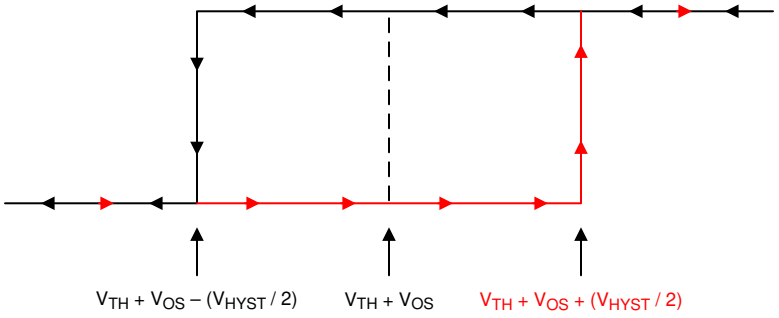

図 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown below.

ADVANCE INFORMATION

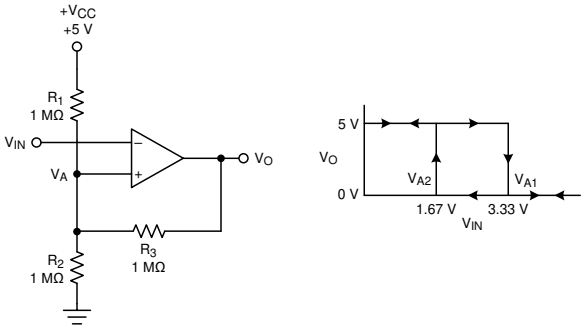

図 7-3. TLV351x-Q1 in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

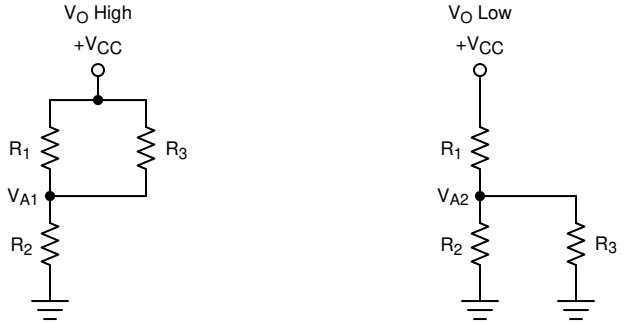

図 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown above on the left.

The equation below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown above on the right.

Use equation below to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The equation below defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown below.

ADVANCE INFORMATION

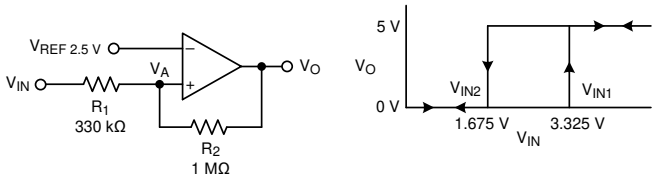

図 7-5. TLV351x-Q1 in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

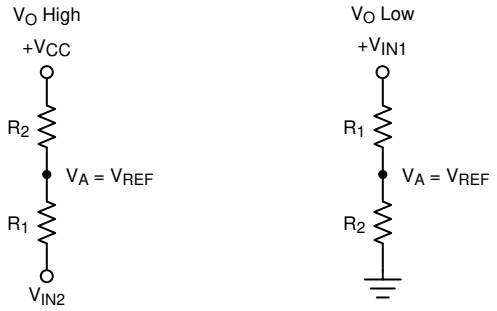

図 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF},, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use the equation below to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use equation below to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown below.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.2 Typical Applications

7.2.1 Low-Side Current Sensing

The figure below shows a simple low-side current sensing circuit using a high-speed comparator. Since this design does not utilze an amplifier, the response time is only limited by the propagation delay of the comparator. With faster response time, the design is well-suited for short-circuit detection when speed is more important than accuracy. When the voltage across the shunt resistor reaches the critical over-current threshold created by R1 and R2, the comparator output changes state.

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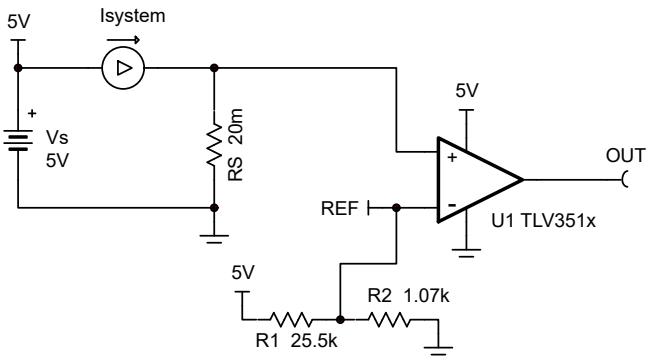

図 7-7. Current Sensing

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (overcurrent) event occurs when system current (Isystem) reaches 10A
- Alert signal (OUT) is active high
- Operate from a 5V power supply

7.2.1.2 Detailed Design Procedure

To minimize power dissipation and voltage drop across the shunt resistor (RS), a value of 20mΩ is selected. Since the overcurrent level of 10A creates a 200mV drop across RS, R1 and R2 are calculated to create the voltage divider value of 200mV from the regulated 5V supply voltage. If the system is expected to operate close to the 10A maximum, hysteresis can be added to the design as shown in Non-Inverting Comparator With Hysteresis.

7.2.1.3 Application Curve

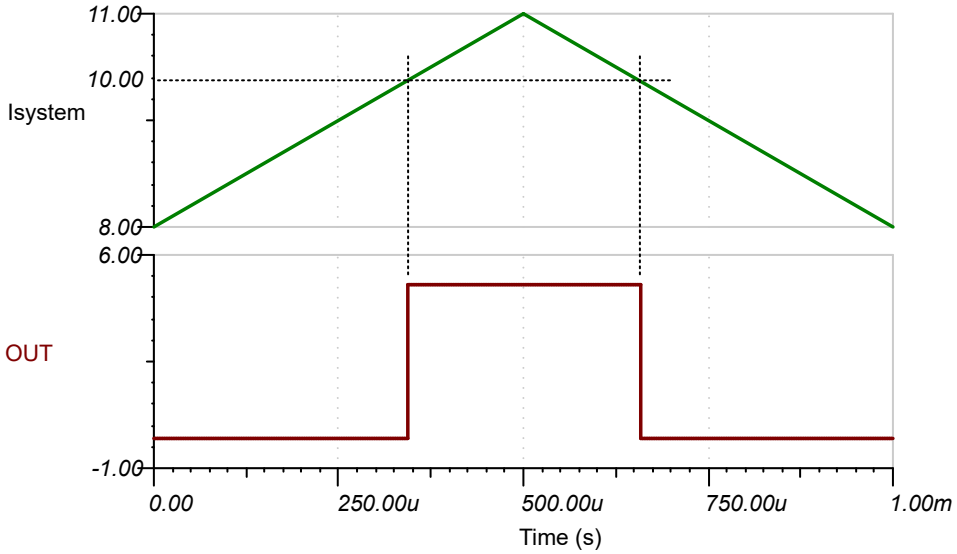

図 7-8. Current Sensing Results

7.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed

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supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from both "split" supplies ((V+) &(V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output will now swing "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

7.4.2 Layout Example

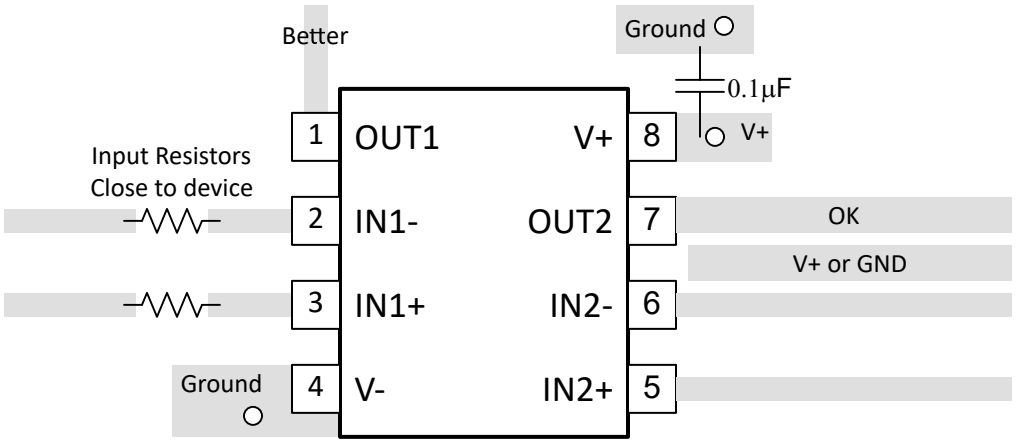

図 7-9. Dual Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

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8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLV3511QDCKRQ1	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

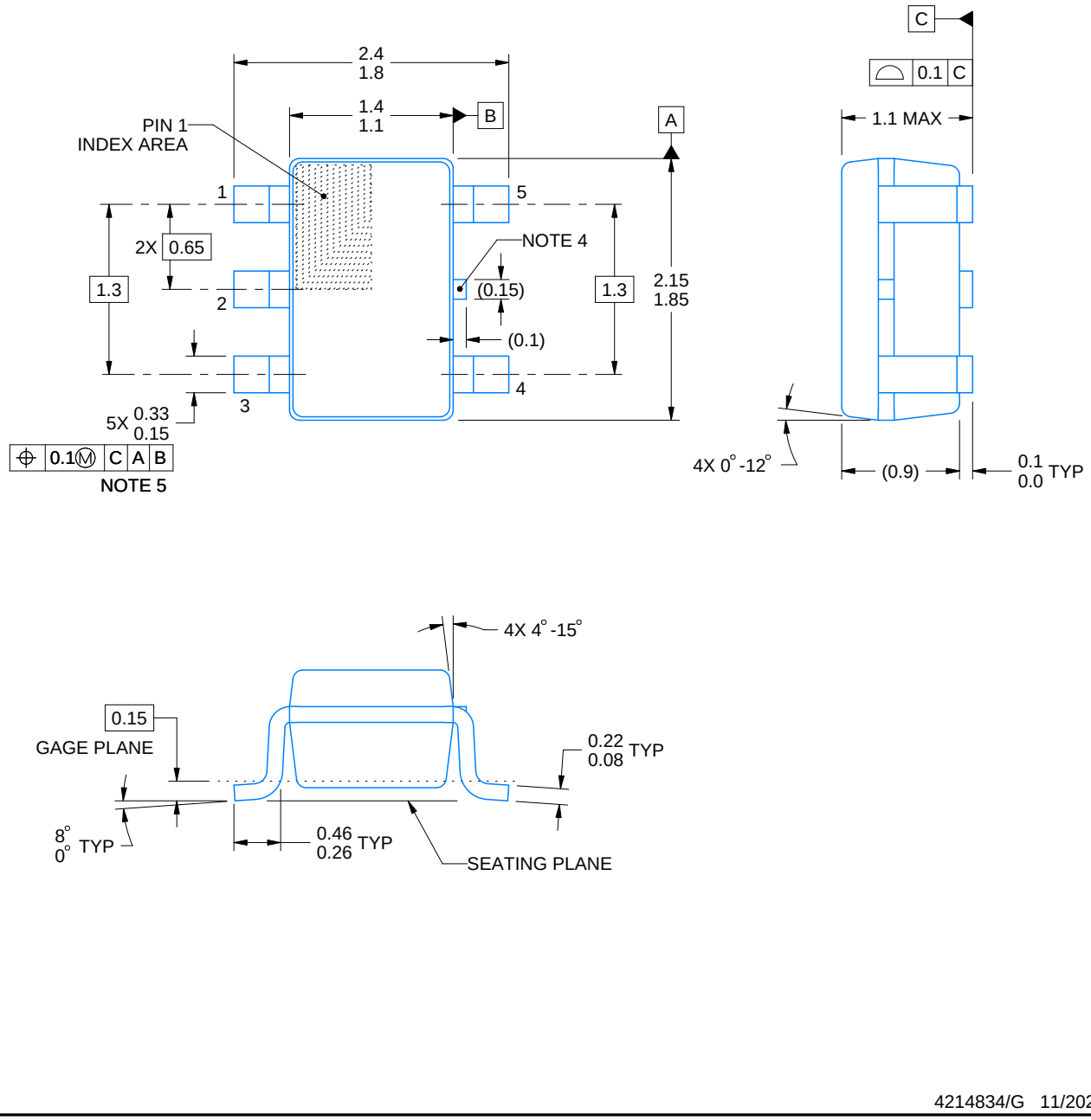
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

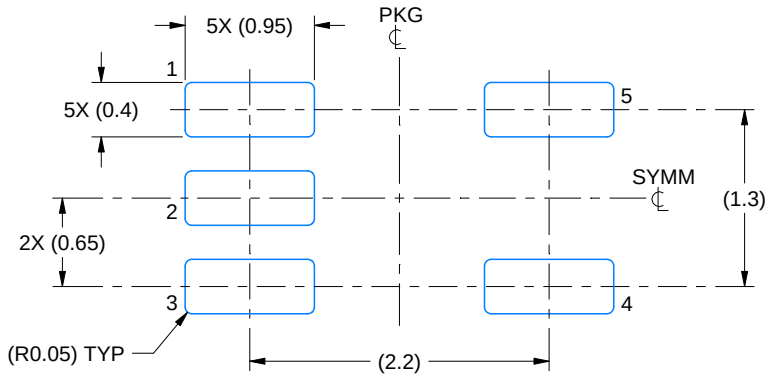
SMALL OUTLINE TRANSISTOR



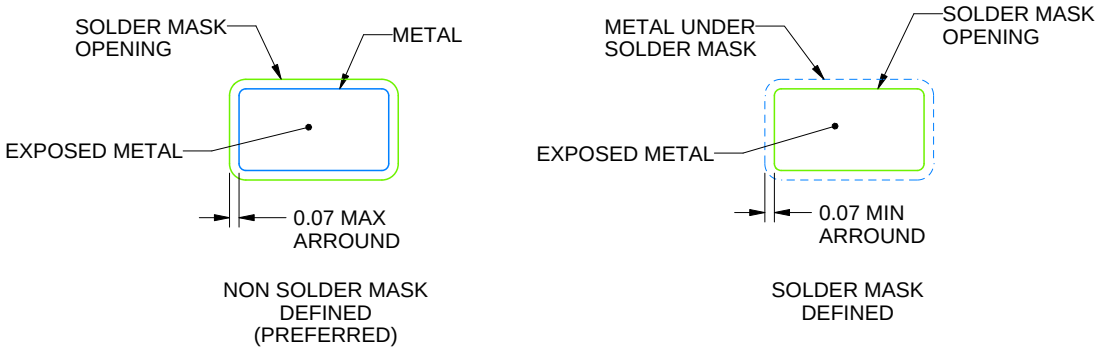
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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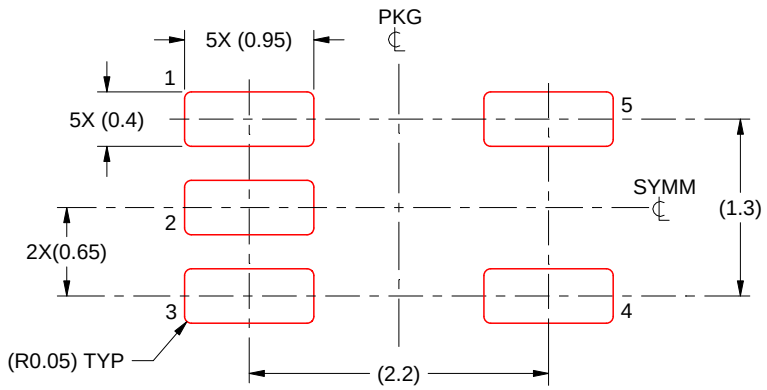
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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