TLV62585 QFNまたはSOT563パッケージの 3A高効率同期整流降圧コンバータ

1 特長

- 最大 95% の効率
- 低 $R_{DS(ON)}$ の電源スイッチ 56mΩ / 32mΩ
- 入力電圧範囲：2.5V～5.5V
- 出力電圧は 0.6V～V_{IN} の範囲で調整可能
- パワー・セーブ・モードにより軽負荷時の効率を向上
- 100% デューティ･サイクル動作によりドロップアウト電圧が最小限
- 動作時静止電流：35µA
- 標準スイッチング周波数：1.5MHz
- 短絡保護 (ヒカップ)
- 出力放電
- パワー・グッド出力
- サーマル・シャットダウン保護機能
- 2mm × 2mm の QFN または 1.6mm x 1.6mm の SOT563 パッケージで供給
- WEBENCH® Power Designer により TLV62585 を使用するカスタム設計を作成

2 アプリケーション

- 汎用 POL (ポイント・オブ・ロード) 電源
- バッテリ駆動アプリケーション
- ワイヤレス・ルータ、ソリッド・ステート・ドライブ
- セットトップ・ボックス、多機能プリンタ
- モータ制御

3 概要

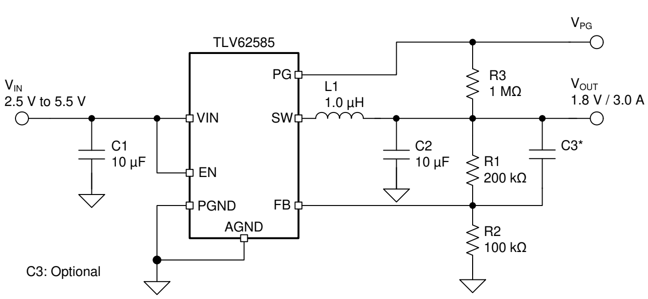
TLV62585は、高効率な小型ソリューション･サイズ向けに最適化された高周波数同期整流降圧コンバータです。このデバイスは最大3Aの出力電流を供給できるスイッチを内蔵しています。中～高負荷時に、コンバータはスイッチング周波数が1.5MHz (標準値)のパルス幅変調(PWM)で動作します。軽負荷時には、デバイスは自動的に省電力モード(PSM)へ移行し、負荷電流範囲の全体にわたって高い効率を維持します。シャットダウン時には、消費電流が2µA未満に減少します。

製品情報(1)

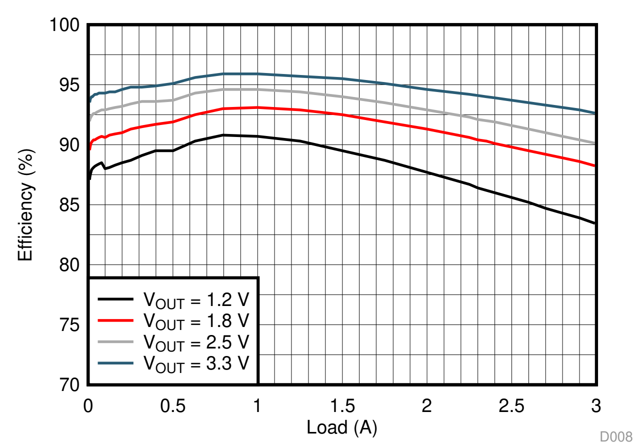
型番	パッケージ	本体サイズ(公称)
TLV62585RWT	QFN (12)	2.00mm×2.00mm
TLV62585DRL	SOT563 (6)	1.60mm×1.60mm
TLV62585PDRL		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



5V入力電圧の効率



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (June 2018) から **Revision F** に変更	**Page**
• Changed Temperature Range for 1% Accuracy from 25°C to 0°C-85°C	7

Revision D (April 2018) から **Revision E** に変更	**Page**
• TLV62585DRL および TLV62585PDRL を*製品プレビューから量産データ*に変更	4
• 追加 PCB layout recommendation for TLV62585PDRL	16

Revision C (November 2017) から **Revision D** に変更	**Page**
• 「*製品情報*」表に TLV62585DRL および TLV62585PDRL を追加	4
• Added DRL and PDRL devices to the *Pin Configurations and Functions*	5
• Added the DRL Thermal Information	6
• Added 図 22	15

Revision B (September 2017) から **Revision C** に変更	**Page**
• Changed HBM From: ±1000 To: ±2000 in the *ESD Ratings* table	6

Revision A (August 2017) から **Revision B** に変更	**Page**
• デバイス・ステータスを事前情報から量産データに変更	1
• Changed HBM From: TBD To: ±1000 in the *ESD Ratings* table	6

2017年7月発行のものから更新 **Page**

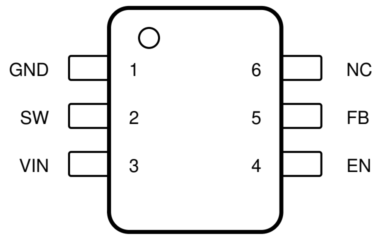
5 概要（続き）

内部補償回路により、ソリューションを小型化し、外付け部品を少なく抑えています。内部のソフトスタート回路により、スタートアップ時の突入電流が制限されます。短絡保護、サーマル・シャットダウン保護、出力放電、パワー・グッドなどの機能も内蔵されています。

このデバイスは、2mm×2mmのQFN、または1.6mm×1.6mmのSOT-563パッケージで供給されます。

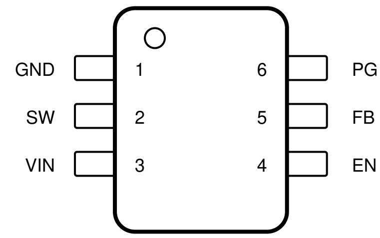
6 Pin Configuration and Functions

DRL Package
6-Pin (SOT563)
Top View



Not to scale

PDRL Package
6-Pin (SOT563)
Top View



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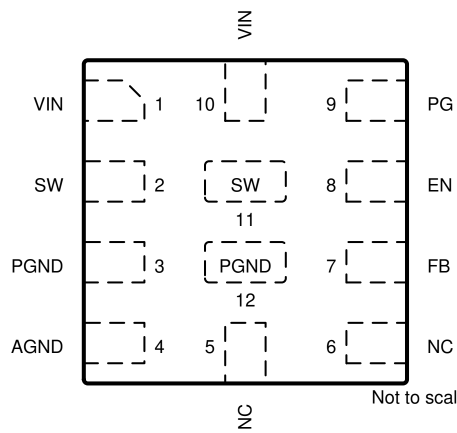
RWT Package
12-Pin (QFN)
Top View



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Pin Functions

PIN				I/O	DESCRIPTION
NAME	RWT (QFN)	DRL (SOT563)	PDRL (SOT563)		
VIN	1, 10	3	3	PWR	Power supply voltage pin.
SW	2, 11	2	2	PWR	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
GND	-	1	1	PWR	Ground pin.
PGND	3, 12	-	-	PWR	Power ground pin.
AGND	4	-	-	-	Ground pin.
NC	5, 6	6	-	-	No connection pin. Leave these pins open, or connect those pins to the output or to AGND.
FB	7	5	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
EN	8	4	4	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
PG	9	-	6	O	Power good open drain output pin. The pull-up resistor can not be connected to any voltage higher than 5.5 V. If unused, leave it floating or connect to AGND.

7 Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage at Pins (1)	VIN, EN, PG	–0.3	6	V
	FB	–0.3	3	
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns) (2)	–3.0	9	
Temperature	Operating Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) All voltage values are with respect to network ground terminal.
(2) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.5		5.5	V
V_{OUT}	Output voltage range	0.6		V_{IN}	V
I_{SINK_PG}	Sink current at PG pin			1	mA
I_{OUT}	Output current	0		3	A
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TLV62585		UNIT
		RWT [QFN]	DRL [SOT]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.7	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.1	43.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	27.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.8	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.7	26.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = 25 °C, and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN	No load, device not switching		35		µA
I_{SD}	Shutdown current into VIN	EN = Low		0.7	2	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling		2.3	2.45	V
	Under voltage lock out hysteresis			150		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis			20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage	V_{IN} = 2.5 V to 5.5 V	1.2			V
V_{IL}	Low-level input voltage	V_{IN} = 2.5 V to 5.5 V			0.4	V
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		900		µs
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal		95%		
		V_{OUT} falling, referenced to V_{OUT} nominal		90%		
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		µA
$t_{PG,DLY}$	Power good delay	V_{FB} falling		40		µs
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode, 2.5 V ≤ VIN ≤ 5.5 V, 0°C to 85°C	594	600	606	mV
		PWM mode, 2.5 V ≤ VIN ≤ 5.5 V, -40°C to 125°C	588	600	612	
$I_{FB,LKG}$	Feedback input leakage current	V_{FB} = 0.6 V		0.01		µA
R_{DIS}	Output discharge FET on-resistance	EN = Low, V_{OUT} = 1.8 V		10		Ω
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			56		mΩ
	Low-side FET on-resistance			32		mΩ
I_{LIM}	High-side FET switch current limit		4	4.6		A
f_{SW}	PWM switching frequency	V_{OUT} = 1.8V, I_{OUT} = 1 A		1.5		MHz

7.6 Typical Characteristics

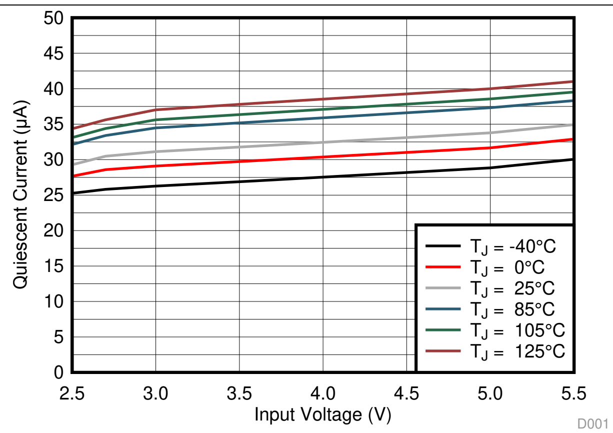


図 1. Quiescent Current vs Input Voltage

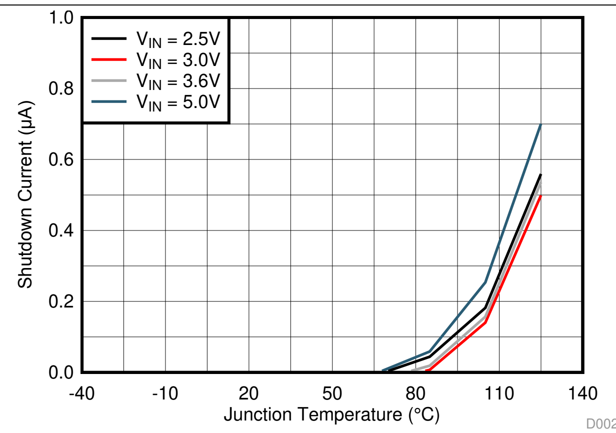


図 2. Shutdown Current vs Junction Temperature

8 Detailed Description

8.1 Overview

The TLV62585 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off-time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

8.2 Functional Block Diagram

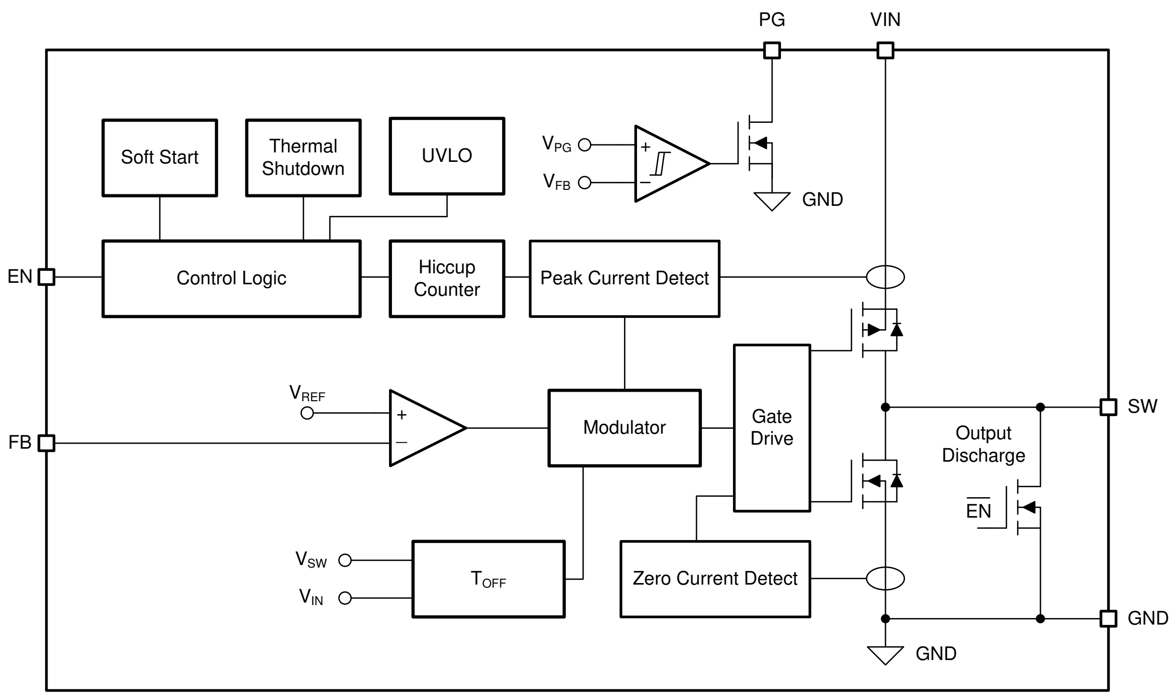


図 3. Functional Block Diagram

8.3 Feature Description

8.3.1 Power Save Mode

The device automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor, or adding a feed forward capacitor, as shown in 図 14.

8.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times R_{DS(ON)} + R_L \quad (1)$$

Where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

Feature Description (continued)

8.3.3 Soft Start

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TLV62585 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.4 Switch Current Limit and Short Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a over load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off-time.

When this switch current limits is triggered 32 times, the device reduces the current limit for further 32 cycles and then stops switching to protect the output. The device then automatically start a new startup after a typical delay time of 500 μs has passed. This is named HICCUP short circuit protection. The devices repeat this mode until the high load condition disappears. HICCUP protection is also enabled during the startup.

8.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO} with a hysteresis of 150 mV.

8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

8.4 Device Functional Modes

8.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 0.7 μA.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal output discharge FET discharges the output through the SW pin smoothly.

8.4.2 Power Good

The TLV62585 has a power good output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown			√
UVLO	1.4 V < V_{IN} < 2.3 V		√
Power Supply Removal	$V_{IN} \leq$ 1.4 V	√	

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV62585 is a synchronous step-down converter in which output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

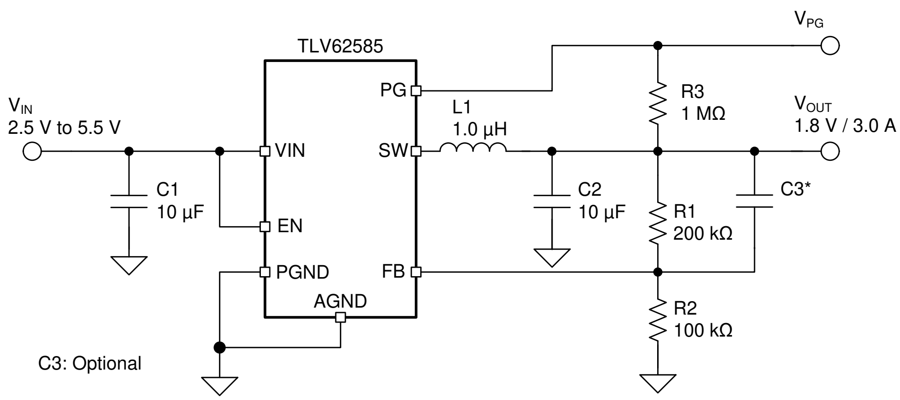


図 4. 1.8-V Output Voltage Application

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	3 A

表 3 lists the components used for the example.

表 3. List of Components(1)

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic capacitor, 10 V, X7R, size 0805, GRM21BR71A106ME51	Murata
C2	22 µF, Ceramic capacitor, 6.3 V, X7T, size 0805, GRM21BD70J226ME44	Murata
C3	Optional	Std
L1	1 µH, Power Inductor, size 4 mm × 4 mm × 1.5 mm, XFL4020-102ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0603;	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%, size 0603;	Std
R3	1 MΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

(1) See *Third-Party Products* disclaimer.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62585 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 式 2:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

R2 must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

9.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, 表 4 outlines possible inductor and capacitor value combinations for most applications.

表 4. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH](1)	NOMINAL C_{OUT} [µF](2)(3)			
	10	22	47	100
0.47				
1	+	+(4)	+	
2.2				

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) For low output voltage applications (< 1.8 V), more output capacitance is recommended (usually ≥ 22 µF) for smaller ripple. For output capacitance higher than 47 µF, a feed forward capacitor is needed.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(4) Typical application configuration. Other '+' mark indicates recommended filter combinations.

9.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 3 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value (3)

TI recommends choosing the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of 式 3. A higher inductor value is also useful to lower ripple current but increases the transient response time as well.

9.2.2.5 Input and Output Capacitor Selection

The architecture of the TLV62585 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

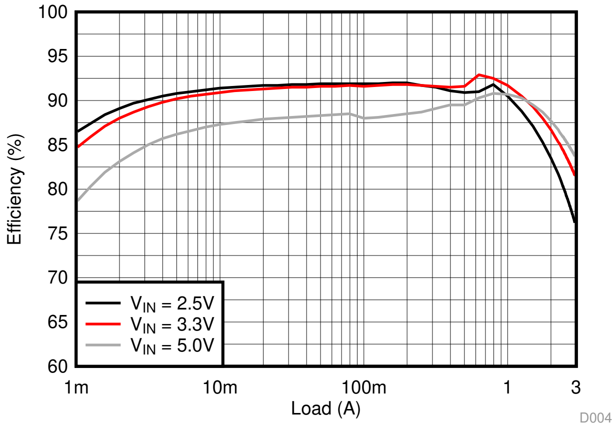
The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 10-µF input capacitor is sufficient; a larger value reduces input voltage ripple.

The TLV62585 is designed to operate with an output capacitor of 10 µF to 47 µF, as outlined in 表 4.

A feed forward capacitor reduces the output ripple in PSM and improves the load transient response. A 22-pF capacitor is good for the 1.8-V output typical application.

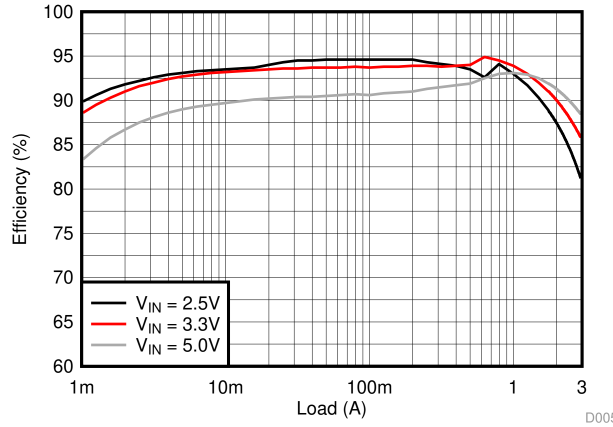
9.2.3 Application Curves

V_{IN} = 5 V, V_{OUT} = 1.8 V, T_A = 25 ºC, unless otherwise noted.



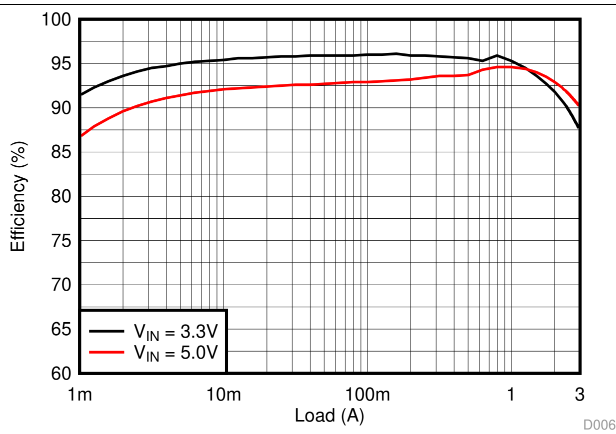
V_{OUT} = 1.2 V

図 5. Efficiency



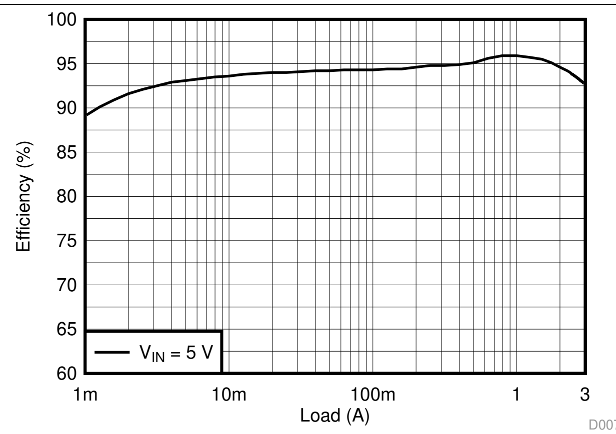
V_{OUT} = 1.8 V

図 6. Efficiency



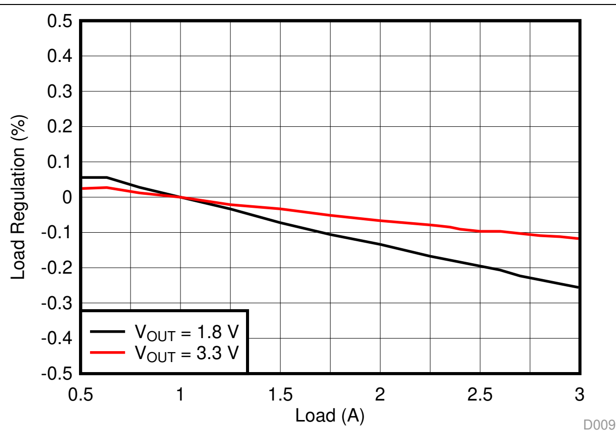
V_{OUT} = 2.5 V

図 7. Efficiency



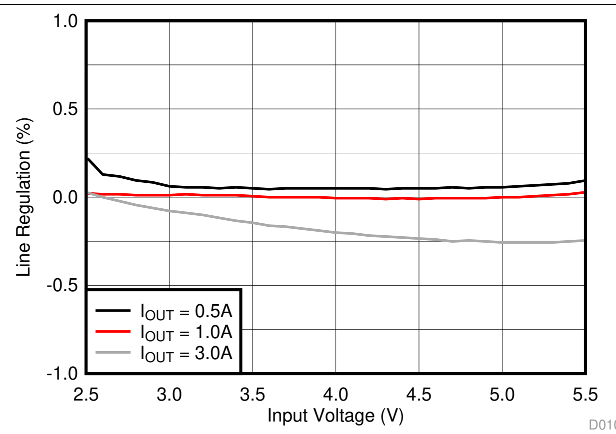
V_{OUT} = 3.3 V

図 8. Efficiency



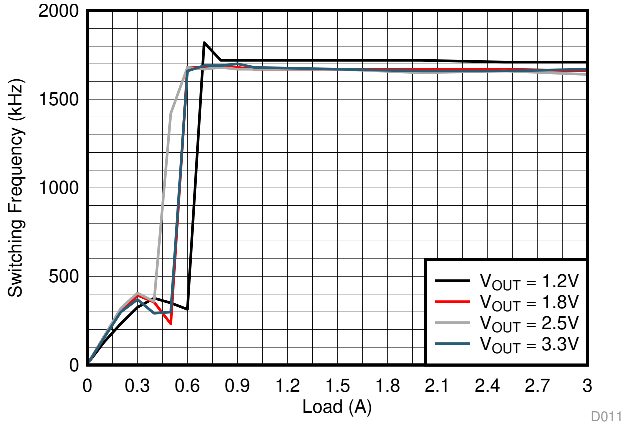
V_{IN} = 5 V

図 9. Load Regulation



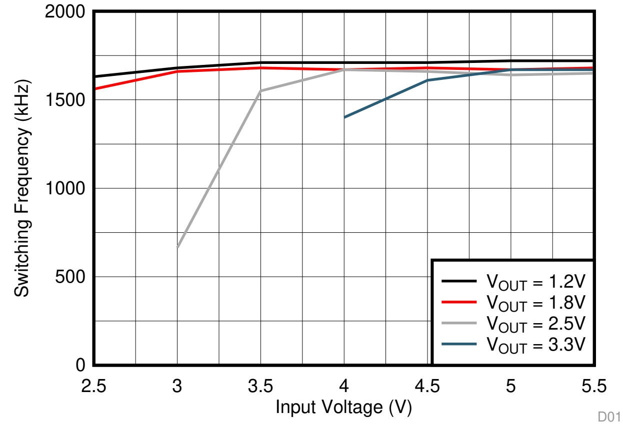
V_{OUT} = 1.8 V

図 10. Line Regulation



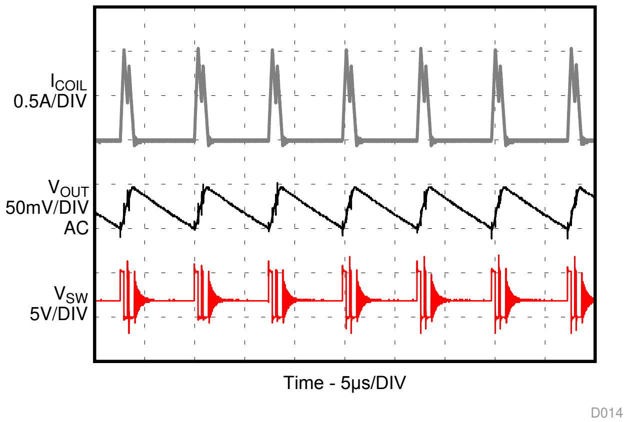
V_{IN} = 5 V

図 11. Switching Frequency



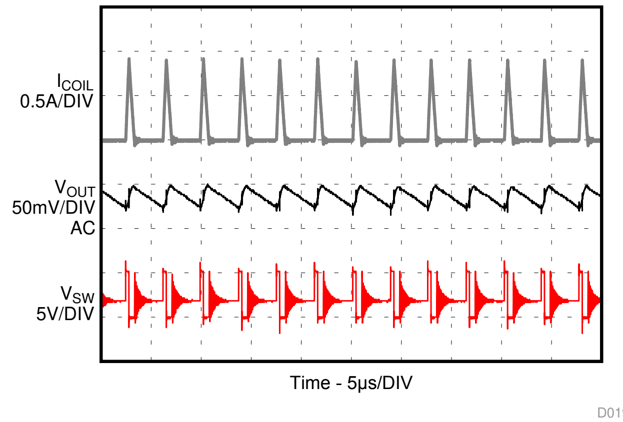
I_{OUT} = 1 A

図 12. Switching Frequency



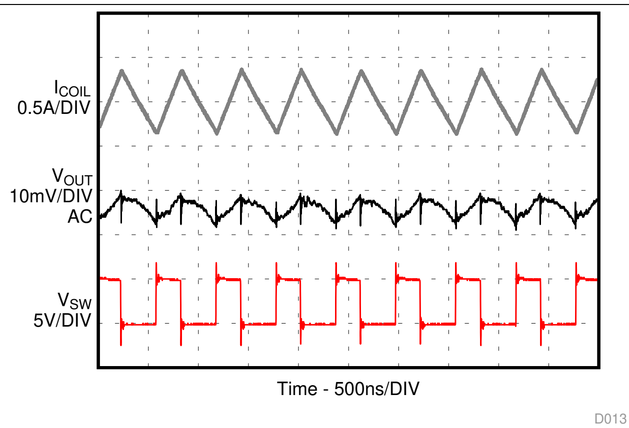
I_{OUT} = 0.1 A

図 13. PSM Operation



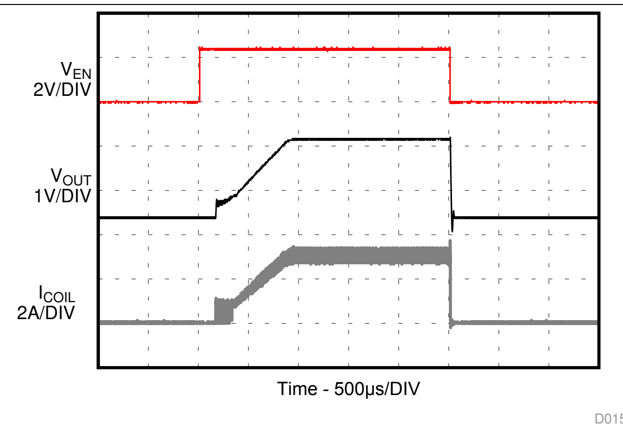
I_{OUT} = 0.1 A C3 = 22 pF

図 14. PSM Operation with A Feedforward Capacitor



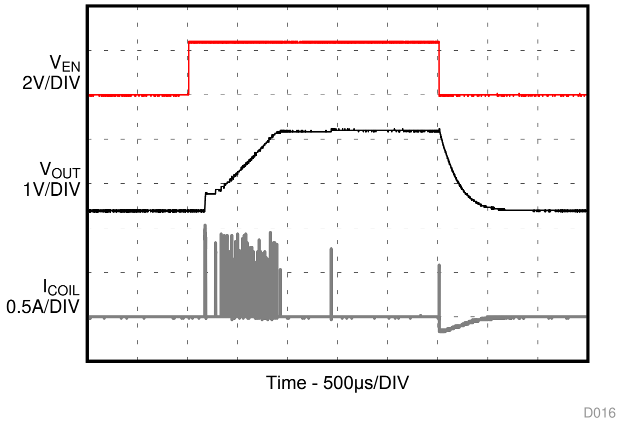
I_{OUT} = 3 A

図 15. PWM Operation



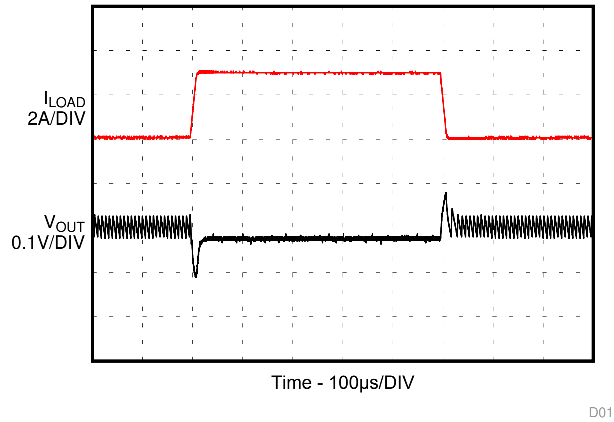
R_{OUT} = 0.6 Ω

図 16. Start-Up and Shut-Down with Load



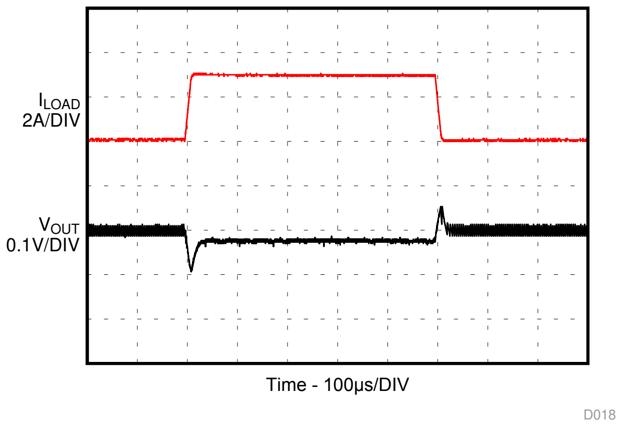
No Load

図 17. Start-Up and Shut-Down without Load



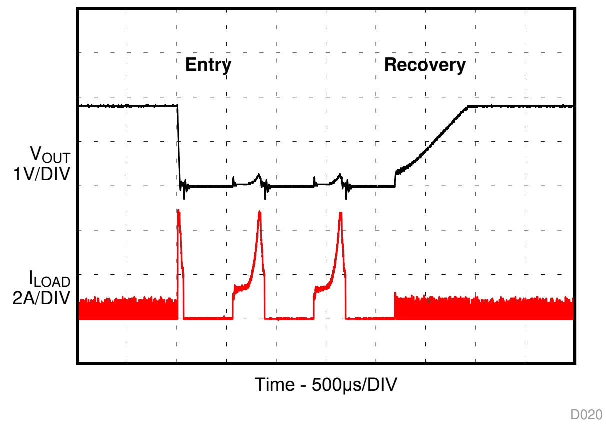
I_{OUT} = 0.1 A to 3 A

図 18. Load Transient



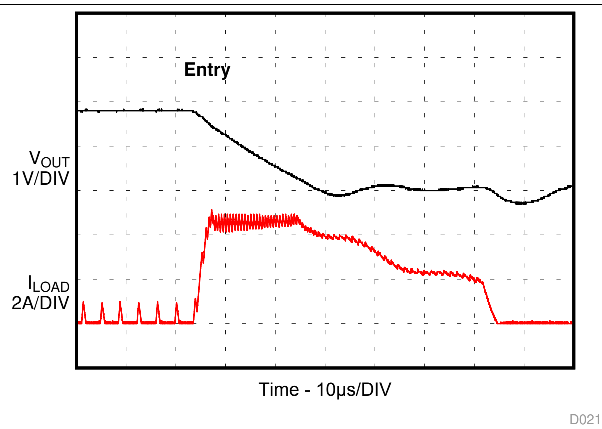
I_{OUT} = 0.1 A to 3 A　　C3 = 22 pF

図 19. Load Transient with A Feedforward Capacitor



I_{OUT} = 0.1 A

図 20. Output Short Protection (HICCUP)



I_{OUT} = 0.1 A

図 21. Output Short Protection (HICCUP) - Zoom In

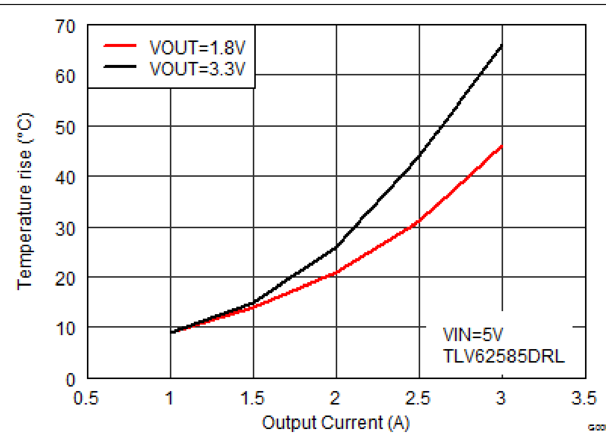


図 22. Temperature Rise of DRL Package on EVM

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TLV62585 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- A common ground should be used. GND layers might be used for shielding.

See 図 23 and 図 24 for the recommended PCB layout.

11.2 Layout Example

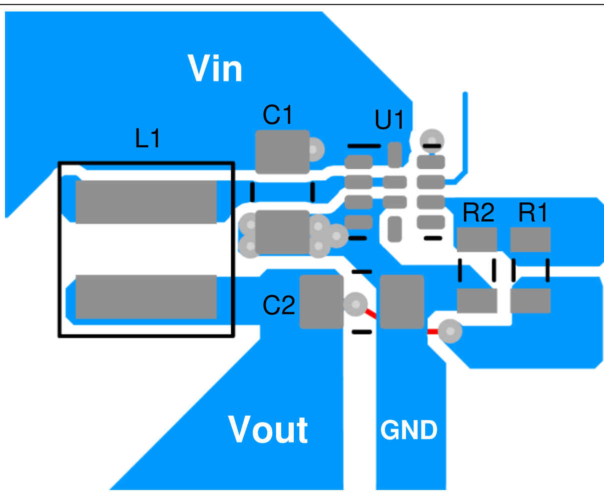


図 23. PCB Layout Recommendation (TLV62585RWT)

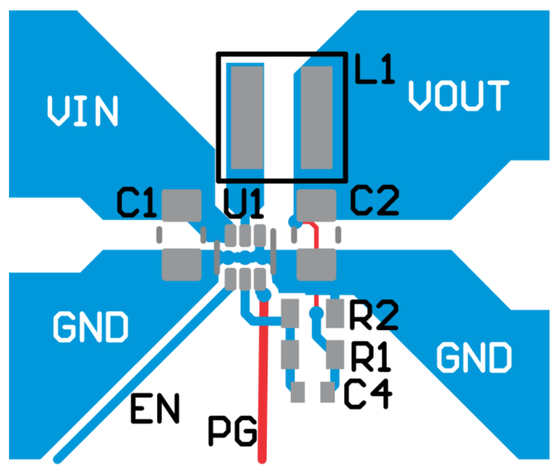


図 24. PCB Layout Recommendation (TLV62585PDRL)

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see: .

- *Thermal Characteristics Application Notes*, SZZA017 and SPRA953

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.1.2 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TLV62585を使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs』(英語)*
- *『Semiconductor and IC Package Thermal Metrics』(英語)*

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 商標

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WEBENCH is a registered trademark of Texas Instruments.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62585DRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BQ	Samples
TLV62585DRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BQ	Samples
TLV62585PDRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BP	Samples
TLV62585PDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BP	Samples
TLV62585RWTR	ACTIVE	VQFN-HR	RWT	12	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	17BI	Samples
TLV62585RWTT	ACTIVE	VQFN-HR	RWT	12	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	17BI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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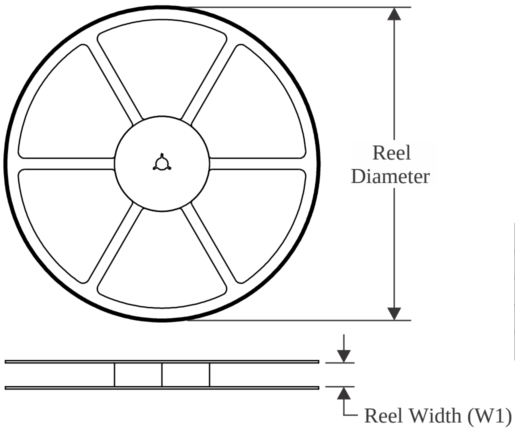
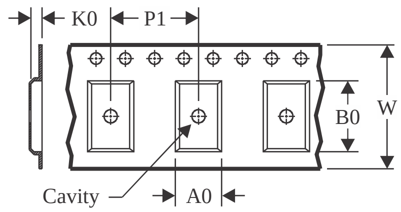
TAPE AND REEL INFORMATION

REEL DIMENSIONS

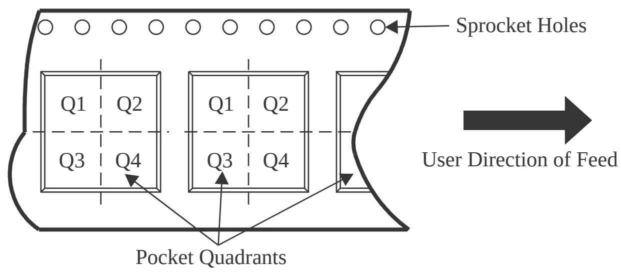


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

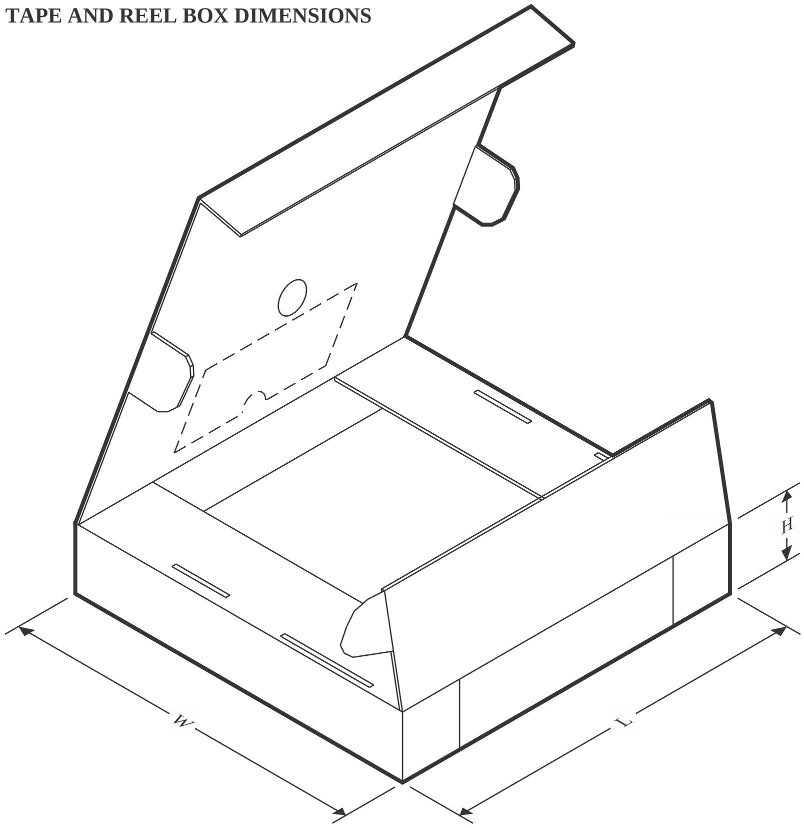
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

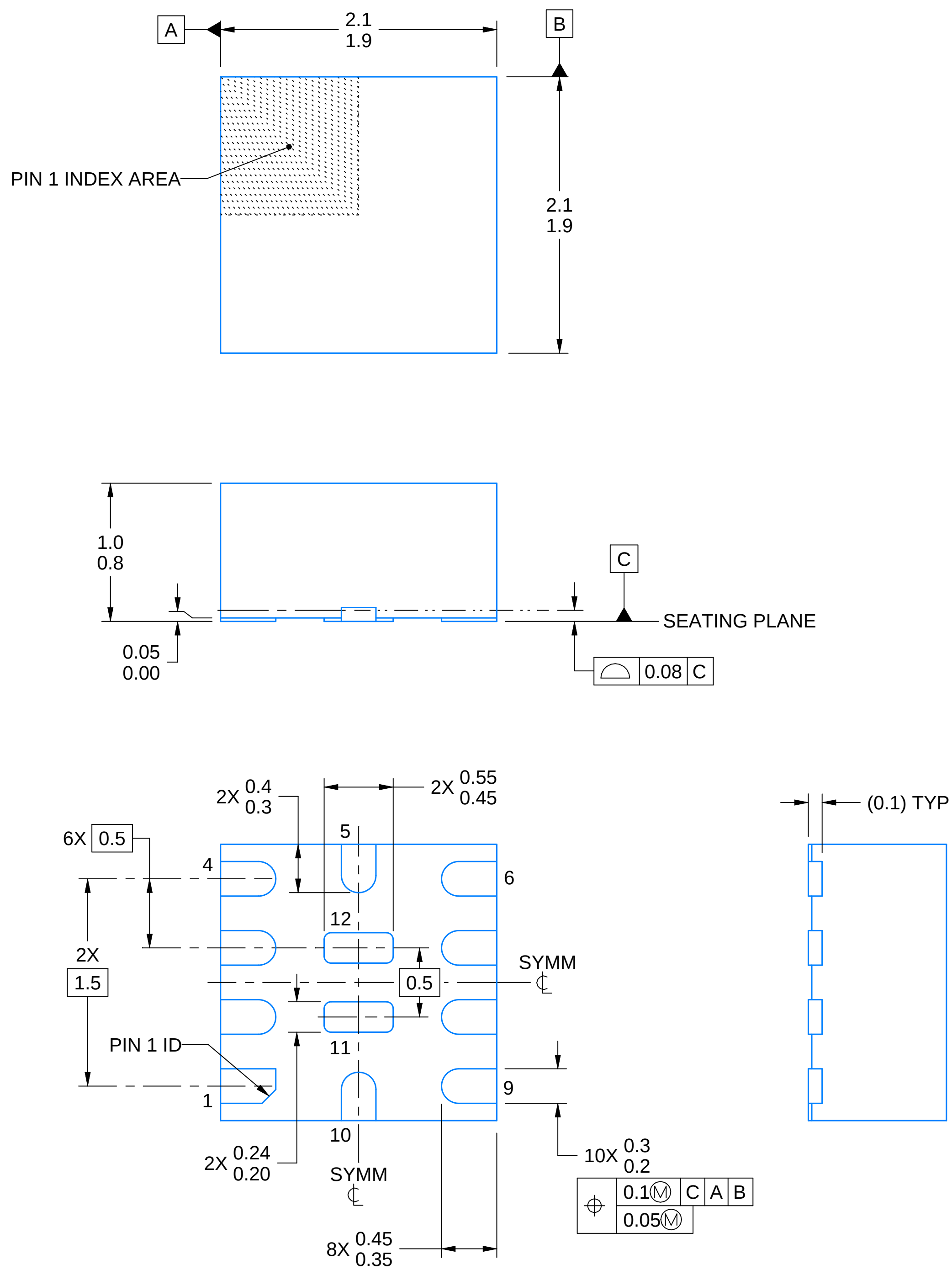
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62585DRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585DRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585PDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585PDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

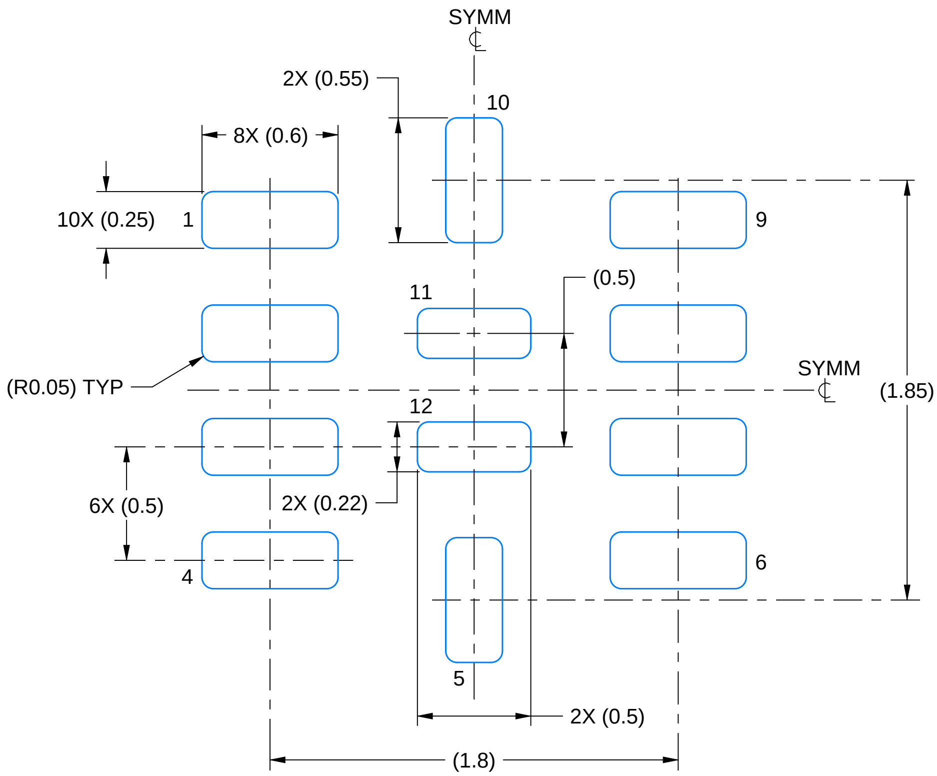
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62585DRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62585DRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62585PDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62585PDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0



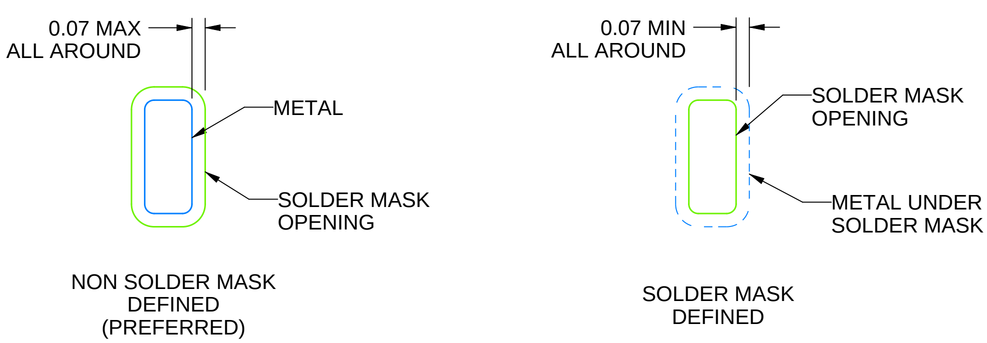
4223084/B 10/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

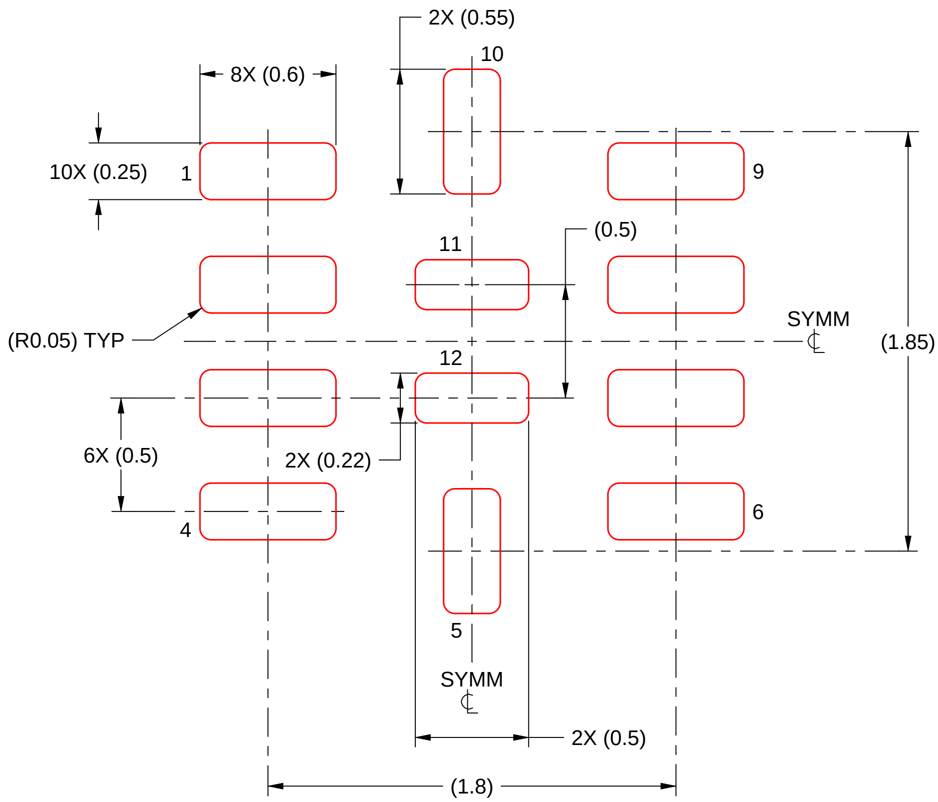


SOLDER MASK DETAILS

4223084/B 10/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.

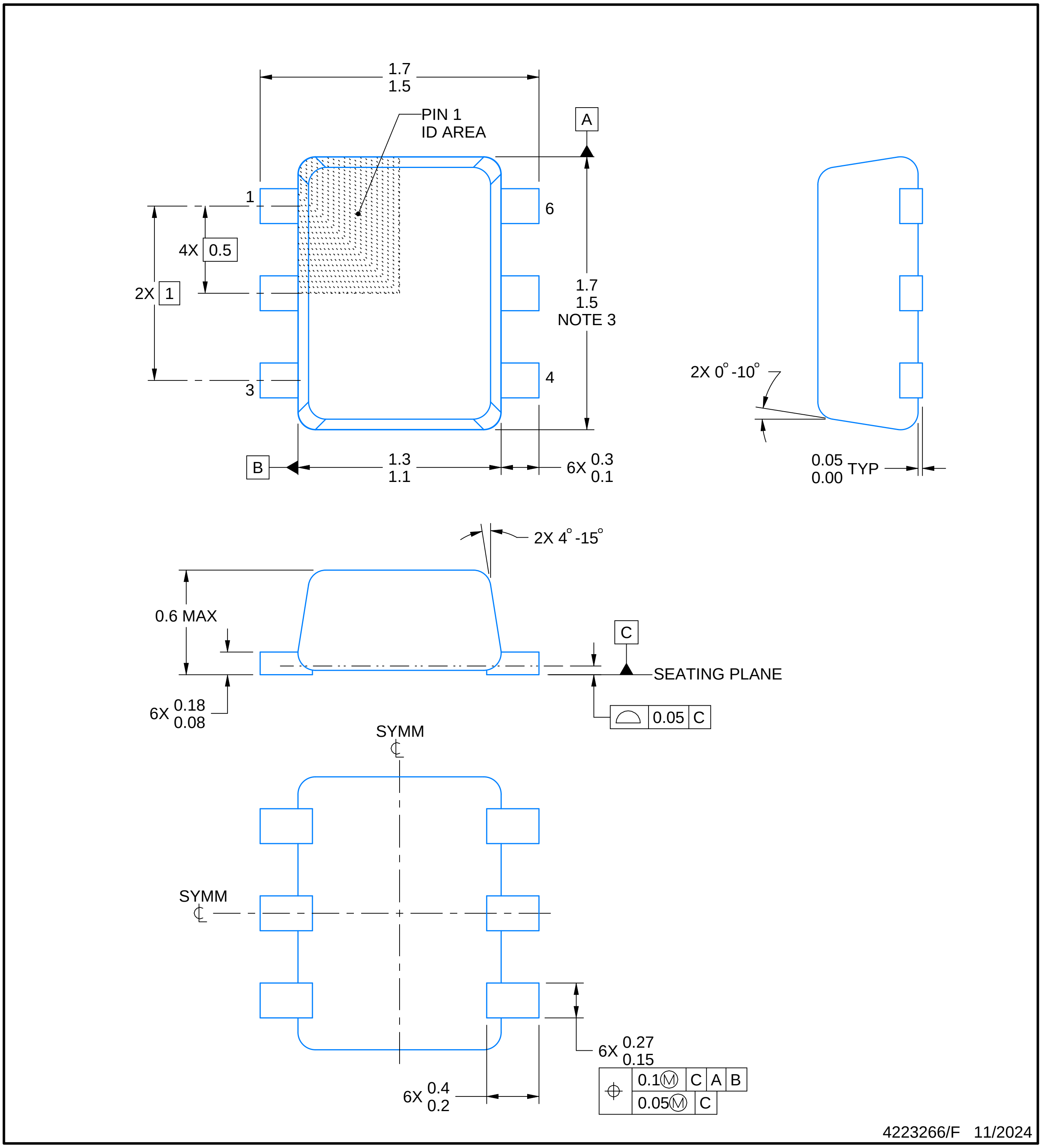


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223084/B 10/2018

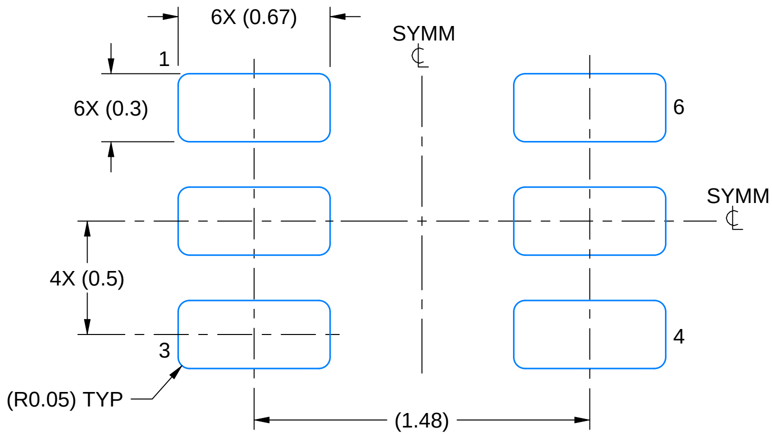
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

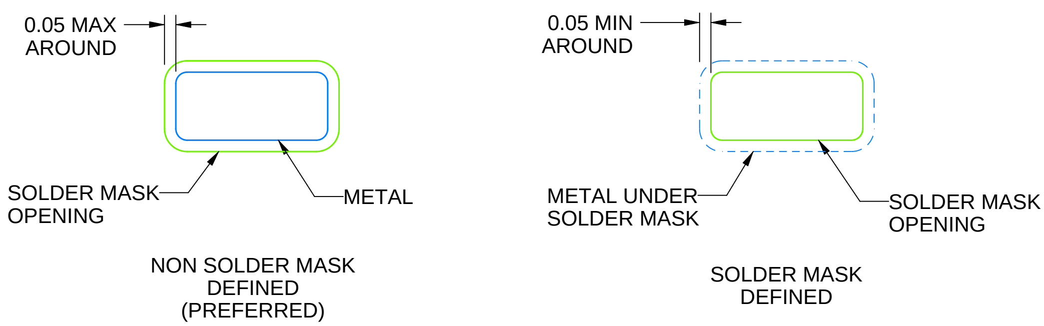


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X

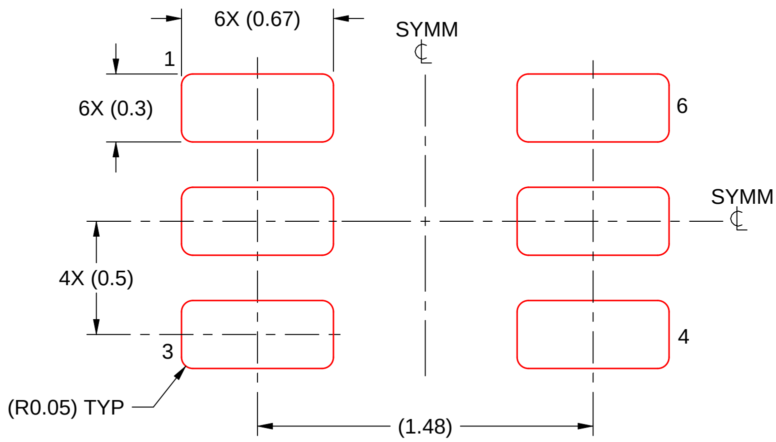


SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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