TLV761 16V、1A、固定出力リニア電圧レギュレータ

1 特長

- 業界標準の LM1117 および TLV1117 (x1117) デバイスとピン互換 (一部のパッケージ)
- 入力電圧範囲 (V_{IN}):2.5V ～ 16V (絶対最大定格 20V)
- 出力電圧範囲 (V_{OUT}):
  - 0.8V ～ 13V (固定、100mV 刻み)
- 出力電流:最大 1A
- 小さい静止電流 (I_Q):
  - 60µA (標準値) ～ 1.5µA (シャットダウン時)
- ライン、負荷、温度の全範囲にわたって 1% の出力精度
- 高 PSRR:1kHz で 60dB、1MHz で 40dB
- 内部ソフトスタート時間:500µs (標準値)
- フォールドバック電流制限および過熱保護
- 1µF のセラミック出力コンデンサで安定動作
- 温度範囲:-40℃～+125℃
- パッケージ:
  - 4 ピン、6.5mm × 7mm SOT-223
  - 3 ピン、6.6mm x 10.11mm の TO-252 (開発中製品)

2 アプリケーション

- 家電製品
- ホーム・シアターおよびエンターテインメント
- モーター・ドライブ
- HVAC およびビル・セキュリティ・システム
- スマート・メーター

3 概要

TLV761 は、より厳密な出力精度と、スタンバイ消費電力を低減させる小さい静止電流 (I_Q) とによって、従来の x1117 レギュレータ (TLV1117 または LM1117) の機能を向上させるリニア電圧レギュレータです。TLV761 はその他の固定 SOT-223、TO-252 レギュレータとピン互換です。

TLV761 の入力電圧範囲は 2.5V～16V であり、0.8V～13V の出力電圧範囲を持っているため、幅広いアプリケーションに対応できます。

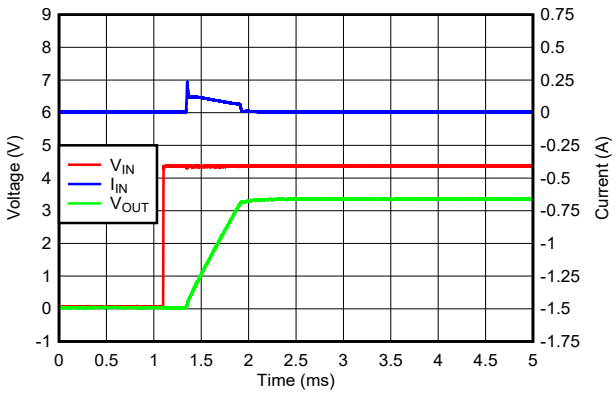
TLV761 の広帯域の PSRR 特性 (標準値) は、1kHz で 60dB、1MHz で 40dB を超え、上流の DC/DC コンバータのスイッチング周波数を減衰して、レギュレータ後のフィルタ処理を最小化できます。

さらに、TLV761 は、起動時の突入電流を減らすために内部ソフトスタート機能を備えているため、入力容量を最小化することで設計のスペースとコストを節約できます。TLV761 は、過負荷電流フォルトまたは短絡発生時のデバイスの消費電力を制限するフォールドバック電流制限機能を備えています。

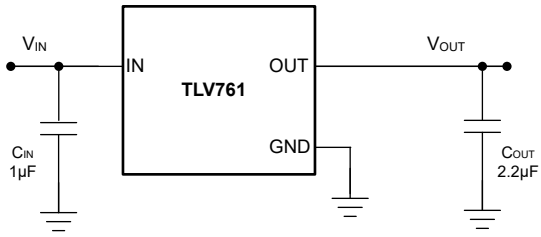
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TLV761	DCY (SOT-223、4)	6.5mm × 7mm
	KVU (TO-252、3)(3)	6.6mm × 10.11mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) プレビュー情報 (量産データではありません)。



22µF の C_{OUT} を使用した場合の突入電流



代表的なアプリケーション回路

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

Copyright © 2024 Texas Instruments Incorporated

4 Pin Configuration and Functions

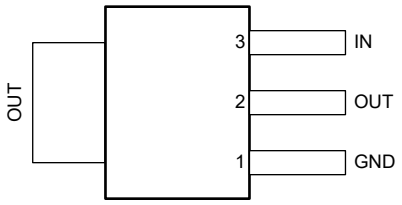


図 4-1. DCY Package, 4-Pin SOT-223 (Top View)

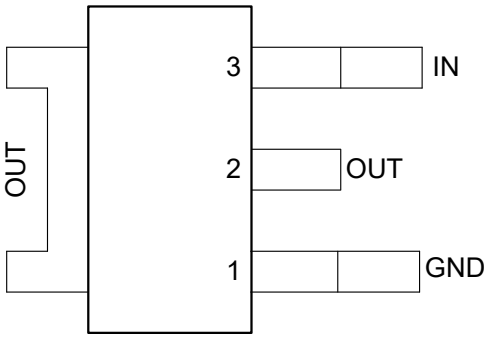


図 4-2. KVU Package (Preview), 3-Pin TO-252 (Top View)

表 4-1. Pin Functions

PIN				DESCRIPTION
NAME	DCY	KVU	FUNCTION	
GND	1	1	—	Ground pin
OUT	2, Tab	2, Tab	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
IN	3	3	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.

Copyright © 2024 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage (2)	V_{IN}	–0.3	20	V
	V_{OUT} (3)	–0.3	V_{IN} + 0.3	
Current	Maximum output current	Internally limited		A
Power	Power dissipation	Package limited (4)		W
Temperature	Operating junction (T_J)	–50	150	°C
	Storage (T_{STG})	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) V_{IN} + 0.3 V or 18 V (whichever is smaller).
(4) See thermal information for further details.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		16	V
V_{OUT}	Output voltage	0.8		13.5	
I_{OUT}	Output current (2.5 V ≤ V_{IN} < 3 V)	0		0.8	A
I_{OUT}	Output current (V_{IN} ≥ 3 V)	0		1	
C_{OUT} ESR	Output capacitor ESR	2		500	mΩ
C_{OUT}	Output capacitor(1)	1	2.2	220	µF
C_{IN}	Input capacitor(2)		1		
T_J	Junction temperature	–40		125	°C

(1) Effective output capacitance of 0.47 µF minimum required for stability.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47 µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of systemlevel instability such as ringing or oscillation, especially in the presence of load transients

Copyright © 2024 Texas Instruments Incorporated

5.4 Thermal Information

THERMAL METRIC[1]		TLV761		UNIT
		DCY (SOT–223)	KVU (TO–252)	
		4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.4	67.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.6	71.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.7	45.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.9	31.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.4	45.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	40.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.5V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10mA, C_{IN} = 1.0µF and C_{OUT} = 1.0µF (unless otherwise noted); typical values are at T_J= 25ºC

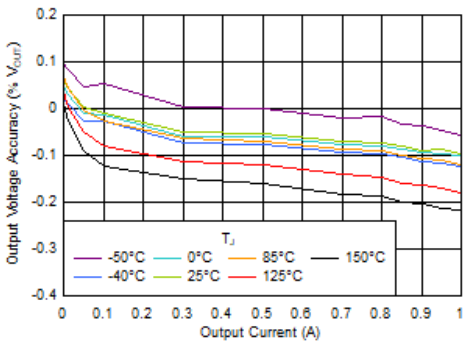
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Nominal output accuracy	T_J = 25°C	–1		1	%
V_{OUT}	Output accuracy over temperature	VIN ≥ 3.0V, $V_{OUT(NOM)}$ ≤ 9.0V, 1mA ≤ I_{OUT} ≤ 1A	–1.75		1.75	%
		$V_{OUT(NOM)}$ > 9.0V, 1mA ≤ I_{OUT} ≤ 1A	–1.5		1.5	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation[1]	$V_{OUT(NOM)}$ ≤ 9.0V, $V_{OUT(NOM)}$ + 1.5V ≤ V_{IN} ≤ 16V, I_{OUT} = 10mA			0.02	%/V
		$V_{OUT(NOM)}$ > 9.0V, $V_{OUT(NOM)}$ + 1.5V ≤ V_{IN} ≤ 16V, I_{OUT} = 10mA			9.9	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 3.0V		0.1	0.75	%/A
V_{DO}	Dropout voltage[2]	V_{IN} ≥ 3.0V, I_{OUT} = 1A		0.9	1.6	V
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} ≥ 3.0V	1.1		1.6	A
I_{SC}	Short-circuit current limit	V_{OUT} = 0V	150	250	350	mA
I_Q	Quiescent current	I_{OUT} = 0mA		65	100	µA
$I_{PULLDOWN}$	Output pulldown current[3]	V_{IN} = 1.8V, V_{OUT} = 2.5V	0.7		1.1	mA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 300mA, f = 120Hz		70		dB
V_n	Output noise voltage	BW = 10Hz to 100kHz, V_{IN} = 3.3V, V_{OUT} = 0.8V, I_{OUT} = 100mA		60		μV_{RMS}
V_{UVLO+}	UVLO threshold rising	V_{IN} rising		2.2	2.4	V
$V_{UVLO(HYS)}$	UVLO hysteresis			130		mV
V_{UVLO-}	UVLO threshold falling	V_{IN} falling	1.9			V
$T_{SD(shutdown)}$	Thermal shutdown temperature	Temperature increasing		180		ºC
$T_{SD(reset)}$	Thermal shutdown reset temperature	Temperature falling		160		ºC

(1) Line regulation is measured with V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater).
(2) V_{DO} is measured with V_{IN} = 95% x $V_{OUT(nom)}$ for fixed output devices. V_{DO} is not measured for fixed output devices when V_{OUT} < 2.5 V.
(3) $I_{PULLDOWN}$ is measured with V_{IN} = 1.8 V (lower than UVLO falling threshold, with LDO in disabled state) and 2.5 V applied on V_{OUT} externally.

Copyright © 2024 Texas Instruments Incorporated

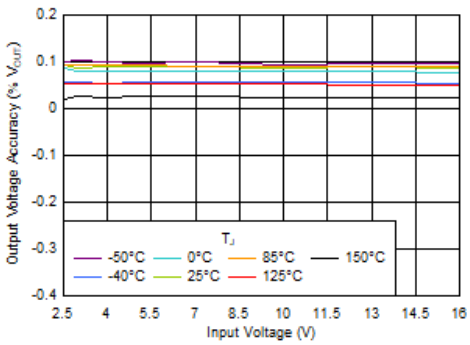
5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



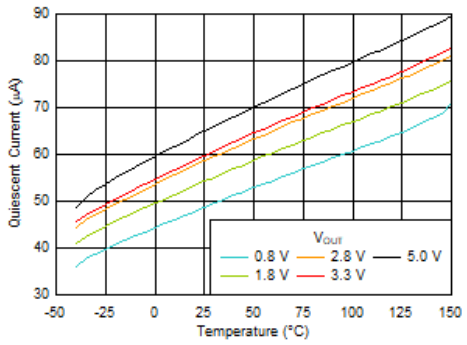
For V_{IN} ≥ 3.0 V

図 5-1. V_{OUT} Accuracy vs I_{OUT}



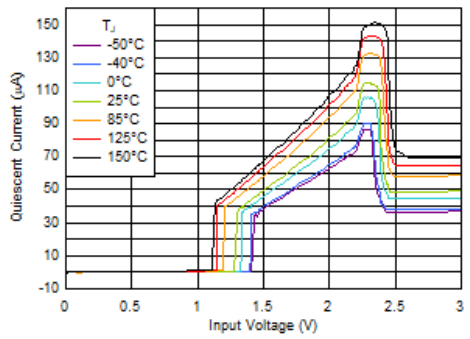
I_{OUT} = 10 mA

図 5-2. V_{OUT} Accuracy vs V_{IN}



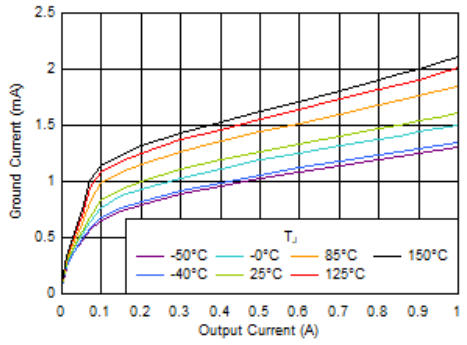
I_{OUT} = 0 mA

図 5-3. I_Q vs Temperature



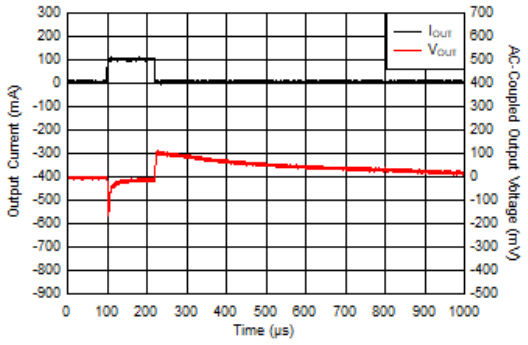
I_{OUT} = 0 mA

図 5-4. I_Q Increase Below Minimum V_{IN}



For V_{IN} ≥ 3.0 V

図 5-5. I_{GND} vs I_{OUT}



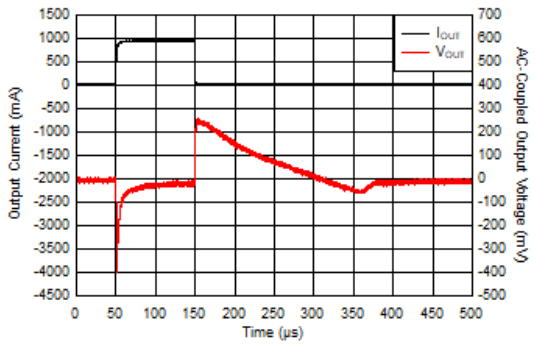
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.4 A/µs

図 5-6. I_{OUT} Transient From 0 mA to 100 mA

Copyright © 2024 Texas Instruments Incorporated

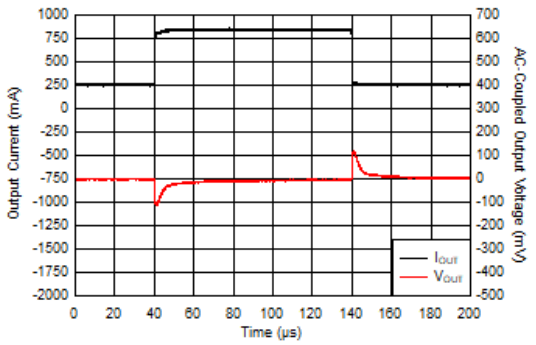
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



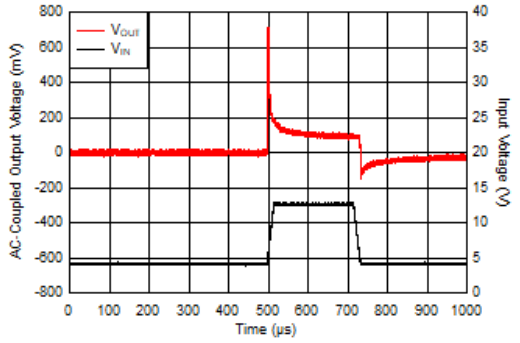
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.5 A/µs

図 5-7. I_{OUT} Transient From 1 mA to 1 A



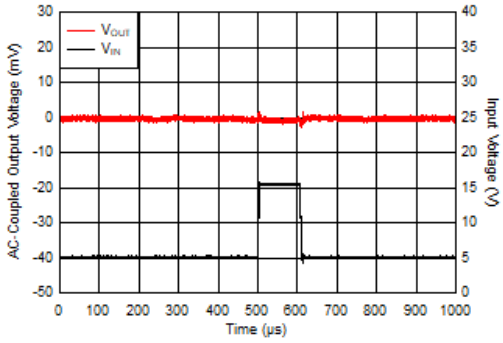
V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.8 A/µs

図 5-8. I_{OUT} Transient From 250 mA to 850 mA



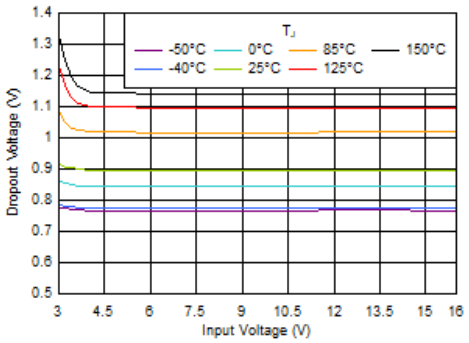
V_{IN} = 5 V V_{OUT} = 3.3 V, I_{OUT} = 1 A, V_{IN} ramp rate = 0.6 V/µs

図 5-9. V_{IN} Transient in Dropout From 4 V to 13 V



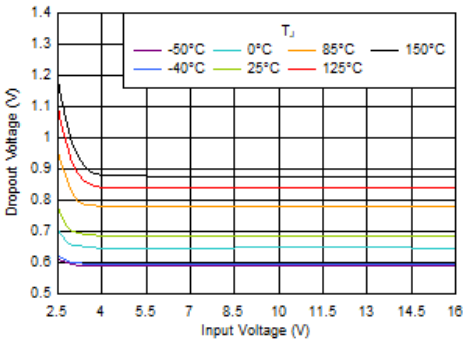
V_{OUT} = 3.3 V, I_{OUT} = 33 µA, V_{IN} ramp rate = 1.6 V/µs

図 5-10. V_{IN} Transient From 5 V to 16 V



I_{OUT} = 1.0 A

図 5-11. V_{DO} vs V_{IN}



I_{OUT} = 0.8 A

図 5-12. V_{DO} vs V_{IN}

Copyright © 2024 Texas Instruments Incorporated

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)

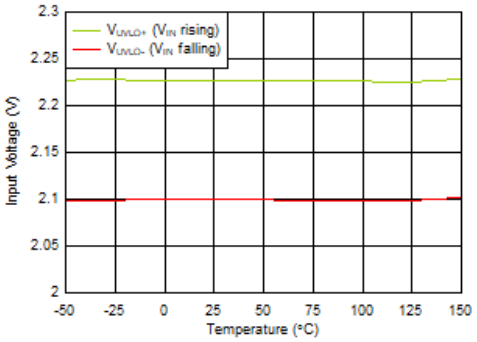
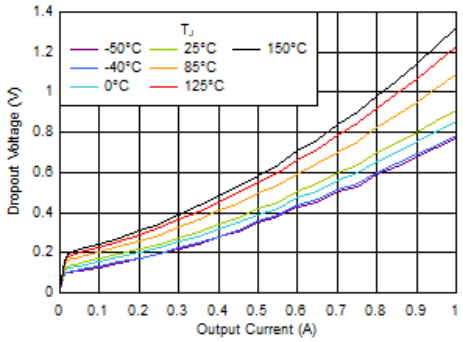
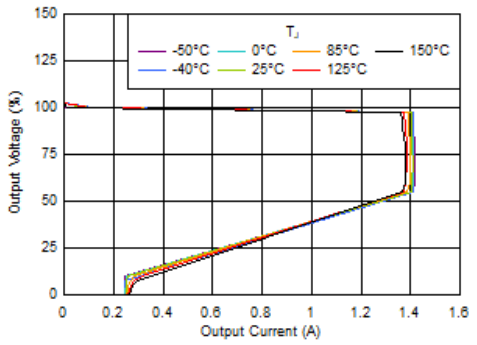


図 5-13. UVLO Thresholds vs Temperature



For V_{IN} ≥ 3.0 V

図 5-14. V_{DO} vs I_{OUT}



For V_{IN} ≥ 3.0 V

図 5-15. Foldback Current Limit vs Temperature

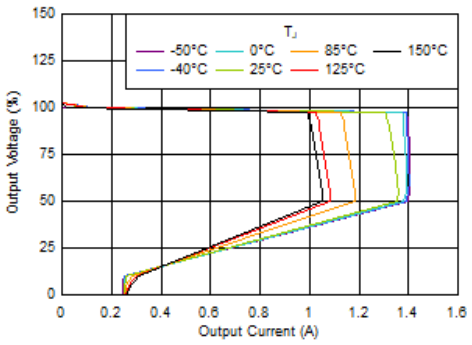
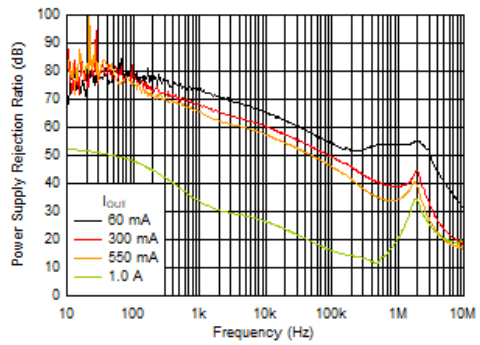
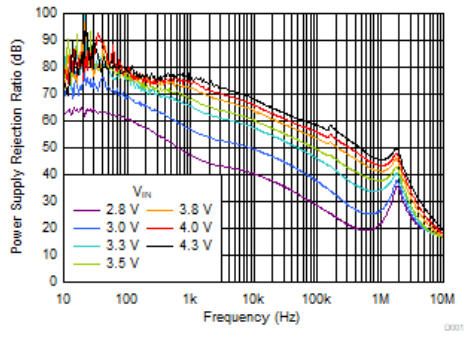


図 5-16. Foldback Current Limit vs Temperature



V_{OUT} = 1.8 V, V_{IN} = 3.3 V

図 5-17. PSRR vs I_{OUT}



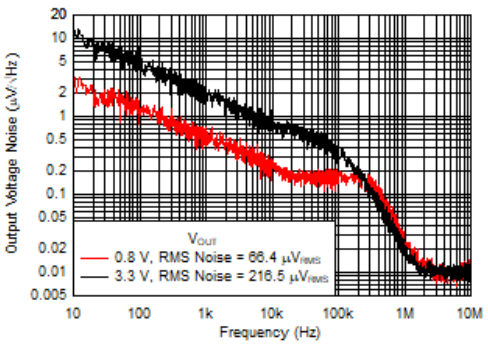
V_{OUT} = 1.8 V, I_{OUT} = 0.55 A

図 5-18. PSRR vs V_{IN}

Copyright © 2024 Texas Instruments Incorporated

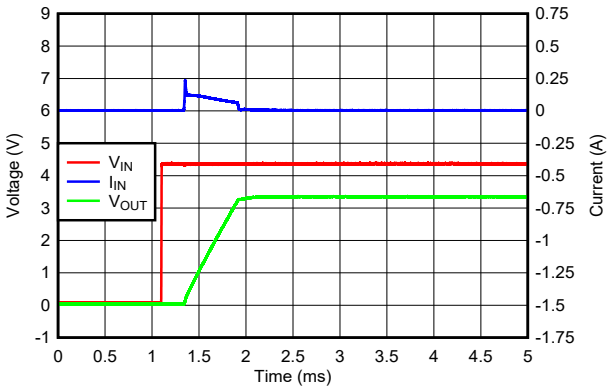
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



I_{OUT} = 0.1 A, RMS noise BW = 10 Hz to 100 kHz

図 5-19. Output Noise (V_n) vs V_{OUT}



I_{OUT} = 0.1 A, C_{OUT} = 22 µF

図 5-20. Inrush Current With 22 µF at C_{OUT}

Copyright © 2024 Texas Instruments Incorporated

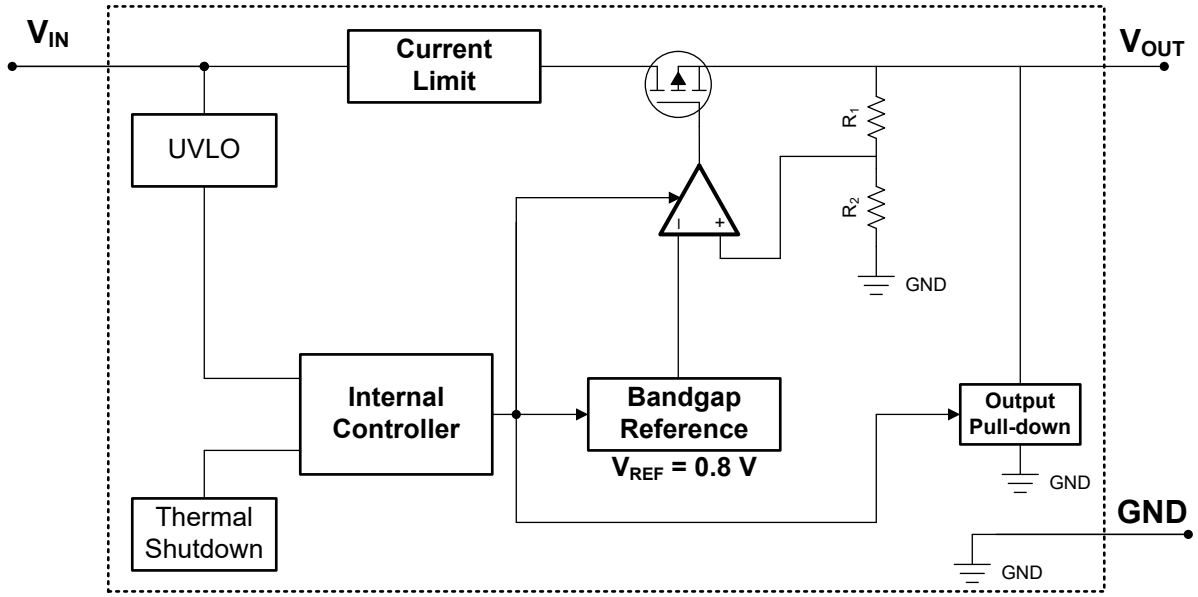
6 Detailed Description

6.1 Overview

The TLV761 is a low quiescent current, high PSRR linear regulator capable of sourcing load current up to 1 A. This device is designed for high current applications such as appliances where there are increasingly stringent requirements for standby and active power consumption.

This device features integrated foldback current limit, thermal shutdown, internal output pulldown, and undervoltage lockout (UVLO). This device delivers excellent line and load transient performance. The TLV761 is low noise and exhibits very good PSRR. The operating ambient temperature range of the device is –40°C to +125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

Copyright © 2024 Texas Instruments Incorporated

6.3.2 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 50% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 6-1 shows a diagram of the foldback current limit.

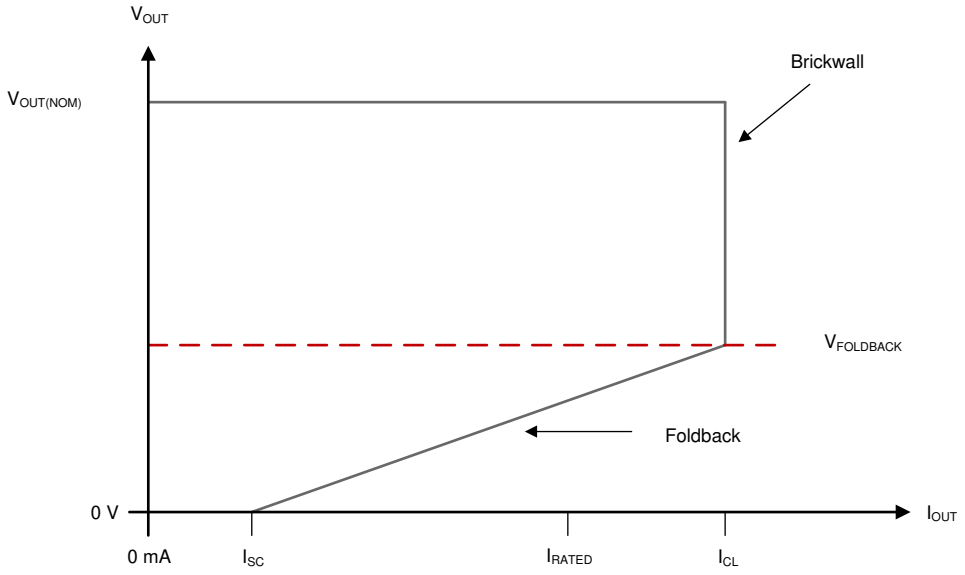


図 6-1. Foldback Current Limit

6.3.3 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

Copyright © 2024 Texas Instruments Incorporated

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

Copyright © 2024 Texas Instruments Incorporated

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.1.3 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Copyright © 2024 Texas Instruments Incorporated

図 7-1 shows one approach for protecting the device.

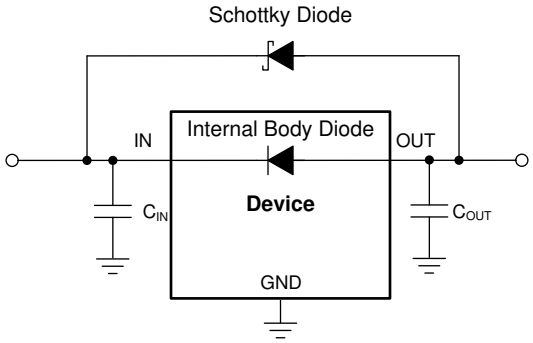


図 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

Copyright © 2024 Texas Instruments Incorporated

7.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J). As described in the following equations, use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (5)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2 Typical Application

The TLV761 is a low quiescent current linear regulator designed for high current applications. Unlike most typical high current linear regulators, the TLV761 consumes significantly less quiescent current. This device delivers excellent line and load transient performance. The device is low noise and exhibits a very good PSRR. As a result, the TLV761 is designed for high current applications that require very sensitive power-supply rails.

This regulator offers both current limit and thermal protection. The operating ambient temperature range of the device is –40°C to +125°C.

図 7-2 shows a typical application circuit for this device.

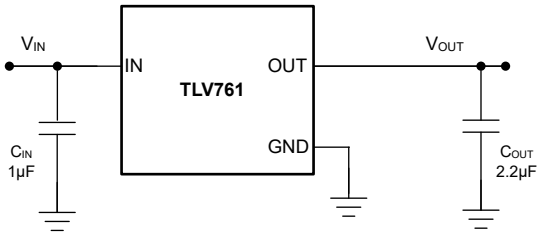


図 7-2. Typical Application Circuit

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	12 V
Output voltage	3.3 V
Output current	50 mA

7.2.2 Detailed Design Procedure

For this design example, the 3.3-V, fixed-version TLV76133 is selected and is powered by a standard 12-V input supply. The dropout voltage (V_{DO}) is kept within the TLV761 dropout voltage specification for the 3.3-V output voltage option to keep the device in regulation under all load and temperature conditions for this design. A 1.0-µF output capacitor is recommended for excellent load transient response. The input capacitor is optional and is used to reduce the input impedance of the circuit and improve the transient response.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude.

7.3 Best Design Practices

Place input and output capacitors as close to the device as possible.

Use a ceramic output capacitor.

Do not exceed the device absolute maximum ratings.

7.4 Power Supply Recommendations

Connect a low output impedance power supply directly to the INPUT pin of the device . Inductive impedances between the input supply and the INPUT pin can create significant voltage excursions at the INPUT pin during start-up or load transient events.

Copyright © 2024 Texas Instruments Incorporated

7.5 Layout

7.5.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve characteristic AC performance such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the GND pin of the device. Higher value ESR capacitors can degrade PSRR performance.

7.5.2 Layout Examples

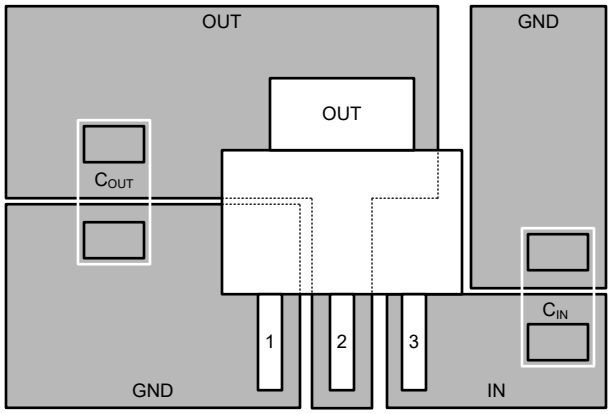


図 7-3. Layout Example for DCY (SOT-223) Package

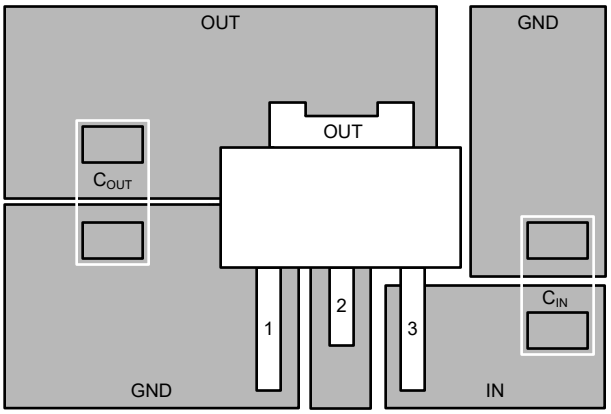


図 7-4. Layout Example for KVU (TO-252) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Available Options(1) (2)

PRODUCT	V_{OUT}
TLV761**xxyyyz**	**xx** is the nominal output voltage (for example 33 = 3.3 V). **yyy** is the package designator. **z** is the package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) The device is available in factory-programmable fixed output voltage increments of 50 mV upon request.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV1117 Adjustable and Fixed Low-Dropout Voltage Regulator* data sheet
- Texas Instruments, *LM1117 800-mA Low-Dropout Linear Regulator* data sheet

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Copyright © 2024 Texas Instruments Incorporated

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (February 2023) to Revision C (April 2024)	Page
• 「事前情報」として KVU (TO-252) パッケージをドキュメントに追加	1
• Added KVU package information to *Pin Configuration and Functions* section	3
• Increased absolute maximum ratings to 20V for Input pin	4
• Added thermal numbers for KVU (TO-252) package	5
• Changed output voltage value from *5 V* to *3.3 V* in *Design Parameters* table	16
• Added *Layout Example for KVU (TO-252) Package* image to *Layout Examples* section	17

Changes from Revision A (December 2022) to Revision B (February 2023)	Page
• Deleted $I_{SHUTDOWN}$ curves and all data below V_{IN} < 3.0 V in *Electrical Characteristics* table and *Typical Characteristics* section	6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV76118DCYR	OBSOLETE	SOT-223	DCY	4		TBD	Call TI	Call TI	-40 to 125		
TLV76112DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76112C	Samples
TLV76118DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76118C	Samples
TLV76125DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76125C	Samples
TLV76130DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76130C	Samples
TLV76133DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76133C	Samples
TLV76133KVUR	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	TLV76133	Samples
TLV76136DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76136C	Samples
TLV76150DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76150C	Samples
TLV76150KVUR	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	TLV76150	Samples
TLV76180DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	76180C	Samples
TLV761C0DCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	761C0C	Samples
TLV761C0KVUR	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	TLV761C0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

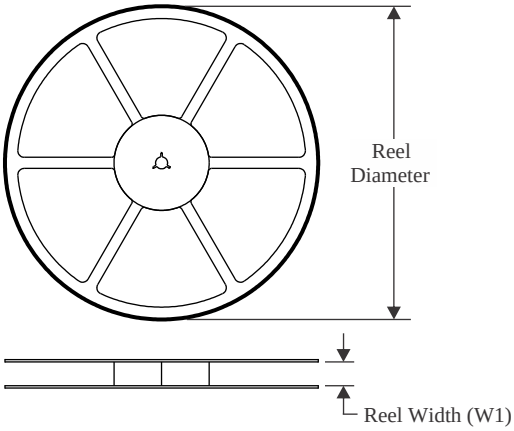
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

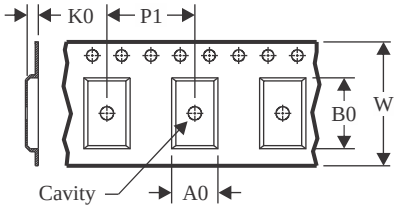
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

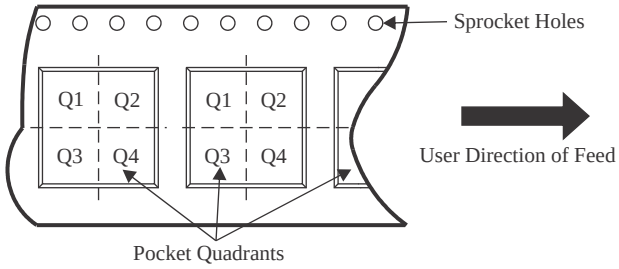


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

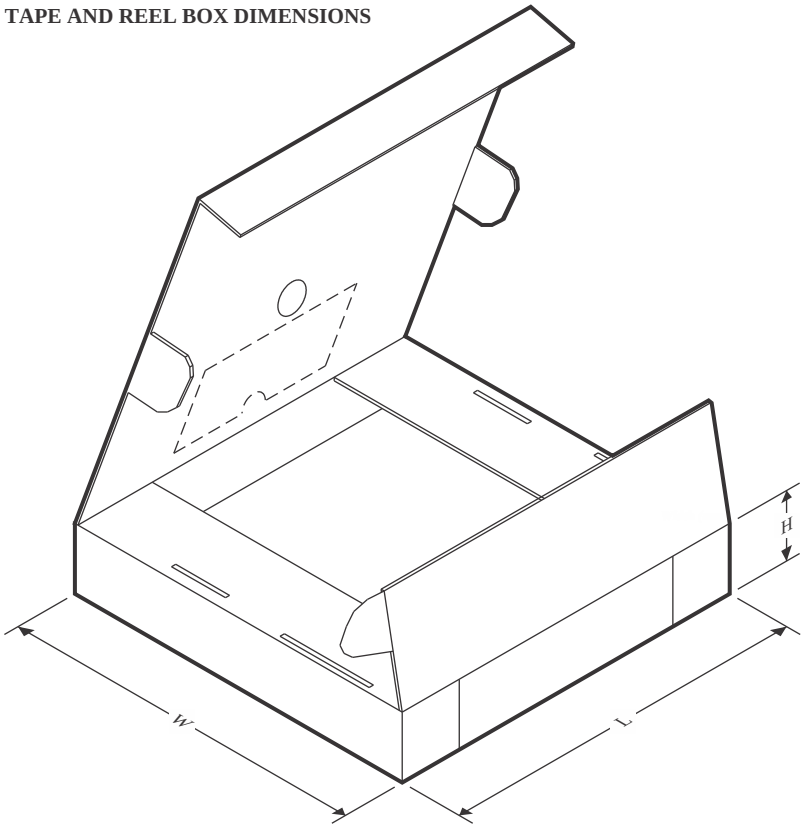
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV76112DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76118DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76125DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76130DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76133DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76133KVUR	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV76136DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76150DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV76150KVUR	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV76180DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV761C0DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV761C0KVUR	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

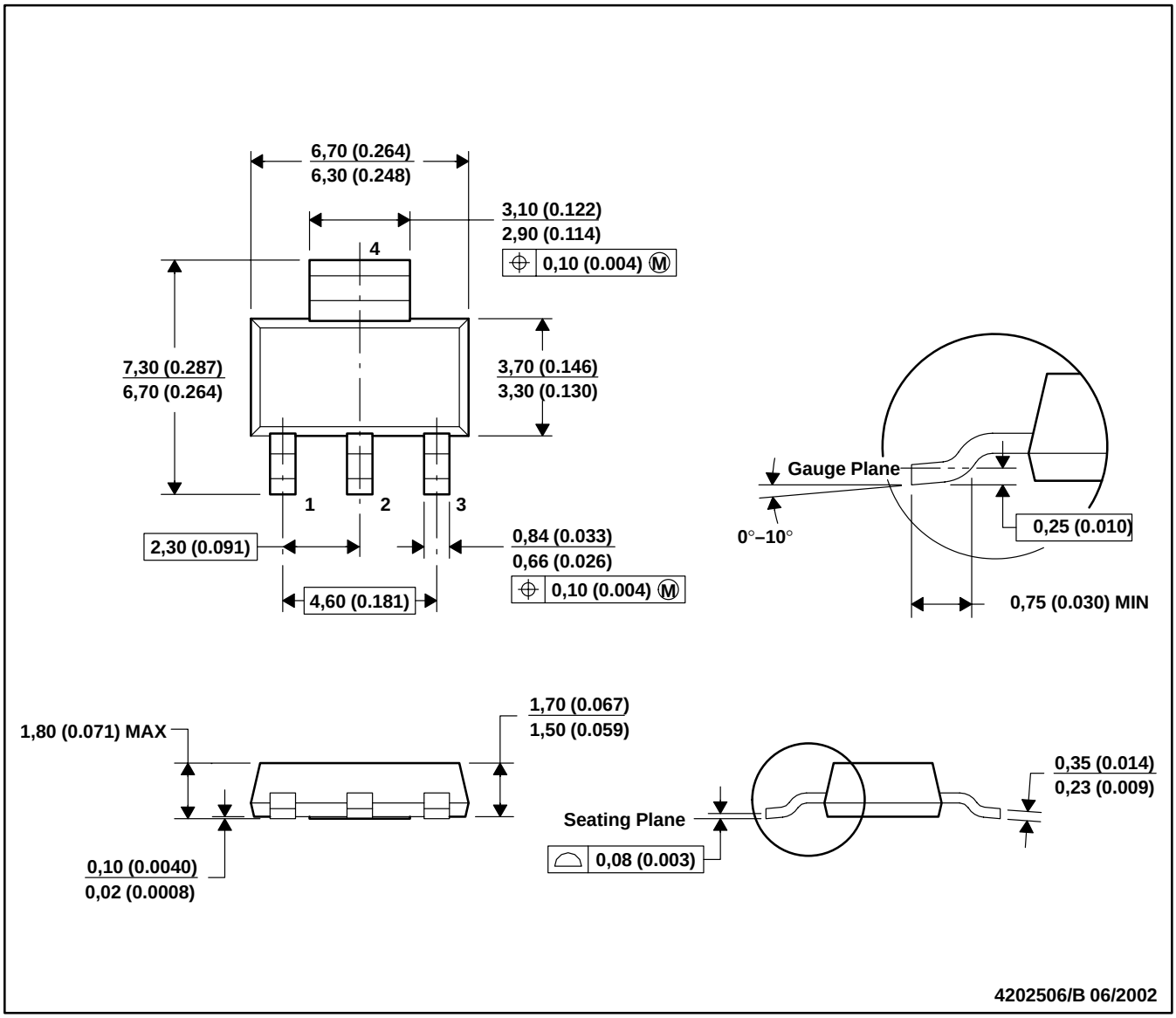


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV76112DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76118DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76125DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76130DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76133DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76133KVUR	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV76136DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76150DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV76150KVUR	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV76180DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV761C0DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV761C0KVUR	TO-252	KVU	3	2500	340.0	340.0	38.0

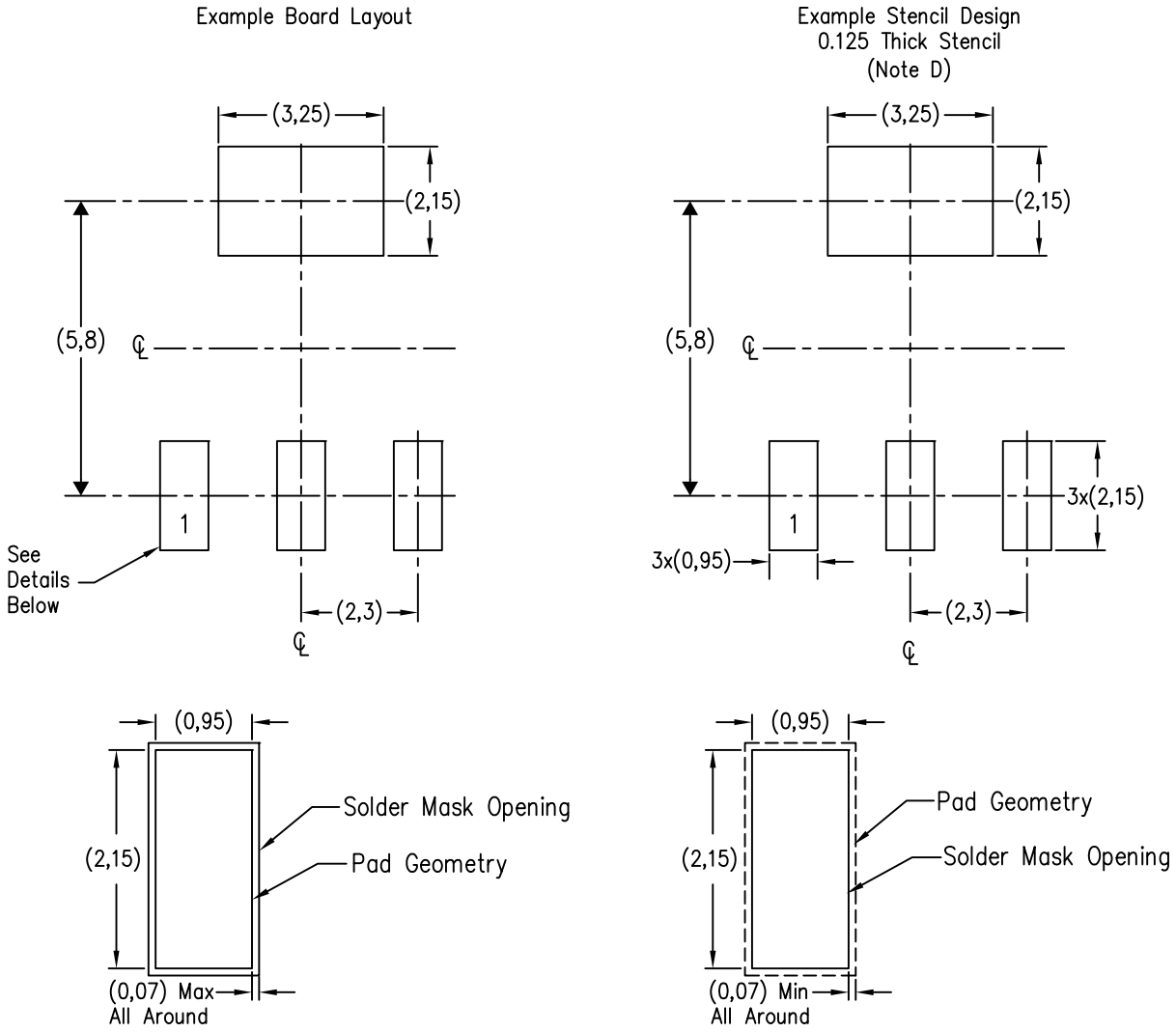
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



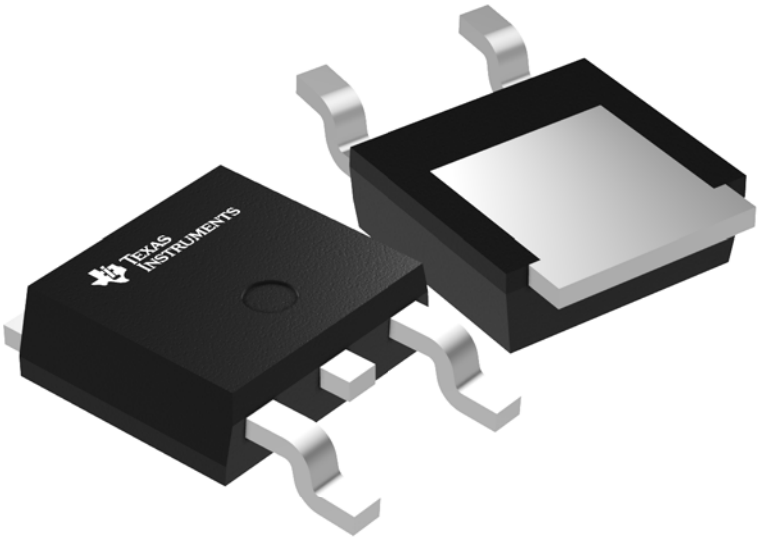
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



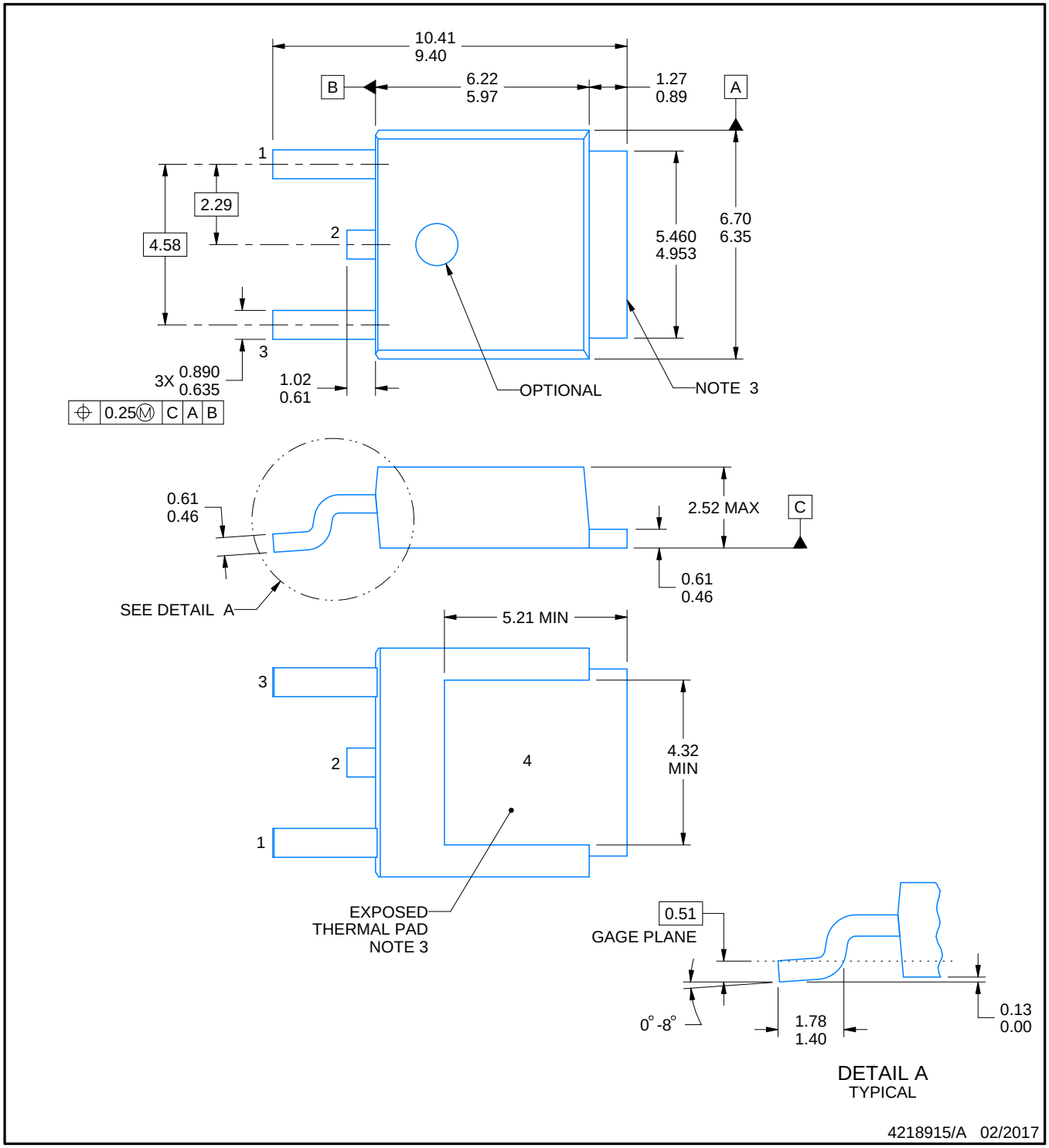
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

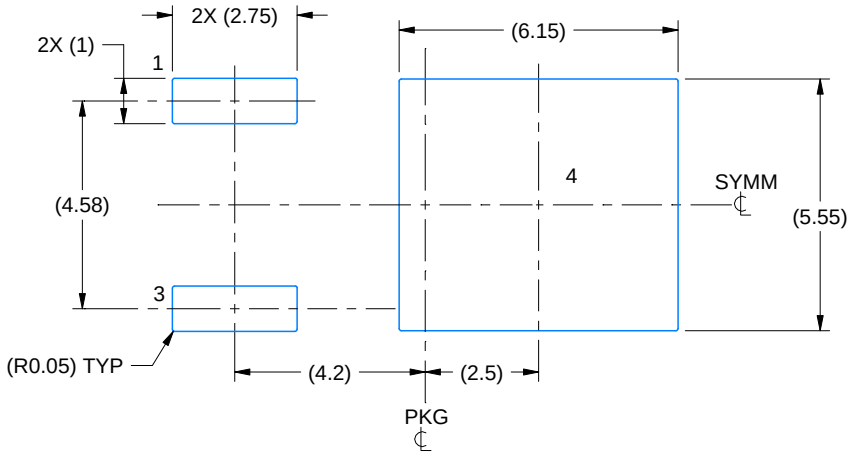
TO-252 - 2.52 mm max height

TO-252

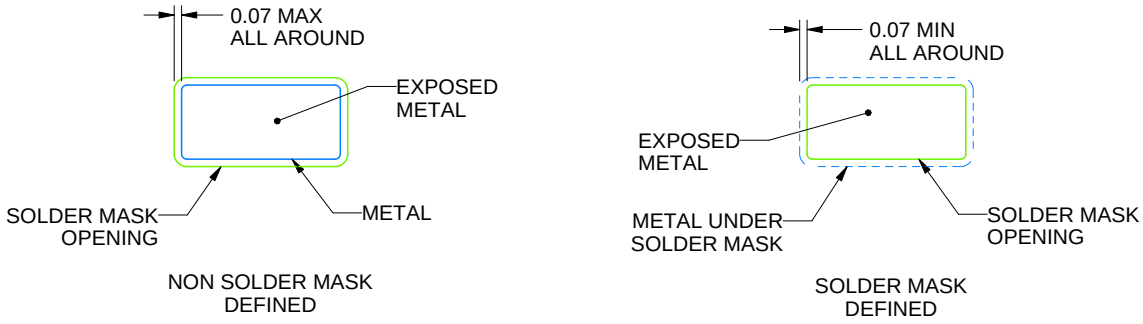


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

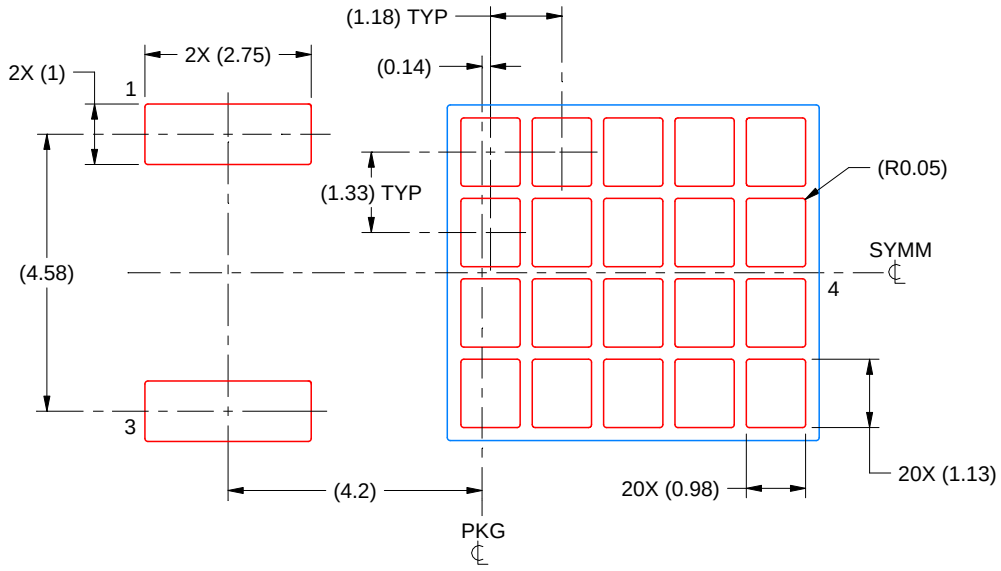
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated