TLV774 300mA、小型、高 PSRR、調整可能な低ドロップアウト レギュレータ

1 特長

- 高 PSRR：60dB (1kHz)、45dB (1MHz)
- V_{IN} 範囲：1.4V～5.5V
- 固定出力電圧範囲：0.6V～3.3V
- 出力電圧精度：2%
- Low ドロップアウト電圧：
  - 全温度範囲について 300mA で最大 310mV ($1.2V_{OUT}$)
- フォールドバック電流制限
- アクティブな出力プルダウン抵抗
- パッケージ：
  - 1mm × 1mm の 4 ピン X2SON (DQN)

2 アプリケーション

- スマートフォン
- タブレット
- ゲーム機
- ノート PC
- ストリーミング メディア プレーヤ
- セットトップ ボックス
- カメラ モジュール

3 概要

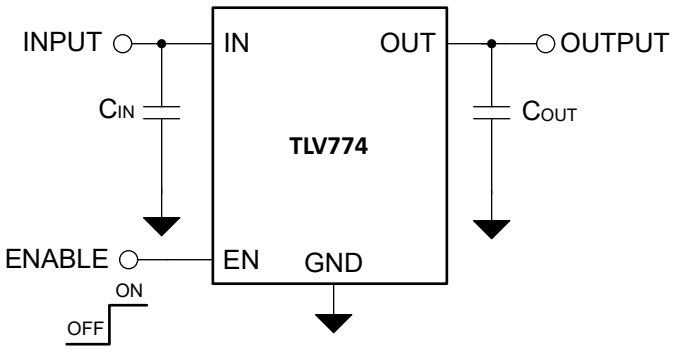
TLV774 は、300mA の出力電流を供給できる小型の低ドロップアウト (LDO) リニア電圧レギュレータです。この LDO は、高 PSRR の電源になるよう設計されています。また、このデバイスは各種の回路の要件を満たす負荷およびライン過渡性能も提供します。1.4V～5.5V の入力電圧範囲と 0.6V～3.3V の出力電圧範囲に対応する TLV774 は、さまざまなアプリケーションで使用できる柔軟性を備えています。

TLV774 は、過度な突入電流を回避するための内部ソフトスタートを備えているため、スタートアップ時の入力電圧降下を最小限に抑えることができます。LDO がディセーブルされると、アクティブ プルダウン回路により出力が迅速に放電され、既知のスタートアップ状態が得られます。EN 入力により、外部の論理信号を使用してレギュレーション出力をイネーブルまたはディセーブルできます。LDO は小さなセラミック コンデンサで安定して動作するため、パッケージ サイズ全体を小型化できます。動作時の接合部温度範囲は、−40℃～+125℃です。この LDO は、標準の 1mm × 1mm X2SON (DQN) パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TLV774	DQN (X2SON、4)	1mm × 1mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路

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4 Pin Configuration and Functions

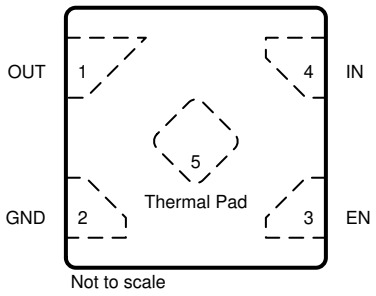


図 4-1. DQN Package, 1mm × 1mm, 4-Pin X2SON (Top View)

表 4-1. Pin Functions

NAME	X2SON	TYPE(1)	DESCRIPTION
EN	3	I	Enable input. A low voltage (< $V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{EN(HI)}$) on this pin enables the regulator output.
GND	2	G	Common ground.
IN	4	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground. See the *セクション 5.3* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *セクション 5.3* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode (V_{EN}< $V_{EN(LOW)}$).
Thermal Pad	5	—	Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance.

(1) I = input, O = output, I/O = input or output, and G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6.5	V
	Output, V_{OUT}	–0.3	6.0 or V_{IN} + 0.3 (2)	
	Enable, V_{EN}	–0.3	6.5	
Current	Maximum output, I_{OUT} (4)	Internally limited		A
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The maximum value of V_{OUT} is the lesser of 6.0V or (V_{IN} + 0.3V).
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.4		5.5	V
V_{EN}	Enable input voltage	0		5.5	V
V_{OUT}	Nominal output voltage range	0.6		3.3	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor(2)		1		µF
C_{OUT}	Output capacitance(3)	0.47		40	µF
ESR	Output capacitor effective series resistance			100	mΩ
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47µF minimum is recommended to counteract the effect of source resistance and inductance, which in some cases causes symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients. If needed use a larger input capacitance, depending on the characteristics of the input voltage source.
(3) Effective output capacitance of 0.47µF minimum and 40µF maximum is required for stability. The effective output capacitance accounts for tolerance, temperature, voltage, and any other factors that affect the value, and is often 50% smaller than the capacitors specified value.

5.4 Thermal Information

THERMAL METRIC[1]		TLV774 DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	209.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	172.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	171.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	149.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

specifications apply for T_J = 25℃, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.4 V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25℃

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance		0.6V ≤ V_{OUT} < 1.8V	–2.5		2.5	%
			1.8V ≤ V_{OUT} ≤ 3.3V	–2		2	
		T_J = –40℃ to 85℃	0.6V ≤ V_{OUT} < 1.2V	–3.33		3.33	
			1.2V ≤ V_{OUT} < 1.8V	–3		3	
			1.8V ≤ V_{OUT} < 2.5V	–2.75		2.75	
			2.5V ≤ V_{OUT} ≤ 3.3V	–2.5		2.5	
ΔV_{OUT} / ΔV_{IN}	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V			0.01	0.1	%/V
ΔV_{OUT} / ΔI_{OUT}	Load regulation	I_{OUT} = 1mA to 300mA			85	110	µV/mA
I_{GND}	Quiescent ground current	I_{OUT} = 0mA, T_J = –40°C to 85°C	V_{EN} = V_{IN} = 1.6V		76		µA
			V_{EN} = V_{IN} = 4V		89		
			V_{EN} = V_{IN} = 5.5V		98	141	
I_{SHDN}	Shutdown ground current	V_{EN} < $V_{EN(LOW)}$, V_{IN} = 5.5V, T_J = –40°C to 85°C			0.01	2	µA
V_{DO}	Dropout voltage	I_{OUT} = 300mA, V_{IN} = $V_{OUT(NOM)}$	1.2V ≤ V_{OUT} < 1.8V(1) (2)			265	mV
			1.8V ≤ V_{OUT} < 2.5V			170	
			2.5V ≤ V_{OUT} < 2.8V			125	
			2.8V ≤ V_{OUT} ≤ 3.3V		100	145	
		I_{OUT} = 300mA, V_{IN} = $V_{OUT(NOM)}$, T_J = –40°C to 85°C	1.2V ≤ V_{OUT} < 1.8V(1) (2)			310	
			1.8V ≤ V_{OUT} < 2.5V			200	
			2.5V ≤ V_{OUT} < 2.8V			150	
			2.8V ≤ V_{OUT} ≤ 3.3V			165	
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, T_J = –40°C to 85°C		350		800	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0V			73		mA
PSRR	Power-supply rejection ratio	I_{OUT} = 150mA, V_{IN} = V_{OUT} + 1.0V	f = 1kHz		60		dB
			f = 100kHz		56		
			f = 1MHz		45		
V_N	Output noise voltage	BW = 10Hz to 100kHz, I_{OUT} = 50mA			75 x Vout		μV_{RMS}
$R_{PULLDOWN}$	Output automatic discharge pulldown resistance	V_{EN} < $V_{EN(LOW)}$ (output disabled), V_{IN} = 3.3V			135		Ω
T_{SD}	Thermal shutdown	T_J rising			160		°C
		T_J falling			140		
$V_{EN(LOW)}$	Low input threshold	V_{EN} falling until the output is disabled, T_J = –40°C to 85°C				0.3	V
$V_{EN(HI)}$	High input threshold	V_{EN} rising until the output is enabled, T_J = –40°C to 85°C		0.9			V
I_{EN}	EN input leakage current	V_{EN} = 5.5V and V_{IN} = 5.5V			0.01	1	µA

(1) For V_{OUT} < 1.4V, dropout is tested with V_{IN} = 1.4V.
(2) For V_{OUT} ≤ 1.0V, Dropout voltage < headroom voltage. At V_{IN} = 1.4V, a 1.0V or lower output device is not in dropout. Headroom voltage = V_{IN} - V_{OUT}.

5.6 Switching Characteristics

specifications apply for T_J = 25℃, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.4V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); all typical values are at T_J = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time (V_{EN})	From V_{EN} > $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, V_{IN} rise time = 1V/µs		400		µs

5.7 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)

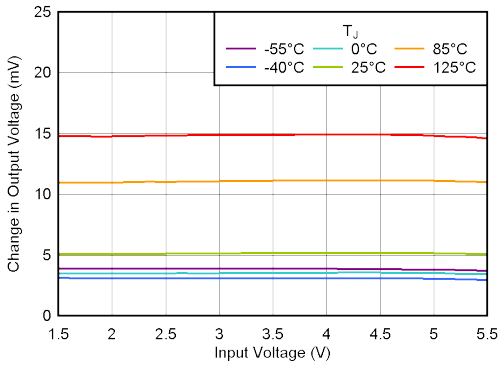


図 5-1. Line Regulation vs V_{IN}

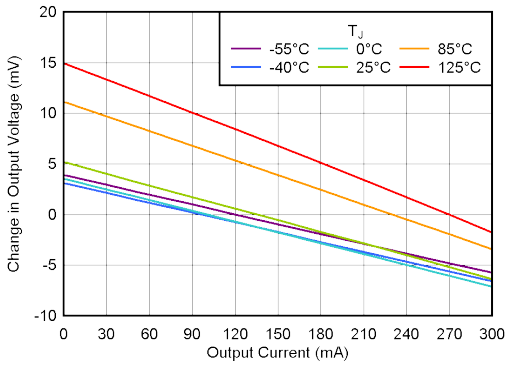


図 5-2. Load Regulation vs I_{OUT}

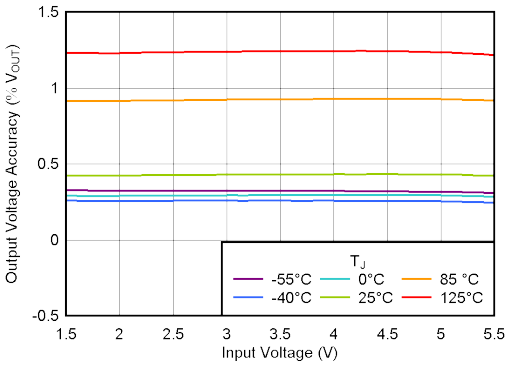


図 5-3. Output Voltage Accuracy vs V_{IN}

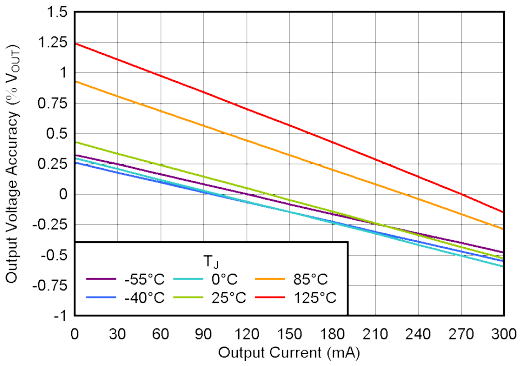
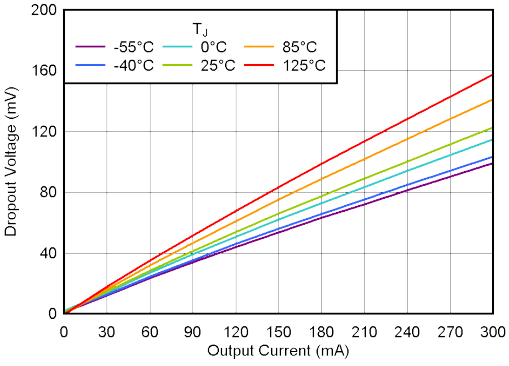
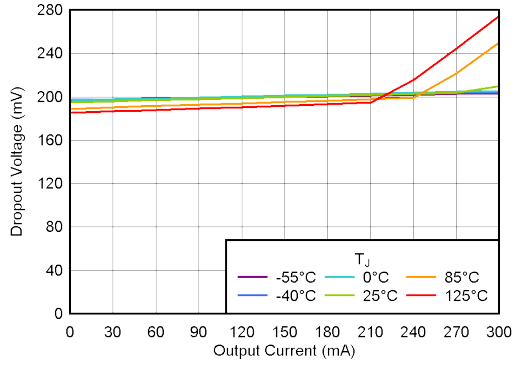


図 5-4. Output Voltage Accuracy vs I_{OUT}



V_{OUT} = 3.3V, Test condition: V_{IN} = $V_{OUT(NOM)}$

図 5-5. Dropout Voltage vs I_{OUT}



V_{OUT} = 1.2V, Test condition: V_{IN} = 1.4V

図 5-6. Dropout Voltage vs I_{OUT}

5.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)

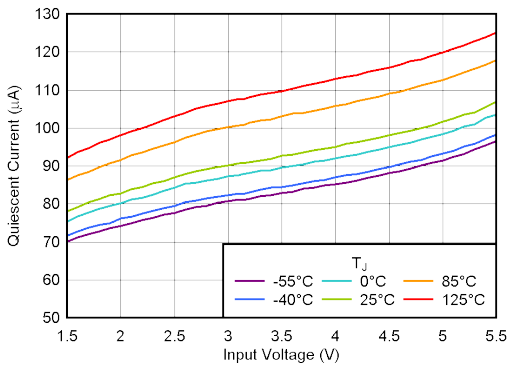


図 5-7. Quiescent Current vs V_{IN}

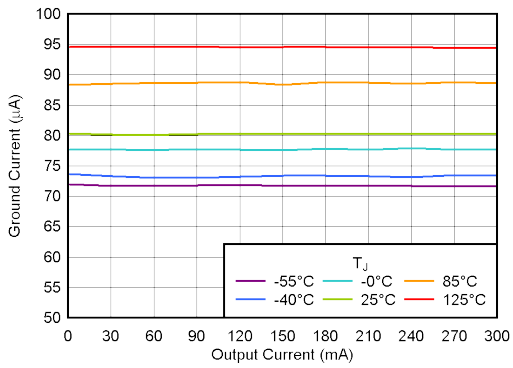
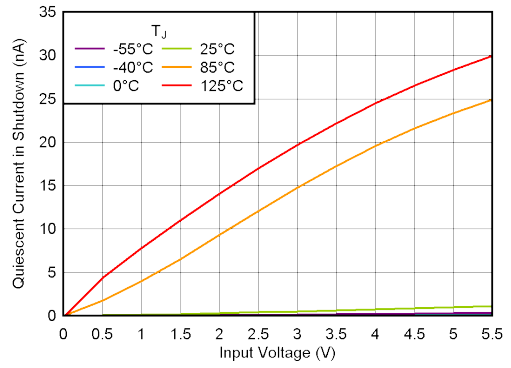
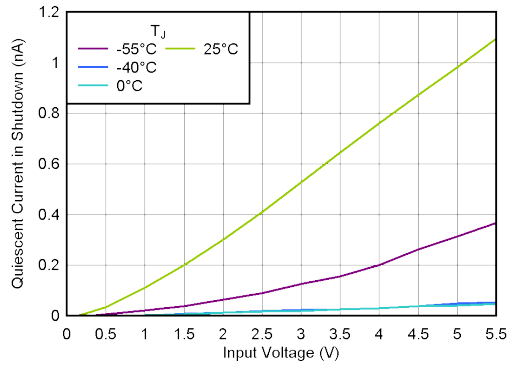


図 5-8. Ground Current vs I_{OUT}



V_{EN} = 0V, C_{IN}= 0µF

図 5-9. Shutdown Current vs V_{IN}



V_{EN} = 0V, C_{IN}= 0µF

図 5-10. Shutdown Current vs V_{IN}

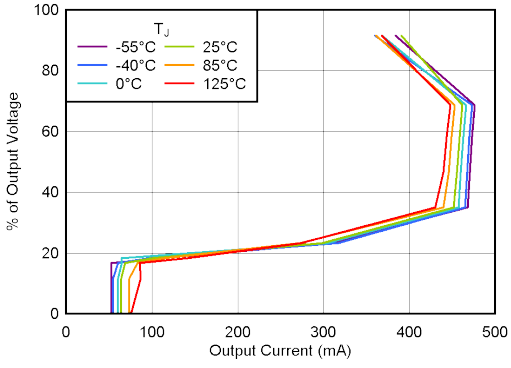


図 5-11. Current Limit

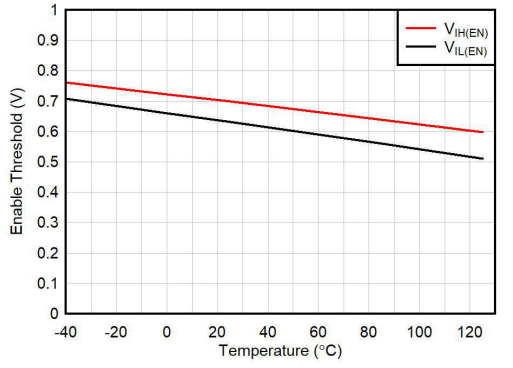
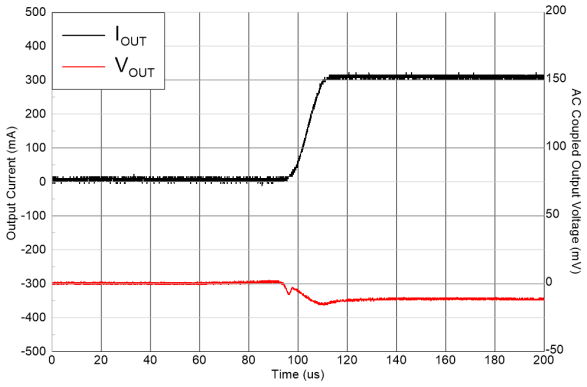


図 5-12. Enable Logic Threshold vs Temperature

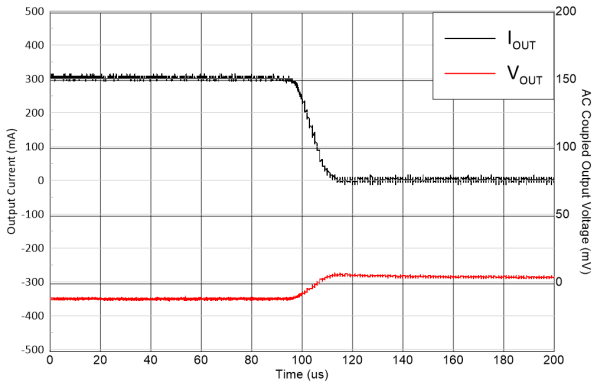
5.7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V, I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



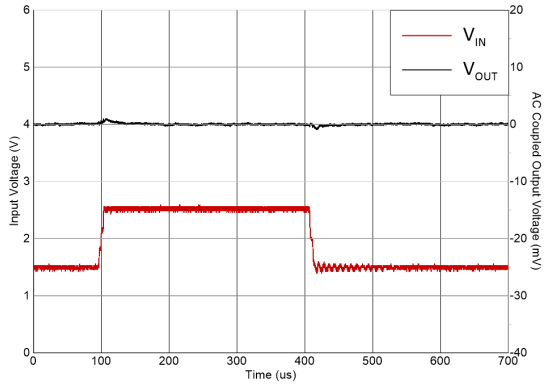
V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 0mA to 300mA, T_{RISING} = 10µs

図 5-13. Load Transient



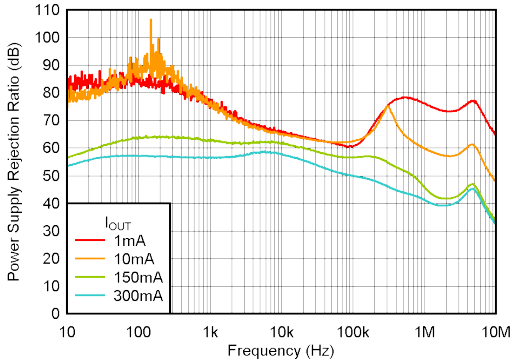
V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 300mA to 0mA, $T_{FALLING}$ = 10µs

図 5-14. Load Transient



V_{IN} = V_{OUT} + 0.3V to V_{OUT} +1.3V

図 5-15. Line Transient



V_{IN} = $V_{OUT(nom)}$ + 1.0V

図 5-16. PSRR vs Frequency

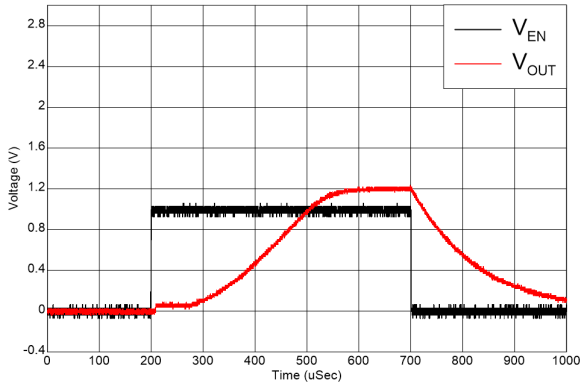
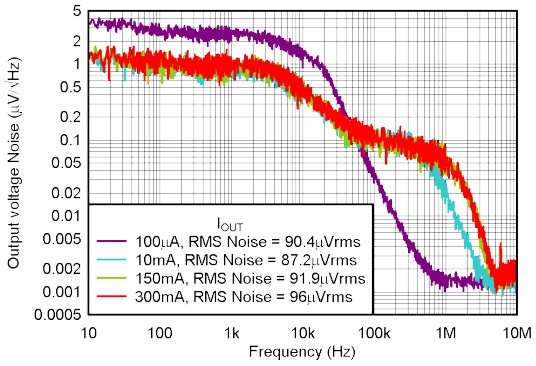


図 5-17. Start-Up



V_{OUT} = 1.2V, RMS Noise BW = 10Hz to 100kHz

図 5-18. Noise

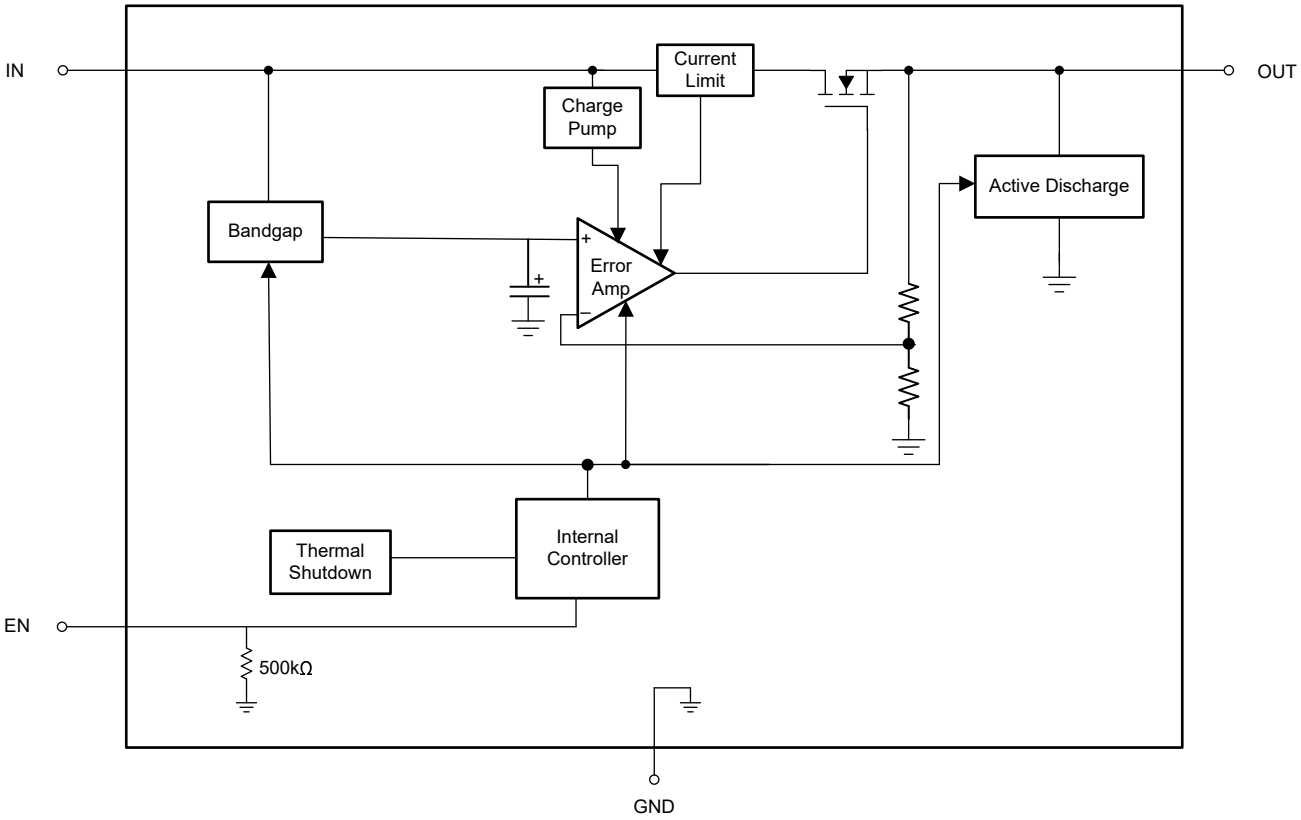
6 Detailed Description

6.1 Overview

The TLV774 provides high PSRR and good transient response in a small, 300mA LDO.

This LDO is designed to operate with a single 1µF input capacitor and a single 1µF ceramic output capacitor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *セクション 5.3* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.2 Active Discharge

The regulator has an internal MOSFET that connects a pulldown resistor between the output and ground when the device is disabled. This connection actively discharges the output voltage. The active discharge circuit is activated by the enable pin or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses. Reverse current flow from the output to the input potentially causes damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current termed the *short-circuit current limit (I_{SC})*. I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 6-1 shows a diagram of the foldback current limit.

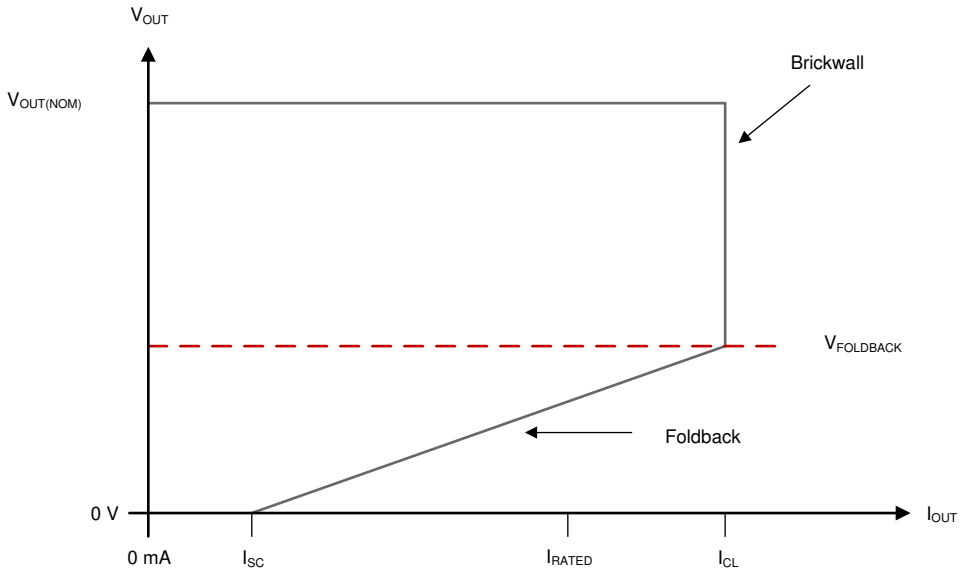


図 6-1. Foldback Current Limit

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the セクション 5.3 table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

6.4.3 Disabled

Shutdown the device output by forcing the enable pin voltage to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor turns off and internal circuits shut down. The output voltage is also actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *セクション 5.3* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. For typical operation of the TLV774, connect a 1µF capacitor to the input. Use a higher value capacitor if large, fast rise-time, load, or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *セクション 5.3* table for stability. Make sure the minimum derated output capacitance is equal to or greater than 0.47µF. When the output voltage is ramping up, the inrush current depends on the size of the output capacitance. During start-up, the output current is potentially as high as the current limit value for larger output capacitors.

7.2 Typical Application

7.2.1 Application

図 7-1 shows a typical application circuit for the TLV774.

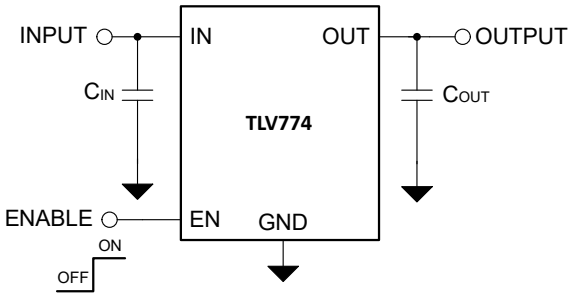


図 7-1. TLV774 Typical Application

7.2.2 Design Requirements

表 7-1 summarizes the design requirements for 図 7-1.

表 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.0V ± 5%
Output voltage	3.3V
Output current	200mA
Maximum ambient temperature	85°C

7.2.3 Detailed Design Procedure

For this design example, the 3.3V output version (TLV77433) is selected. A nominal 4.0V input supply is assumed. Use a minimum 1µF input capacitor to minimize the effect of resistance and inductance between the 4.0V source and LDO input. Use a minimum 0.47µF output capacitance for stability and good load transient response. The dropout voltage (V_{DO}) is less than 165mV maximum at a 3.3V output voltage and 300mA output current. There are no dropout issues with a minimum 3.8V input voltage (4.0V − 5%) and a maximum 200mA output current.

7.2.4 Application Curves

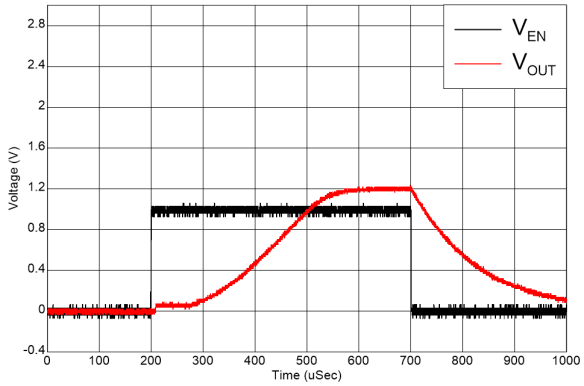


図 7-2. Start-Up

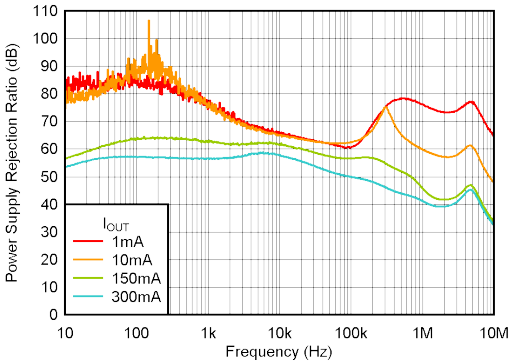


図 7-3. PSRR

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.4V to 5.5V. Make sure the input supply is well regulated and free of spurious noise. Also make sure the output voltage is well regulated and dynamic performance is optimum. Thus, set the input supply to at least $V_{OUT(nom)}$ + 0.5V or 1.4V, whichever is greater.

Use a 1µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via wicks solder or solder paste away from the thermal pad joint during the soldering process. Thus, leading to a compromised solder joint on the thermal pad.

7.4.2 Layout Example

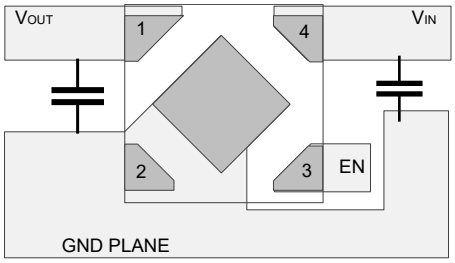


図 7-4. DQN Package (X2SON) Typical Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TLV774**xx(x)(P)yyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number. Otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V). **(P)** indicates an active output discharge feature. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Know Your Limits* application note

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2024) to Revision A (December 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• デバイスのステータスを「事前情報」から「量産」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV77408PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV77412PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV77418PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV77433PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TLV77408PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R2	Samples
TLV77412PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4	Samples
TLV77433PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

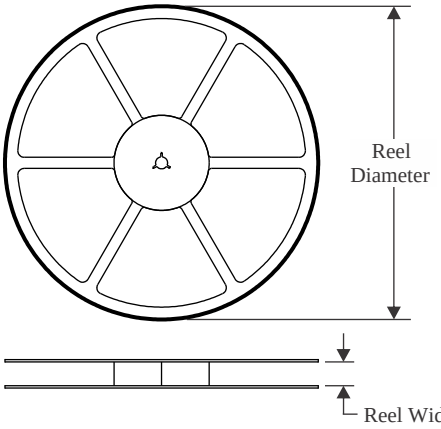
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

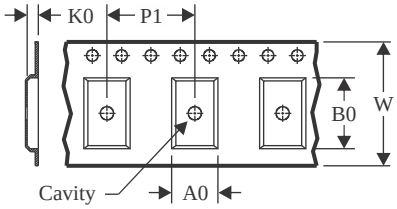
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

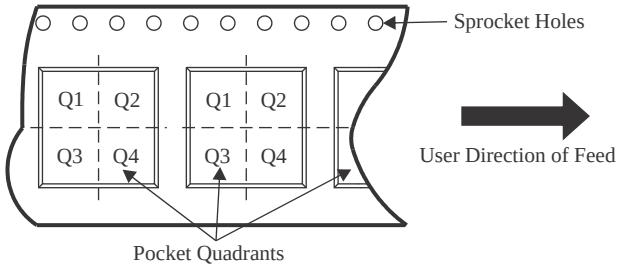


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

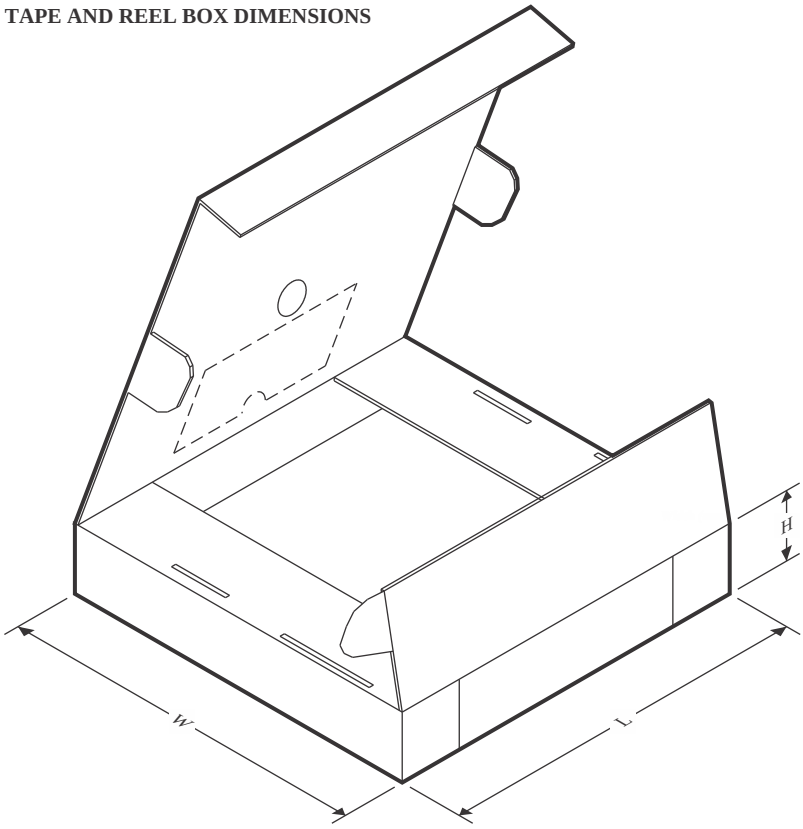
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV77408PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV77412PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV77433PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV77408PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV77412PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV77433PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

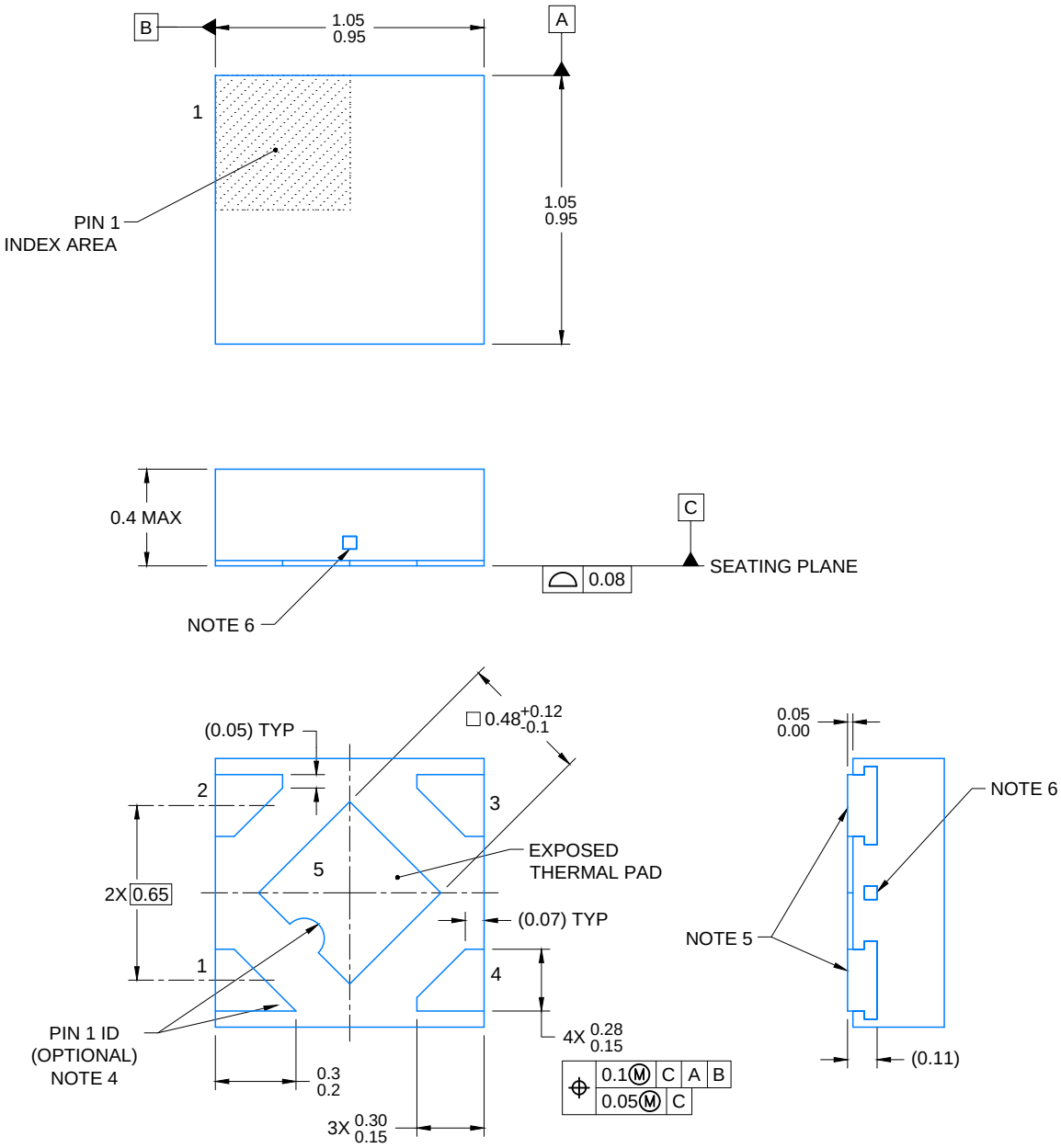
4210367/F

PACKAGE OUTLINE

DQN0004A

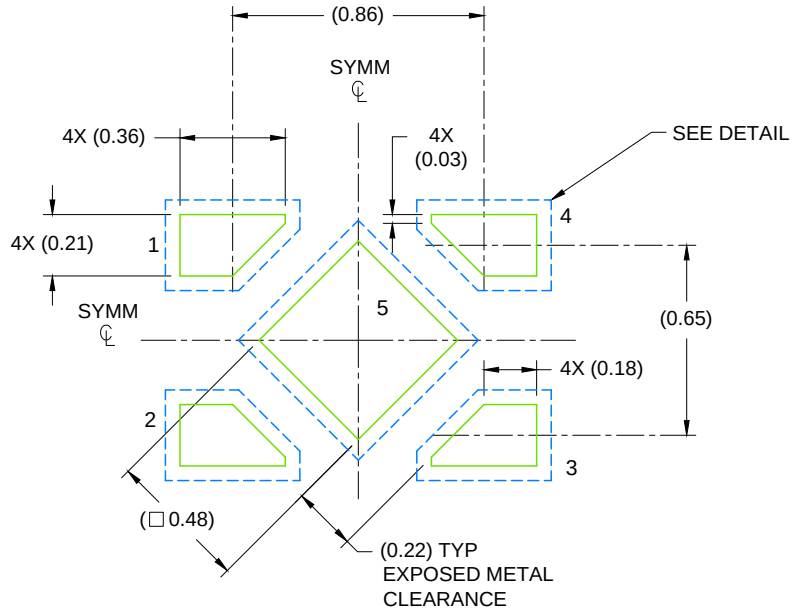
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



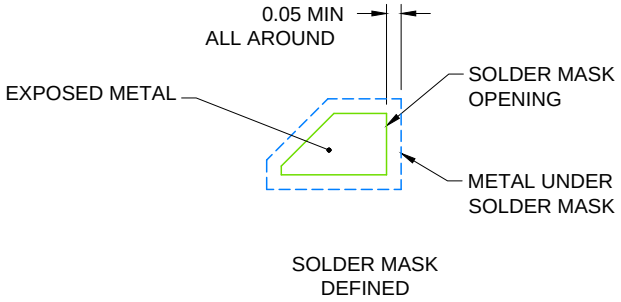
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

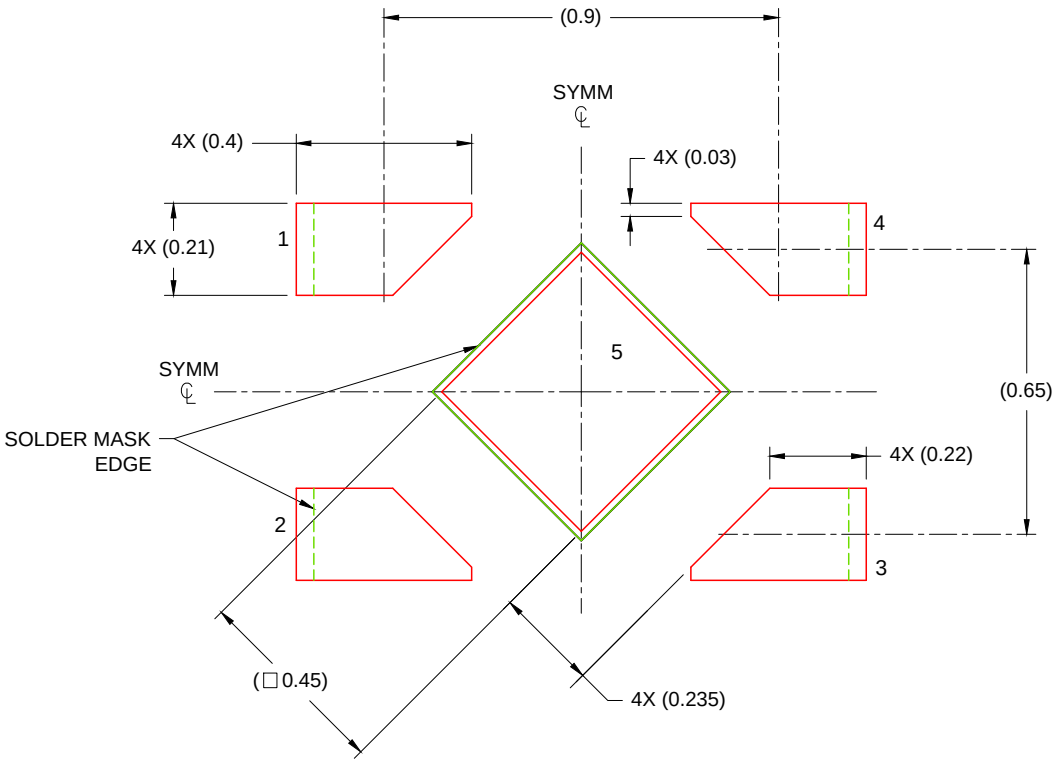


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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