TEXAS INSTRUMENTS
TMP4718
JAJSJN1A – MAY 2023 – REVISED SEPTEMBER 2023

TMP4718 高精度リモート / ローカル温度センサ、ピン・プログラマブル型アラート・スレッショルド付き

1 特長

- 電源電圧範囲:1.62V～5.5V
- 広い動作範囲:-40℃～125℃
- リモート・チャネル精度:1℃
  - 分解能:0.125℃
- ローカル・チャネル精度:1℃
  - 分解能:1℃
- I²C および SMBus インターフェイスをサポート
- 低消費電力
- リモート・ダイオードのフォルト検出
- プログラム可能なデジタル・フィルタ
- 直列抵抗キャンセル
- $\overline{\text{ALERT}}$ および $\overline{\text{T_CRIT}}$ の制限をプログラム可能
  - デバウンス用のフォルト・キュー
- $\overline{\text{ALERT}}$ および $\overline{\text{T_CRIT}}$ のデフォルトのパワーアップ制限 (高温) を調整可能
- 電源に依存しない 1.2V のロジック互換入力スレッショルド

2 アプリケーション

- 標準的ノート PC
- ラック・サーバー向けマザーボード
- スマート・ネットワーク・インターフェイス・カード (NIC)
- スモール・セル基地局
- ベースバンド・ユニット (BBU)
- ソフトウェア無線
- FPGA 温度のモニタリング

3 概要

TMP4718 は高精度の 1℃温度センサで、1 つのローカル統合センサと 1 つのリモート温度センサ入力を持ち、一般的な MMBT3904 NPN トランジスタなどのダイオード接続トランジスタに接続して、従来のサーミスタや熱電対を置き換えることができます。リモート入力は、マイクロプロセッサ、マイクロコントローラ、または FPGA に内蔵されているサブストレート・サーマル・トランジスタまたはダイオードに接続して、IC のダイ温度を監視することもできます。

TMP4718 は、メイン電源レールに関係なく最低 0.8V までのロジック・レベルで動作する、I2C および SMBus 通信に対応しています。これにより、2 次側の低電圧電源を必要とせずに、低電圧 1.2V MCU との相互運用性を実現できます。TMP4718 には、最大 1kΩ の直列抵抗による温度誤差を自動的に除去する直列抵抗キャンセル機能が含まれているため、サーマル・ダイオードへの配線の柔軟性が向上します。本デバイスは、プログラマブル・オフセット機能により、特定のユーザー環境で事前較正されたデータに基づいて、オフセット調整された温度データをレポートできます。測定は、プログラム可能な変換時間を使用して自動的に実行することも、I²C コマンドによってトリガされるワンショット変換を使用して実行することもできます。

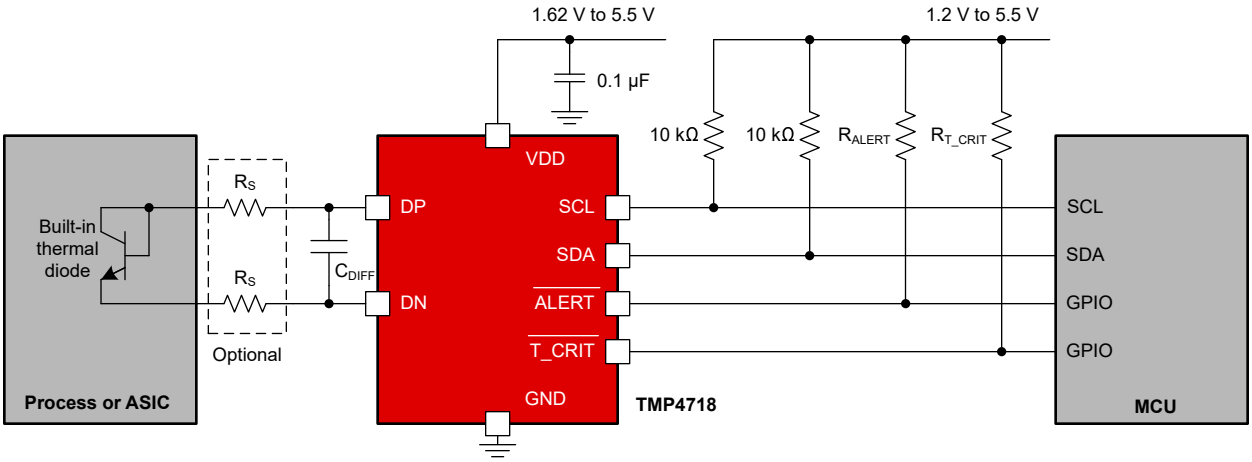
TMP4718A と TMP4718B は同じ機能を提供しますが、SMBus または I²C のデバイス・アドレスが異なります。これにより、システムは同じバス上で 2 つのセンサをサポートできます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
TMP4718	DGK (VSSOP、8)	3.00mm × 4.90mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



概略ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2023) to Revision A (September 2023)	Page
• データシートのステータスを「事前情報」から「量産データ」に変更	1

5 Device Comparison

表 5-1. Device Comparison

DEVICE	7-BIT I²C ADDRESS	
	HEX	BINARY
TMP4718ADGKR	0x4C	1001100'b
TMP4718BDGKR	0x4D	1001101'b

6 Pin Configuration and Functions

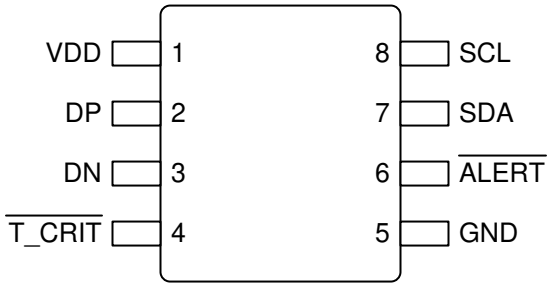

図 6-1. DGK Package 8-Pin VSSOP (Top View)

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	DGK		
VDD	1	P	Supply Pin. Bypass to GND with a 0.1-µF capacitor.
DP	2	I/O	Positive connection to remote temperature sensors. Connect DP to DN if no remote diode is used. Place a 470-pF capacitor between DP and DN for noise filtering (if needed).
DN	3	I/O	Negative connection to remote temperature sensor. Connect DP to DN if no remote diode is used. Place a 470-pF capacitor between DP and DN for noise filtering (if needed).
$\overline{\text{T_CRIT}}$	4	I/O	Open-drain critical temperature alert pin. A pullup resistor to VDD (or a separate bus) is required. The pullup resistor value is used to configure the default $\overline{\text{T_CRIT}}$ and $\overline{\text{ALERT}}$ high-temperature limits for the Remote and Local channels. See *Adjustable Default $\overline{\text{T_CRIT}}$ High-Temperature Limit* for more information.
GND	5	G	Ground connection
$\overline{\text{ALERT}}$	6	I/O	Open-drain temperature alert pin. A pullup resistor to VDD (or a separate bus) is required. The pullup resistor value is used to configure the default $\overline{\text{T_CRIT}}$ and $\overline{\text{ALERT}}$ high-temperature limits for the Remote and Local channels. See *Adjustable Default $\overline{\text{T_CRIT}}$ High-Temperature Limit* for more information.
SDA	7	I/O	Open-drain serial data line. Requires a pullup resistor.
SCL	8	I	Open-drain serial clock Input line. Note I²C clock stretching is not supported.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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7 Specifications

7.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	6	V
I/O voltage	DP	–0.3	1.65	V
	DN	–0.3	0.3	V
	$\overline{\text{ALERT}}$, $\overline{\text{T_CRIT}}$, SCL, SDA	–0.3	6	V
I/O current	$\overline{\text{ALERT}}$, $\overline{\text{T_CRIT}}$, SDA	–10	10	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.62	3.3	5.5	V
$V_{I/O}$	DP	0		1.2	
	DN	0		0	
	$\overline{\text{ALERT}}$, $\overline{\text{T_CRIT}}$, SCL, SDA	0		5.5	
$I_{I/O}$	$\overline{\text{ALERT}}$, $\overline{\text{T_CRIT}}$, SDA			3	mA
T_A	Operating ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TMP4718 DGK (VSSOP) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	107.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	105.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note, SPRA953.

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7.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR_L}	Local temperature accuracy	T_A = –40°C to 125°C		–1		1	°C
T_{ERR_R}	Remote temperature accuracy (Optimized for MMBT3904 NPN Transistor)	T_D = –10°C to 85°C, T_A = –10°C to 85°C		–0.8		0.8	°C
		T_D = –55°C to 125°C	T_A = –10°C to 85°C	–1.0		1.0	°C
			T_A = –40°C to 125°C	–1.5		1.5	°C
PSR	Supply Sensitivity on accuracy	Remote temperature sensor, one-shot mode, V_{DD} = 1.62 V to 5.5 V			0.1		°C/V
T_{RES_L}	Temperature resolution (local)	Including sign bit			8		Bits
		LSB			1		°C
T_{RES_R}	Temperature resolution (remote)	Including sign bit			11		Bits
		LSB			0.125		°C
T_{REPEAT}	Repeatability[1]	V_{DD} = 3.3 V,1-Hz conversion cycle, no averaging			1		LSB
t_{RT}	Response time (Stirred Liquid, mounted on 2-layer 62-mil PCB)	τ = 63% 25°C to 75°C	Local temperature sensor		1.5		s
		τ = 63% 25°C to75 °C	Remote temperature sensor (MMBT3904 NPN Transistor)		0.5		s
V_{FMAX}	Maximum supported forward diode voltage					1.1	V
R_{SERIES}	Maximum supported series resistance on remote channel					1000	Ω
t_{CONV}	Conversion time	Local conversion only, one-shot mode		16	17.7	19.4	ms
		Remote conversion + local conversion, one-shot mode		32	34.3	37	ms
t_{VAR}	Timing variation	Conversion period		–10		10	%
DIGITAL INPUT/OUTPUT							
C_{IN}	Input capacitance	$\overline{ALERT}$, $\overline{T_CRIT}$, SCL, SDA	f = 100 kHz		5		pF
$C_{I/O}$	$\overline{ALERT}$ and $\overline{T_CRIT}$ pin capacitance for resistor detection					1	nF
R_{TOL}	$\overline{ALERT}$ and $\overline{T_CRIT}$ pullup resistor tolerance requirement			–1		1	%
V_{IH}	Input logic high level	SCL, SDA		0.9			V
V_{IL}	Input logic low level	SCL, SDA				0.4	V
I_{LI}	Input leakage current	$\overline{ALERT}$, $\overline{T_CRIT}$, SCL, SDA		–0.1		0.1	µA
I_{LO}	Output leakage current	$\overline{ALERT}$, $\overline{T_CRIT}$, SDA		–0.1		0.1	µA
V_{OL}	Output low level	$\overline{ALERT}$, $\overline{T_CRIT}$, SDA, I_{OL} = 3 mA				0.4	V
POWER SUPPLY							
I_{DD_ACTIVE}	Active conversion current	T_A = –40°C to 125°C Serial bus inactive	Local sensor		100	150	µA
			Remote sensor		220	320	µA
I_{DD_AVG}	Average current consumption	Serial bus inactive, continuous conversion	Conversion period = 2 s		4.5		µA
			Conversion period = 0.125 s		45		µA
I_{DD_SB}	Standby current[2]	Serial bus inactive	T_A = 25°C		1	1.5	µA
			T_A = –40°C to 125°C			5.5	µA

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Over free-air temperature range and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD_SD}	Shutdown current	Serial bus inactive	T_A = 25°C		0.5	0.8	µA
			T_A = –40°C to 125°C			5	µA
		Serial bus active. fs = 400 kHz			6.9		µA
		Serial bus active. fs = 1 MHz			15.2		µA
V_{POR}	Power-on reset threshold voltage	Supply rising			1.2	1.4	V
	Brownout detect	Supply falling		1.0	1.1		V
t_{POR}	Device initialization time(3)					35	ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Quiescent current between conversions in continuous conversion mode
(3) Refer to *Device Initialization, Resistor Decoding, and Default Temperature Conversion* for additional details

7.6 I²C Interface Timing

minimum and maximum specifications are over –40 °C to 125 °C and V_{DD} = 1.62 V to 5.5 V (unless otherwise noted)(1)

		STANDARD MODE		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency(2)	1	100	1	400	1	1000	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	4.7	–	1.3	–	0.5	–	µs
$t_{(SUSTA)}$	Repeated START condition setup time	4.7	–	0.6	–	0.26	–	µs
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	4.0	–	0.6	–	0.26	–	µs
$t_{(SUSTO)}$	STOP condition setup time	4.0	–	0.6	–	0.26	–	µs
$t_{(HDDAT)}$	Data hold time(3)	0	3450	0	900	0	150	ns
$t_{(SUDAT)}$	Data setup time	250	–	100	–	50	–	ns
$t_{(LOW)}$	SCL clock low period	4.7	–	1.3	–	0.5	–	µs
$t_{(HIGH)}$	SCL clock high period	4.0	–	0.6	–	0.26	–	µs
$t_{(VDAT)}$	Data valid time (data response time)(4)	–	3.45		0.9	–	0.45	µs
t_R	Clock and data rise time	–	1000	20	300	–	120	ns
t_F	Clock and fall time	–	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V)	120	ns
$t_{timeout}$	Timeout (SCL = GND)	20	30	20	30	20	30	ms

(1) The controller and target have the same I/O supply value. Values are based on statistical analysis of samples tested during initial release.
(2) The TMP4718 is equipped with a 50-ns spike filter on both SCL and SDA lines. The filter allows the device to be used alongside I3C devices without impacting the communcation.
(3) The maximum $t_{(HDDAT)}$ can be 3.45 µs and 0.9 µs for Standard Mode and Fast Mode, but must be less than the maximum of $t_{(VDAT)}$ by a transition time.
(4) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

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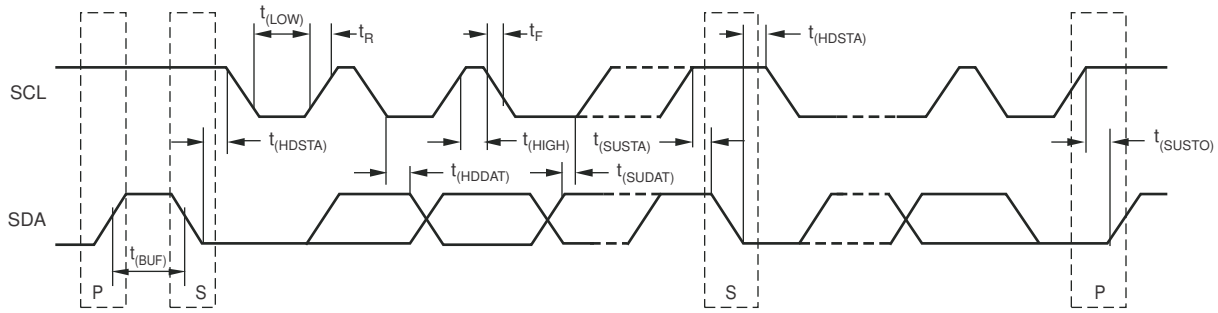

図 7-1. Two-Wire Timing Diagram

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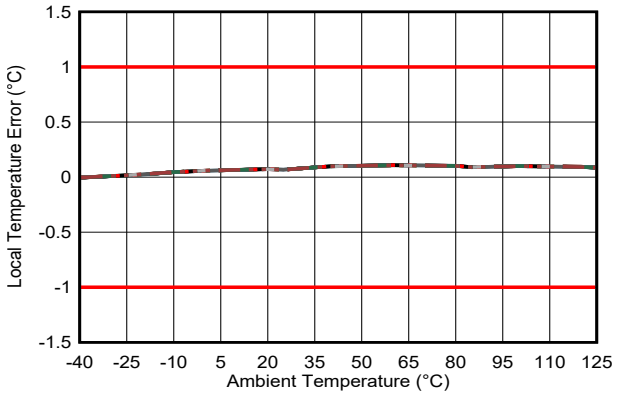
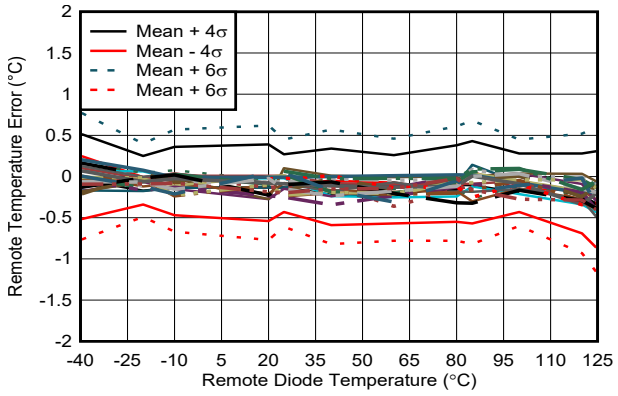
7.8 Typical Characteristics

at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)



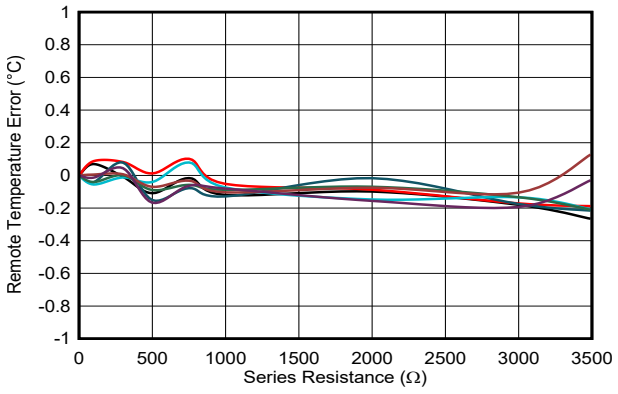
V_{DD} = 1.62 V to 5.5 V

図 7-2. Local Temperature Error vs Temperature



Characterized with MMBT3904 NPN Transistor; T_A = 25°C; 30 units

図 7-3. Remote Temperature Error vs Temperature



Characterized with MMBT3904 NPN Transistor; 7 units

図 7-4. Remote Temperature Error vs Series Resistance

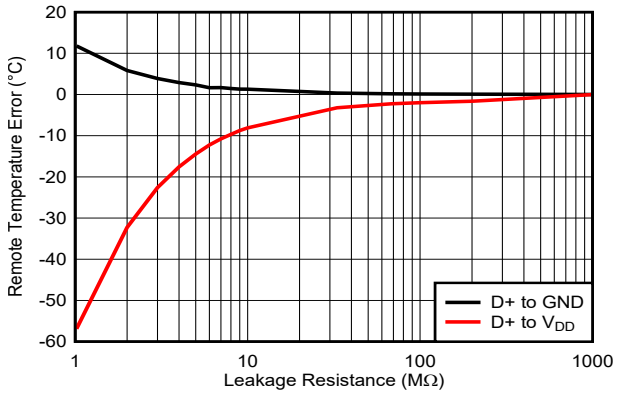
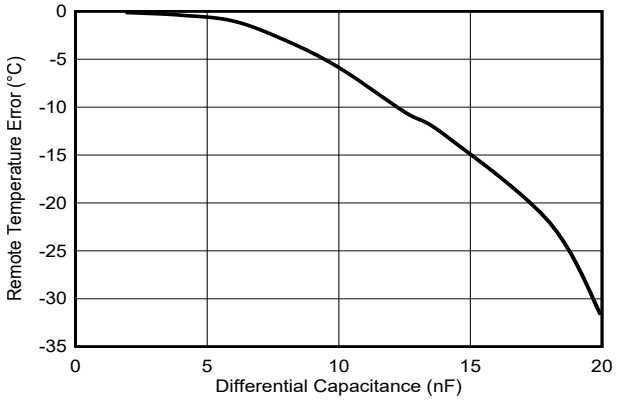
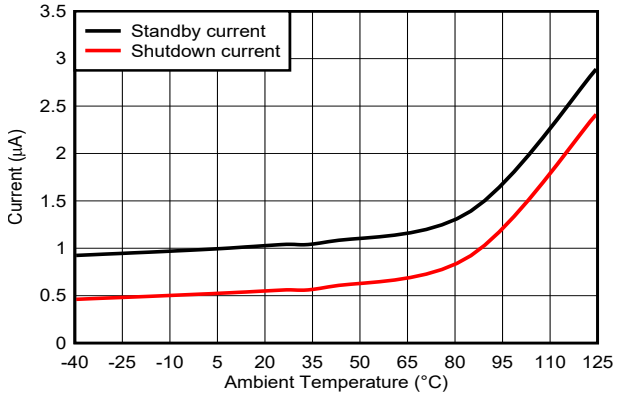


図 7-5. Remote Temperature Error vs Diode Parallel Leakage Resistance



Characterized with MMBT3904 NPN Transistor

図 7-6. Remote Temperature Error vs Differential Capacitance



V_{DD} = 3.3 V

図 7-7. Standby and Shutdown Current vs Temperature

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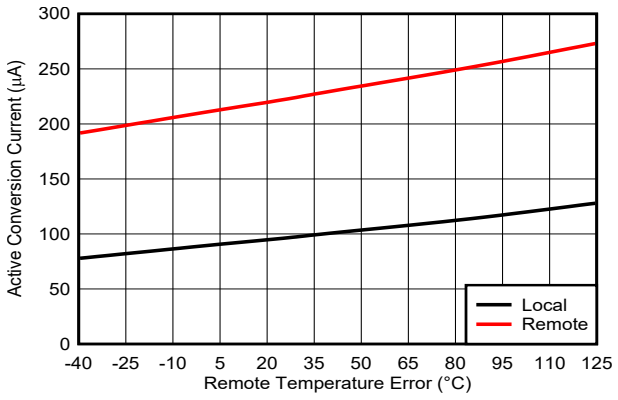
7.8 Typical Characteristics (continued)

at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)



V_{DD} = 3.3 V

図 7-8. Active Current vs Temperature

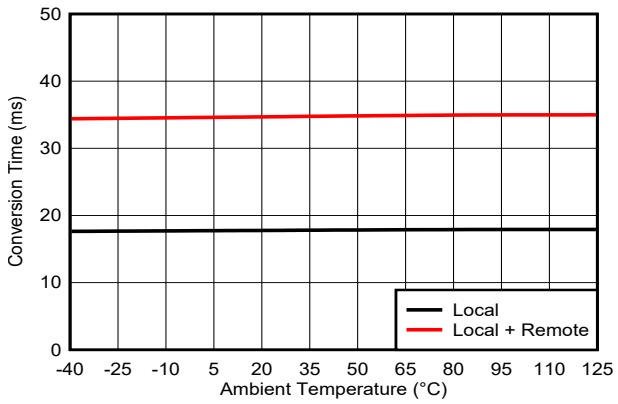
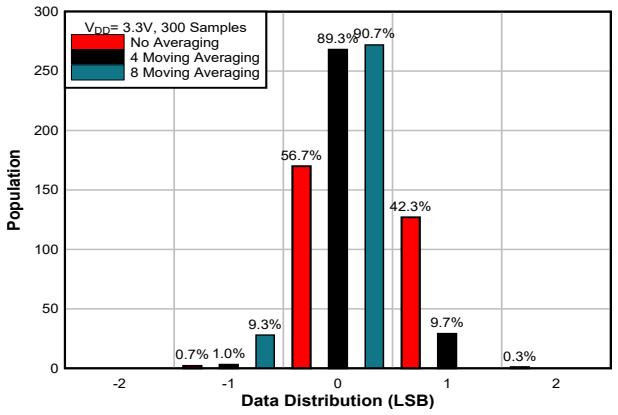
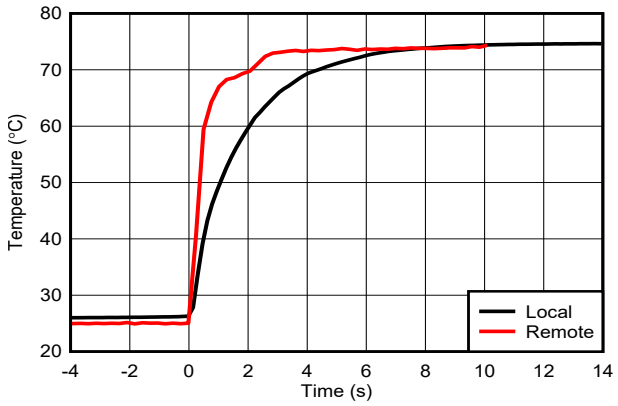


図 7-9. Conversion Time vs Temperature



Characterized with MMBT3904 NPN Transistor

図 7-10. Remote Temperature Noise Data Distribution (300 Samples)



Local: soldered devices on 62mil 2-layer FR4 PCB

Remote: characterized with MMBT3904 NPN Transistor

図 7-11. Response Time (Stirred Liquid)

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8 Detailed Description

8.1 Overview

The TMP4718 is a digital temperature sensor that combines a local temperature measurement channel and a remote-junction temperature measurement channel in a single 8-pin package. The device is I^2C and SMBus compatible and is specified over a temperature range of −40°C to 125°C. The TMP4718 includes series resistance cancellation, programmable temperature alerts, and the ability to change the default power-up $\overline{T_CRIT}$ high-temperature limits through the $\overline{T_CRIT}$ and $\overline{ALERT}$ pullup resistors.

8.2 Functional Block Diagram

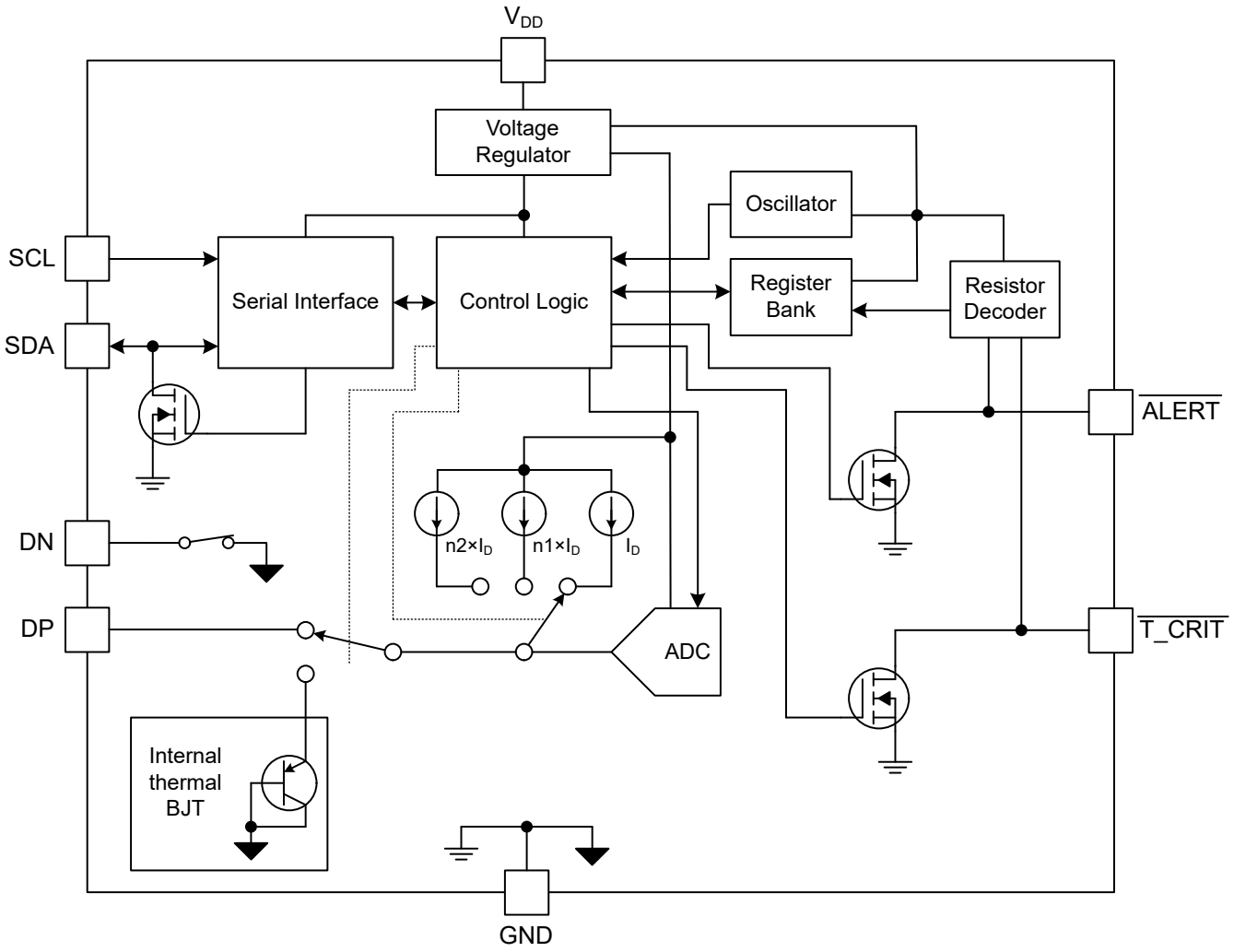


図 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 1.2-V Logic Compatible Inputs

The device includes static input thresholds independent of supply to maintain compatibility with a 1.2-V logic I^2C or SMBus. This removes the need for a translator when operating with a bus voltage different from the supply voltage of the device.

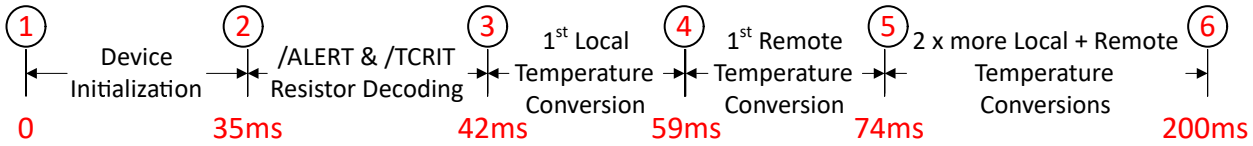
8.3.2 Series Resistance Cancellation

Series resistance cancellation automatically eliminates the temperature error caused by the resistance of the routing to the remote transistor or by the resistors of the optional external low-pass filter. A total of up to 1 kΩ of series resistance can be canceled by the device, thus eliminating the need for additional characterization and temperature offset correction.

8.3.3 Device Initialization, Resistor Decoding, and Default Temperature Conversion

When V_{DD} goes above V_{POR} (power-on reset threshold), the device initiates the power-on reset (POR) sequence and starts loading default configuration settings into the device from the memory. After the device initialization is complete, the device starts the ALERT and T_CRIT pin resistors decoding sequence and loads the $\overline{\text{T_CRIT}}$ high temperature limit decoded into the device. The device then starts default local and remote temperature conversion. The converted result and corresponding output ($\overline{\text{ALERT}}$ or $\overline{\text{T_CRIT}}$) is asserted if the corresponding limit is crossed.

The device initialization, resistor decoding, and default conversion takes approximately 200 ms. During device initialization, the supply voltage V_{DD} shall be hold stable and above V_{POR} (falling) to avoid any device misbehavior. During resistor decoding, the resistor pullup voltage shall also be kept stable to prevent wrong threshold from getting decoded. 図 8-2 depicts the details timing sequence for the device initialization and default temperature conversion.



1. V_{DD} > V_{POR}. Device initialization started.
2. Device initialization completed and power supply stablized. /ALERT and /TCRIT pin resistor decoding started.
3. Resistor decoding completed. Default T_CRIT high-temperature limit loaded into device.
4. 1st Local temperature conversion completed and result available in registers. ALERT and T_CRIT output asserted if local temperature limit crossed.
5. 1st Remote temperature conversion completed and result available in registers. ALERT and T_CRIT output asserted if remote temperature limit crossed.
6. A total of 3 times (default fault queue setting) of Local + Remote temperature conversions completed and result available in registers. ALERT and T_CRIT output asserted if limit crossed.

図 8-2. Device Initialization, Resistor Decoding, and Default Temperature Conversion Timing

8.3.4 Adjustable Default $\overline{\text{T_CRIT}}$ High-Temperature Limit

The default Remote and Local $\overline{\text{T_CRIT}}$ high-temperature limits are adjustable with the use of pullup resistors on the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins. The values of the resistors are decoded within the first 50 ms after device power-up, after which the device sets the Remote and Local $\overline{\text{T_CRIT}}$ high-temperature limits. 表 8-1 shows the values of each limit. Note the following rules when choosing the resistors:

1. The value of the pullup resistors must be within 1% of the nominal value specified in the table below for proper decoding.

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2. If no pullup resistor is connected, the decoded resistance value is the highest resistance value from the table (that is, 18.7 kΩ).
3. If the pin is grounded, the decoded resistance value is the lowest resistance value from the table (that is, 2 kΩ).
4. The $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins can share the same pullup resistor, resulting one of the five $\overline{\text{T_CRIT}}$ limits (77°C, 89°C, 101°C, 113°C or 125°C) to be stored in the device.
5. The resistor decoding scheme functions regardless of the pullup voltage on the pins.
6. The decoded threshold value can be overwritten by writing desired values into the THigh_Crit_Remote and THigh_Crit_Local registers.

表 8-1. $\overline{\text{T_CRIT}}$ High-Temperature Limits

$\overline{\text{T_CRIT}}$ LIMIT (°C)		$\overline{\text{T_CRIT}}$ PIN PULLUP RESISTOR VALUE				
		<2 kΩ	7.5 kΩ	10.5 kΩ	14 kΩ	>18.7 kΩ
$\overline{\text{ALERT}}$ pin pullup resistor value	<2 kΩ	77°C	87°C	97°C	107°C	117°C
	7.5 kΩ	79°C	89°C	99°C	109°C	119°C
	10.5 kΩ	81°C	91°C	101°C	111°C	121°C
	14 kΩ	83°C	93°C	103°C	113°C	123°C
	>18.7 kΩ	85°C	95°C	105°C	115°C	125°C

8.3.5 $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ Output

The TMP4718 $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins are active-low open drain outputs. The $\overline{\text{ALERT}}$ pin is asserted at the end of a conversion cycle when the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit. The $\overline{\text{T_CRIT}}$ pin is asserted at the end of a conversion cycle when the measured temperature exceeds the T_CRIT limit defined in the limit register. The $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins can be used to notify the system of overtemperature or undertemperature conditions and protect from thermally induced system damages. Note the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ outputs are activated only when the corresponding bits are configured in the Alert_Mask register.

8.3.6 Fault Queue

The device includes a fault queue feature. When enable in the register settings, the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ will only be generated if there are three consecutive temperature conversion results beyond the limits. When this feature is disabled, only one temperature conversion result beyond the limits will generate an $\overline{\text{ALERT}}$ or $\overline{\text{T_CRIT}}$ warning.

This feature only applies to the remote channel and will have no effect on the local channel. The fault queue is enabled upon device POR (that is, three successive temperature results beyond the limits triggers an ALERT or T_CRIT warning).

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8.3.7 Filtering

Remote junction temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals that can corrupt measurements. A digital filter is available for the remote temperature measurements to reduce the effect of noise. This filter is programmable and has two levels when enabled. Level 1 performs a moving average of four consecutive samples. Level 2 performs a moving average of eight consecutive samples. The output of the digital filter is stored in the remote temperature result register, and the temperature limits are compared to this value. The filter responses to impulse and step inputs are shown in 図 8-3 and 図 8-4, respectively. The filter can be enabled or disabled by programming the desired levels in register settings. The digital filter is disabled by default.

The averages are cleared after the filter is set to 00h. Filtering can be used with both continuous conversions or one-shot conversions.

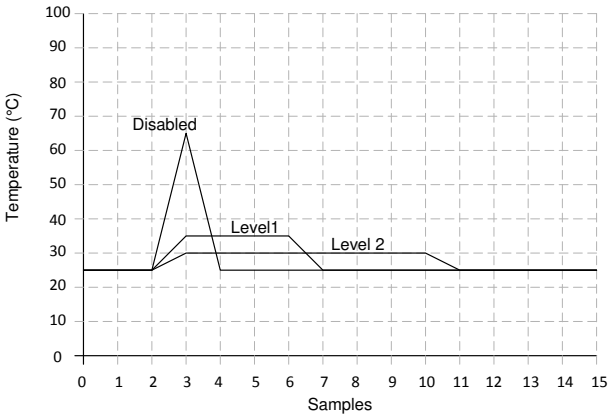

図 8-3. Filter Response to Impulse Inputs

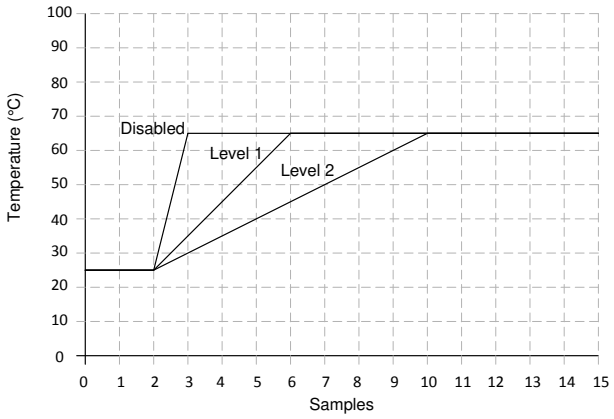

図 8-4. Filter Response to Step Inputs

In addition to the built-in digital filter of the device, TI recommends the user add an external capacitor between DP and DN pin on the remote channel. The capacitor acts as a bypass filter to help reduce high-frequency EMI noise when the device is operating in a noisy environment. The recommended optimal value for the capacitor is 470 pF and the value should not exceed 3 nF to allow proper operation of the temperature sensor.

8.3.8 One-Shot Conversions

Users can write any data to the one-shot register to trigger a manual single one-shot conversion. This allows for greater control of the device and flexibility of system implementation. This feature is only available in shutdown mode and writes to the one-shot register will have no effect in continuous conversion mode. For best performance in one shot mode, TI recommends to have the communication bus idle during temperature conversion (within t_{CONV} after a conversion is triggered).

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8.4 Device Functional Modes

The device can be configured to operate in different modes of operation through the configuration register or the filter and alert mode register.

8.4.1 Interrupt and Comparator Mode

The $\overline{\text{ALERT}}$ pin of the device can be programmed into two different $\overline{\text{ALERT}}$ output modes. In the interrupt mode, the device will assert the $\overline{\text{ALERT}}$ pin if the temperature exceeds the limits set by the temperature limit registers. After the Alert Status is read and interrupt bits cleared, the $\overline{\text{ALERT}}$ pin is deasserted. In Comparator Mode, the device will assert the $\overline{\text{ALERT}}$ pin if the measured temperature exceeds the limits and clear when the temperature returns below the limits.

8.4.1.1 Interrupt Mode

When bit 0 of the Remote Diode Temperature Filter and Alert Mode Setting register is set to 0, the Alert Mode is set to Interrupt mode. In this mode, the $\overline{\text{ALERT}}$ pin is asserted at the end of a conversion cycle if the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit defined in the limit registers. In this mode, the TMP4718 will set the $\overline{\text{ALERT}}$ mask bit of the Configuration Register during a read of the Status Register if any flag in Status Register, except the ADC_Busy flag and Remote Diode Open flag, is set. This prevents the $\overline{\text{ALERT}}$ pin from triggering until the controller has reset the ALERT mask bit (write 0 to Alert_MSK bit).

The ALERT High Status flags will set at the end of a conversion cycle when the measured temperature exceeds a High Alert Limit register limit. There are separate High Limit values and status register flags for the remote and local temperature measurements. The status register flags will only set to their respective temperature measurements.

The Remote $\overline{\text{ALERT}}$ Low Status flag will set at the end of a conversion cycle when the measured remote temperature is below the Remote Low Alert Limit register limit.

The Status Register limit flags are cleared after a read command of the Status Register from the controller and will be set again at the end of a proceeding temperature conversion cycle if the measured temperature is outside the set limits.

図 8-5 shows the behavior of the ALERT pin and flags while in Interrupt mode.

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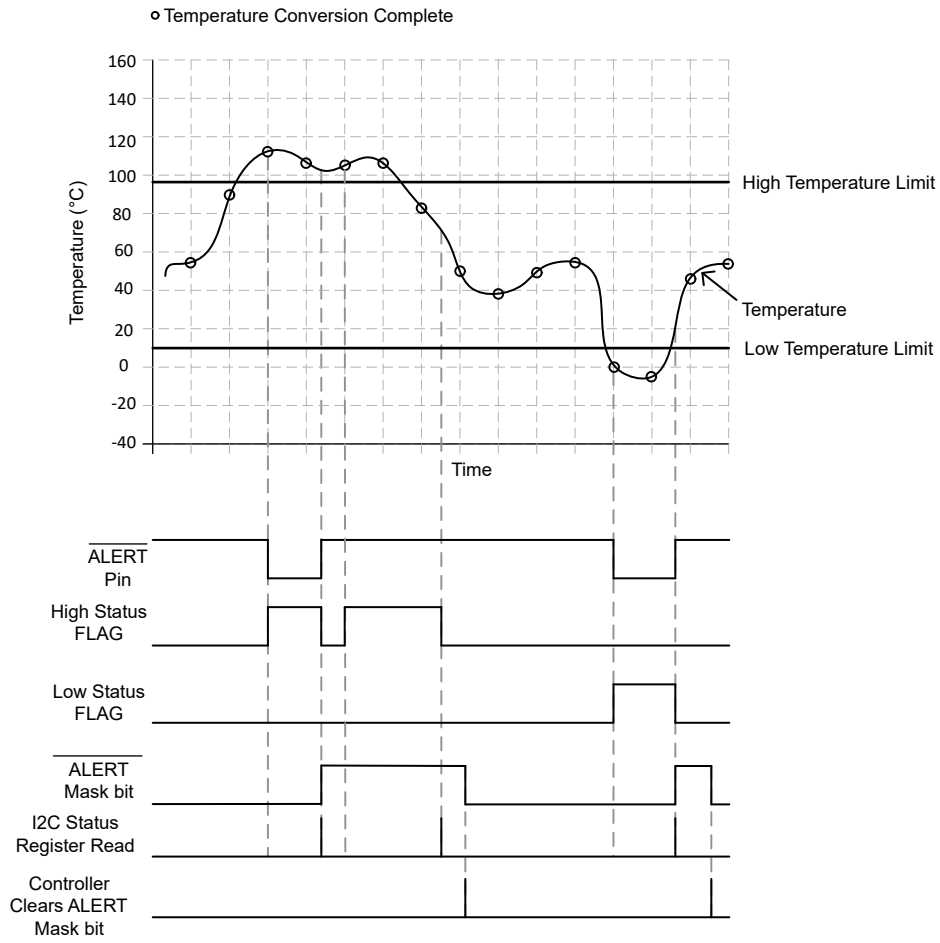

図 8-5. Alert Interrupt Mode Timing Diagram

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8.4.1.2 Comparator Mode

When bit 0 of the Remote Diode Temperature Filter and Alert Mode Setting register is set to 1, the Alert Mode is set to Comparator mode. In this mode, the $\overline{\text{ALERT}}$ pin is asserted at the end of a conversion cycle if the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit defined in the limit registers. The $\overline{\text{ALERT}}$ pin deasserts at the end of proceeding conversion cycle if the measured temperature is equal to or below a High Alert limit and equal to or above a Low Alert limit defined in the limit registers.

The $\overline{\text{ALERT}}$ High Status flags will set at the end of a conversion cycle when the measured temperature exceeds a High Alert Limit register limit and clear at the end of a conversion cycle when the measured temperature is equal to or below the High Limit value. There are separate High Limit values and status register flags for the remote and local temperature measurements. The status register flags will only set or clear to the respective temperature measurements.

The Remote $\overline{\text{ALERT}}$ Low Status flag will set at the end of a conversion cycle when the measured temperature is below the Remote Low Alert Limit register limit and will clear at the end of a conversion cycle when the measured remote temperature is equal to or above the low Limit value.

図 8-6 shows the behavior of the $\overline{\text{ALERT}}$ pin and flags while in Comparator mode.

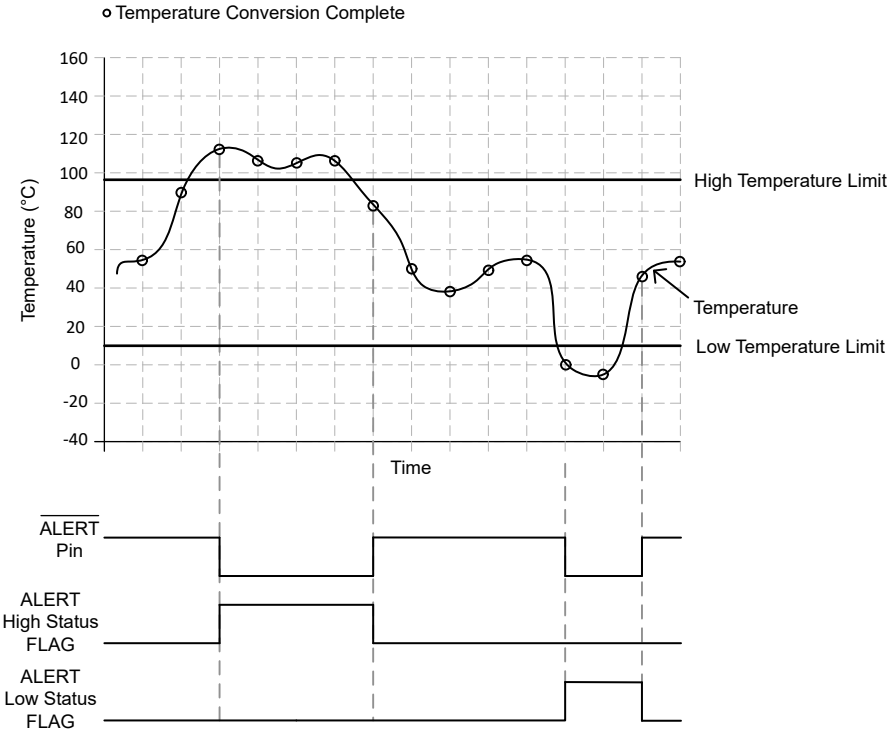

図 8-6. Alert Comparator Mode Timing Diagram

8.4.1.3 $\overline{\text{T_CRIT}}$ Output

The TMP4718 $\overline{\text{T_CRIT}}$ pin is an active-low, open-drain output which is asserted at the end of a conversion cycle when the measured temperature exceeds a $\overline{\text{T_CRIT}}$ Limit defined in the $\overline{\text{T_CRIT}}$ limit registers. The $\overline{\text{T_CRIT}}$ pin deasserts at the end of a conversion cycle if the temperature measurement is less than the $\overline{\text{T_CRIT}}$ limit – $\overline{\text{T_CRIT}}$ Hysteresis. The $\overline{\text{T_CRIT}}$ Hysteresis is set in the $\overline{\text{T_CRIT}}$ Hysteresis register. A $\overline{\text{T_CRIT}}$ Status register flag is set at the end of a conversion cycle when the measured temperature exceeds a $\overline{\text{T_CRIT}}$ Limit. When the TMP4718 is set in interrupt mode, the status register flag is cleared by reading the status register. Reading the status register will set the $\overline{\text{ALERT}}$ mask bit of the Configuration Register. The $\overline{\text{ALERT}}$ mask bit does not mask the $\overline{\text{T_CRIT}}$ pin. The status register flag will continue to set after the end of a conversion cycle until the

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temperature measurement is below the $\overline{\text{T_CRIT}}$ limit – $\overline{\text{T_CRIT}}$ Hysteresis value or the device is reset. There are separate $\overline{\text{T_CRIT}}$ Limit values and status register flags for the remote and local temperature measurements.

図 8-7 shows the behavior of the $\overline{\text{T_CRIT}}$ pin and flags in interrupt mode.

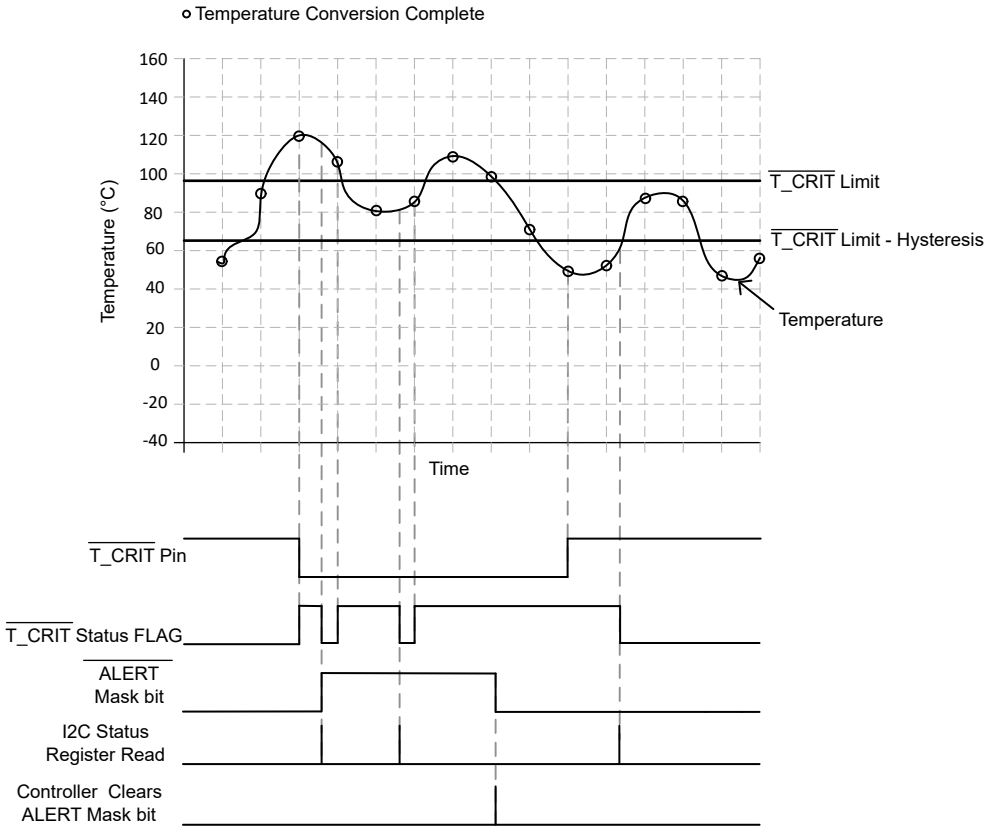

図 8-7. $\overline{\text{T_CRIT}}$ Output Timing Diagram-Interrupt Mode

When the TMP4718 is in comparator the status register flag is only cleared at the end of a conversion cycle if temperature measurement is below the $\overline{\text{T_CRIT}}$ limit – $\overline{\text{T_CRIT}}$ Hysteresis value. The $\overline{\text{ALERT}}$ mask bit does not set after reading the status register in comparator mode. 図 8-8 shows the behavior of the $\overline{\text{T_CRIT}}$ pin and flags in comparator mode.

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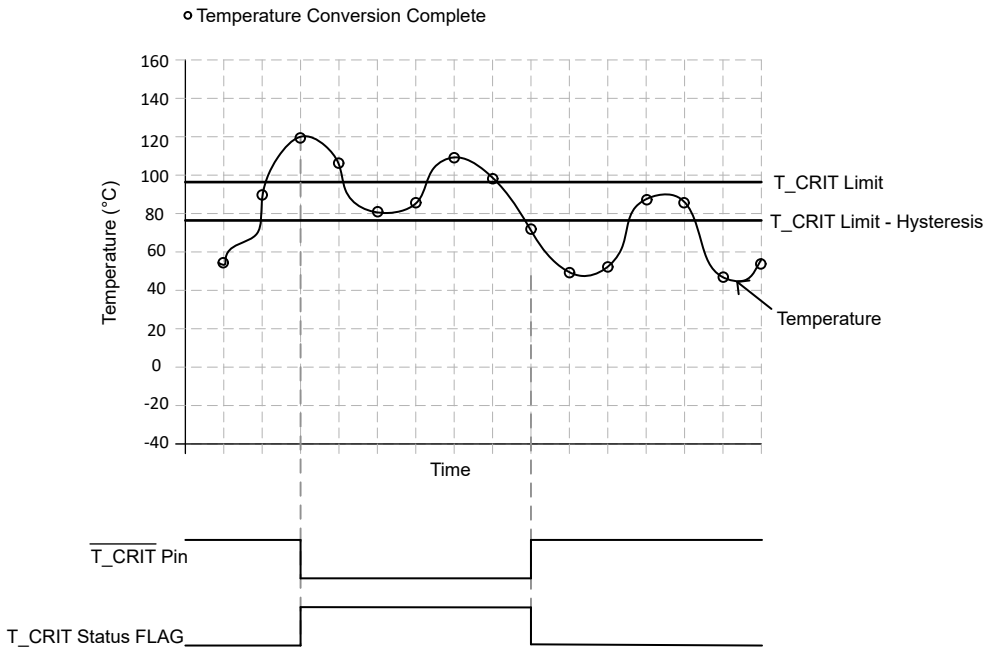

図 8-8. T_CRIT Output Timing Diagram-Comparator Mode

8.4.2 Shutdown Mode

When the Mode bit is set to 1 in the Configuration register, the device immediately enters the low-power shutdown mode. If the device is making a temperature conversion, the device will stop the conversion and discard the partial result. In this mode, the device powers down all active circuitry and can be used in conjunction with the One_Shot bit to perform temperature conversions. Engineers can use the device for battery-operated systems and other low-power consumption applications because the device typically only consumes 0.5 µA in Shutdown Mode.

Entering Shutdown Mode will not clear any active Alerts and will not deassert the ALERTor T_CRIT pins.

8.4.3 Continuous Conversion Mode

When the Mode bit is set to 0 in the Configuration register, the device operates in continuous conversion mode. The device continuously performs temperature conversions in this mode. The device does not wait until the end of the conversion period to update the temperature, instead the temperature result register is updated at the end of the temperature conversion. While the ADC is converting, the ADC_Busy bit is set to 1 in the Alert Status register.

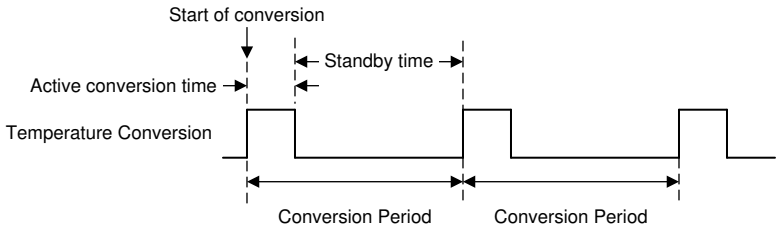

図 8-9. Conversion Period Timing Diagram

8.5 Programming

8.5.1 Temperature Data Format

Local Temperature data is represented by a 8-bit, two's complement word with an LSB (Least Significant Bit) equal to 1°C.

表 8-2. Local Temperature Data Format

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
127°C	0111 1111	7F
25°C	0001 1001	19
2°C	0000 0010	02
1°C	0000 0001	01
0°C	0000 0000	00
−1°C	1111 1110	FE
−2°C	1111 1101	FD
−25°C	1110 0110	E6
−128°C	1000 0000	80

Remote Temperature data is represented by an 11-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.125°C.

表 8-3. Remote Temperature Data Format

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
127.875°C	0111 1111 1110 0000	7FE0
25.750°C	0001 1001 1100 0000	19C0
2.250°C	0000 0010 0100 0000	0240
1.125°C	0000 0001 0010 0000	0120
0°C	0000 0000 0000 0000	0000
−1.125°C	1111 1110 1110 0000	FEE0
−2.250°C	1111 1101 1100 0000	FDC0
−25.750°C	1110 0110 0100 0000	E640
−127.875°C	1000 0000 0010 0000	8020

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8.5.2 I²C and SMBus Interface

The TMP4718 has a standard bidirectional I²C interface that can be configured or read by a controller. Each target on the I²C bus has a specific device address to differentiate between other target devices that are on the same I²C bus. Many target devices require configuration upon start-up to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. The TMP4718 includes 50-ns glitch suppression filters, allowing the device to coexist on I3C mixed bus.

The physical I²C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to a supply through a pullup resistor. The size of the pullup resistor is determined by the amount of capacitance on the I²C lines. See also the *I2C Bus Pullup Resistor Calculation* application note. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition (see 図 8-10 and 図 8-11). See the *Writes* and *Reads* sections for detail procedures on how the controller can access the TMP4718.

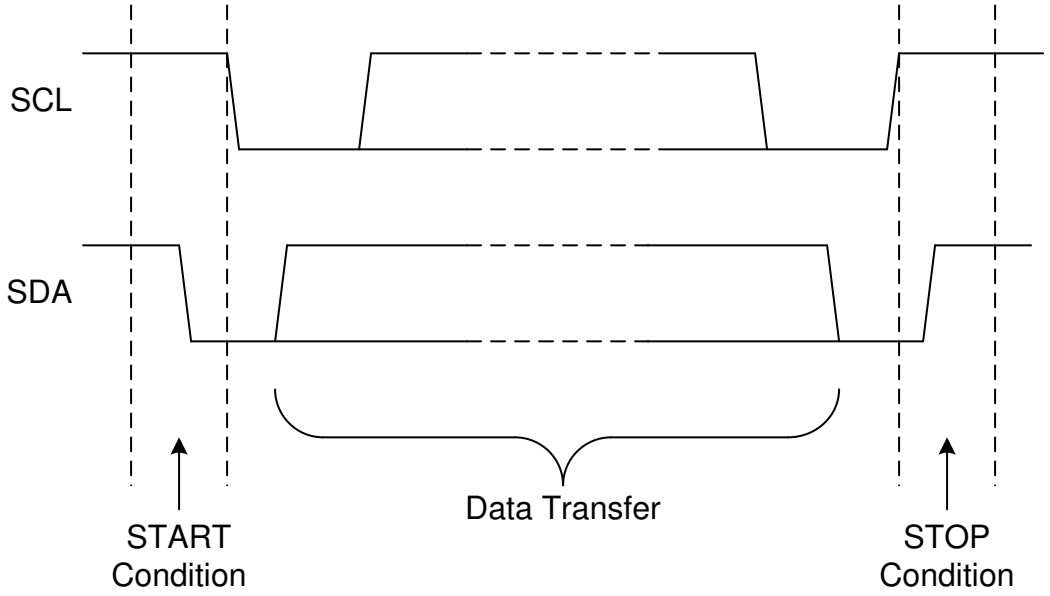

図 8-10. Definition of Start and Stop Conditions

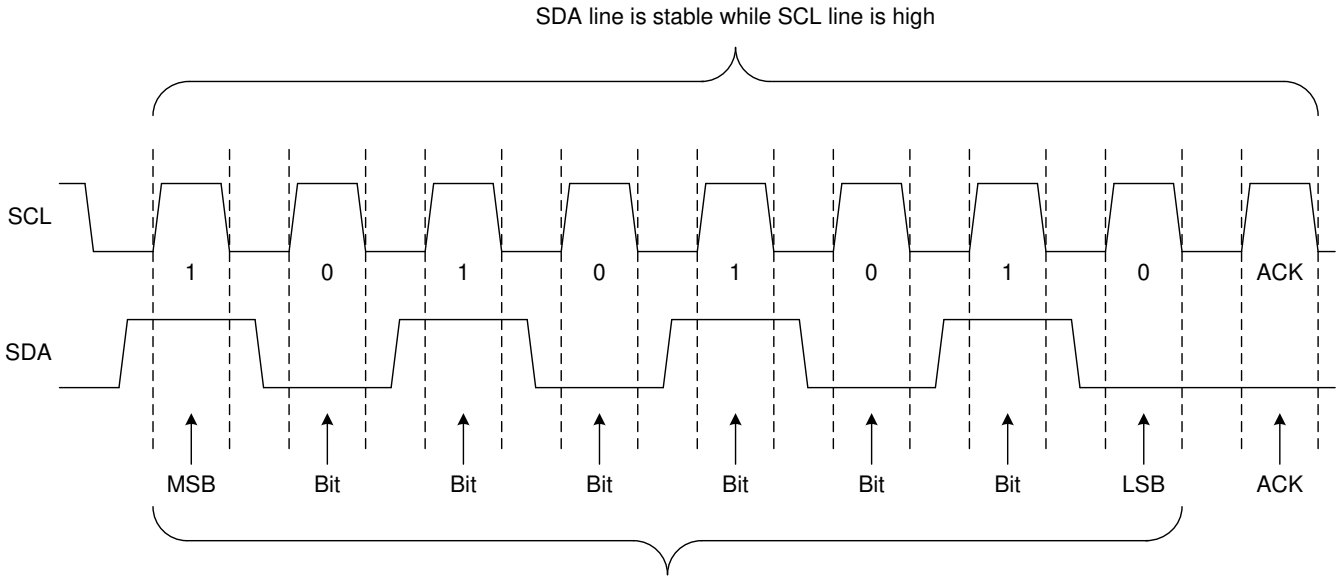

図 8-11. Bit Transfer

8.5.3 Device Address

To communicate with the TMP4718, the controller must first address the target device through an address byte. The address byte has seven address bits and a read-write (R/W) bit that indicates the intent of executing a read or write operation. The TMP4718 offers two different target addresses based on the two different device part numbers shown below.

DEVICE	7-BIT I²C ADDRESS	
	HEX	BINARY
TMP4718ADGKR	0x4C	1001100'b
TMP4718BDGKR	0x4D	1001101'b

8.5.4 Bus Transactions

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

The TMP4718 includes a timeout feature that will automatically reset the I²C state machine after the SCL line is held low for 30 ms. After the timeout the TMP4718 will wait for a new start condition to respond to I_2C communication.

8.5.4.1 Writes

To write on the I²C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/W bit) set to 0, which signifies a write. The target acknowledges, letting the controller know it is ready. After this, the controller starts sending the register pointer followed by the register data to the target. The controller terminates the transmission with a STOP condition.

Writes to read-only registers or register locations outside of the register map will be ignored and the TMP4718 will NACK the data the controller tries to send.

図 8-12 shows an example of writing a single byte write communication. TMP4718 does not support multiple byte writes.

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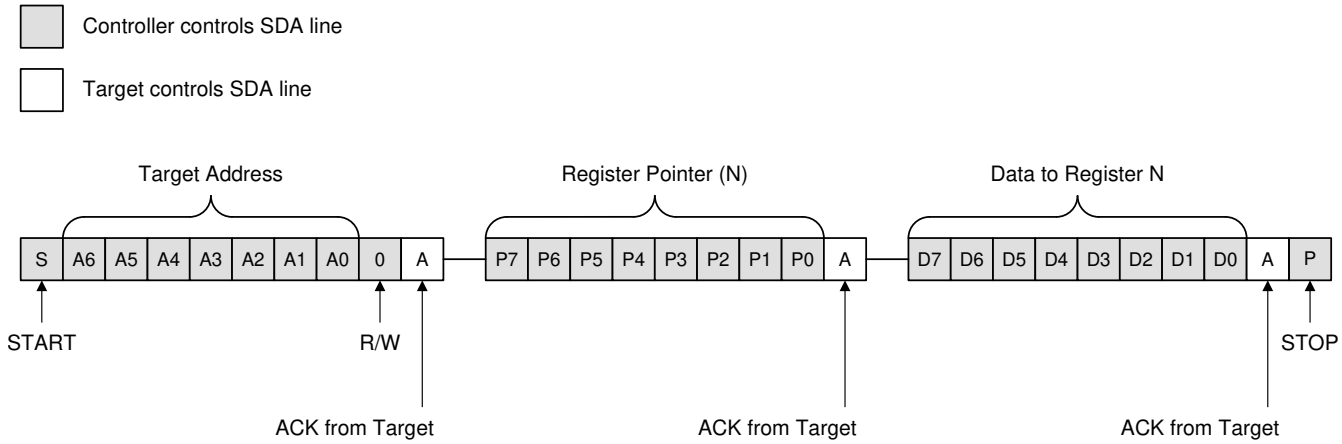

図 8-12. Write to Single Register

8.5.4.2 Reads

For a read operation, the controller sends a START condition followed by the target address with the R/W bit set to 0 (signifying a write). The target acknowledges the write request, and the controller sends the Register Pointer. After the Register Pointer, the host will initiate a restart followed by the target address with the R/W bit set to 1 (signifying a read). The controller will continue to send out clock pulses but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that the controller is ready for more data. 図 8-13 shows an example of reading a single byte from a target register. The TMP4718 does not support multiple register reads with a single transaction.

If repeated reads from the same register are desired, the pointer register bytes do not have to be continually sent, as shown in 図 8-14. The TMP4718 remembers the pointer register value until the value is changed by the next write operation. Note after the device POR, the pointer address is defaulted to 0h. Therefore, the controller can read (and re-read) the Temp_Local register content without setting the pointer value.

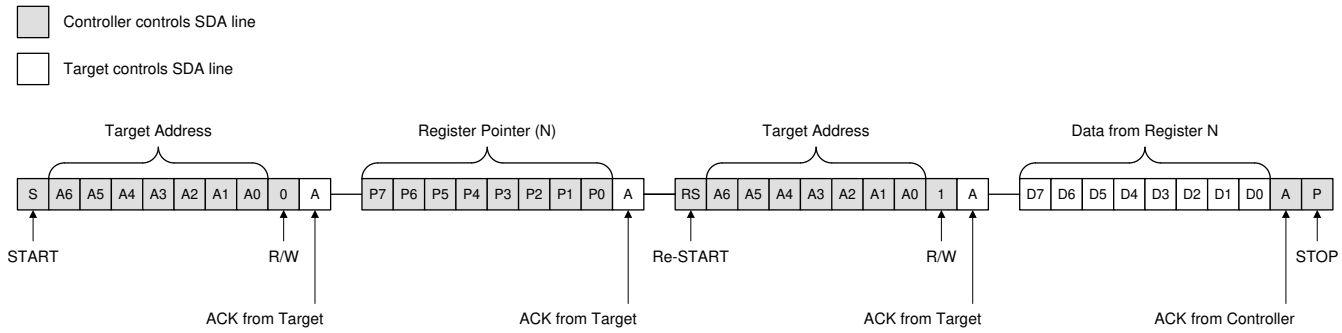

図 8-13. Read from Single Register

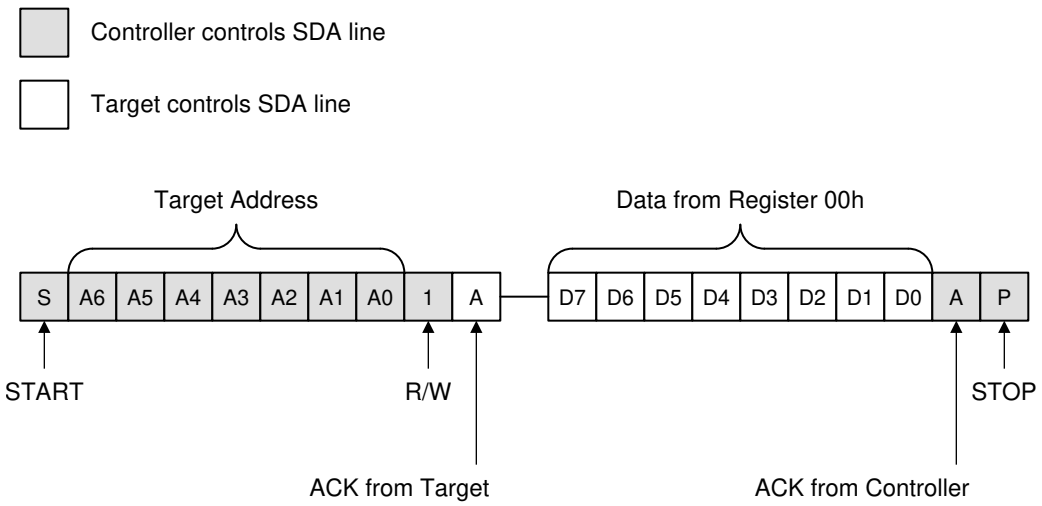

図 8-14. Repeated Read from Single Register

8.5.5 SMBus Alert Mode

When bit 0 of the Filter_Alert_Mode Register is set to 0, the Interrupt/ SMBus Alert mode is enabled. In this mode, the $\overline{\text{ALERT}}$ pin is asserted at the end of a conversion cycle if the measured temperature exceeds a High Alert Limit or goes below a Low Alert Limit defined in the limit registers. In this mode, the TMP4718 sets the $\overline{\text{ALERT}}$ mask bit of the Configuration Register during a read of the Status Register if any flag in Status Register, except the ADC_Busy flag and Remote Diode Open flag, is set. This prevents the $\overline{\text{ALERT}}$ pin from triggering until the controller resets the $\overline{\text{ALERT}}$ mask bit (write 0 to Alert_MSK bit).

The $\overline{\text{ALERT}}$ High Status flags set at the end of a conversion cycle when the measured temperature exceeds a High Alert Limit register limit. There are separate High Limit values and status register flags for the remote and local temperature measurements. The status register flags will only set to their respective temperature measurements.

The Remote $\overline{\text{ALERT}}$ Low Status flag sets at the end of a conversion cycle when the measured remote temperature is below the Remote Low Alert Limit register limit.

The Status Register limit flags are cleared after a read command of the Status Register from the controller and are set again at the end of a proceeding temperature conversion cycle if the measured temperature is outside the set limits.

When the $\overline{\text{ALERT}}$ pin is connected to the SMBus alert line, there can be multiple devices on the same output. For the controller to resolve which target is generating an alert, the controller can send a SMBus ALERT Response Address (ARA) command. If the TMP4718 is generating an alert and an ARA command is sent, the TMP4718 sets the ALERT MASK bit in the Configuration register and send the target address to the controller. An ARA command will not clear any Status register flags.

図 8-15 shows the behavior of the $\overline{\text{ALERT}}$ pin and flags while in SMBus Alert mode.

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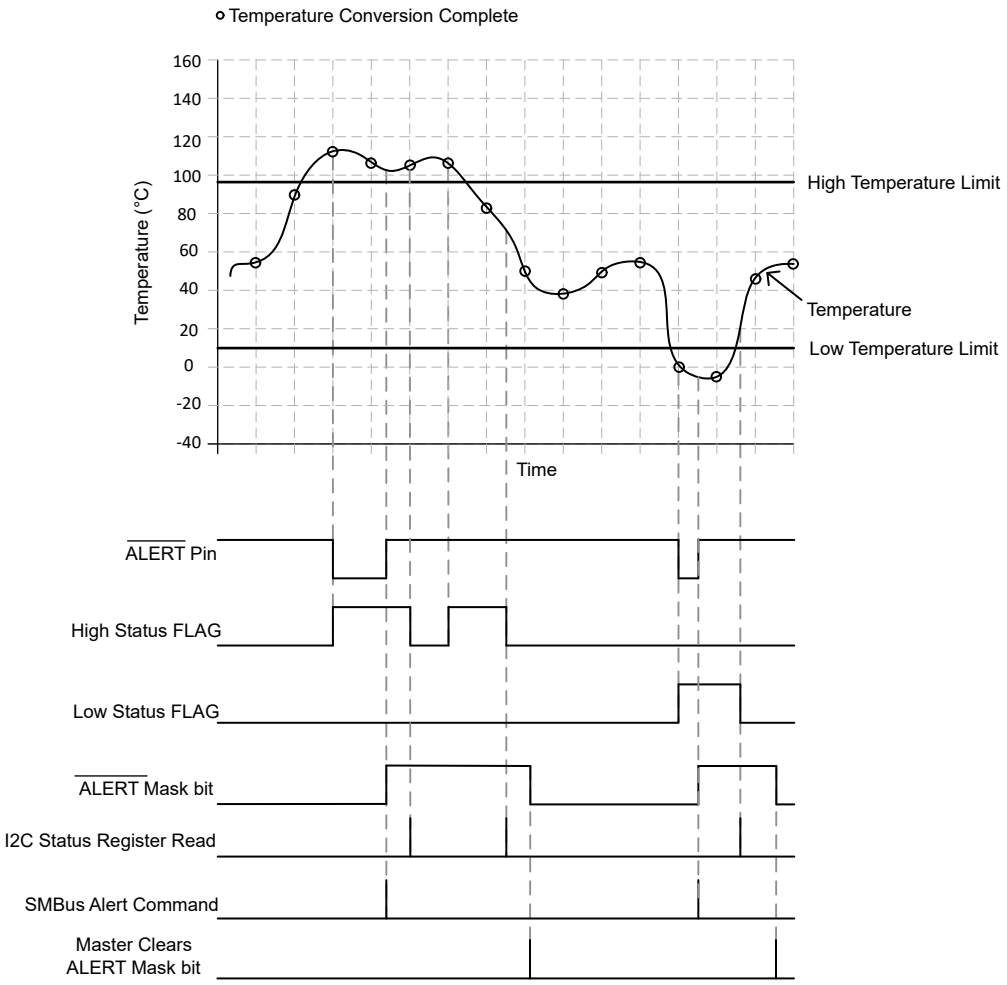

図 8-15. Alert SMBus Mode Timing Diagram

8.6 Register Map

表 8-4. TMP471 Registers

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	00h	Temp_Local	Local temperature register	GO
01h	R	00h	Temp_Remote_MSB	Remote temperature MSB register	GO
02h	R/RC	00h	Alert_Status	Alert status register	GO
03h or 09h	R/W	05h	Configuration	Configuration register	GO
04h or 0Ah	R/W	08h	Conv_Period	Conversion period register	GO
05h or 0Bh	R/W	46h	THigh_Limit_Local	Local high limit register	GO
06h	R	00h	Reserved	Reserved	
07h or 0Dh	R/W	46h	THigh_Limit_Remote_MSB	Remote high limit MSB register	GO
08h or 0Eh	R/W	D8h	TLow_Limit_Remote_MSB	Remote low limit MSB register	GO
0Ch	R	00h	Reserved	Reserved	
0Fh	W	00h	One_Shot	One shot conversion register	GO
10h	R	00h	Temp_Remote_LSB	Remote temperature LSB register	GO
11h	R/W	00h	Remote_Offset_MSB	Remote temperature offset MSB	GO
12h	R/W	00h	Remote_Offset_LSB	Remote temperature offset LSB	GO
13h	R/W	00h	THigh_Limit_Remote_LSB	Remote high limit LSB register	GO
14h	R/W	00h	TLow_Limit_Remote_LSB	Remote low limit LSB register	GO
16h	R/W	07h	Alert_Mask	Alert mask register	GO
19h	R/W	XXh	THigh_Crit_Remote	Remote Crit limit register	GO
20h	R/W	XXh	THigh_Crit_Local	Local Crit limit register	GO
21h	R/W	0Ah	Crit_Hysteresis	Crit hysteresis register	GO
2Dh	R/W	00h	Log1	Data log 1 register	GO
2Eh	R/W	00h	Log2	Data log 2 register	GO
2Fh	R/W	00h	Log3	Data log 3 register	GO
BFh	R/W	00h	Filter_Alert_Mode	Filter and alert mode register	GO
FDh	R	50h	Chip_ID	Chip ID register	GO
FEh	R	60h	Vendor_ID	Vendor ID register	GO
FFh	R	90h	Device_Rev_ID	Device and Revision ID register	GO

表 8-5. TMP471 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.6.1 Temp_Local Register (Address = 00h) [reset = 00h]

This register stores the latest temperature conversion result in a 8-bit two's complement format with a LSB (Least Significant Bit) equal to 1°C.

Return to Register Map.

図 8-16. Temp_Local Register

7	6	5	4	3	2	1	0
Temp_Local[7:0]							
R-00h							

表 8-6. Temp_Local Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Temp_Local[7:0]	R	00h	8-bit local temperature conversion result. Temperature data is represented by a 8-bit, two's complement byte with an LSB (Least Significant Bit) equal to 1°C.

8.6.2 Temp_Remote_MSB Register (Address = 01h) [reset = 00h]

This register stores the latest temperature conversion result Most Significant Byte (MSB) in a 11-bit two's complement format with a least significant bit equal to 0.125°C.

Return to Register Map.

図 8-17. Temp_Remote_MSB Register

7	6	5	4	3	2	1	0
Temp_Remote[10:3]							
R-00h							

表 8-7. Temp_Remote_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Temp_Remote[10:3]	R	0h	11-bit remote temperature channel conversion result Most Significant Byte Temperature data is represented by a 11-bit, two's complement word with a least significant bit equal to 0.125°C.

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8.6.3 Alert_Status Register (Address = 02h) [reset = 00h]

This register shows the current alert status of the device.

Return to Register Map.

図 8-18. Alert_Status Register

7	6	5	4	3	2	1	0
ADC_Busy	THigh_LA	Reserved	THigh_RA	TLow_RA	Remote_DC	TCrit_R	TCrit_L
R-0h	R-0h	Reserved	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-8. Alert_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_Busy	R	0h	Indicates if the ADC is busy in the middle of a conversion 0h = The ADC is idle 1h = The ADC is converting
6	THigh_LA	R	0h	Indicates if the measured local temperature result is higher than the local high limit register setting. 0h = The local temperature is within normal operation 1h = The local temperature exceeds the limit
5	Reserved	R	0h	Reserved
4	THigh_RA	R	0h	Indicates if the measured remote temperature result is higher than the remote high limit register setting. 0h = The remote temperature is within normal operation 1h = The remote temperature exceeds the high alert limit
3	TLow_RA	R	0h	Indicates if the measured remote temperature result is lower than the remote low limit register setting. 0h = The remote temperature is within normal operation 1h = The remote temperature exceeds the low alert limit
2	Remote_DC	R	0h	Indicates if the remote temperature channel is disconnected. This bit does not affect the $\overline{\text{ALERT}}$ or $\overline{\text{T_CRIT}}$ pin. 0h = The remote channel is connected 1h = The remote channel is disconnected
1	TCrit_R	R	0h	Indicates if the measured remote temperature result is above the limit configured in the THigh_Crit_Remote register. 0h = The remote temperature is within normal operation 1h = The remote temperature exceeds the limit
0	TCrit_L	R	0h	Indicates if the measured local temperature result is above the limit configured in the THigh_Crit_Local register. 0h = The local temperature is within normal operation 1h = The local temperature exceeds the limit

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8.6.4 Configuration Register (Address = 03h or 09h) [reset = 05h]

This register is used to configure the operation of the device. Changes to the configuration register will disrupt an on-going conversion (except when configuring the device into Shutdown mode) and will be serviced after completion of the conversion.

Return to Register Map.

図 8-19. Configuration Register

7	6	5	4	3	2	1	0
Alert_Mask	Mode	Reserved			Remote_En	WTC_En	Fault_Q
R/W-0h	R/W-0h	R-0h			R/W-1h	R/W-0h	R/W-1h

表 8-9. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Alert_Mask	R/W	0h	Controls the functionality of the $\overline{\text{ALERT}}$ pin. This bit is set after reading an active alert and must be cleared for the $\overline{\text{ALERT}}$ pin to assert again. 0h = The $\overline{\text{ALERT}}$ pin is enabled 1h = The $\overline{\text{ALERT}}$ is masked and will not output a low
6	Mode	R/W	0h	Controls the operation mode of the device. 0h = Continuous mode enabled 1h = Shutdown mode enabled
5:3	Reserved	R	0h	Reserved
2	Remote_En	R/W	1h	Enables of disables the remote channel operation. 0h = The remote channel monitoring is disabled 1h = The remote channel monitoring is enabled
1	WTC_En	R/W	0h	Enables the override of the previously stored value for the critical temperature limits. 0h = $\overline{\text{T_CRIT}}$ Limit cannot be changed 1h = $\overline{\text{T_CRIT}}$ Limit can be changed
0	Fault_Q	R/W	1h	Configures the fault queue feature for the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins. This only affects the remote channel. 0h = Fault queue is disabled, only 1 temperature result beyond the limits will trigger an $\overline{\text{ALERT}}$ or $\overline{\text{T_CRIT}}$ warning 1h = Fault queue is enabled, three successive temperature results beyond the limits will trigger an $\overline{\text{ALERT}}$ or $\overline{\text{T_CRIT}}$ warning

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8.6.5 Conv_Period Register (Address = 04h or 0Ah) [reset = 08h]

This register is used to configure the conversion period of the device. Setting a reserved configuration will stop conversions but not change the device mode.

Return to Register Map.

図 8-20. Conv_Period Register

7	6	5	4	3	2	1	0
Reserved				Conv_Period[3:0]			
R-0h				R/W-8h			

表 8-10. Conv_Period Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved
3:0	Conv_Period[3:0]	R/W	8h	Conversion period setting. This bit field changes the conversion period of the device at the next possible interval but will not restart an on-going conversion period. Writing an unsupported value to this setting will put the device in Shutdown mode. 0h = 16 s / 0.0625 Hz 1h = 8 s / 0.125Hz 2h = 4 s / 0.25 Hz 3h = 2 s / 0.5 Hz 4h = 1 s / 1 Hz 5h = 0.5 s / 2 Hz 6h = 0.25 s / 4 Hz 7h = 0.125 s / 8 Hz 8h = 0.0625 s / 16 Hz (default) 9h-Fh = Reserved

8.6.6 THigh_Limit_Local Register (Address = 05h or 0Bh) [reset = 46h]

This register is used to configure Local temperature high limit. The default value 46h corresponds to a limit setting of 70°C.

Return to Register Map.

図 8-21. THigh_Limit_Local Register

7	6	5	4	3	2	1	0
THigh_Limit_Local[7:0]							
R/W-46h							

表 8-11. THigh_Limit_Local Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Limit_Local[7:0]	R/W	46h	8-bit local temperature alert high limit setting. Temperature alert high limit format is an 8-bit two's complement byte with a least significant bit equal to 1°C

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8.6.7 THigh_Limit_Remote_MSB Register (Address = 07h or 0Dh) [reset = 46h]

This register is used to configure the high alert limit for the remote channel. The default value 460h corresponds to a limit setting of 70°C.

Return to Register Map.

図 8-22. THigh_Limit_Remote_MSB Register

7	6	5	4	3	2	1	0
THigh_Limit_Remote[10:3]							
R/W-46h							

表 8-12. THigh_Limit_Remote_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Limit_Remote[10:3]	R/W	46h	11-bit remote temperature alert high limit setting. Temperature alert high limit format is an 11-bit two's complement word with a least significant bit equal to 0.0125°C

8.6.8 TLow_Limit_Remote_MSB Register (Address = 08h or 0Eh) [reset = D8h]

This register is used to configure the low alert limit for the remote channel. The default value D8h corresponds to -40°C.

Return to Register Map.

図 8-23. TLow_Limit_Remote_MSB Register

7	6	5	4	3	2	1	0
Tlow_Limit_Remote[10:3]							
R/W-D8h							

表 8-13. TLow_Limit_Remote_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TLow_Limit_Remote[10:3]	R/W	D8h	11-bit remote temperature alert low limit setting. Temperature alert low limit format is an 11-bit two's complement word with a least significant bit equal to 0.0125°C

8.6.9 One_Shot Register (Address = 0Fh) [reset = 00h]

Write to this register to trigger a One Shot conversion in Shutdown Mode (that is, Bit 6 of the Configuration Register written to 1).

Return to Register Map.

図 8-24. One_Shot Register

7	6	5	4	3	2	1	0
One_Shot[7:0]							
W-00h							

表 8-14. One_Shot Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	One_Shot[7:0]	W	00h	Writing any value to this register will trigger a One_Shot conversion while in Shutdown Mode. In continuous mode there will be no effect.

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8.6.10 Temp_Remote_LSB Register (Address = 10h) [reset = 00h]

This register contains bits Temp_Remote[2:0] of the remote temperature result.

Return to Register Map.

図 8-25. Temp_Remote_LSB Register

7	6	5	4	3	2	1	0
Temp_Remote[2:0]			Reserved				
R-0h			R-00h				

表 8-15. Temp_Remote_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Temp_Remote[2:0]	R	0h	11-bit remote temperature channel conversion result Least Significant Byte Temperature data is represented by a 11-bit, two's complement word with a least significant bit equal to 0.125°C.
4:0	Reserved	R	00h	Reserved

8.6.11 Remote_Offset_MSB Register (Address = 11h) [reset = 00h]

This register contains the most significant byte of the remote channel offset. Use this register to input a static offset calibration for remote temperature measurements.

Return to Register Map.

図 8-26. Remote_Offset_MSB Register

7	6	5	4	3	2	1	0
Remote_Offset[10:3]							
R/W-00h							

表 8-16. Remote_Offset_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Remote_Offset[10:3]	R/W	00h	11-bit remote temperature channel remote offset most significant byte Temperature data is represented by a 11-bit, two's complement word with a least significant bit equal to 0.125°C.

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8.6.12 Remote_Offset_LSB Register (Address = 12h) [reset = 00h]

This register contains the least significant byte of the remote channel offset. Use this register to input a static offset calibration for remote temperature measurements.

Return to Register Map.

図 8-27. Remote_Offset_LSB Register

7	6	5	4	3	2	1	0
Remote_Offset[2:0]			Reserved				
R/W-0h			R-00h				

表 8-17. Remote_Offset_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Remote_Offset[2:0]	R/W	0h	11-bit remote temperature channel remote offset least significant byte Temperature data is represented by a 11-bit, two's complement word with a least significant bit equal to 0.125°C.
4:0	Reserved	R	00h	Reserved

8.6.13 THigh_Limit_Remote_LSB Register (Address = 13h) [reset = 00h]

This register is used to configure the high alert limit for the remote channel.

Return to Register Map.

図 8-28. THigh_Limit_Remote_LSB Register

7	6	5	4	3	2	1	0
THigh_Limit_Remote[2:0]			Reserved				
R/W-0h			R-00h				

表 8-18. THigh_Limit_Remote_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	THigh_Limit_Remote[2:0]	R/W	0h	11-bit remote temperature alert high limit setting. Temperature alert high limit format is an 11-bit two's complement word with a least significant bit equal to 0.0125°C
4:0	Reserved	R	00h	Reserved

8.6.14 TLow_Limit_Remote_LSB Register (Address = 14h) [reset = 00h]

This register is used to configure the low alert limit for the remote channel.

Return to Register Map.

図 8-29. TLow_Limit_Remote_LSB Register

7	6	5	4	3	2	1	0
Tlow_Limit_Remote[2:0]			Reserved				
R/W-0h			R-00h				

表 8-19. TLow_Limit_Remote_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TLow_Limit_Remote[2:0]	R/W	0h	11-bit remote temperature alert low limit setting. Temperature alert low limit format is an 11-bit two's complement word with a least significant bit equal to 0.0125°C

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表 8-19. TLow_Limit_Remote_LSB Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4:0	Reserved	R	00h	Reserved

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8.6.15 Alert_Mask Register (Address = 16h) [reset = 07h]

Controls which alerts are masked. Masking an alert prevents the $\overline{\text{ALERT}}$ pin from being asserted low.

Return to Register Map.

図 8-30. Alert_Mask Register

7	6	5	4	3	2	1	0
THigh_LA	Reserved		THigh_RA	TLow_RA	Reserved	TCrit_R	TCrit_L
R/W-0h	R-0h		R/W-0h	R/W-0h	R-1h	R/W-1h	R/W-1h

表 8-20. Alert_Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THigh_LA	R/W	0h	Mask setting for THigh_LA 0h = THigh_LA is enabled to output the $\overline{\text{ALERT}}$ pin 1h = THigh_LA is masked and will not output a low on the $\overline{\text{ALERT}}$ pin
6:5	Reserved	R	0h	Reserved
4	THigh_RA	R/W	0h	Mask setting for THigh_RA 0h = THigh_RA is enabled to output the $\overline{\text{ALERT}}$ pin 1h = THigh_RA is masked and will not output a low on the $\overline{\text{ALERT}}$ pin
3	TLow_RA	R/W	0h	Mask setting for TLow_RA 0h = TLow_RA is enabled to output the $\overline{\text{ALERT}}$ pin 1h = TLow_RA is masked and will not output a low on the $\overline{\text{ALERT}}$ pin
2	Reserved	R	1h	Reserved
1	TCrit_R	R/W	1h	Mask setting for TCrit_R 0h = TCrit_R is enabled to output the $\overline{\text{ALERT}}$ pin 1h = TCrit_R is masked and will not output a low on the $\overline{\text{ALERT}}$ pin
0	TCrit_L	R/W	1h	Mask setting for TCrit_L 0h = TCrit_L is enabled to output the $\overline{\text{ALERT}}$ pin 1h = TCrit_L is masked and will not output a low on the $\overline{\text{ALERT}}$ pin

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8.6.16 THigh_Crit_Remote Register (Address = 19h) [reset = XXh]

This register is used to configure the citical limit for the remote channel. The default value for this register is configured by the pull-up resistors through the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins. Note the WTC_En bit in the Configuration register needs to be set to 1h before writting to this register.

Return to Register Map.

図 8-31. THigh_Crit_Remote Register

7	6	5	4	3	2	1	0
THigh_Crit_Remote[7:0]							
R/W-XXh							

表 8-21. THigh_Crit_Remote Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Crit_Remote[7:0]	R/W	XXh	8-bit remote temperature crit limit setting. Temperature crit limit format is an 8-bit two's complement word with a least significant bit equal to 1°C

8.6.17 THigh_Crit_Local Register (Address = 20h) [reset = XXh]

This register is used to configure the critical limit for the local channel. The default value for this register is configured by the pull-up resistors through the $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins. Note the WTC_En bit in the Configuration register needs to be set to 1h before writing to this register.

Return to Register Map.

図 8-32. THigh_Crit_Local Register

7	6	5	4	3	2	1	0
THigh_Crit_Local[7:0]							
R/W-XXh							

表 8-22. THigh_Crit_Local Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THigh_Crit_Local[7:0]	R/W	XXh	8-bit local temperature crit limit setting. Temperature crit limit format is an 8-bit two's complement word with a least significant bit equal to 1°C

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8.6.18 Crit_Hysteresis Register (Address = 21h) [reset = 0Ah]

This register is used to configure the critical hysteresis for both remote and local channels. The value for this register is a 5-bit integer value with a least significant bit equal to 1°C. Default value is 10°C.

Return to Register Map.

図 8-33. Crit_Hysteresis Register

7	6	5	4	3	2	1	0
Reserved			Crit_Hysteresis[4:0]				
R-0h			R/W-0Ah				

表 8-23. Crit_Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved
4:0	Crit_Hysteresis[4:0]	R/W	0Ah	5-bit temperature critical hysteresis. Temperature crit hysteresis format is an 5-bit integer byte with a least significant bit equal to 1°C

8.6.19 Log1 Register (Address = 2Dh) [reset = 00h]

This register is available as a general purpose log register. This register will have no impact on device operation.

Return to Register Map.

図 8-34. Log1 Register

7	6	5	4	3	2	1	0
Log1[7:0]							
R/W-00h							

表 8-24. Log1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Log1[7:0]	R/W	0h	General purpose data log.

8.6.20 Log2 Register (Address = 2Eh) [reset = 00h]

This register is available as a general purpose log register. This register will have no impact on device operation.

Return to Register Map.

図 8-35. Log2 Register

7	6	5	4	3	2	1	0
Log2[7:0]							
R/W-00h							

表 8-25. Log2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Log2[7:0]	R/W	0h	General purpose data log.

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8.6.21 Log3 Register (Address = 2Fh) [reset = 00h]

This register is available as a general purpose log register. This register will have no impact on device operation.

Return to Register Map.

図 8-36. Log3 Register

7	6	5	4	3	2	1	0
Log3[2:0]							
R/W-00h							

表 8-26. Log3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Log3[7:0]	R/W	0h	General purpose data log.

8.6.22 Filter_Alert_Mode Register (Address = BFh) [reset = 00h]

This register controls the remote diode filter level and the alert mode of operation.

Return to Register Map.

図 8-37. Filter_Alert_Mode Register

7	6	5	4	3	2	1	0
Reserved					Filter_Level[1:0]		Alert_Mode
R-00h					R/W-0h		R/W-0h

表 8-27. Filter_Alert_Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0h	Reserved
2:1	Filter_Level[1:0]	R/W	0h	Controls the filter level. The filter is a moving average of the Remote temperature conversion results. 0h = 0 moving average 1h = 4 moving average 2h = 4 moving average 3h = 8 moving average
0	Alert_Mode	R/W	0h	Controls the $\overline{\text{ALERT}}$ pin mode of operation 0h = Interrupt or SMBus Alert mode 1h = Comparator mode

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8.6.23 Chip_ID Register (Address = FDh) [reset = 50h]

This register contains the Chip ID for identifying the device.

Return to Register Map.

図 8-38. Chip_ID Register

7	6	5	4	3	2	1	0
Chip_ID[7:0]							
R-50h							

表 8-28. Chip_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Chip_ID[7:0]	R	50h	Chip ID of the device.

8.6.24 Vendor_ID Register (Address = FEh) [reset = 60h]

This register contains the Vendor ID for identifying the device.

Return to Register Map.

図 8-39. Vendor_ID Register

7	6	5	4	3	2	1	0
Vendor_ID[7:0]							
R-60h							

表 8-29. Vendor_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Vendor_ID[7:0]	R	60h	Vendor ID of the device.

8.6.25 Device_Rev_ID Register (Address = FFh) [reset = 91h]

This register contains the Device and Revision ID for identifying the device.

Return to Register Map.

図 8-40. Device_Rev_ID Register

7	6	5	4	3	2	1	0
Device_ID[3:0]				Rev_ID[3:0]			
R-9h				R-0h			

表 8-30. Device_Rev_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Device_ID[3:0]	R	9h	Device ID of the device.
3:0	Rev_ID[3:0]	R	1h	Revision ID of the device.

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9 Application and Implementation

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9.1 Application Information

The TMP4718 operates with a two-wire I^{2}C or SMBus compatible interface. The interfaces support static input thresholds independent of supply to maintain compatibility with a 1.2-V logic I^{2}C or SMBus. The following section shows an example implementation of proper device operation.

9.2 Typical Application

図 9-1 depicts the completed design.

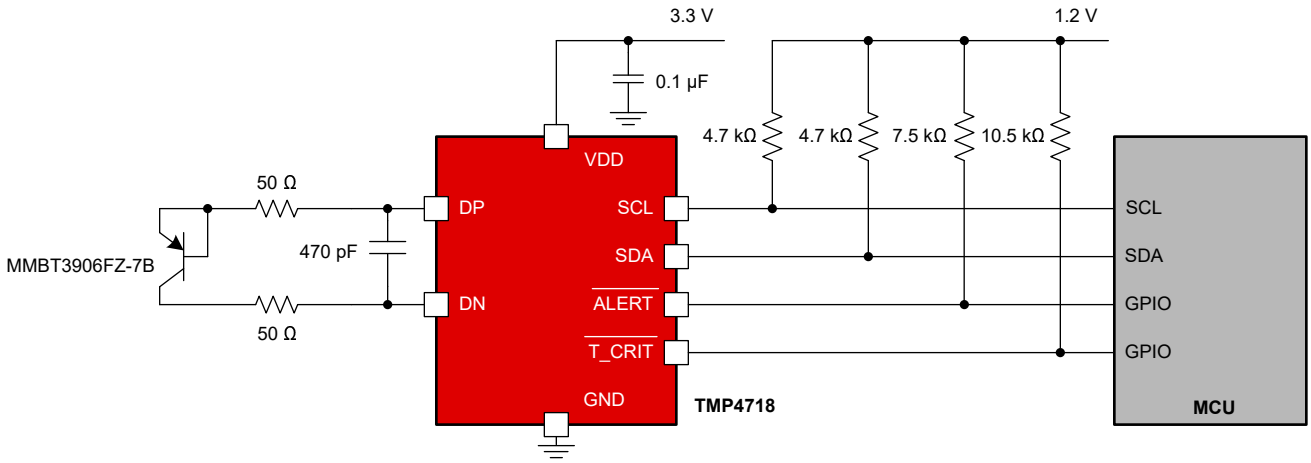

図 9-1. TMP4718 Design Example

9.2.1 Design Requirements

In this design example, the requirement is to design a temperature monitoring system using the TMP4718 with the MMBT3906FZ-7B as the bipolar sensing transistor. The default $\overline{\text{T_CRIT}}$ high temperature limit for this example is 99°C. 表 9-1 lists the design parameters for this application.

表 9-1. Design Parameters

PARAMETER	VALUE
Supply	3.3 V
I/O Pullup Voltage	1.2 V
Default $\overline{\text{T_CRIT}}$ high temperature limit	99°C
Bipolar Transistor	MMBT3906FZ-7B (Diodes Inc.)

9.2.2 Detailed Design Procedure

The ideality factor (η) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. Compensating for ideality factor differences is simple if the diode manufacturer specifies the n-factor

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in the respective data sheet. If the ideality factor of the transistor is not specified, the manufacturer may be able to provide the n-factor value by a special request.

The TMP4718 provides an offset register to allow for a one point offset calibration that compensates for errors. Temperature errors associated with ideality factors of different processors or transistor types may be reduced in a specific temperature range of concern through use of offset calibration. Typical ideality factor specification differences cause a gain variation of the transfer function, so the center of the temperature range can be used as the target temperature for calibration purposes. The TMP4718 is calibrated for the ideality factor of 1.004, so use 式 1 to calculate the required temperature correction factor (T_{CF}) needed to compensate for a target ideality factor that differs from 1.004.

$$T_{CF} = \left(\frac{\eta_{SENSOR} - \eta_{DIODE}}{\eta_{SENSOR}}\right) \times \left(T_{CR} + 273K\right) \quad (1)$$

where:

- η_{SENSOR} is the ideality factor of the temperature sensor, In the case of TMP4718, η_{SENSOR} is calibrated to approximately 1.004.
- η_{DIODE} is the ideality factor of the thermal diode integrated in a processor or a discrete transistor used to measure the temperature at a remote spot.
- T_{CR} is the temperature value at the center of the temperature range of interest.
- T_{CF} is the temperature to compensate for a target ideality factor that can be programmed to the offset register for more accuracy temperature measurement.

In this example, the temperature of interest is from 60°C to 100°C, therefore the 80°C is the center of the temperature range and shall be used in the equation for calculation. The MMBT3906FZ-7B bipolar transistor, which has an ideality factor of approximately 1.01, is selected for this design example. Use 式 2 to calculate the correction factor:

$$T_{CF} = \left(\frac{1.004 - 1.01}{1.004}\right) \times (80 + 273K) = -2.11 \quad (2)$$

The TMP4718 has a remote temperature resolution of 0.125°C. Therefore, 2.125°C is the closest value that can be programmed into the offset register to be subtracted from the remote temperature sensor temperature readings to compensate for the differing typical ideality factors.

The design calls for the default $\overline{\text{T_CRIT}}$ high-temperature limit of 99°C at device power up, which is programmed using the pullup resistors on $\overline{\text{ALERT}}$ and $\overline{\text{T_CRIT}}$ pins. Referring to *Adjustable Default $\overline{\text{T_CRIT}}$ High-Temperature Limit*, the 99°C trip point requires a 7.5-kΩ pullup resistor on the $\overline{\text{ALERT}}$ pin and a 10.5-kΩ pullup resistor on the $\overline{\text{T_CRIT}}$ pin. The default limit allows the $\overline{\text{T_CRIT}}$ pin to engage at the desired threshold and alerts the system of a thermal condition at device power up without any initial software configuration.

Remote junction temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals, and noise can corrupt measurements. The TMP4718 device has a built-in, 65-kHz filter on the inputs of D+ and D– to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor is recommended to make the application more robust against unwanted coupled signals. For this capacitor, select a value of between 100 pF and 3 nF. Some applications attain better overall accuracy with additional series resistance; however, this increased accuracy is application-specific. When series resistance is added, the total value should not be greater than 1 kΩ. If filtering is required, suggested component values are 470 pF and 50 Ω on each input; exact values are application-specific.

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9.2.3 Application Curves

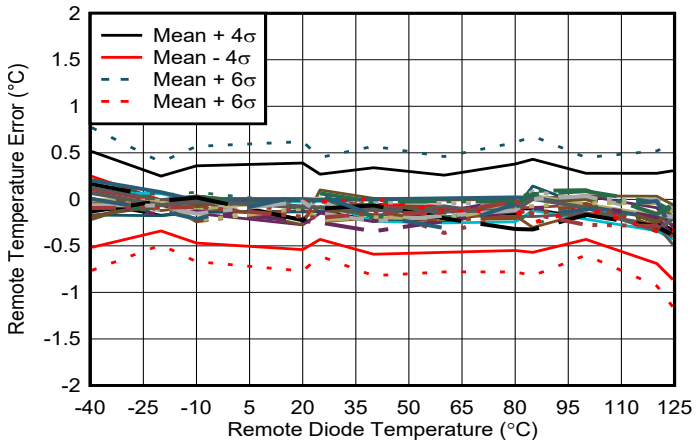

図 9-2. Remote Temperature Accuracy vs Temperature

9.3 Power Supply Recommendations

The TMP4718 device operates with a power-supply range of 1.62 V to 5.5 V. The device is optimized for operation at a 3.3-V supply but can measure temperature accurately in the full supply range. A power-supply bypass capacitor is recommended. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

9.4 Layout

9.4.1 Layout Guidelines

Remote temperature sensing on the TMP4718 device measures very small voltages using very low currents, therefore noise at the device inputs must be minimized. Most applications using the TMP4718 have high digital content, with several clocks and logic-level transitions that create a noisy environment. The layout must adhere to the following guidelines:

1. Place the TMP4718 device as close to the remote junction sensor as possible.
2. Route the DP and DN traces next to each other and shield them from adjacent signals through the use of ground guard traces. If a multilayer PCB is used, bury these traces between the ground or V+ planes to shield them from extrinsic noise sources. 5-mil (0.127 mm) PCB traces are recommended.
3. Minimize additional thermocouple junction induced offset voltage caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the DP and DN connections to cancel any thermocouple effects.
4. Use a 0.1-µF local bypass capacitor directly between the VDD and GND of the TMP4718 device. For optimum measurement performance, minimize filter capacitance between DP and DN to 3 nF or less. This capacitance includes any cable capacitance between the remote temperature sensor and the TMP4718 device. The external capacitor shall be placed as close to the DP and DN pin as possible.
5. If the connection between the remote temperature sensor and the TMP4718 device is less than 8-in (20.32 cm) long, use a twisted-wire pair connection. For lengths greater than 8 inches, use a twisted, shielded pair with the shield grounded as close to the TMP4718 device as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60-Hz pickup.
6. Thoroughly clean and remove all flux residue in and around the pins of the TMP4718 device to avoid any leakage induced temperature measurement error.
7. If series resistors are added, equal value shall be used for the DP and DN connections and the value shall not be greater than 1 kΩ. Place the resistors as closed to the DP and DN pins as possible.

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9.4.2 Layout Example

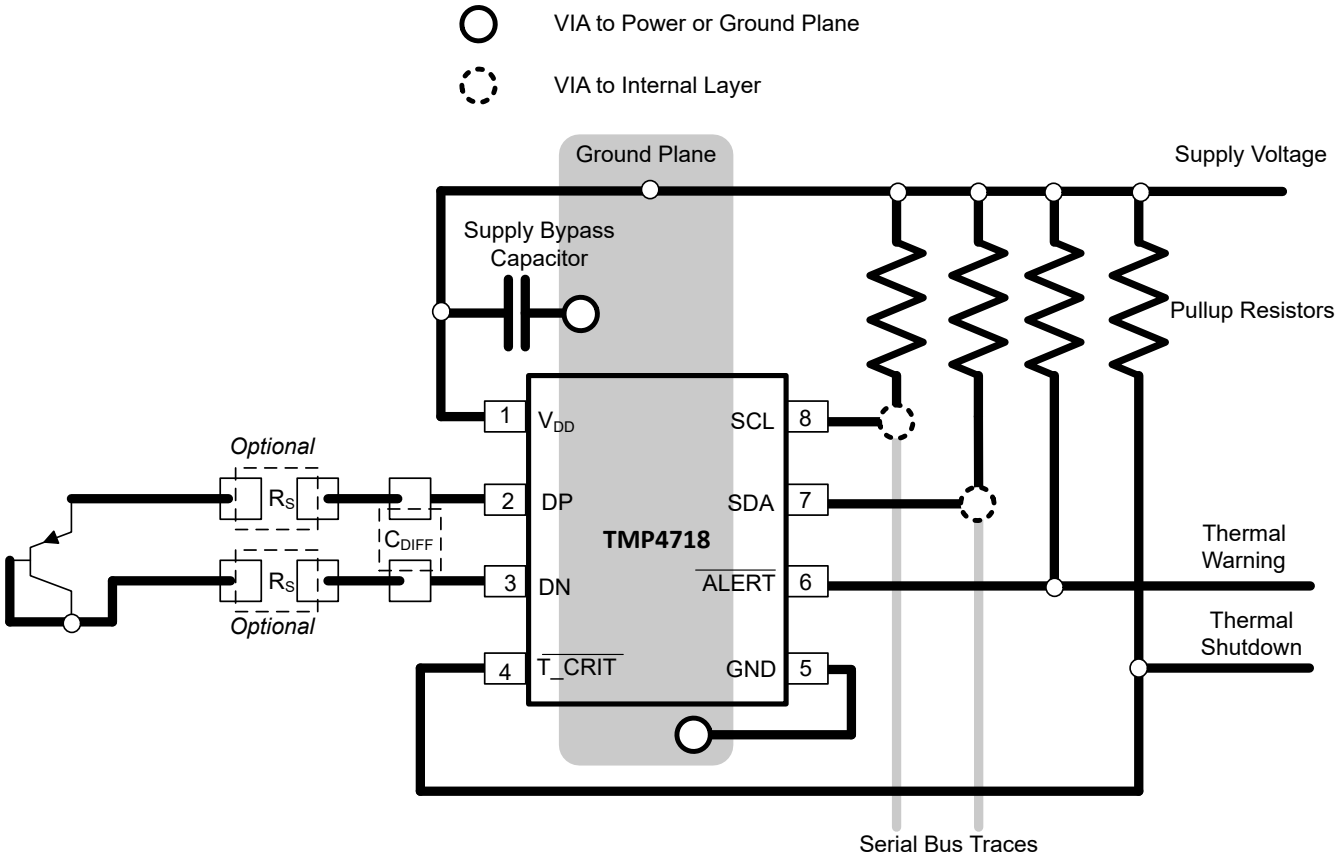

図 9-3. TMP4718 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *I2C Bus Pullup Resistor Calculation* application note
- Texas Instruments, *TMP4718EVM User's Guide*

10.2 ドキュメントの更新通知を受け取る方法

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10.3 サポート・リソース

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP4718ADGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	35ET
TMP4718ADGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	35ET
TMP4718BDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	35FT
TMP4718BDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	35FT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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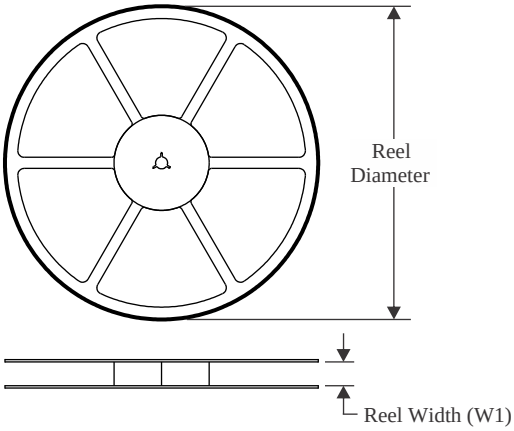
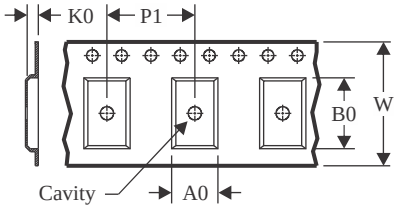
TAPE AND REEL INFORMATION

REEL DIMENSIONS

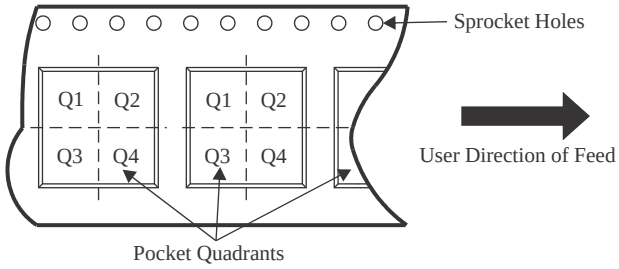


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

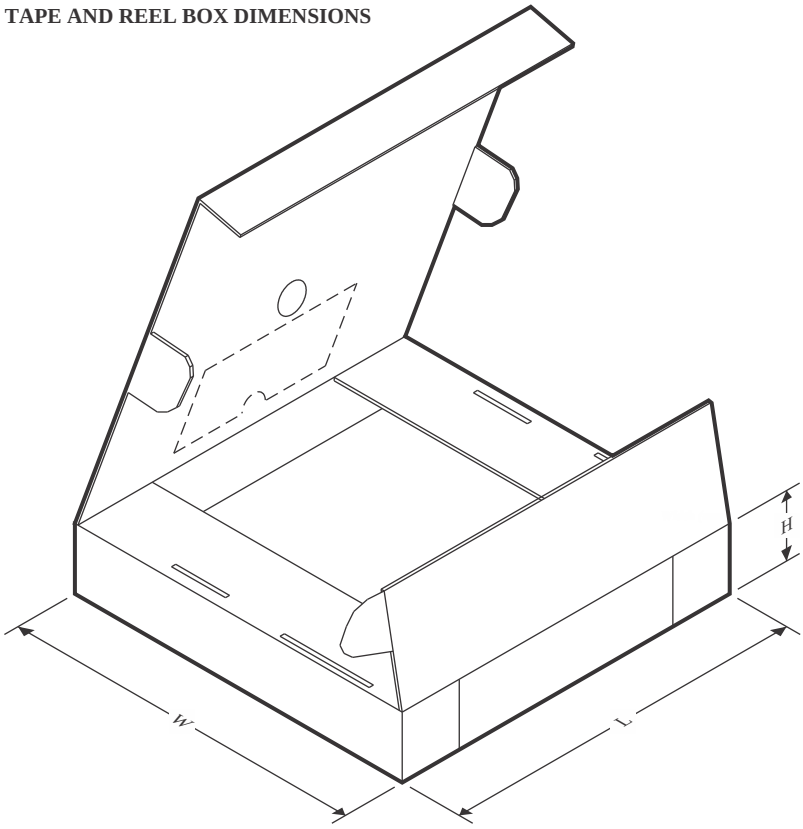
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP4718ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMP4718ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP4718BDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMP4718BDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

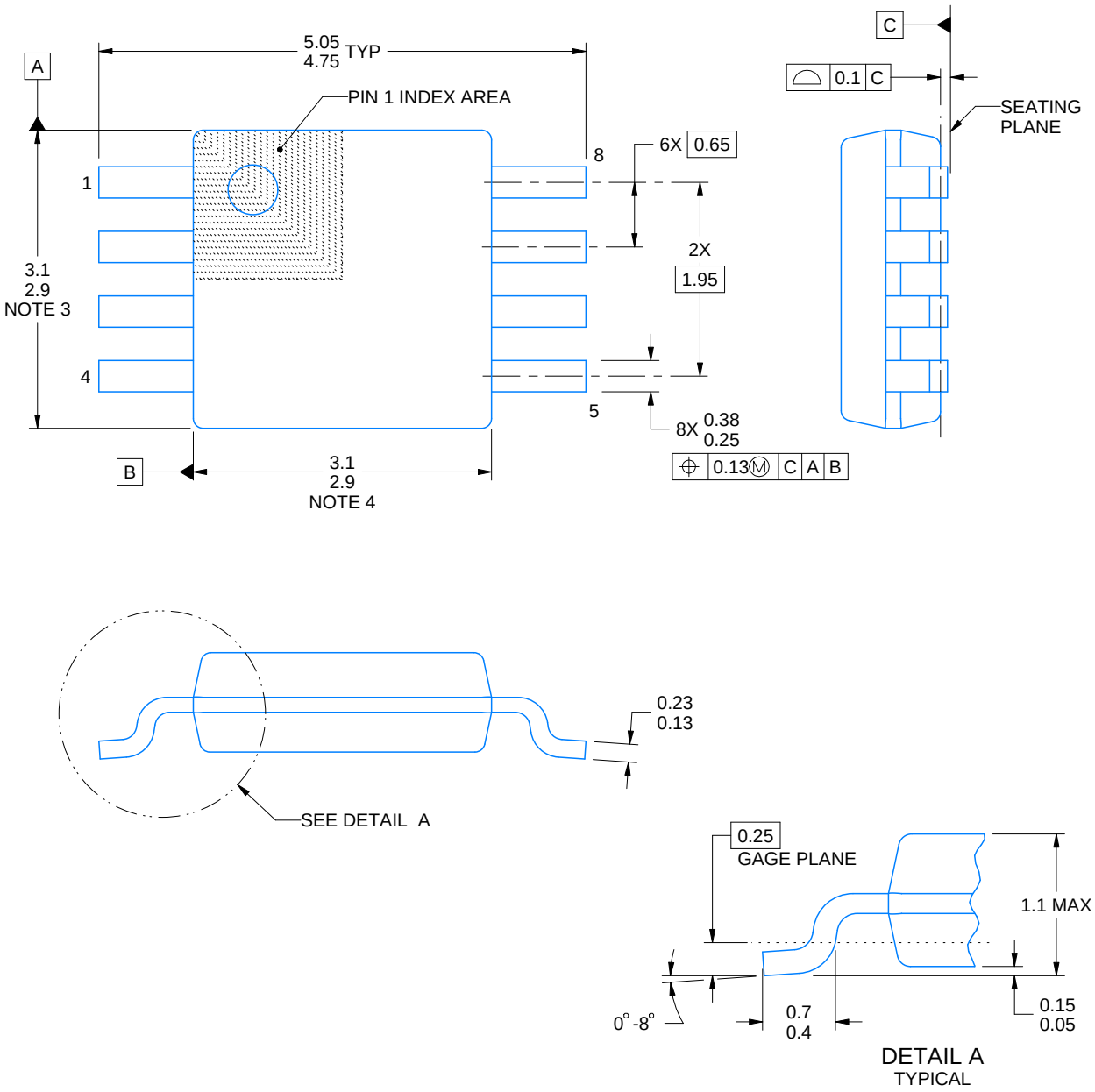
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP4718ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP4718ADGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TMP4718BDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP4718BDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

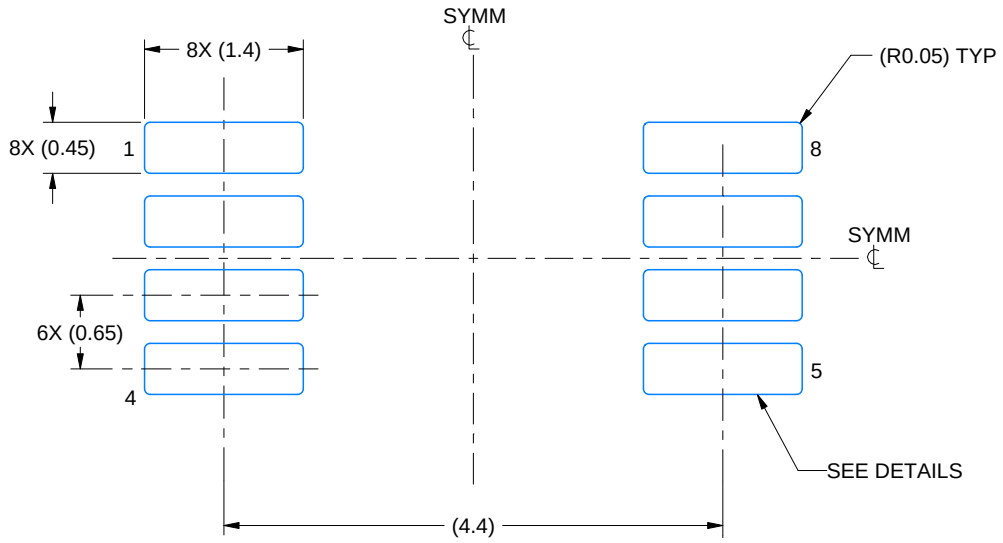
SMALL OUTLINE PACKAGE



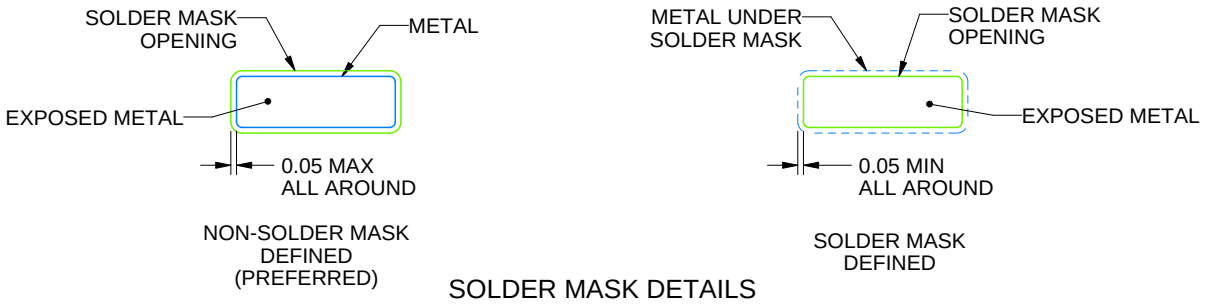
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

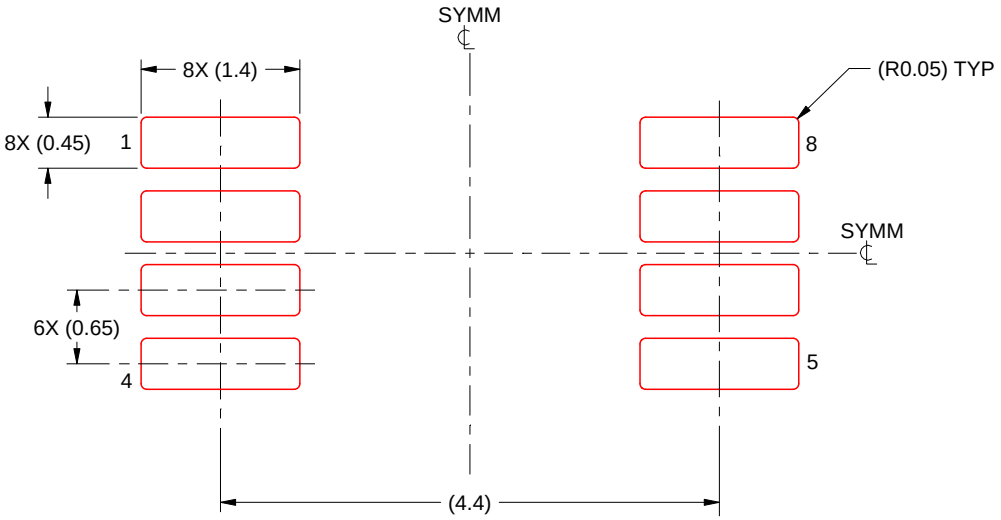


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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