

TMUX6119 $\pm 16.5V$ 、低容量、低リーク電流、高精度のSPDTスイッチ

1 特長

- 広い電源電圧範囲: $\pm 5V \sim \pm 16.5V$ (デュアル) または $10V \sim 16.5V$ (シングル)
- すべてのピンで、JESD78 Class II Level A 準拠の $100mA$ を満たすラッチアップ性能
- 小さいオン容量: $6.4pF$
- 低い入力リーク電流: $0.5pA$
- 低い電荷注入: $0.19pC$
- レール・ツー・レール動作
- 低いオン抵抗: 120Ω
- 遷移時間: $68ns$
- Break-Before-Make のスイッチング動作
- ENピンとSELピンを V_{DD} に接続可能、プルダウン内蔵
- ロジック・レベル: $2V \sim V_{DD}$
- 低い消費電流: $17\mu A$
- 人体モデル(HBM) ESD保護: すべてのピンで $\pm 2kV$
- 業界標準のSOT-23パッケージ

2 アプリケーション

- ファクトリ・オートメーションと産業プロセス制御
- プログラマブル・ロジック・コントローラ (PLC)
- アナログ入力モジュール
- ATE試験装置
- デジタル・マルチメータ
- バッテリ・モニタリング・システム

3 概要

TMUX6119は、最新のCMOS (相補型金属酸化膜半導体) 単極双投(SPDT)スイッチです。このデバイスは、デュアル電源($\pm 5V \sim \pm 16.5V$)、単一電源($10V \sim 16.5V$)、非対称電源のいずれでも適切に動作します。デジタル入力ピンの両方 (ENおよびSEL) にTTL (Transistor-Transistor Logic) 互換のスレッシュホールドがあり、TTL/CMOSとのロジック互換性が保証されます。

TMUX6119は、ENピンの制御によりイネーブルまたはディセーブルにできます。ディセーブルのときは、両方のチャンネル・スイッチがオフになります。イネーブルのとき、SELピンを使用してチャンネルA (SAからDへ) またはチャンネルB (SBからDへ) をオンにできます。各チャンネルは両方向に同等の良好な伝導率を持ち、入力信号範囲は電源よりも広く伸びています。TMUX6119のスイッチは、Break-Before-Make (BBM) スwitchング動作を行います。

TMUX6119は、テキサス・インスツルメンツの高精度スイッチおよびマルチプレクサ・ファミリの製品です。

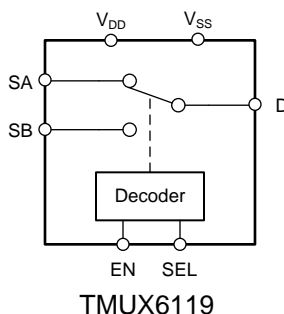
TMUX6119はリーク電流と電荷注入が非常に小さいため、高精度の測定アプリケーションに使用可能です。また、このデバイスはスイッチがOFF位置のとき、電源電圧までの信号レベルをブロックすることで、絶縁性能も非常に優れています。消費電流が $17\mu A$ と低いため、携帯用アプリケーションで使用できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TMUX6119	SOT-23 (8)	2.90mmx1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

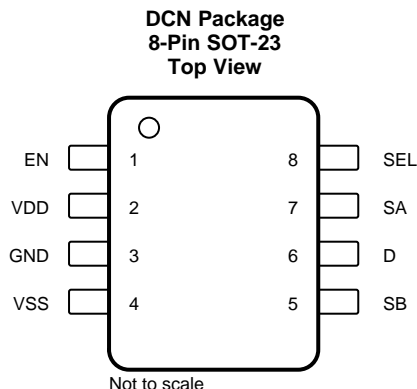
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年9月発行のものから更新

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•	ドキュメントのステータスを「事前情報」から「量産データ」に変更	1
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5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
EN	1	I	Active high digital input. When this pin is low, both switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on.
V _{DD}	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.
GND	3	P	Ground (0 V) reference
V _{SS}	4	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{SS} and GND.
SB	5	I/O	Source pin B. Can be an input or output.
D	6	I/O	Drain pin. Can be an input or output.
SA	7	I/O	Source pin A. Can be an input or output.
SEL	8	I	Logic control input.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		-0.3	18	V
V_{SS} to GND		-18	0.3	V
V_{DIG}	Digital input pin (SEL, EN) voltage	GND -0.3	$V_{DD}+0.3$	V
I_{DIG}	Digital input pin (SEL, EN) current	-30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
I_{ANA_IN}	Analog input pin (Sx) current	-30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
I_{ANA_OUT}	Analog output pin (D) current	-30	30	mA
T_A	Ambient temperature	-55	140	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX6119	UNIT
		DCN (SOT-23)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	138.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	73.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} ⁽¹⁾	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (single supply, $V_{SS} = 0$ V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	-16.5		-5	V

- (1) When $V_{SS} = 0$ V, V_{DD} can range from 10 V to 36 V.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S ⁽²⁾	Source pins voltage	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (SEL, EN) voltage	0		V_{DD}	V
I_{CH}	Channel current ($T_A = 25^\circ\text{C}$)	-25		25	mA
T_A	Ambient temperature	-40		125	$^\circ\text{C}$

(2) V_{DD} and V_{SS} can be any value as long as $10\text{ V} \leq (V_{DD} - V_{SS}) \leq 36\text{ V}$.

6.5 Electrical Characteristics (Dual Supplies: $\pm 15\text{ V}$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	$V_S = 0\text{ V}$, $I_S = 1\text{ mA}$			120	135	Ω
					140	165	Ω
		$V_S = \pm 10\text{ V}$, $I_S = 1\text{ mA}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		210	Ω	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		245	Ω	
ΔR_{ON}	On-resistance mismatch between channels	$V_S = \pm 10\text{ V}$, $I_S = 1\text{ mA}$		2.4	6	Ω	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		9	Ω	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		11	Ω	
R_{ON_FLAT}	On-resistance flatness	$V_S = -10\text{ V}$, 0 V , $+10\text{ V}$, $I_S = 1\text{ mA}$		22	45	Ω	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		47	Ω	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		49	Ω	
R_{ON_DRIFT}	On-resistance drift	$V_S = 0\text{ V}$			0.5		$\% / ^\circ\text{C}$
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	Switch state is off, $V_S = +10\text{ V} / -10\text{ V}$, $V_D = -10\text{ V} / +10\text{ V}$		-0.02	0.005	0.02	nA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		-0.12	0.05	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		-1	0.2	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	Switch state is off, $V_S = +10\text{ V} / -10\text{ V}$, $V_D = -10\text{ V} / +10\text{ V}$		-0.02	0.005	0.02	nA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		-0.12	0.05	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		-1	0.2	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, $V_S = +10\text{ V} / -10\text{ V}$, $V_D = -10\text{ V} / +10\text{ V}$		-0.04	0.01	0.04	nA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		-0.25	0.1	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		-1.8	0.4	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		M Ω
POWER SUPPLY							
I_{DD}	V_{DD} supply current	$V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$			16	21	μA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		22	μA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		23	μA	
I_{SS}	V_{SS} supply current	$V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$			7	10	μA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		11	μA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		12	μA	

(1) When V_S is positive, V_D is negative, and vice versa.

6.6 Switching Characteristics (Dual Supplies: ±15 V)

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	$V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$		68	86	ns
		$V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			110	ns
		$V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			121	ns
t_{OFF}	Enable turn-off time	$V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$		57	64	ns
		$V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			78	ns
		$V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			82	ns
t_{TRAN}	Transition time	$V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$		68	88	ns
		$V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			99	ns
		$V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			106	ns
t_{BBM}	Break-before-make time delay	$V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	8	37		ns
Q_J	Charge injection	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$		-0.19		pC
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$		-85		dB
X_{TALK}	Channel-to-channel crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$		-93		dB
I_L	Insertion loss	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$		-7.7		dB
ACPSRR	AC Power Supply Rejection Ratio	$R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $V_{PP} = 0.62\text{ V}$ on V_{DD} , $f = 1\text{ MHz}$		-55		dB
		$R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $V_{PP} = 0.62\text{ V}$ on V_{SS} , $f = 1\text{ MHz}$		-55		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$		700		MHz
THD	Total harmonic distortion + noise	$R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz		0.08		%
C_{IN}	Digital input capacitance	$V_{IN} = 0\text{ V}$ or V_{DD}		0.8		pF
$C_{S(OFF)}$	Source off-capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$		1.9	2.8	pF
$C_{D(OFF)}$	Drain off-capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$		4.3	4.7	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$		6.4	8.1	pF

(1) Specified by design; not subject to production testing.

6.7 Electrical Characteristics (Single Supply: 12 V)

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	$V_S = 10\text{ V}$, $I_S = 1\text{ mA}$			230	265	Ω
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			355	Ω
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			405	Ω
ΔR_{ON}	On-resistance mismatch between channels	$V_S = 10\text{ V}$, $I_S = 1\text{ mA}$			1	9	Ω
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			12	Ω
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			14	Ω
R_{ON_DRIFT}	On-resistance drift	$V_S = 0\text{ V}$			0.48		%/ $^\circ\text{C}$

Electrical Characteristics (Single Supply: 12 V) (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	Switch state is off, $V_S = 10\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/10\text{ V}$		-0.02	0.005	0.02	nA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.08		0.04	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-0.75		0.13	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	Switch state is off, $V_S = 10\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/10\text{ V}$		-0.02	0.005	0.02	nA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.08		0.04	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-0.75		0.13	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, $V_S =$ floating, $V_D = 1\text{ V}/10\text{ V}$		-0.04	0.01	0.04	nA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.16		0.08	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-1.5		0.25	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		M Ω
POWER SUPPLY							
I_{DD}	V_{DD} supply current	$V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$			11	14	μA
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			16	μA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			17	μA

(1) When V_S is positive, V_D is negative, and vice versa.

6.8 Switching Characteristics (Single Supply: 12 V)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$			73	91	ns
		$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				119	ns
		$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				130	ns
t_{OFF}	Enable turn-off time	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$			60	69	ns
		$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				82	ns
		$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				88	ns
t_{TRAN}	Transition time	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$			73	93	ns
		$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				104	ns
		$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				112	ns
t_{BBM}	Break-before-make time delay	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		10	45		ns
Q_J	Charge injection	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$			0.1		pC
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$			-85		dB
X_{TALK}	Channel-to-channel crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$			-100		dB
I_L	Insertion loss	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$			-15		dB
ACPSRR	AC Power Supply Rejection Ratio	$R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $V_{PP} = 0.62\text{ V}$, $f = 1\text{ MHz}$			-55		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$			440		MHz
C_{IN}	Digital input capacitance	$V_{IN} = 0\text{ V}$ or V_{DD}			1		pF

(1) Specified by design; not subject to production testing.

Switching Characteristics (Single Supply: 12 V) (continued)

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{S(OFF)}$	Source off-capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$		2	2.9	pF
$C_{D(OFF)}$	Drain off-capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$		4.9	5.3	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$		7.4	8.9	pF

6.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

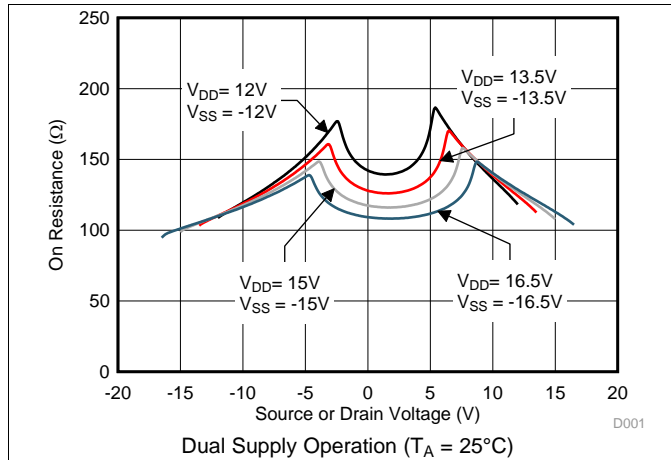


图 1. On-Resistance vs Source or Drain Voltage

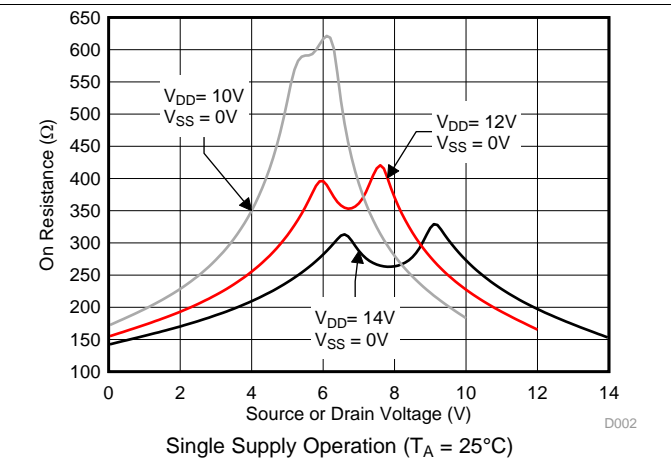


图 2. On-Resistance vs Source or Drain Voltage

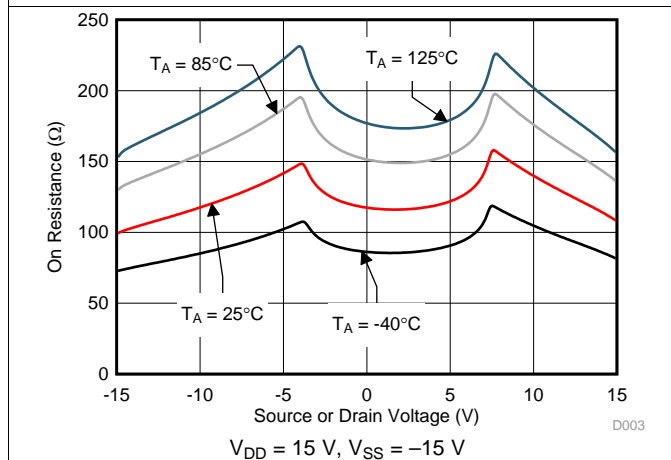


图 3. On-Resistance vs Source or Drain Voltage

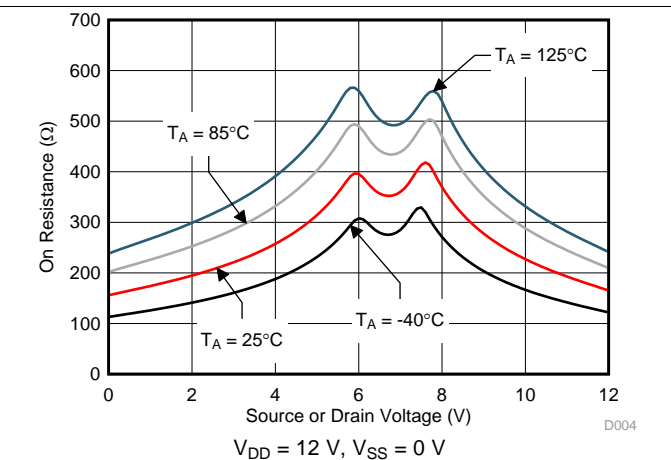


图 4. On-Resistance vs Source or Drain Voltage

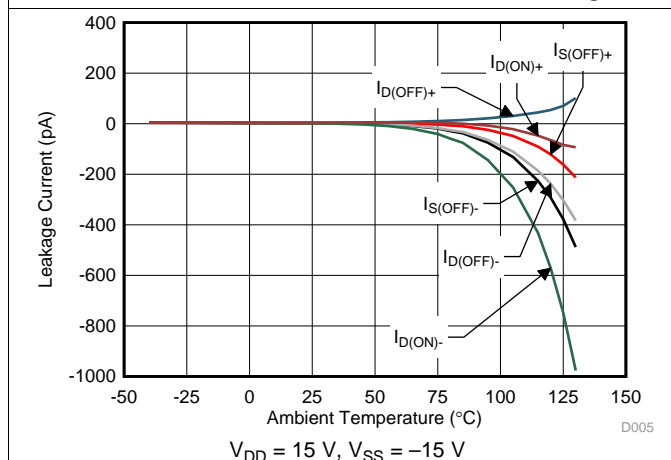


图 5. Leakage Current vs Temperature

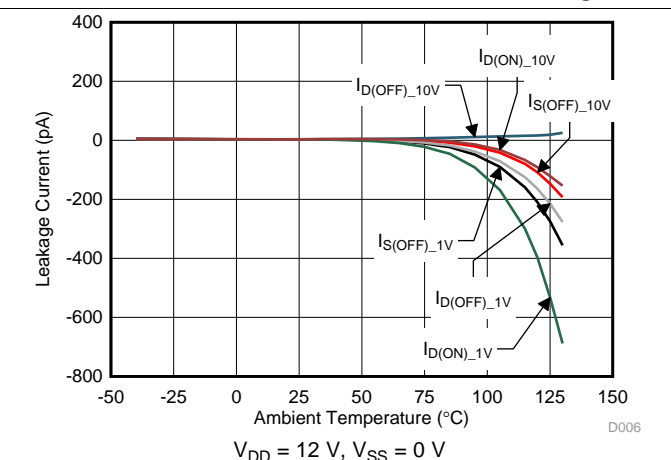
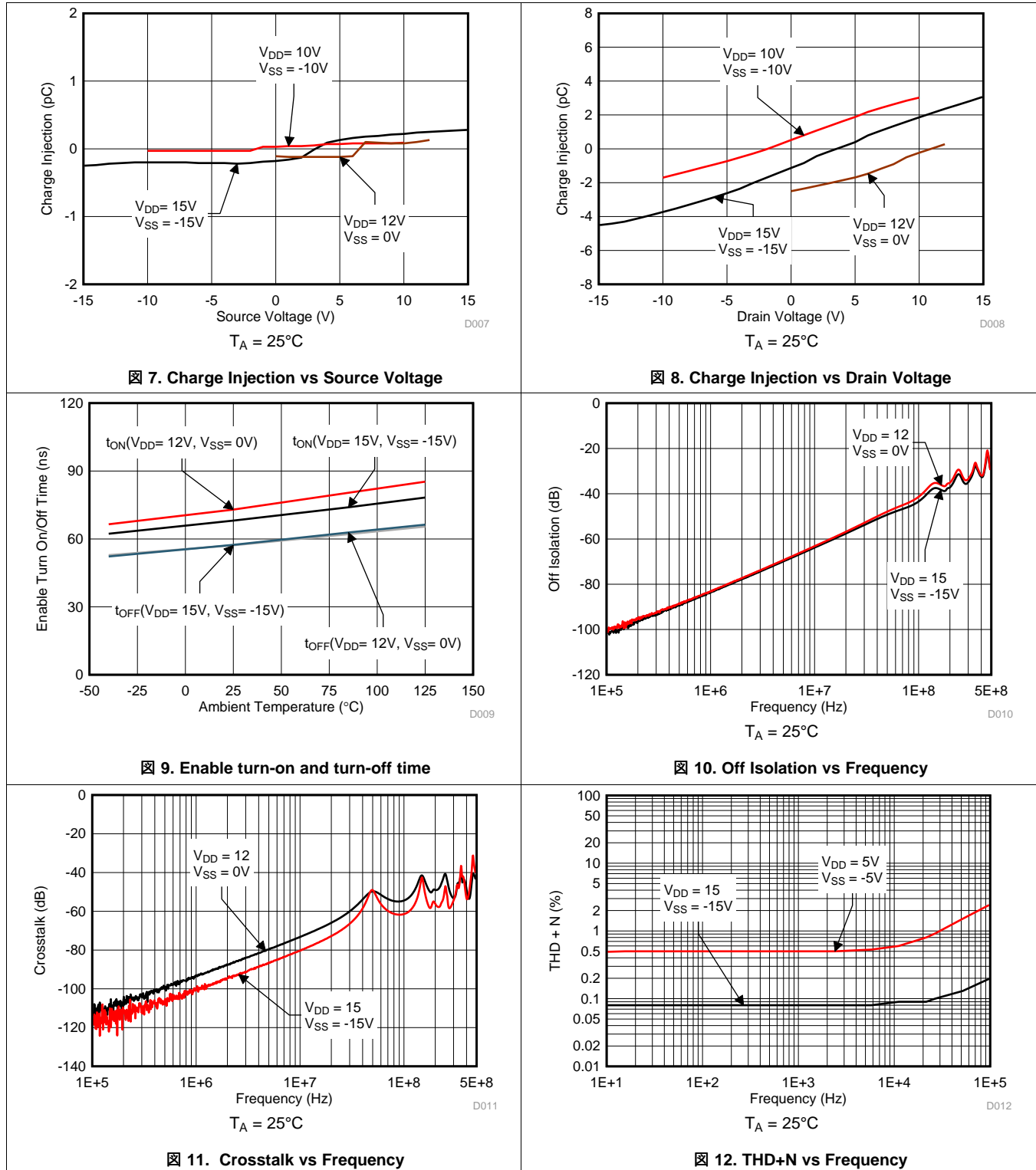


图 6. Leakage Current vs Temperature

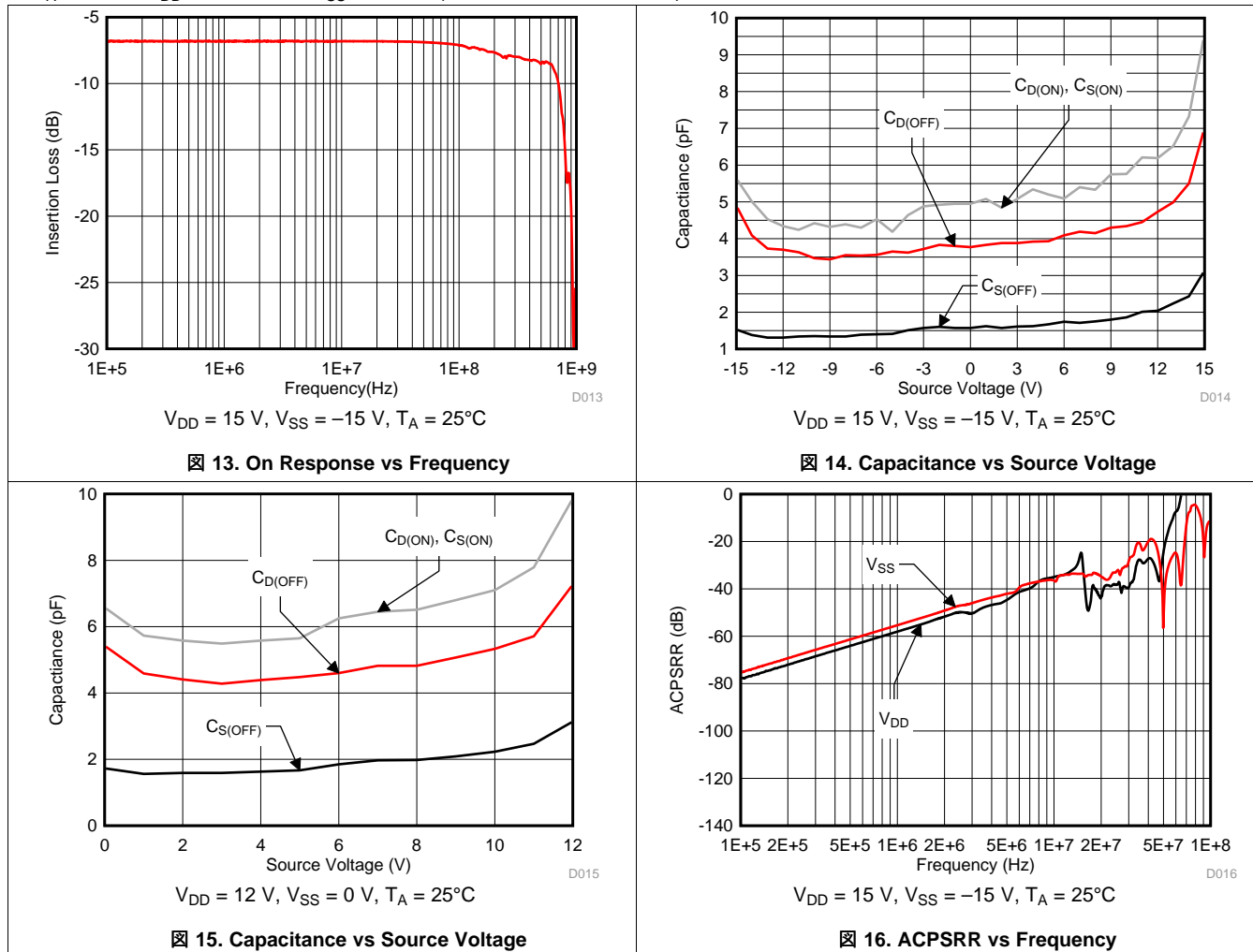
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)



7 Parameter Measurement Information

7.1 Truth Tables

表 1 shows the truth tables for the TMUX6119.

表 1. TMUX6119 Truth Table

EN	SEL	STATE	
		Switch A (SA to D)	Switch B (SB to D)
0	X ⁽¹⁾	OFF	OFF
1	0	ON	OFF
1	1	OFF	ON

(1) X denotes *don't care*.

8 Detailed Description

8.1 Overview

The TMUX6119 has a low on and off leakage currents and ultra-low charge injection, allowing the device to be used in high precision measurement applications. The device also provides excellent isolation capability by blocking signal levels up to the supplies when the switches are in the OFF position. A low supply current of 17 μA enables usage in portable applications.

8.1.1 On-Resistance

The on-resistance of the TMUX6119 is the ohmic resistance across the source (SA or SB) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in [Figure 17](#). Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in [Equation 1](#):

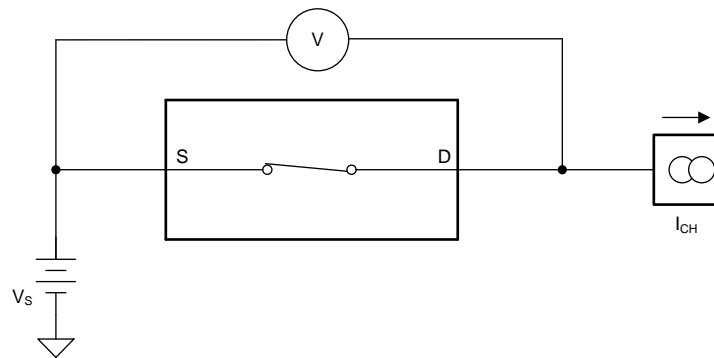


Figure 17. On-Resistance Measurement Setup

$$R_{\text{ON}} = V / I_{\text{CH}} \quad (1)$$

8.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{\text{S(OFF)}}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{\text{D(OFF)}}$.

The setup used to measure both off-leakage currents is shown in [Figure 18](#).

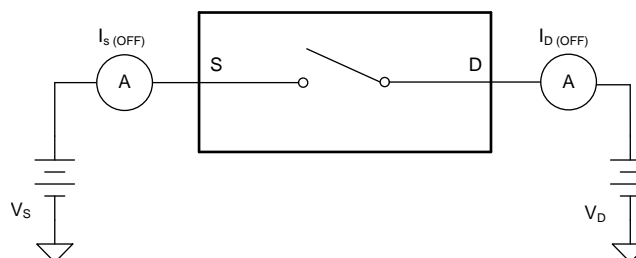


Figure 18. Off-Leakage Measurement Setup

Overview (continued)

8.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. Figure 19 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

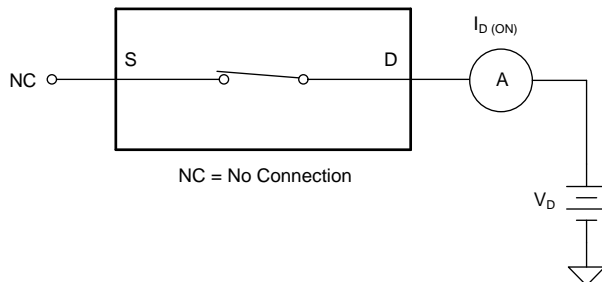


Figure 19. On-Leakage Measurement Setup

8.1.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX6119 to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. Figure 20 shows the setup used to measure transition time, denoted by the symbol t_t .

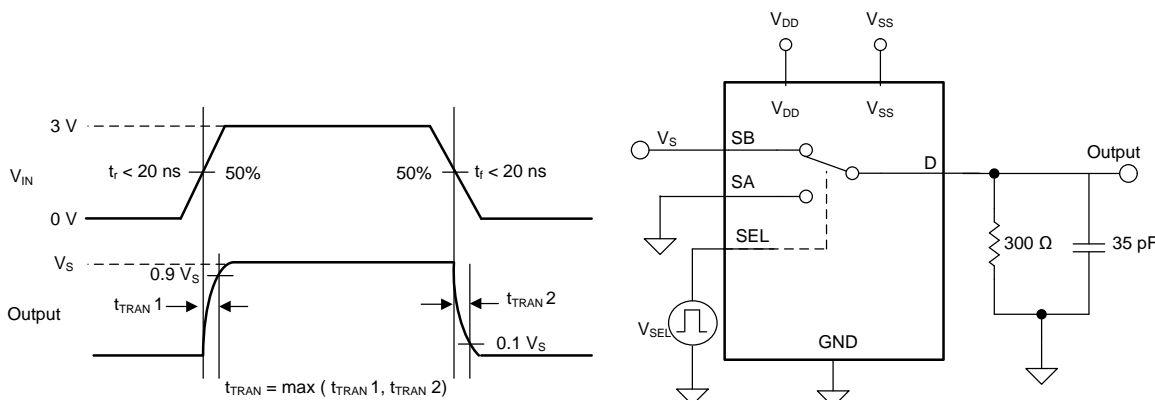


Figure 20. Transition-Time Measurement Setup

Overview (continued)

8.1.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX6119 is switching. The TMUX6119 output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. [Figure 21](#) shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM} .

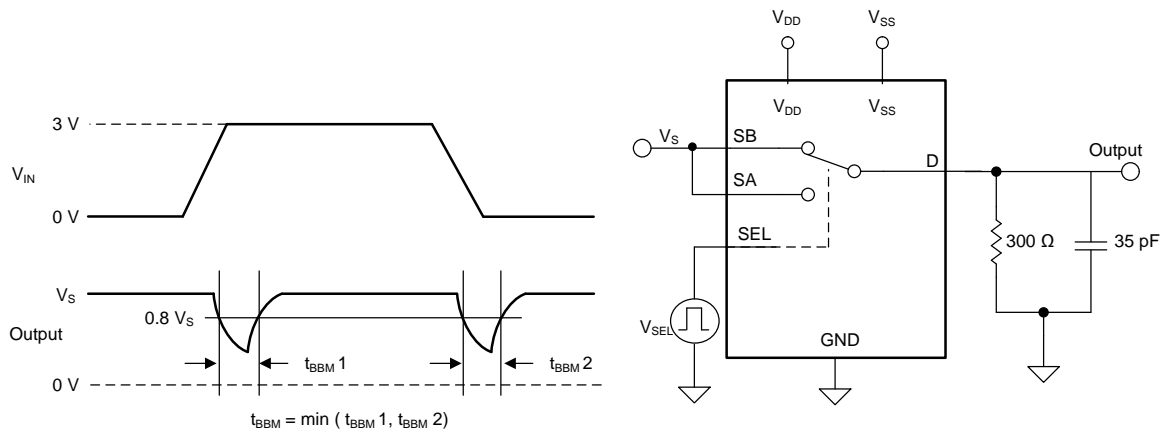


Figure 21. Break-Before-Make Delay Measurement Setup

8.1.6 Enable Turn-On and Enable Turn-Off Time

Enable turn-on time is defined as the time taken by the output of the TMUX6119 to rise to a 90% final value after the EN signal has risen to a 50% final value. [Figure 22](#) shows the setup used to measure turn-on time. Enable turn-on time is denoted by the symbol t_{ON} .

Enable turn off time is defined as the time taken by the output of the TMUX6119 to fall to a 10% initial value after the EN signal has fallen to a 50% initial value. [Figure 22](#) shows the setup used to measure turn-off time. Enable Turn-off time is denoted by the symbol t_{OFF} .

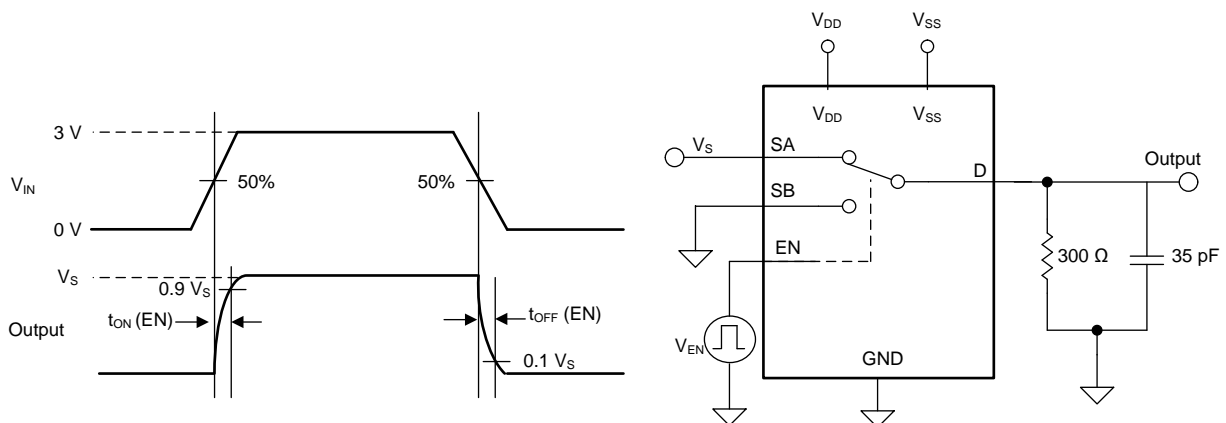


Figure 22. Turn-On and Turn-Off Time Measurement Setup

Overview (continued)

8.1.7 Charge Injection

The TMUX6119 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ} . Figure 23 and Figure 24 shows the setup used to measure charge injection from source to drain and from drain to source. The charge injection is optimized for the TMUX6119 from the direction of source to drain.

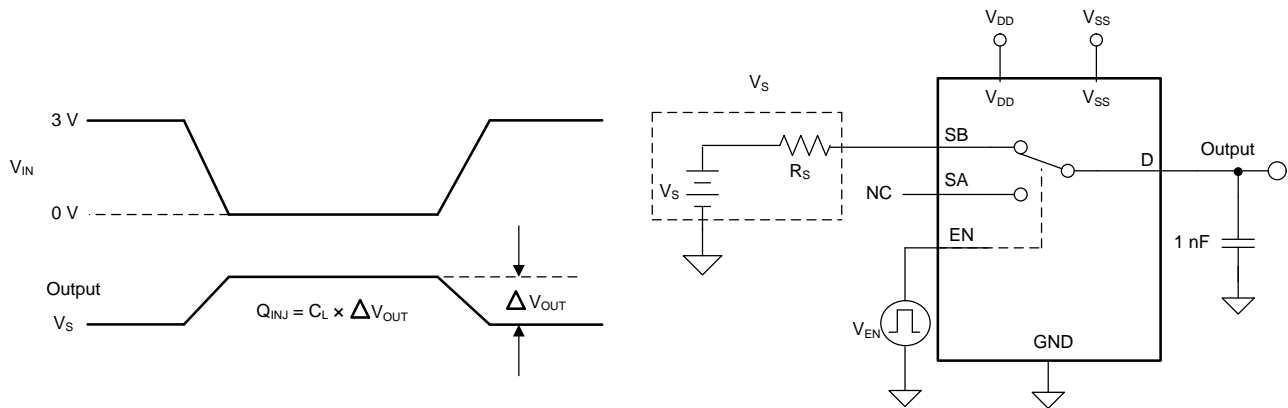


Figure 23. Source to Drain Charge-Injection Measurement Setup

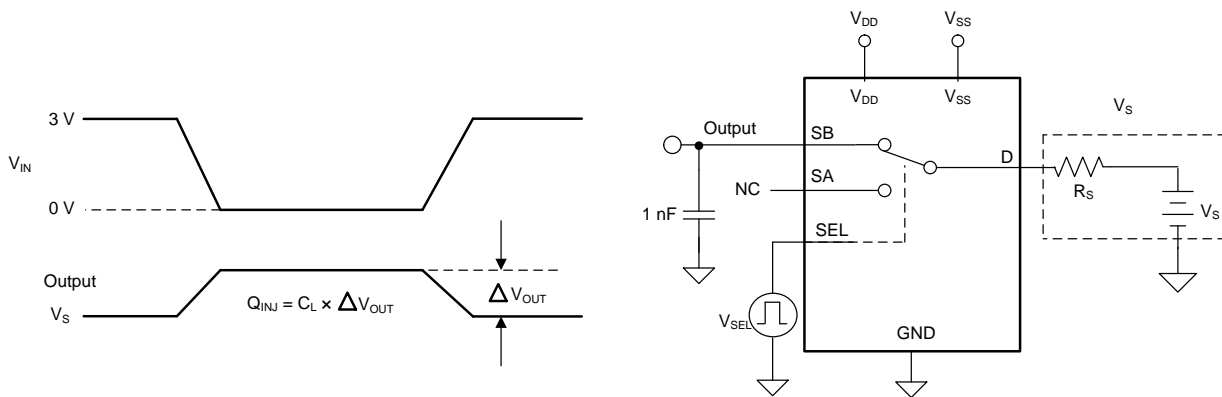
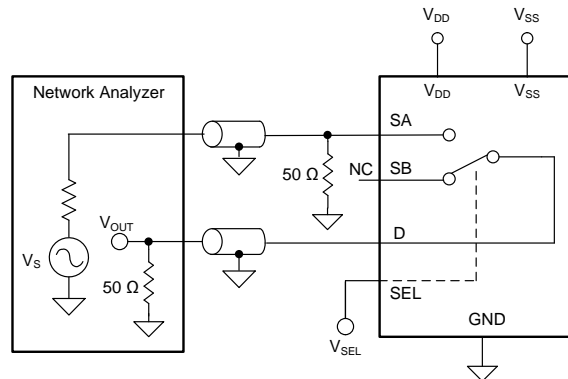


Figure 24. Drain to Source Charge-Injection Measurement Setup

8.1.8 Off Isolation

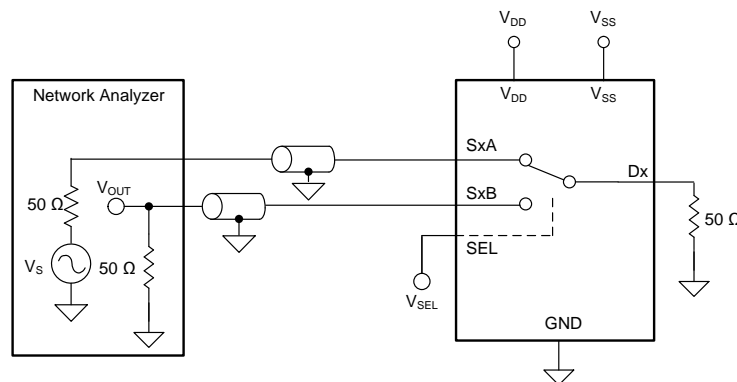
Off isolation is defined as the voltage at the drain pin (D) of the TMUX6119 when a 1- V_{RMS} signal is applied to the source pin (SA or SB) of an off-channel. Figure 25 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.

Overview (continued)

Figure 25. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_S} \right) \quad (2)$$

8.1.9 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (SA or SB) of an off-channel, when a 1- V_{RMS} signal is applied at the source pin of an on-channel. Figure 26 shows the setup used to measure, and Equation 3 is the equation used to compute, channel-to-channel crosstalk.


Figure 26. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_S} \right) \quad (3)$$

8.1.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin of an on-channel, and the output is measured at the drain pin of the TMUX6119. Figure 27 shows the setup used to measure bandwidth of the mux. Use Equation 4 to compute the attenuation.

Overview (continued)

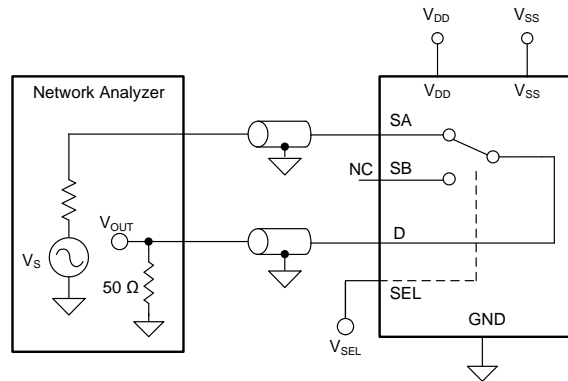


Figure 27. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log} \left(\frac{V_2}{V_1} \right) \tag{4}$$

8.1.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6119 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 28 shows the setup used to measure THD+N of the TMUX6119.

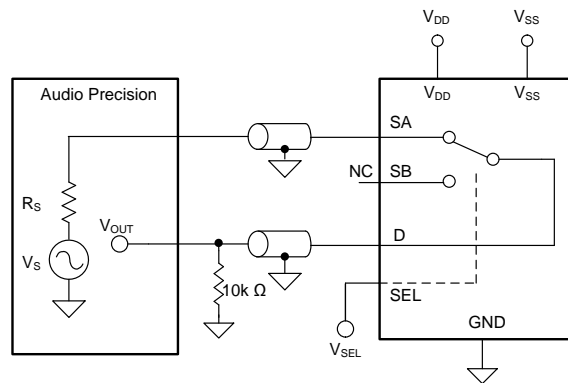
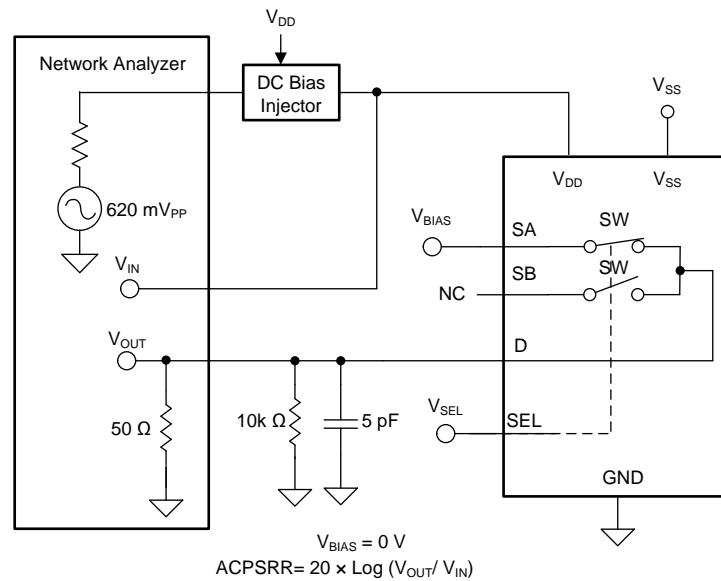


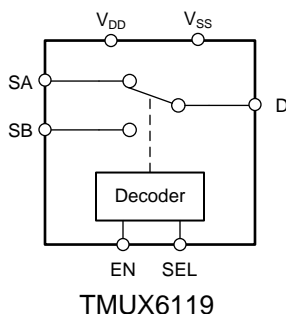
Figure 28. THD+N Measurement Setup

Overview (continued)
8.1.12 AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR. [Figure 29](#) shows the setup used to measure ACPSRR of the TMUX6119.


Figure 29. AC PSRR Measurement Setup

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Ultra-low Leakage Current

The TMUX6119 provide extremely low on- and off-leakage currents. The TMUX6119 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. [Fig 30](#) shows typical leakage currents of the TMUX6119 versus temperature.

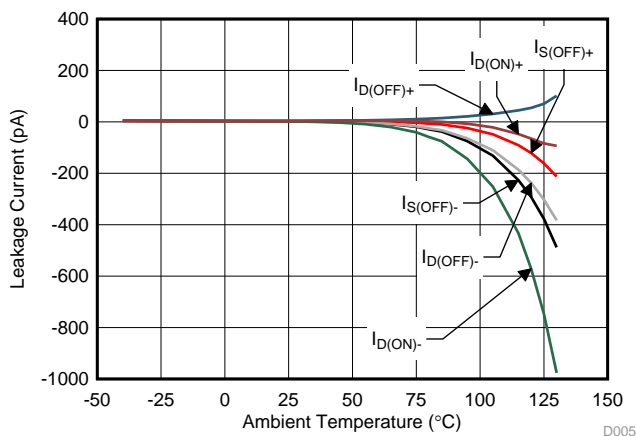
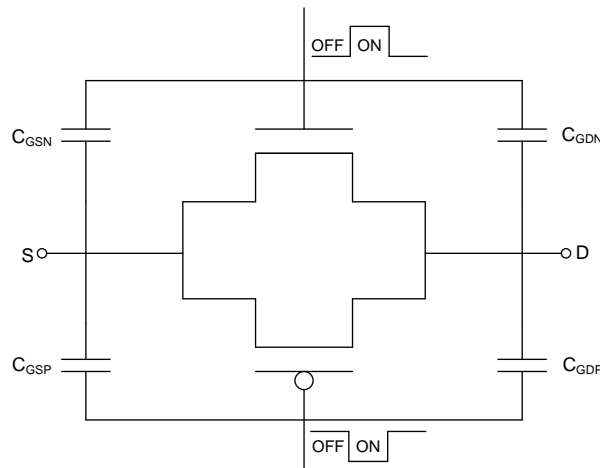


Fig 30. Leakage Current vs Temperature

8.3.2 Ultra-low Charge Injection

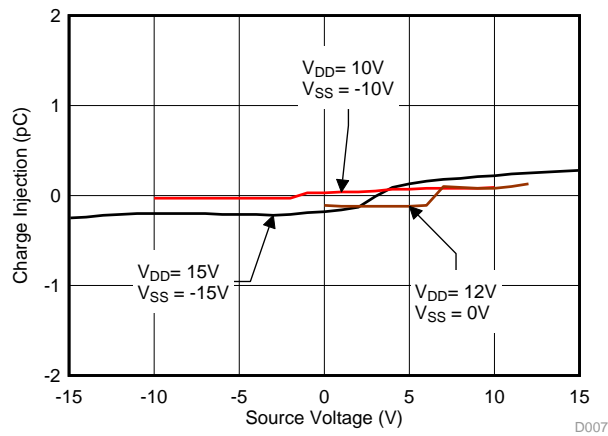
The TMUX6119 is implemented with simple transmission gate topology, as shown in [Fig 31](#). Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

Feature Description (continued)



31. Transmission Gate Topology

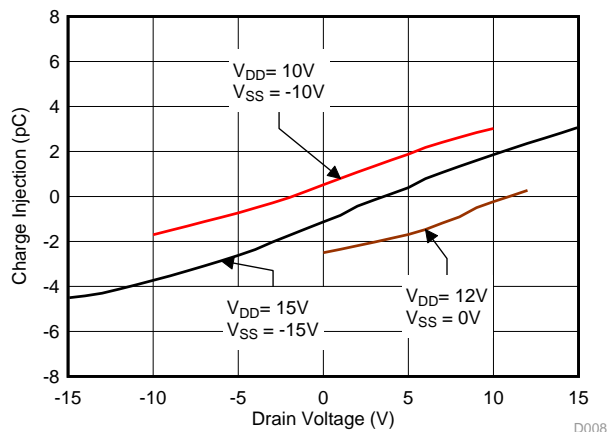
The TMUX6119 utilizes special charge-injection cancellation circuitry that reduces the source (SA or SB)-to-drain (D) charge injection to as low as 0.19 pC at $V_S = 0$ V, as shown in 32.



32. Charge Injection vs Source Voltage

The drain (D)-to-source (SA or SB) charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. 33 shows the drain-to-source charge injection across the full signal range.

Feature Description (continued)



33. Charge Injection vs Drain Voltage

8.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6119 conducts equally well from source (SA or SB) to drain (D) or from drain (D) to source (SA or SB). Each TMUX6119 channel has very similar characteristics in both directions. The valid analog signal for TMUX6119 ranges from V_{SS} to V_{DD} . The input signal to the TMUX6119 swings from V_{SS} to V_{DD} without any significant degradation in performance.

8.4 Device Functional Modes

When the EN pin of the TMUX6119 is pulled high, one of the two switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both switches remain open irrespective of the state of the SEL pin. The EN pin is weakly pull-down internally through a 6MΩ resistor, thereby setting each channel to the open state if the EN pin is not actively driven. The SEL pin is also weakly pulled-down through an internal 6MΩ resistor, allowing channel A (SA to D) to be selected by default when EN pin is driven high. Both the EN pin and the SEL pin can be connected to V_{DD} (as high as 16.5 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX6119 offers outstanding input / output leakage current and ultra-low charge injection performance. The on-capacitance of the TMUX6119 is also very low. These properties make the TMUX6119 ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

9.2 Typical Application

One application to take advantage of TMUX6119's precision performance is the implementation of the chopper amplifier. The chopper amplifier was developed in the 1950s to achieve ultra-low offset voltage and low offset voltage drift over time and temperature. It also drastically reduces low frequency 1/f (flicker) noise. These attributes make the chopper amplifier ideal for small signal conditioning. [Figure 34](#) illustrates a classic example of a simple chopper amplifier implemented with two TMUX6119 SPDT switches.

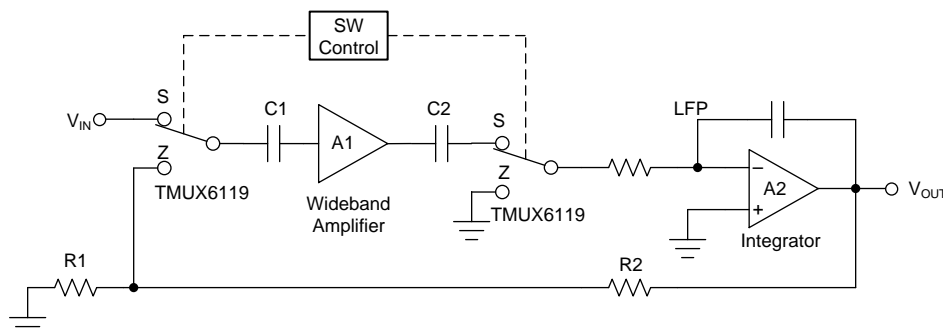


Figure 34. Example of classic chopper amplifier implemented with two TMUX6119

9.2.1 Design Requirements

The goal of a chopper-amplifier design is to produce extremely high DC precision by continuously self-cancelling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage, while reducing low-frequency 1/f (flicker) voltage.

Typical Application (continued)

9.2.2 Detailed Design Procedure

The theory of operation for the chopper amplifier relies on the concept of converting a DC input signal to AC before feeding it into an AC-coupled wideband amplifier. The conversion utilizes a SPDT switches to “chop” the input DC signal into an AC voltage. The output of the amplifier is then modulated by another SPDT switch to convert the signal back to DC. The output of the switch is then low-pass filtered (or integrated) to smooth and produce the final DC output.

The operation of the chopper amplifier consists of 2 phases, the sampling (S) phase and the auto-zero (Z) phase. During the auto-zero phase, the switches are toggled to the Z position, and capacitors C1 and C2 are charged to the amplifier input and output offset voltage, respectively. During the sampling phase, the switches are toggled to the S position, during which VIN is connected to VOUT through C1, the wideband amplifier, C2, and the integrator. Input DC voltage is AC-coupled by capacitor C1 and amplified by the wideband amplifier A1. C2 helps reduce any DC component caused by the amplifier’s input offset voltage, and the integrator helps smooth out the output signals to produce desired DC voltage output.

Several mechanisms helps reduce overall noise of the chopper-amplifier design. The DC gain, being the product of the AC stage and the DC gain of the integrator, can easily reach an open-loop gain of 160 dB or higher and therefore reduce the gain error, $V_{OUT}/(A1 \times A2)$ to almost zero. The offset and drift in the output integrator stage are nulled by the DC gain of the preceding AC stage. DC drifts in the AC stage are also non-factors because the amplification stage is AC-coupled. The 1/f noise of the wideband amplifier is modulated to higher frequencies by the demodulator.

Note that the input signal frequency shall be much less than one-half of the chopping frequency to prevent aliasing errors in this chopper amplifier implementation. The chopper frequency, in turn, is restricted by the wideband amplifier’s gain-phase limitations as well as errors induced by switch transition time and charge injection. The TMUX6119’s switch transition time is only 68 ns (typ) and average charge injection is less than 0.19pC, making it ideal for the chopper amplifier implementation. However, the input signal frequency is still limited by the amplifier’s performance. If higher sampling frequency is required, a chopper-stabilized amplifier, or an integrated zero-drift amplifier (such as the [OPA2188](#)), can be used to satisfy the requirement.

9.2.3 Application Curve

Fast transition time and small charge injection are two critical parameters for the SPDT switches used in the chopper amplifier design. [Figure 35](#) shows the plot for the charge injection vs. source voltage for the TMUX6119.

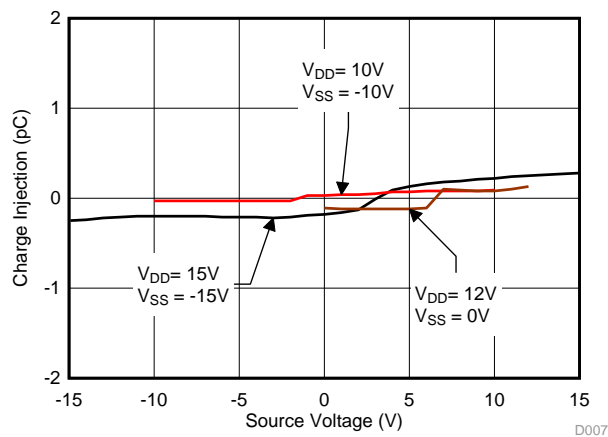


Figure 35. Charge Injection vs Source Voltage

10 Power Supply Recommendations

The TMUX6119 operates across a wide supply range of $\pm 5\text{ V}$ to $\pm 16.5\text{ V}$ (10 V to 16.5 V in single-supply mode). They also perform well with unsymmetric supplies such as $V_{DD} = 12\text{ V}$ and $V_{SS} = -5\text{ V}$. For reliable operation, use a supply decoupling capacitor ranging between $0.1\ \mu\text{F}$ to $10\ \mu\text{F}$ at both the V_{DD} and V_{SS} pins to ground.

The on-resistance of the TMUX6119 varies with supply voltage, as illustrated in [Figure 36](#).

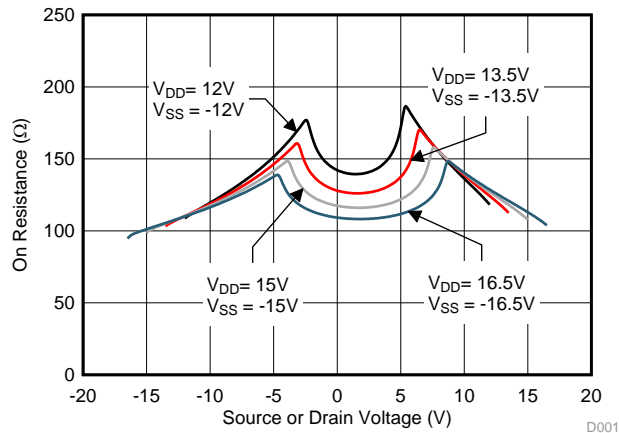


Figure 36. On-Resistance Variation With Supply and Input Voltage

11 Layout

11.1 Layout Guidelines

Figure 37 shows an example of a PCB layout with the TMUX6119.

Some key considerations are:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1- μF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible. In case of the differential signal, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

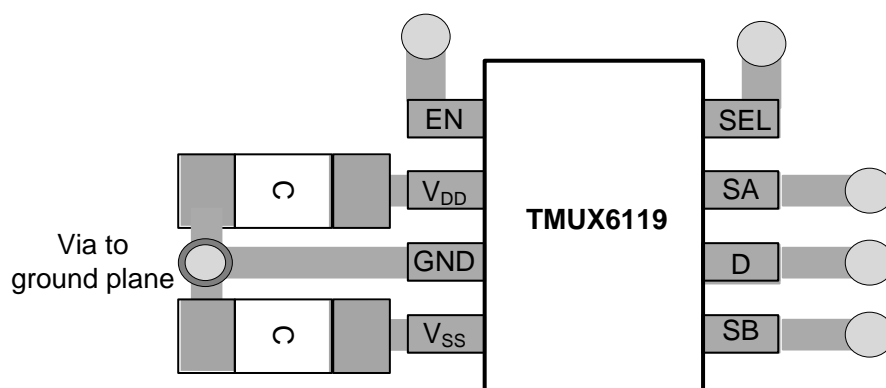


Figure 37. TMUX6119 Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

- 『[OPA2188](#)ドリフト係数 $0.03\mu\text{V}/^\circ\text{C}$ 、低ノイズ、レール・ツー・レール出力、36V、ゼロ・ドリフト・オペアンプ』(SBOS525)

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E2E is a trademark of Texas Instruments.

12.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6119DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1QAC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

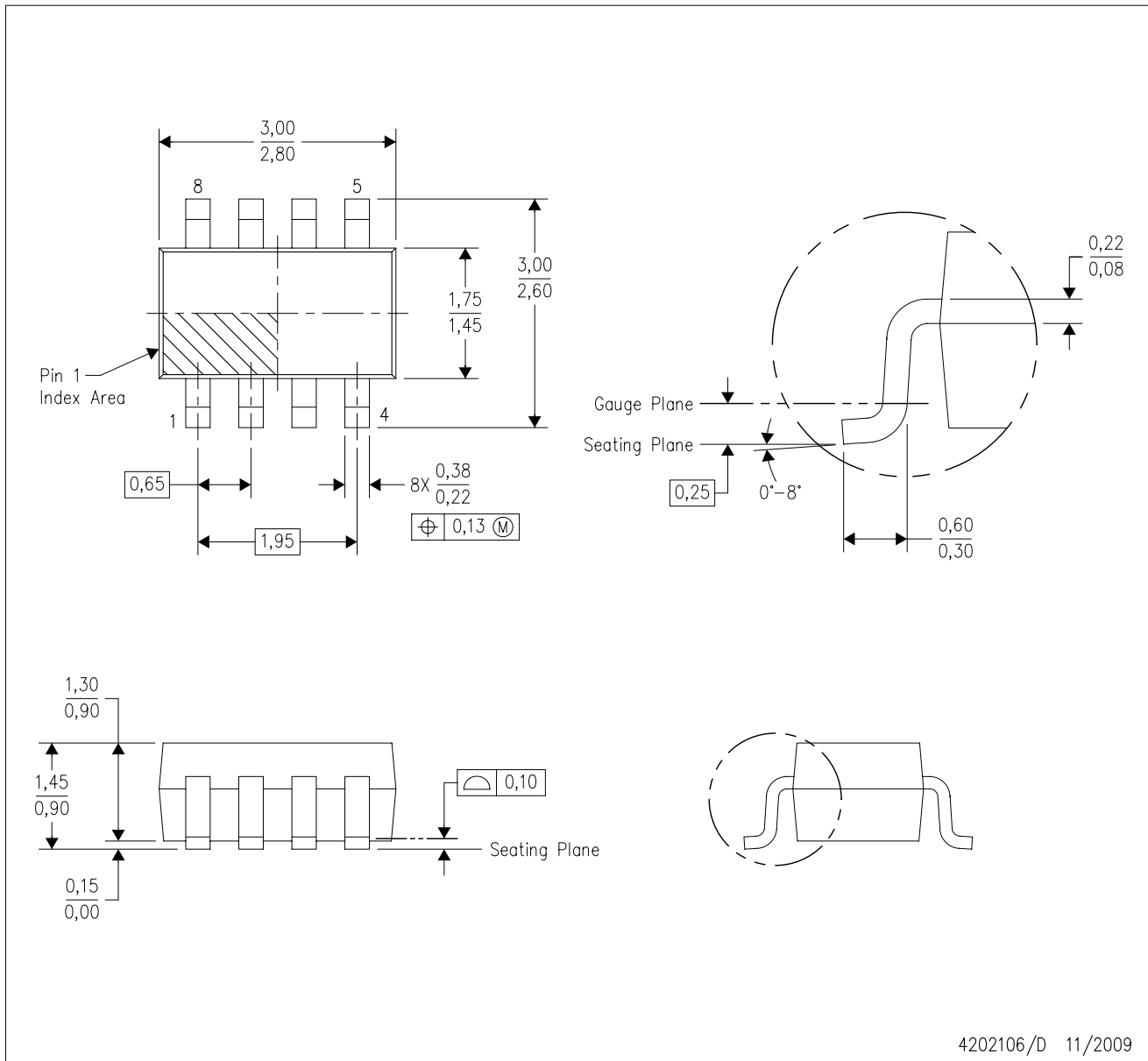
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
 - D. Package outline inclusive of solder plating.
 - E. A visual index feature must be located within the Pin 1 index area.
 - F. Falls within JEDEC MO-178 Variation BA.
 - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

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