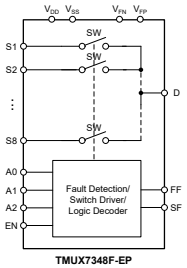
TMUX7348F-EP ±60V 耐圧、ラッチアップ耐性、 故障保護、エンハンスド製品、可変故障スレッショルドを備えた 8 : 1 マルチプレクサ

1 特長

- VID V62/24625
- 防衛、航空宇宙、および医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一の製造、アセンブリ、テスト施設
  - 軍用温度範囲:–55℃～125℃ T_A
  - 長期にわたる製品ライフ サイクル
- 幅広い電源電圧範囲:
  - デュアル電源:±5V～±22V
  - シングル電源:8V～44V
- フォルト保護機能を搭載:
  - 過電圧保護、ソース - 電源間またはソース - ドレイン間:±85V
  - 過電圧保護:±60V
  - 電源オフ保護:±60V
  - 調整可能な過電圧トリガ スレッショルド
    - V_{FP}:3V～V_{DD}、V_{FN}:0V～V_{SS}
  - 全体および特定のフォルト チャネル情報を示す割り込みフラグ
  - 障害が発生していないチャネルは低リーク電流で動作を維持
- デバイス構造に基づくラッチアップ耐性
- 1.8V ロジック対応
- フェイルセーフ ロジック:電源から独立して最大 44V
- ブレイク ビフォー メイクのスイッチング動作
- 業界標準の TSSOP パッケージ

2 アプリケーション

- 航空機のコックピット・ディスプレイ
- 飛行制御ユニット
- レーダー
- ソナー
- 電子戦
- 追尾フロント・エンド



機能ブロック図

3 概要

TMUX7348F-EP は現代的な CMOS (Complementary Metal-Oxide Semiconductor) アナログ マルチプレクサで、8:1 (シングル エンド) 構成です。本デバイスはデュアル電源 (±5V～±22V)、シングル電源 (8V～44V)、または非対称電源 (V_{DD} = 12V、V_{SS} = -5V など) で適切に動作します。過電圧保護機能は、電源供給および電源オフの状況で利用できるため、TMUX7348F-EP は、電源シーケンスを正確に制御できないアプリケーションに最適です。

本デバイスは、電源オンと電源オフのどちらの状態でも、グランドに対して +60V および -60V までのフォルト電圧を阻止します。電源を喪失した場合、スイッチの入力状態やロジックの制御ステータスに関係なく、スイッチ チャネルはオフ状態を維持します。通常動作状態では、いずれかの Sx ピンのアナログ入力信号レベルが正のフォルト電源電圧 (V_{FP}) または負のフォルト電源電圧 (V_{FN}) よりもスレッショルド電圧 (V_T) だけ上回ると、チャネルはオフになり、Sx ピンは高インピーダンスになります。フォルト チャネルを選択している場合、ドレイン ピン (D または Dx) は、フォルト電源電圧 (V_{FP} または V_{FN}) にプルされます。このデバイスには 2 つのアクティブ LOW 割り込みフラグ (FF および SF) があり、フォルトの詳細が示されています。FF フラグは、いずれかのソース入力でフォルト状態が発生しているかどうかを示します。一方、SF フラグはどの特定の入力でフォルト状態が発生しているかをデコードするために使用します。

低静電容量、低電荷注入、フォルト保護内蔵により、TMUX7348F-EP は、高性能と高堅牢性の両方が重要なフロント エンド データ アクイジション アプリケーションで使用できます。

パッケージ情報

部品番号 (1)	パッケージ (2)	パッケージ サイズ(4)
TMUX7348F-EP	PW (TSSOP、20)(3)	6.5mm × 4.4mm

(1) セクション 4 を参照してください。
(2) 詳細については、セクション 12 を参照してください。
(3) 開発中パッケージです。
(4) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX7348F-EP	+60V/ –60V Tolerant, Fault-protected, Latch-up Immune, Enhanced Product, 8:1 Multiplexers with Adjustable Fault Threshold

5 Pin Configuration and Functions

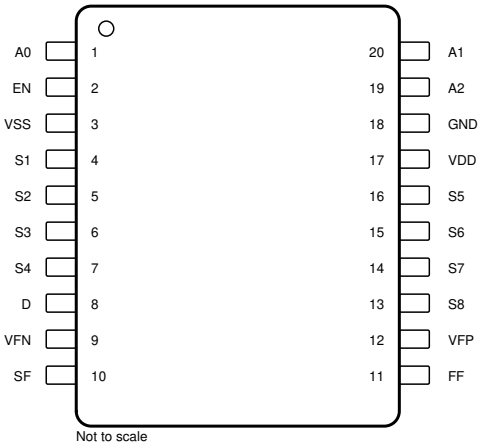

図 5-1. PW Package, 20-Pin TSSOP (Top View)

表 5-1. Pin Functions: TMUX7348F-EP

PIN		TYPE[1]	DESCRIPTION
NAME	NO.[2]		
A0	1	I	Logic control input address 0 (A0). The pin has a 4 MΩ internal pull-down resistor. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault. See セクション 8.4.3 for more details.
A1	20	I	Logic control input address 1 (A1). The pin has a 4 MΩ internal pull-down resistor. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault. See セクション 8.4.3 for more details.
A2	19	I	Logic control input address 2 (A2). The pin has a 4 MΩ internal pull-down resistor. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault. See セクション 8.4.3 for more details.
D	8	I/O	Drain pin. Can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range.
EN	2	I	Active high logic enable (EN) pin. The pin has a 4 MΩ internal pull-down resistor. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states. See セクション 8.4.3 for more details.
FF	11	O	General fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on any of the source (Sx) input pins. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1 kΩ pull-up resistor.
GND	18	P	Ground (0 V) reference
S1	4	I/O	Overvoltage protected source pin 1. Can be an input or output.
S2	5	I/O	Overvoltage protected source pin 2. Can be an input or output.
S3	6	I/O	Overvoltage protected source pin 3. Can be an input or output.
S4	7	I/O	Overvoltage protected source pin 4. Can be an input or output.
S5	16	I/O	Overvoltage protected source pin 5. Can be an input or output.
S6	15	I/O	Overvoltage protected source pin 6. Can be an input or output.
S7	14	I/O	Overvoltage protected source pin 7. Can be an input or output.
S8	13	I/O	Overvoltage protected source pin 8. Can be an input or output.
SF	10	O	Specific fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on a specific pin, depending on the state of A0, A1, and A2 , as shown in 表 8-1. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1 kΩ pull-up resistor.
V_{DD}	17	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
V_{FN}	9	P	Negative fault voltage supply that determines the overvoltage protection triggering threshold on the negative side. Connect to V_{SS} if the triggering threshold is to be the same as the device's negative supply. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{FN} and GND.
V_{FP}	12	P	Positive fault voltage supply that determines the overvoltage protection triggering threshold on the positive side. Connect to V_{DD} if the triggering threshold is to be the same as the device's positive supply. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{FP} and GND.
V_{SS}	3	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.

(1) I = input, O = output, I/O = input and output, P = power
(2) Preview package

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		48	V
V_{DD} to GND		–0.3	48	V
V_{SS} to GND		–48	0.3	V
V_{FP} to GND	Positive fault clamping voltage	–0.3	V_{DD} + 0.3	V
V_{FN} to GND	Negative fault clamping voltage	V_{SS} – 0.3	0.3	V
V_S to GND	Source input pin (Sx) voltage to GND	–65	65	V
V_S to V_{DD}	Source input pin (Sx) voltage to V_{DD}	–90		V
V_S to V_{SS}	Source input pin (Sx) voltage to V_{SS}		90	V
V_D	Drain pin (D or Dx) voltage	V_{FN}–0.7	V_{FP}+0.7	V
V_{EN} or V_{Ax}	Logic control input pin voltage (EN, A0, A1, A2)(2)	GND –0.7	48	V
V_{xF}	Logic output pin (SF, FF) voltage(2)	GND –0.7	6	V
I_{EN} or I_{Ax}	Logic control input pin current (EN, A0, A1, A2)(2)	–30	30	mA
I_{xF}	Logic output pin (SF, FF) current(2)	–10	10	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx or D)	I_{DC} ± 10 %(3)	I_{DC} ± 10 %(3)	mA
T_{stg}	Storage temperature	–65	150	°C
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C
P_{tot} (4)	Total power dissipation		800	mW

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Stresses have to be kept at or below both voltage and current ratings at all time.
(3) Refer to Recommended Operating Conditions for I_{DC} ratings.
(4) For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 12.0 mW/°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

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6.3 Thermal Information

THERMAL METRIC[1]		TMUX7348F-EP PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential		8		44	V
V_{DD}	Positive power supply voltage		5		44	V
V_{FP}	Positive fault clamping voltage		3		V_{DD}	V
V_{FN}	Negative fault clamping voltage		V_{SS}		0	V
V_S	Source pin (Sx) voltage (non-fault condition)		V_{FN}		V_{FP}	V
V_S to GND	Source pin (Sx) voltage (fault condition)		–60		60	V
V_S to V_{DD} (2)	Source pin (Sx) voltage to V_{DD} or V_D (fault condition)	Source pin (Sx) voltage to V_{DD} or V_D (fault condition)	–85			V
V_S to V_{SS} (2)	Source pin (Sx) voltage to V_{SS} or V_D (fault condition)	Source pin (Sx) voltage to V_{SS} or V_D (fault condition)			85	V
V_D	Drain pin (D, Dx) voltage		V_{FN}		V_{FP}	V
V_{EN} or V_{Ax}	Logic control input pin voltage (EN, A0, A1, A2)		0		44	V
V_{xF}	Logic output pin (SF, FF) voltage		0		5.5	V
T_A	Ambient temperature		–55		125	°C
I_{DC} (3)	Continuous current through switch	T_A = 25°C			9	mA
		T_A = 85°C			6.5	
		T_A = 125°C			5	

(1) V_{DD} and V_{SS} can be any value as long as 8V ≤ (V_{DD} – V_{SS}) ≤ 44V.
(2) Under a fault condition, the potential difference between source pin (Sx) and supply pins (V_{DD} and V_{SS}.) or source pin (Sx) and drain pins (D, Dx) may not exceed 85V.
(3) Fault supplies are tied to the primary supplies (V_{FP}= V_{DD}, V_{FN} = V_{SS})

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6.5 Electrical Characteristics (Global)

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_T	Threshold voltage for fault detector		–55°C to +125°C		0.7		V
LOGIC INPUT/ OUTPUT							
V_{IH}	High-level input voltage	EN, Ax pins	–55°C to +125°C	1.3		44	V
V_{IL}	Low-level input voltage	EN, Ax pins	–55°C to +125°C	0		0.8	V
$V_{OL(FLAG)}$	Low-level output voltage	FF and SF pins, I_O = 5mA	–55°C to +125°C			0.35	V
POWER SUPPLY							
V_{UVLO}	Undervoltage lockout (UVLO) threshold voltage (V_{DD} – V_{SS})	Rising edge, single supply	–55°C to +125°C	5.1	6	6.4	V
		Falling edge, single supply	–55°C to +125°C	5	5.8	6.3	V
V_{HYS}	V_{DD} Undervoltage lockout (UVLO) hysteresis	Single supply	–55°C to +125°C		0.2		V
$R_{D(OVP)}$	Drain resistance to supply rail during overvoltage event on selected source pin		25°C		40		kΩ

6.6 ±15V Dual Supply: Electrical Characteristics

V_{DD} = +15V ± 10%, V_{SS} = –15V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10V to +10V, I_S = –1mA	25°C		180	250	Ω
			–40°C to +85°C			330	
			–55°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10V to +10V, I_S = –1mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–55°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = –10V to +10V, I_S = –1mA	25°C		1.5	3.5	Ω
			–40°C to +85°C			4	
			–55°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0V, I_S = –1mA	–55°C to +125°C		1.2		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–55°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–55°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is on V_S = V_D = ±10V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–55°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = ± 60V, GND = 0V, V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V	–55°C to +125°C		±110		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0V	–55°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	–55°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60V, GND = 0V, V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, –15.5V ≤ V_D ≤ 16.5V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–55°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–55°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–55°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2	± 0.6	2	µA
			–55°C to +125°C	–2		2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0V	25°C	–1.1	± 0.6	1.1	µA
			–55°C to +125°C	–1.2		1.2	
SWITCHING CHARACTERISTICS							
$t_{ON\ (EN)}$	Enable turn-on time	V_S = 10V, R_L = 4kΩ, C_L= 12pF	25°C		165	265	ns
			–40°C to +85°C			285	
			–55°C to +125°C			330	

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6.6 ±15V Dual Supply: Electrical Characteristics (続き)

V_{DD} = +15V ± 10%, V_{SS} = –15V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{OFF\ (EN)}$	Enable turn-off time	V_S = 10V, R_L = 4kΩ, C_L= 12pF	25°C		350	400	ns
			–40°C to +85°C			400	
			–55°C to +125°C			440	
t_{TRAN}	Transition time	V_S = 10V, R_L = 4kΩ, C_L= 12pF	25°C		170	225	ns
			–40°C to +85°C			245	
			–55°C to +125°C			285	
$t_{RESPONSE}$	Fault response time	V_{FP} = 15V, V_{FN} = –15V, R_L = 4kΩ, C_L= 12pF	25°C		300		ns
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 15V, V_{FN} = –15V, R_L = 4kΩ, C_L= 12pF	25°C		1.4		µs
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 15V, V_{FN} = –15V, V_{PU} = 5V, R_{PU} = 1kΩ, C_L= 12pF	25°C		110		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 15V, V_{FN} = –15V, V_{PU} = 5V, R_{PU} = 1kΩ, C_L= 12pF	25°C		0.9		µs
t_{BBM}	Break-before-make time delay	V_S = 10V, R_L = 4kΩ, C_L= 12pF	–55°C to +125°C	50	120		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1nF	25°C		–15		pC
O_{ISO}	Off-isolation	R_S = 50Ω, R_L = 50Ω, C_L = 5pF, V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 1MHz	25°C		–82		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50Ω, R_L = 50Ω, C_L = 5pF, V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 1MHz	25°C		–95		dB
BW	–3dB bandwidth	R_S = 50Ω, R_L = 50Ω, C_L = 5pF, V_S = 200mV_{RMS}, V_{BIAS} = 0V	25°C		150		MHz
I_{LOSS}	Insertion loss	R_S = 50Ω, R_L = 50Ω, C_L = 5pF, V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 1MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40Ω, R_L = 10kΩ, V_S = 15 V_{PP}, V_{BIAS} = 0V, f = 20Hz to 20kHz	25°C		0.0014		%
$C_{S(OFF)}$	Input off-capacitance	f = 1MHz, V_S = 0V	25°C		3.5		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1MHz, V_S = 0V	25°C		28		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1MHz, V_S = 0V	25°C		30		pF

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6.6 ±15V Dual Supply: Electrical Characteristics (続き)

V_{DD} = +15V ± 10%, V_{SS} = –15V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		0.24	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		0.14	0.4	mA
			–40°C to +85°C			0.4	
			–55°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		0.075		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60V, V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–55°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60V, V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60V, V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		0.15		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = ± 60V, V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		9		µA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = ± 60V, V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 5V or V_{DD}	25°C		9		µA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 0V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = V_{FP} = 16.5V, V_{SS} = V_{FN} = –16.5V, V_{Ax} = 0V, 5V, or V_{DD}, V_{EN} = 0V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–55°C to +125°C			0.4	

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

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6.7 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V, I_S = –1 mA	25°C		180	250	Ω
			–40°C to +85°C			330	
			–55°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V, I_S = –1 mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–55°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = –15 V to +15 V, I_S = –1 mA	25°C		8	10	Ω
			–40°C to +85°C			12	
			–55°C to +125°C			12	
R_{FLAT}	On-resistance flatness	V_S = –13.5 V to +13.5 V, I_S = –1 mA	25°C		1.5	3.5	Ω
			–40°C to +85°C			4	
			–55°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –1 mA	–55°C to +125°C		1.2		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–55°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–55°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–55°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V	–55°C to +125°C		±95		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V	–55°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	–55°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V –21V ≤ V_D ≤ 22V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–55°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–55°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–55°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2.2	± 0.6	2.2	µA
			–55°C to +125°C	–2.2		2.2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–1.1	± 0.6	1.1	µA
			–55°C to +125°C	–1.2		1.2	

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6.7 ±20 V Dual Supply: Electrical Characteristics (続き)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		175	300	ns
			–40°C to +85°C			325	
			–55°C to +125°C			380	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		350	400	ns
			–40°C to +85°C			400	
			–55°C to +125°C			445	
t_{TRAN}	Transition time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		170	245	ns
			–40°C to +85°C			270	
			–55°C to +125°C			315	
$t_{RESPONSE}$	Fault response time	V_{FP} = 20 V, V_{FN} = –20 V, R_L = 4 kΩ, C_L= 12 pF	25°C		300		ns
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 20 V, V_{FN} = –20 V, R_L = 4 kΩ, C_L= 12 pF	25°C		1.3		µs
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 20 V, V_{FN} = –20 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		110		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 20 V, V_{FN} = –20 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		0.9		µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C	50	120		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF	25°C		–17		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–85		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–95		dB
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V	25°C		150		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10k Ω, V_S = 20 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20k Hz	25°C		0.0014		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		3.5		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 0 V	25°C		28		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 0 V	25°C		30		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.24	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.14	0.4	mA
			–40°C to +85°C			0.4	
			–55°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.075		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–55°C to +125°C			1	

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6.7 ±20 V Dual Supply: Electrical Characteristics (続き)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		9		µA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		9		µA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	mA
			–55°C to +125°C			0.5	mA
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	mA
			–55°C to +125°C			0.4	mA

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

6.8 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		180	250	Ω
			–40°C to +85°C			330	
			–55°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–55°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		7	30	Ω
			–40°C to +85°C			45	
			–55°C to +125°C			75	
R_{FLAT}	On-resistance flatness	V_S = 1 V to 7.8 V, I_S = –1 mA	25°C		1.5	7	Ω
			–40°C to +85°C			8	
			–55°C to +125°C			8	
R_{ON_DRIFT}	On-resistance drift	V_S = 6 V, I_S = –1 mA	–55°C to +125°C		1.2		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–55°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–55°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–55°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V	–55°C to +125°C		±145		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V	–55°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	–55°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V 1V ≤ V_D ≤ 13.2V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–55°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–55°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–55°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2	± 0.6	2	µA
			–55°C to +125°C	–2		2	µA
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–1.1	± 0.6	1.1	µA
			–55°C to +125°C	–1.2		1.2	

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6.8 12 V Single Supply: Electrical Characteristics (続き)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		160	265	ns
			–40°C to +85°C			285	
			–55°C to +125°C			330	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		420	485	ns
			–40°C to +85°C			485	
			–55°C to +125°C			545	
t_{TRAN}	Transition time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		160	215	ns
			–40°C to +85°C			230	
			–55°C to +125°C			270	
$t_{RESPONSE}$	Fault response time	V_{FP} = 12 V, V_{FN} = 0 V, R_L = 4 kΩ, C_L= 12 pF	25°C		220		ns
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 12 V, V_{FN} = 0 V, R_L = 4 kΩ, C_L= 12 pF	25°C		0.69		µs
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 12 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		110		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 12 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		0.65		µs
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C	30	100		ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 1 nF	25°C		–11		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–76		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–93		dB
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V	25°C		130		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10k Ω, V_S = 6 V_{PP}, V_{BIAS} = 6 V, f = 20 Hz to 20k Hz	25°C		0.0022		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V	25°C		4		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 6 V	25°C		31		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 6 V	25°C		34		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.24	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.14	0.4	mA
			–40°C to +85°C			0.4	
			–55°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.075		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–55°C to +125°C			1	

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6.8 12 V Single Supply: Electrical Characteristics (続き)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.17		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		9		µA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		7.5		µA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–55°C to +125°C			0.4	

(1) When V_S is 10 V, V_D is 1 V. Or when V_S is 1 V, V_D is 10 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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6.9 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 28 V, I_S = –1 mA	25°C		180	250	Ω
			–40°C to +85°C			330	
			–55°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 28 V, I_S = –1 mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–55°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 30 V, I_S = –1 mA	25°C		8	65	Ω
			–40°C to +85°C			75	
			–55°C to +125°C			90	
R_{FLAT}	On-resistance flatness	V_S = 1 V to 28 V, I_S = –1 mA	25°C		1.5	3	
			–40°C to +85°C			4	
			–55°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 18 V, I_S = –1 mA	–55°C to +125°C		1.2		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–55°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current[2]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–55°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is on V_S = V_D = 30 V or 1 V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–55°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current durring overvoltage	V_S = 60 / –40 V, GND = 0V V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V	–55°C to +125°C		±110		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0V V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V	–55°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0V V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	–55°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = 60 / –40 V, GND = 0V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V 1V ≤ V_D ≤ 39.6V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–55°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–55°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–55°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–3.2	± 0.6	3.2	µA
			–55°C to +125°C	–3.2		3.2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–1.1	± 0.6	1.1	µA
			–55°C to +125°C	–1.2		1.2	

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6.9 36 V Single Supply: Electrical Characteristics (続き)

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	25°C		185	390	ns
			–40°C to +85°C			460	
			–55°C to +125°C			530	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	25°C		380	450	ns
			–40°C to +85°C			450	
			–55°C to +125°C			490	
t_{TRAN}	Transition time	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	25°C		185	230	ns
			–40°C to +85°C			245	
			–55°C to +125°C			285	
$t_{RESPONSE}$	Fault response time	V_{FP} = 36 V, V_{FN} = 0 V, R_L = 4 kΩ, C_L= 12 pF	25°C		210		ns
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 36 V, V_{FN} = 0 V, R_L = 4 kΩ, C_L= 12 pF	25°C		0.67		µs
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 36 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		110		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 36 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		0.65		µs
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C	50	100		ns
Q_{INJ}	Charge injection	V_S = 18 V, C_L = 1 nF	25°C		–16		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–78		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–95		dB
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V	25°C		130		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10k Ω, V_S = 18 V_{PP}, V_{BIAS} = 18 V, f = 20 Hz to 20k Hz	25°C		0.0014		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 18 V	25°C		4		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 18 V	25°C		31		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 18 V	25°C		34		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.24	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.14	0.4	mA
			–40°C to +85°C			0.4	
			–55°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.075		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–55°C to +125°C			1	

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6.9 36 V Single Supply: Electrical Characteristics (続き)

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.12		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		9		µA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		7.5		µA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–55°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–55°C to +125°C			0.4	

(1) When V_S is 30 V, V_D is 1 V. Or when V_S is 1 V, V_D is 30 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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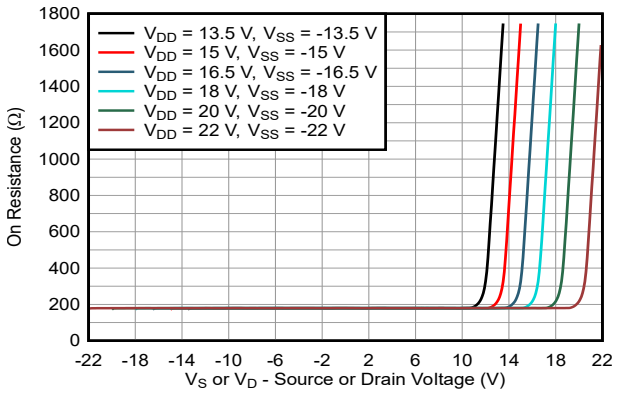
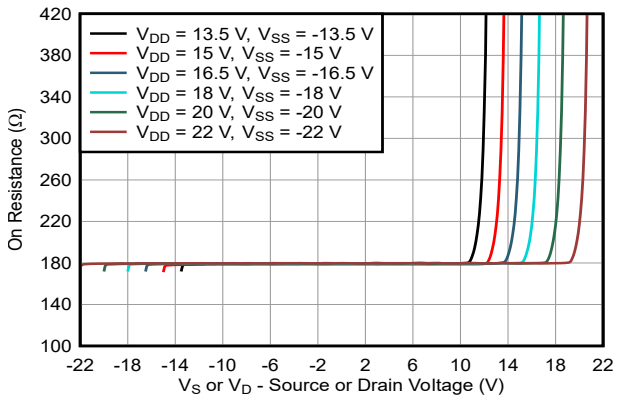
6.10 Typical Characteristics

at T_A = 25°C, V_{DD} = 15V, and V_{SS} = –15V (unless otherwise noted)



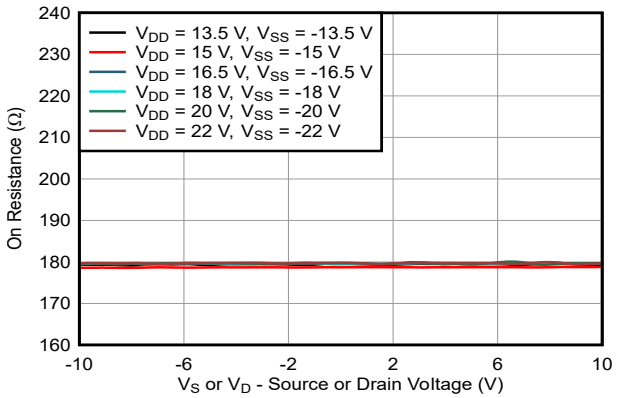
Dual Supply Voltages

図 6-1. On-Resistance vs Source or Drain Voltage



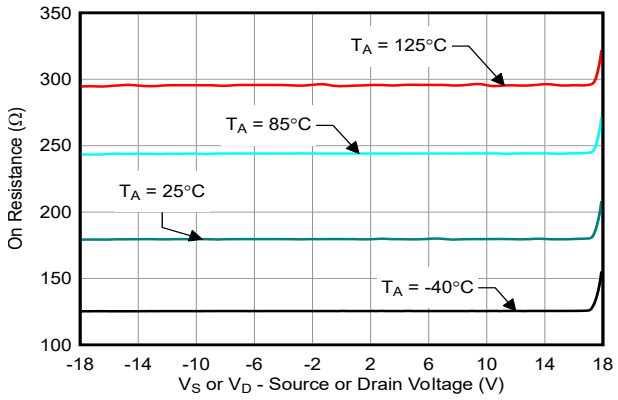
Dual Supply Flat R_{ON} Region

図 6-2. On-Resistance vs Source or Drain Voltage



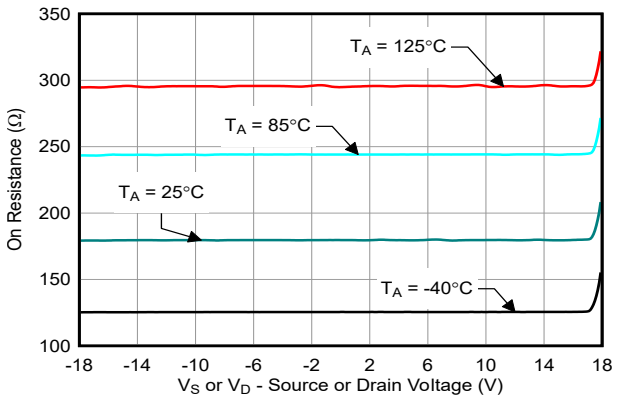
Flattest R_{ON} region for all supply voltages shown

図 6-3. On-Resistance vs Source or Drain Voltage



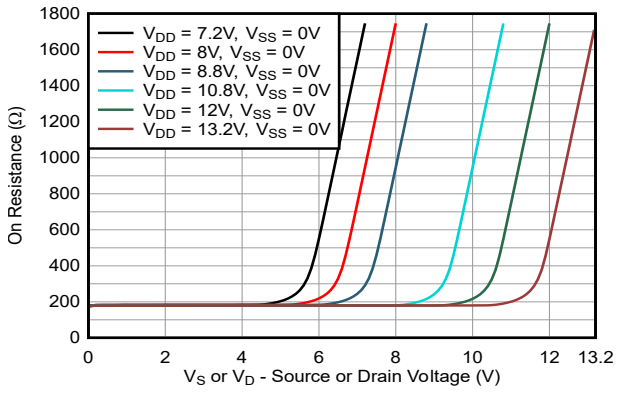
±15V Supply Flattest R_{ON} Region

図 6-4. On-Resistance vs Source or Drain Voltage



±20V Supply Flattest R_{ON} Region

図 6-5. On-Resistance vs Source or Drain Voltage



Single Supply Voltages

図 6-6. On-Resistance vs Source or Drain Voltage

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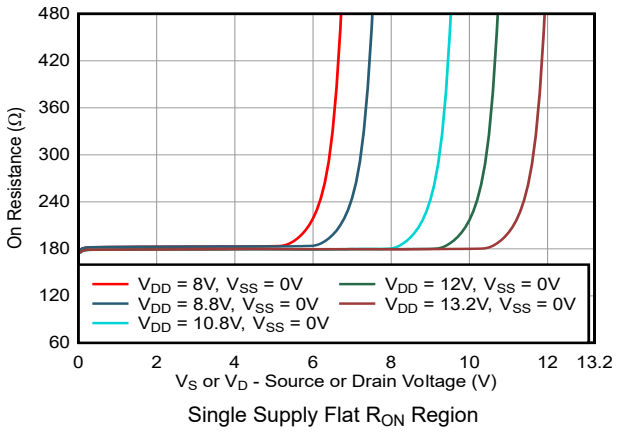
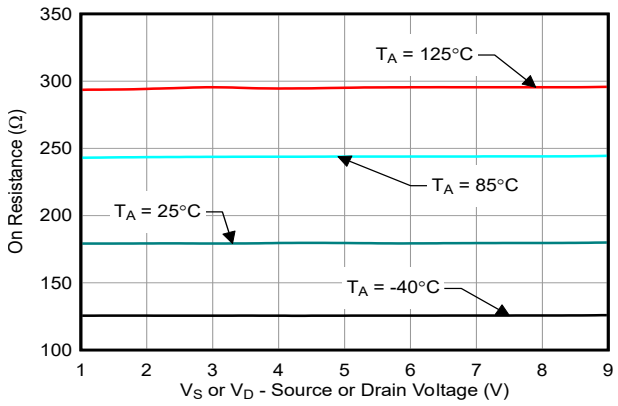
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15V, and V_{SS} = –15V (unless otherwise noted)



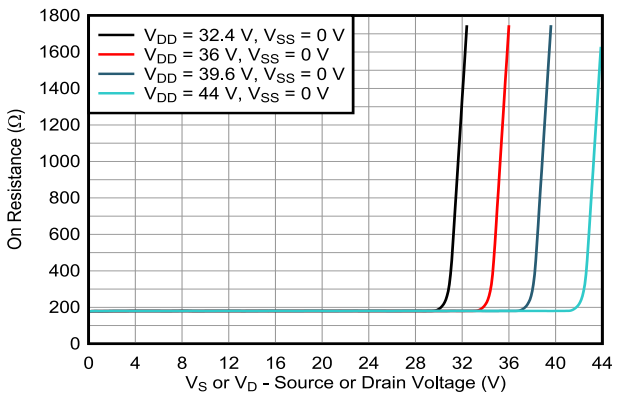
Single Supply Flat R_{ON} Region

図 6-7. On-Resistance vs Source or Drain Voltage



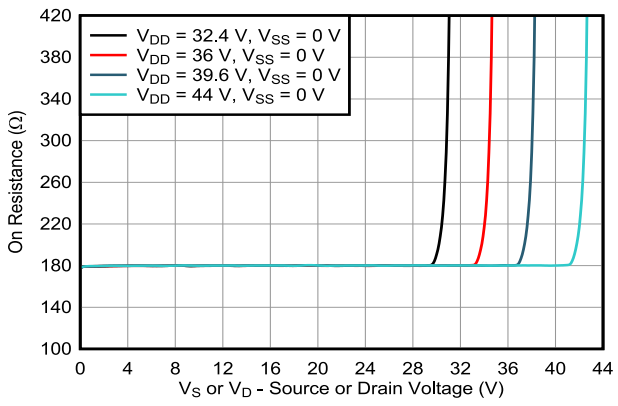
12V Supply Flattest R_{ON} Region

図 6-8. On-Resistance vs Source or Drain Voltage



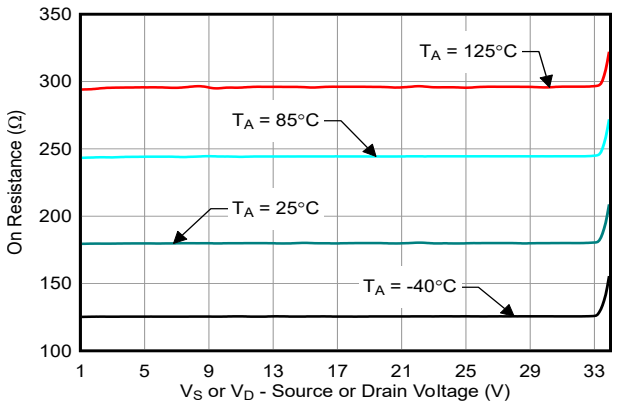
Single Supply Voltages

図 6-9. On-Resistance vs Source or Drain Voltage



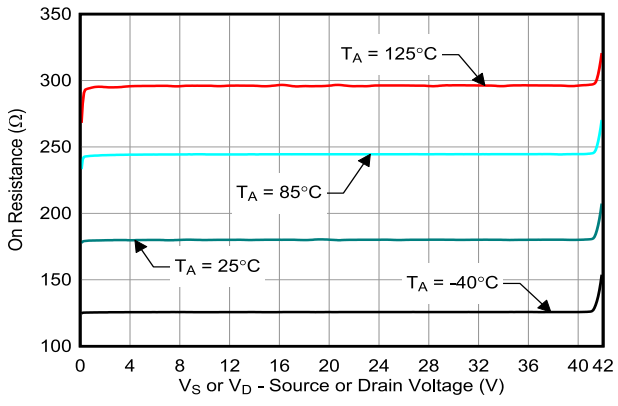
Single Supply Flat R_{ON} Region

図 6-10. On-Resistance vs Source or Drain Voltage



36V Supply Flattest R_{ON} Region

図 6-11. On-Resistance vs Source or Drain Voltage



44V Supply Flattest R_{ON} Region

図 6-12. On-Resistance vs Source or Drain Voltage

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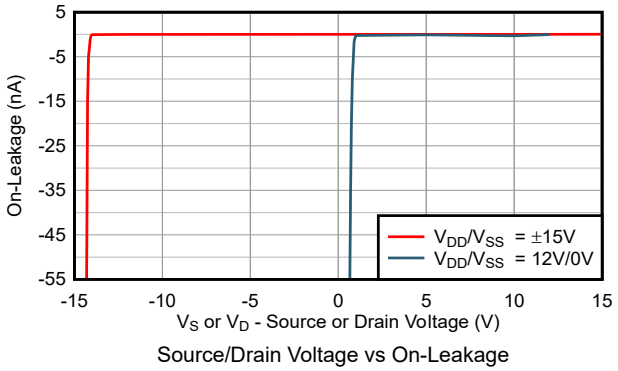
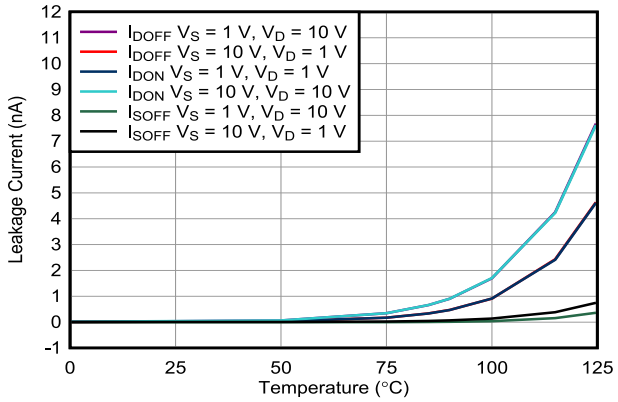
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15V, and V_{SS} = –15V (unless otherwise noted)



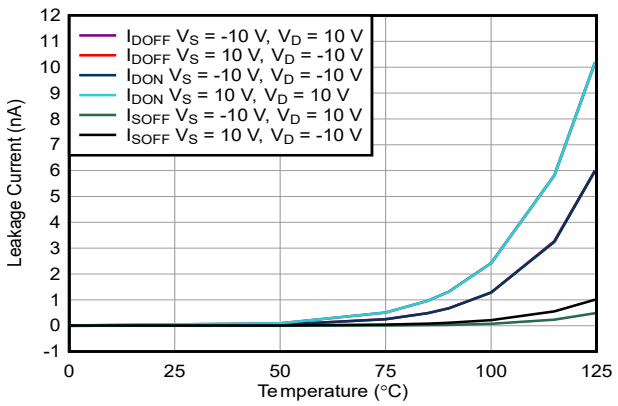
Source/Drain Voltage vs On-Leakage

図 6-13. Source or Drain Voltage vs On-Leakage



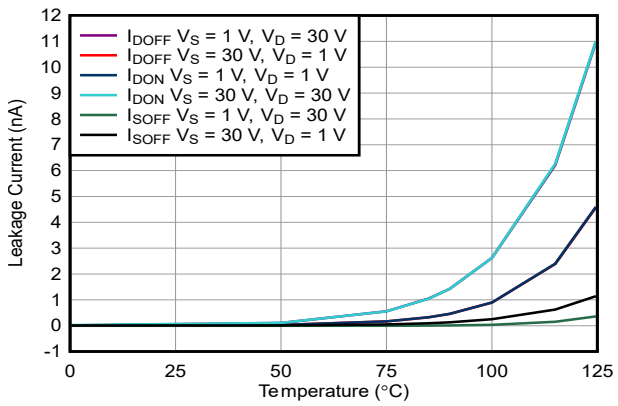
V_{DD} = 12V, V_{SS} = 0 V

図 6-14. Leakage Current vs Temperature



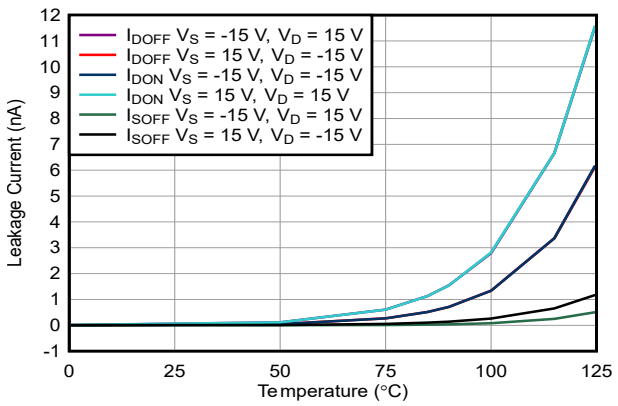
V_{DD} = 15V, V_{SS} = -15V

図 6-15. Leakage Current vs Temperature



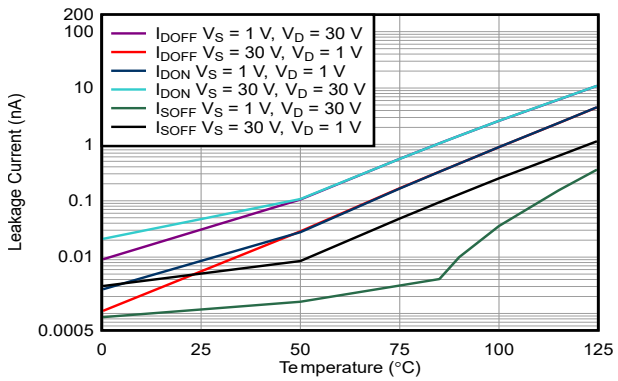
V_{DD} = 36V, V_{SS} = 0V

図 6-16. Leakage Current vs Temperature



V_{DD} = 20V, V_{SS} = -20V

図 6-17. Leakage Current vs Temperature



V_{DD} = 36V, V_{SS} = 0V

図 6-18. Leakage Current vs Temperature

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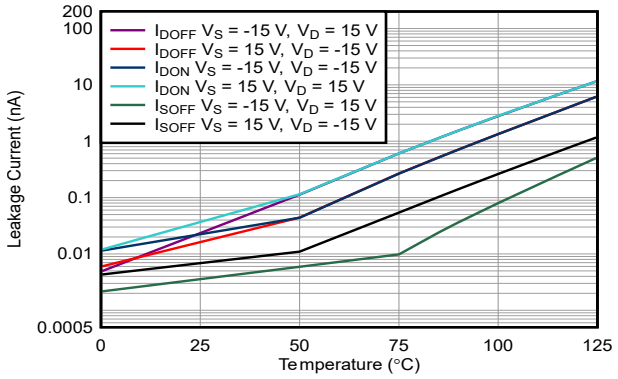
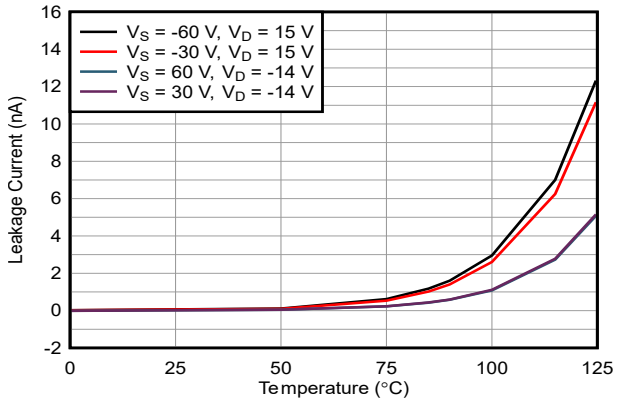
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15V, and V_{SS} = –15V (unless otherwise noted)



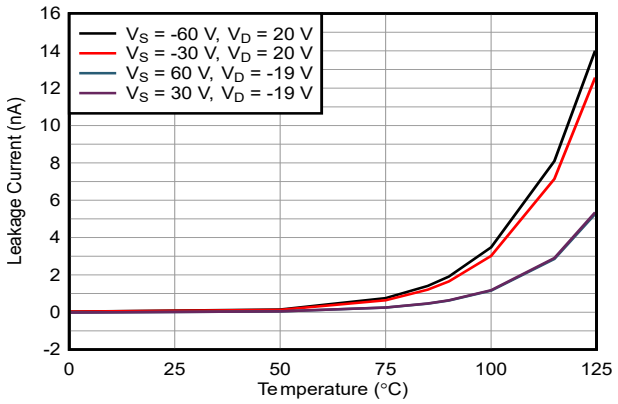
V_{DD} = 20V, V_{SS} = -20V

図 6-19. Leakage Current vs Temperature



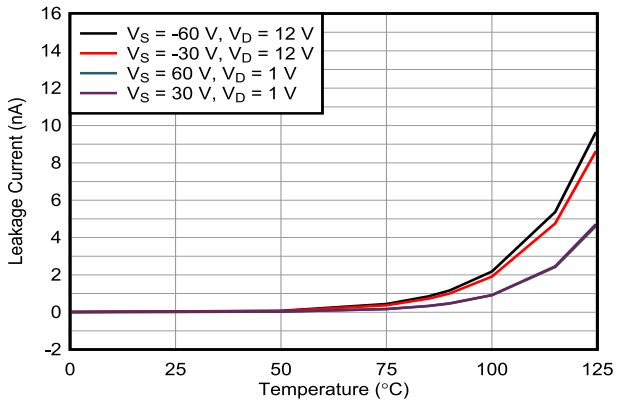
V_{DD} = 15V, V_{SS} = -15V

図 6-20. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



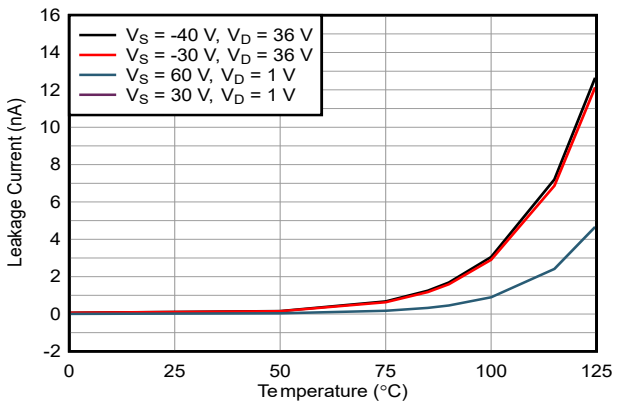
V_{DD} = 20V, V_{SS} = -20V

図 6-21. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



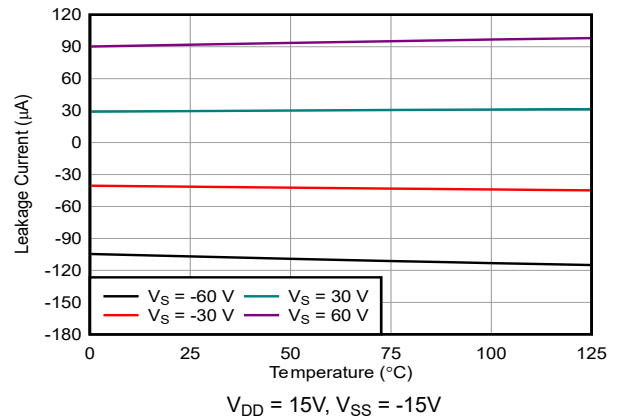
V_{DD} = 12V, V_{SS} = 0V

図 6-22. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



V_{DD} = 36V, V_{SS} = 0V

図 6-23. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



V_{DD} = 15V, V_{SS} = -15V

図 6-24. $I_{S(FA)}$ Overvoltage Leakage Current vs Temperature

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6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15V, and V_{SS} = –15V (unless otherwise noted)

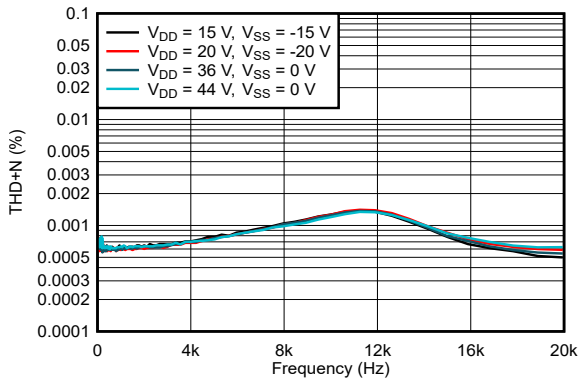

図 6-25. THD+N vs Frequency

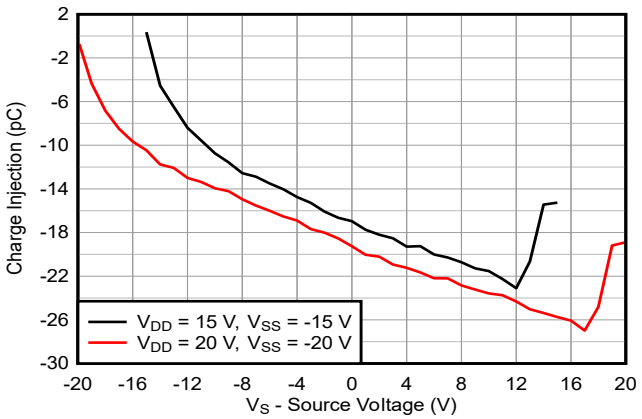

図 6-26. Charge Injection vs Source Voltage – Dual Supply

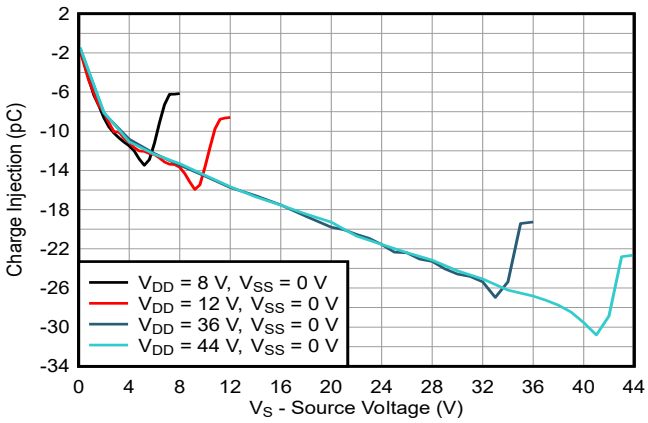

図 6-27. Charge Injection vs Source Voltage – Single Supply

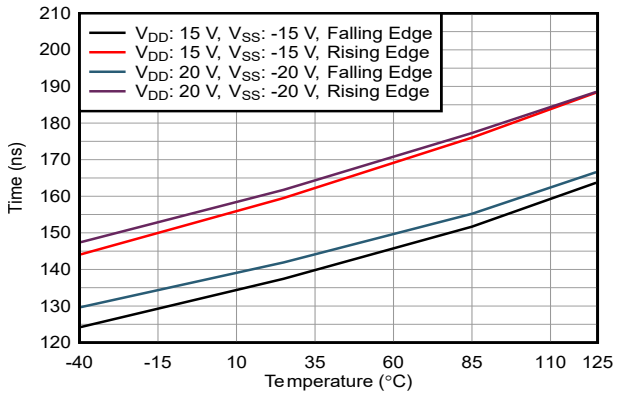

図 6-28. Transition Times vs Temperature

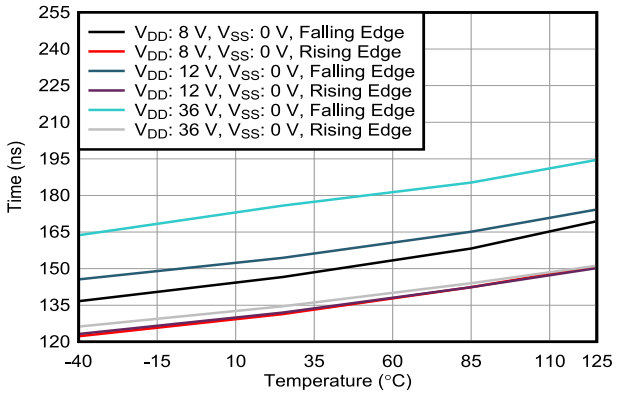

図 6-29. Transition Times vs Temperature

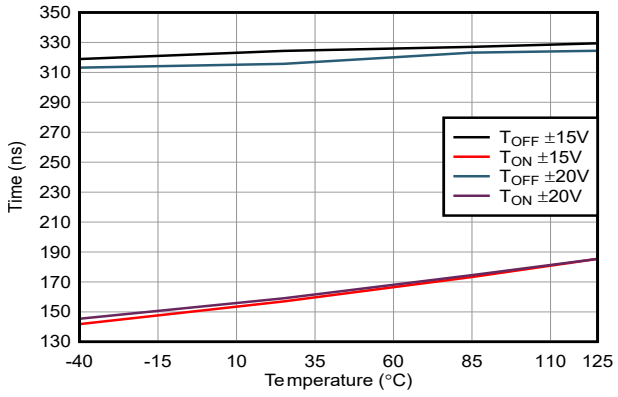

図 6-30. Turn-On and Turn-Off Times vs Temperature

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6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15V, and V_{SS} = –15V (unless otherwise noted)

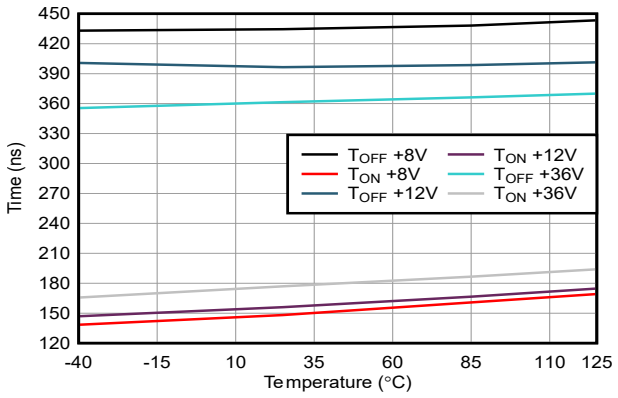

図 6-31. Turn-On and Turn-Off Times vs Temperature

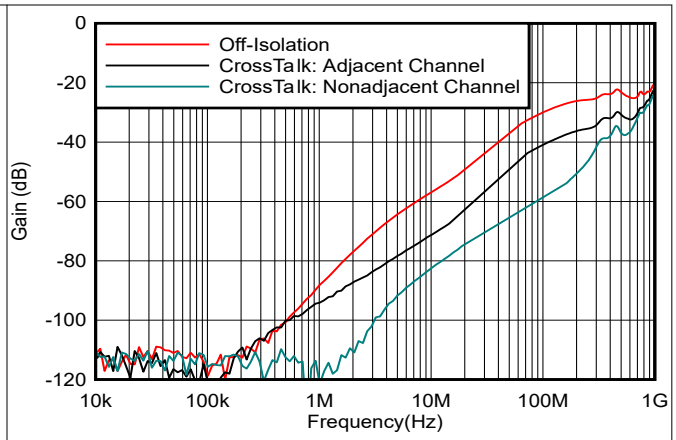

図 6-32. Off Isolation and Crosstalk vs Frequency

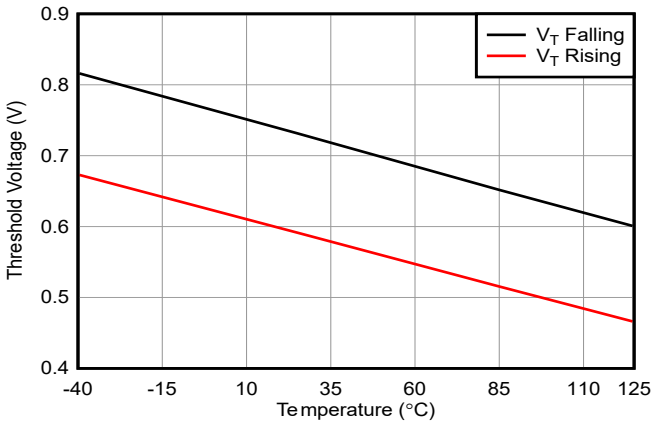

図 6-33. Threshold Voltage vs Temperature

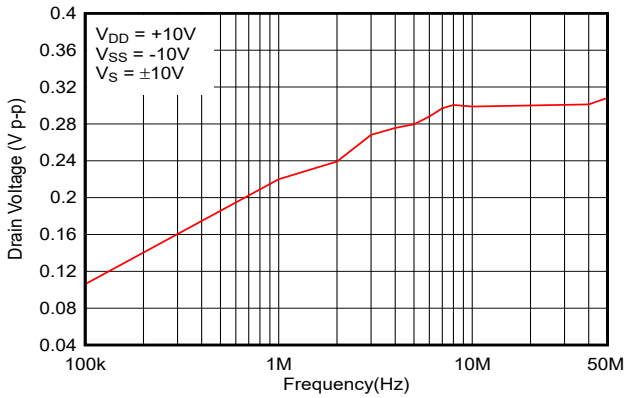

図 6-34. Large Signal Voltage Off Isolation vs Frequency

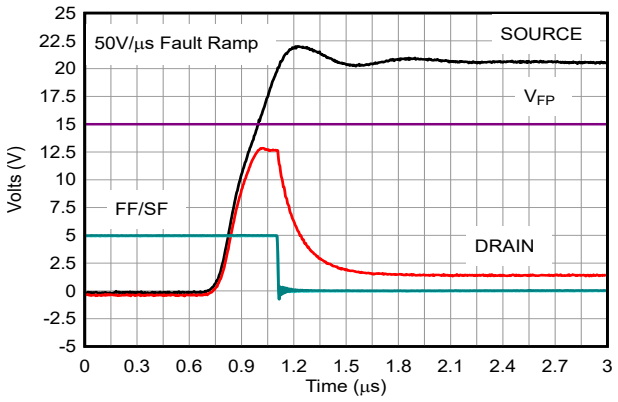

図 6-35. Drain Output Response – Positive Overvoltage

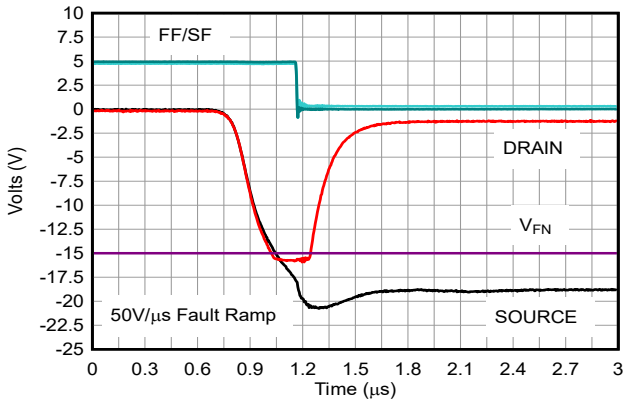

図 6-36. Drain Output Response – Negative Overvoltage

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15V, and V_{SS} = –15V (unless otherwise noted)

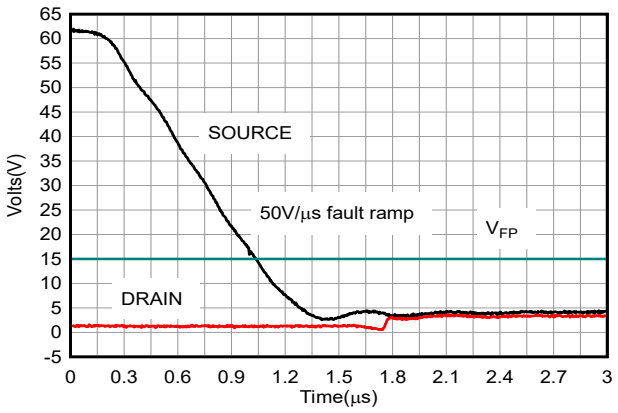

図 6-37. Drain Output Recovery – Positive Overvoltage

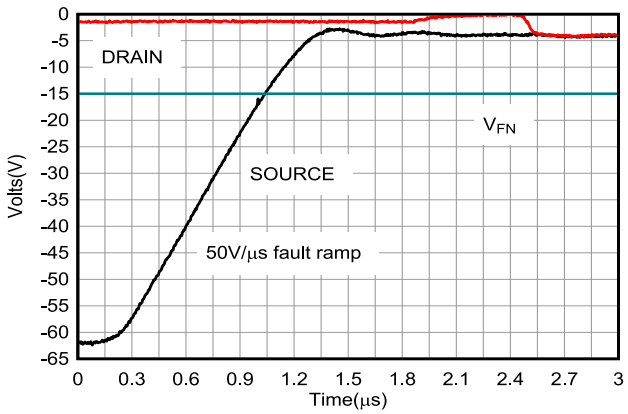

図 6-38. Drain Output Recovery – Negative Overvoltage

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7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of the TMUX7348F-EP is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 7-1. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

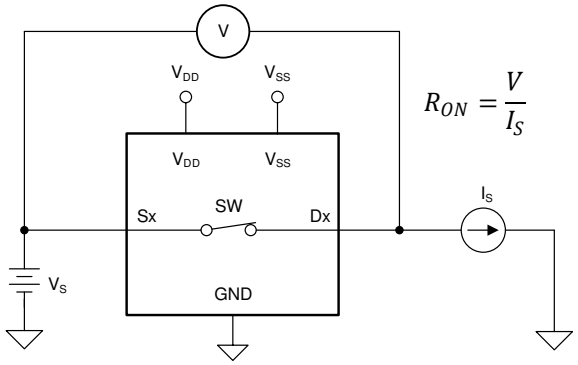

図 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

図 7-2 shows the setup used to measure both off-leakage currents.

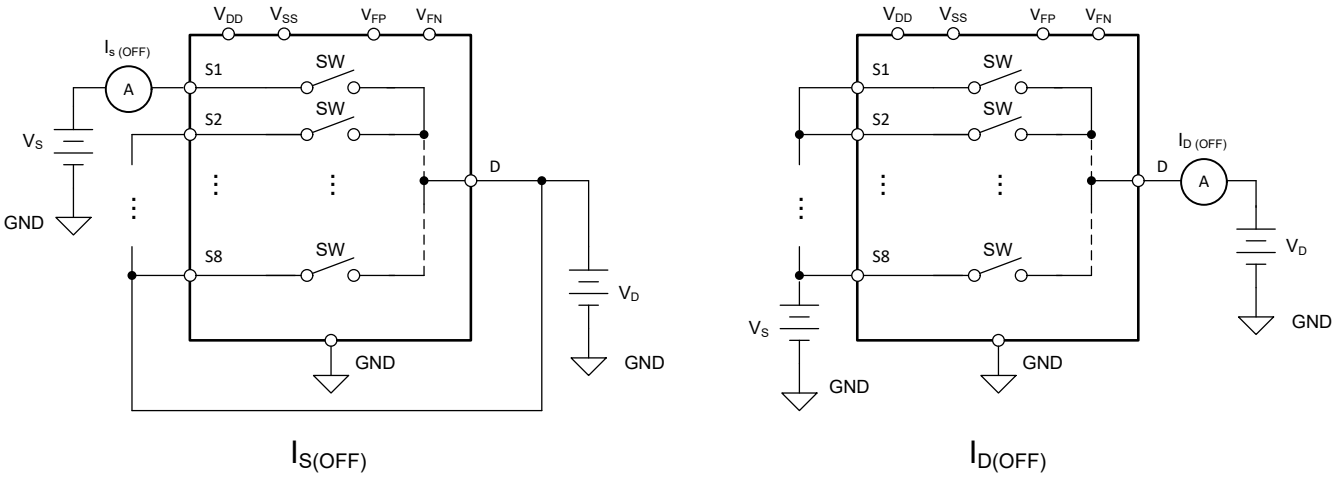

図 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. 図 7-3 shows the circuit used for measuring the on-leakage currents.

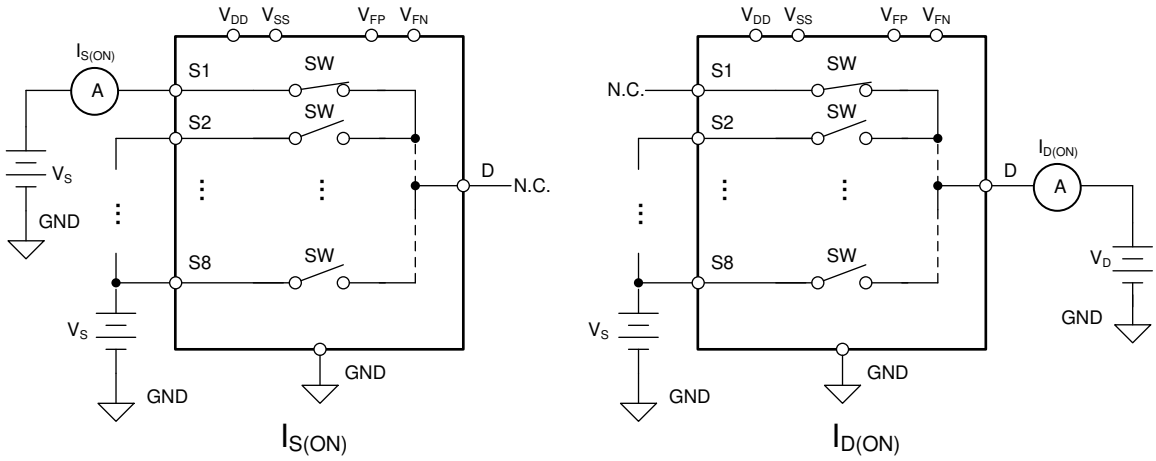

図 7-3. On-Leakage Measurement Setup

7.4 Input and Output Leakage Current Under Overvoltage Fault

If any of the source pin voltage goes above the fault supplies (V_{FP} or V_{FN}), the overvoltage protection feature of the TMUX7348F-EP is triggered to turn off the switch under fault, keeping the fault channel in high-impedance state. $I_{S(FA)}$ and $I_{D(FA)}$ denotes the input and output leakage current under overvoltage fault conditions, respectively. For $I_{D(FA)}$ the device is disabled to measure leakage current on the drain pin without being impacted by the 40 kΩ impedance to the fault supply. When the overvoltage fault occurs, the supply (or supplies) can either be in normal operating condition (図 7-4) or abnormal operating condition (図 7-5). During abnormal operating condition, the supply (or supplies) can either be unpowered (V_{DD}= V_{SS} = V_{FN} = V_{FP} = 0 V) or floating (V_{DD}= V_{SS} = V_{FN} = V_{FP} = No Connection), and remains within the leakage performance specifications.

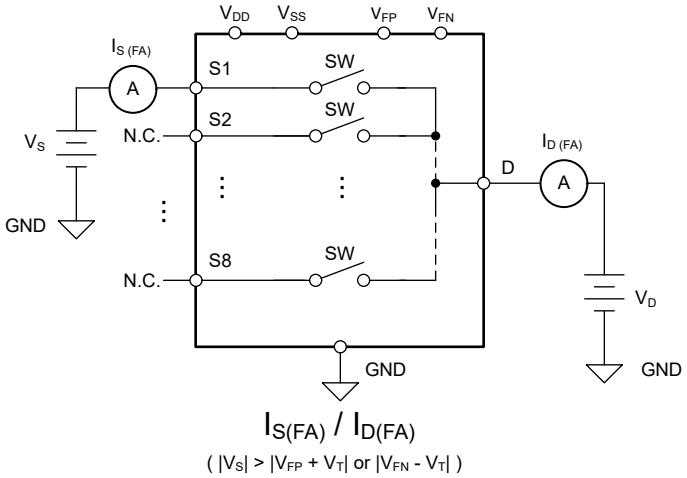

図 7-4. Measurement Setup for Input and Output Leakage Current under Overvoltage Fault with Normal Supplies

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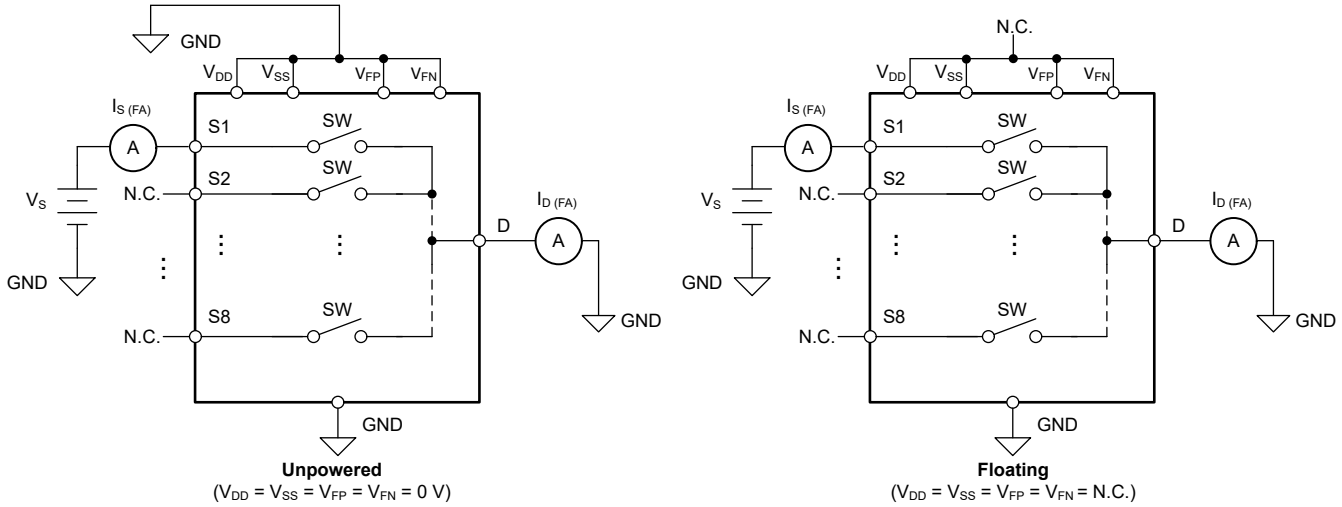

図 7-5. Measurement Setup for Input and Output Leakage Current Under Overvoltage Fault with Unpowered or Floating Supplies

7.5 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX7348F-EP. The ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. 図 7-6 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

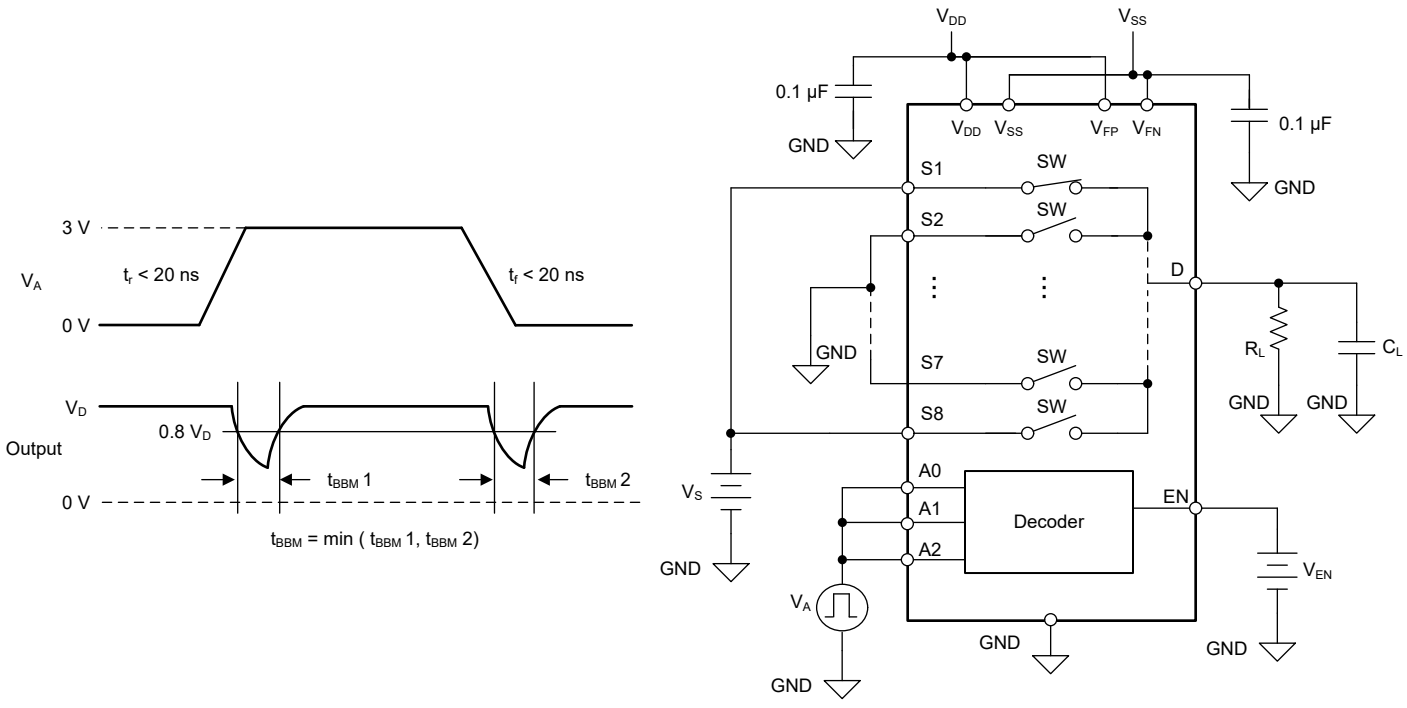

図 7-6. Break-Before-Make Delay Measurement Setup

7.6 Enable Delay Time

$t_{ON(EN)}$ time is defined as the time taken by the output of the TMUX7348F-EP to rise to a 90% final value after the EN signal has risen to a 50% final value. $t_{OFF(EN)}$ is defined as the time taken by the output of the TMUX7348F-EP to fall to a 10% initial value after the EN signal has fallen to a 50% initial value. 図 7-7 shows the setup used to measure the enable delay time.

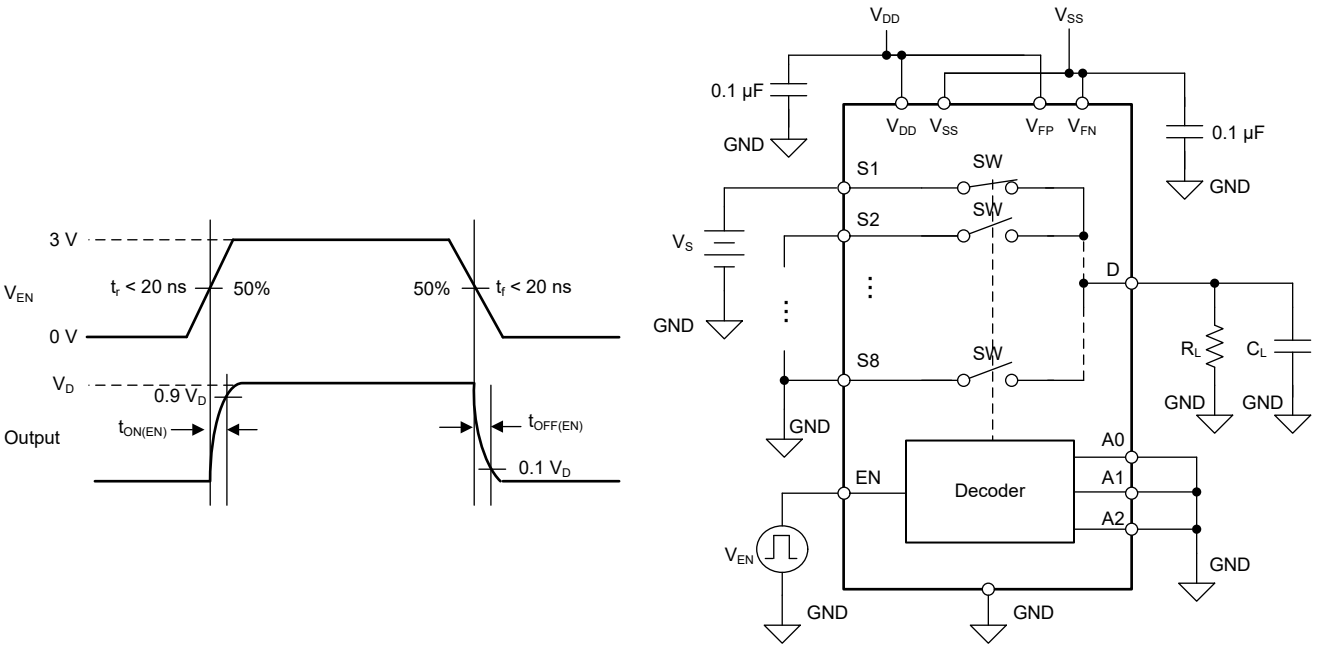

図 7-7. Enable Delay Measurement Setup

7.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the address signal (Ax) has fallen or risen to 50% of the transition. 図 7-8 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

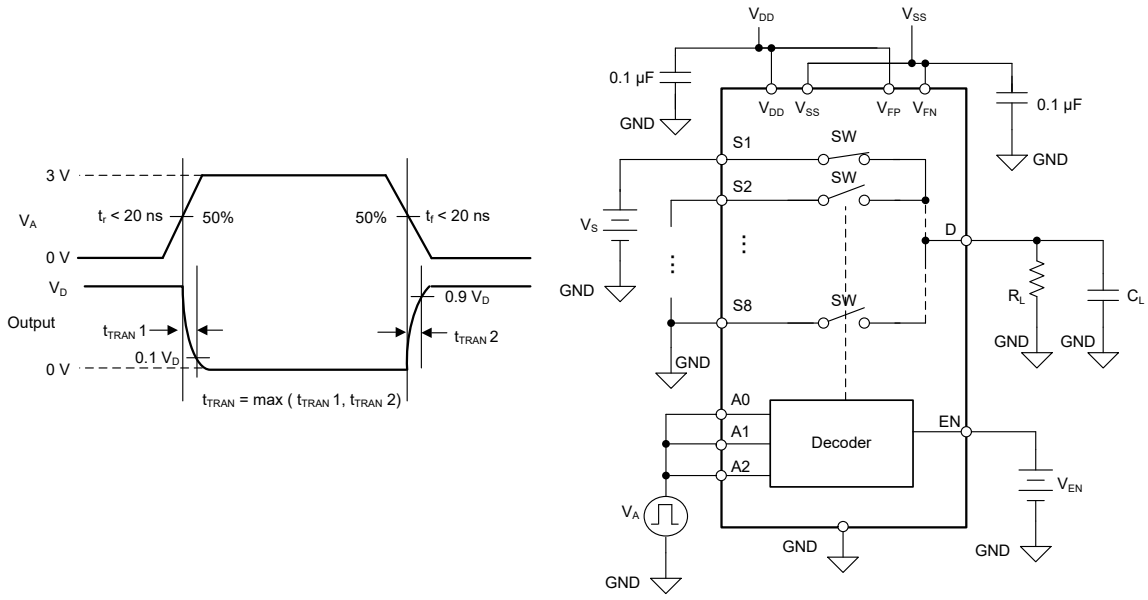

図 7-8. Transition Time Measurement Setup

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7.8 Fault Response Time

Fault response time ($t_{RESPONSE}$) measures the delay between the source voltage exceeding the fault supply voltage (V_{FP} or V_{FN}) by 0.5 V and the drain voltage failing to 50% of the maximum output voltage. 図 7-9 shows the setup used to measure $t_{RESPONSE}$.

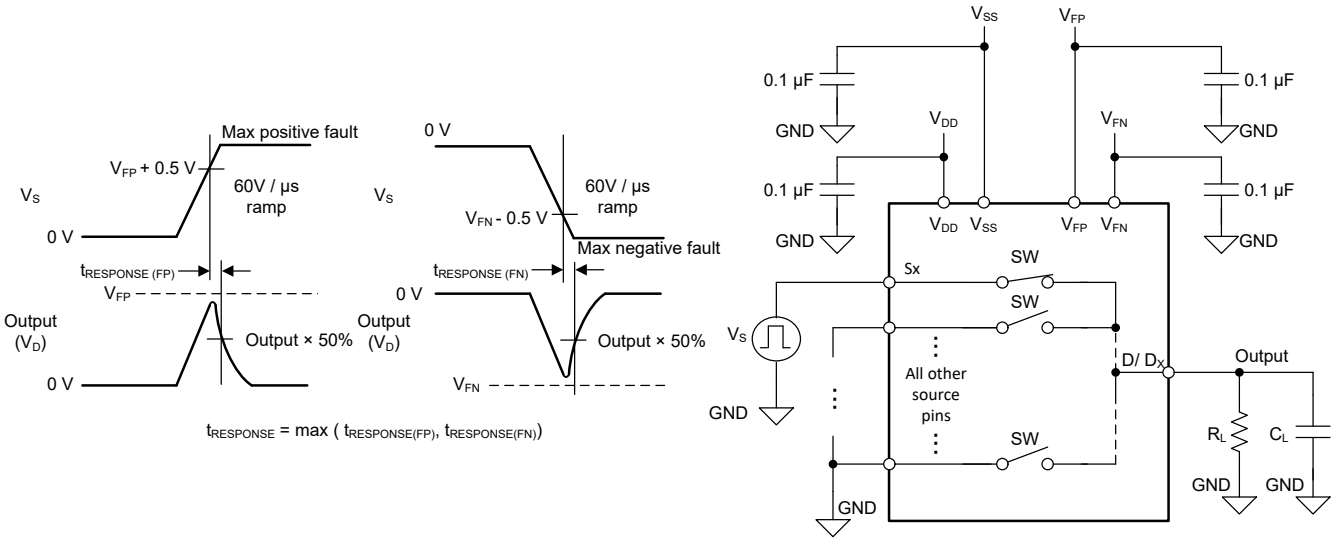

図 7-9. Fault Response Time Measurement Setup

7.9 Fault Recovery Time

Fault recovery time ($t_{RECOVERY}$) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage (V_{FP} or V_{FN}) plus 0.5 V and the drain voltage rising from 0 V to 50% of the final output voltage. 図 7-10 shows the setup used to measure $t_{RECOVERY}$.

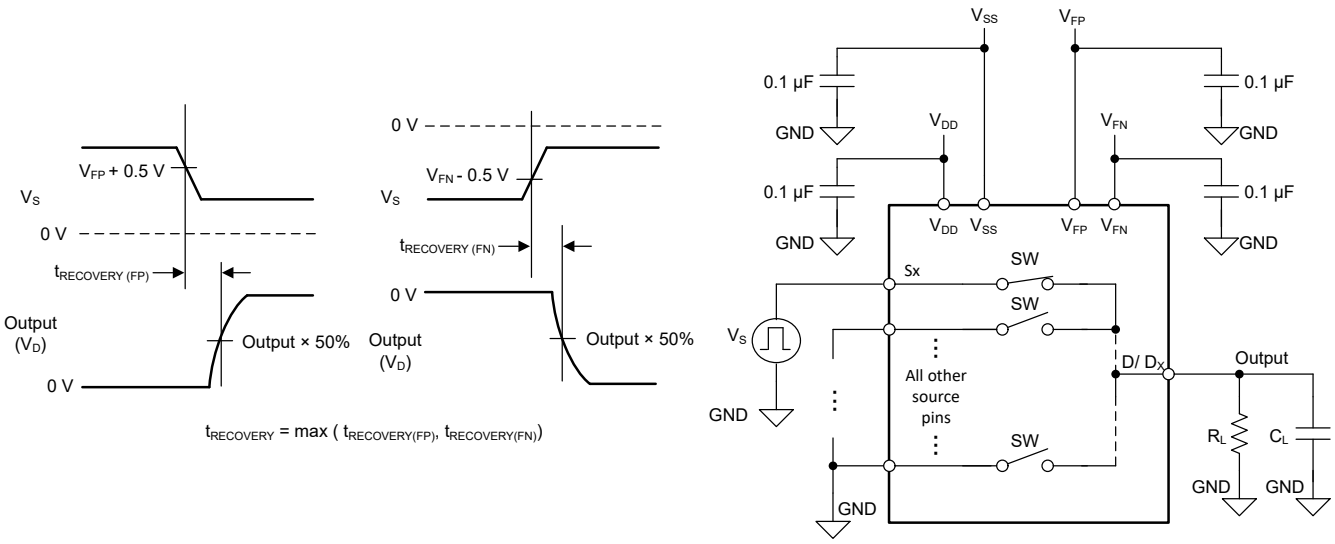

図 7-10. Fault Recovery Time Measurement Setup

7.10 Fault Flag Response Time

Fault flag response time ($t_{RESPONSE(FLAG)}$) measures the delay between the source voltage exceeding the fault supply voltage (V_{FP} or V_{FN}) by 0.5 V and the general fault flag (FF) pin or specific fault flag (SF) pin to go below 10% of its original value. 図 7-11 shows the setup used to measure $t_{RESPONSE(FLAG)}$.

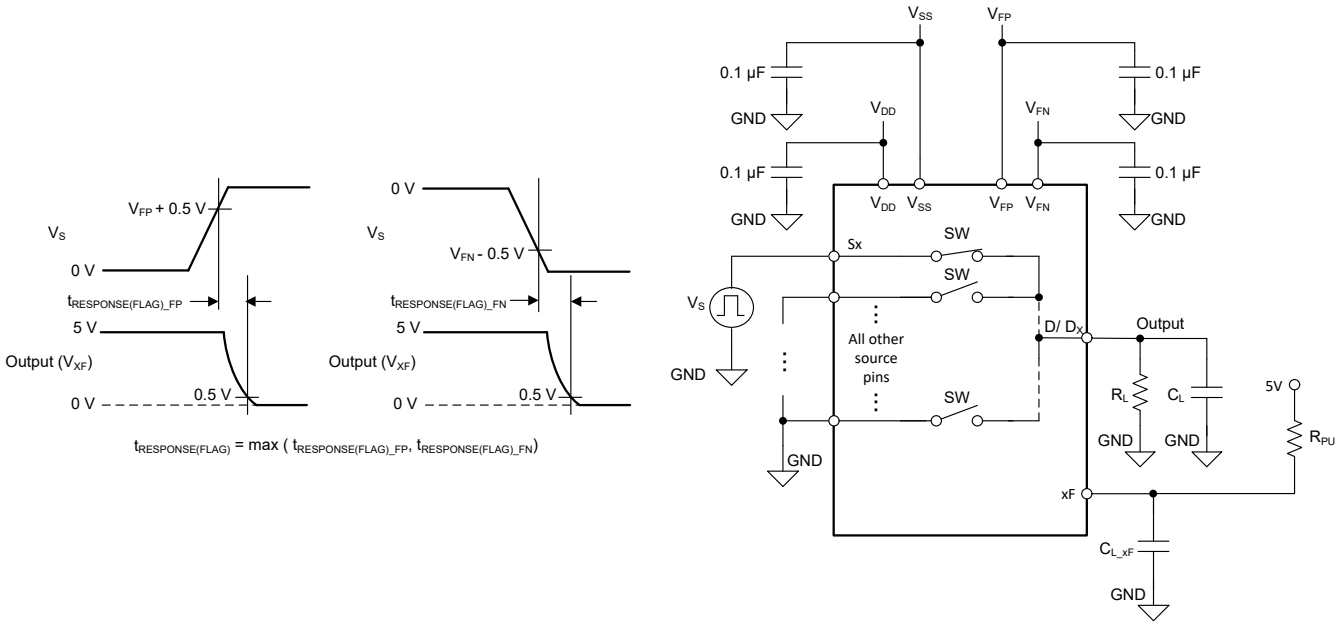

図 7-11. Fault Flag Response Time Measurement Setup

7.11 Fault Flag Recovery Time

Fault flag recovery time ($t_{RECOVERY(FLAG)}$) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage (V_{FP} or V_{FN}) plus 0.5 V and the general fault flag (FF) pin or the specific fault flag (SF) pin to rise above 3 V with 5 V external pull-up. 図 7-12 shows the setup used to measure $t_{RECOVERY(FLAG)}$.

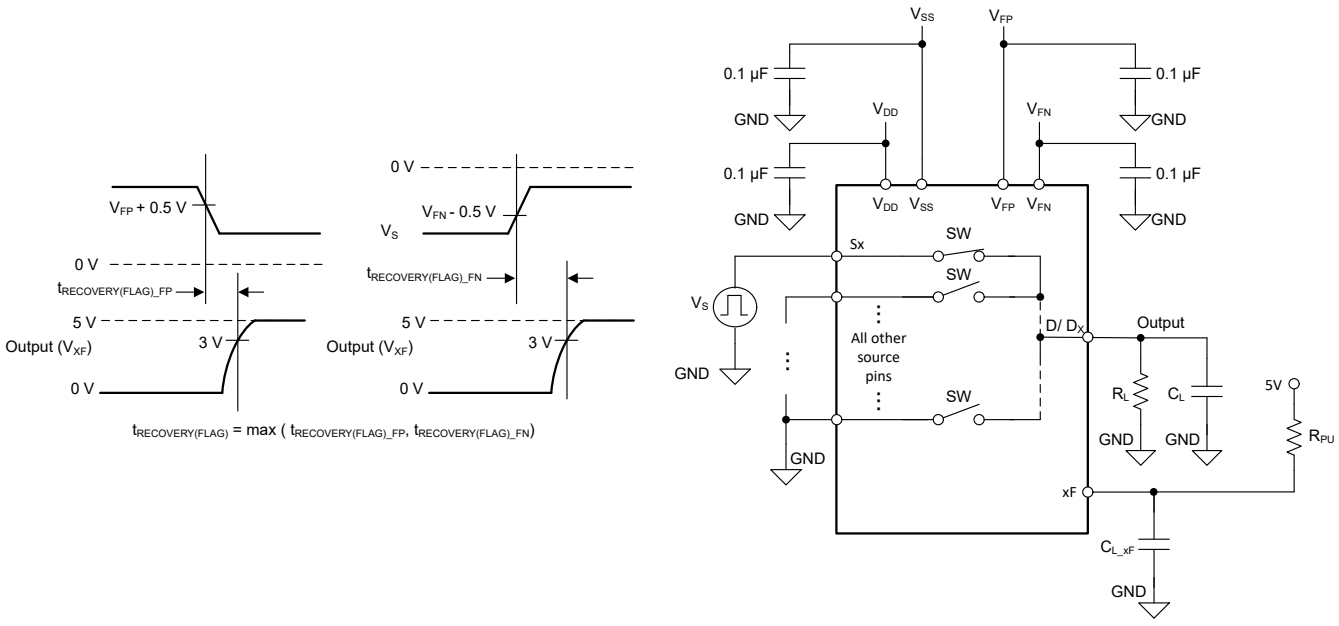

図 7-12. Fault Flag Recovery Time Measurement Setup

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7.12 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the logic input to the analog output during switching, and is denoted by the symbol Q_{INJ}. 図 7-13 shows the setup used to measure charge injection from the source to drain.

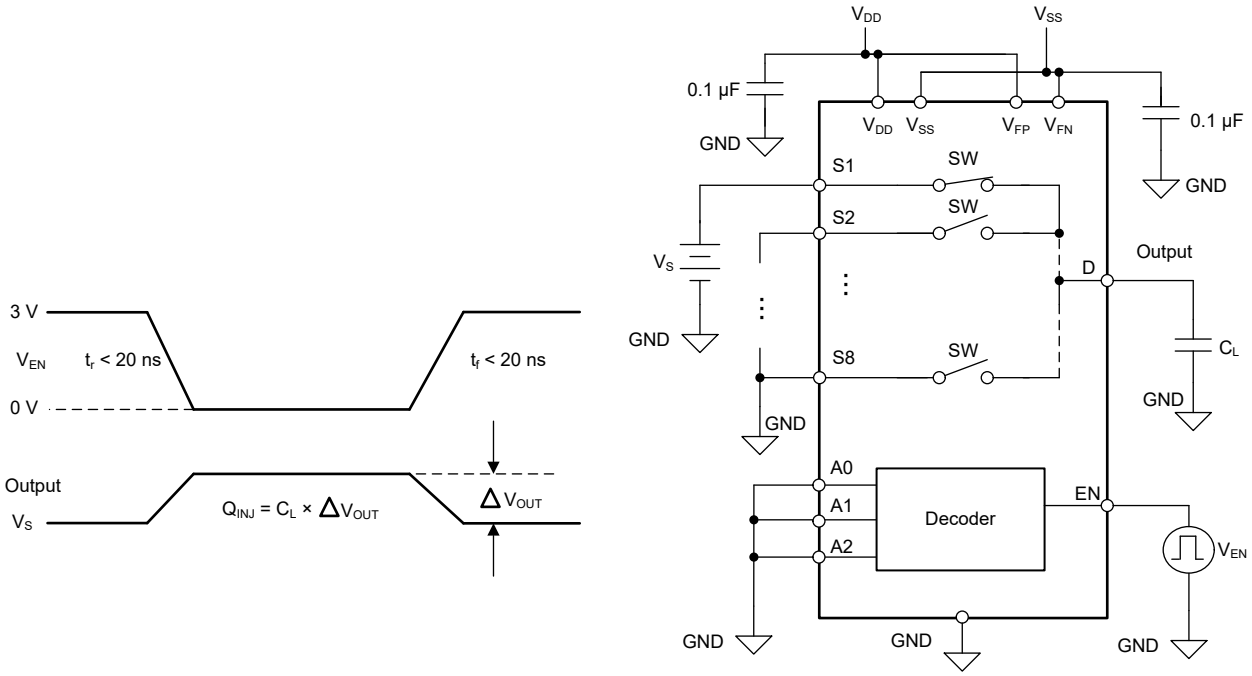

図 7-13. Charge-Injection Measurement Setup

7.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. 図 7-14 shows the setup used to measure, and the equation used to calculate off isolation.

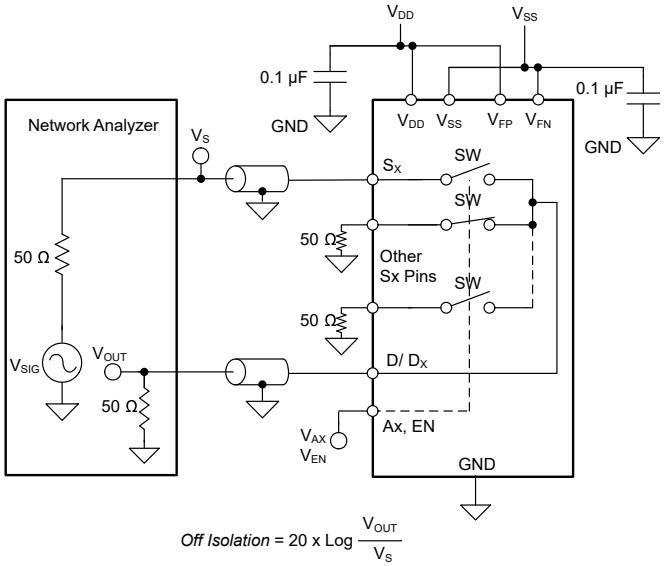

図 7-14. Off Isolation Measurement Setup

7.14 Crosstalk

Intra-channel crosstalk ($X_{TALK(INTRA)}$) is defined as the voltage at the source pin (Sx) of an off-switch input when a signal is applied at the source pin of an on-switch input in the same channel (as shown in 図 7-15).

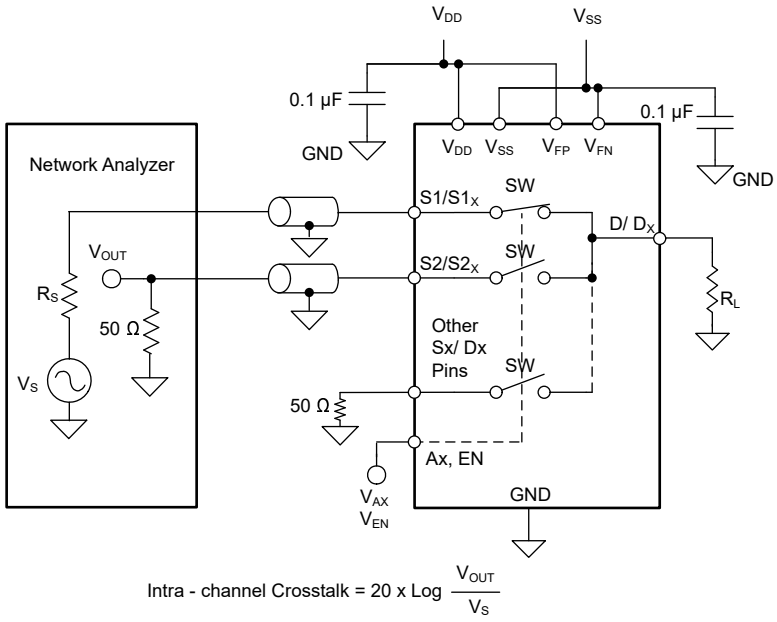

図 7-15. Intra-Channel Crosstalk Measurement Setup

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7.15 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D or Dx) of the TMUX7348F-EP. 図 7-16 shows the setup used to measure bandwidth of the switch.

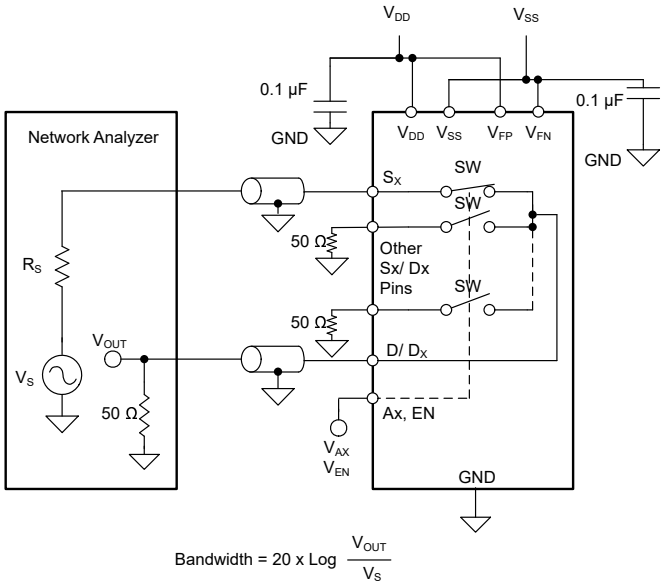


図 7-16. Bandwidth Measurement Setup

7.16 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The on-resistance of the TMUX7348F-EP varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 図 7-17 shows the setup used to measure THD+N of the devices.

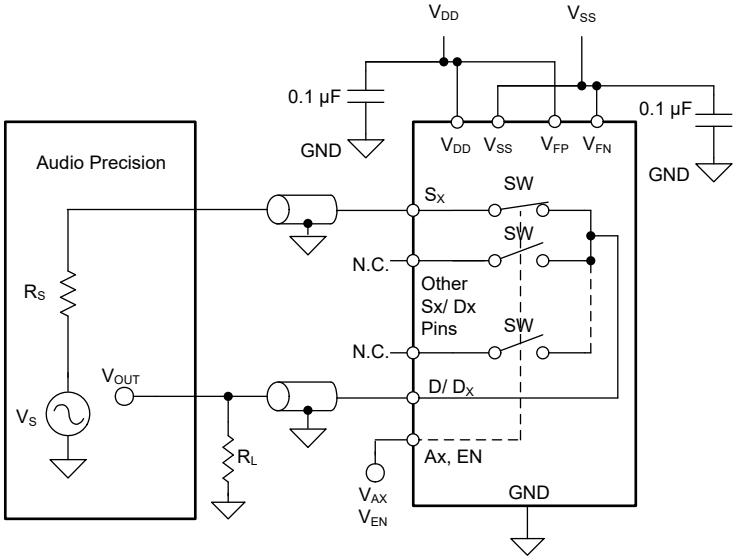


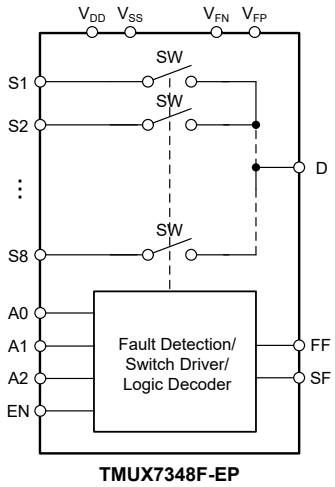
図 7-17. THD+N Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX7348F-EP is a modern complementary metal-oxide semiconductor (CMOS) analog multiplexer in a 8:1 configuration. This device works well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as V_{DD} = 15 V, V_{SS} = –5 V). This device has an overvoltage protection feature on the source pins under powered and powered-off conditions, allowing it to be used in harsh industrial environments.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Flat ON- Resistance

The TMUX7348F-EP is designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operation region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

8.3.2 Protection Features

The TMUX7348F-EP offer a number of protection features to enable robust system implementations.

8.3.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60 V or -60 V, regardless of supply voltage. This allows the device to handle typical voltage fault condition in industrial applications. Take caution: the device is rated to handle a maximum stress of 85 V across different pins, such as the following:

1. **Between source pins and supply rails:**

   For example, if the device is powered by V_{DD} supply of 20 V, then the maximum negative signal level on any source pin is –60 V to maintain the 60 V maximum rating on any source pin. If the device is powered by V_{DD} supply of 40 V, then the maximum negative signal level on any source pin is reduced to –45 V to maintain the 85 V maximum rating across the source pin and the supply.
2. **Between source pins and one or more of the drain pins:**

   For example, if channel S1(A) is ON and the voltage on S1(A) pin is 40 V. In this case, the drain voltage is also 40 V. The maximum negative voltage on any of the other source pins is –45 V to maintain the 85 V maximum rating across the source pin and the drain pin.

8.3.2.2 Powered-Off Protection

When the supplies of TMUX7348F-EP are removed (V_{DD}/ V_{SS} = 0 V or floating), the source (Sx) pins of the device remain in the high impedance (Hi-Z) state, and the source (Sx) and drain (Dx) pins of the device remain within the leakage performance mentioned in the *Electrical Characteristics*. Powered-off protection minimizes system complexity by removing the need to control the power supply sequencing of the system. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, the signal on the input source pins can back-power the supply rails through the internal ESD diodes and potentially cause damage to the system. For more information on powered-off protection refer to the *Eliminate Power Sequencing with Powered-Off Protection Signal Switches* application brief.

The switch remains OFF regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present for proper operation. Source and drain voltage levels of up to ±60 V are blocked in the powered-off condition.

8.3.2.3 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. The switch is specified to be in the OFF state, regardless of the state of the logic signals. The logic inputs are protected against positive faults of up to +44 V in the powered-off condition, but do not offer protection against the negative overvoltage condition.

Fail-safe logic also allows the TMUX7348F-EP to interface with a voltage greater than V_{DD} during normal operation to add maximum flexibility in system design. For example, with a V_{DD} of = 15 V, the logic control pins could be connected to +24 V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 44 V.

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8.3.2.4 Overvoltage Protection and Detection

The TMUX7348F-EP detect overvoltage inputs by comparing the voltage on a source pin (Sx) with the fault supplies (V_{FP} and V_{FN}). A signal is considered overvoltage if it exceeds the fault supply voltages by the threshold voltage (V_T).

When an overvoltage is detected, the switch automatically turns OFF regardless of the logic controls. The source pin becomes high impedance and only allows small leakage current to flow through the switch, and the overvoltage does not appear on the drain. When the overvoltage channel is selected by the logic control, the drain pin (D or Dx) is pulled to the supply that was exceeded. For example, if the source voltage exceeds V_{FP}, then the drain output is pulled to V_{FP}. If the source voltage exceeds V_{FN}, then the drain output is pulled to V_{FN}. The pull-up impedance is approximately 40 kΩ, and as a result, the drain current is limited to roughly 1 mA during a shorted load (to GND) condition.

図 8-1 shows a detailed view of how the pullup or down controls the output state of the drain pin under a fault scenario.

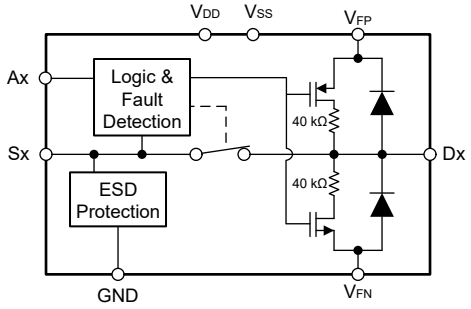

図 8-1. Detailed Functional Diagram

V_{FP} and V_{FN} are required fault supplies that set the level at which the overvoltage protection is engaged. V_{FP} can be supplied from 3 V to V_{DD}, while the V_{FN} can be supplied from V_{SS} to 0 V. If the fault supplies are not available in the system, the V_{FP} pin must be connected to V_{DD}, while the V_{FN} pin must be connected to V_{SS}. In this case, overvoltage protection then engages at the primary supply voltages V_{DD} and V_{SS}.

8.3.2.5 Adjacent Channel Operation During Fault

When the logic pins are set to a channel under a fault, the overvoltage detection will trigger, the switch will open, and the drain pin will be pulled up or down as described in セクション 8.3.2.4. During such an event, all other channels not under a fault can continue to operate as normal. For example, if S1 voltage exceeds V_{FP}, and the logic pins are set to S1, the drain output is pulled to V_{FP}. Then if the logic pins are changed to set S4, which is not in overvoltage or undervoltage, the drain will disconnect from the pullup to V_{FP} and the S4 switch will be enabled and connected to the drain, operating as normal. If the logic pins are switched back to S1, the S4 switch will be disabled, the drain pin will be pulled up to V_{FP} again, and the switch from S1 to drain will not be enabled until the overvoltage fault is removed.

8.3.2.6 ESD Protection

All pins on the TMUX7348F-EP support HBM ESD protection level up to ±3.5 kV, which helps the device from getting ESD damages during the manufacturing process.

The drain pins (D or Dx) have internal ESD protection diodes to the fault supplies V_{FP} and V_{FN}. Therefore, the voltage at the drain pins must not exceed the fault supply voltages to prevent excessive diode current. The source pins have specialized ESD protection that allows the signal voltage to reach ±60 V regardless of the supply voltage level. Exceeding ±60 V on any source input may damage the ESD protection circuitry on the device and cause the device to malfunction if the damage is excessive.

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8.3.2.7 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX7348F-EP is constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX7348F-EP to be used in harsh environments. For more information on latch-up immunity refer to the *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report.

8.3.2.8 EMC Protection

The TMUX7348F-EP is not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specification: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistors, are required to prevent source input voltages from going above the rated ±60 V limits.

When selecting a TVS protection device, it is critical to ensure that the maximum working voltage is greater than both the normal operating range of the input source pins to be protected and any known system common-mode overvoltage that may be present due to incorrect wiring, loss of power, or short circuit. 図 8-2 shows an example of the proper design window when selecting a TVS device.

Region 1 denotes normal operation region of TMUX7348F-EP where the input source voltages stay below the fault supplies V_{FP} and V_{FN}. Region 2 represents the range of possible persistent DC (or long duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX7348F-EP. The TVS breakdown voltage must be selected to be less than the absolute maximum rating of the TMUX7348F-EP, but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin system designers must impose when selecting the TVS protection device to prevent accidental triggering of ESD cells of the TMUX7348F-EP.

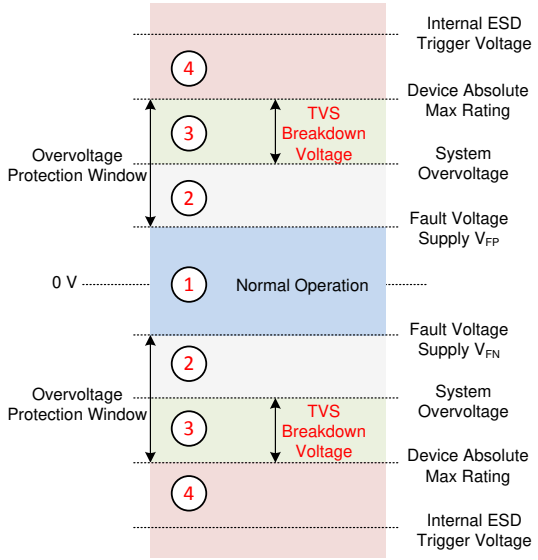

図 8-2. System Operation Regions and Proper Region of Selecting a TVS Protection Device

8.3.3 Overvoltage Fault Flags

The voltages on the source input pins of the TMUX7348F-EP are continuously monitored, and the status of whether an overvoltage condition occurs is indicated by an active low general fault flag (FF). The voltage on the FF pin indicates if any of the source input pins are experiencing an overvoltage condition. If any source pin voltage exceeds the fault supply voltages by a V_T, the FF output is pulled-down to below V_{OL}.

The specific fault (SF) output pins, likewise, can be used to decode which inputs are experiencing an overvoltage condition. The SF pin is pulled-down to below V_{OL} when an overvoltage condition is detected on a specific source input pin, depending on the state of the A0, A1, A2, and EN logic pins (表 8-1 provides more information).

Both the FF pin and SF pin are open-drain output and external pull-up resistors of 1 kΩ are recommended. The pull-up voltage can be in the range of 1.8 V to 5.5 V, depending on the controller voltage the device interfaces with.

8.3.4 Bidirectional and Rail-to-Rail Operation

The TMUX7348F-EP conducts equally well from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Each signal path has very similar characteristics in both directions. It is important to note, however, that the overvoltage protection is implemented only on the source (Sx) side. The voltage on the drain is only allowed to swing between V_{FP} and V_{FN} and no overvoltage protection is available on the drain side.

The primary supplies (V_{DD} and V_{SS}) define the on-resistance profile of the switch channel, whereas the fault voltage supplies (V_{FP} and V_{FN}) define the signal range that can be passed through from source to drain of the device. It is good practice to use voltages on V_{FP} and V_{FN} that are lower than V_{DD} and V_{SS} to take advantage of the flat on-resistance region of the device for better input-to-output linearity. The flattest on-resistance region extends from V_{SS} to roughly 3 V below V_{DD}. Once the signal is within 3 V of V_{DD} the on-resistance will exponentially increase and may impact desired signal transmission.

8.3.5 1.8 V Logic Compatible Inputs

The TMUX7348F-EP has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the TMUX7348F-EP to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of material (BOM) cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V Logic Muxes and Switches*.

8.3.6 Integrated Pull-Down Resistor on Logic Pins

The TMUX7348F-EP have internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.4 Device Functional Modes

The TMUX7348F-EP offer two modes of operation (Normal mode and Fault mode) depending on whether any of the input pins experience an overvoltage condition.

8.4.1 Normal Mode

In Normal mode operation, signals of up to V_{FP} and V_{FN} can be passed through the switch from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). The address (Ax) pins and the enable (EN) pin determine which switch path to turn on (表 8-1 provides more information). The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies ($V_{DD} – V_{SS}$) must be higher or equal to 8 V. With a minimum V_{DD} of 5 V.
- V_{FP} must be between 3 V and V_{DD}, and V_{FN} must be between V_{SS} and 0 V.
- The input signals on the source (Sx) or the drain (D or Dx) must be between V_{FP}+ V_T and $V_{FN} – V_T$.
- The logic control (Ax and EN) must have selected the switch.

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8.4.2 Fault Mode

The TMUX7348F-EP enters into Fault mode when any of the input signals on the source (Sx) pins exceed V_{FP} or V_{FN} by a threshold voltage V_T. Under the overvoltage condition, the switch input experiencing the fault automatically turns OFF regardless of the logic status, and the source pin becomes high impedance with a negligible amount of leakage current flowing through the switch. When the fault channel is selected by the logic control, the drain pin (D or Dx) is pulled to the fault supply that was exceeded through a 40 kΩ internal resistor.

In the Fault mode, the general fault flag (FF) is asserted low. The specific flag (SF) is asserted low when a specific input path is selected, according to 表 8-1.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (D or Dx) pin, if used as signal input, must stay in between V_{FP} and V_{FN} at all time since no overvoltage protection is implemented on the drain pin.

8.4.3 Truth Tables

表 8-1 provides the truth tables for the TMUX7348F-EP under normal and fault conditions.

表 8-1. TMUX7348F-EP Truth Table

EN	A2	A1	A0	Normal Condition	Fault Condition							
					State of Specific Flag (SF) when fault occurs on							
				On Switch	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	0	None	0	1	1	1	1	1	1	1
0	0	0	1	None	1	0	1	1	1	1	1	1
0	0	1	0	None	1	1	0	1	1	1	1	1
0	0	1	1	None	1	1	1	0	1	1	1	1
0	1	0	0	None	1	1	1	1	0	1	1	1
0	1	0	1	None	1	1	1	1	1	0	1	1
0	1	1	0	None	1	1	1	1	1	1	0	1
0	1	1	1	None	1	1	1	1	1	1	1	0
1	0	0	0	S1	0	1	1	1	1	1	1	1
1	0	0	1	S2	1	0	1	1	1	1	1	1
1	0	1	0	S3	1	1	0	1	1	1	1	1
1	0	1	1	S4	1	1	1	0	1	1	1	1
1	1	0	0	S5	1	1	1	1	0	1	1	1
1	1	0	1	S6	1	1	1	1	1	0	1	1
1	1	1	0	S7	1	1	1	1	1	1	0	1
1	1	1	1	S8	1	1	1	1	1	1	1	0

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMUX7348F-EP is part of the fault protected switches and multiplexers family of devices. The ability to protect downstream components from overvoltage events up to ±60 V makes these switches and multiplexers suitable for harsh environments.

9.2 Typical Application

In large applications, telemetry subsystems must take information from many sensors to monitor the overall health and performance of the system. This can result in the need for multiple ADCs and amplifiers to measure all this sensor data and send it to the processor. By using a multiplexer, the number of components in the system can drastically be reduced to save system cost, weight, and size. Additionally, the ADC and other downstream components will be protected from any overvoltage or miswiring events on the sensor inputs (up to **±**60-V), because of the fault protection on the TMUX7348F-EP. These fault conditions may include, but are not limited to: human error from wiring connections incorrectly, component failure or wire shorts, electromagnetic interference (EMI) and transient disturbances.

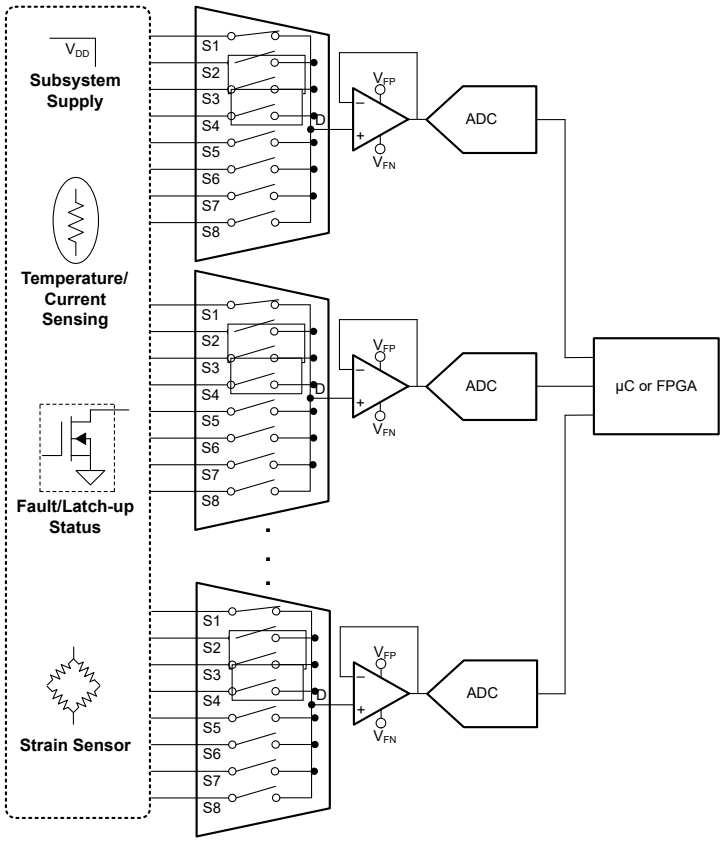

図 9-1. Typical Application

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9.2.1 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux	+15 V
Negative supply (V_{SS}) mux	-15 V
Positive fault voltage supply (V_{FP}) mux and ADC	+10 V
Negative fault voltage supply (V_{FN}) mux and ADC	-10 V
Power board supply voltage	24 V
Input / output signal range non-faulted	-10 V to 10 V
Overvoltage protection levels	-60 V to 60 V
Control logic thresholds	1.8 V compatible, up to 44 V
Temperature range	-55°C to +125°C

9.2.2 Detailed Design Procedure

The following image shows a high level telemetry use case, where multiple sensors need to be monitored by the system. Here, multiple TMUX7348F-EP are used to expand the sensor count, and this scheme can be scaled up or down depending on the sensor count. If the board supply voltage is higher than the fault voltage supply (V_{FP} or V_{FN}) of the multiplexer, then the TMUX7348F-EP will disconnect the source input from passing the signal to protect the downstream ADC. The drain pin of the mux will be pulled up to the fault voltage supply voltage V_{FP} through a 40 kΩ resistor to allow the ADC to determine a fault condition has occurred.

9.2.3 Application Curves

The example application utilizes the fault protection of the TMUX7348F-EP to protect downstream components from potential miswiring conditions from the power module board. 図 9-2 shows an example of positive overvoltage fault response with a fast fault ramp rate of 58 V/µs. 図 9-3 shows the extremely flat on-resistance across source voltage while operating within a common signal range of ±10 V. These features make the TMUX7348F-EP an excellent solution for factory automation applications that may face various fault conditions but also require excellent linearity and low distortion.

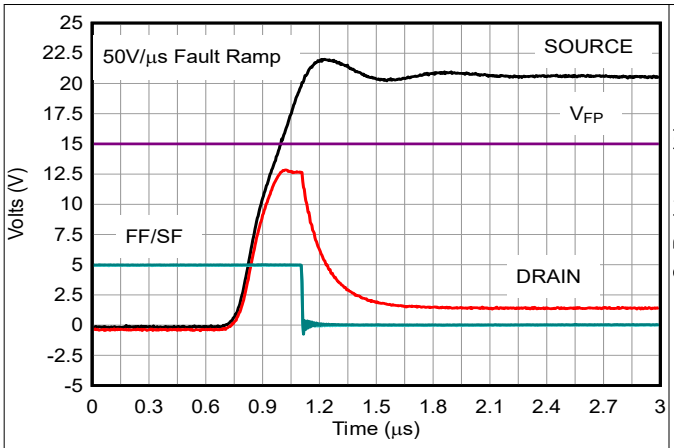

図 9-2. Positive Overvoltage Response

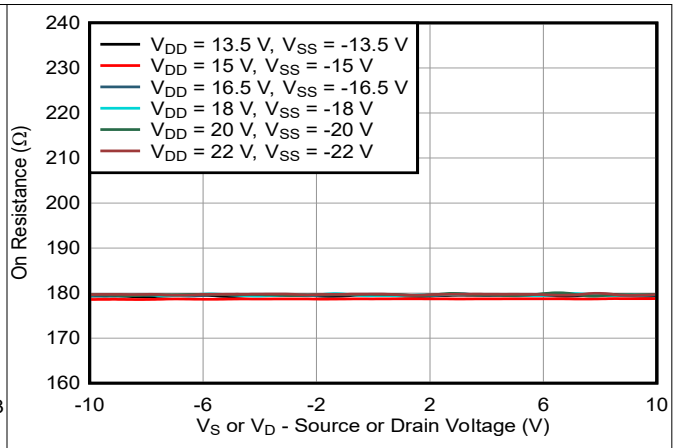

図 9-3. R_{ON} Flatness in Non-Fault Region

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9.3 Power Supply Recommendations

The TMUX7348F-EP operate across a wide supply range of ±5 V to ±22 V (8 V to 44 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped.

The fault supplies (V_{FP} and V_{FN}) provide the current required to operate the fault protection, and thus, must be low impedance supplies. They can be derived from the primary supplies by using a resistor divider and buffer or be an independent supply rail. The fault supplies must not exceed the primary supplies as it might cause unexpected behavior of the switch. Use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{FP} and V_{FN} pins to ground for improved supply noise immunity.

The positive supply (V_{DD}) must be ramped before the positive fault rail (V_{FP}) for proper power sequencing of the TMUX7348F-EP. Similarly, the negative supply (V_{SS}) must be ramped before the negative fault voltage rail (V_{FN}).

9.4 Layout

9.4.1 Layout Guidelines

The following images show examples of a PCB layout with the TMUX7348F-EP. Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and V_{SS} to GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
- Multiple decoupling capacitors can be used if their is a lot of noise in the system. For example, a 0.1-µF and 1-µF can be placed on the supply pins. If multiple capacitors are used, then it is recommended to place the lowest value capacitor closest to the supply pin.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

9.4.2 Layout Example

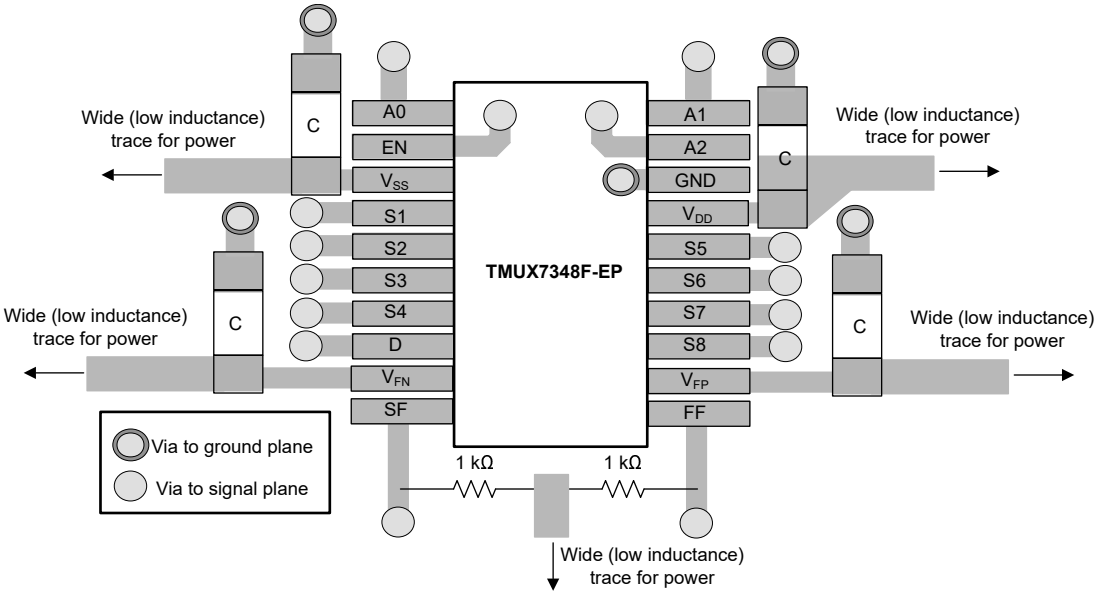

図 9-4. TMUX7348F-EP Layout Example

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Eliminate Power Sequencing with Powered-Off Protection Signal Switches* application brief
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Improving Analog Input Modules Reliability Using Fault Protected Multiplexers* application report
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *Protection Against Overvoltage Events, Miswiring, and Common Mode Voltages* application report
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report

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10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2023) to Revision A (January 2025)	Page
• ドキュメントのステータスを「*事前情報*」から「*量産データ*」に変更	1

DATE	REVISION	NOTES
November 2023	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX7348FPWTEP	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TM7348EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMUX7348F-EP :

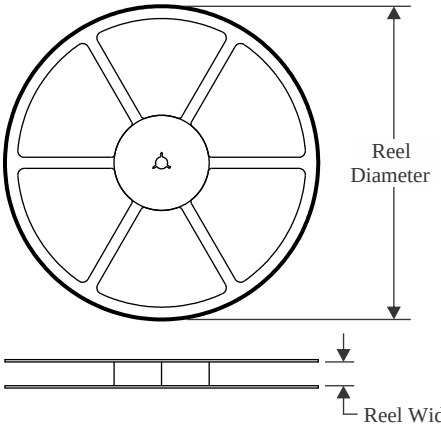
- Catalog : TMUX7348F

NOTE: Qualified Version Definitions:

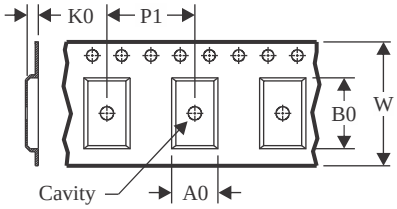
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

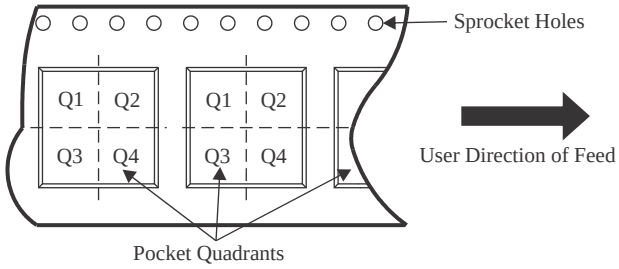


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

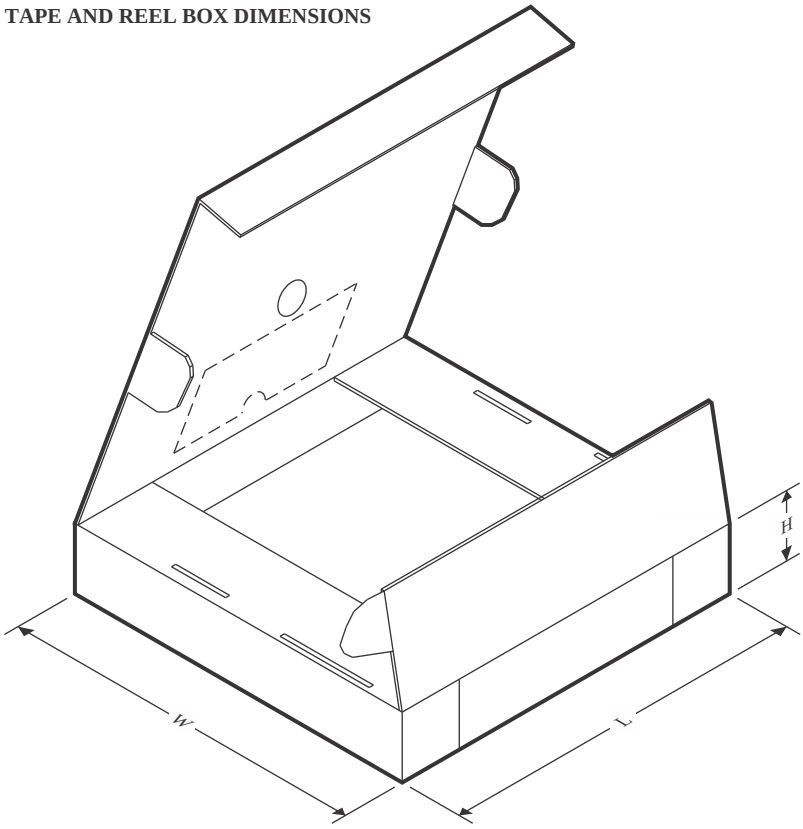
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7348FPWTEP	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

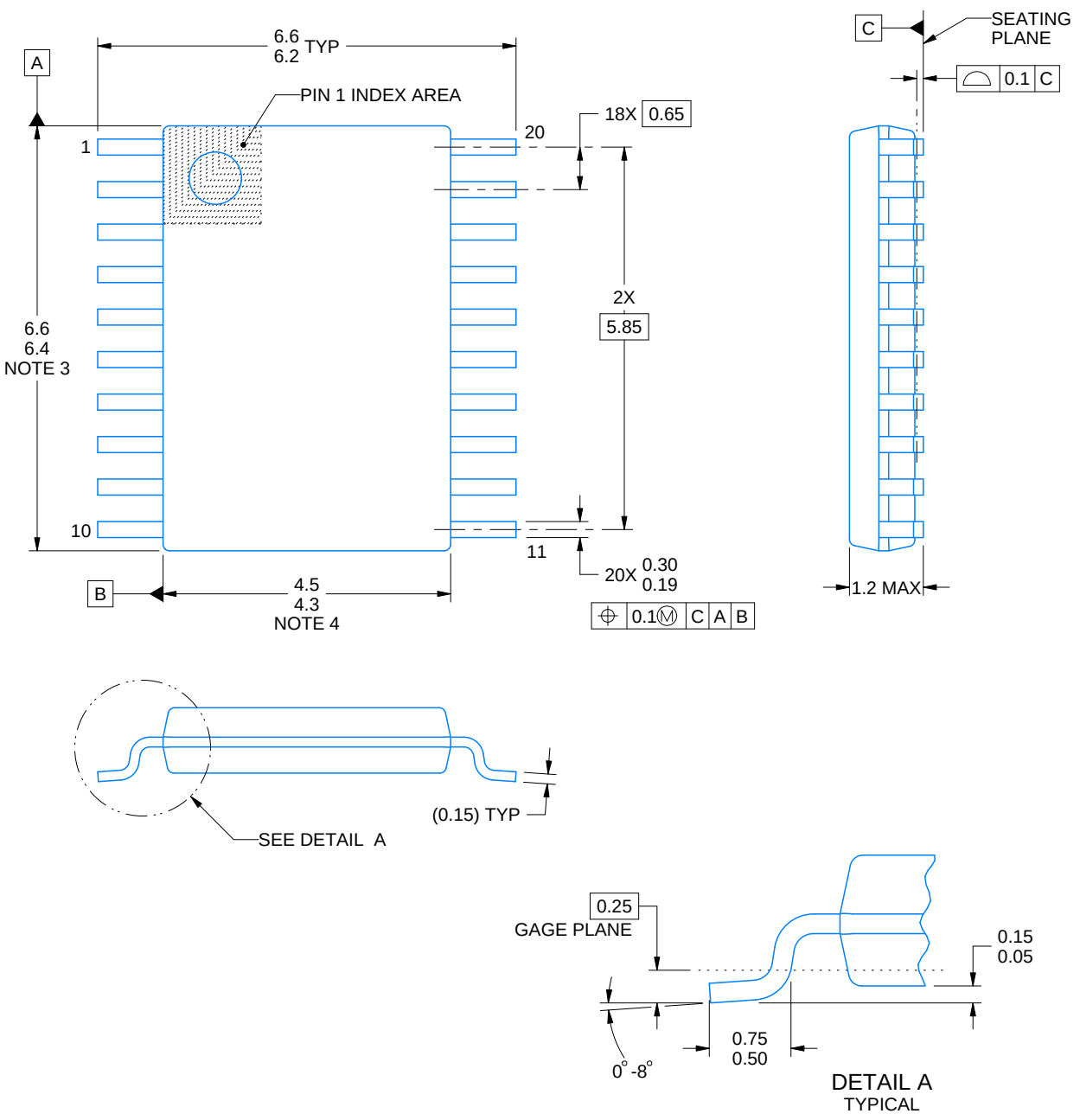
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7348FPWTEP	TSSOP	PW	20	250	353.0	353.0	32.0

PACKAGE OUTLINE

PW0020A

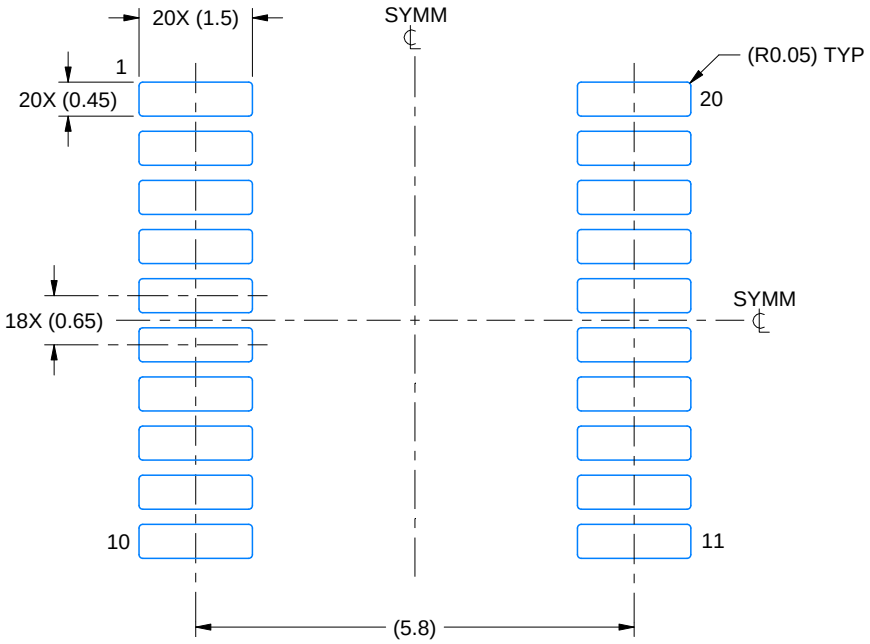
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



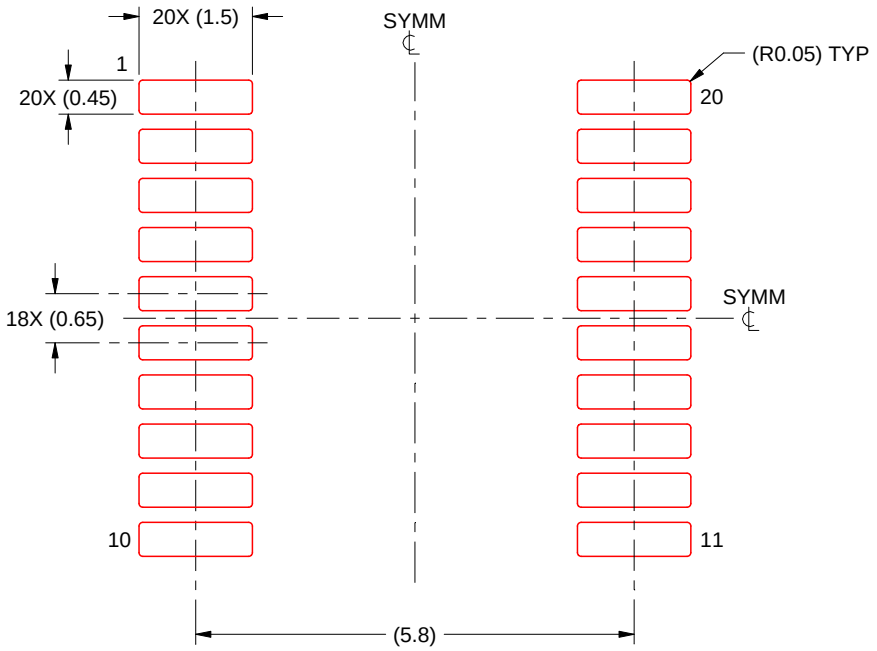
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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