

TMUXHS4412 4 チャンネル、20Gbps、2:1/1:2、差動マルチプレクサ / デマルチプレクサ

1 特長

- 4 つの差動チャンネルに対して、双方向パッシブ 2:1 マルチプレクサ / 1:2 デマルチプレクサを実現します
- 最大 20Gbps のデータ伝送能力
- 最大 16Gbps の PCI Express 4.0 をサポート
- USB 3.2、USB 4.0、TBT 3.0、DP 2.0、SATA、SAS、MIPI DSI/CSI、FPD-Link III、LVDS、SFI、イーサネットの各インターフェイスもサポート
- 3dB で 13GHz の広い差動帯域幅
- PCIe 4.0 信号処理に適した優れた動的特性
 - 挿入損失: -1.3dB (8GHz)
 - 反射損失: -22dB (8GHz)
 - クロストーク: -58dB (8GHz)
- 適応型同相電圧トラッキング
- 0~1.8V の同相電圧をサポート
- 3.3V または 1.8V の単一電源電圧 VCC
- 超低消費電力のアクティブ モード (320μA) とスタンバイモード (0.1μA)
- 産業用温度範囲 (-40°C~105°C) のオプション
- DS160PR421 と DS160PR412 を搭載したピン互換 PCIe 4.0 リニアリドライバ オプション
- 3.5mm × 9mm の QFN パッケージで供給

2 アプリケーション

- PC とノート PC
- ゲーム、ホームシアター、エンターテインメント、TV
- データセンターおよびエンタープライズ・コンピューティング
- 医療用アプリケーション
- 試験および測定機器
- ファクトリ・オートメーションおよび制御
- 航空宇宙および防衛
- 電子 POS (EPOS)
- ワイヤレス・インフラ

3 概要

TMUXHS4412 は高速双方向パッシブ スイッチで、マルチプレクサ (mux) とデマルチプレクサ (demux) 両方の構成に使用できます。TMUXHS4412 は、PCI Express 4.0 など最高 20Gbps のデータレートの多数の高速差動インターフェイスに使用できるアナログ差動パッシブ マルチプレクサ / デマルチプレクサです。電氣的チャンネルのシグナル インテグリティに余裕がある場合には、さらに高いデータレートで使用できます。TMUXHS4412 は、同相電圧範囲 (CMV) が 0V~1.8V、差動振幅が最大 1800mVpp の差動信号をサポートしています。適応型 CMV トラッキングにより、デバイスを通るチャンネルが同相電圧範囲全体にわたって変化しないようにしています。

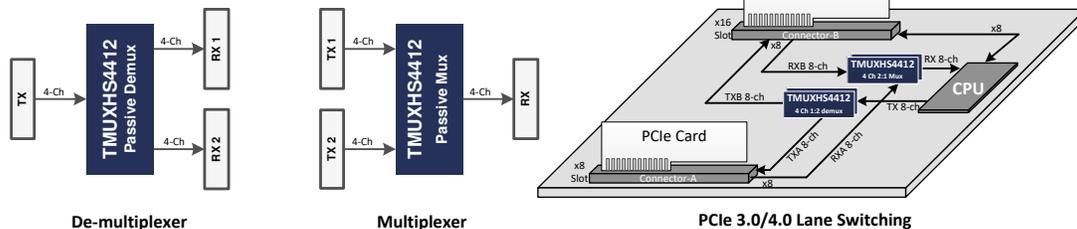
TMUXHS4412 の優れた動的特性は、信号アイ ダイアグラムの減衰の最小化、超低ジッタを可能にしています。このデバイスのシリコン設計は、高い周波数の信号帯域でも優れた周波数応答が得られるように最適化されています。このデバイスのシリコン信号トレースとスイッチ ネットワークは、最良のペア内スキュー性能が得られるように整合されています。

TMUXHS4412 は、産業用および高信頼性用途などの多数の堅牢なアプリケーションに適した拡張産業用温度範囲で動作します。

パッケージ情報 (1)

部品番号	パッケージ	パッケージ サイズ(2)
TMUXHS4412	RUA (WQFN, 42)	9mm × 3.5mm × 0.5mm ビッチ
TMUXHS4412I		

- (1) 供給されているすべてのパッケージについては、[セクション 10](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション使用事例



Table of Contents

1 特長	1	6.4 Device Functional Modes.....	11
2 アプリケーション	1	7 Application and Implementation	12
3 概要	1	7.1 Application Information.....	12
4 Pin Configuration and Functions	3	7.2 Typical Applications.....	13
5 Specifications	5	7.3 Systems Examples.....	17
5.1 Absolute Maximum Ratings.....	5	7.4 Power Supply Recommendations.....	18
5.2 ESD Ratings.....	5	7.5 Layout.....	18
5.3 Recommended Operating Conditions.....	5	8 Device and Documentation Support	20
5.4 Thermal Information.....	5	8.1 Related Documentation.....	20
5.5 Electrical Characteristics.....	6	8.2 ドキュメントの更新通知を受け取る方法.....	20
5.6 High-Speed Performance Parameters.....	6	8.3 サポート・リソース.....	20
5.7 Switching Characteristics.....	7	8.4 Trademarks.....	20
5.8 Typical Characteristics.....	8	8.5 静電気放電に関する注意事項.....	20
6 Detailed Description	10	8.6 用語集.....	20
6.1 Overview.....	10	9 Revision History	20
6.2 Functional Block Diagram.....	10	10 Mechanical, Packaging, and Orderable Information	20
6.3 Feature Description.....	11		

4 Pin Configuration and Functions

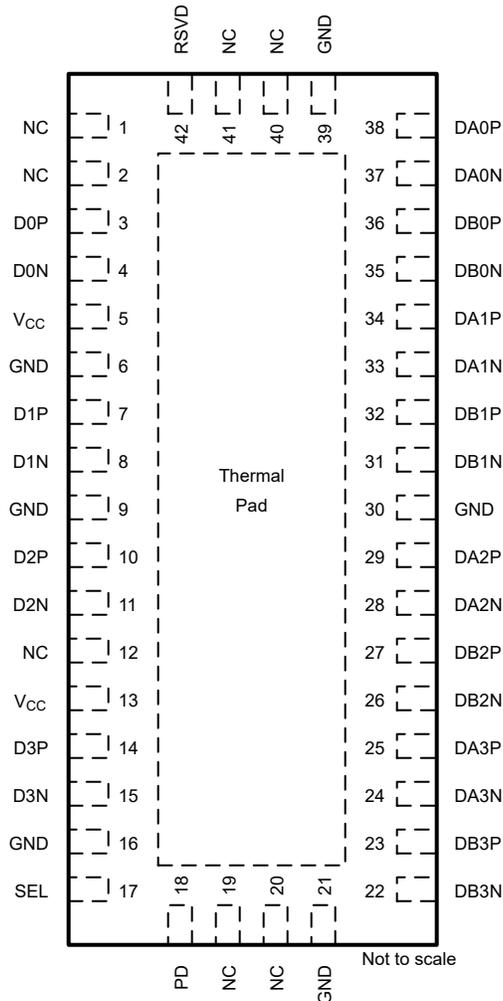


図 4-1. RUA Package 42-Pin WQFN Top View

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D0P	3	I/O	Common Port (D), channel 0, high-speed positive signal
D0N	4	I/O	Common Port, channel 0, high-speed negative signal
D1P	7	I/O	Common Port, channel 1, high-speed positive signal
D1N	8	I/O	Common Port, channel 1, high-speed negative signal
D2P	10	I/O	Common Port, channel 2, high-speed positive signal
D2N	11	I/O	Common Port, channel 2, high-speed negative signal
D3P	14	I/O	Common Port, channel 3, high-speed positive signal
D3N	15	I/O	Common Port, channel 3, high-speed negative signal
DA0P	38	I/O	Port A (DA), channel 0, high-speed positive signal
DA0N	37	I/O	Port A, channel 0, high-speed negative signal
DA1P	34	I/O	Port A, channel 1, high-speed positive signal
DA1N	33	I/O	Port A, channel 1, high-speed negative signal
DA2P	29	I/O	Port A, channel 2, high-speed positive signal

表 4-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
DA2N	28	I/O	Port A, channel 2, high-speed negative signal
DA3P	25	I/O	Port A, channel 3, high-speed positive signal
DA3N	24	I/O	Port A, channel 3, high-speed negative signal
DB0P	36	I/O	Port B (DB), channel 0, high-speed positive signal
DB0N	35	I/O	Port B, channel 0, high-speed negative signal
DB1P	32	I/O	Port B, channel 1, high-speed positive signal
DB1N	31	I/O	Port B, channel 1, high-speed negative signal
DB2P	27	I/O	Port B, channel 2, high-speed positive signal
DB2N	26	I/O	Port B, channel 2, high-speed negative signal
DB3P	23	I/O	Port B, channel 3, high-speed positive signal
DB3N	22	I/O	Port B, channel 3, high-speed negative signal
GND	6, 9, 16, 21,30, 39	G	Ground
PD	18	I	Active-low chip enable. H: Shutdown
NC	1, 2, 12, 19, 20, 40, 41	NA	Leave unconnected
RSVD	42	NA	Reserved - TI test mode. Pulldown to GND using a resistor such as 4.7kΩ
SEL	17	I	Port select pin. L: Common Port (D) to Port A (DA) H: Common Port (D) to Port B (DB)
V _{CC}	5, 13	P	3.3 or 1.8V power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC-ABS} MAX	Supply voltage	-0.5	4	V	
V _{HS-ABS} MAX	Voltage	Differential I/O pins	-0.5	2.4	V
V _{CTR-ABS} MAX	Voltage	Control pins	-0.5	V _{CC} +0.4	V
T _{STG}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
V _{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT	
V _{CC}	Supply voltage	1.8 V supply voltage mode	1.71	1.8	1.98	V
		3.3 V supply voltage mode	3.0	3.3	3.6	V
V _{CC-RAMP}	Supply voltage ramp time	0.1		100	ms	
V _{IH}	Input high voltage	SEL, PD pins	0.75V _{CC}		V	
V _{IL}	Input low voltage	SEL, PD pins		0.25V _{CC}	V	
V _{DIFF}	High-speed signal pins differential voltage		0	1.8	V _{pp}	
V _{CM}	High speed signal pins common mode voltage	1.8 V supply voltage mode, biased from common port (D)	0	0.9	V	
		3.3 V supply voltage mode, biased from D or DA/DB ports.	0	1.8	V	
T _A	Operating free-air/ambient temperature	TMUXHS4412	0	70	°C	
		TMUXHS4412I	-40	105	°C	

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUXHS4412	UNIT
		RUA (WQFN)	
		42 PINS	
R _{θJA}	Junction-to-ambient thermal resistance - High K	32.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	21.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	14.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	14.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	7.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	PD = 0; $0 V \leq V_{CM} \leq 1.8$; SEL = 0 or V_{CC}		320	480	μA
I_{STDN}	Device shutdown current	PD = V_{CC}		0.1	2	μA
C_{ON}	Output ON capacitance to GND	PD = 0; $f = 8$ GHz		0.45		pF
R_{ON}	Output ON resistance	$0 V \leq V_{CM} \leq 1.8 V$; $I_O = -8$ mA		5	8	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, PD)	$V_{IN} = 3.6 V$			2	μA
$I_{IL,CTRL}$	Input low current, control pins (SEL, PD)	$V_{IN} = 0 V$			1	μA
$R_{CM,HS}$	Common mode resistance to ground on D pins (Dx[P/N])	Each pin to GND		1.0	1.4	M Ω
$I_{IH,HS,SEL}$	Input high current, high-speed pins [Dx/DAx/DBx] [P/N]	$V_{IN} = 1.8 V$ for selected port, D and DA pins with SEL = 0, and D and DB pins with SEL = V_{CC}			5	μA
$I_{IH,HS,NSEL}$	Input high current, high-speed pins [Dx/DAx/DBx] [P/N]	$V_{IN} = 1.8 V$ for non-selected port, DB with SEL = 0, and DA with SEL = V_{CC} ⁽¹⁾			150	μA
$I_{HIZ,HS}$	Leakage current through turned off switch between Dx[P/N] and [DA/DB]x[P/N]	PD = V_{CC} ; Dx[P/N] = 1.8 V, [DA/DB]x[P/N] = 0 V and Dx[P/N] = 0 V, [DA/DB]x[P/N] = 1.8 V			4	μA
$R_{A,p2n}$	DC Impedance between Dx[P] and Dx[N] pins	PD = 0 and V_{CC}		20		K Ω

(1) There is a 20-k Ω pull-down in non-selected port.

5.6 High-Speed Performance Parameters

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	$f = 10$ MHz	-0.4		dB
		$f = 2.5$ GHz	-0.7		
		$f = 4$ GHz	-0.8		
		$f = 5$ GHz	-0.9		
		$f = 8$ GHz	-1.3		
		$f = 10$ GHz	-1.8		
BW	-3-dB bandwidth		13		GHz
R_L	Differential return loss	$f = 10$ MHz	-30		dB
		$f = 2.5$ GHz	-23		
		$f = 4$ GHz	-23		
		$f = 5$ GHz	-22		
		$f = 8$ GHz	-22		
		$f = 10$ GHz	-15		
O_{IRR}	Differential OFF isolation	$f = 10$ MHz	-57		dB
		$f = 2.5$ GHz	-27		
		$f = 4$ GHz	-22		
		$f = 5$ GHz	-20		
		$f = 8$ GHz	-15		
		$f = 10$ GHz	-12		
X_{TALK}	Differential crosstalk	$f = 10$ MHz	-73		dB
		$f = 2.5$ GHz	-64		
		$f = 4$ GHz	-61		
		$f = 5$ GHz	-61		
		$f = 8$ GHz	-58		
		$f = 10$ GHz	-54		
SCD11,22	Mode conversion - differential to common mode	$f = 8$ GHz	-29		dB
SCD21,12	Mode conversion - differential to common mode	$f = 8$ GHz	-25		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SDC11,22	Mode conversion - common mode to differential	$f = 8 \text{ GHz}$		-29		dB
SDC21,12	Mode conversion - common mode to differential	$f = 8 \text{ GHz}$		-25		dB

5.7 Switching Characteristics

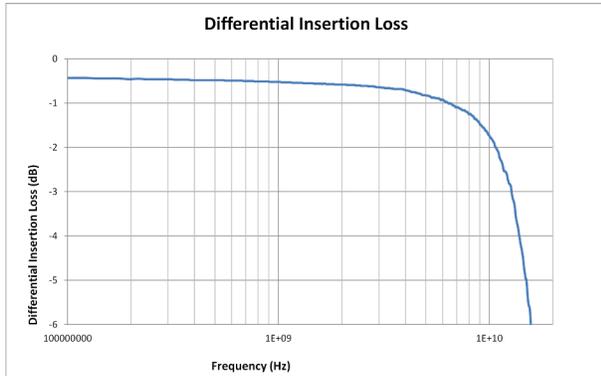
PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	$f = 1 \text{ GHz}$		50		ps
t_{SW_ON}	Switching time SEL-to-Switch ON	Biased from DA/DB side with CMV difference is <100mV, DA/DB pins at 90% of final value			130	ns
t_{SW_OFF}	Switching time SEL-to-Switch OFF	Biased from DA/DB side with CMV difference is <100mV, DA/DB pins at 90% of final value			100	ns
t_{SK_INTRA}	Intra-pair output skew between P and N pins for same channel	$f = 1 \text{ GHz}$		4.0		ps
t_{SK_INTER}	Inter-pair output skew between channels	$f = 1 \text{ GHz}$		4.0		ps

TMUXHS4412

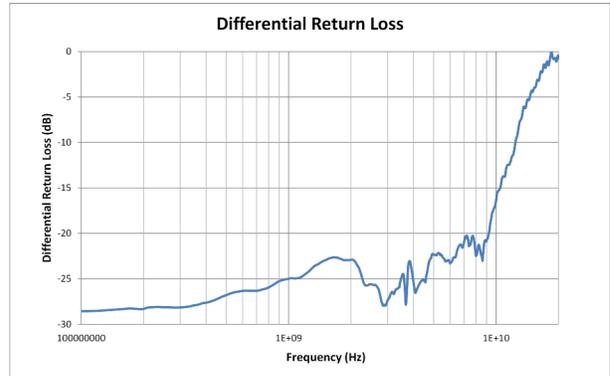
JAJSKW6A – DECEMBER 2020 – REVISED OCTOBER 2024

5.8 Typical Characteristics

The following figures show differential insertion loss on the top plot and return loss on the bottom plot of a typical TMUXHS4412 channel. Note measurements are performed in TI evaluation board with board and equipment parasitics calibrated out.

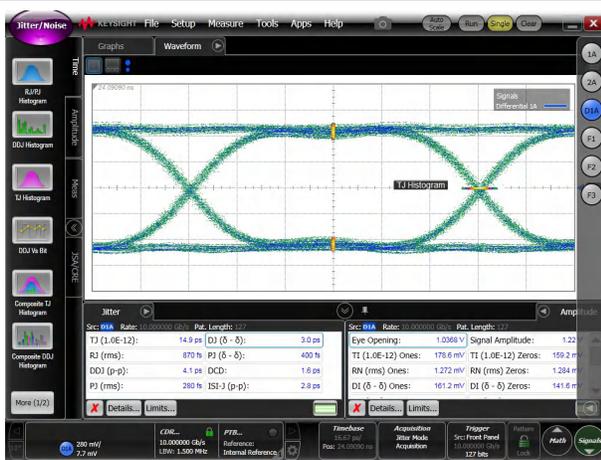


5-1. S-Parameter Plots for a TMUXHS4412 Channel: Differential Insertion Loss

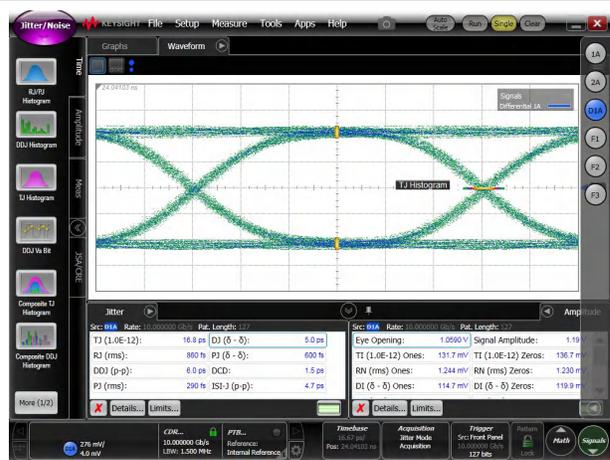


5-2. S-Parameter Plots for a TMUXHS4412 Channel: Return Loss vs Frequency

The following figures show side-by-side comparisons of 10Gbps signals through calibration traces and a typical TMUXHS4412 channels.



5-3. Jitter Decomposition of 10Gbps PRBS-7 Signals in TI Evaluation Board Through Calibration Traces



5-4. Jitter Decomposition of 10Gbps PRBS-7 Signals in TI Evaluation Board Through a Typical TMUXHS4412 Channel

The following figures show side-by-side comparisons of 20Gbps signals through calibration traces and a typical TMUXHS4412 channels.

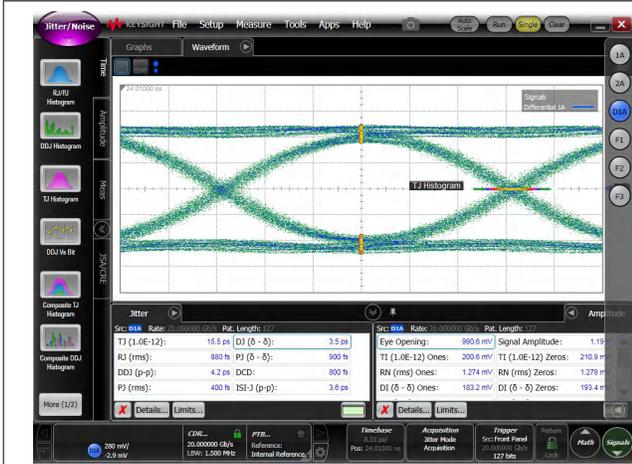


図 5-5. Jitter Decomposition of 20Gbps PRBS-7 Signals in TI Evaluation Board Through Calibration Traces

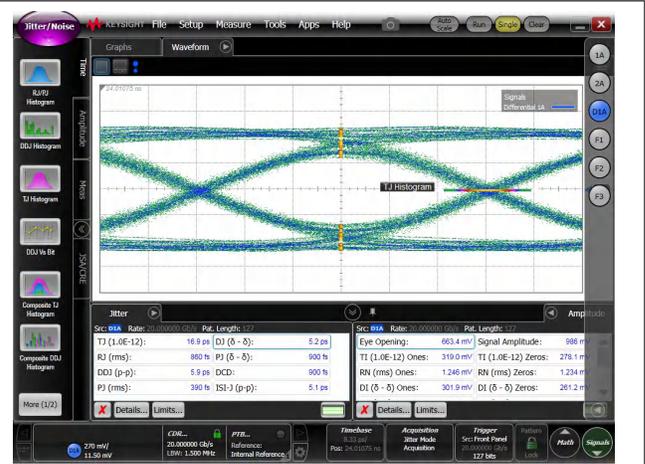


図 5-6. Jitter Decomposition of 20Gbps PRBS-7 Signals in TI Evaluation Board Through a Typical TMUXHS4412 Channels

6 Detailed Description

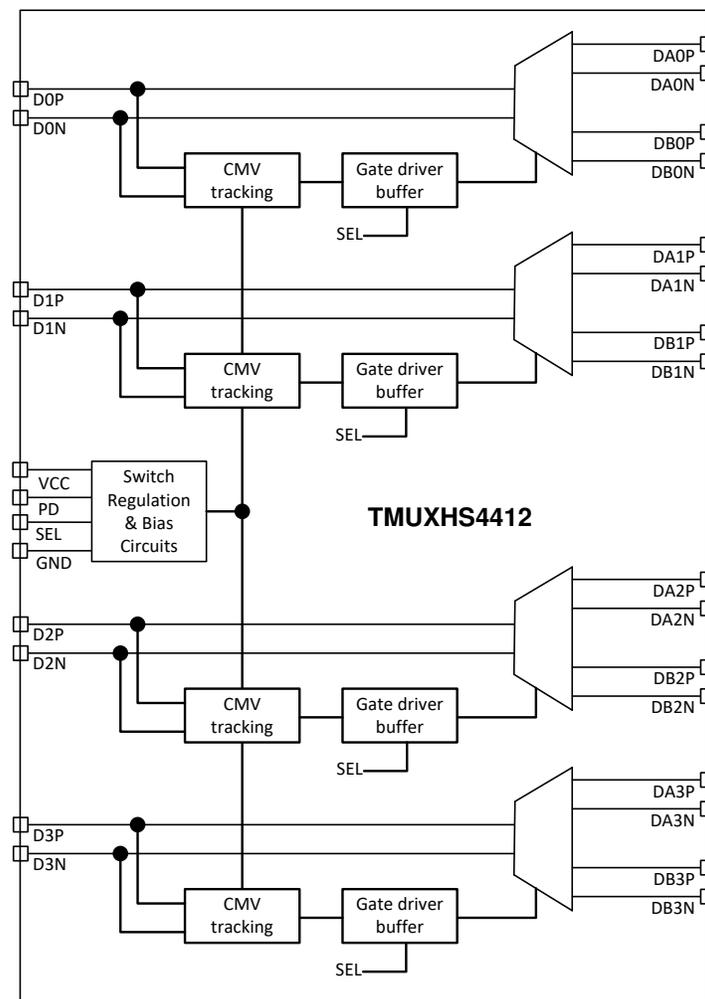
6.1 Overview

The TMUXHS4412 is an analog passive mux/demux that can work for any high-speed interface as long as the signaling is differential, has a common-mode voltage (CMV) that is within valid range (0V to 1.8V for 3.3V supply voltage mode), and has amplitude up to 1800mVpp-differential. The device has adaptive input voltage tracking to help users ensure the channel remains unchanged for the entire common-mode voltage range. Two channels of the device can be used for electrical signals that have different CMV between them. Two channels can also be used in such a way that the device switches two different interface signals with different data and electrical characteristics.

Excellent dynamic characteristics of the device allow high speed switching with minimum attenuation to the signal eye diagram with very little added jitter. While the device is recommended for the interfaces up to 20Gbps, actual data rate where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained the device can potentially be used for higher data rates.

The TMUXHS4412 is only recommended for differential signaling. If the two signals on differential lines are completely uncorrelated, then internal circuits can create certain artifacts. TI recommends to analyze the data line biasing of the device for such single-ended use cases. The device parameters are characterized for differential signaling only.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Enable and Power Savings

The TMUXHS4412 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes very little current to achieve ultra-low power in systems where power saving is critical. To enter standby mode, the PD control pin is pulled high through a resistor and must remain high. For active/normal operation, pull the PD control pin low to GND or dynamically controlled to switch between H or L.

6.3.2 Data Line Biasing

The TMUXHS4412 has a weak pulldown of 1MΩ from D[0/1/2/3][P/N] pins to GND. While these resistors biases the device data channels to common-mode voltage (CMV) of 0V with very weak strength, TI recommends that the device is biased by a stronger impedance from either side of the device to a valid value. To avoid double biasing, ensure appropriate AC coupling capacitors are on either side of the device.

In certain use cases where both sides of the TMUXHS4412 is AC-coupled, TI recommends to use appropriate CMV biasing for the device. 10kΩ to GND or any other bias voltage in the CMV range for each D[0/1/2/3][P/N] pin will suffice for most use cases.

The high-speed data ports incorporate 20kΩ pulldown resistors that are switched in when a port is not selected and switched out when the port is selected. For example: when SEL = L, the DB[0/1/2/3][P/N] pins have 20kΩ resistors to GND. The feature ensures that unselected port is always biased to a known voltage for long term reliability of the device and the electrical channel.

The positive and negative terminals of data pins D[0/1/2/3] have a weak (20kΩ) differential resistor in between the terminals for device switch regulation operation. This does not impact signal integrity or functionality of high-speed differential signaling that typically has much stronger differential impedance (such as 100Ω).

6.4 Device Functional Modes

表 6-1. Port Select Control Logic ⁽¹⁾

PORT D CHANNEL	PORT DA OR PORT DB CHANNEL CONNECTED TO PORT D CHANNEL	
	SEL = L	SEL = H
D0P	DA0P	DB0P
D0N	DA0N	DB0N
D1P	DA1P	DB1P
D1N	DA1N	DB1N
D2P	DA2P	DB2P
D2N	DA2N	DB2N
D3P	DA3P	DB3P
D3N	DA3N	DB3N

- (1) The TMUXHS4412 can tolerate polarity inversions for all differential signals on Ports D, DA, and DB. In such flexible implementation, users must ensure that the same polarity is maintained on Port D versus Ports DA/DB.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TMUXHS4412 is an analog 4-channel high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The TMUXHS4412 can be used for many high-speed interfaces including:

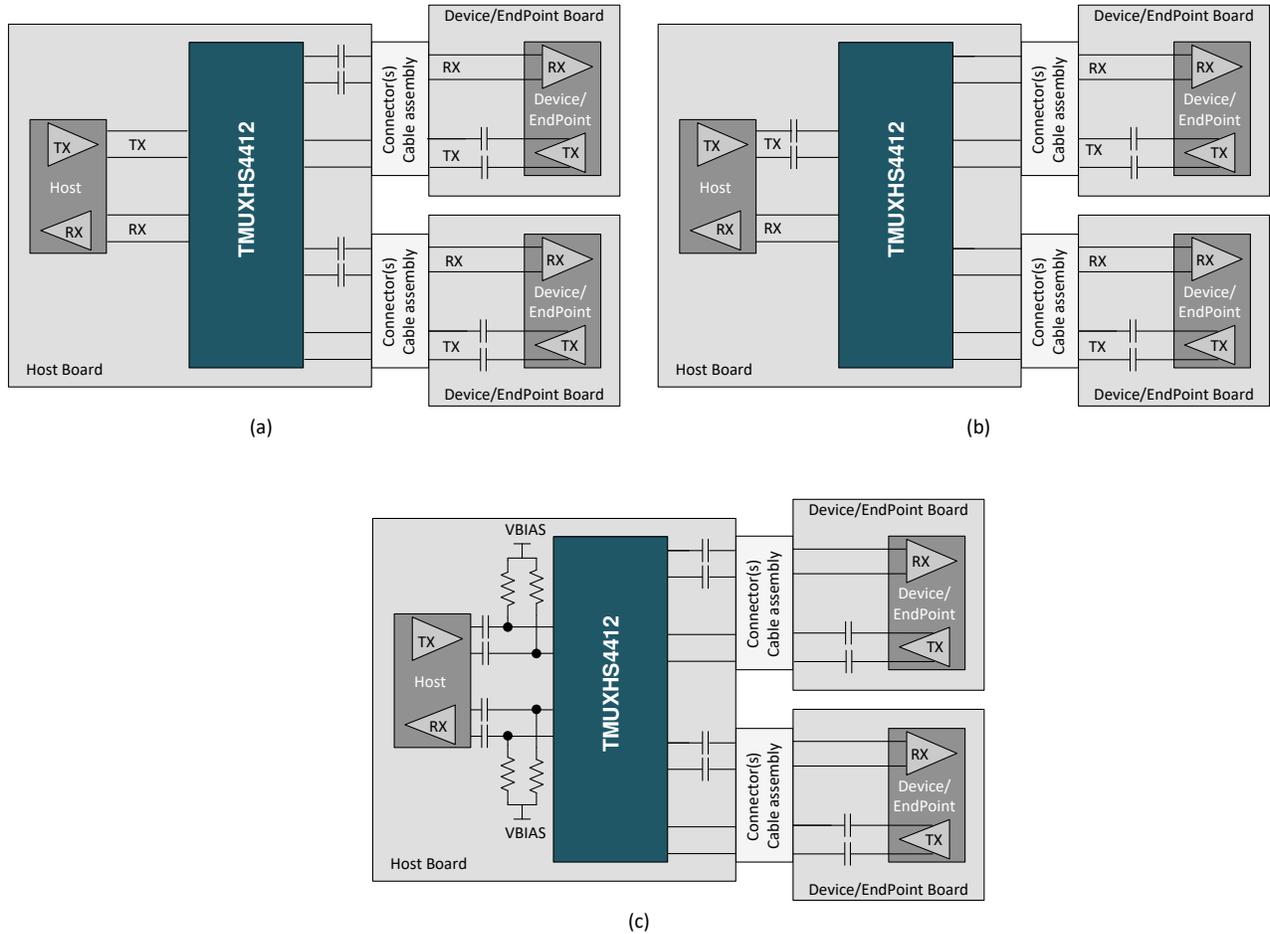
- Peripheral Component Interconnect Express (PCIe) Gen 1.0, 2.0, 3.0, 4.0
- USB 4.0
- Universal Serial Bus (USB) 3.2 Gen 1.0, 2.0
- Serial ATA (SATA/eSATA)
- Serial Attached SCSI (SAS)
- Display Port (DP) 1.4, 2.0
- Thunderbolt (TBT) 3.0
- MIPI Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- Low Voltage Differential Signaling (LVDS)
- Serdes Framer Interface (SFI)
- Ethernet Interfaces

The mux/demux selection pin SEL can easily be controlled by an available GPIO pin of a controller or hard tie to voltage level H or L as an application requires.

The TMUXHS4412 with adaptive voltage tracking technology can support applications where the common mode is different between the RX and TX pair. The switch paths of the TMUXHS4412 have internal weak pulldown resistors of 1M Ω on the common port pins. While these resistors biases the device data channels to common-mode voltage (CMV) of 0V with a weak strength, TI recommends to bias the device from either side of the device to a valid value (in the range of 0V to 1.8V in 3.3V supply voltage mode). It is expected that the system/host controller and device/end point common-mode bias impedances are much stronger (smaller) than the TMUXHS4412 internal pulldown resistors and are therefore not impacted.

Many interfaces require AC coupling between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option to provide AC coupling. Avoid the 0603, 0805 size capacitors and C-packs. When placing AC-coupling capacitors, symmetric placement is best. The capacitor value must be chosen according to the specific interface the device is being used. Make sure the value of the capacitor matches the positive and negative signal pair. For many interfaces such as USB 3.2 and PCIe, the designer can place them along the TX pairs on the system board, which are usually routed on the top layer of the board. Use the appropriate value for AC-coupling capacitors based on the application and interface specifications.

The AC-coupling capacitors have several placement options. Typical use cases warrant that the capacitors are placed on one side of the TMUXHS4412. In certain use cases, if both sides of the TMUXHS4412 is AC-coupled, TI recommends to use appropriate CMV biasing for the device. 10k Ω to GND or any other bias voltage in the valid CMV range for each D[0/1/2/3][P/N] pin of the common port suffice for most use cases. [Figure 7-1](#) shows a few placement options. Note for brevity not all channels are illustrated in the block diagrams. Some interfaces such as USB SS and PCIe recommend placing AC-coupling capacitors on the TX signals before a connector. Option (a) features TX AC-coupling capacitors on the connector side of the TMUXHS4412. Option (b) illustrates the capacitors on the host of the TMUXHS4412. Option (c) showcases where the TMUXHS4412 is AC-coupled on both sides. VBIAS must be within the valid CMV of the device.



7-1. AC-Coupling Capacitors Placement Options Between Host and Device / Endpoint

7.2 Typical Applications

7.2.1 PCIe Lane Muxing

The TMUXHS4412 can be used to switch PCIe lanes between two slots. In many PC and server motherboards, the CPU does not have enough PCIe lanes to provide desired system flexibility for end customers. In such applications, the TMUXHS4412 can be used to switch PCIe TX and RX lanes between two slots. 7-2 provides a schematic where four TMUXHS4412 are used to switch eight PCIe lanes (8-TX and 8-RX channels). Note the common-mode voltage (CMV) bias for the TMUXHS4412 must be within the valid range. In implementations where receiver CMV bias of a PCIe root complex or an end point can not be ensured within the CMV range, additional DC-blocking capacitors and appropriate CMV biasing must be implemented. One side of the device has AC-coupling capacitors. Additionally the PD pin must be low for device to work. This pin can be driven by a processor.

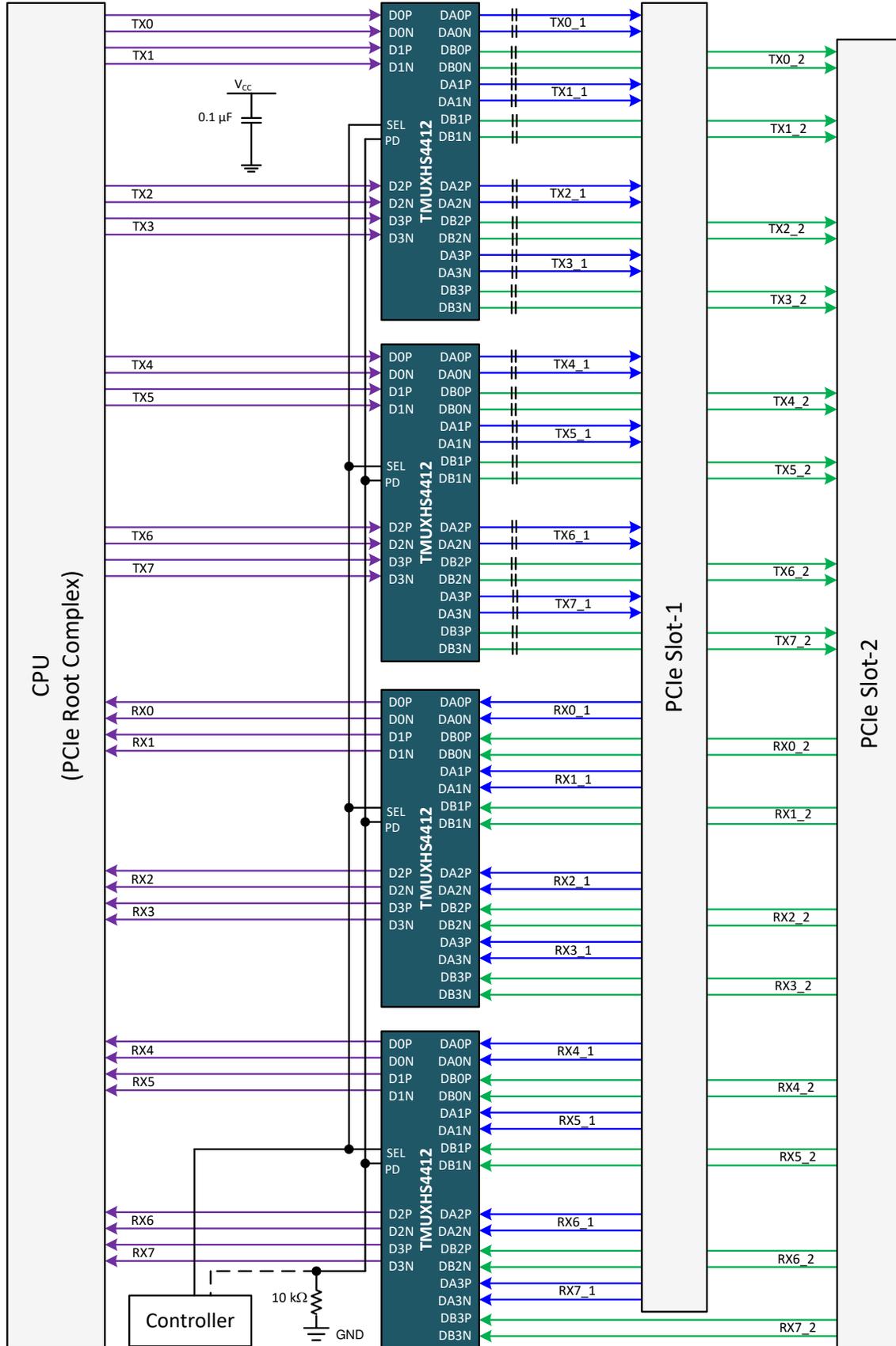


図 7-2. PCIe Lane Muxing

7.2.1.1 Design Requirements

表 7-1 provides various parameters and the expected values to implement the PCIe lane switching topology. Note the recommendation is for illustration purpose only.

表 7-1. Design Parameters

DESIGN PARAMETER	VALUE (V _{CC} = 3.3V)	VALUE (V _{CC} = 1.8V)
Dx[P/N], DAx[P/N], DBx[P/N] CM input voltage	0V to 1.8V	0V to 0.9V Must be biased from Dx[P/N] side)
SEL/PD pin max voltage for low	<0.25 × V _{CC}	
SEL/PD pin min voltage for high	>0.75 × V _{CC}	
AC coupling capacitor for PCIe TX pins	75nF to 265nF	
Decoupling capacitor for V _{CC}	0.1μF	

7.2.1.2 Detailed Design Procedure

The TMUXHS4412 is a high-speed passive switch device that can behave as a mux or demux. The TMUXHS4412 is a passive switch that provides no signal conditioning capability, therefore signal integrity is important. To implement PCIe lane switching topology, the designer must understand the following.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Provide a control signal for the SEL and PD pins.
- The thermal pad must be connected to ground.
- See the application schematics on recommended decouple capacitors from V_{CC} pins to ground.

7.2.1.3 Pin-to-Pin Passive Versus Redriver Option

For 8-lane PCIe lane muxing application a topology with four TMUXHS4412 devices is illustrated. TMUXHS4412 is a passive mux/demux component that does not provide any signal conditioning. If a specific board implementation has too much loss from CPU to PCIe CEM connectors, a signal conditioning device such as linear redriver may be required for best fidelity of the PCIe link. DS160PR421 is a PCIe 4.0 linear redriver with integrated mux and DS160PR412 is a PCIe 4.0 linear redriver with integrated demux. Both of these devices are pin-to-pin (p2p) compatible with the TMUXHS4412, which allows an easy transition if signal conditioning function is needed to extend the PCIe link reach. 図 7-3 illustrates p2p passive versus redriver option to implement PCIe lane switching.

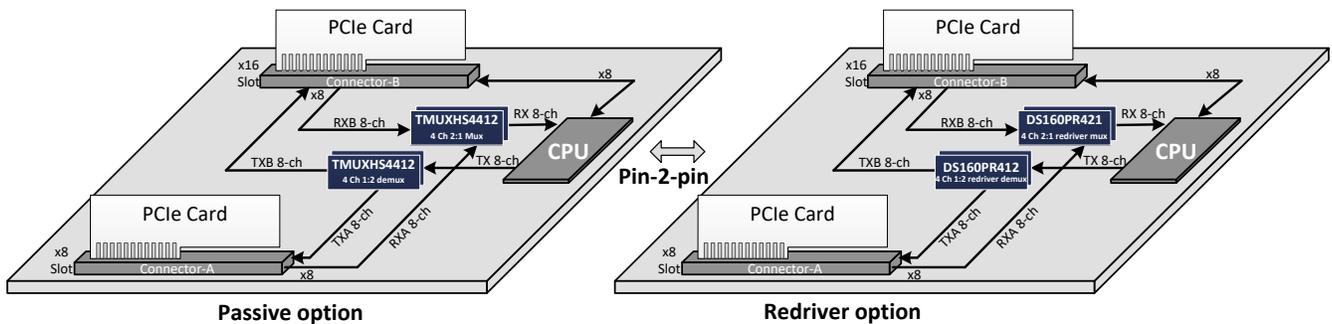


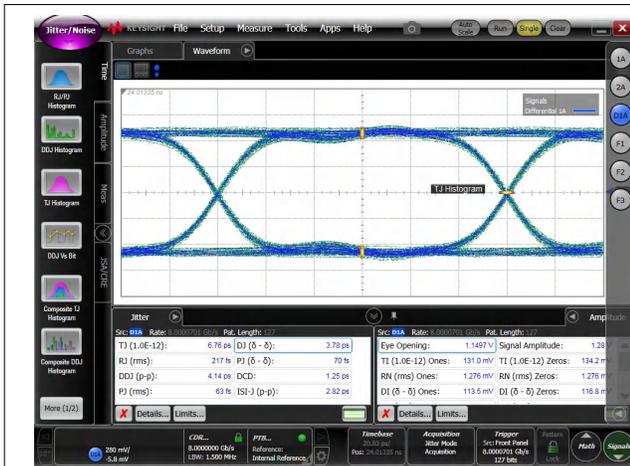
図 7-3. Pin-to-Pin Passive vs Redriver Option for PCIe Lane Switching

TMUXHS4412

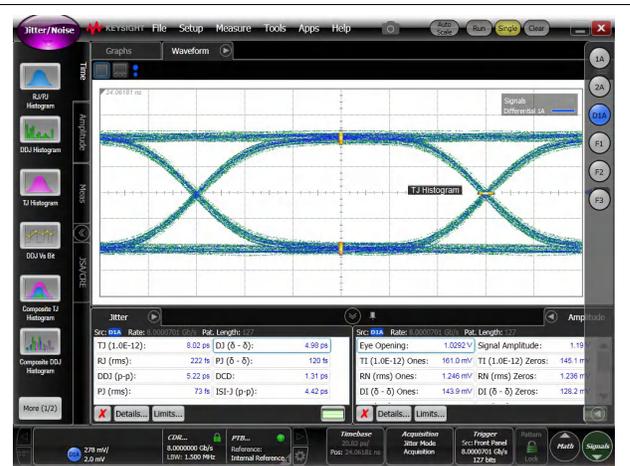
JAJSKW6A – DECEMBER 2020 – REVISED OCTOBER 2024

7.2.1.4 Application Curves

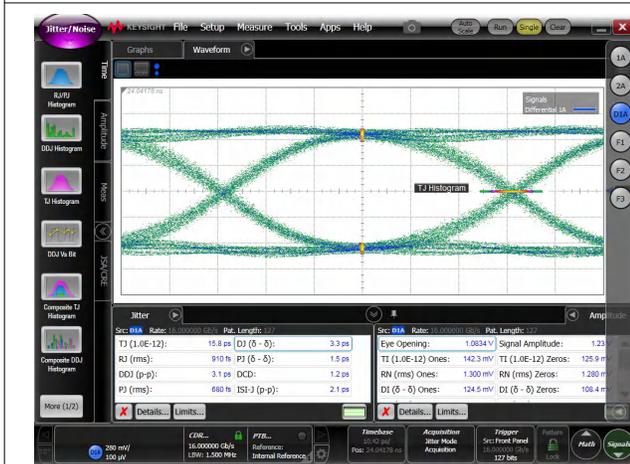
The following figures show the eye diagrams for PRBS-7 signals through calibration trace and TMUXHS4412 for PCIe 3.0 (8Gbps) and PCIe 4.0 (16Gbps), respectively.



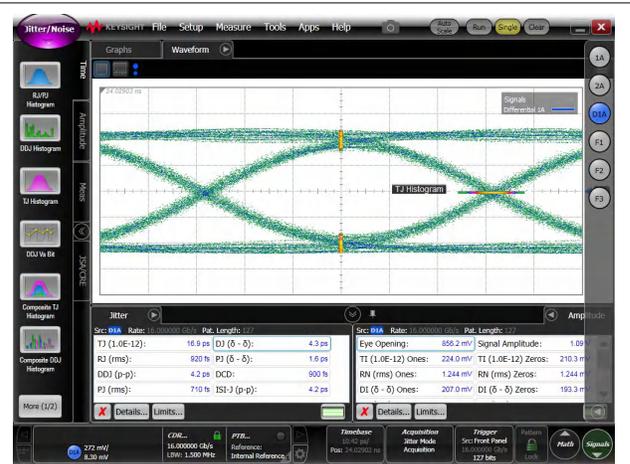
7-4. 8Gbps PRBS-7 Signals in TI Evaluation Board Through Calibration Traces



7-5. 8Gbps PRBS-7 Signals in TI Evaluation Board Through a Typical TMUXHS4412 Channel



7-6. 16Gbps PRBS-7 Signals in TI Evaluation Board Through Calibration Traces



7-7. 16Gbps PRBS-7 Signals in TI Evaluation Board Through a Typical TMUXHS4412 Channel

7.3 Systems Examples

7.3.1 PCIe Muxing for Hybrid SSD

Figure 7-8 illustrates a use case where a hybrid SSD is shared by CPU and an IO expander (PCH).

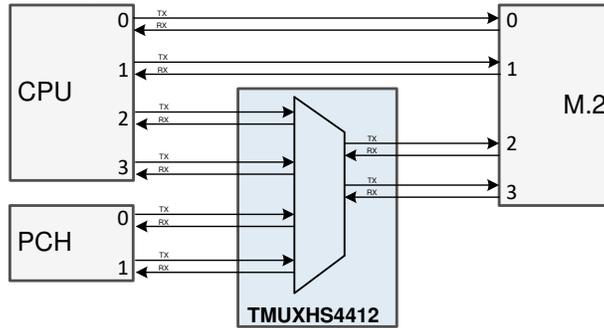


Figure 7-8. PCIe Muxing to M.2 Connectivity for Hybrid SSD

7.3.2 DisplayPort Main Link

Figure 7-9 shows an application block diagram to implement DisplayPort (DP) main link switch either in mux or demux configuration. Note DP link also has sideband signals such as Auxiliary (AUX) and Hot Plug Detect (HPD) which must be switched outside of this device.

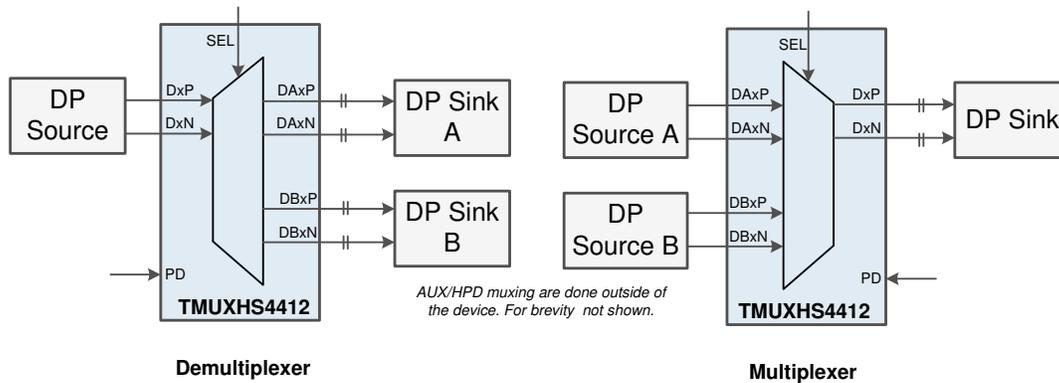


Figure 7-9. DisplayPort Main Link Demultiplexing/Multiplexing

7.3.3 USB 4.0 / TBT 3.0 Demuxing

Figure 7-10 shows an application block diagram where TMUXHS4412 is used to demultiplex USB 4.0 / TBT 3.0 TX and RX signals. Note SBU signals within USB-C interface must be switched outside of this device.

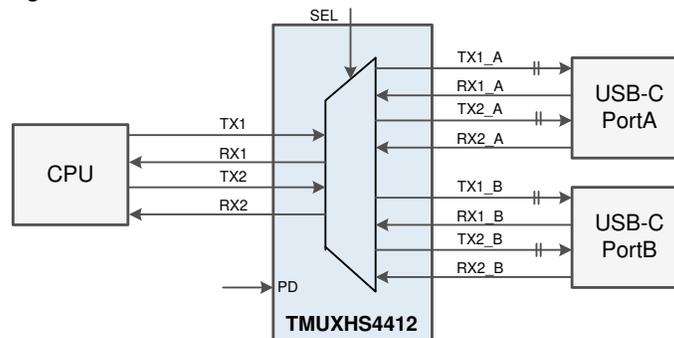


Figure 7-10. USB 4.0 / TBT 3.0 Demultiplexing

7.4 Power Supply Recommendations

The TMUXHS4412 does not require a power supply sequence. However, TI recommends that PD is asserted low after device supply V_{CC} is stable and in specification. TI also recommends to place ample decoupling capacitors at the device V_{CC} near the pin.

7.5 Layout

7.5.1 Layout Guidelines

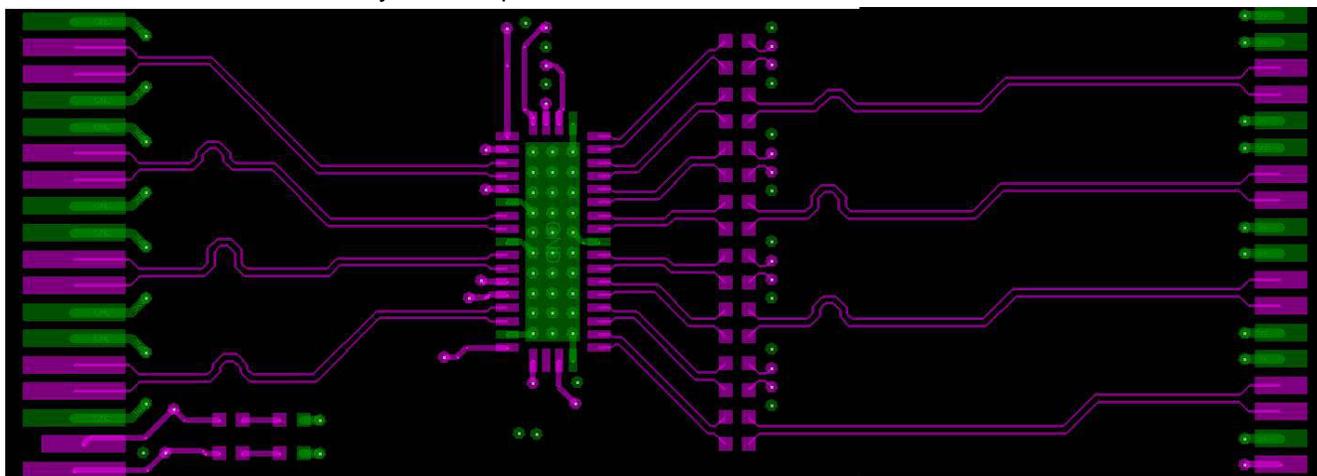
On a high-K board, TI always recommends to solder the PowerPAD™ integrated circuit package onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD integrated circuit package. On a high-K board, the TMUXHS4412 can operate over the full temperature range by soldering the Power-pad onto the thermal land without vias.

For high speed layout guidelines refer to the [High-Speed Layout Guidelines for Signal Conditioners and USB Hubs application note](#).

On a low-K board, for the device to operate across the temperature range, the designer must use a 1oz Cu trace connecting the GND pins to the thermal land. A general PCB design guide for PowerPAD integrated circuit packages is provided in [PowerPAD™ Thermally Enhanced Package application note](#).

7.5.2 Layout Example

☒ 7-11 shows TMUXHS4412 layout example.



☒ 7-11. TMUXHS4412 Layout Example

☒ 7-12 shows a layout illustration here four TMUXHS4412 is used to switch eight PCIe lanes between two PCIe connectors.

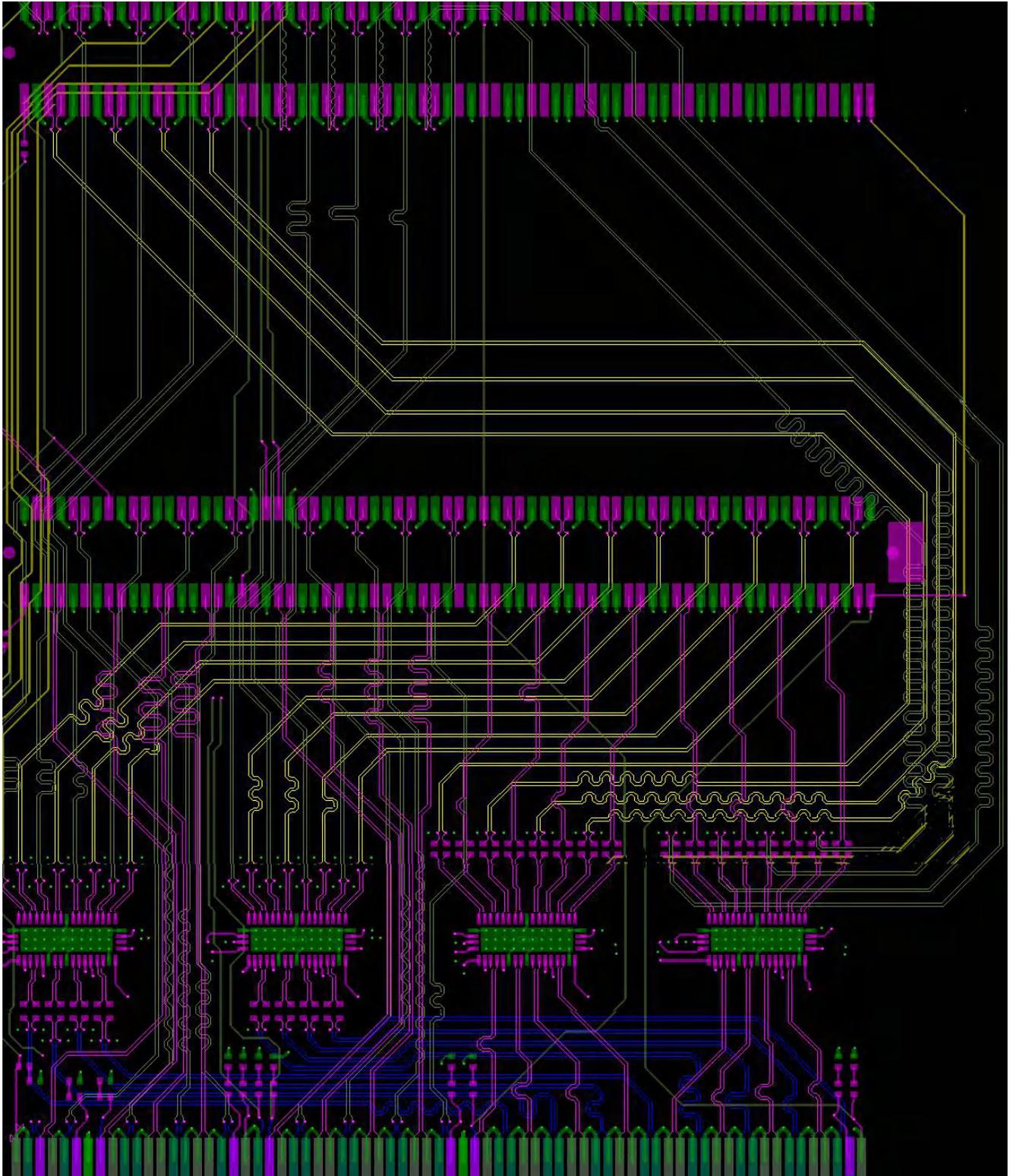


図 7-12. Layout Example for PCIe Lane Muxing Application

8 Device and Documentation Support

8.1 Related Documentation

8.1.1 Documentation Support

For related documentation, see the following:

- Texas Instruments, [DS160PR412 PCIe® 4.0 16Gbps 4-Channel Linear Redriver with Integrated 1:2 Demux data sheet](#)
- Texas Instruments, [DS160PR421 PCIe® 4.0 16Gbps 4-Channel Linear Redriver with Integrated 2:1 Mux data sheet](#)
- Texas Instruments, [High-Speed Layout Guidelines for Signal Conditioners and USB Hubs application note](#)
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package application note](#)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

8.4 Trademarks

PowerPAD™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2020) to Revision A (October 2024)

Page

- | | |
|--|---|
| • Changed Charged-device model (CDM) value from 250V to 1000V..... | 5 |
|--|---|

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUXHS4412IRUAR	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HS4412
TMUXHS4412IRUAR.A	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HS4412
TMUXHS4412IRUAT	Active	Production	WQFN (RUA) 42	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HS4412
TMUXHS4412IRUAT.A	Active	Production	WQFN (RUA) 42	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HS4412
TMUXHS4412RUAR	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS4412
TMUXHS4412RUAR.A	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS4412
TMUXHS4412RUAT	Active	Production	WQFN (RUA) 42	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS4412
TMUXHS4412RUAT.A	Active	Production	WQFN (RUA) 42	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS4412

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXHS4412IRUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TMUXHS4412IRUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TMUXHS4412RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TMUXHS4412RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXHS4412IRUAR	WQFN	RUA	42	3000	367.0	367.0	35.0
TMUXHS4412IRUAT	WQFN	RUA	42	250	210.0	185.0	35.0
TMUXHS4412RUAR	WQFN	RUA	42	3000	367.0	367.0	35.0
TMUXHS4412RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

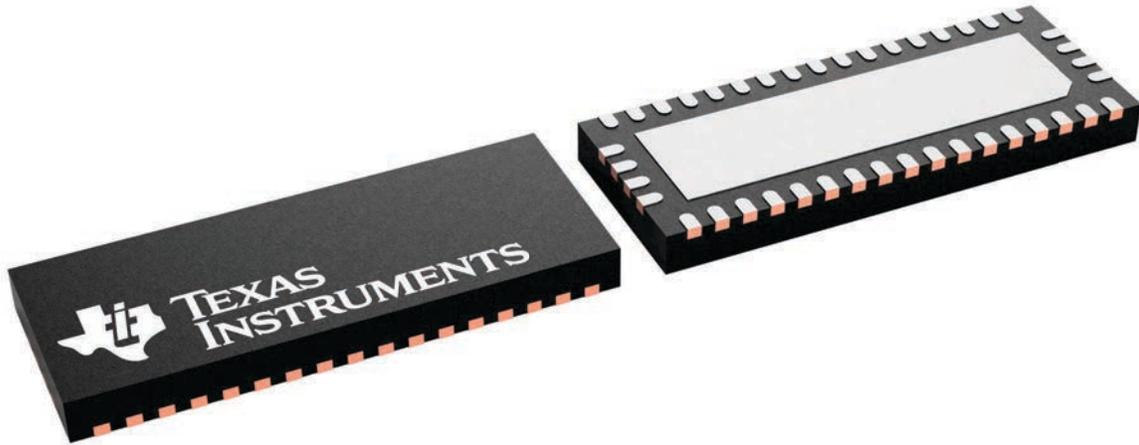
RUA 42

WQFN - 0.8 mm max height

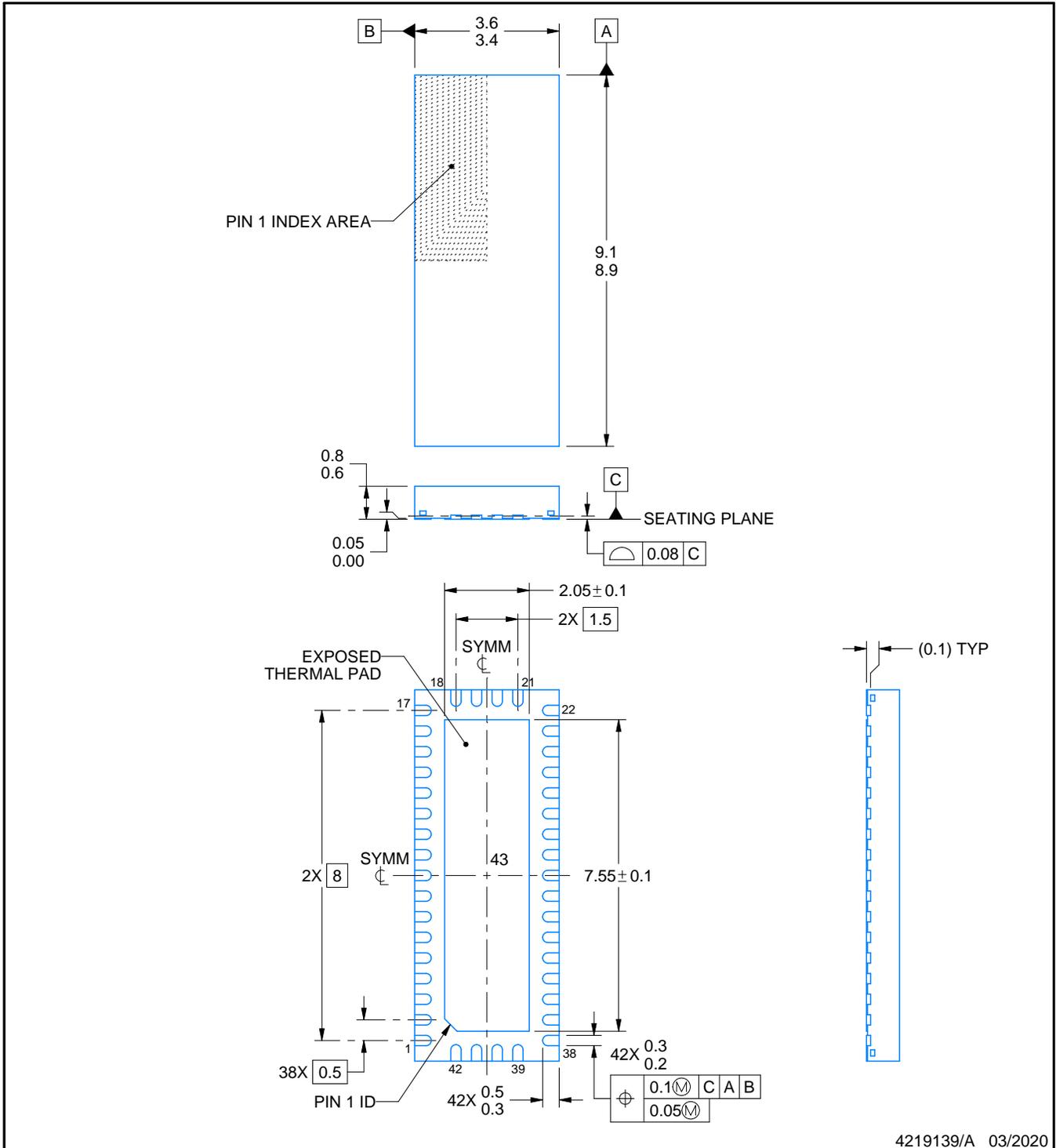
9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A



4219139/A 03/2020

NOTES:

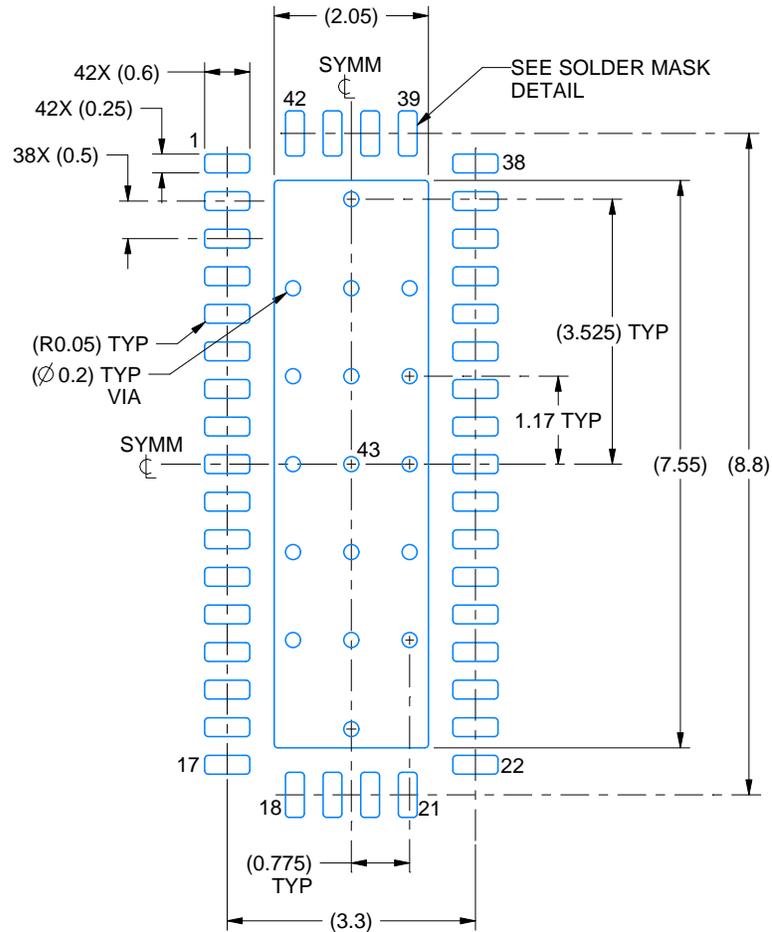
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

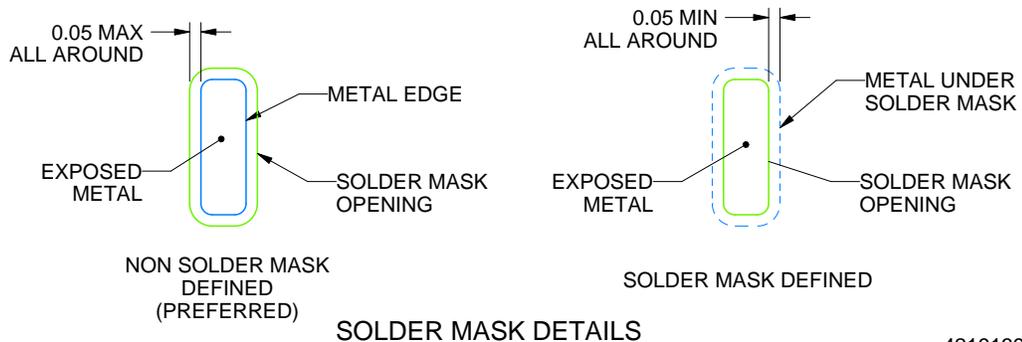
RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4219139/A 03/2020

NOTES: (continued)

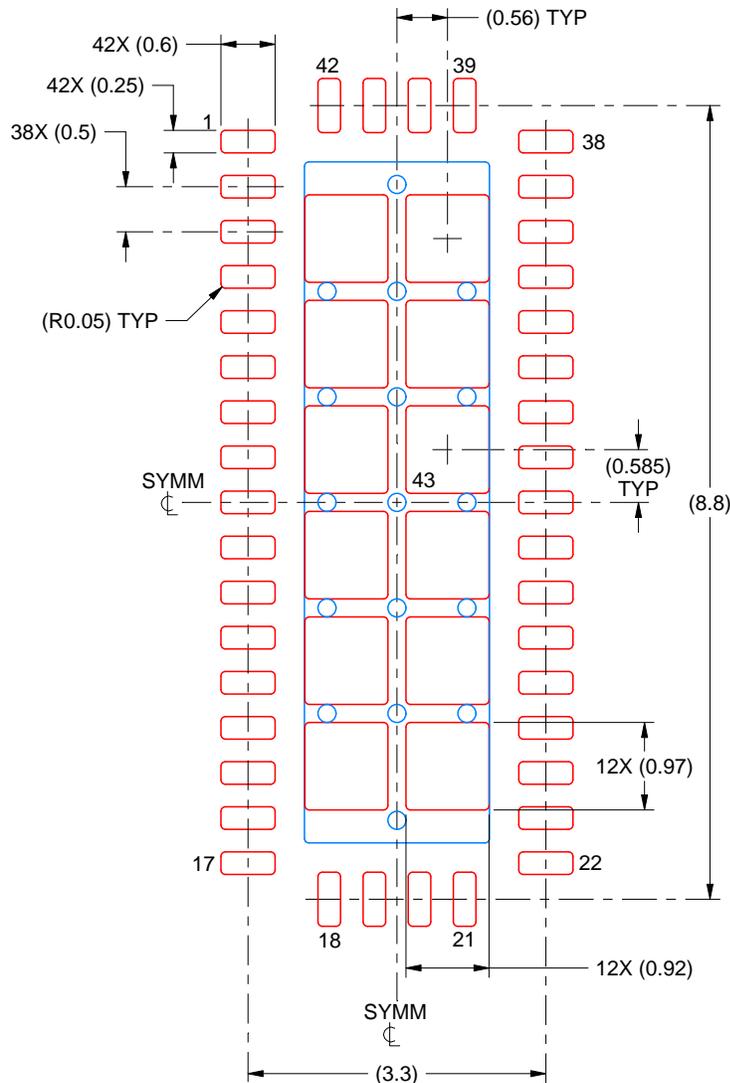
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日 : 2025 年 10 月