TPD1S514x V_{BUS} ピン用の過電圧、サージ、ESD 保護機能搭載 USB チャージャ・ファミリ

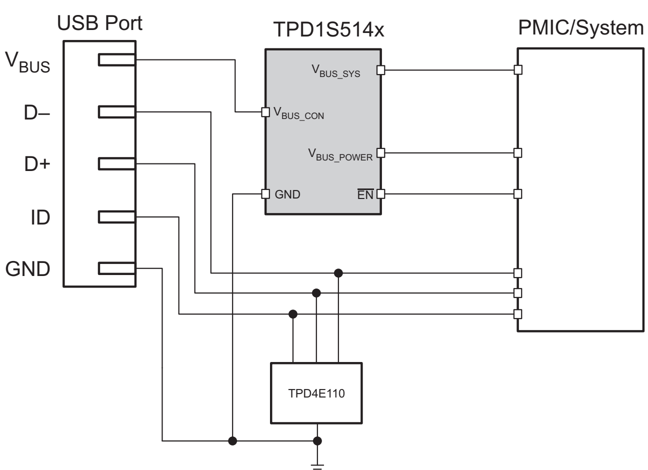
1 特長

- V_{BUS_CON} で最大 DC 30V の過電圧保護
- 高精度の OVP (許容誤差 ±1% 未満)
- 低 R_{ON} の nFET スイッチで、ホストおよび充電モードに対応
- 専用の V_{BUS_POWER} ピンにより、デッド・バッテリ状態での柔軟な起動オプションを提供
- V_{BUS} ラインの過渡保護
  - IEC 61000-4-2 接触放電 ±15kV
  - IEC 61000-4-2 エアーギャップ放電 ±15kV
  - IEC 61000-4-5 開路電圧 100V
    - 高精度のクランプ回路により、V_{BUS_SYS} 電圧を V_{OVP} 未満に制限
- USB 突入電流に準拠
- サーマル・シャットダウン (TSD) 機能

2 アプリケーション

- 携帯電話
- タブレット
- 電子書籍
- 携帯用メディア･プレーヤ
- 5V、9V、12V の電源レール

TPD1S514 ファミリの回路保護方式



3 概要

TPD1S514 ファミリは、5V、9V、12V の USB V_{BUS} ライン、または他の電力バス用の、シングル･チップ保護ソリューションで構成されます。双方向 nFET スイッチにより、V_{BUS_CON} ピンのいかなる過電圧条件からも内部システム回路を保護しながら、充電とホストのどちらのモードでも安全な電流フローを保証します。V_{BUS_CON} ピンでは、このデバイスは最大 DC 30V の過電圧保護に対応できます。$\overline{EN}$ ピンが LOW になった後、TPD1S514 ファミリのすべてのデバイスはソフトスタート遅延により 20ms 待ってから nFET をオンにします。

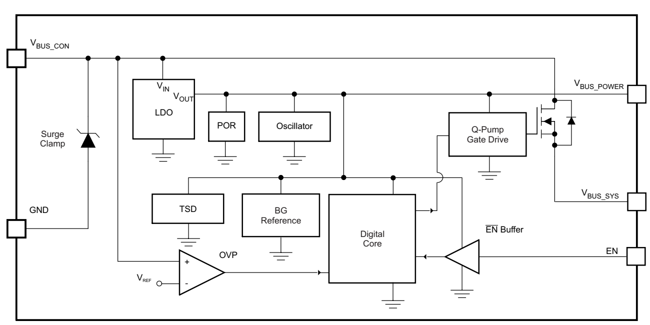
TPD1S514 ファミリの代表的なアプリケーション･インターフェイスは、携帯電話、タブレット、電子書籍、携帯用メディア･プレーヤなどで一般的に使用されている USB 接続の V_{BUS} ラインです。また TPD1S514 ファミリは、5V、9V、12V 電源レールのインターフェイスを使用する任意のシステムに使用可能です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPD1S514x	WCSP (12)	1.29mm × 1.99mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

TPD1S514 ファミリのブロック図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (October 2015) から Revision F に変更	**Page**
• Changed I_{POWER} from 1 mA to 10 mA in the *Absolute Maximum Ratings* table	4

Revision D (July 2015) から Revision E に変更	**Page**
• TPD1S514-3 のプレビュー・ステータスを削除	1
• Changed Max value of I_{VBUS_SLEEP} PARAMETER for TPD1S514-3 (Preview) from 308 µA to 335 µA.	5
• Updated TEST CONDITIONS for T_{OFF_DELAY} PARAMETER.	8

Revision C (July 2015) から Revision D に変更	**Page**
• TPD1S514 および TPD1S514-3 (プレビュー) 追加	1

Revision B (September 2014) から Revision C に変更	**Page**
• プレビューの TPD1S514-3 と、「特長」のプログラム可能性の記述を削除	1

Revision A (July 2014) から Revision B に変更	**Page**
• 丸め誤差を修正するため本体サイズを 変更	1

2014年4月発行のものから更新	**Page**
• TPD1S514-2 のプレビュー・ステータスを削除	1
• Updated Device Comparison table.	3
• Updated Electrical Characteristics OVP Circuit table.	7

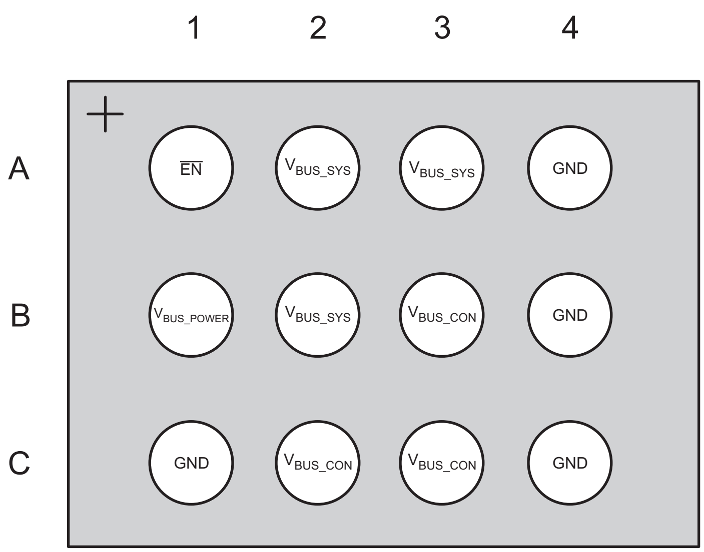
5 Device Comparison Table

TPD1S514 Family	V_{OVP} (V)			V_{OVP_HYS} (mV)	V_{BUS_POWER} (V)(1)		T_Startup delay (ms) options	T_Soft Start (ms) options
	MIN	TYP	MAX	TYP	MIN	TYP	TYP	TYP
TPD1S514-1	5.9	5.95	5.99	100	4.7	4.95	20	3.5
TPD1S514-2	9.9	9.98	10.05	100	4.7	4.95		
TPD1S514-3	13.5	13.75	14	100	4.7	4.95		
TPD1S514	5.9	5.95	5.99	20	6.2	6.48		

(1) With V_{BUS_CON} > 6.5V. See Sections *V_{BUS_POWER}, TPD1S514-1, TPD1S514-2, TPD1S514-3* and *V_{BUS_POWER}, TPD1S514* for full description.

6 Pin Configuration and Functions

YZ Package
12-Pin WCSP
Top Side, See Through View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	A1	I	Enable Active-Low Input. Drive $\overline{EN}$ low to enable the switch. Drive $\overline{EN}$ high to disable the switch.
V_{BUS_POWER}	B1	O	5-V Power source controlled by V_{BUS_CON}.
V_{BUS_SYS}	A2, A3, B2	I/O	Connect to internal VBUS plane.
V_{BUS_CON}	B3, C2, C3	I/O	Connect to USB connector VBUS pin; IEC 61000-4-2 ESD protection and IEC 61000-4-5 Surge protection.
GND	A4, B4, C1, C4	G	Connect to PCB ground plane.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector		–0.3	30	V
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB		–0.3	20	V
I_{BUS}	Continuous input current on V_{BUS_CON} pin(3)			3.5	A
I_{OUT}	Continuous output current on V_{BUS_CON} pin(3)			3.5	A
I_{PEAK}	Peak Input and Output Current on V_{BUS_CON}, V_{BUS_SYS} pin (10 ms)			8	A
I_{DIODE}	Continuous forward current through the FET body diode			1	A
I_{POWER}	Continuous current through V_{BUS_POWER}			10	mA
$V_{\overline{EN}}$	Voltage on Input pin ($\overline{EN}$)			7	V
V_{BUS_POWER}	Continuous Voltage at V_{BUS_POWER}	TPD1S514-1		See(4)	V
		TPD1S514-2		See(4)	
		TPD1S514-3		See(4)	
		TPD1S514		See(4)	
	IEC 61000-4-5 open circuit voltage (t_p = 1.2/50 µs)	V_{BUS_CON} pin		100	V
	IEC 61000-4-5 peak pulse current (t_p = 8/20µs)	V_{BUS_CON} pin		30	A
	IEC 61000-4-5 peak pulse power (t_p = 8/20µs)	V_{BUS_CON} pin		900	W
C_{LOAD}	Output load capacitance	V_{BUS_SYS} pin	0.1	100	µF
C_{CON}	Input capacitance	V_{BUS_CON} pin	0.1	50	µF
C_{POW}	V_{BUS_POWER} capacitance	V_{BUS_POWER} pin	0.1	4.7	µF
T_A	Operating free air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) Thermal limits and power dissipation limits must be observed.
(4) 6.9 V or V_{BUS_CON} + 0.3 V, whichever is smaller.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±500	
		IEC 61000-4-2 Contact Discharge	V_{BUS_CON} pin	±15000	
		IEC 61000-4-2 Air-gap Discharge	V_{BUS_CON} pin	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector	TPD1S514-1	3.5	5	5.9	V
		TPD1S514-2	3.5	9	9.9	
		TPD1S514-3	3.5	12	13.5	
		TPD1S514	3.5	5	5.9	
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB	TPD1S514-1	3.9	5	5.9	V
		TPD1S514-2	3.9	9	9.9	
		TPD1S514-3	3.9	12	13.5	
		TPD1S514	3.9	5	5.9	
C_{LOAD}	Output load capacitance	V_{BUS_SYS} pin		2.2		µF
C_{CON}	Input capacitance	V_{BUS_CON} pin		1		µF
C_{POWER}	Capacitance on V_{BUS_POWER}	V_{BUS_POWER} pin		1		µF
T_A	Operating free-air temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPD1S514 Family YZ (WCSP) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Supply Current Consumption

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		DEVICE NAME	TYP	MAX	UNIT
I_{VBUS_SLEEP}	V_{BUS_CON} Operating Current Consumption	Measured at V_{BUS_CON} pin, $\overline{EN}$ = 5 V	V_{BUS_CON} = 5 V	TPD1S514-1	150	245	µA
			V_{BUS_CON} = 9 V	TPD1S514-2	176	281	
			V_{BUS_CON} = 12 V	TPD1S514-3	195	335	
			V_{BUS_CON} = 5 V	TPD1S514	150	245	
I_{VBUS}		Measured at V_{BUS_CON} pin, $\overline{EN}$ = 0 V and no load	V_{BUS_CON} = 5 V	TPD1S514-1	228	354	µA
			V_{BUS_CON} = 9 V	TPD1S514-2	250	413	
			V_{BUS_CON} = 12 V	TPD1S514-3	270	456	
			V_{BUS_CON} = 5 V	TPD1S514	228	354	
I_{VBUS_SYS}	V_{BUS_SYS} operating current consumption	Measured at V_{BUS_SYS} pin, V_{BUS_CON} = Hi-Z, $\overline{EN}$ = 0 V	V_{BUS_SYS} = 5 V	TPD1S514-1	210	354	µA
			V_{BUS_SYS} = 9 V	TPD1S514-2	250	424	
			V_{BUS_SYS} = 12 V	TPD1S514-3	333	461	
			V_{BUS_SYS} = 5 V	TPD1S514	210	354	
I_{HOST_LEAK}	Host mode leakage current	Measured at V_{BUS_SYS} pin, V_{BUS_CON} = Hi-Z, $\overline{EN}$ = 5 V	V_{BUS_SYS} = 5 V	TPD1S514-1	90	218	µA
			V_{BUS_SYS} = 9 V	TPD1S514-2	290	491	
			V_{BUS_SYS} = 12 V	TPD1S514-3	506	696	
			V_{BUS_SYS} = 5 V	TPD1S514	90	218	

7.6 Electrical Characteristics $\overline{EN}$ Pin

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	$\overline{EN}$	V_{BUS_CON} = 5 V	1.2		6	V
V_{IL}	Low-level input voltage	$\overline{EN}$	V_{BUS_CON} = 5 V	0		0.8	V
I_{IL}	Input leakage current	$\overline{EN}$	$V_{\overline{EN}}$ = 0 V, V_{BUS_CON} = 5 V			1	µA
I_{IH}	Input leakage current	$\overline{EN}$	$V_{\overline{EN}}$ = 5 V, V_{BUS_CON} = 5 V			10	µA

7.7 Thermal Shutdown Feature

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHDN}	Thermal shutdown	V_{BUS_CON} = 5 V, $\overline{EN}$ = 0 V, Junction temperature decreases from thermal shutdown level until the nFET switch turns off.		145		°C
Thermal shutdown hysteresis		V_{BUS_CON} = 5 V, $\overline{EN}$ = 0 V, Junction temperature decreases from thermal shutdown level until the nFET switch turns on.		25		°C

7.8 Electrical Characteristics nFET Switch

T = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{ON}	Switch ON resistance	V_{BUS_CON} = 5 V, I_{OUT} = 1 A	TPD1S514-1		39	50	mΩ
		V_{BUS_CON} = 9 V, I_{OUT} = 1 A	TPD1S514-2		39	50	
		V_{BUS_CON} = 12 V, I_{OUT} = 1 A	TPD1S514-3		39	50	
		V_{BUS_CON} = 5 V, I_{OUT} = 1 A	TPD1S514		39	50	

7.9 Electrical Characteristics OVP Circuit

T = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OVP}	Input voltage protection threshold	V_{BUS_CON}	V_{BUS_CON} increasing from 0 V to 20 V	TPD1S514-1	5.90	5.95	5.99	V
				TPD1S514-2	9.9	9.98	10.05	
				TPD1S514-3	13.5	13.75	14	
				TPD1S514	5.90	5.95	5.99	
V_{HYS_OVP}	Hysteresis on OVP	V_{BUS_CON}	V_{BUS_CON} decreasing from 20 V to 0 V	TPD1S514-1		100		mV
				TPD1S514-2		100		
				TPD1S514-3		100		
				TPD1S514		20		
V_{UVLO}	Input under voltage lockout	V_{BUS_CON}	V_{BUS_CON} voltage rising from 0 V to 5 V		2.7	3.1	3.5	V
V_{HYS_UVLO}	Hysteresis on UVLO	V_{BUS_CON}	Difference between rising and falling UVLO thresholds			80		mV
$V_{UVLO\_FALLING}$	Input undervoltage lockout	V_{BUS_CON}	V_{BUS_CON} voltage falling from 5 V to 0 V		2.6	3.0	3.4	V
V_{UVLO_SYS}	V_{BUS_SYS} undervoltage lockout	V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0 V to 5 V		2.8	3.7	4.3	V
$V_{HYS\_UVLO\_SYS}$	V_{BUS_SYS} UVLO Hysteresis	V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}			500		mV
$V_{UVLO\_SYS\_FALLING}$	V_{BUS_SYS} undervoltage lockout	V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 5 V to 0 V		2.6	3.0	3.4	V

7.10 Electrical Characteristics V_{BUS_POWER} Circuit

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CLAMP}	Output voltage on V_{BUS_POWER} during OVP	V_{BUS_CON} = 20 V	TPD1S514-1		5.0	5.5	V
			TPD1S514-2		5.0	5.5	
			TPD1S514-3		5.0	5.5	
			TPD1S514		6.48	6.68	
V_{BUS_POWER}	Output voltage on V_{BUS_POWER} during normal operation	V_{BUS_CON} = 5 V, I_{BUS_POWER} = 1 mA;	TPD1S514-1	4.7	4.95		V
			TPD1S514-2	4.7	4.95		
			TPD1S514-3	4.7	4.95		
			TPD1S514	4.7	4.98		
$I_{BUS\_POWER\_MAX}$	Output current on V_{BUS_POWER}	V_{BUS_CON} = 5 V – 15 V				3	mA

7.11 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DELAY}	USB charging turn-ON Delay	Measured from $\overline{EN}$ asserted LOW to nFET begins to Turn ON, excludes soft-start time	TPD1S514-1		20		ms
			TPD1S514-2				
			TPD1S514-3				
			TPD1S514				
t_{SS}	USB charging rise time (soft-start delay)	Force 5 V on VBUS_CON, measured from V_{BUS_SYS} rises from 10% to 90% (with 1 MΩ load/ NO C_{LOAD})	TPD1S514-1		3.5		ms
			TPD1S514-2				
			TPD1S514-3				
			TPD1S514				
t_{OFF_DELAY}	USB charging turn-OFF time	Measured from $\overline{EN}$ asserted High to V_{BUS_SYS} falling to 10% with R_{LOAD} = 10 Ω and No C_{LOAD} on V_{BUS_SYS}	TPD1S514-1		5.5		µs
			TPD1S514-2				
			TPD1S514-3				
			TPD1S514				
OVER VOLTAGE PROTECTION							
$t_{OVP\_response}$	OVP response time	Measured from OVP Condition to FET Turn OFF[1]				100	ns

(1) Specified by design, not production tested

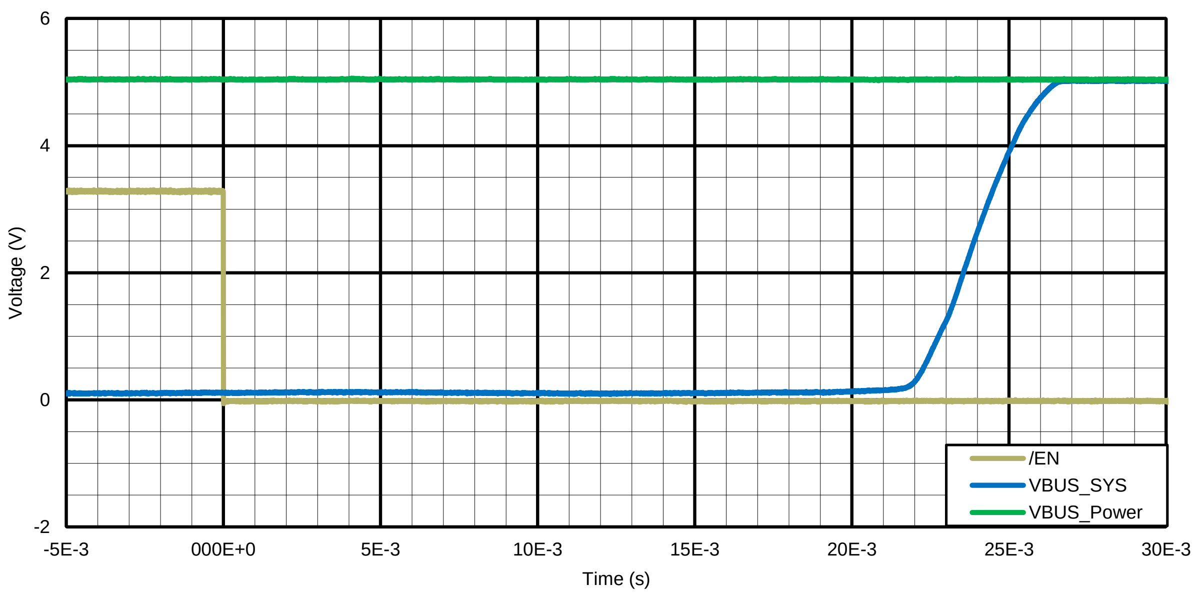


Figure 1. TPD1S514-1 Response to Set $\overline{EN}$ Low

7.12 TPD1S514-1 Typical Characteristics

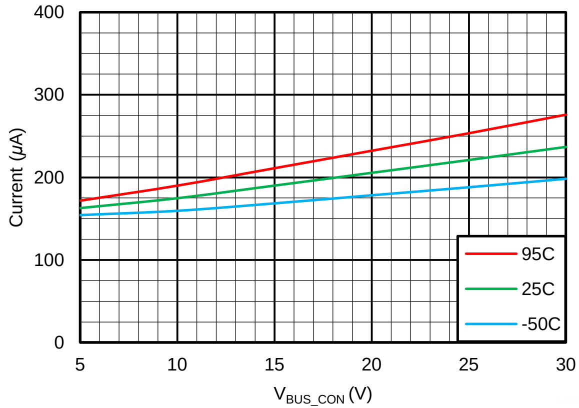


Figure 2. In Supply Current vs Supply Voltage

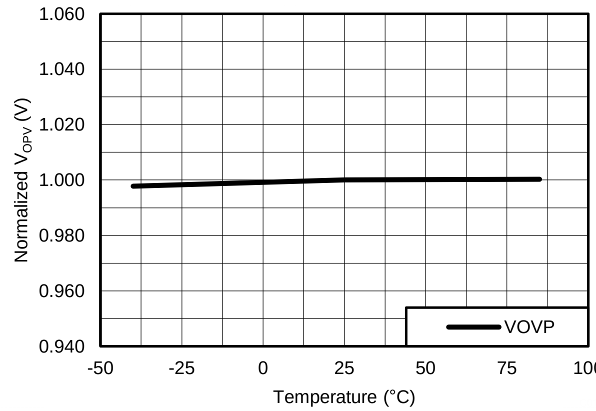


Figure 3. Normalized V_{OVP} vs Temperature

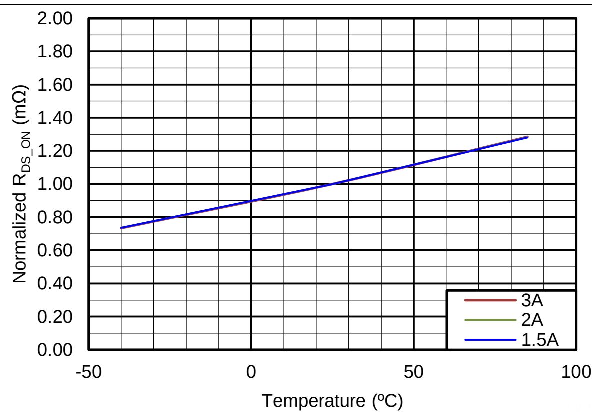


Figure 4. Normalized R_{ON} vs Temperature

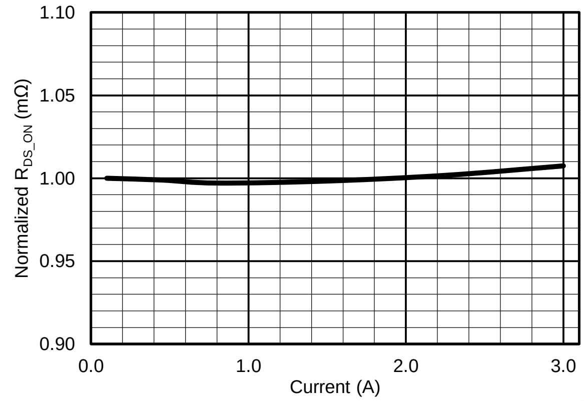


Figure 5. Normalized R_{ON} vs Output

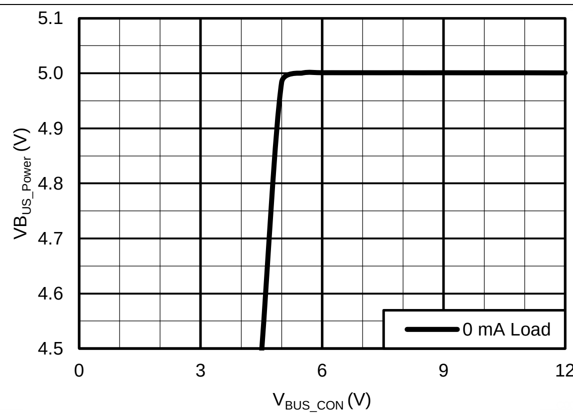


Figure 6. V_{BUS_POWER} vs V_{BUS_CON} With No Load

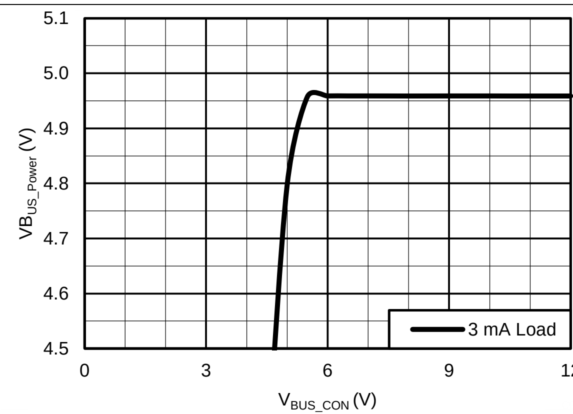


Figure 7. V_{BUS_POWER} vs V_{BUS_CON} With 3 mA Load

TPD1S514-1 Typical Characteristics (continued)

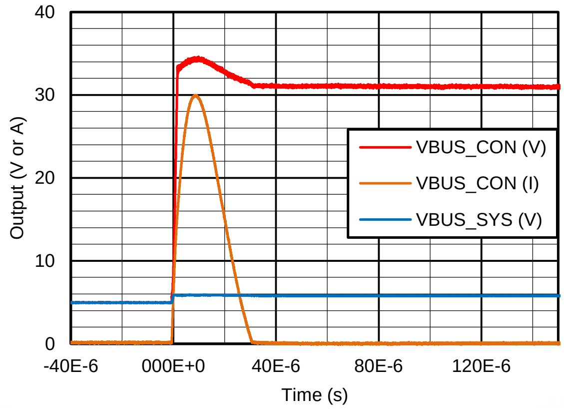


Figure 8. 100 V Surge With Device

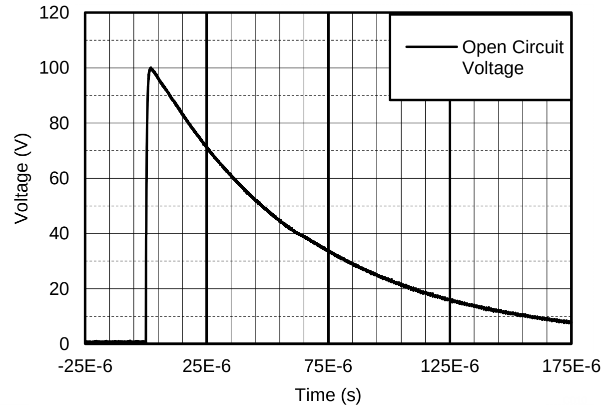


Figure 9. 100 V Surge Without Device

8 Detailed Description

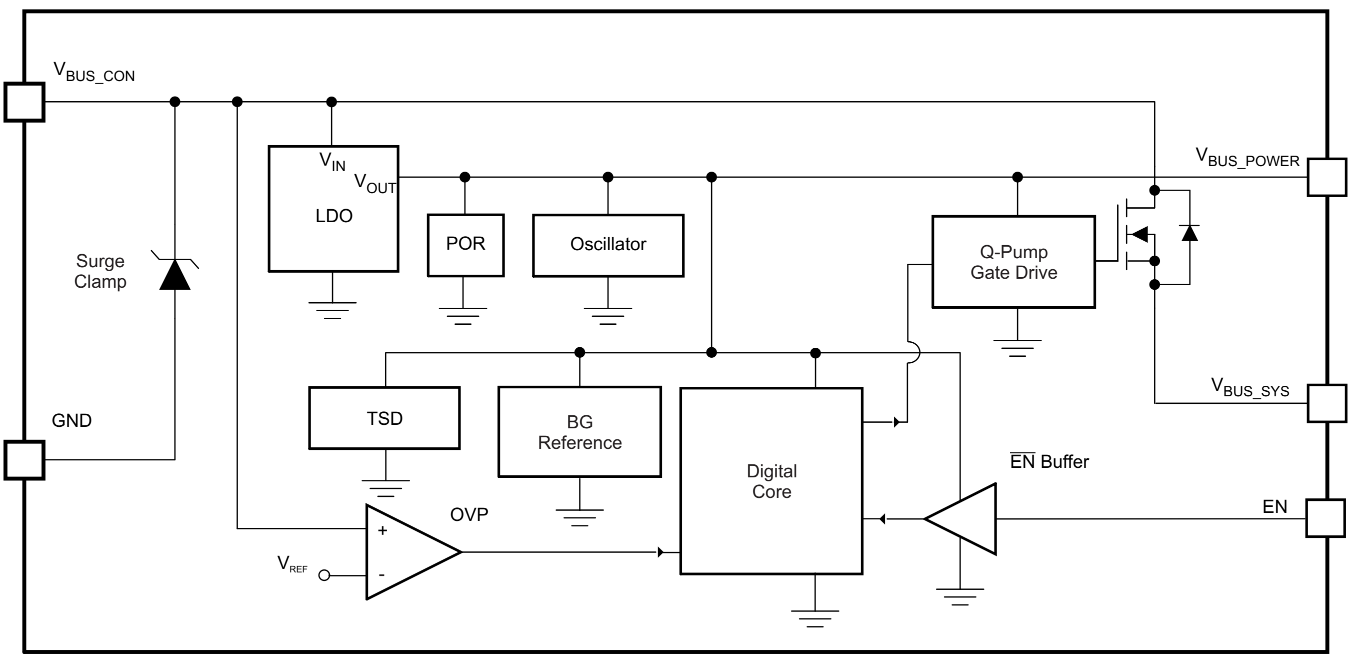
8.1 Overview

The TPD1S514 Family provides single-chip ESD, surge, and over voltage protection solutions for portable USB Charging and Host interfaces. Each device offers over voltage protection at the V_{BUS_CON} pin up to 30-V DC. The TPD1S514 Family offers an ESD and Precision Clamp for the V_{BUS_CON} pin, thus eliminating the need for external TVS clamp circuits in the application.

Each device has an internal oscillator and charge pump which controls turning ON the internal nFET switch. The internal oscillator controls the timers which enable the charge pump. If V_{BUS_CON} is less than V_{OVP}, the internal charge pump is enabled. After a 20 ms internal delay, the charge-pump starts-up, and turns ON the internal nFET switch through a soft start. If at any time V_{BUS_CON} rises above V_{OVP}, the nFET switch is turned OFF within 100 ns.

The TPD1S514 Family of devices also have a V_{BUS_POWER} pin which follows V_{BUS_CON} up to 4.9 V at 3 mA (except for TPD1S514, which follows V_{BUS_CON} up to 6.48 V, after which it is regulated to that voltage) to power the system from V_{BUS_CON}. In the case where the system battery state cannot power the system, voltage from an external charger can be provided to power the system. V_{BUS_POWER} is supplied by an always on LDO regulator supplied by V_{BUS_CON}. V_{BUS_POWER} output voltage remains regulated to 4.9 V (except for TPD1S514, which follows V_{BUS_CON} up to 6.48 V, after which it is regulated to that voltage) at up to 30-V DC on V_{BUS_CON} and during IEC 61000-4-5 surge events of up to 100 V open circuit voltage on V_{BUS_CON}.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Over Voltage Protection on V_{BUS_CON} up to 30 V DC

When the V_{BUS_CON} voltage rises above V_{OVP}, the internal nFET switch is turned OFF, removing power from the system side. V_{BUS_CON} can tolerate up to 30-V DC. The response to over voltage is very rapid, with the nFET switch turning off in less than 100 ns. When the V_{BUS_CON} voltage returns back to below $V_{OVP} – V_{HYS\_OVP}$, the nFET switch is turned ON again after an internal delay of t_{OVP_RECOV} (t_{DELAY}). This time delay ensures that the V_{BUS_CON} supply has stabilized before turning the switch back on. After t_{OVP_RECOV}, the TPD1S514 Family device turns on the nFET through a soft start. Once the OVP condition is cleared the nFET is turned completely ON.

Feature Description (continued)

8.3.2 Precision OVP (< ±1% Tolerance)

1% OVP trip threshold accuracy allows use of the entire input charging range while protecting sensitive system-side components from over voltage conditions.

8.3.3 Low R_{ON} nFET Switch Supports Host and Charging Mode

The nFET switch has a total on resistance (R_{ON}) of 39 mΩ. This equates to a voltage drop of less than 140 mV when charging at the maximum 3.5 A current level. Such low R_{ON} helps provide maximum potential to the system as provided by an external charger or by the system when in Host Mode.

8.3.4 V_{BUS_POWER}, TPD1S514-1, TPD1S514-2, TPD1S514-3

The V_{BUS_POWER} pin provides up to 3 mA and 5 V for powering the system using V_{BUS_CON}. V_{BUS_POWER} follows V_{BUS_CON} after 3.5 V and up to the regulated 5 V. In the case where the system battery state cannot power the system, voltage from an external charger can power the system. V_{BUS_POWER} is supplied by an always on LDO regulator supplied by V_{BUS_CON}. The V_{BUS_POWER} output voltage remains regulated to 5 V at up to 30-V DC on V_{BUS_CON} and during IEC 61000-4-5 surge events of up to 100 V.

8.3.5 V_{BUS_POWER}, TPD1S514

The V_{BUS_POWER} pin provides up to 3 mA and 6.48 V for powering the system using V_{BUS_CON}. V_{BUS_POWER} follows V_{BUS_CON} after 3.5 V and up to the regulated 6.48 V. In the case where the system battery state cannot power the system, voltage from an external charger can be provided to power the system. V_{BUS_POWER} is supplied by an always on LDO regulator supplied by V_{BUS_CON}. The V_{BUS_POWER} output voltage remains regulated to 6.48 V at up to 30-V DC on V_{BUS_CON} and during IEC 61000-4-5 surge events of up to 100 V.

8.3.6 Powering the System When Battery is Discharged

There are two methods for powering the system under a dead battery condition. Case 1: The $\overline{EN}$ pin can be tied to ground so that the nFET is always ON (when $V_{UVLO} < V_{BUS\_CON} < V_{OVP}$) and an external charger can power V_{BUS}. Case 2: If $\overline{EN}$ is controlled by a Power Management Unit (PMIC) or other logic, V_{BUS_POWER} can be used to power the PMIC. In Case 2, once the device is enabled, t_{DELAY} + t_{SS}, work together to meet the USB Inrush Current compliance.

8.3.7 ±15 kV IEC 61000-4-2 Level 4 ESD Protection

The V_{BUS_CON} pin can withstand ESD events up to ±15 kV Contact and Air-Gap. An ESD clamp diverts the current to ground.

8.3.8 100 V IEC 61000-4-5 µs Surge Protection

The V_{BUS_CON} pin can withstand surge events up to 100 V open circuit voltage (V_{PP}), or 900 W. A Precision Clamp diverts the current to ground and active circuitry switches OFF the nFET earlier than 100 ns before an over voltage can get through to V_{BYS_SYS}. The ultra-fast response time of the TPD1S514 Family holds the voltage on V_{BUS_SYS} to less than V_{OVP} during surge events of up to 100 V_{PP}.

8.3.9 Startup and OVP Recovery Delay

Upon startup or recovering from an over voltage, the TPD1S514 Family of devices have a built in startup delay. An internal oscillator controls a charge pump to control the delay. Once a manufactured pre-programmed time, t_{DELAY}, has elapsed, the charge pump is enabled which turns ON the nFET. A manufactured pre-programmed soft start, t_{SS}, is used when turning ON the nFET. Once the device is enabled, these start delays, t_{DELAY} + t_{SS}, work together to meet the USB Inrush Current compliance.

8.3.10 Thermal Shutdown

The TPD1S514 Family has an over-temperature protection circuit to protect against system faults or improper use. The basic function of the thermal shutdown (TSD) circuit is to sense when the junction temperature has exceeded the absolute maximum rating and shuts down the device until the junction temperature has cooled to a safe level.

8.4 Device Functional Modes

8.4.1 Operation With V_{BUS_CON} < 3.5 V (Minimum V_{BUS_CON})

The TPD1S514 Family operates normally (nFET ON) with input voltages above 3.5 V. The maximum UVLO voltage is 3.5 V and the device will operate at input voltages above 3.5 V. The typical UVLO voltage is 3.1 V and the device may operate at input voltages above that point. The device may also operate at input voltages as low as 2.7 V, the minimum UVLO. At input voltages between 0.6 V and 1.2 V, the state of output pins may not be controlled internally.

8.4.2 Operation With V_{BUS_CON} > V_{OVP}

The TPD1S514 Family operates normally (nFET ON) with input voltages below V_{OVP_min}. The typical OVP voltage is V_{OVP_TYP} and the device may operate at input voltages below that point. The device may also operate at input voltages as high as V_{OVP_MAX}.

Table 1. V_{OVP} Values

DEVICE NAME	V_{OVP}		
	MIN	TYP	MAX
TPD1S514-1	5.9	5.95	5.99
TPD1S514-2	9.9	9.98	10.05
TPD1S514-3	13.5	13.75	14
TPD1S514	5.9	5.95	5.99

8.4.3 OTG Mode

The TPD1S514 Family of devices UVLO and OVP voltages are referenced to V_{BUS_CON} voltage. In OTG mode, V_{BUS_SYS} is driving the V_{BUS_CON}. Under this situation, initially V_{BUS_CON} is powered through the body diode of the nFET by V_{BUS_SYS}. Once the UVLO threshold on V_{BUS_CON} is met, the nFET turns ON. If there is a short to ground on V_{BUS_CON} the OTG supply is expected to limit the current.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPD1S514 Family of devices offer V_{BUS} port protection implementing UVLO and OVP, with an LDO supplied V_{BUS_POWER} pin to regulate an output supply pin of 3 mA at 5 V (except for TPD1S514, which follows V_{BUS_CON} up to 6.48 V, after which it is regulated to that voltage). The V_{BUS_POWER} pin can be used to power the system from an external source on V_{BUS_CON} in case the system's battery state cannot power the system.

9.2 Typical Applications

9.2.1 TPD1S514-1 USB 2.0/3.0 Case 1: Always Enabled

The $\overline{EN}$ pin can be tied to ground so that the nFET is ON when $V_{UVLO} < V_{BUS\_CON} < V_{OVP}$ and an external charger can power V_{BUS}. V_{BUS_POWER} should be tied to ground with a 1-µF capacitor for LDO stability. USB Inrush Current compliance tests will need to be handled by the rest of the system since the start delays t_{DELAY} and t_{SS} implement only after the device changes from disabled to enabled, or after any UVLO or OVP event.

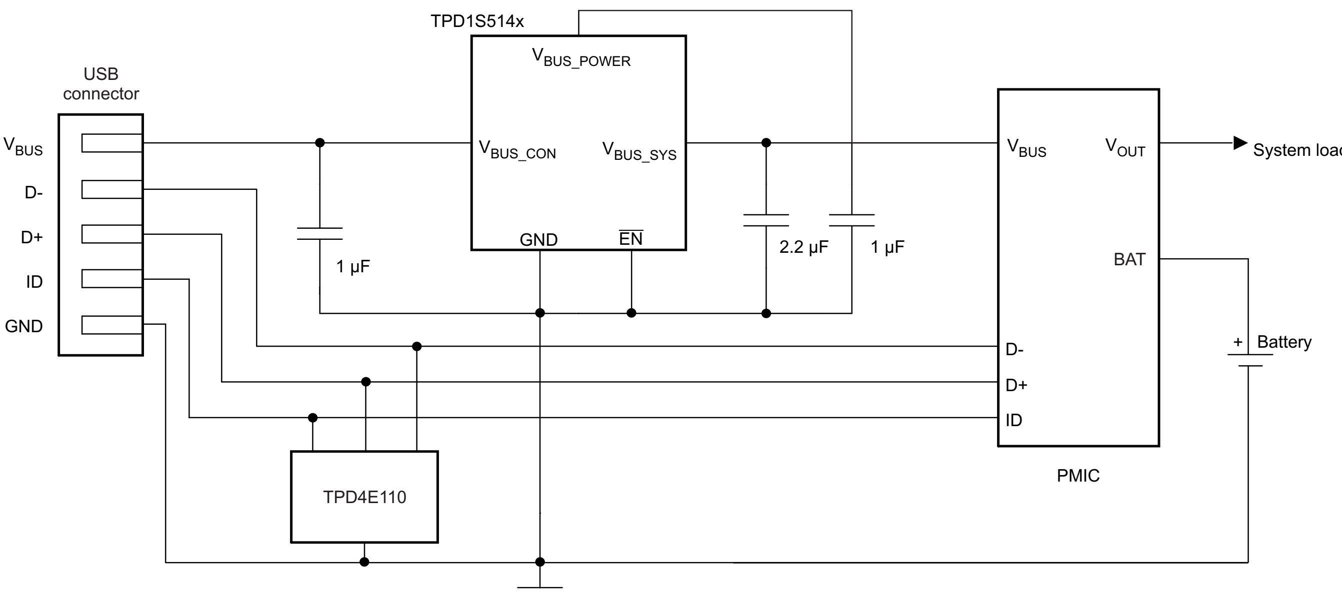


Figure 10. Always on, TPD1S514-1

9.2.1.1 Design Requirements

For this example, use the following input parameters from Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Signal range on V_{BUS_CON}	3.5 V – 5.9 V
Signal range on V_{BUS_SYS}	3.9 V – 5.9 V
Signal on $\overline{EN}$	Tie to system ground plane

9.2.1.2 Detailed Design Procedure

To begin the design process the designer needs to know the V_{BUS} voltage range.

9.2.1.2.1 V_{BUS} Voltage Range

The UVLO trip-point is a maximum 3.5 V and the OVP trip-point is a minimum 5.9 V. This provides some headroom for the USB 2.0 specified minimum 4.4 V (Low-power) or 4.75 V (Full-power) and 5.25 V maximum; or the USB 3.0 specified minimum 4.45 V and 5.25 V maximum.

9.2.1.2.2 Discharged Battery

Connecting $\overline{EN}$ to ground sets the part active at all times. OVP and UVLO are always active, even when the system battery is fully discharged. In the case of a discharged system battery, V_{BUS_SYS} can be used to power the system when a source with voltage between V_{UVLO} and V_{OVP} is attached to V_{BUS_CON}.

9.2.1.3 Application Curves

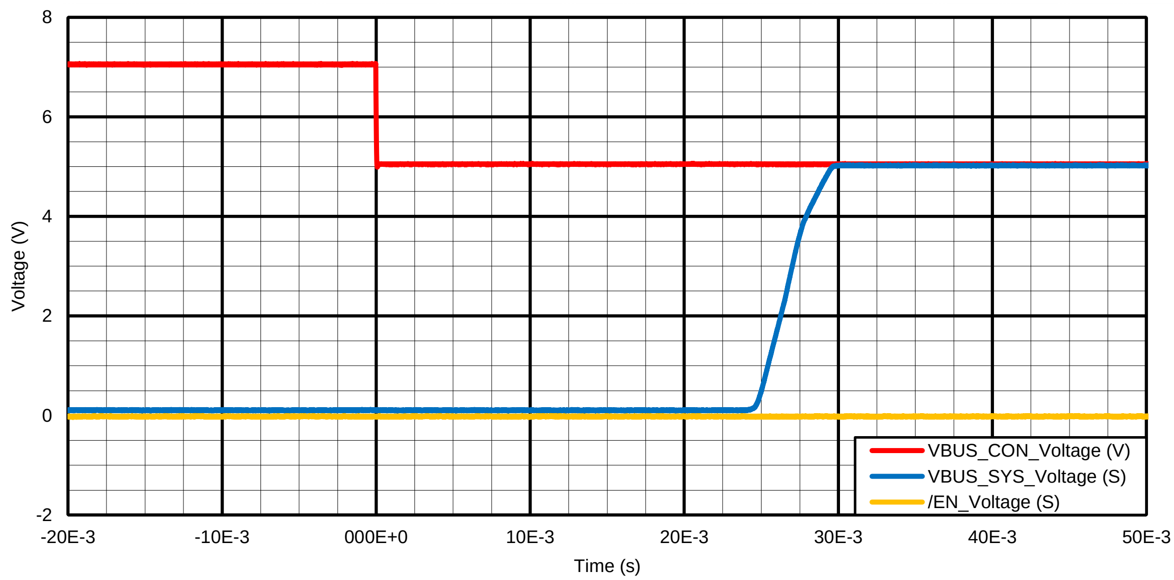


Figure 11. V_{BUS_SYS} Recovery Time From Over Voltage on V_{BUS_CON}

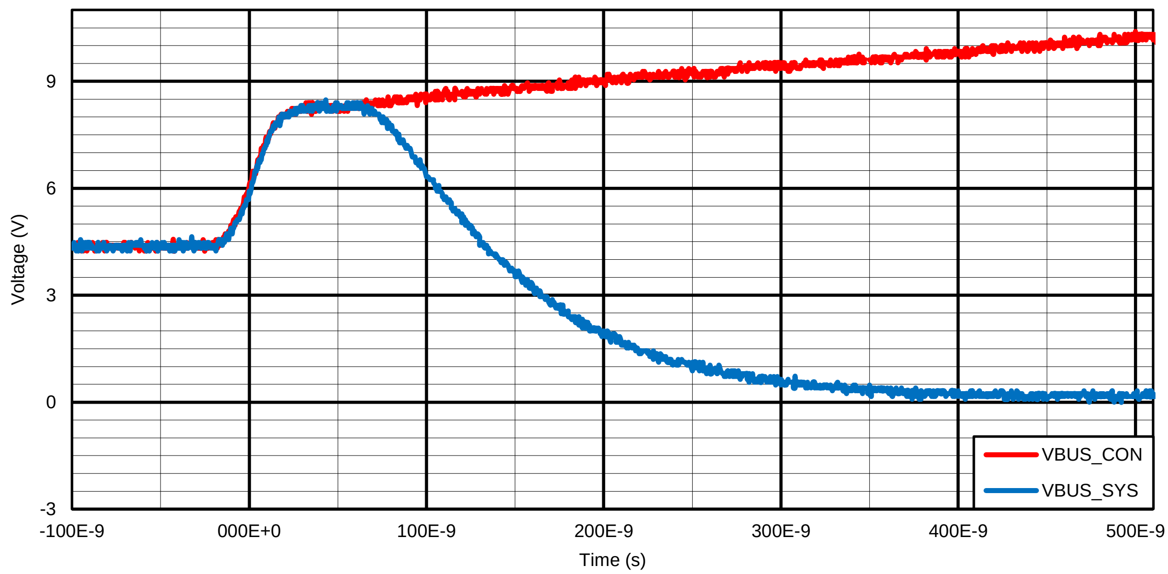


Figure 12. OVP Response

9.2.2 TPD1S514-1 USB 2.0/3.0 Case 2: PMIC Controlled $\overline{EN}$

The TPD1S514 Family offers more flexibility to system designers to power up the system during a dead battery condition. Refer to Figure 13, the V_{BUS_POWER} pin supplies 4.95 V and 3 mA to power the PMIC in a dead battery condition. Regardless of $\overline{EN}$ state, V_{BUS_POWER} is available to the PMIC. Utilizing this power, the PMIC can enable the TPD1S514 Family of devices when a valid V_{BUS_CON} voltage is present.

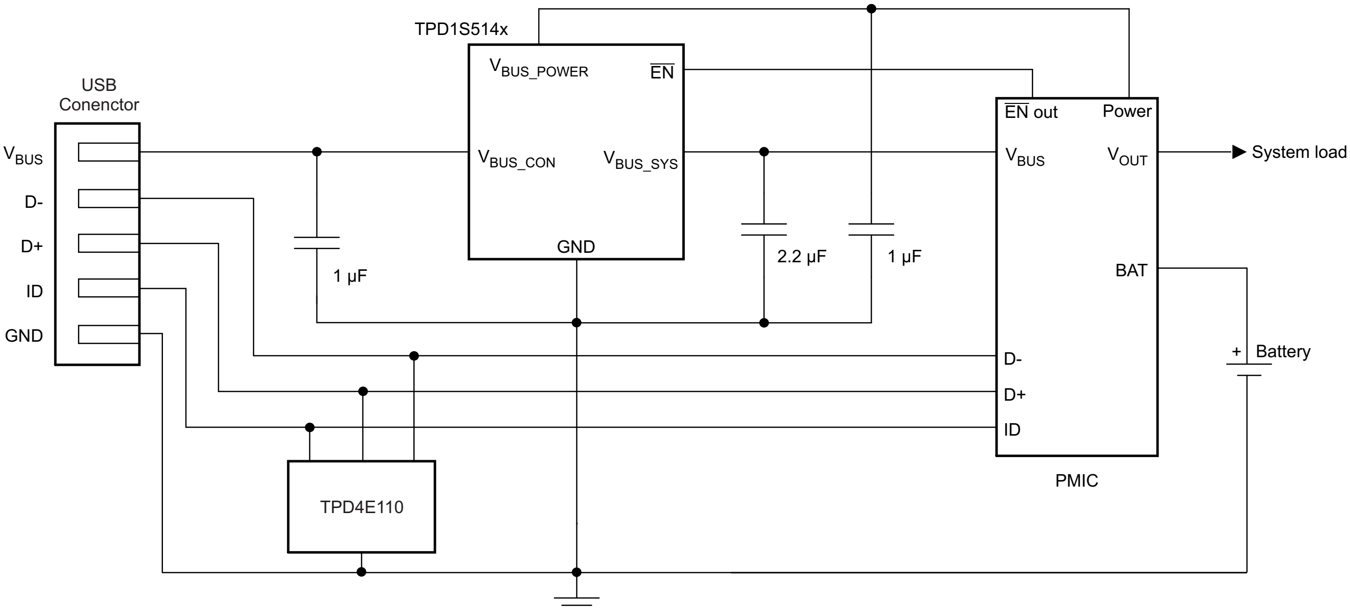


Figure 13. PMIC Controlled $\overline{EN}$, TPD1S514-1

9.2.2.1 Design Requirements

For this example, use the following table as input parameters:

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Signal range on V_{BUS_CON}	3.5 V – 5.9 V
Signal range on V_{BUS_SYS}	3.9 V – 5.9 V
Drive $\overline{EN}$ low (enabled)	0 V – 0.8 V
Drive $\overline{EN}$ high (disabled)	1.2 V – 6.0 V

9.2.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon. The designer needs to know the following:

- V_{BUS} voltage range
- PMIC power requirement

9.2.2.2.1 V_{BUS} Voltage Range

The UVLO trip-point is a maximum 3.5 V and the OVP trip-point is a minimum 5.9 V. This provides some headroom for the USB 2.0 specified minimum 4.4 V (Low-power) or 4.75 V (Full-power) and 5.25 V maximum; or the USB 3.0 specified minimum 4.45 V and 5.25 V maximum.

9.2.2.2.2 PMIC Power Requirement

The V_{BUS_POWER} pin can source up to 3 mA of current and maintain a minimum 4.8 V, 4.95 V typical. TPD1S514-1 design provides an LDO regulator supplied voltage source which can be used to provide power to a PMIC when its internal battery supplied power is unavailable. When selecting a matching PMIC, ensure its power requirement can be met by the V_{BUS_POWER} pin if designing for this scenario.

9.2.2.2.3 Discharged Battery

Powering the PMIC from V_{BUS_POWER} allows logic control of the $\overline{EN}$ pin to set TPD1S514-1 active and begin charging the battery and powering up the rest of the system.

9.2.2.3 Application Curve

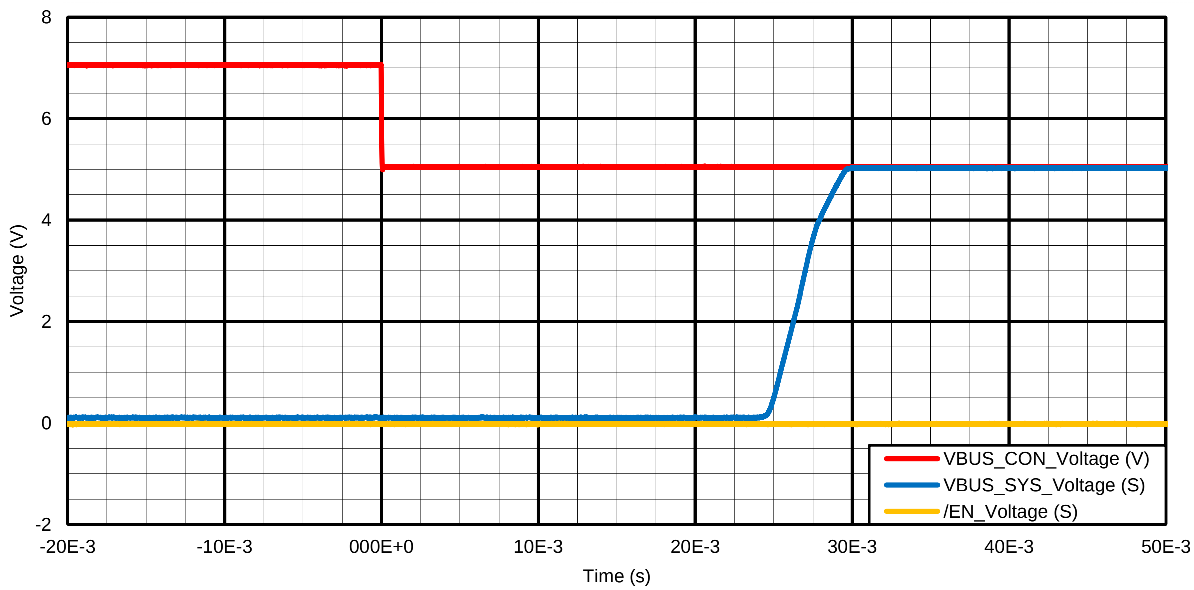


Figure 14. V_{BUS_SYS} Recovery Time From Over Voltage on V_{BUS_CON}

10 Power Supply Recommendations

The TPD1S514 Family is designed to receive power from a USB 3.0 (or lower) V_{BUS} source. It can operate normally (nFET ON) between a minimum 3.5 V and a maximum V_{OVP_MIN} V. Thus, the power supply (with a ripple of V_{RIPPLE}) requirement for the TPD1S514 Family of devices to be able to switch the nFET ON is between 3.5 V + V_{RIPPLE} and V_{OVP_MIN} – V_{RIPPLE}, where V_{OVP_MIN} is:

Table 4. V_{OP_MIN} Values

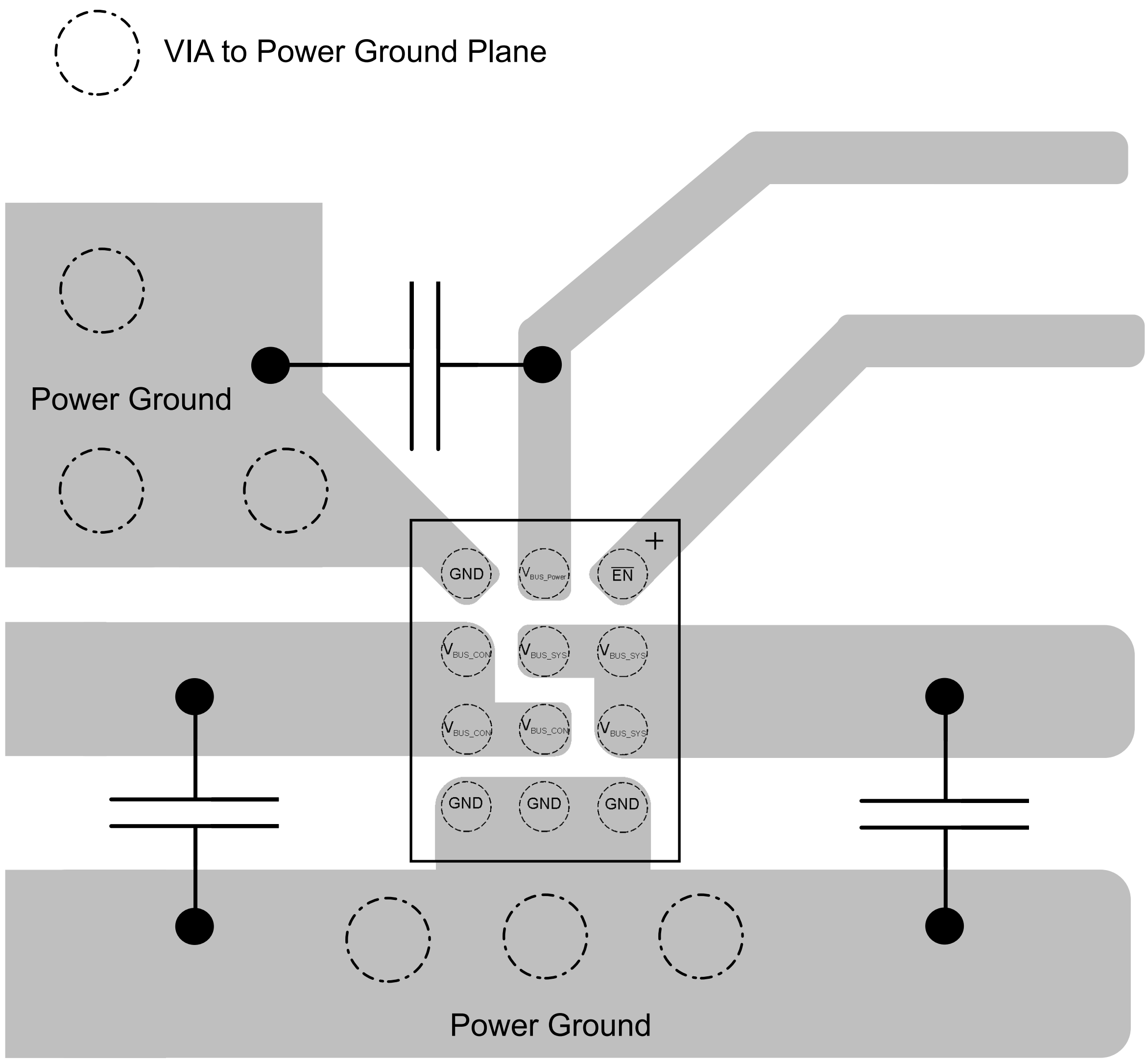
DEVICE NAME	V_{OVP_MIN}
TPD1S514-1	5.90 V
TPD1S514-2	9.9 V
TPD1S514-3	13.5 V
TPD1S514	5.90 V

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example



When designing layout for the TPD1S514 Family, note that V_{BUS_CON} and V_{BUS_SYS} pins allow extra wide traces for good power delivery. In the example shown, these pins are routed with 50 mil (1.27 mm) wide traces. Place the V_{BUS_CON}, V_{BUS_SYS}, and V_{BUS_POWER} capacitors as close to the pins as possible. Use external and internal ground planes and stitch them together with VIAs as close to the GND pins of TPD1S514 as possible. This allows for a low impedance path to ground so that the device can properly dissipate any surge or ESD events.

Figure 15. Layout Recommendation

12 デバイスおよびドキュメントのサポート

12.1 コミュニティ・リソース

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD1S514-1YZR	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH5141
TPD1S514-1YZR.A	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH5141
TPD1S514-2YZR	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH5142
TPD1S514-2YZR.A	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH5142
TPD1S514-3YZR	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH5143
TPD1S514-3YZR.A	Active	Production	DSBGA (YZ) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH5143

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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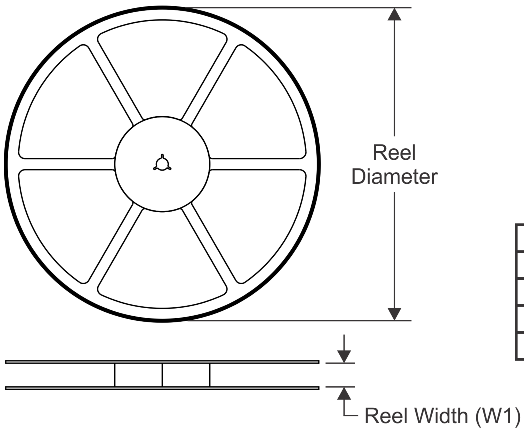
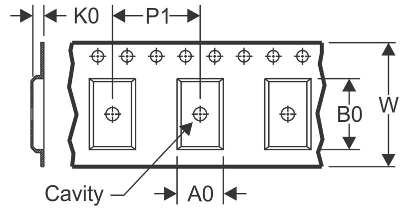
TAPE AND REEL INFORMATION

REEL DIMENSIONS

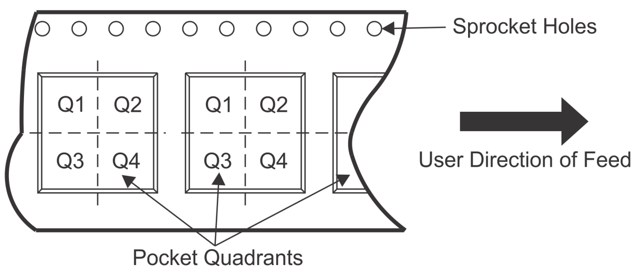


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

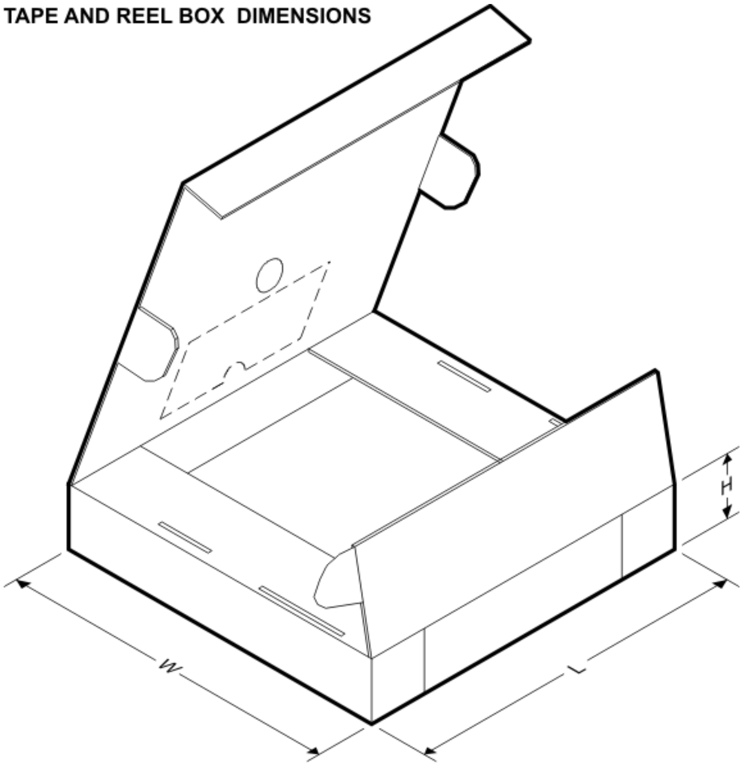
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1S514-1YZR	DSBGA	YZ	12	3000	180.0	8.4	1.39	2.09	0.75	4.0	8.0	Q2
TPD1S514-2YZR	DSBGA	YZ	12	3000	180.0	8.4	1.39	2.09	0.75	4.0	8.0	Q2
TPD1S514-3YZR	DSBGA	YZ	12	3000	180.0	8.4	1.39	2.09	0.75	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1S514-1YZR	DSBGA	YZ	12	3000	182.0	182.0	20.0
TPD1S514-2YZR	DSBGA	YZ	12	3000	182.0	182.0	20.0
TPD1S514-3YZR	DSBGA	YZ	12	3000	182.0	182.0	20.0

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