TPS1HC100-Q1、100mΩ、2.5A、シングル チャネル、車載スマート ハイサイド スイッチ

1 特長

- 12V 車載システム向け、包括的な診断機能搭載、シングルチャネル スマート ハイサイド パワー スイッチ
  - オープンドレイン ステータス出力
  - 電流センス アナログ出力
- 広い動作電圧範囲:3V～28V
- 低いスタンバイ電流:85℃ で 0.5µA 未満
- 動作時の接合部温度:–40℃ ～ 150℃
- 1.8V、3.3V、5V のロジック互換
- フォルト検出電圧スケーリングによる ADC 保護
- プログラム可能な電流制限:1.9A のとき ±18% の精度
- 高精度の電流センス:1A で ±6%
- 保護
  - 過負荷および短絡保護
  - 誘導性負荷の負電圧クランプ
  - 低電圧誤動作防止 (UVLO) 保護
  - 自己回復可能なサーマル シャットダウンおよびスイング
  - GND および電源喪失時の保護
  - 外付け部品を使ったバッテリ逆極性保護
- 診断機能
  - オンおよびオフ状態における出力の開放負荷とバッテリ短絡の検出
  - 過負荷およびグランド短絡検出
  - サーマル シャットダウンおよびスイング検出
- 認定
  - AEC-Q100 車載グレード 1 温度認定済み
  - 機能安全対応
    - 機能安全システムの設計に役立つ資料を利用可能
  - AECQ100-12 グレード A に従ってテスト済み、100 万回の GND 短絡テスト
  - 電気過渡的外乱への耐性に関する ISO7637-2 および ISO16750-2 認証
- 熱特性強化型 14 ピン PWP パッケージ

2 アプリケーション

- 車載ディスプレイ モジュール
- ADAS モジュール
- コンフォート シート モジュール
- HVAC (エアコン) 制御モジュール
- ボディ コントロール モジュール

3 概要

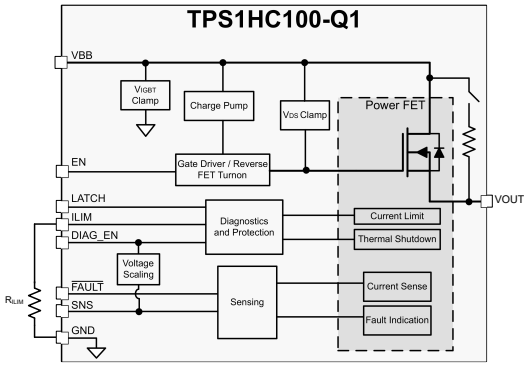
TPS1HC100-Q1 デバイスは、各種の保護機能を搭載したハイサイド パワー スイッチで、NMOS パワー FET とチャージ ポンプを内蔵して、各種負荷をインテリジェントに制御することを目標にしています。高精度の電流センスとプログラマブル電流制限機能により、市場で差別化できます。

低ロジック高スレッショルド、V_{IH}、1.5V の入力ピンにより、マイコンの GPIO 信号を 1.8V で使用できます。高精度の電流検出により、キャリブレーションを追加することなく、さらに優れたリアルタイム監視効果と高精度の診断機能を得ることができます。外部の高精度電流制限機能により、アプリケーションごとに電流制限値を設定できます。本デバイスは、スタートアップまたは短絡状態時に突入電流を効果的にクランプすることで、システムの信頼性を大きく向上させます。TPS1HC100-Q1 デバイスは、ワット数の低い電球、LED、リレー、ソレノイド、ヒーターなど、幅広い種類の抵抗性、誘導性、容量性負荷のためのハイサイド パワー スイッチとして使用できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS1HC100-Q1	PWP (HTSSOP、14)	5mm × 6.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

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4 Pin Configuration and Functions

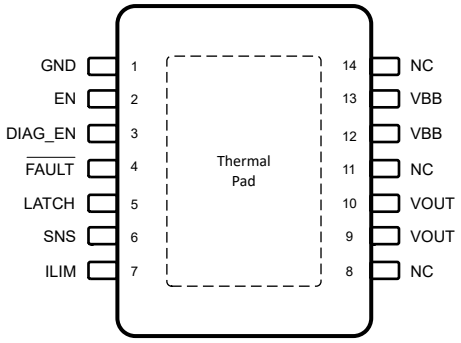


図 4-1. PWP Package 14-Pin HTSSOP Top View

表 4-1. Pin Functions

over operating free-air temperature range (unless otherwise noted)

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND	Power	Ground of device. Connect to resistor-diode ground network to have reverse battery protection.
2	EN	I	Input control for channel activation
3	DIAG_EN	I	Enable-disable pin for diagnostics, internal pulldown
4	$\overline{\text{FAULT}}$	O	Open drain global fault output. Referred to $\overline{\text{FAULT}}$, $\overline{\text{FLT}}$, or fault pin.
5	LATCH	I	Thermal shutdown behavior, latch off or auto retry, internal pull down
6	SNS	O	Output corresponding sense value based on sense ratio
7	ILIM	O	Adjustable current limit. Short to ground or leave floating if external current limit is not used.
8, 11, 14	NC	N/A	No internal connection
9, 10	VOUT	Power	Output of high side switch, connected to load
12, 13	VBB	Power	Power supply
Thermal Pad	Pad	—	Thermal Pad, internally shorted to ground

4.1 Recommended Connections for Unused Pins

The TPS1HC100-Q1 is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins can be considered as optional.

表 4-2. Connections For Optional Pins

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SNS	Ground through 1-kΩ resistor	Analog sense is not available.
LATCH	Float or ground through R_{PROT} resistor	With LATCH unused, the device auto-retries after a fault. If latched behavior is desired, but the system describes limited I/O, it is possible to use one microcontroller output to control the latch function of several high-side channels.
ILIM	Float	If the ILIM pin is left floating, the device is set to the default internal current-limit threshold.
DIA_EN	Float or ground through R_{PROT} resistor	With DIA_EN unused, the analog sense, open-load, and short-to-battery diagnostics are not available.
$\overline{FAULT}$	Float	Open drain $\overline{FAULT}$ signal is not able to be used

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, V_{BB}			28	V
Load dump voltage, V_{LD}	ISO16750-2:2010(E)		36	V
Reverse Polarity Voltage	Maximum duration 3 minutes	–18		V
Enable pin current, I_{EN}		–1	20	mA
Enable pin voltage, V_{EN}		–1	7	V
Diagnostic Enable pin current, I_{DIA_EN}		–1	20	mA
Diagnostic Enable pin voltage, V_{DIA_EN}		–1	7	V
Sense pin current, I_{SNS}		–100	10	mA
Sense pin voltage, V_{SNS}		–1	5.5	V
Latch pin current, I_{LATCH}		–1	10	mA
Latch pin voltage, V_{LATCH}		–1	7	V
FLT pin current, I_{FLT}		–30	10	mA
FLT pin voltage, V_{FLT}		–0.3	7	V
Reverse ground current, I_{GND}	V_{BB} < 0 V		–50	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002 Classification Level H2(2)	All pins except VS and VOUT	±2000	V
		Human-body model (HBM), per AEC Q100-002 Classification Level H3A(2)	VS and VOUT	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) All ESD strikes are with reference from the pin mentioned to GND
(2) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{VBB_NOM}	Nominal supply voltage (1)	3.5	18	V
V_{VBB_EXT}	Extended supply voltage(2)	2.6	28	V
V_{VBB_SC}	Short circuit supply voltage capability		28	V
V_{EN}	Enable voltage	–1	5.5	V
V_{DIA_EN}	Diagnostic Enable voltage	–1	5.5	V
V_{LATCH}	Latch voltage	–1	5.5	V
V_{SNS}	Sense voltage	–1	7	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND

(2) Device will function within extended operating range, however some timing parametric values might not apply. See the respective sections for what voltages are used. Additionally more explanation can be found in Power Supply Recommendations

5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS1HC100-Q1 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

5.5 Electrical Characteristics

V_{BB} = 6 V to 28 V, T_A = -40°C to 125°C (unless otherwise noted); Typical application is 13.5V, 10Ω, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{Clamp}	VDS clamp voltage		T_J=25°C	35		43	V
			T_J = -40°C to 150°C	33		45	V
V_{UVLOR}	V_{BB} undervoltage lockout rising	Measured with respect to the GND pin of the device		3.0	3.5	4.0	V
V_{UVLOF}	V_{BB} undervoltage lockout falling			2.4	2.6	3.0	V
I_{SB}	Standby current (total device leakage including MOSFET channel)	V_{BB} ≤ 28 V, V_{EN} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V	T_J = 25°C			0.3	µA
			T_J = 85°C			0.5	µA
I_{NOM}	Continuous load current, per channel	Channel enabled, T_{AMB} = 85°C			2		A
$I_{OUT(standby)}$	Output leakage current	V_{BB} ≤ 28 V, T_J = 25°C V_{EN} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V			0.01	0.1	µA
		V_{BB} ≤ 28 V, T_J = 85°C V_{EN} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V				0.3	µA
I_{DIA}	Current consumption in diagnostic mode	V_{BB} ≤ 28 V, I_{SNS} = 0 mA V_{EN} = 0 V, V_{DIA_EN} = 5 V, V_{OUT} = 0V			1.3	1.5	mA
I_Q	Quiescent current channel enabled	V_{BB} ≤ 28 V V_{EN} = V_{DIA_EN} = 5 V, I_{OUTx} = 0 A			1.6	2.5	mA
t_{STBY}	Standby mode delay time	V_{ENx} = V_{DIA_EN} = 0 V to standby			20		ms
RON CHARACTERISTICS							
R_{ON}	On-resistance (Includes MOSFET channel and metallization on die)	6 V ≤ V_{BB} ≤ 28 V, I_{OUT}= 1 A	T_J = 25°C		88		mΩ
			T_J = 150°C			176	mΩ
		3V ≤ V_{BB} ≤ 6V, I_{OUT} =1A	T_J = 25°C			190	mΩ
			T_J = 150°C			250	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	-18 V ≤ V_{BB} ≤ -6 V	T_J = 25°C		94		mΩ
			T_J = 150°C			188	mΩ
CURRENT SENSE CHARACTERISTICS							

5.5 Electrical Characteristics (続き)

V_{BB} = 6 V to 28 V, T_A = -40°C to 125°C (unless otherwise noted); Typical application is 13.5V, 10Ω, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}	I_{OUT} = 1 A			1040		
I_{SAT_SNS}	Saturated sense current level	Maximum amount of load current that can be sensed			6		A
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V, VBB ≥ 6 V	I_{OUT} = 4 A		3.87		mA
				–6		6	%
		V_{EN} = V_{DIA_EN} = 5 V, VBB ≥ 5 V	I_{OUT} = 2 A		1.93		mA
				–6		6	%
			I_{OUT} = 1 A		0.96		mA
				–6		6	%
			I_{OUT} = 500 mA		0.48		mA
				–6		6	%
			I_{OUT} = 200 mA		0.192		mA
				–6		6	%
			I_{OUT} = 100 mA		0.096		mA
				–6		6	%
			I_{OUT} = 50 mA		0.048		mA
				–7		7	%
			I_{OUT} = 20 mA		0.0192		mA
				–15		15	%
			I_{OUT} = 10 mA		0.0096		mA
				–40		40	%
			I_{OUT} = 5 mA		0.0048		mA
				–70		70	%
SNS CHARACTERISTICS							
V_{SNSFH}	V_{SNS} fault high-level	V_{DIA_EN} = 5 V		4.75	5	5.5	V
		V_{DIA_EN} = 3.3 V		3.3	3.5	3.75	V
V_{SNSFH}	V_{SNS} fault high-level	V_{DIA_EN} = V_{IH}		2.8	3.15	3.5	V
I_{SNSFH}	I_{SNS} fault high-level	V_{DIA_EN} > $V_{IH,DIAG\_EN}$			6.6		mA
$I_{SNSleak}$	I_{SNS} leakage	V_{DIA_EN} = 5 V, IL = 0 mA	T_A = 25℃			1.8	µA
			T_A = 125℃			2.2	µA
V_{BB_ISNS}	V_{BB} headroom needed for full current sense and fault functionality	V_{DIAG_EN} = 3.3V		5.3			V
V_{BB_ISNS}	V_{BB} headroom needed for full current sense and fault functionality	V_{DIAG_EN} = 5V		6.5			V
CURRENT LIMIT CHARACTERISTICS							
I_{CL_LINPK}	Linear Mode peak	T_J = -40°C to 150°C dI/dt < 0.01 A/ms	I_{ILIM} = 0.7A to 7A	0.9 × I_{CL}		1.4 × I_{CL}	A
I_{CL_ENPS}	Peak current enabling into permanent short	T_J = -40°C to 150°C	R_{ILIM} = 7.15K to 71.5K			2 × I_{CL}	A
I_{OVCR}	OVCR Peak current threshold when short is applied while switch enabled	T_J = -40°C to 150°C	R_{ILIM} > 35kΩ			6.5	A
			15kΩ ≤ R_{ILIM} ≤ 35kΩ			9.5	A
			R_{ILIM} < 15kΩ			16	A

5.5 Electrical Characteristics (続き)

V_{BB} = 6 V to 28 V, T_A = -40°C to 125°C (unless otherwise noted); Typical application is 13.5V, 10Ω, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CL}	I_{CL} Current Limit Threshold	T_J = -40°C to 150°C	R_{ILIM} = GND	5	7	9	A
			R_{ILIM} = open, or out of range		3		A
K_{CL}	Current Limit Ratio	T_J = -40°C to 150°C	R_{ILIM} = 7.15 kΩ	36.34	44.3	55.41	A * kΩ
			R_{ILIM} = 25 kΩ	45	48.5	57.25	A * kΩ
			R_{ILIM} = 71.5 kΩ	36.75	49	61.26	A * kΩ
FAULT CHARACTERISTICS							
R_{VOL}	Open-load (OL) detection internal pull-up resistor	V_{EN} = 0 V, V_{DIA_EN} = 5 V			150		kΩ
t_{OL}	Open-load (OL) detection deglitch time	V_{EN} = 0 V, V_{DIA_EN} = 5 V, When $V_{BB} - V_{OUT} < V_{OL}$, duration longer than t_{OL}. Openload detected.			350	1000	µs
V_{OL}	Open-load (OL) detection voltage	V_{EN} = 0 V, V_{DIA_EN} = 5 V			2	2.5	V
V_{FLT}	$\overline{FLT}$ low output voltage	$I_{\overline{FLT}}$ = 2.5 mA				0.5	V
t_{OL1}	OL and STB indication-time from EN falling	V_{EN} = 5 V to 0 V, V_{DIA_EN} = 5 V I_{OUT} = 0 mA, V_{OUT} = V_{BB} - V_{OL}			350	1000	µs
t_{OL2}	OL and STB indication-time from DIA_EN rising	V_{EN} = 0 V, V_{DIA_EN} = 0 V to 5 V I_{OUT} = 0 mA, V_{OUT} = V_{BB} - V_{OL}				1000	µs
T_{ABS}	Thermal shutdown				165		°C
T_{REL}	Relative thermal shutdown				60		°C
T_{HYS}	Thermal shutdown hysteresis				25		°C
t_{FAULT_FLT}	Fault indication-time	V_{DIA_EN} = 5 V Time between fault and $\overline{FLT}$ asserting				60	µs
t_{FAULT_SNS}	Fault indication-time	V_{DIA_EN} = 5 V Time between fault and I_{SNS} settling at V_{SNSFH}				60	µs
t_{RETRY}	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown).		1	2	3	ms
EN PIN CHARACTERISTICS							
$V_{IL, EN}$	Input voltage low-level	No GND Network				0.8	V
$V_{IH, EN}$	Input voltage high-level	No GND Network		1.5			V
$V_{IHYS, EN}$	Input voltage hysteresis				280		mV
R_{EN}	Internal pulldown resistor			200	350	500	kΩ
$I_{IL, EN}$	Input current low-level	V_{EN} = 0.8 V			2.2		µA
$I_{IH, EN}$	Input current high-level	V_{EN} = 5 V			14		µA
DIA_EN PIN CHARACTERISTICS							
V_{IL, DIA_EN}	Input voltage low-level	No GND Network				0.8	V
V_{IH, DIA_EN}	Input voltage high-level	No GND Network		1.5			V
V_{IHYS, DIA_EN}	Input voltage hysteresis				280		mV
R_{DIA_EN}	Internal pulldown resistor			100	250	450	kΩ
I_{IL, DIA_EN}	Input current low-level	V_{DIA_EN} = 0.8 V			3.2		µA
I_{IH, DIA_EN}	Input current high-level	V_{DIA_EN} = 5 V			20		µA
LATCH PIN Characteristics							
$V_{IL, LATCH}$	Input voltage low-level	No GND Network				0.8	V

5.5 Electrical Characteristics (続き)

V_{BB} = 6 V to 28 V, T_A = -40°C to 125°C (unless otherwise noted); Typical application is 13.5V, 10Ω, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH, LATCH}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, LATCH}$	Input voltage hysteresis			280		mV
R_{LATCH}	Internal pulldown resistor		0.5	1	1.5	MΩ
$I_{IL, LATCH}$	Input current low-level	V_{DIA_EN} = 0.8 V		2.2		µA
$I_{IH, LATCH}$	Input current high-level	V_{DIA_EN} = 5 V		5		µA

5.6 SNS Timing Characteristics

V_{BB} = 6 V to 18 V, T_J = -40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIA_EN 50% of V_{DIA_EN} to 90% of settled ISNS	V_{ENx}= 5 V, V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ, I_L = 1A			30	µs
$t_{SNSION1}$	Settling time from rising edge of DIA_EN 50% of V_{DIA_EN} to 90% of settled ISNS	V_{EN} = 5 V, V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ, I_L = 30 mA			30	µs
$t_{SNSION2}$	Settling time from rising edge of EN and DIA_EN 50% of V_{DIA_EN} V_{EN} to 90% of settled ISNS	V_{EN} = V_{DIA_EN} = 0 V to 5 V VBB = 13.5V R_{SNS} = 1 kΩ, R_{LOAD} = 10Ω			150	µs
$t_{SNSION3}$	Settling time from rising edge of EN with DIA_EN HI; 50% of V_{DIA_EN} V_{EN} to 90% of settled ISNS	V_{EN} = 0 V to 5 V, V_{DIA_EN} = 5 V VBB = 13.5V R_{SNS} = 1 kΩ, R_{LOAD} = 10Ω			150	µs
$t_{SNSIOFF}$	Settling time from falling edge of DIA_EN	V_{EN} = 5 V, V_{DIA_EN} = 5 V to 0 V VBB = 13.5V R_{SNS} = 1 kΩ, R_L = 10 Ω			20	µs
$t_{SETTLEH}$	Settling time from rising edge of load step	V_{EN} = 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, I_{OUT} = 0.5 A to 3 A			20	µs
$t_{SETTLEL}$	Settling time from falling edge of load step	V_{EN} = 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, I_{OUT} = 3 A to 0.5 A			20	µs

5.7 Switching Characteristics

V_{BB} = 13.5 V, T_J = -40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Channel Turnon delay time (from Standby)	V_{BB} = 13.5 V, R_L = 10 Ω 50% of EN to 10% of VOUT	10	40	55	µs
t_{DR}	Channel Turnon delay time (from Active)	V_{BB} = 13.5 V, R_L = 10Ω 50% of EN to 10% of VOUT	10	30	45	µs
t_{DF}	Channel Turnoff delay time	V_{BB} = 13.5 V, R_L = 10 Ω 50% of EN to 90% of VOUT	10	30	45	µs
SR_R	VOUT rising slew rate	V_{BB} = 13.5 V, 20% to 80% of V_{OUT}, R_L = 10 Ω	0.1	0.25	0.5	V/µs
SR_F	VOUT falling slew rate	V_{BB} = 13.5 V, 80% to 20% of V_{OUT}, R_L = 10 Ω	0.1	0.25	0.5	V/µs
f_{max}	Maximum PWM frequency(1)			0.4	2	kHz
t_{ON}	Channel Turnon time	V_{BB} = 13.5 V, R_L = 10 Ω 50% of EN to 80% of VOUT	30	70	145	µs
t_{OFF}	Channel Turnoff time	V_{BB} = 13.5 V, R_L = 10Ω 50% of EN to 20% of VOUT	39	70	145	µs

5.7 Switching Characteristics (続き)

V_{BB} = 13.5 V, T_J = -40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON} - t_{OFF}	Turnon and off matching	1ms enable pulse V_{BB} = 13.5 V, R_L = 10 Ω	–30		30	µs
		200-µs enable pulse, V_{BB} = 13.5 V, R_L = 10 Ω,	–30		30	µs
Δ_{PWM}	PWM accuracy - average load current	200-µs enable pulse (1ms period), V_{BB} = 13.5 V, R_L = 10 Ω	–25		25	%
		≤500Hz, 50% Duty cycle V_{BB} = 13.5 V, R_L = 10 Ω	–10		10	%
E_{ON}	Switching energy losses during turnon	V_{BB} = 13.5 V, R_L = 10 Ω		0.5		mJ
E_{OFF}	Switching energy losses during turnoff	V_{BB} = 13.5 V, R_L = 10 Ω		0.5		mJ

5.8 Typical Characteristics

All the following data are based on the mean value of the three lots samples, V_{VBB} = 13.5 V if not specified.

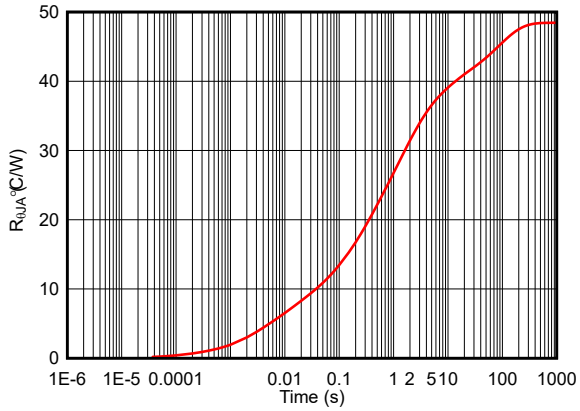
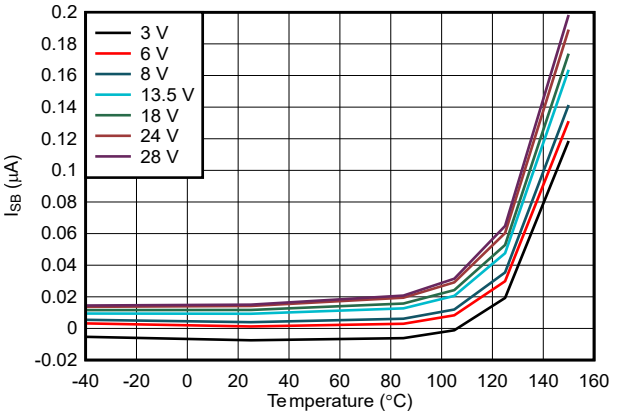
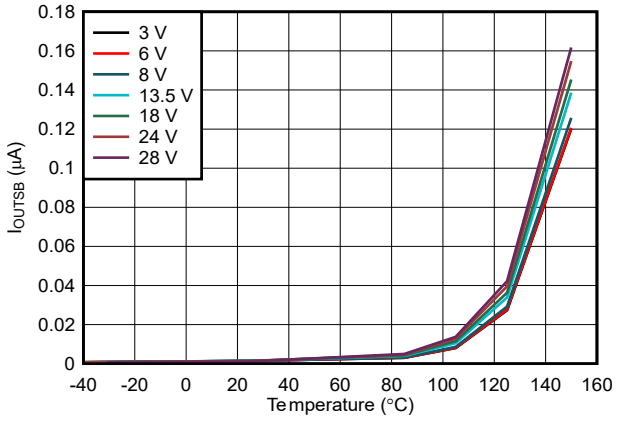


図 5-1. Transient Thermal Impedance



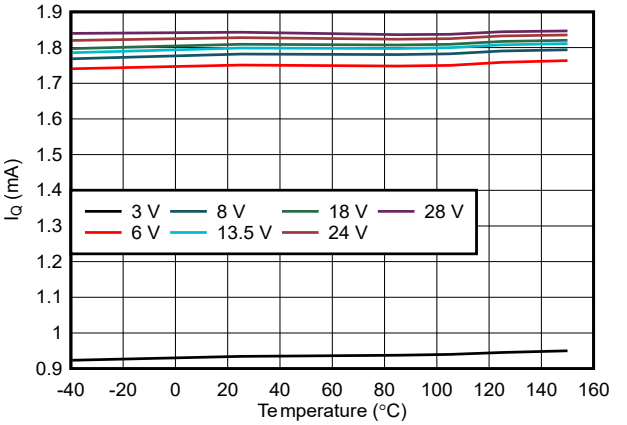
V_{OUT} = 0 V V_{EN} = 0 V V_{DIAG_EN} = 0 V
V_{BB} Varied

図 5-2. Standby Current I_{SB} vs. Temperature



V_{OUT} = 0 V V_{EN} = 0 V V_{DIAG_EN} = 0 V
V_{BB} Varied

図 5-3. Output Leakage Current $I_{OUT,STBY}$ vs Temperature

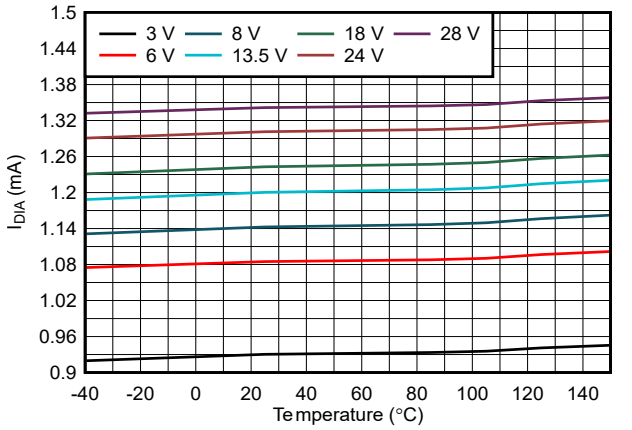


I_{OUT} = 0 A V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} Varied

図 5-4. Quiescent Current I_Q vs Temperature

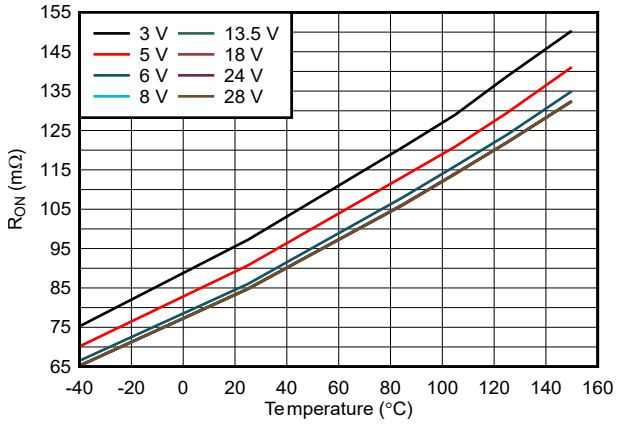
5.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VBB} = 13.5 V if not specified.



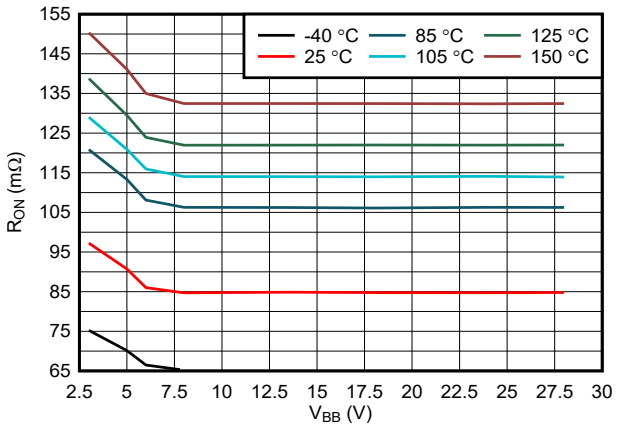
I_{OUT} = 0 A V_{EN} = 0 V V_{DIAG_EN} = 5 V
V_{BB} Varied

図 5-5. Diagnostic Current I_{DIA} vs Temperature



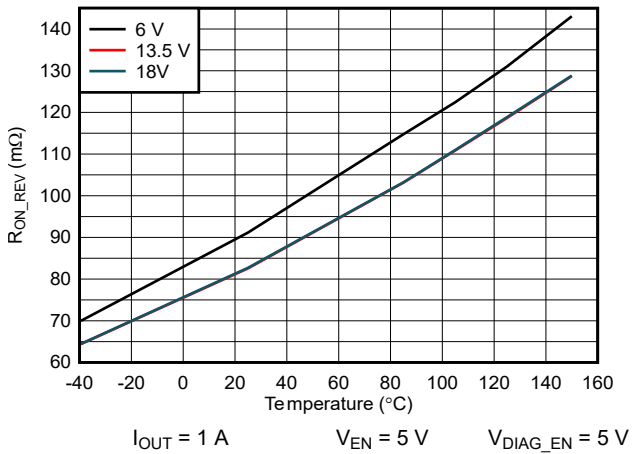
I_{OUT} = 1 A V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} Varied

図 5-6. R_{DSON} vs Temperature



I_{OUT} = 1 A V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} Varied

図 5-7. R_{DSON} vs V_{BB}

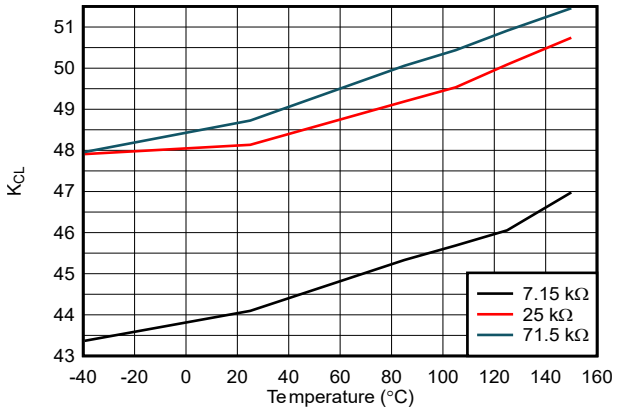


I_{OUT} = 1 A V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} Varied

図 5-8. R_{ONREV} vs Temperature

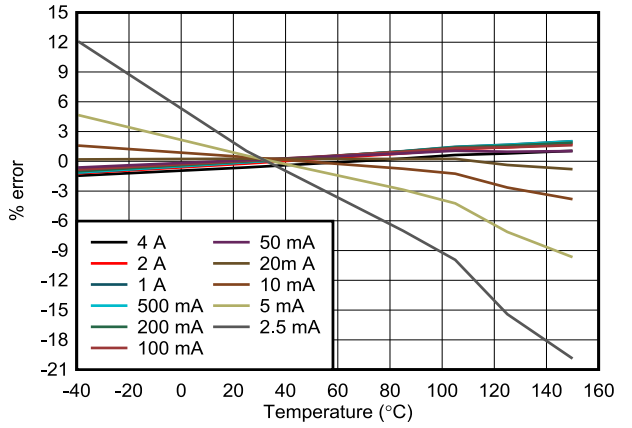
5.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VBB} = 13.5 V if not specified.



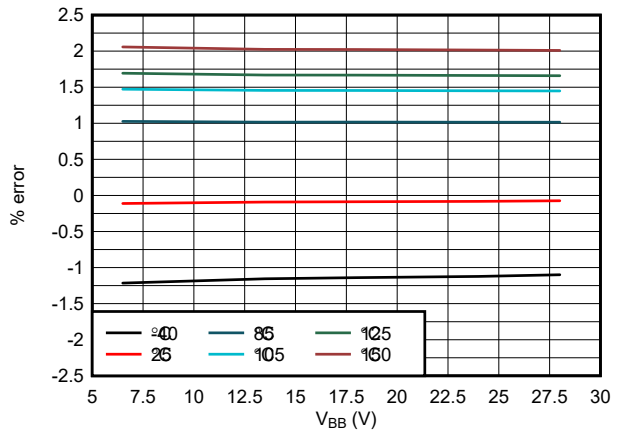
R_{OUT} = 5µH and 100 mΩ V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} = 13.5 V

図 5-9. K_{CL} vs Temperature



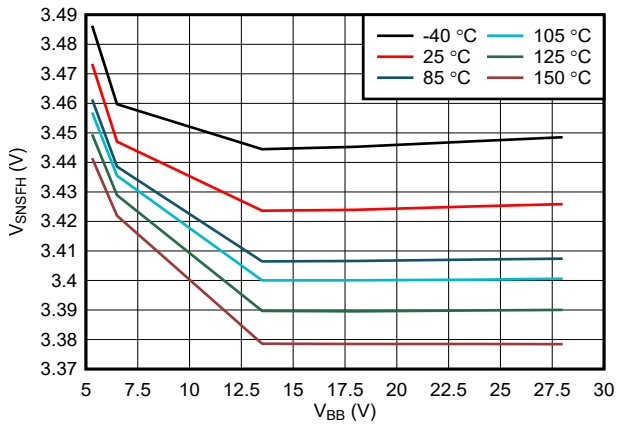
R_{OUT} varied V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} = 13.5 V R_{SNS} = 1 kΩ

図 5-10. KSNS Error vs Temperature



I_{OUT} = 1A V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-11. KSNS Error vs VBB

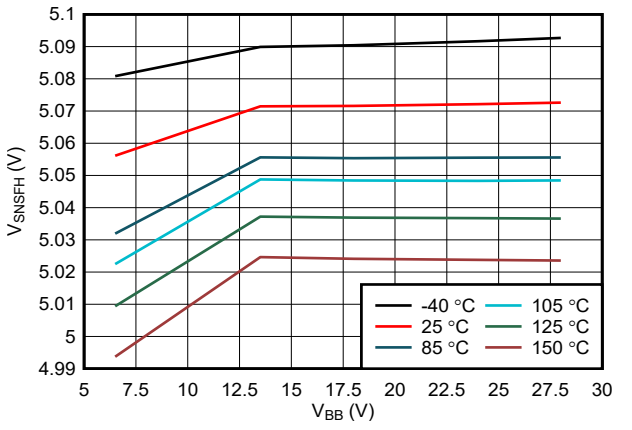


R_{OUT} = 5µH and 100 mΩ V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-12. VSNSFH (3.3 V) vs VBB

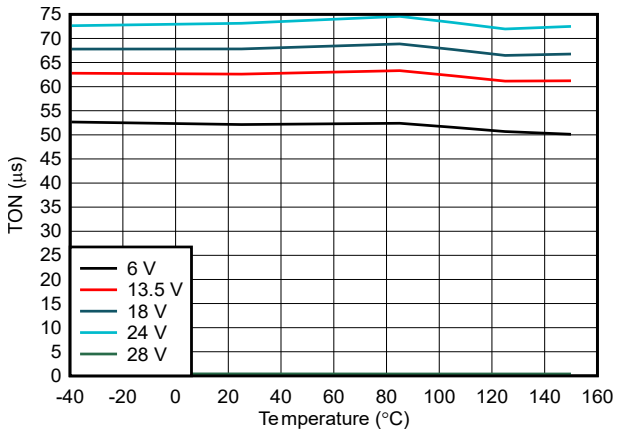
5.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VBB} = 13.5 V if not specified.



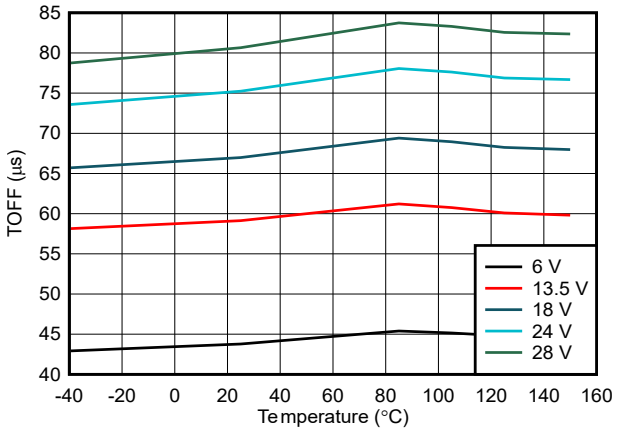
R_{OUT} = 5µH and 100 mΩ V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-13. VSNSFH (5 V) vs VBB



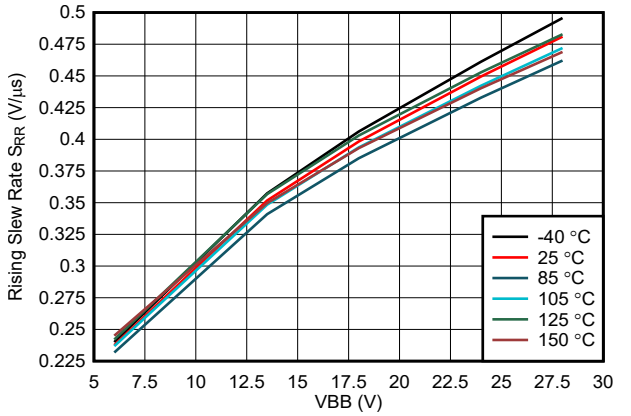
R_{OUT} = 10 Ω V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-14. Turn on time T_{ON} vs Temperature



R_{OUT} = 10 Ω V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-15. Turn off time T_{OFF} vs Temperature

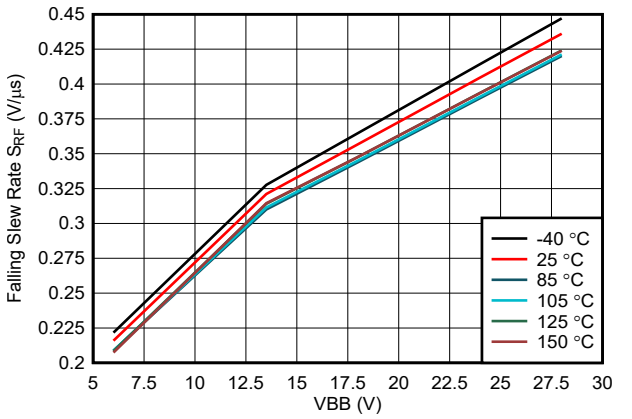


R_{OUT} = 10 Ω V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-16. Rising Slew Rate SRR vs Temperature

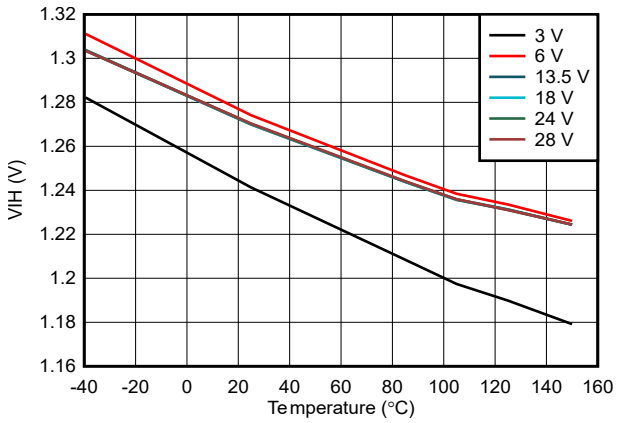
5.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VBB} = 13.5 V if not specified.



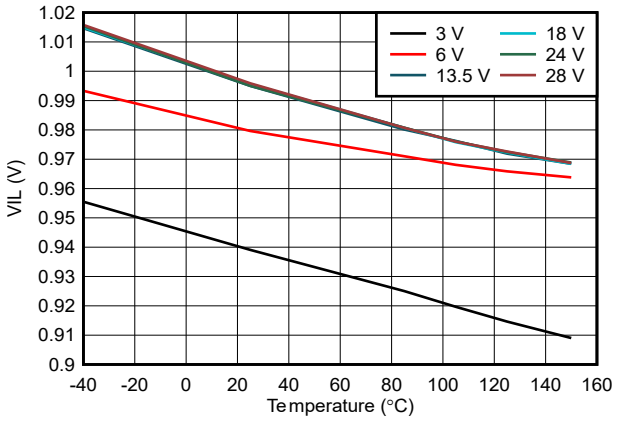
R_{OUT} = 10 Ω V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-17. Falling Slew Rate SRF vs Temperature



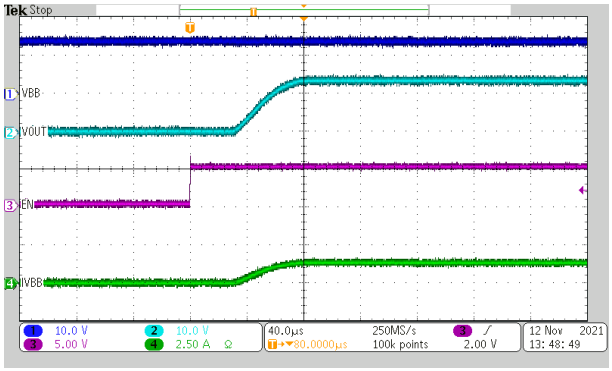
R_{OUT} = 1 kΩ V_{EN} = 0 to 3.3 V V_{DIAG_EN} = 0 to 3.3 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-18. V_{IH} vs Temperature



R_{OUT} = 1 kΩ V_{EN} = 3.3 to 0 V V_{DIAG_EN} = 3.3 to 0 V
V_{BB} varied R_{SNS} = 1 kΩ

図 5-19. V_{IL} vs Temperature

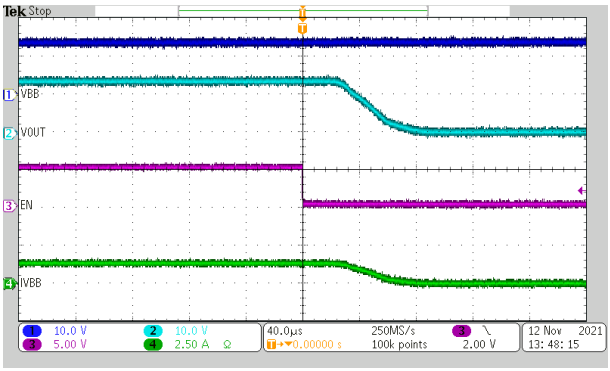


R_{OUT} = 10 Ω V_{EN} = 0 to 5 V V_{DIAG_EN} = 0 V
V_{BB} = 13.5 V R_{SNS} = 1 kΩ

図 5-20. Turn-on Time (t_{ON})

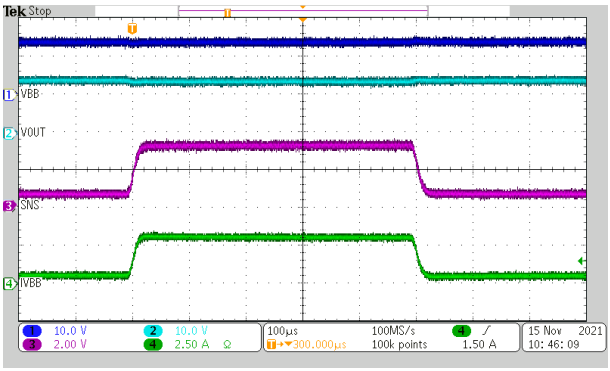
5.8 Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VBB} = 13.5 V if not specified.



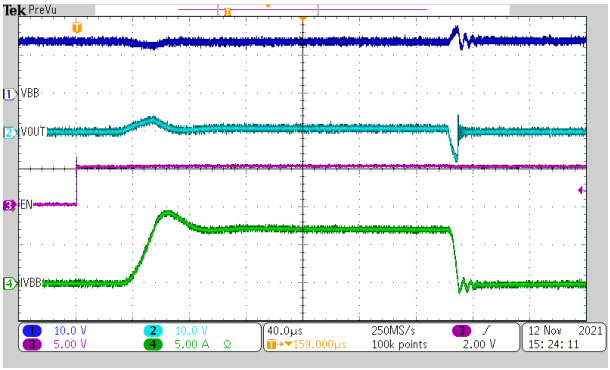
R_{OUT} = 10 Ω V_{EN} = 5 to 0 V V_{DIAG_EN} = 0 V
V_{BB} = 13.5 V R_{SNS} = 1 kΩ

図 5-21. Turn-off Time (t_{OFF})



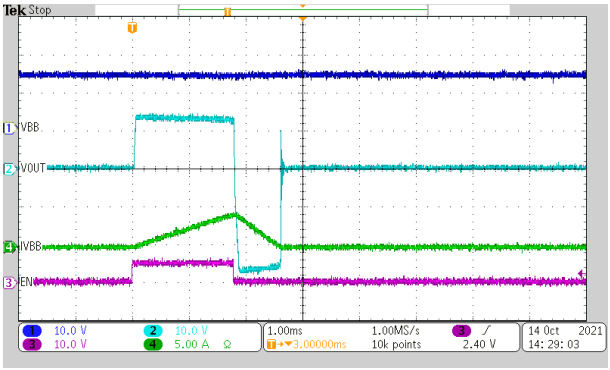
I_{OUT} = 500 mA to 3 A V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} = 13.5 V R_{SNS} = 1 kΩ

図 5-22. ISNS Settling Time (t_{SNSION}) on Load Step



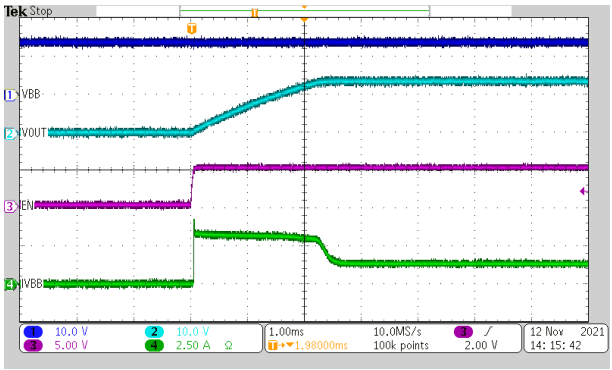
R_{OUT} = 5 µH and 100 mΩ V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} = 13.5 V R_{SNS} = 1 kΩ R_{ILIM} = GND

図 5-23. Short Circuit With ILIM Shorted to Ground



R_{OUT} = 5 mH V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} = 13.5 V R_{SNS} = 1 kΩ R_{ILIM} = GND

図 5-24. 5mH Inductive Load Driving



R_{OUT} = 470 µF and 10 Ω V_{EN} = 5 V V_{DIAG_EN} = 5 V
V_{BB} = 13.5 V R_{SNS} = 1 kΩ R_{ILIM} = open

図 5-25. 470-µF Capacitive Load Driving

6 Parameter Measurement Information

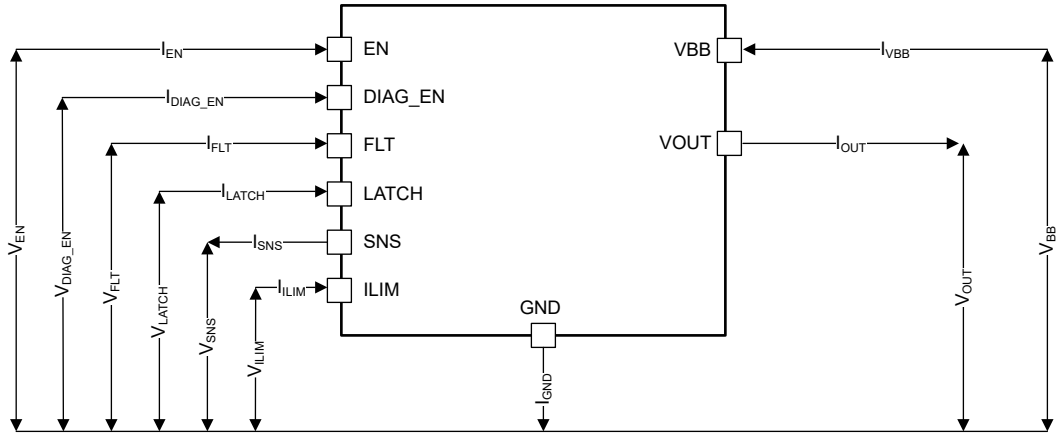
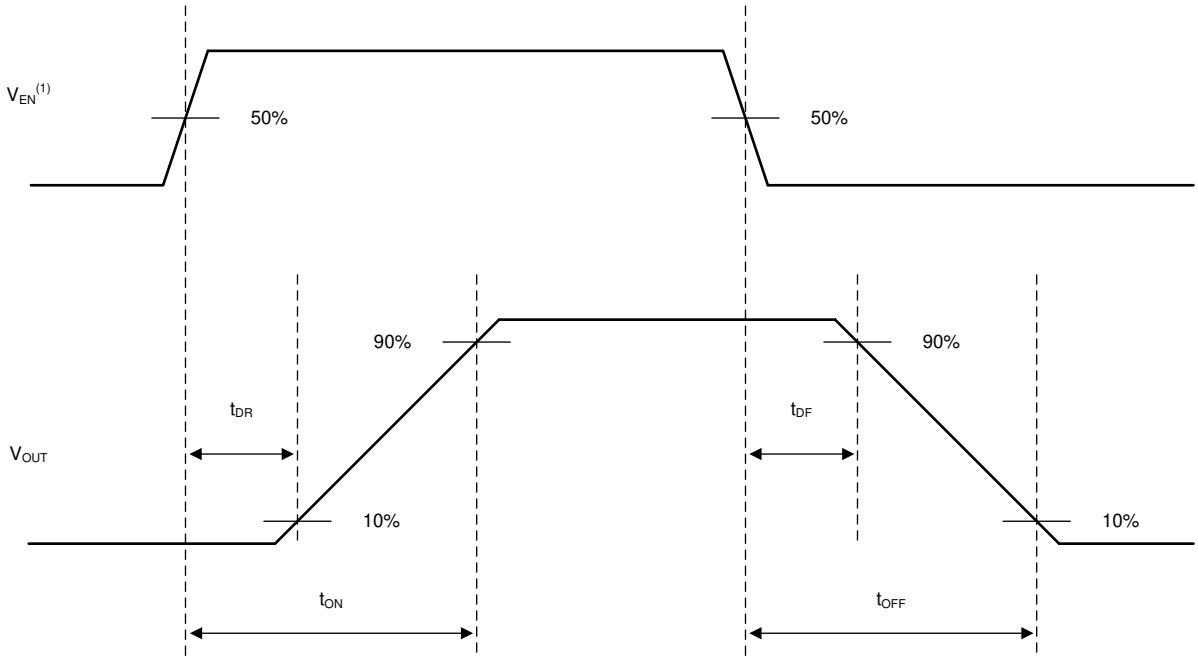
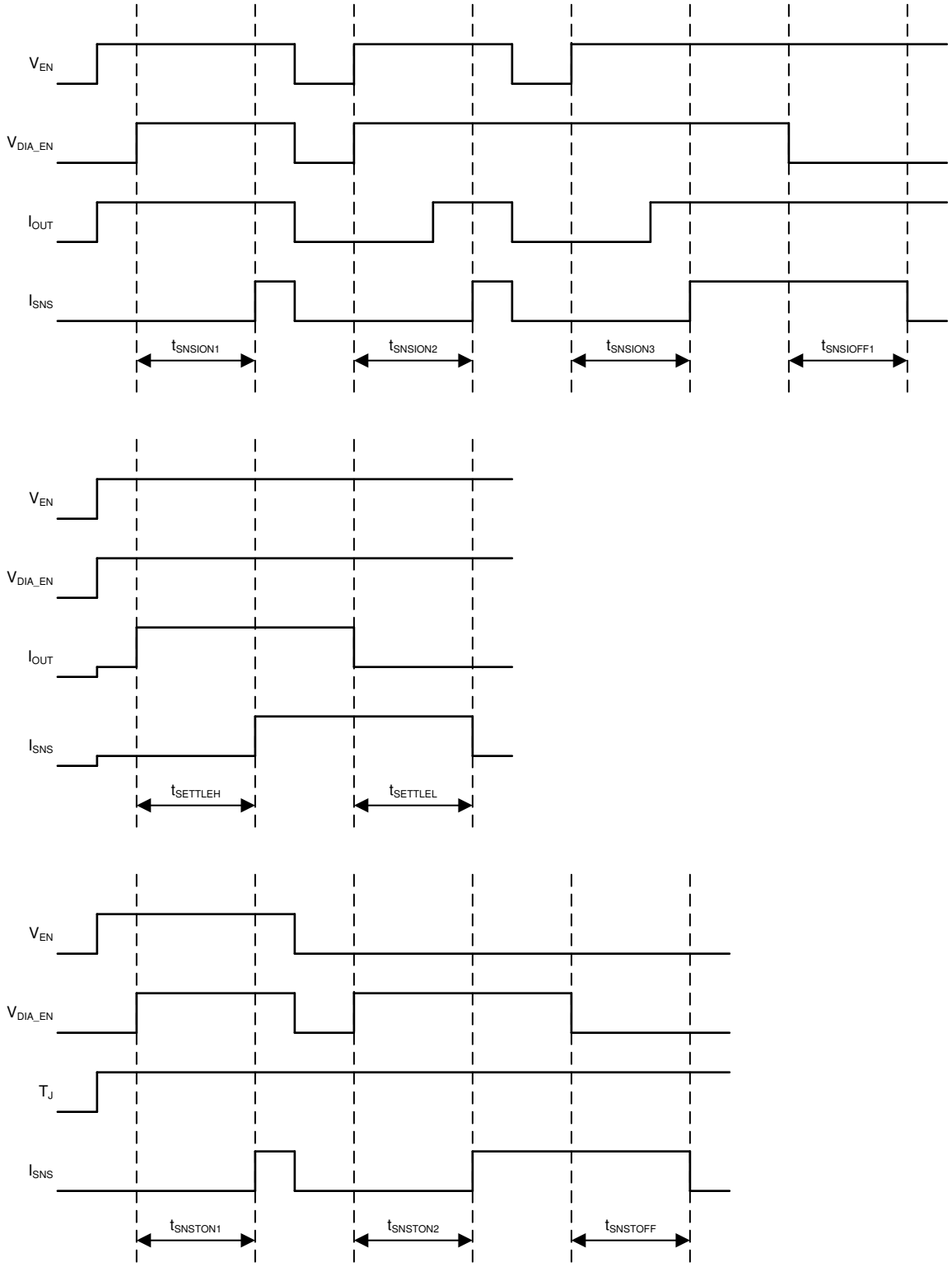


図 6-1. Parameter Definitions



Rise and fall time of V_{EN} is 100 ns.

図 6-2. Switching Characteristics Definitions



Rise and fall times of control signals are 100 ns. Control signals include: EN, DIA_EN.

図 6-3. SNS Timing Characteristics Definitions

7 Detailed Description

7.1 Overview

The TPS1HC100-Q1 is a single-channel, fully-protected, high-side power switch with an integrated NMOS power FET and charge pump. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. Low logic high threshold, V_{IH}, of 1.5 V on the input pins allow use of MCU GPIO signals of 1.8 V. A programmable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two pins to support both digital status and analog current-sense output, both of which can be set to the high-impedance state when diagnostics are disabled, for multiplexing the MCU analog or digital interface among devices.

The digital status report is implemented with an open-drain structure on the fault pin. When a fault condition occurs, the pin is pulled down to GND. An external pullup is required to match the microcontroller supply level. High-accuracy current sensing allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, which is reflected as voltage on the SNS pin. K_{SNS} is a constant value across the temperature and supply voltage. The current-sensing function operates normally within a wide linear region from 0 to 4 V. The SNS pin can also report a fault by forcing a voltage of V_{SNSFH} that scales with the diagnostic enable voltage so that the maximum voltage seen by the system's ADC is within an acceptable value. This action removes the need for an external zener diode or resistor divider on the SNS pin.

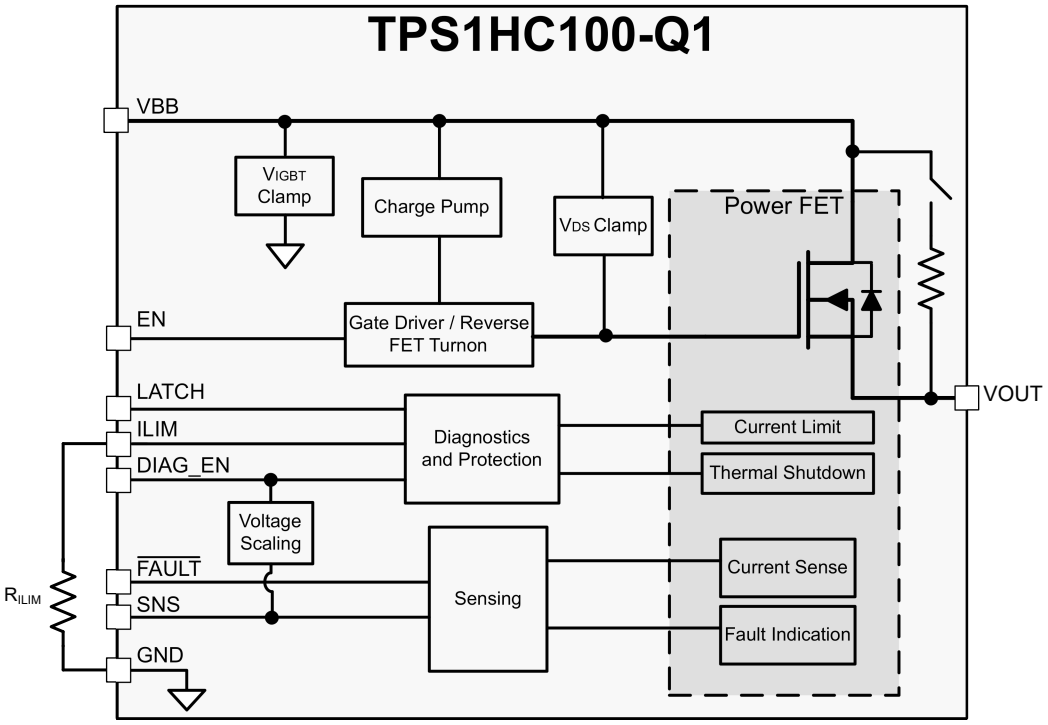
The external high-accuracy current limit allows setting the current limit value by application. The current limit highly improves the reliability of the system by clamping the inrush current effectively under start-up or short-circuit conditions. Also, the current limit can save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit is also implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain to source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself. With the benefits of process technology and excellent IC layout, the TPS1HC100-Q1 device can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. For more details, see *Inductive-Load Switching-Off Clamp*.

Short-circuit reliability is critical for smart high-side power-switch devices. The standard of AEC-Q100-012 is to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short-to-GND certification.

The TPS1HC100-Q1 device can be used as a high-side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Accurate Current Sense

The high-accuracy current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

K_{SNS} is the ratio of the output current and the sense current. The accuracy values of K_{SNS} quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.

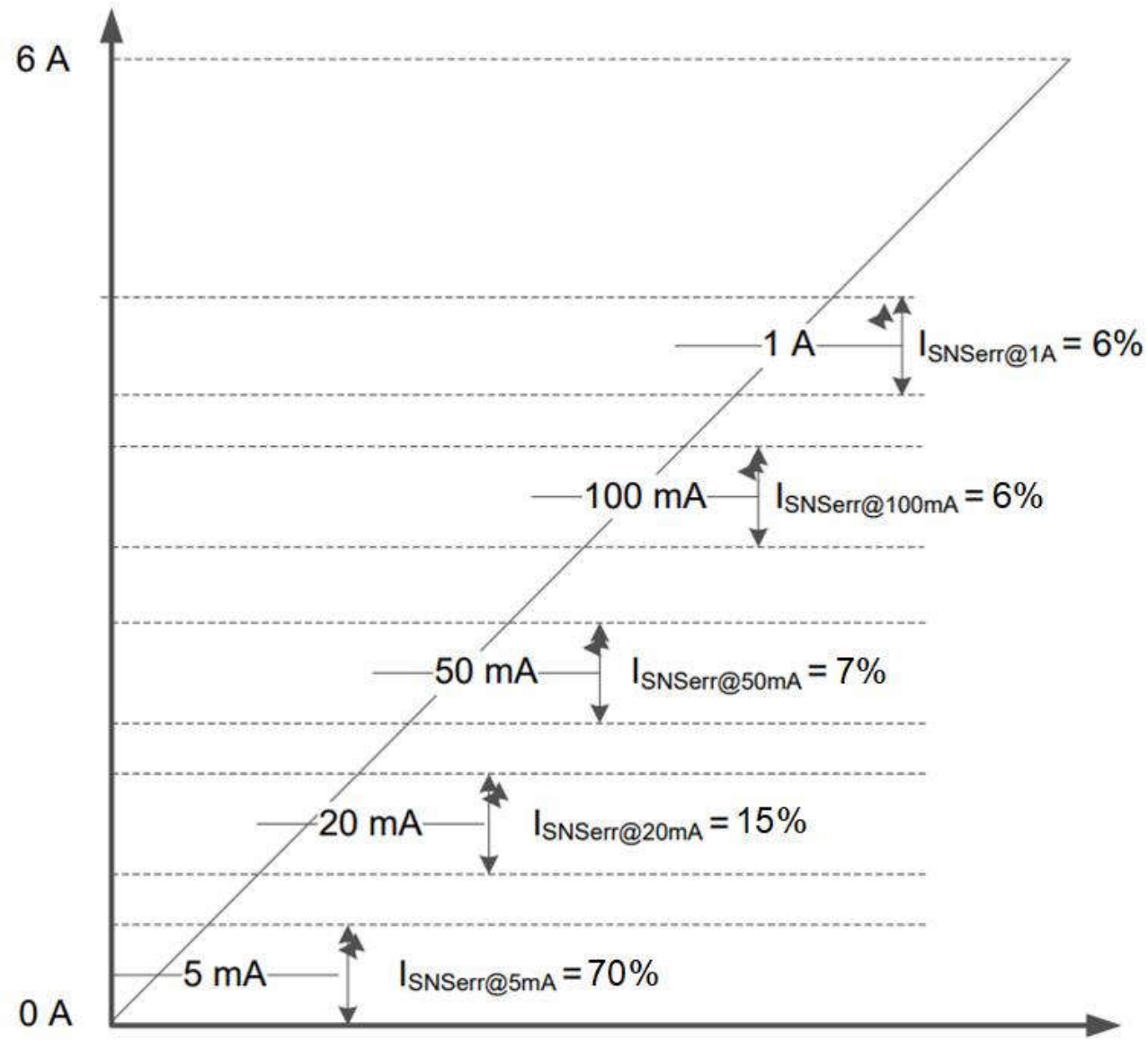


図 7-1. Current-Sense Accuracy

The maximum voltage out on the SNS pin is clamped to V_{SNSFH}, which is the fault voltage level. To make sure that this voltage is not higher than the system can tolerate, TI has correlated the voltage coming in on the DIAG_EN pin with the maximum voltage out on the SNS pin. If DIAG_EN is between V_{IH} and 3.3 V, the maximum output on the SNS pin is approximately 3.3 V. However, if the voltage at DIAG_EN is above 3.3 V, then the fault SNS voltage, V_{SNSFH}, tracks that voltage up to 5 V. Tracking is done because the GPIO voltage output that is powering the diagnostics through DIAG_EN is close to the maximum acceptable ADC voltage within the same microcontroller. Therefore, the sense resistor value, R_{SNS}, can be chosen to maximize the range of currents needed to be measured by the system. The R_{SNS} value must be chosen based on application need. The maximum usable R_{SNS} value is bounded by the ADC minimum acceptable voltage, $V_{ADC,min}$, for the smallest load current needed to be measured by the system, $I_{LOAD,min}$. The minimum acceptable R_{SNS} value has to ensure the V_{SNS} voltage is below the V_{SNSFH} value so that the system can determine faults. This difference between the maximum readable current through the SNS pin, $I_{LOAD,max} \times R_{SNS}$, and the V_{SNSFH} is called the headroom voltage, V_{HR}. The headroom voltage is determined by the system but is important so that there is a difference between the maximum readable current and a fault condition. Therefore, the minimum R_{SNS} value has

to be the V_{SNSFH} minus the V_{HR} times the sense current ratio, K_{SNS} divided by the maximum load current the system must measure, $I_{LOAD,max}$. This boundary equation can be seen in 式 1.

$$(V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \geq R_{SNS} \geq V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \quad (1)$$

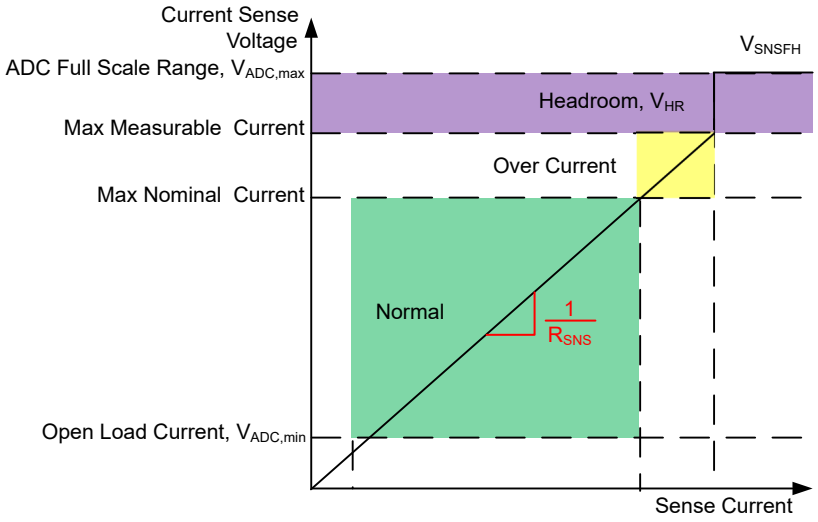


図 7-2. Voltage Indication on the Current-Sense Pin

The maximum current the system wants to read, $I_{LOAD,max}$, must be below the current limit threshold because after the current limit threshold is tripped the V_{SNS} value goes to V_{SNSFH}. Additionally, currents being measured must be below 6 A to ensure that the current sense output is not saturated.

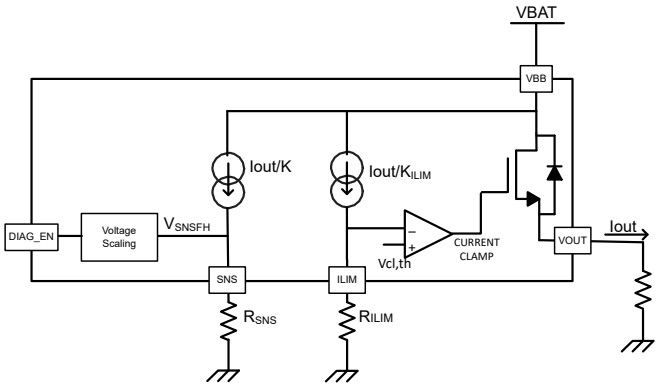


図 7-3. Current-Sense and Current-Limit Block Diagram

Because this scheme adapts based on the voltage coming in from the MCU, there is no need to have a Zener diode on the SNS pin to protect from high voltages.

7.3.2 Programmable Current Limit

A high-accuracy current limit allows higher reliability, which protects the power supply during short circuit or power up. Also, a current limit can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limiting offers protection from over-stressing to the load and integrated power FET. The current limit regulates the output current to the set value, and pulls up the SNS pin to V_{SNSFH} and asserts the $\overline{FLT}$ pin as diagnostic reports. The three current-limit thresholds are:

- External programmable current limit – an external resistor, R_{ILIM}, is used to set the channel current limit. When the current through the device exceeds I_{CL} (current limit threshold), a closed loop steps in immediately.

V_{GS} voltage regulates accordingly, leading to the V_{DS} voltage regulation. When the closed loop is set up, the current is clamped at the set value. The external programmable current limit provides the capability to set the current-limit value by application.

Additionally, this value can be dynamically changed by changing the resistance on the ILIM pin. This information can be seen in the *Applications* section.

- Internal current limit: ILIM pin shorted to ground – if the external current limit is out of range on the lower end or the I_{LIM} pin is shorted to ground, the internal current limit is fixed and typically 7 A. To use the internal current limit for large-current applications, tie the ILIM pin directly to the device GND.
- Internal current limit: ILIM pin open – if the external resistor is out of range on the higher end or the ILIM pin is open, the current limit reverts to 3 A or half the current limit range. This level is still above the nominal operation for the device to operate in DC steady state but is low enough that if a pin fault occurs and the R_{ILIM} opens up, the current does not default to the highest rating and put additional stress on the power supply.

Both the internal current limit ($I_{lim,nom}$) and external programmable current limit are always active when V_{BB} is powered and EN is high. The lower value one (of I_{LIM} and the external programmable current limit) is applied as the actual current limit. The typical deglitch time for the current limit to assert is 2.5 µs.

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must be connected with device GND. Calculate R_{ILIM} with Equation 2.

$$R_{ILIM} = K_{CL} / I_{LIM} \quad (2)$$

For better protection from a *hot short* condition (when V_{BB} is high, channel is on, and a short to GND happens suddenly), an over current protection, OVCR, circuit is triggered that makes sure to limit the maximum current the device allows to go through. With this OVCR, the device is protected during *hot short* events.

For more information about the current limiting feature, see the *Short-Circuit and Overload Protection* section.

Current Limit Accuracy

The TPS1HC100-Q1 has very tight accuracy of the current limit regulation level across the full range of currents and temperature. This accuracy is defined at several defined R_{ILIM} values, 7.15 kΩ, 25 kΩ, and 71.5 kΩ specified in the Electrical Characteristics. As the current limit is changed with the R_{ILIM}, the KCL ratio value also slightly changes. Additionally, the current limit architecture in the device allows for the tightest variation at current limit set by a 25-kΩ R_{ILIM}, 1.9 A, of +18%, -7% and at the lower and upper ends of the range, 690 mA and 6.15 A respectively, to be about ±25%. Then, using the boundaries for R_{ILIM} of 7.15 kΩ and 71.5 kΩ, a graph can be built to linearly interpret the error for RILIM values that are inside of the range. This graph can be seen in the figure below.

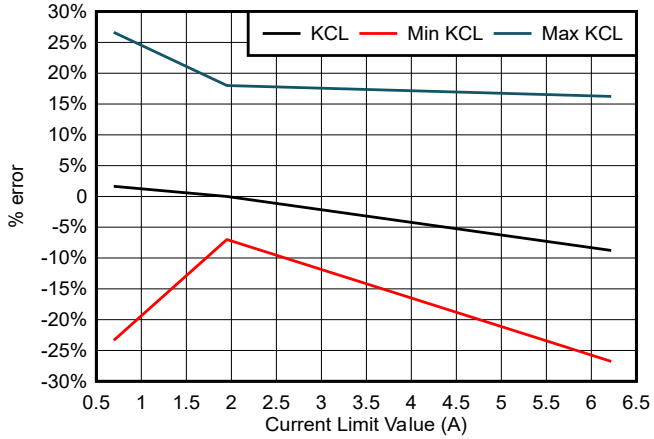


図 7-4. Current Limit Ratio vs Current limit Value With Percent Error

Using this figure, the error can be estimated for any current limit value desired, and the associated KCL value can determine the RILIM resistor appropriate. This graph does not take into account RILIM resistor tolerances, only the error associated with the current limit regulation.

7.3.2.1 Capacitive Charging

図 7-5 shows the typical set up for a capacitive load application and the internal blocks that function when the device is used. Note that all capacitive loads have an associated *load* in parallel with the capacitor that is described as a resistive load but in reality it can be inductive or resistive.

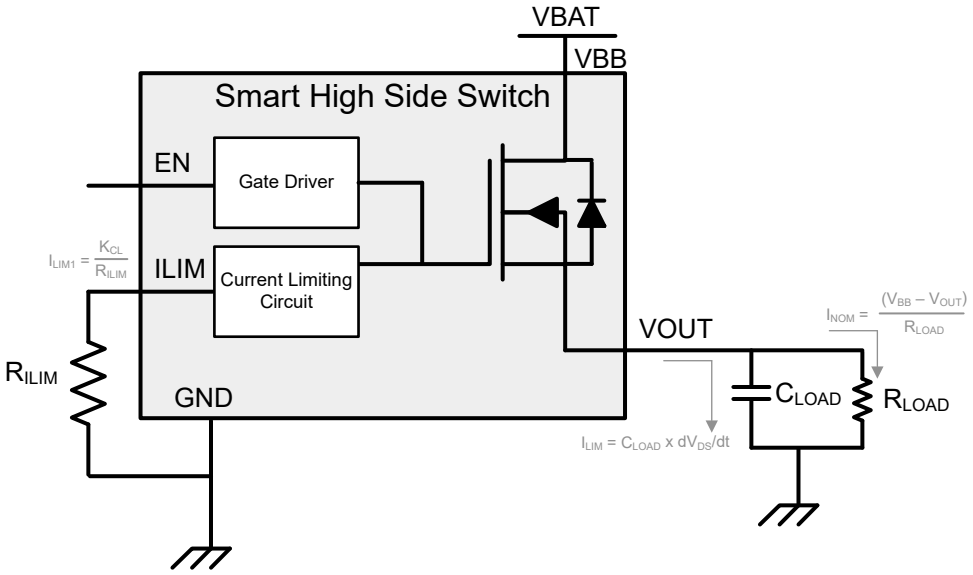


図 7-5. Capacitive Charging Circuit

The first thing to check is that the nominal DC current, I_{NOM}, is acceptable for the TPS1HC100-Q1 device. This check can easily be done by taking the $R_{\theta JA}$ from the *Thermal* section and multiplying the R_{ON} of the TPS1HC100-Q1 and the I_{NOM} with it, add the ambient temperature and if that value is below the thermal shutdown value the device can operate with that load current. For an example of this calculation see the *Applications* section.

The second key care about for this application is to make sure that the capacitive load can be charged up completely without the device hitting thermal shutdown. The reason is because if the device hits thermal shutdown during the charging, the resistive nature of the load in parallel with the capacitor starts to discharge the capacitor over the duration the TPS1HC100-Q1 is off. Note that there are some application with high enough load impedance that the TPS1HC100-Q1 hitting thermal shutdown and trying again is acceptable; however, for the majority of applications, the system must be designed so that the TPS1HC100-Q1 does not hit thermal shutdown while charging the capacitor.

With the current clamping feature of the TPS1HC100-Q1, capacitors can be charged up at a lower inrush current than other high current limit switches. This lower inrush current means that the capacitor takes a little longer to charge all the way up. The time that it takes to charge up follows the equation below.

$$I_{LIM} = C \times d(V_{BB} - V_{DS}) / dt \quad (3)$$

However, because the V_{DS} for a typical 1 A applications is much less than the V_{BB} voltage ($V_{DS} \approx 1A \times 0.1\ \Omega = 100$ mV, $V_{BB} \approx 13.5$ V), the equation can be rewritten and approximated as

$$dt = C \times dV_{BB} / I_{LIM} \quad (4)$$

図 7-6 pictures this charge timing.

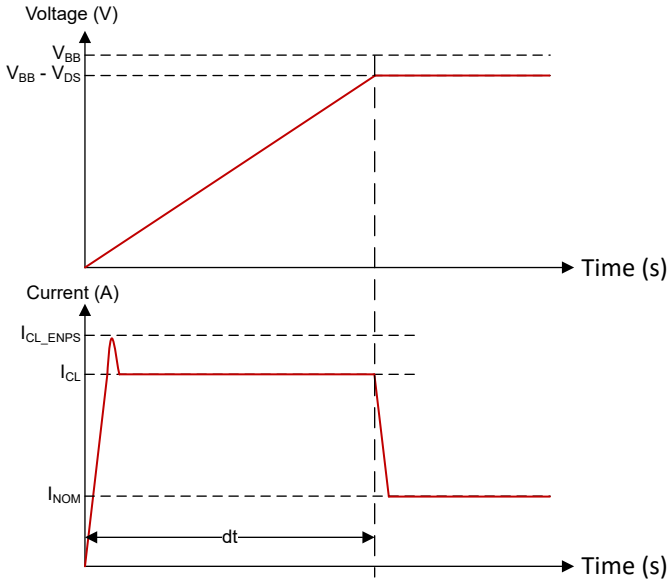


図 7-6. Capacitive Charging Timing

For more information about capacitive charging with high side switches, see the *How to Drive Capacitive Loads* application note application note. This application note has information about the thermal modeling available along with quick ways to estimate if a high side switch is able to charge a capacitor to a given voltage.

7.3.3 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET can break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely $V_{DS,clamp}$, the clamp diode between the drain and gate.

$$V_{DS,clamp} = V_{BAT} - V_{OUT} \tag{5}$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductance-energy dissipation. Both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself, which is called E_{HSD}. If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_{BAT} + E_{LOAD} = E_{BAT} + E_L - E_R \tag{6}$$

From the high-side power switch's view, E_{HSD} equals the integration value during the current-decay period.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t)\,dt \tag{7}$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \tag{8}$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \tag{9}$$

When R approximately equals 0, E_{HSD} can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \frac{V_{BAT} + |V_{OUT}|}{R^2} \quad (10)$$

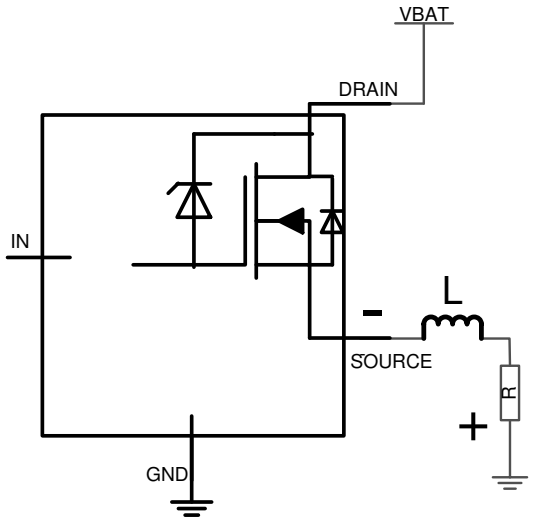


図 7-7. Driving Inductive Load

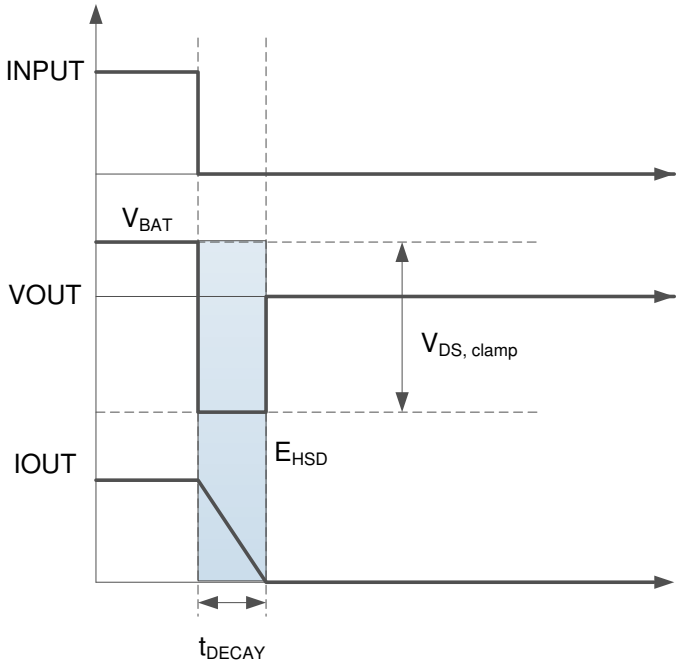


図 7-8. Inductive-Load Switching-Off Diagram

When switching off, battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

See Figure 8-9 for one dedicated inductance, 5 mH. If the maximum switching-off current is lower than the current value shown on the curve, the internal clamp function can be used for the demagnetization energy dissipation. If not, external free-wheeling circuitry is necessary for device protection.

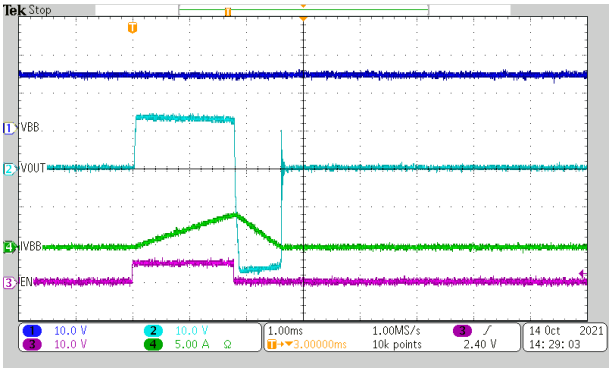


図 7-9. 5-mH Maximum Demagnetization Curve

7.3.4 Full Protections and Diagnostics

表 7-1 is when DIAG_EN is enabled. When DIAG_EN is low, current sense and FLT are disabled. The output is in high-impedance mode. Refer to 表 7-1 for details.

表 7-1. Diagnostic Enable Logic Table

DIAG_EN	IN Condition	Protections and Diagnostics
HIGH	ON	See *Fault Table*
	OFF	
LOW	ON	Diagnostics disabled, protection normal $\overline{FLT}$ is high impedance, SNS is not driven and is clamped to 1.5V if external voltage is applied to the pin
	OFF	

表 7-2. Fault Table

Conditions	EN	VOUT	Latch	$\overline{FLT}$	SNS	Behavior	Recovery
Normal	L	L	x	Hi-Z	0	Normal	
	H	$V_{BB} - I_{LOAD} \times R_{ON}$	x	Hi-Z	I_{Load} / K_{sns}	Normal	
Overcurrent	H	$V_{BB} - I_{LIM} \times R_{LOAD}$	x	L	V_{SNSFH}	Holds the current at the current limit until thermal shutdown or when the overcurrent event is removed. Typical deglitch time for device to recognize overcurrent fault and begin to act on it is 2.5 µs.	
STG, Relative Thermal Shutdown, Absolute Thermal Shutdown	H	H/L	L	L	V_{SNSFH}	Shuts down when devices hits relative or absolute thermal shutdown. Typical deglitch time for device to recognize overcurrent fault and begin to act on it is 2.5 µs. Typical deglitch time for device to recognize a T_{ABS} fault is 20 µs.	Auto retries when T_{HYS} is met and it has been longer than t_{RETRY} amount of time
	H	H/L	H	L	V_{SNSFH}	Shuts down when devices hits relative or absolute thermal shutdown. Typical deglitch time for device to recognize overcurrent fault and begin to act on it is 2.5 µs. Typical deglitch time for device to recognize a T_{ABS} fault is 20 µs.	Stays off until latch or enable is toggled

表 7-2. Fault Table (続き)

Conditions	EN	VOUT	Latch	$\overline{FLT}$	SNS	Behavior	Recovery
Open load, STB	H	H	x	Hi-Z	I_{Load} / K_{SNS} = ~0	Normal behavior, user can judge through SNS pin output if it is an open load or not.	
	L	H	x	L	V_{SNSFH}	Internal pullup resistor is active. If V_{BB} – V_{OUT} < V_{OL} then fault active. Typical deglitch time before fault is indicated is 700 µs.	Clears when fault goes away
Reverse Polarity	x	x	x	x	x	Channel turns on to lower power dissipation. Current into ground pin is limited by external ground network.	

表 7-3. Deglitch Time for Each Fault Condition

Fault Condition	Deglitch Time
ILIM	2.5 µs
TREL	2.5 µs
TABS	20 µs
Open load	700 µs

7.3.4.1 Short-Circuit and Overload Protection

TPS1HC100-Q1 provides output short-circuit protection to ensure that the device prevents current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The device is ensured to protect against short-circuit events regardless of the state of the ILIM pins and with up to 28-V supply at 125°C.

図 7-10 shows the behavior of the TPS1HC100-Q1 when the device is enabled into a short-circuit.

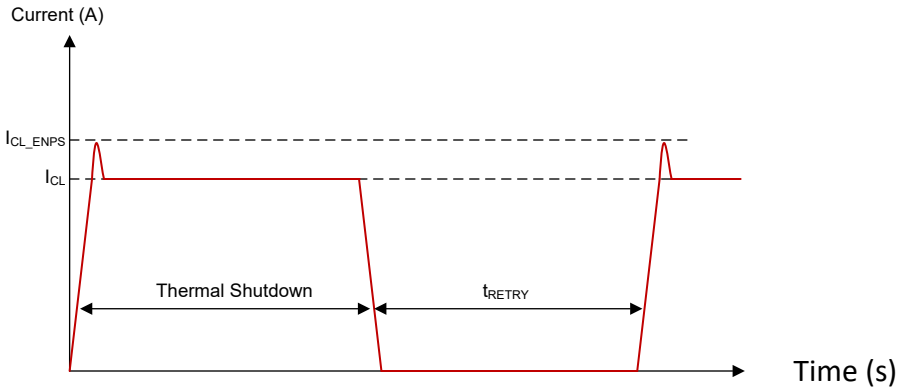


図 7-10. Enable into Short-Circuit Behavior (LATCH = 0)

Due to the low impedance path, the output current rapidly increases until it hits the current limit threshold. Due to the response time of the current limiting circuit, the measured maximum current can temporarily exceed the I_{CL} value defined as I_{CL_ENPS}, however, it settles to the current limit regulation value. The amount of deglitch timing between when the overload is recognized and when the system begins to react on it is about 2.5 µs.

In this state, high power is dissipated in the FET, so eventually the internal thermal protection temperature for the FET is reached and the device safely shuts down. Then, if LATCH pin is low, the part waits t_{RETRY} amount of time and turn back on, unless a T_{ABS} fault was triggered in which case it can AND the t_{RETRY} timer and the T_{HYS} temperature reduction.

図 7-11 shows the behavior of the TPS1HC100-Q1 when a short-circuit occurs when the device is in the on-state and already outputting current. When the internal pass FET is fully enabled, the current clamping settling time is slower so to ensure overshoot is limit. The device implements a fast-trip level at a level I_{OVCR}. When this fast-trip threshold is hit, the device immediately shuts off for a short period of time before quickly re-enabling and clamping the current to I_{CL} level after a brief transient overshoot to the higher peak current (I_{CL_ENPS}) level. The device then keeps the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device safely shuts off.

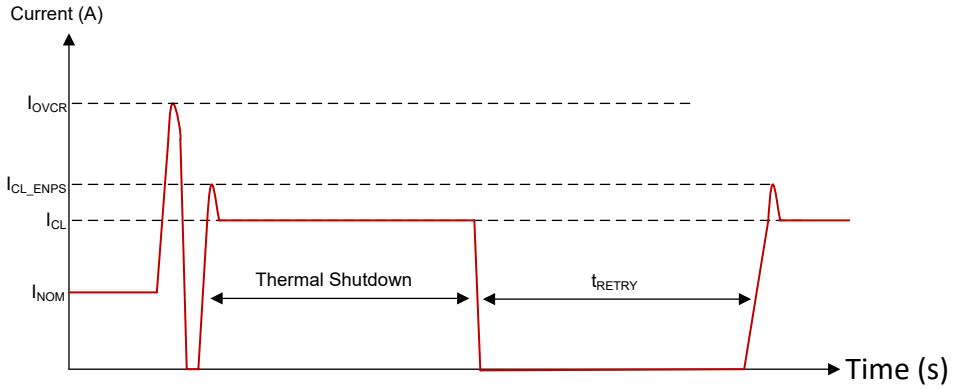


図 7-11. On-State Short-Circuit Behavior

Overload Behavior shows the behavior of the TPS1HC100-Q1 when there is a small change in impedance that sends the load current above the I_{CL} threshold. The current rises (commonly referred to as current creep) to I_{CL_LINPK} above the regulation level. Then the current limit regulation loop kicks in and the current drops to the I_{CL} value.

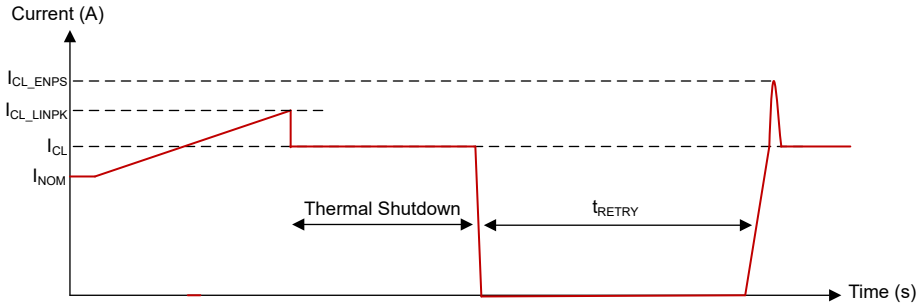


図 7-12. Overload Behavior (Current Creep)

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

7.3.4.2 Open-Load and Short-to-Battery Detection

When the main channel is enabled faults are diagnosed by reading the voltage on the SNS or $\overline{FLT}$ pin and evaluated by the user. A benefit of high-accuracy current sense is that this device can achieve a very low open-load detection threshold, which correspondingly expands the normal operation region. TI suggests 5 mA as the upper limit for the open-load detection threshold and 15 mA as the lower limit for the normal operation current. In 図 7-13, the recommended open-load detection region is shown as the dark-shaded region and the light-shaded region is for normal operation. As a guideline, do not overlap these two regions.

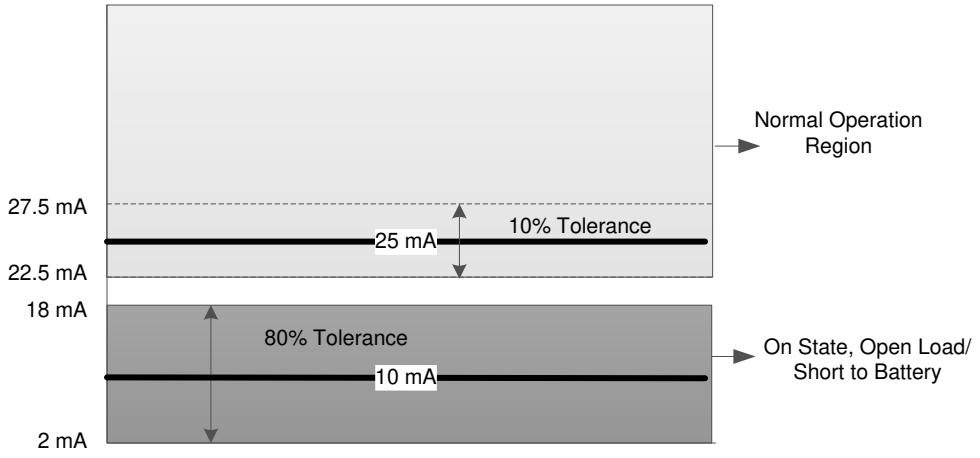


図 7-13. On-State Open-Load Detection and Normal-Operation Diagram

In the off state, if a load is connected, the output voltage is pulled to 0 V. In the case of an open load, the output voltage is close to the supply voltage, $V_{BB} – V_{OUT} < V_{ol,off}$. The FLT pin goes low to indicate the fault to the MCU, and the SNS pin is pulled up to I_{SNSFH}. There is always a leakage current $I_{ol,off}$ present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, TI implemented an internal pullup resistor to offset the leakage current. This pullup current must be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, TI implemented a switch in series with the pullup resistor controlled by the DIAG_EN pin. The pull up resistor value is $R_{pu} \leq 150\ k\Omega$.

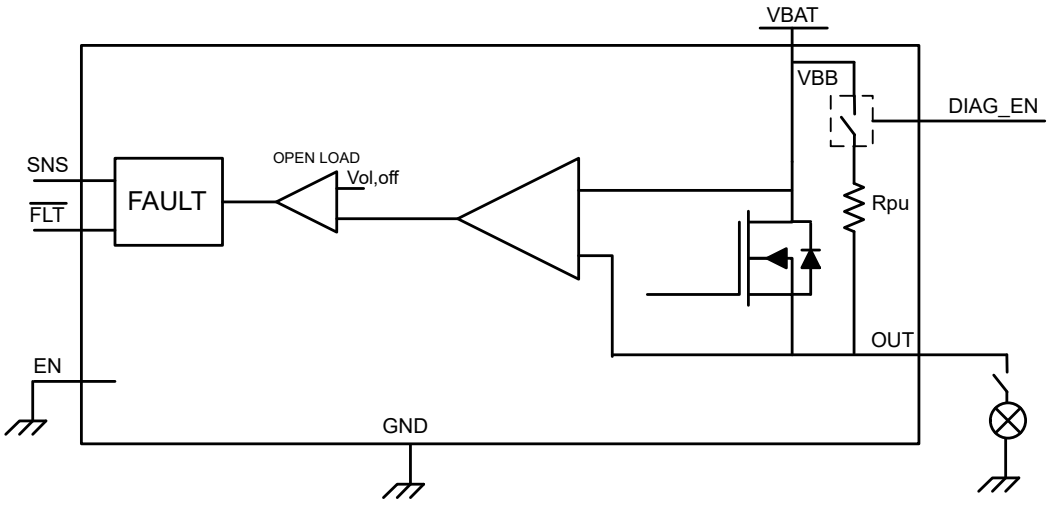


図 7-14. Open-Load Detection Circuit

7.3.4.3 Short-to-Battery Detection

Short-to-battery detection has the same detection mechanism and behavior as open-load detection, both in the on-state and off-state. There is no way to differentiate between open load and short-to-battery in this device, but the system does detect the fault and protect accordingly. See 表 7-2 for more details.

7.3.4.4 Reverse-Polarity and Battery Protection

Reverse-polarity, commonly referred to as reverse battery, occurs when the ground of the device goes to the battery potential, $V_{GND} = V_{BAT}$, and the supply pin goes to ground, $V_{BB} = 0$ V. In this case, if the EN pin has a path to the *ground* plane, then the FET turns on to lower the power dissipation through the main channel and prevent current flow through the body diode. Note that the resistor/diode ground network (if there is not a central blocking diode on the supply) must be present for the device to protect itself during a reverse battery event.

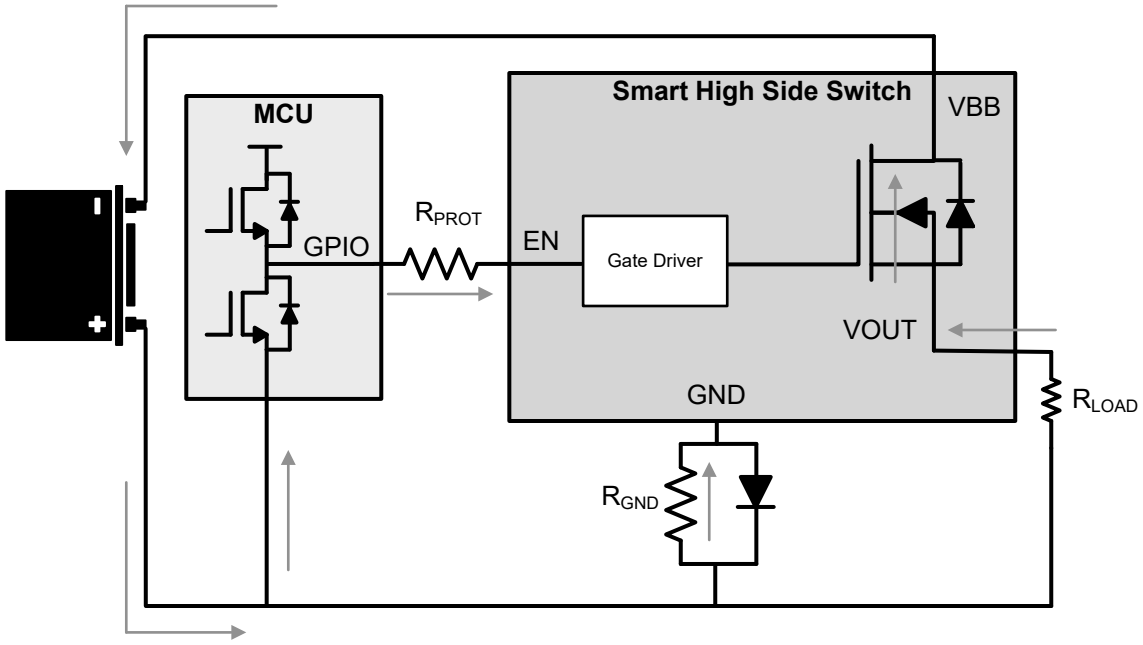


図 7-15. Reverse Battery Circuit

For more external protection circuitry information, see *Reverse Current Protection*. See the fault truth table for more details.

7.3.4.5 Latch-Off Mode

The TPS1HC100-Q1 comes with a latch functionality that decides after the channel is shut down due to a fault, whether or not to automatically try and turn back on, or stay off until other action is taken. This action is done by holding the LATCH pin high for latch-off functionality or holding LATCH low for auto-retry functionality.

The order that occurs is:

1. Device shuts down due to fault (relative thermal shutdown)
2. Wait t_{RETRY}
3. If LATCH = 0
   a. Turn back on the channel
4. If LATCH = 1
   a. Keep off until LATCH = 0 || EN = 0
      i. Then if LATCH = 0 and EN = 1
         1. Turn on channel into auto-retry mode
      ii. If LATCH = 1 and EN = 1
         1. Turn on channel into latch mode where if another fault occurs then output is latched off again

For more information, see *Thermal Protection Behavior*.

7.3.4.6 Thermal Protection Behavior

The thermal protection behavior can be split up into three categories of events that can happen. 図 7-16 shows each of these categories.

1. **Relative thermal shutdown**: the device is enabled into an overcurrent event. The DIAG_EN pin is high so that diagnostics can be monitored on SNS and FLT (however, DIAG_EN being high is not necessary for all protection features to function). The output current rises up to the I_{ILIM} level and the FLT goes low while the

SNS goes to V_{SNSFH}. With this large amount of current going through the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises T_{REL} amount above the controller junction temperature $\Delta T = T_{FET} - T_{CON} > T_{REL}$, the device shuts down. The faults are continually shown on SNS and FLT and the part waits for the t_{RETRY} timer to expire. When t_{RETRY} timer expires, because the LATCH pin is low and EN is still high, the device comes back on into this I_{ILIM} condition.

2. **Absolute thermal shutdown**: the device is still enabled in an overcurrent event with DIAG_EN high and LATCH still low. However, in this case the junction temperature rises up and hits an absolute reference temperature, T_{ABS}, and then shuts down. The device does not recover until both $T_J < T_{ABS} - T_{hys}$ and the t_{RETRY} timer has expired.
3. **Latch-off mode**: the device is enabled into an overcurrent event. The DIAG_EN pin is high so that diagnostics can be monitored on SNS and FLT. The output current rises up to the I_{ILIM} level and the FLT goes low while the SNS goes to V_{SNSFH}. If the part shuts down due to a thermal fault, either relative thermal shutdown or absolute thermal shutdown, the device does not enable the channel until either the LATCH pin or the EN pin is toggled.

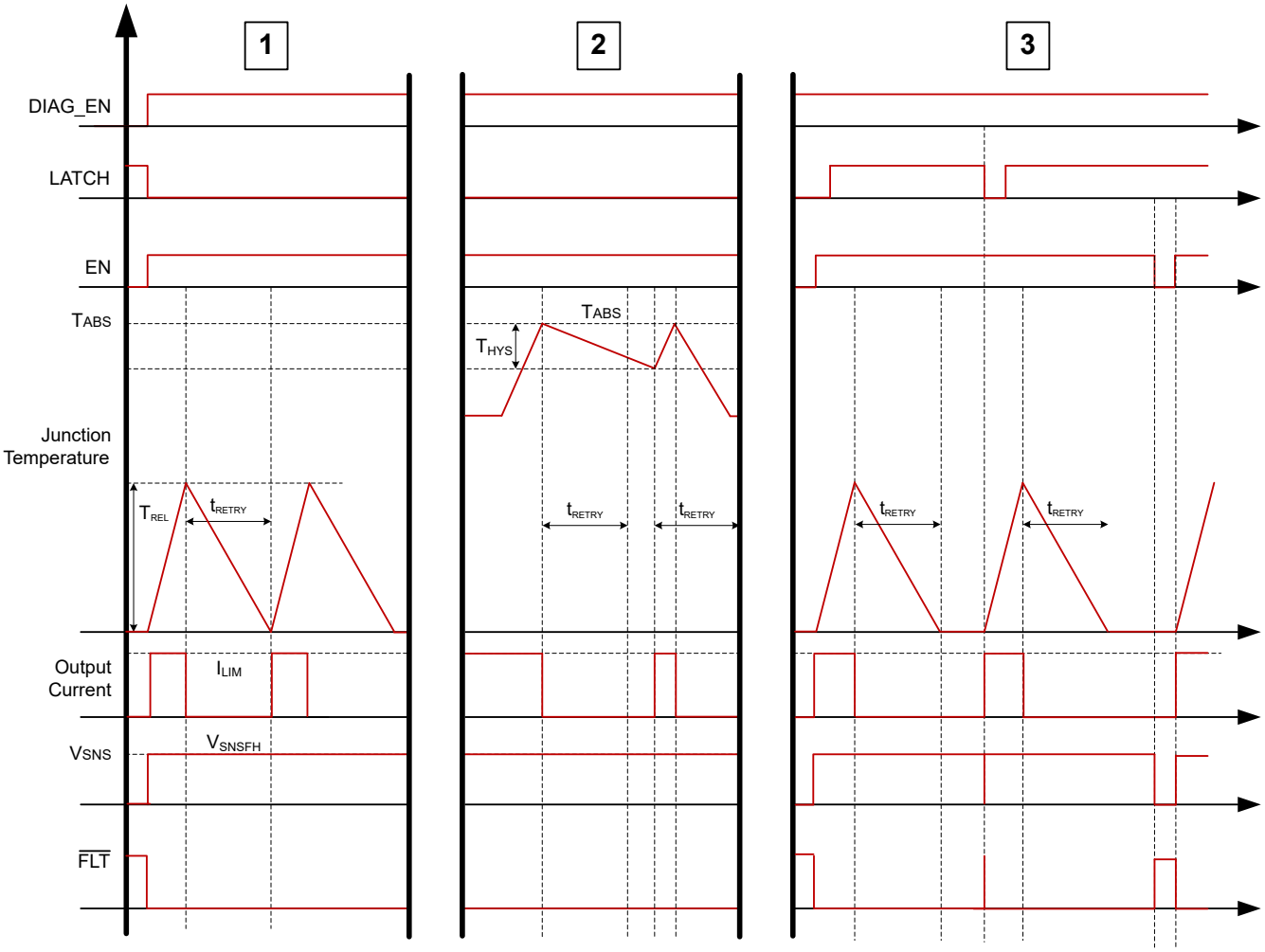


図 7-16. Thermal Behavior

7.3.4.7 UVLO Protection

The device monitors the supply voltage V_{BB} to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{UVLOF}, the output stage is shut down automatically.

When the supply rises up to V_{UVLOR}, the device turns on. If an overcurrent event trips the UVLO threshold, the device shuts off and comes back on into a current limit safely.

7.3.4.8 Loss of GND Protection

When loss of GND occurs, output is turned off regardless of whether the input signal is high or low.

Case 1 (loss of device GND): loss of GND protection is active when the thermal pad (Tab), I_{C_GND}, and current limit ground are one trace connected to the system ground, as shown in 図 7-17.

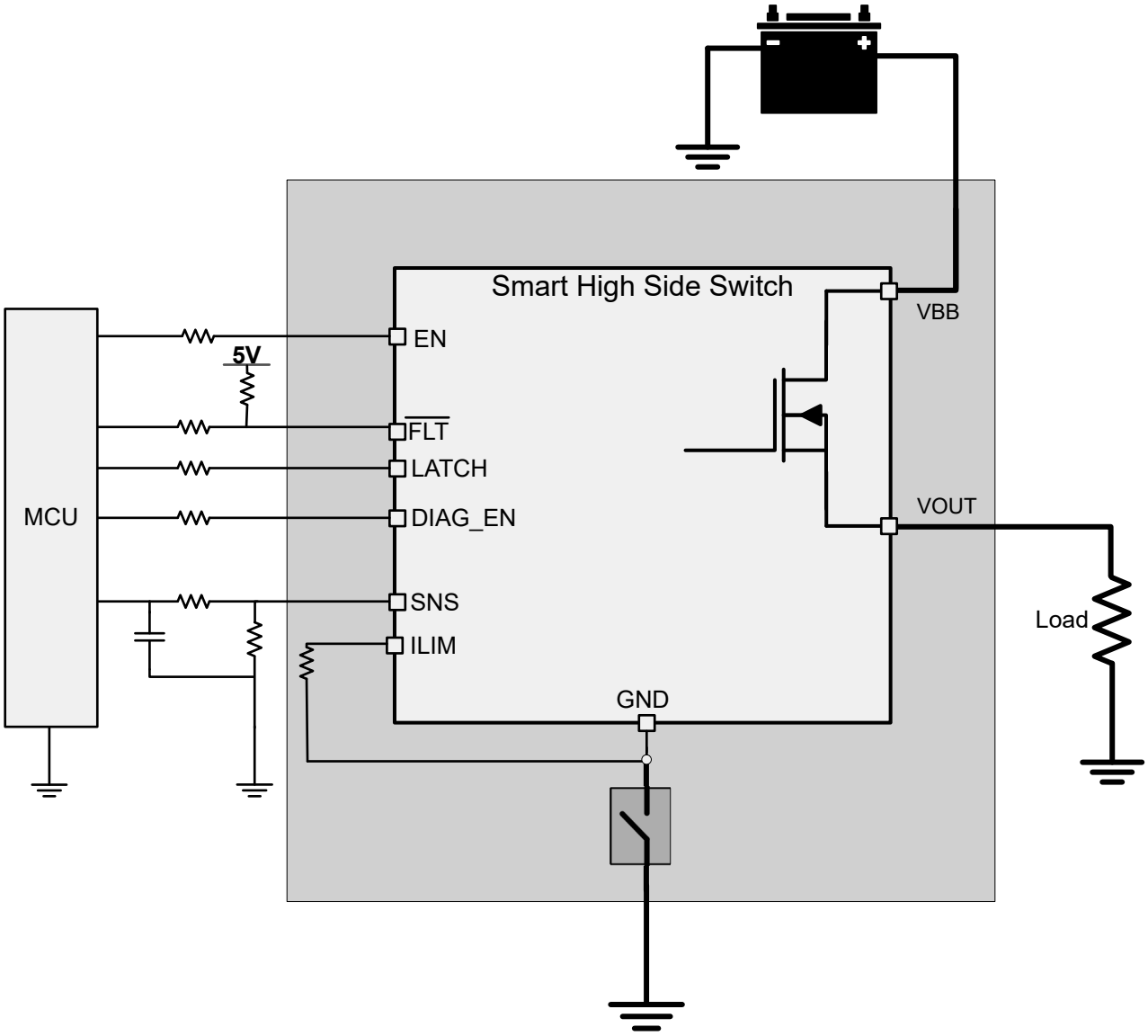


図 7-17. Loss of Device GND

Case 2 (loss of module GND): when the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

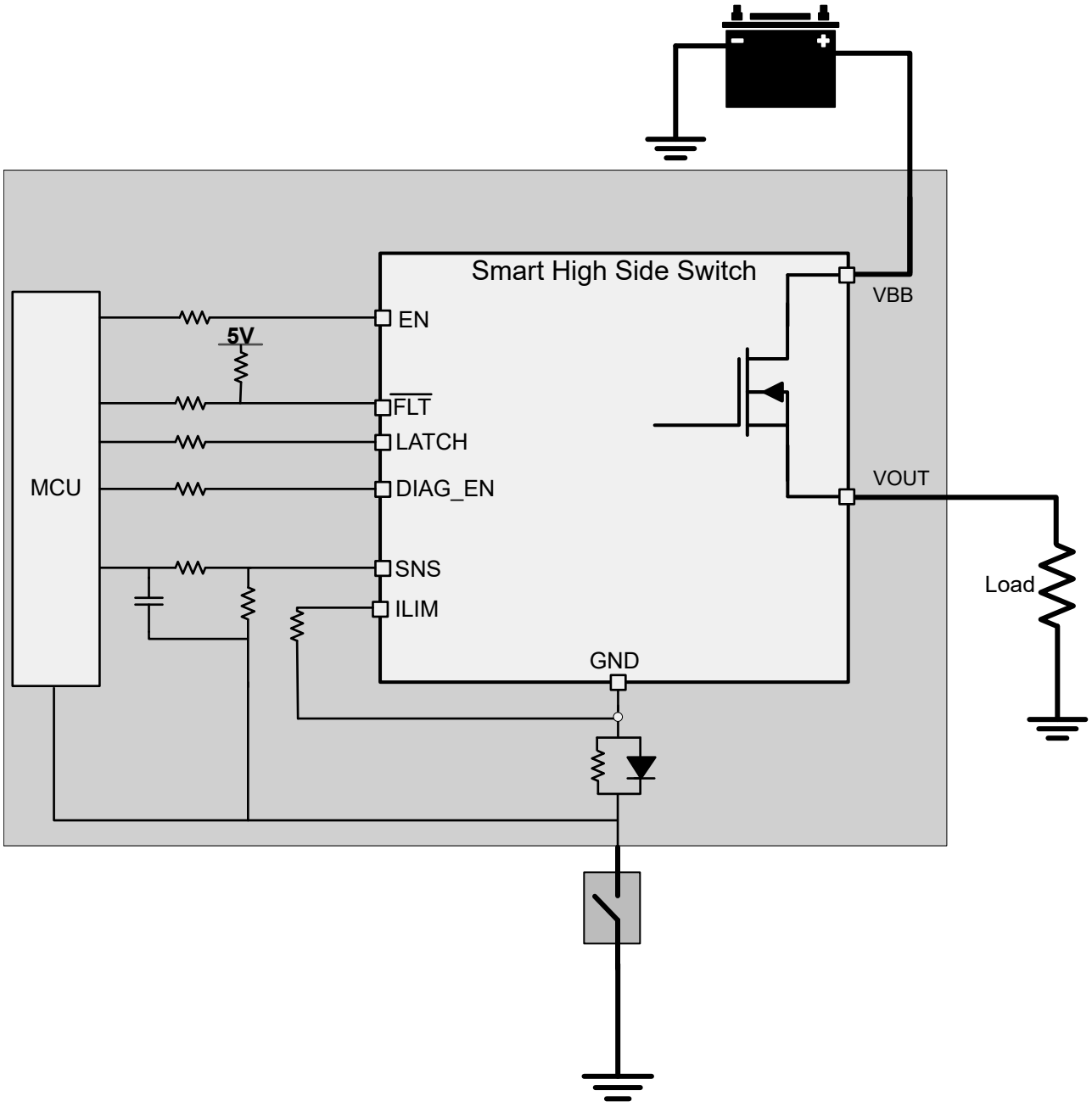


図 7-18. Loss of Module GND

7.3.4.9 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

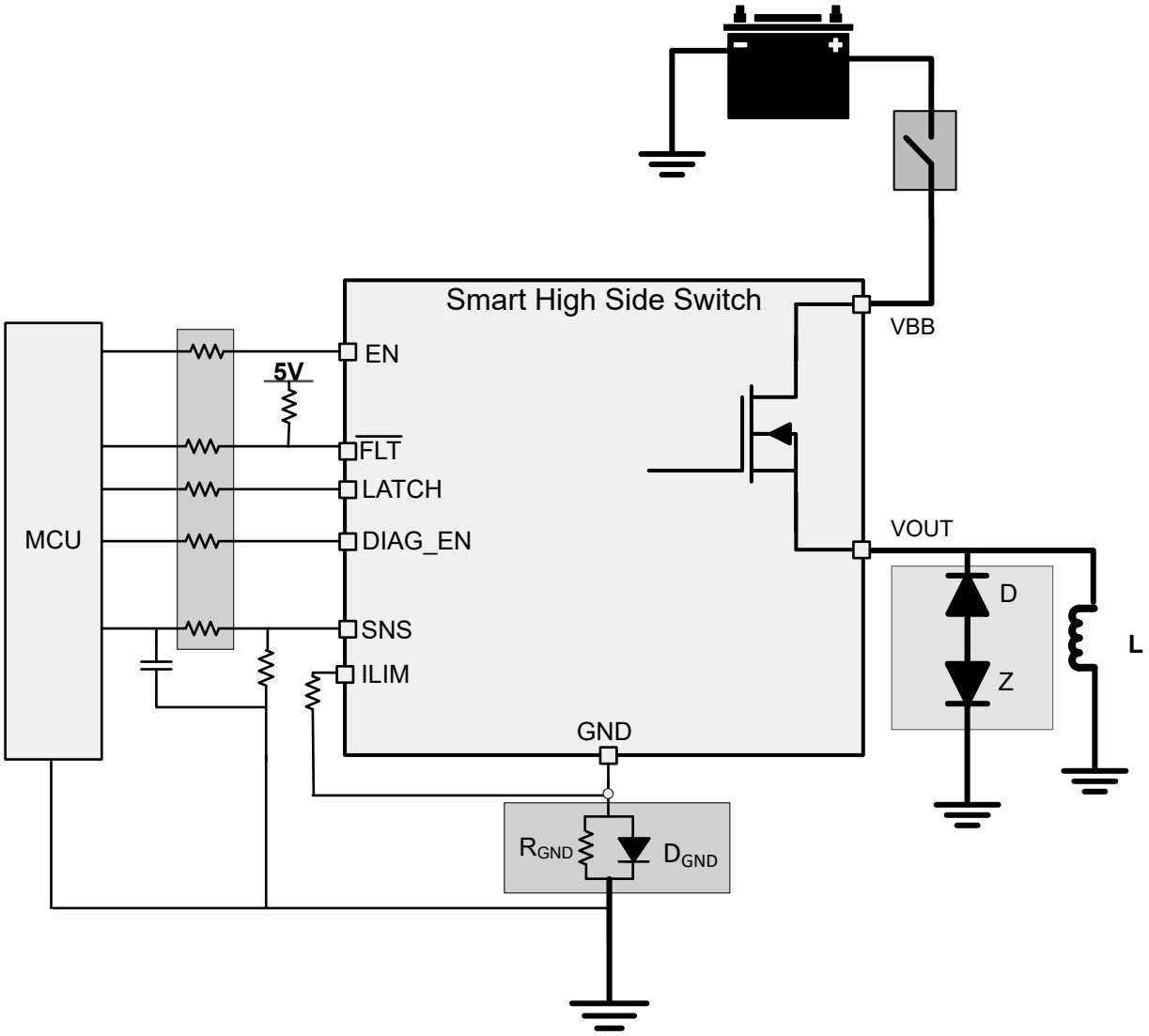


図 7-19. Loss of Battery

7.3.4.10 Reverse Current Protection

Method 1: block diode connected with V_{BB}. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

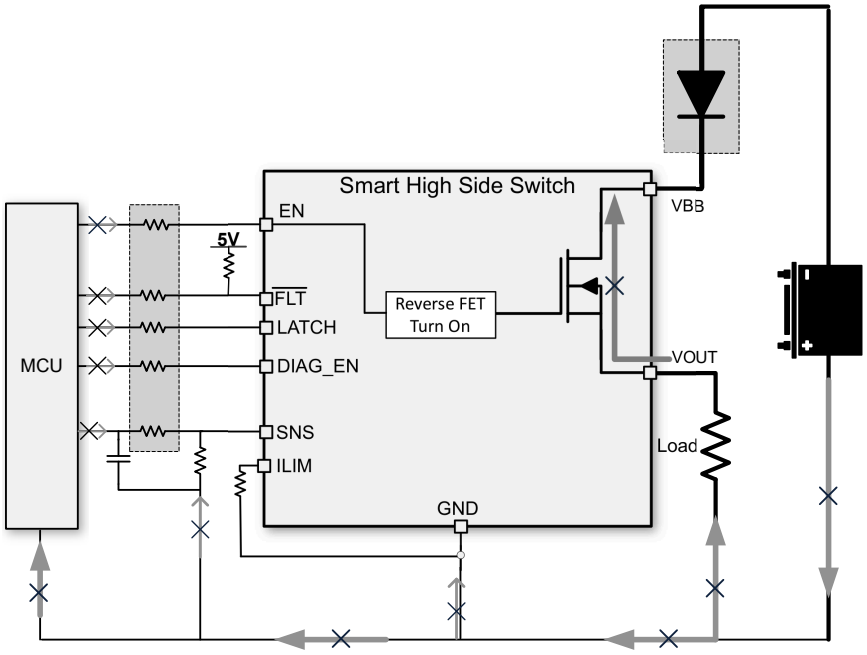


図 7-20. Reverse Protection With Block Diode

Method 2 (GND network protection): only the high-side device is protected under this connection. The load reverse current is limited by the impedance of the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET must not make the heat build up be greater than the absolute maximum junction temperature. This can be calculated using the $R_{ON(REV)}$ value and the $R_{\theta JA}$ specification. In the reverse battery condition it is important that the FET comes on to lower the power dissipation. This action is achieved through the path from EN to system ground where the positive voltage is being applied. No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Connect the current limit programmable resistor to the device GND.

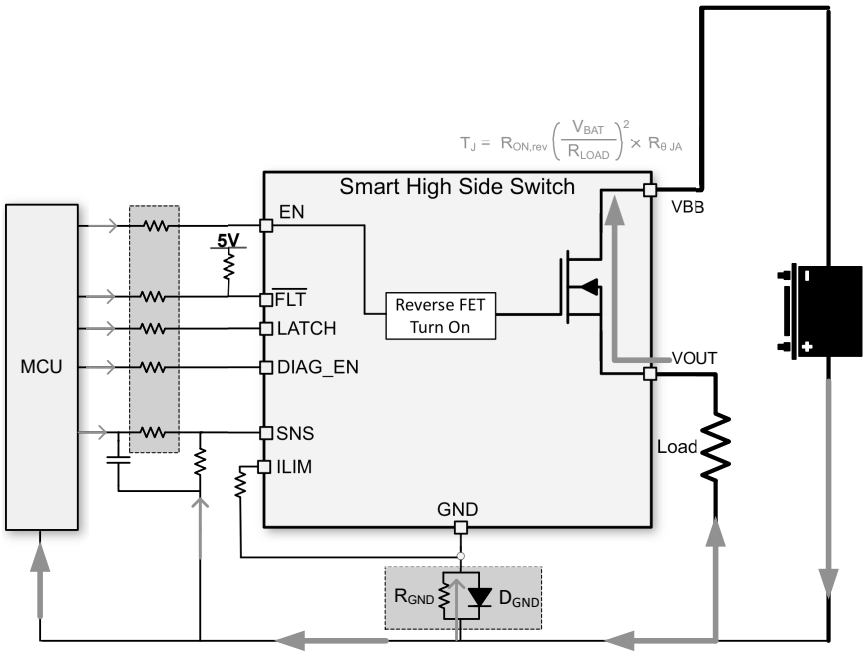


図 7-21. Reverse Protection With GND Network

- **Recommendation – resistor and diode in parallel:** a peak negative spike can occur when the inductive load is switching off, which can damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are a 1-kΩ resistor in parallel with an I_F > 100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

  If multiple high-side power switches are used, the resistor can be shared among devices.
- **Ground Resistor:** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses.

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \tag{11}$$

  where

  – $-V_{CC}$ is the maximum reverse battery voltage (typically –16 V).
  – $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*.
- **Ground Diode:** A diode is needed to block the reverse voltage, which also brings a ground shift (≈ 600 mV). Additionally, the diode must be ≈ 200-V reverse voltage for the ISO 7637 pulse 1 testing so that it does not get biased.

7.3.4.11 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin can damage the MCU I/O pins (more likely, the internal circuitry connected to the pins). Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 5-kΩ resistance for the R_{PROT} resistors.

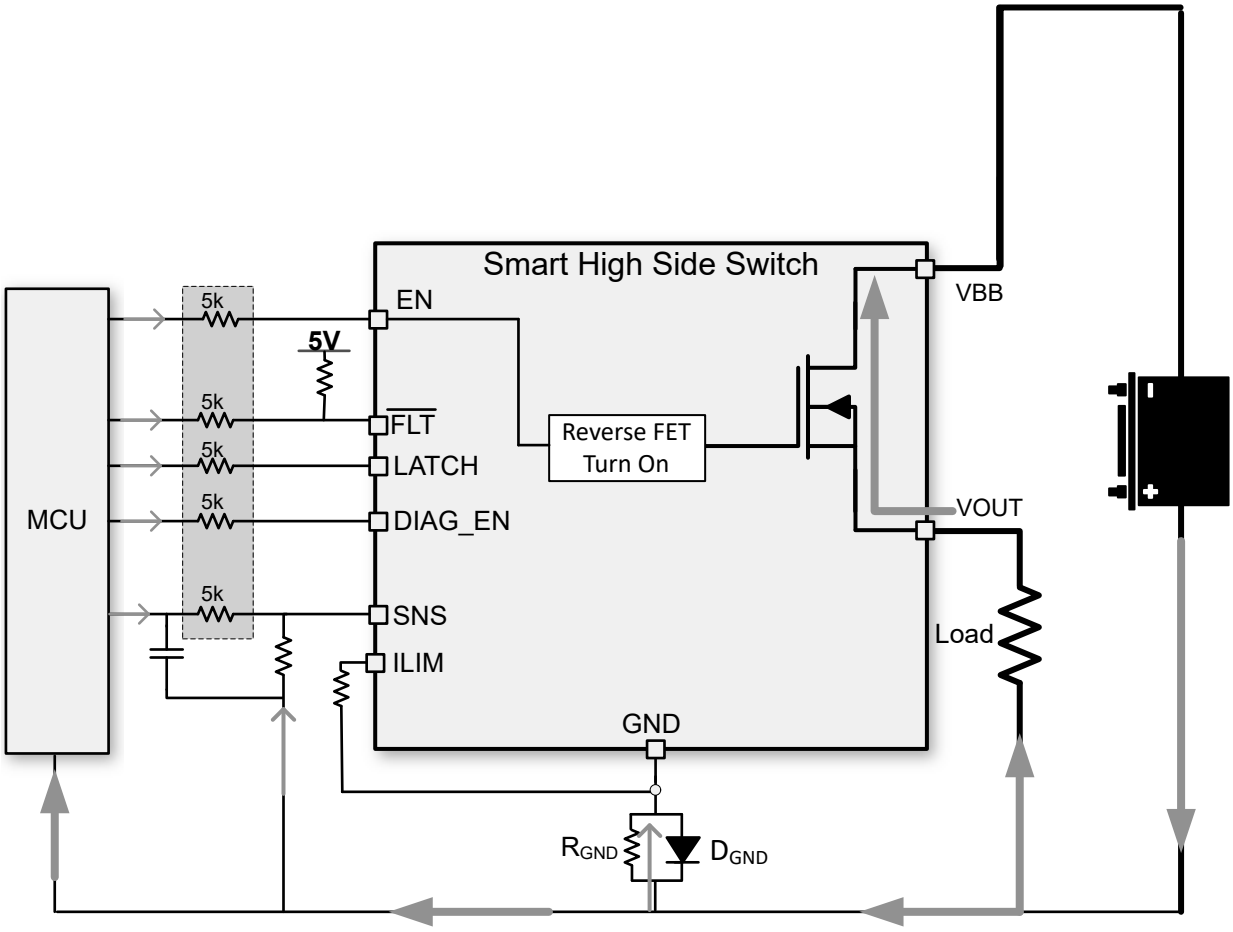


図 7-22. MCU I/O Protections

7.3.5 Diagnostic Enable Function

The diagnostic enable pin, DIAG_EN, offers multiplexing of the microcontroller diagnostic input for current sense or digital status, by sharing the same sense resistor and ADC line or I/O port among multiple devices.

In addition, during the output-off period, the diagnostic disable function lowers the current consumption for the standby condition. The three working modes in the device are normal mode (I_Q), standby mode (I_{STBY}), and standby mode with diagnostic (I_{DIA}). If off-state power saving is required in the system, the standby current is < 500 nA with DIAG_EN low. If the off-state diagnostic is required in the system, the typical standby current is around 1 mA with DIAG_EN high.

7.4 Device Functional Modes

7.4.1 Working Mode

The three working modes in the device are normal mode, standby mode, and standby mode with diagnostic. If an off-state power saving is required in the system, the standby current is less than 500 nA with EN and DIAG_EN low. If an off-state diagnostic is required in the system, the typical standby current is around 1.2 mA

with DIAG_EN high. Note that to enter standby mode requires IN low and t > t_{STBY}. t_{STBY} is the standby-mode deglitch time, which is used to avoid false triggering or interfere with PWM switching. 図 7-23 shows a work-mode state-machine state diagram.

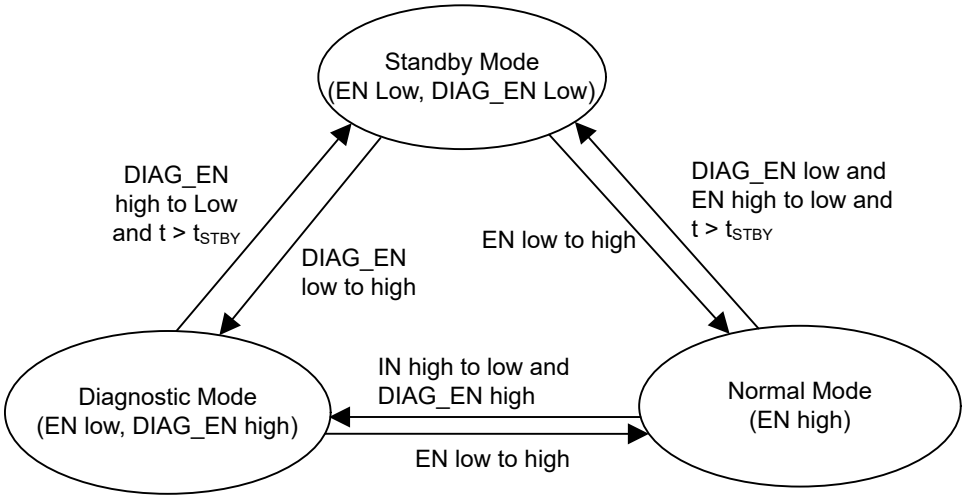


図 7-23. Work-Mode State Machine

8 Application and Implementation

注

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8.1 Application Information

The following discussion notes how to implement the device to distinguish the different fault modes and implement a transient-pulse immunity test.

In some applications, open load, short-to-battery, and short to GND must be distinguished from each other. This action requires two steps.

8.2 Typical Application

図 8-1 shows an example of how to design the external circuitry parameters.

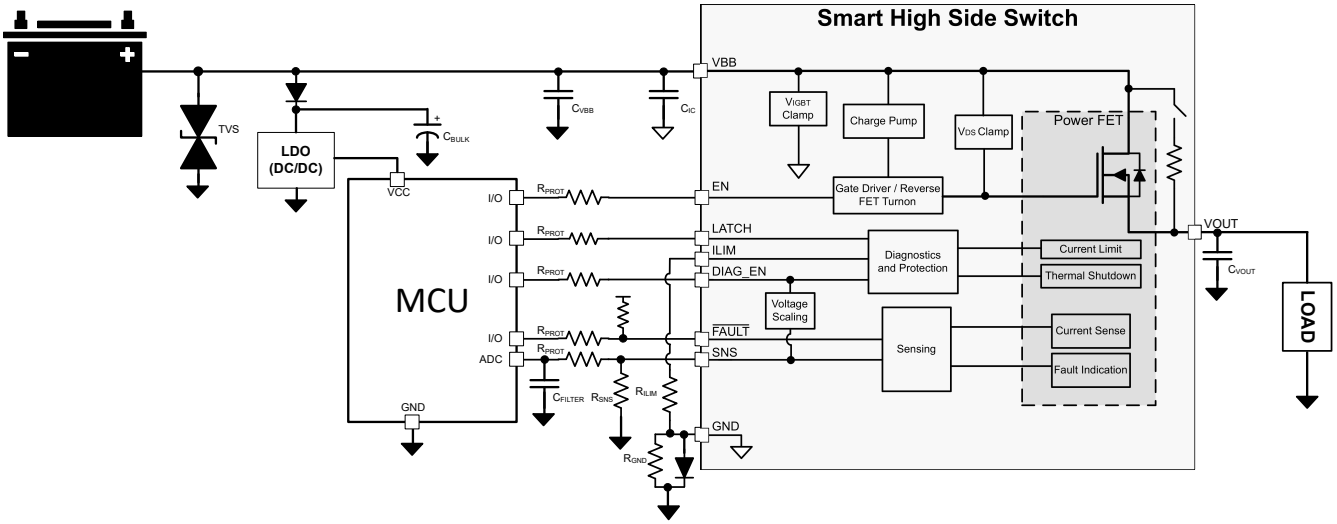

図 8-1. Typical Application Circuitry

8.2.1 Design Requirements

Component	Description	Purpose
TVS	SMBJ39CA (optional)	Filter voltage transients coming from battery (ISO7637-2)
CVBB	220 nF (optional)	Better EMI performance
	100 nF, 1 nF (optional)	Further optimizes EMI performance
CIC	100 nF	Minimal amount of capacitance on input for EMI mitigation
CBULK	10 uF (optional)	There to hold the rail for the LDO; however, helps to filter voltage transients on supply rail. Not a requirement.
RPROT	5 kΩ	Protection resistor for microcontroller and device I/O pins
RILIM	7 kΩ – 70 kΩ	Set current limit threshold
RSNS	1kΩ	Translate the sense current into sense voltage.
CFILTER	100 nF	Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU
CVOUT	22 nF	Improves EMI performance, filtering of voltage transients
	1 nF, 1 nF (optional)	Further optimizes EMI performance
RGND	1 kΩ	Stabilize GND potential during turn-off of inductive load
DGND	BAS21 Diode	Keeps GND close to system ground during normal operation

8.2.2 Detailed Design Procedure

To keep maximum voltage on the SNS pin at an acceptable range for the system, calculate the R_{SNS} as in 式 1. To achieve better current sense accuracy. A 1% accuracy or better resistor is preferred.

$$(V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \leq R_{SNS} \leq V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \quad (12)$$

表 8-1. Typical Application

Parameter	Value
V_{DIAG_EN}	5 V
$I_{LOAD,max}$	2 A
$I_{LOAD,min}$	5 mA
$V_{ADC,min}$	5 mV
V_{HR}	1 V

For this application, an RSNS value of approximately 1 kΩ can be chosen to satisfy the equation requirements.

$$(5\ V - 1\ V) \times 1040 / 4\ A \leq \approx 1\ k\Omega \leq 5\ mV \times 1040 / 5\ mA \quad (13)$$

In other applications, more emphasis can be put on the lower end measurable values, which can increase RSNS. Likewise if the higher currents are of more interest the R_{SNS} can be decreased. Note that the maximum current that can be measured without saturation is 6 A.

Having the maximum SNS voltage scale with the DIAG_EN voltage removes the need for a Zener diode on the SNS pin going to the ADC.

The current limit must be set to an acceptable level, so with the KCL tolerances, the current limit of 4A is chosen. To set the programmable current limit value at 4 A , calculate the R_{LIM} as in Equation 12.

$$R_{LIM} = K_{CL} / I_{LIM} = 45 / 4 = 11.25\ k\Omega \quad (14)$$

For a more accurate current limit estimation with the error tolerances of KCL see the Current Limit Accuracy section and use the graph to estimate the error at each desired current limit value.

TI recommends R_{PROT} = 5 kΩ to ensure the current going into the digital pins (EN, DIAG_EN, LATCH) is limited.

TI recommends a 1-kΩ resistor and 200-V, 0.2-A diode (BAS21 for example) for the GND network.

8.2.2.1 Dynamically Changing Current Limit

The current limit threshold is able to be changed dynamically by altering the resistance going from the current limit pin to the ground of the device on the fly. This alteration allows the system to have a different current limit for start-up, when there can be significant inrush current, and during normal operation. The way this is commonly done is by putting two resistors in parallel on the ILIM pin and having a switch to enable or disable one of the resistors. This set-up can be seen in the figure below. Alternatively, a digital potentiometer can be used to adjust the impedance on the ILIM pin on the fly. Care must be taken so that the capacitance on the ILIM pin is below approximately 100 pF because it can cause the current regulation loop to become unstable. The most common application where this feature is useful is capacitive loads.

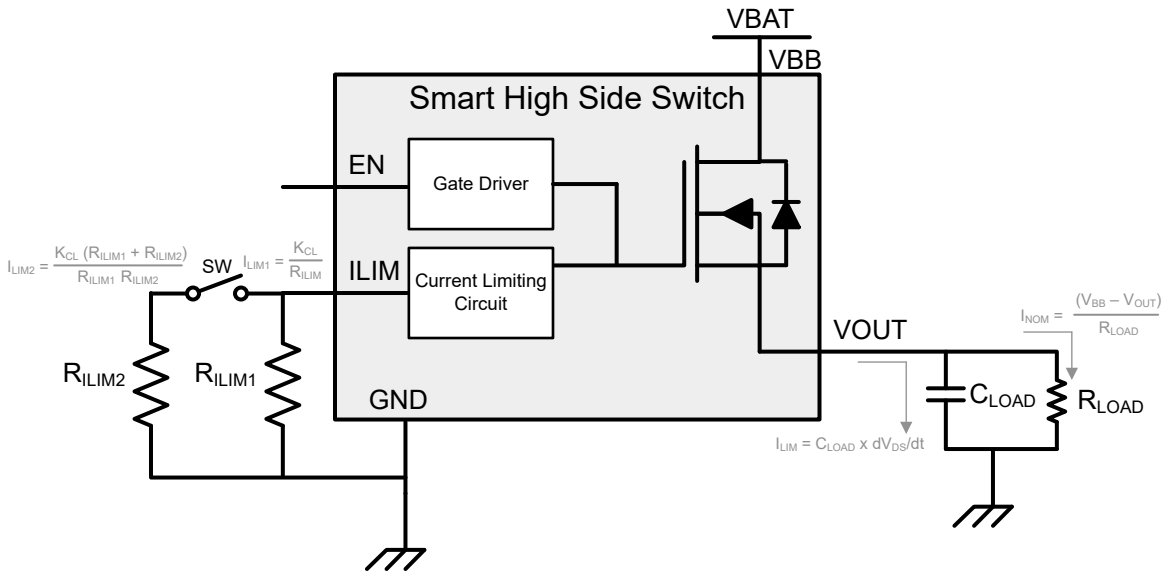

図 8-2. Dynamic Changing Current Limit Setup

In a capacitive charging case, the initial current to charge the capacitor is the inrush current. Depending on the system requirements, dynamically changing the current limit can help either charge up a capacitor faster or charge up a larger capacitor. To allow a higher inrush level of current through in the beginning, the switch can be closed making the current limit be according to the equation below.

$$I_{LIM2} = K_{CL}(R_{ILIM1} + R_{ILIM2}) / (R_{ILIM1} \times R_{ILIM2}) \quad (15)$$

When the inrush event is over and the output voltage is charged up, the switch opens and the current limit is just the R_{ILIM1} equivalent level. This timing can be seen in the figure below.

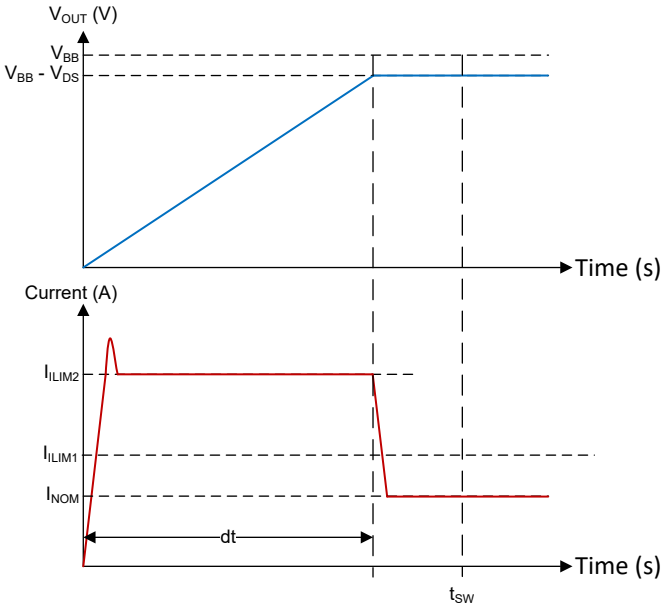

図 8-3. Capacitive Charging Changing Current Limit

Alternatively, if the switch is open, the current limit starts out at a lower value and then the switch can be closed when the capacitance gets charged up. This lower current limit level allows higher value capacitance's to be charged up. The timing diagram can be seen below.

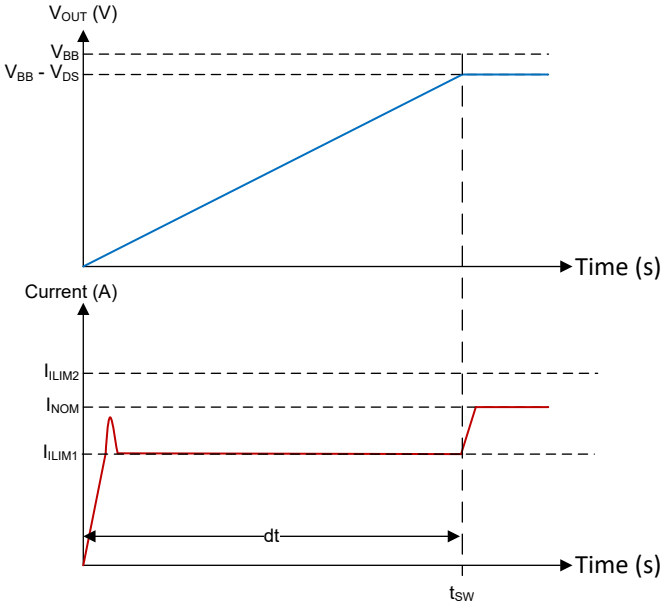

図 8-4. Large Capacitive Charging Changing Current Limit

8.2.2.2 AEC Q100-012 Test Grade A Certification

Short-circuit reliability is critical for smart high-side power switch devices. The AEC-Q100-012 standard is used to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short-to-GND certification.

Three test modes are defined in the AEC Q100-012 standard. See 表 8-2 for cold repetitive short-circuit test – long pulse, cold repetitive short-circuit test – short pulse, and hot repetitive short-circuit test.

表 8-2. Tests

Test Items	Test Condition	Test Cycles
Cold repetitive short-circuit test – short pulse	–40°C, 10-ms pulse, cool down	1M
Cold repetitive short-circuit test – long pulse	–40°C, 300-ms pulse, cool down	1M
Hot repetitive short-circuit test	25°C, continuous short	1000 hr

Different grade levels are specified according to the pass cycles. The TPS1HC100-Q1device gets the certification of Grade A level, 1 million short-to-GND cycles, which is the highest test standard in the market.

表 8-3. Grade Levels

Grade	Number of Cycles	Lots,Samples Per Lot	Number of Fails
A	> 1000000	3, 10	0
B	> 300000 to 1000000	3, 10	0
C	> 100000 to 300000	3, 10	0
D	> 30000 to 100000	3, 10	0
E	> 10000 to 30000	3, 10	0
F	> 3000 to 10000	3, 10	0
G	> 1000 to 3000	3, 10	0
H	300 to 1000	3, 10	0
O	< 300	3, 10	0

8.2.2.3 EMC Transient Disturbances Test

Due to the severe electrical conditions in the automotive environment, immunity capacity against electrical transient disturbances is required, especially for a high-side power switch, which is connected directly to the battery. Detailed test requirements are in accordance with the ISO 7637-2:2011 and ISO 16750-2:2010 standards. The TPS1HC100-Q1 device is tested and certificated by a third-party organization.

表 8-4. ISO 7637-2:2011(E) in 12-V System (1) (2) (3) (4)

Test Item	Test Pulse Severity Level and vs Accordingly		Pulse Duration (t_d)	Minimum Number of Pulses or Test Time	Burst-Cycle Pulse-Repetition Time		Input Resistance (Ω)	Function Performance Status Classification
	Level	Vs/V			MIN	MAX		
1	III	–112	2 ms	500 pulses	0.5 s	e s	10	Status II
2a	III	55	50 µs	500 pulses	0.2 s	5 s	2	Status II
2b	IV	10	0.2 to 2 s	10 pulses	0.5 s	5 s	0 to 0.05	Status II
3a	IV	–220	0.1 µs	1h	90 ms	100 ms	50	Status II
3b	IV	150	0.1 µs	1h	90 ms	100 ms	50	Status II

(1) Tested both under input low condition and high condition.
(2) Considering the worst test condition, it is tested without any filter capacitors in V_{BB} and V_{OUT}
(3) GND pin network is a 1-kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: the function does not perform as designed during the test, but returns automatically to normal operation after the test.

表 8-5. ISO 16750-2:2010(E) Load Dump Test B in 12-V System (1) (2) (3) (4) (5)

Test Item	Test Pulse Severity Level and vs Accordingly		Pulse Duration (t_d)	Minimum Number of Pulses or Test Time	Burst- Cycle Pulse-Repetition Time		Input Resistance (Ω)	Function Performance Status Classification
	Level	Vs/V			MIN (s)	MAX (s)		
Test B		35	40 to 400 ms	5 pulses	60	e	0.5 to 4	Status II

(1) Tested both under input low condition and high condition (DIAG_EN, EN, and VBB are all classified as inputs).
(2) Considering the worst test condition, the device is tested without any filter capacitors on VBB and VOUT.
(3) The GND pin network is a 1-kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: the function does not perform as designed during the test, but returns automatically to normal operation after the test.

(5) Select a 39-V external suppressor.

8.2.3 Application Curves

図 8-5 shows a test example of charging a 470-µF capacitor. Test conditions: V_{BB} = 13.5 V, input is from low to high, load is a 470-µF capacitive load, ILIM pin is shorted to GND. CH4 is the output current. CH3 is the input step. CH2 is the output voltage, VOUT. CH1 is the supply voltage, VBB

図 8-6 shows a test example of a enable into short-circuit inrush current limit. Test conditions: V_{BB}= 13.5 V, input is low to high, load is 5 µH + 100 mΩ, ILIM pin is shorted to GND. CH4 is the output current. CH3 is the input step. CH2 is the output voltage, VOUT. CH1 is the supply voltage, VBB

図 8-7 shows a test example of a load step from 500 mA to 3 A back to 500 mA. Test conditions: V_{BB}= 13.5 V, input is high, load is 6.75 Ω and then changed to 4.5 Ω then back to 6.75 Ω, ILIM pin is shorted to GND. CH4 is the output current. CH3 is the SNS pin. CH2 is the output voltage, VOUT. CH1 is the supply voltage, VBB

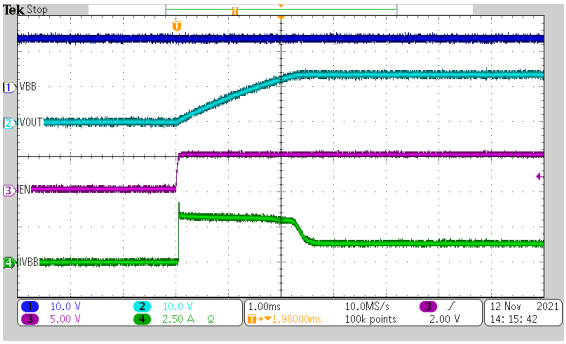

図 8-5. Charging a 470-µF Capacitor

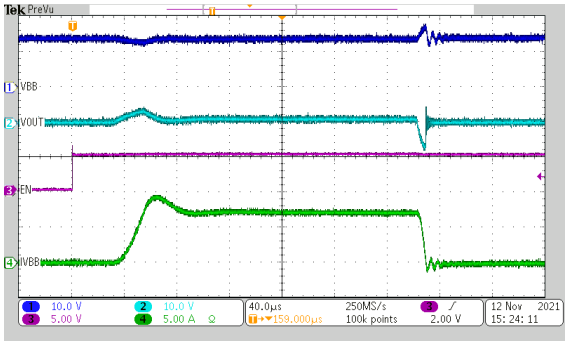

図 8-6. Enable into Short Circuit

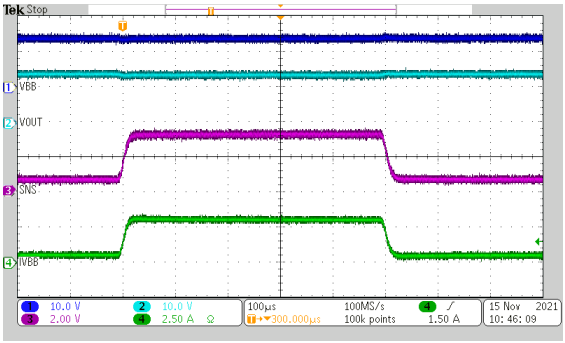

図 8-7. Load Step

8.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system. The supply voltage must be within the range specified in the *Recommended Operating Conditions*.

VBB Voltage Range	Note
3 V to 6 V	Extended lower 12-V automotive battery operation such as cold crank and start-stop. Device is fully functional but current sense and current limit accuracies do not apply as well as timing parametrics can deviate from specification.
6 V to 18 V	Nominal 12-V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.
18 V to 28 V	Extended upper 12-V automotive battery operation such as double battery. Device is fully functional and protected but timing parametrics can deviate from specifications

VBB Voltage Range	Note
35 V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

8.4 Layout

8.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation can be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- Plate shut or plug and cap all thermal vias on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage must be at least 85%.

8.4.2 Layout Example

8.4.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

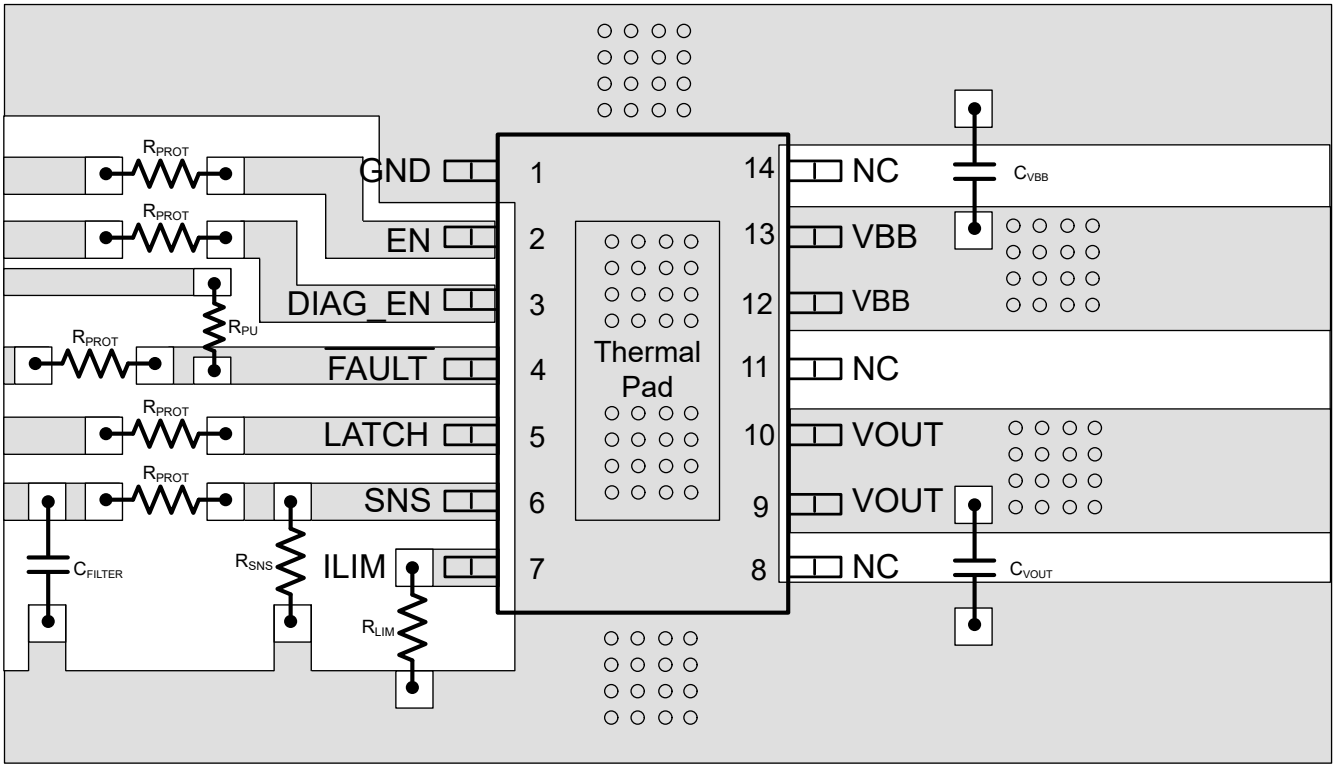

図 8-8. Layout Without a GND Network

8.4.2.2 With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

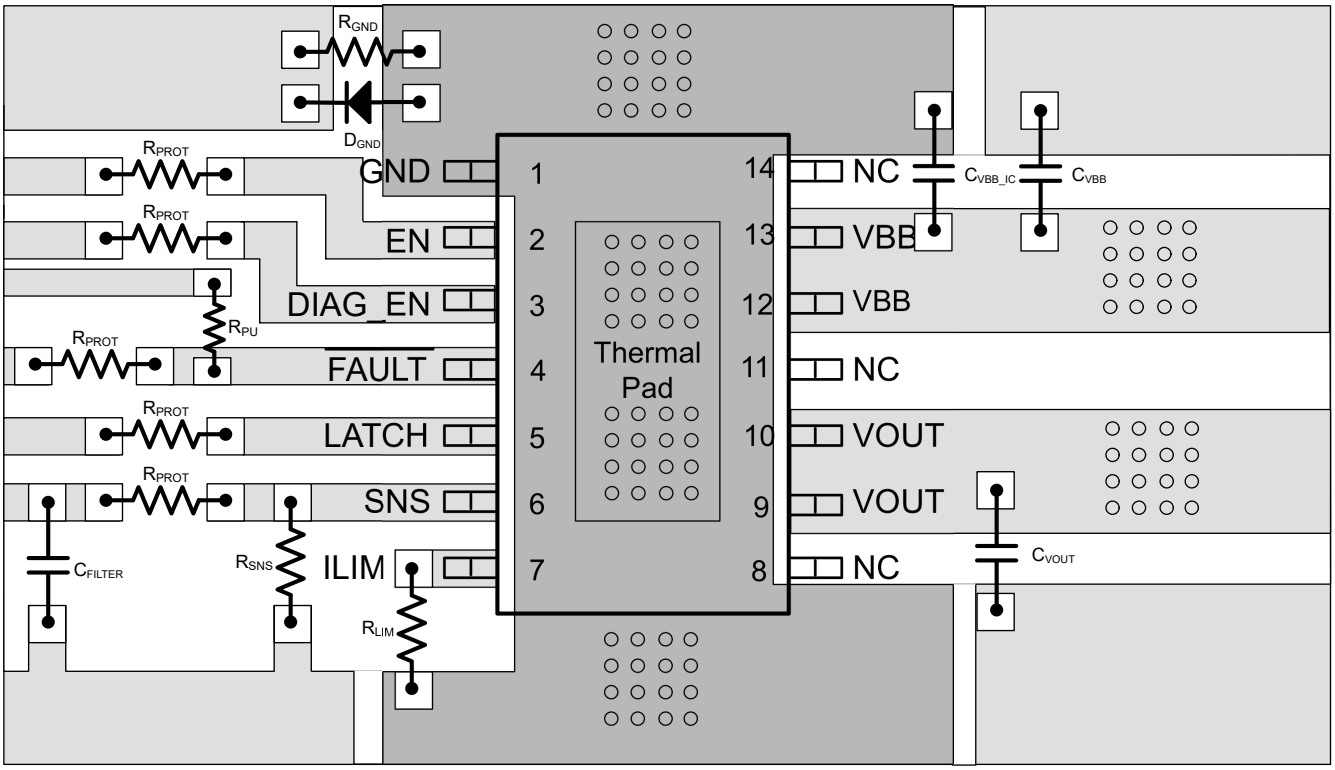

図 8-9. Layout With a GND Network

8.4.3 Thermal Considerations

This device possesses thermal shutdown (T_{ABS}) circuitry as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal shutdown hysteresis, the output turns on again.

Calculate the power dissipated by the device according to Equation 13.

$$P_T = I_{OUT}{}^2 \times R_{DSON} + V_{BB} \times I_Q \quad (16)$$

where

- P_T = total power dissipation of the device

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (17)$$

For more information, please see the *How to Drive Resistive, Inductive, Capacitive, and Lighting Loads* application note.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *How to Drive Resistive, Inductive, Capacitive, and Lighting Loads* application note

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2021) to Revision B (February 2025)	Page
• Added VBB ≥ 5V to the I_{SNSI} parameter test conditions in the *Electric Characteristics* section	6
• Updated "Current-Sense Accuracy" figure in the *Accurate Current Sense* section	21
• Updated "Diagnostic Enable Logic Table" in the *Full Protection and Diagnostics* section	28
• Added line item for clarification to CVBB and CVOUT components in the *Design Requirements* section	43

Changes from Revision * (July 2021) to Revision A (December 2021)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS1HC100BQPWPRQ1	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1HC100Q
TPS1HC100BQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1HC100Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

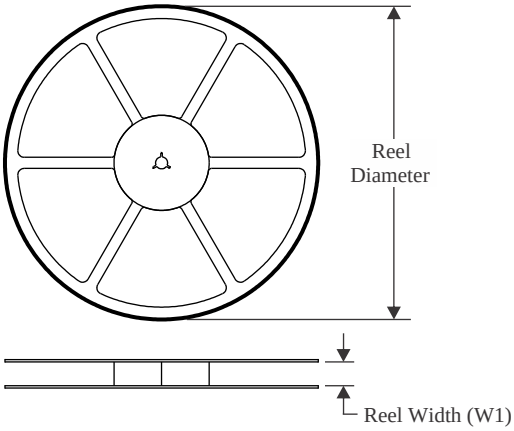
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

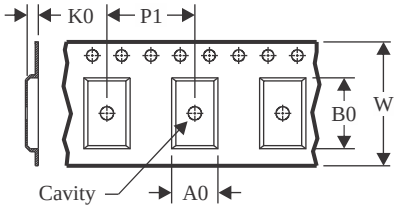
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

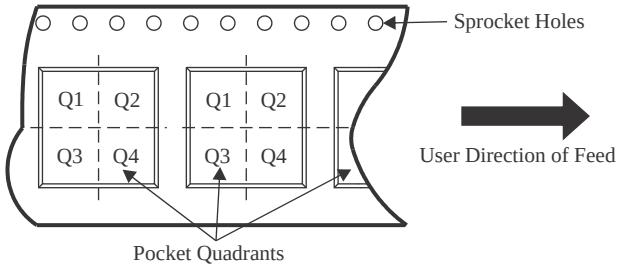


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

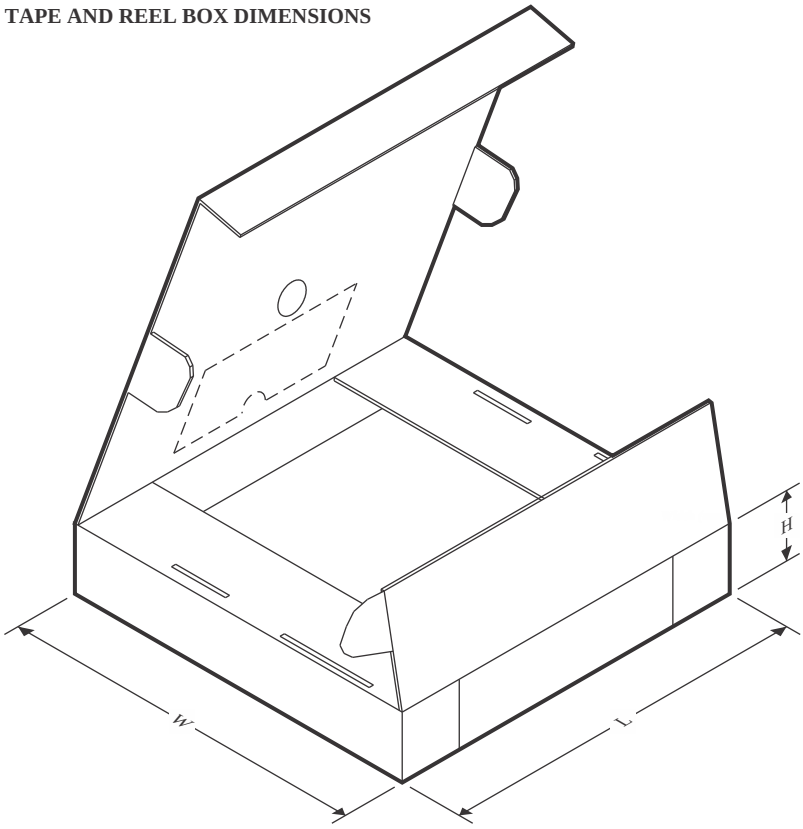
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1HC100BQPWPRQ1	HTSSOP	PWP	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1HC100BQPWPRQ1	HTSSOP	PWP	14	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

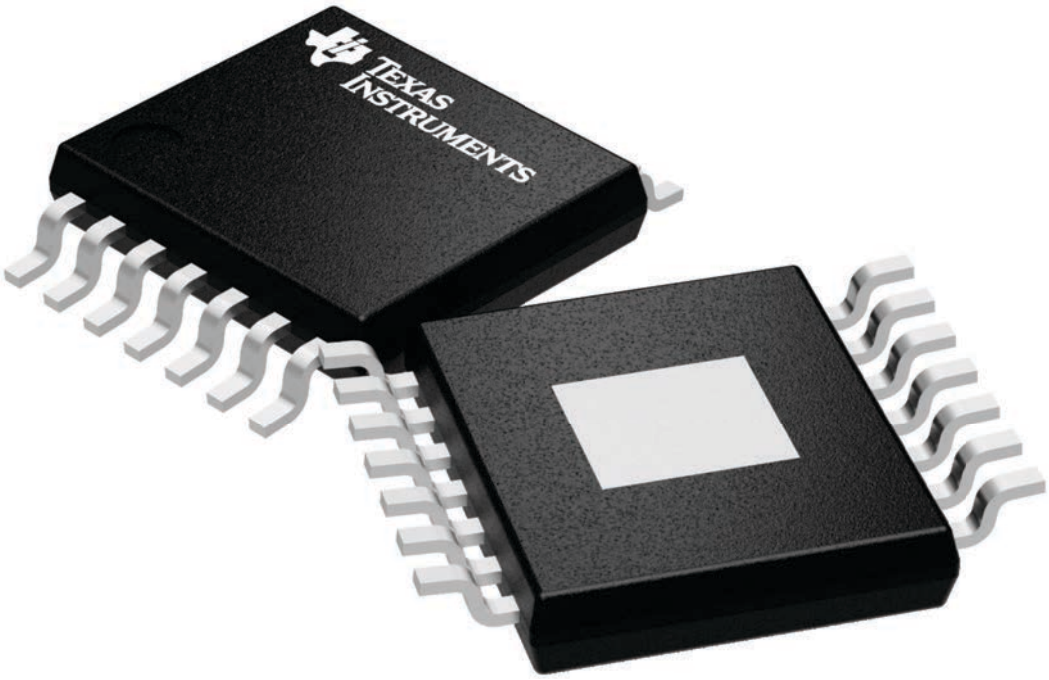
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



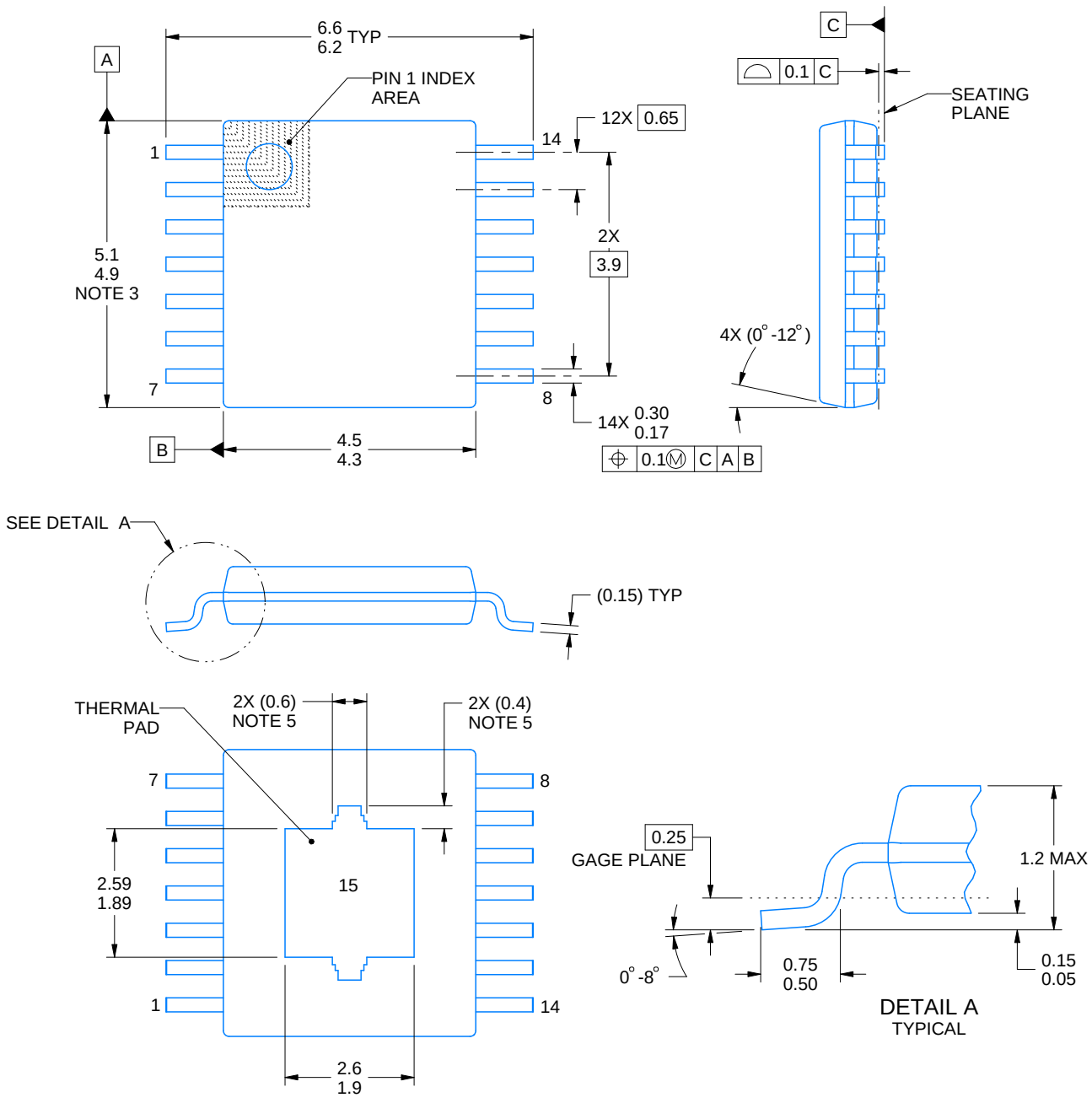
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

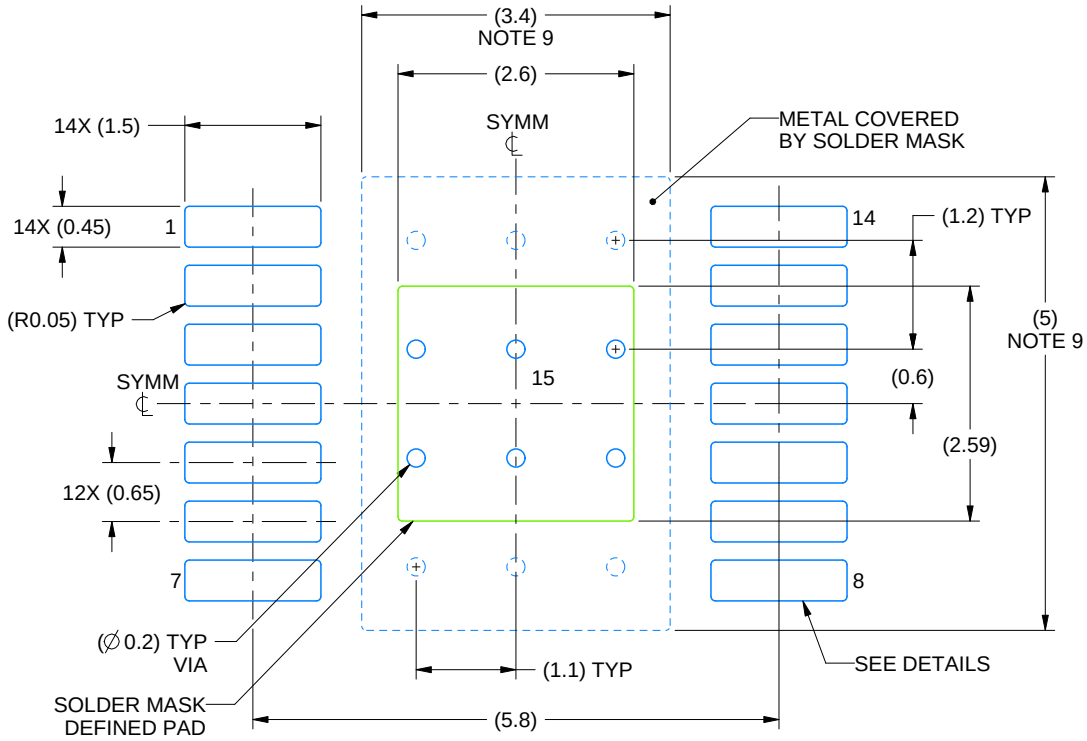
SMALL OUTLINE PACKAGE



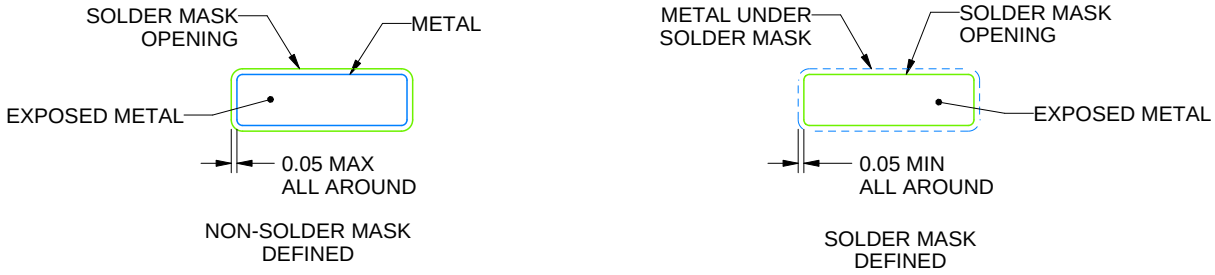
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

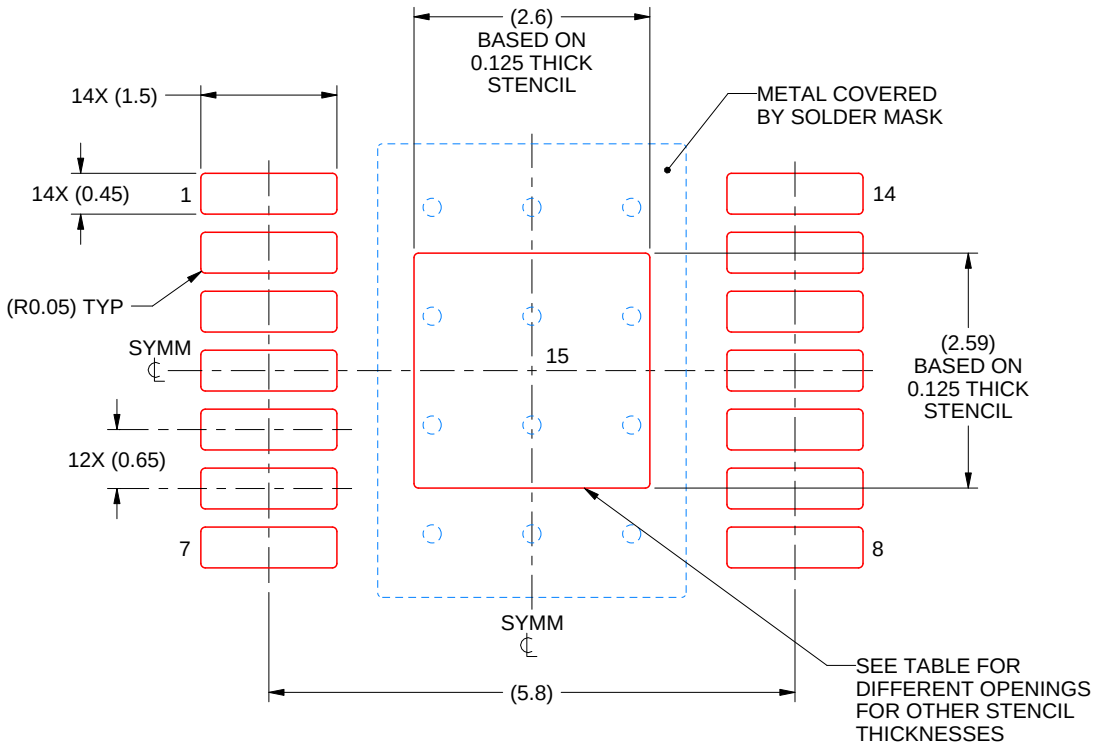


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月