TPS22810-Q1 2.7～18V、79mΩオン抵抗、熱保護付き負荷スイッチ

1 特長

- **車載アプリケーションに対応**
- **下記内容でAEC-Q100認定済み：**
  – デバイス温度グレード2: 動作時周囲温度 -40℃～+105℃
  – デバイスHBM ESD分類レベル2
  – デバイスCDM ESD分類レベルC5
- **シングル・チャネル負荷スイッチを内蔵**
- **最大連続電流**: 2A
- **入力電圧**: 2.7V～18V
- **絶対最大入力電圧**: 20V
- **オン抵抗**(R_{ON})
  – V_{IN} = 12VでR_{ON} = 79mΩ (標準値)
- **静止電流**
  – V_{IN} = 12Vで62µA (標準値)
- **シャットダウン電流**
  – V_{IN} = 12Vで500nA (標準値)
- **サーマル・シャットダウン**
- **低電圧誤動作防止**(UVLO)
- **可変クイック出力放電**(QOD)
- CT**ピンで立ち上がり時間を設定可能**
- SOT23-6**パッケージ**
  – 2.9mm×2.8mm、0.95mmピッチ、高さ1.45mm (DBV)

2 アプリケーション

- **車載用ヘッド・ユニット**
- **サラウンド・ビュー**ECU

3 概要

TPS22810-Q1はシングル・チャネルの負荷スイッチで、立ち上がり時間を設定可能、クイック出力放電(QOD)が内蔵されています。このデバイスにはサーマル・シャットダウン機能があり、接合部の高温からデバイスを保護するため、デバイスの安全動作領域が本質的に維持されます。このデバイスにはNチャネルMOSFETが搭載され、2.7V～18Vの入力電圧範囲で動作でき、最大で2Aの電流をサポートできます。スイッチはオン/オフ入力により制御され、低電圧の制御信号と直接接続が可能です。

デバイスの立ち上がり時間を設定可能なため、大きな負荷容量により発生する突入電流が大幅に減少し、電源ドループが低減、または生じなくなります。低電圧誤動作防止機能は、VIN電圧がスレッショルド値よりも低下した場合にデバイスの電源をオフにし、想定よりも低い電圧の供給によって下流の回路が損害を受けることを防止します。QODピンは設定可能で、デバイスの立ち下がり時間を制御し、電源オフ時の設計を柔軟に行えるようにします。

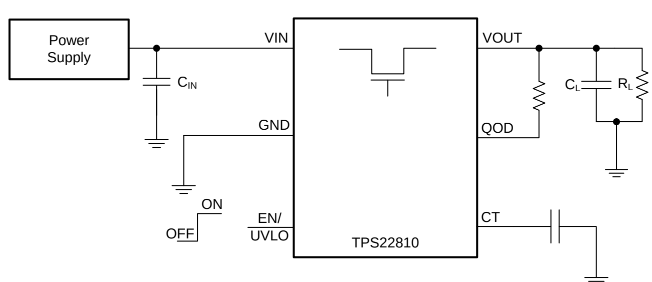
TPS22810-Q1はリード付きSOT-23パッケージ(DBV)で供給されるため、ハンダ接合部の目視検査が可能です。このデバイスは、-40℃～+105℃の周囲温度範囲で動作するよう規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS22810-Q1	SOT-23 (6)	2.90mm×2.80mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



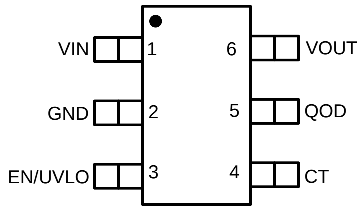
目次

4 改訂履歴

日付	改訂内容	注
2018年 4月	*	初版

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	4	O	Switch slew rate control. Can be left floating
EN/UVLO	3	I	Active high switch control input and UVLO adjustment. Do not leave floating
GND	2	—	Device ground
QOD	5	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways: • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Quick Output Discharge (QOD)* for more information
VIN	1	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND
VOUT	6	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	VIN	–0.3	20	V
V_{OUT}	Maximum Output Voltage Range	VOUT	–0.3	min (20V, V_{IN} + 0.3)	
$V_{EN/UVLO}$	Maximum Enable Pin Voltage Range	EN/UVLO	–0.3	20	V
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]		±3000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (VIN, VOUT, EN/UVLO, and CT)	±750	
			Other pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	2.7	18	V
V_{OUT}	Output Voltage Range	OUT		V_{IN}	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO	0	18	V
IMAX	Maximum continuous switch current, TA = 65°C	IN to OUT		2	A
IMAX	Maximum continuous switch current, TA = 85°C	IN to OUT		1.5	A
IMAX	Maximum continuous switch current, TA = 105°C	IN to OUT		1	A
T_A	Operating free-air temperature		–40	105	°C
C_{IN}	Input Capacitor[(1)]		1		µF

(1) See the Detailed Description section.

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS22810-Q1 DBV (SOT23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature–40°C ≤T_A ≤ +105°C. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{Q,\ VIN}$	Quiescent current	I_{OUT} = 0 A	V_{IN} = 18 V	T_A = –40°C to +85°C		62	80	µA
				T_A = –40°C to +105°C			85	
			V_{IN} = 12 V	T_A = –40°C to +85°C		62	80	
				T_A = –40°C to +105°C			85	
			V_{IN} = 5 V	T_A = –40°C to +85°C		59	80	
				T_A = –40°C to +105°C			85	
			V_{IN} = 3.3 V	T_A = –40°C to +85°C		53	80	
				T_A = –40°C to +105°C			85	
			V_{IN} = 2.7 V	T_A = –40°C to +85°C		49	70	
				T_A = –40°C to +105°C			85	
$I_{SD,\ VIN}$	Shutdown current	V_{EN} = 0 V, V_{OUT} = 0 V	V_{IN} = 18 V	T_A = –40°C to +85°C		0.5	2.3	µA
				T_A = –40°C to +105°C			3.8	
			V_{IN} = 12 V	T_A = –40°C to +85°C		0.5	2.3	
				T_A = –40°C to +105°C			3.8	
			V_{IN} = 5 V	T_A = –40°C to +85°C		0.5	2.3	
				T_A = –40°C to +105°C			3.8	
			V_{IN} = 3.3 V	T_A = –40°C to +85°C		0.5	2.3	
				T_A = –40°C to +105°C			3.8	
			V_{IN} = 2.7 V	T_A = –40°C to +85°C		0.5	2.3	
				T_A = –40°C to +105°C			3.8	
$I_{EN/UVLO}$	EN/UVLO pin input leakage current	V_{IN} = 18 V, I_{OUT} = 0 A		T_A = –40°C to +105°C			0.1	µA
V_{UVR}	VIN UVLO threshold, rising			T_A = –40°C to +105°C	2	2.54	2.62	V
$V_{UVRhyst}$	VIN UVLO hysterisis			T_A = –40°C to +105°C		5		%
V_{ENR}	EN threshold, rising			T_A = –40°C to +105°C	1.13	1.23	1.3	V
V_{ENF}	EN threshold, falling			T_A = –40°C to +105°C	1.08	1.13	1.18	V
V_{SHUTF}	EN threshold voltage for low I_Q shutdown			T_A = –40°C to +105°C	0.5	0.75	0.9	V
R_{ON}	On-resistance	V_{IN} = 18 V, I_{OUT} = –200 mA		T_A = 25°C		79	86	mΩ
				T_A = –40°C to +85°C			105	
				T_A = –40°C to +105°C			115	
		V_{IN} = 12 V, I_{OUT} = –200 mA		T_A = 25°C		79	86	
				T_A = –40°C to +85°C			105	
				T_A = –40°C to +105°C			115	
		V_{IN} = 9 V, I_{OUT} = –200 mA		T_A = 25°C		79	86	
				T_A = –40°C to +85°C			105	
				T_A = –40°C to +105°C			115	
		V_{IN} = 5 V, I_{OUT} = –200 mA		T_A = 25°C		79	86	
				T_A = –40°C to +85°C			105	
				T_A = –40°C to +105°C			115	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA		T_A = 25°C		83	92	
				T_A = –40°C to +85°C			115	
				T_A = –40°C to +105°C			125	
		V_{IN} = 2.7 V, I_{OUT} = –200 mA		T_A = 25°C		86	95	
				T_A = –40°C to +85°C			120	
				T_A = –40°C to +105°C			130	

Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over the following ambient operating temperature–40°C ≤T_A ≤ +105°C. Typical values are for T_A = 25°C.

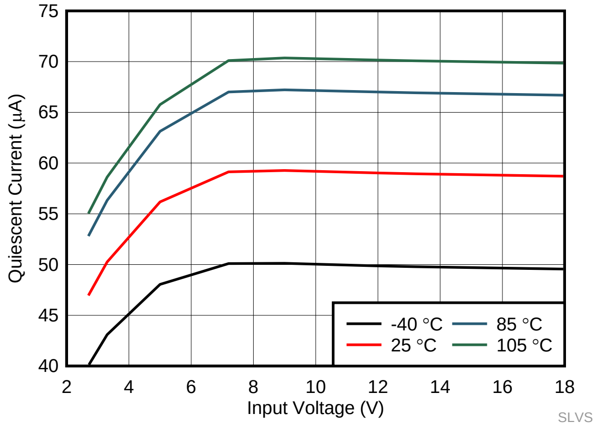
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{PD}	Output pull down resistance	V_{IN} = V_{OUT} = 18 V, $V_{EN/UVLO}$ = 0 V	T_A = –40°C to +105°C		290	350	Ω
		V_{IN} = V_{OUT} = 12 V, $V_{EN/UVLO}$ = 0 V	T_A = –40°C to +105°C		265	350	
		V_{IN} = V_{OUT} = 5 V, $V_{EN/UVLO}$ = 0 V	T_A = –40°C to +105°C		250	400	
T_{SD}	Thermal shutdown threshold	V_{IN} = 18 V	T_A = –40°C to +105°C		160		°C
$T_{SD,HYS}$	Thermal shutdown hysterisis	V_{IN} = 18 V	T_A = –40°C to +105°C		30		°C

6.6 Switching Characteristics

Refer to the timing test circuit in Figure 16 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the EN/UVLO pin is asserted high.

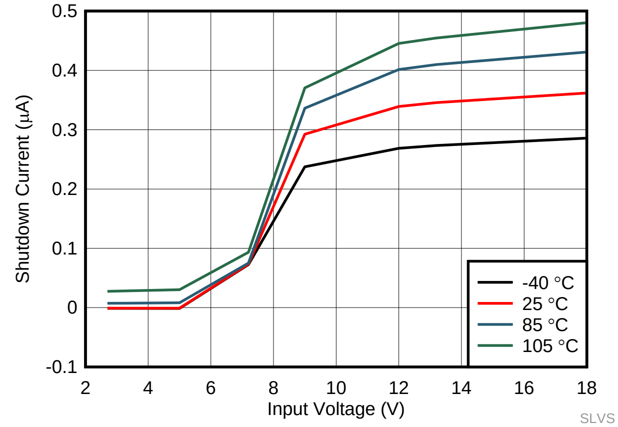
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 18 V, $V_{EN/UVLO}$ = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		520		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		3.3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		700		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		2		
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		180		
V_{IN} = 12 V, $V_{EN/UVLO}$ = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		380		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		3.3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		460		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		2		
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		150		
V_{IN} = 3.3 V, $V_{EN/UVLO}$ = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		185		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		3.3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		120		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		2		
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, C_T = 2200 pF		130		

6.7 Typical DC Characteristics



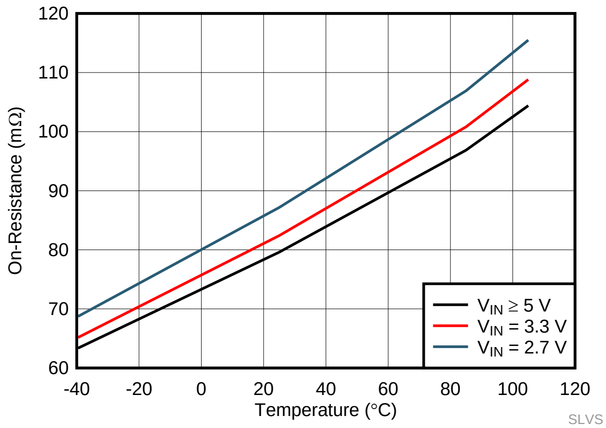
$V_{EN/UVLO}$ = 5 V I_{OUT} = 0 A

図 1. Quiescent Current vs Input Voltage



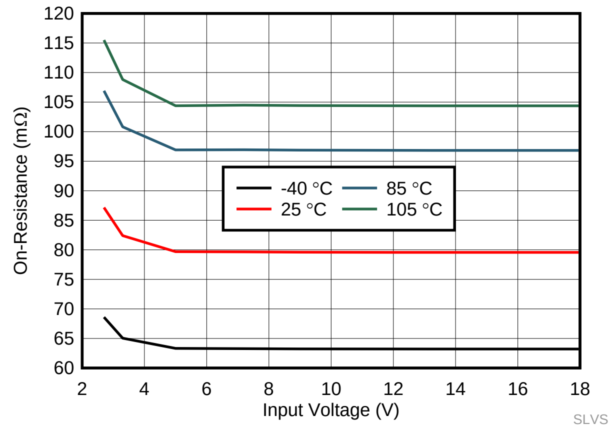
$V_{EN/UVLO}$ = 0 V I_{OUT} = 0 A

図 2. Shutdown Current vs Input Voltage



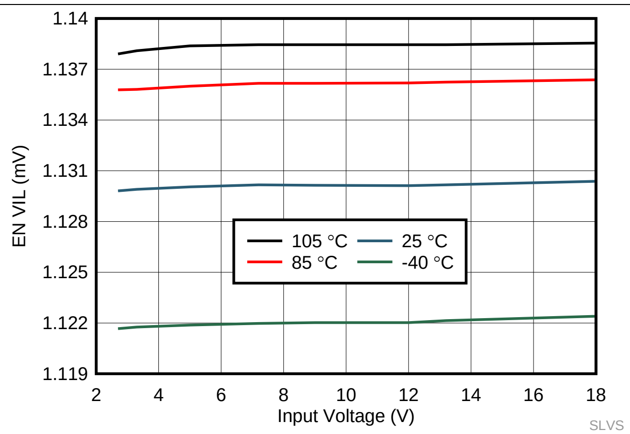
$V_{EN/UVLO}$ = 5 V I_{OUT} = –200 mA

図 3. On-Resistance vs Temperature



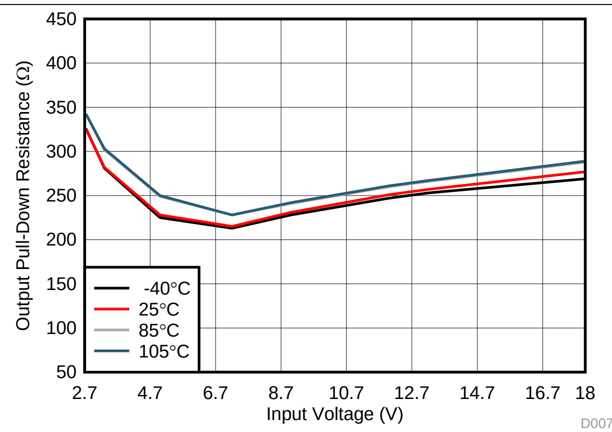
$V_{EN/UVLO}$ = 5 V I_{OUT} = –200 mA

図 4. On-Resistance vs Input Voltage



I_{OUT} = 0 A

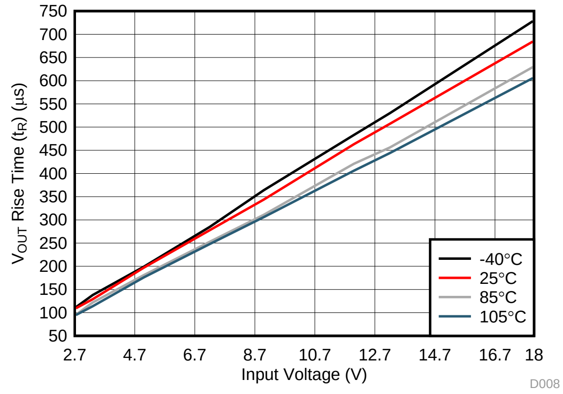
図 5. EN VIL vs Input Voltage



$V_{IN} = V_{OUT}$ $V_{EN/UVLO}$ = 0 V

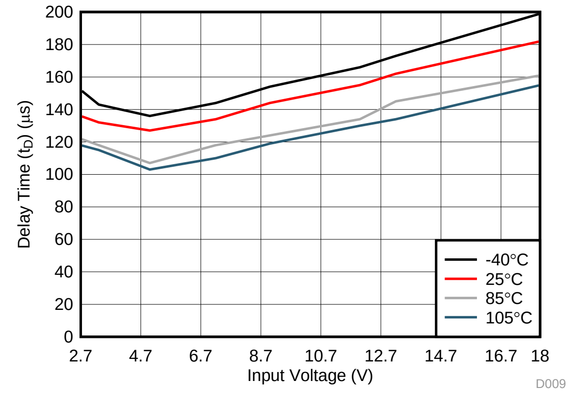
図 6. Output Pull-Down Resistance vs Input Voltage

6.8 Typical AC Characteristics



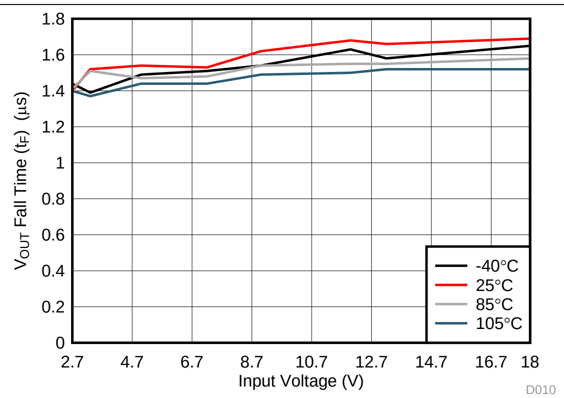
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF
CT = 2200 pF

図 7. V_{OUT} Rise Time (t_R) vs Input Voltage



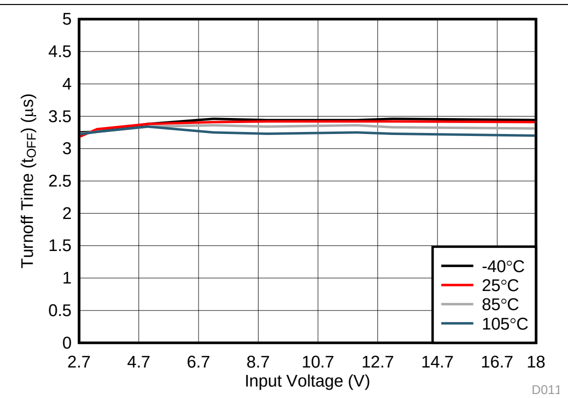
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF
CT = 2200 pF

図 8. Delay Time (t_D) vs Input Voltage



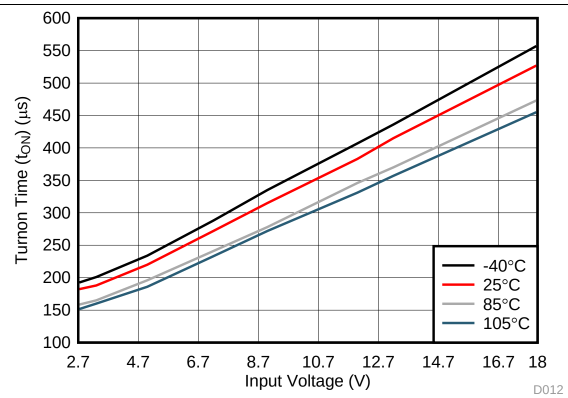
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

図 9. V_{OUT} Fall Time (t_F) vs Input Voltage



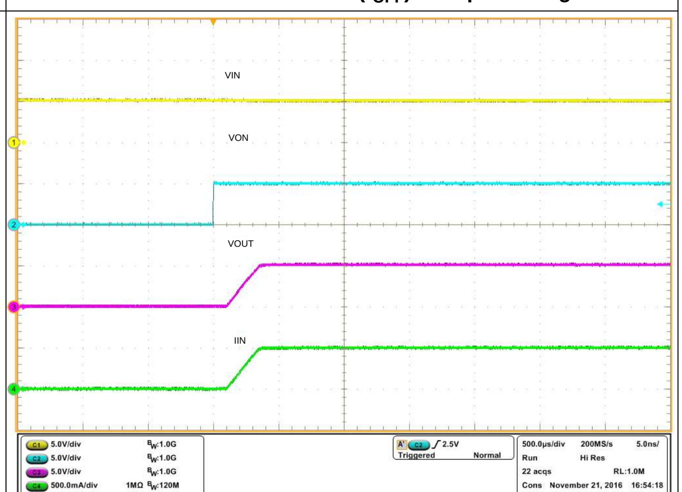
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

図 10. Turnoff Time (t_{OFF}) vs Input Voltage



C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF
CT = 2200 pF

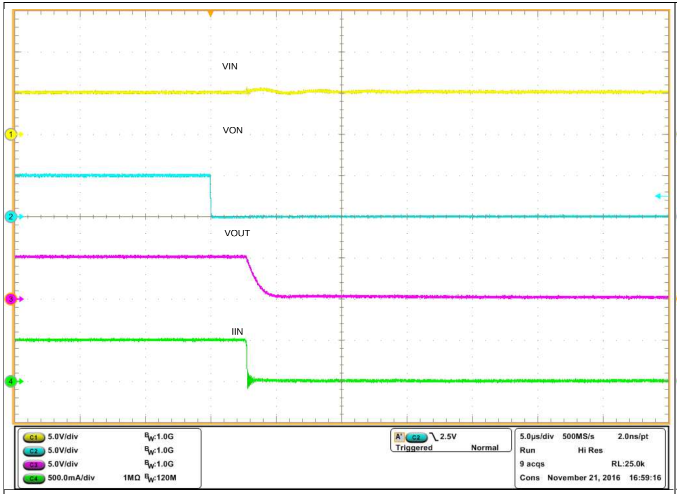
図 11. Turnon Time (t_{ON}) vs Input Voltage



V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω CT = 2200 pF

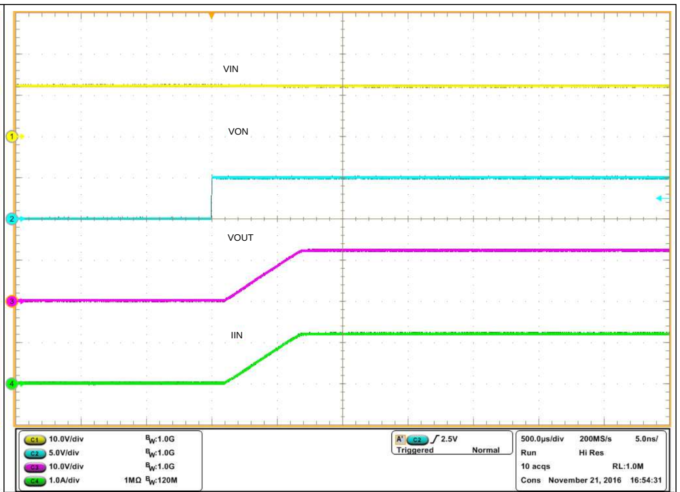
図 12. Rise Time t_R at V_{IN} = 5 V

Typical AC Characteristics (continued)



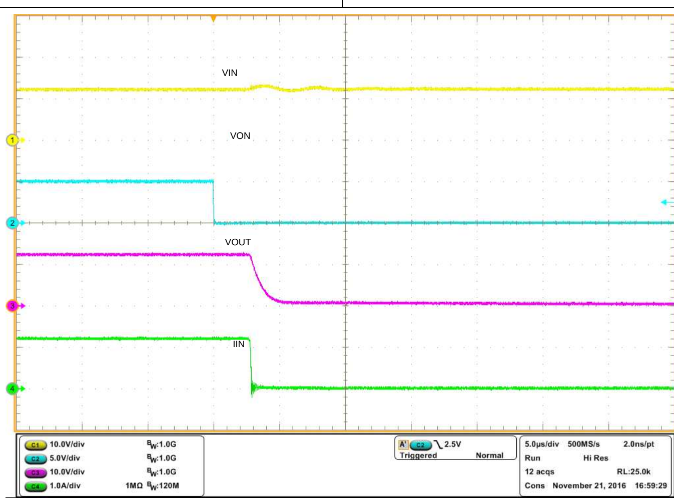
V_{IN} = 5 V　C_{IN} = 1 µF　C_L = 0.1 µF
R_L = 10 Ω　QOD = Open

図 13. Fall Time t_F at V_{IN} = 5 V



V_{IN} = 12 V　C_{IN} = 1 µF　C_L = 0.1 µF
R_L = 10 Ω　CT = 2200 pF

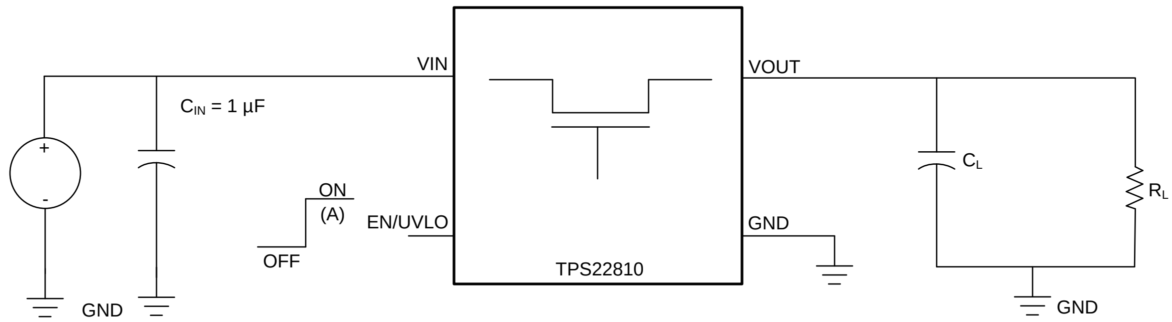
図 14. Rise Time t_R at V_{IN} = 12 V



V_{IN} = 12 V　C_{IN} = 1 µF　C_L = 0.1 µF
R_L = 10 Ω　QOD = Open

図 15. Fall Time t_F at V_{IN} = 12 V

7 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns

図 16. Test Circuit

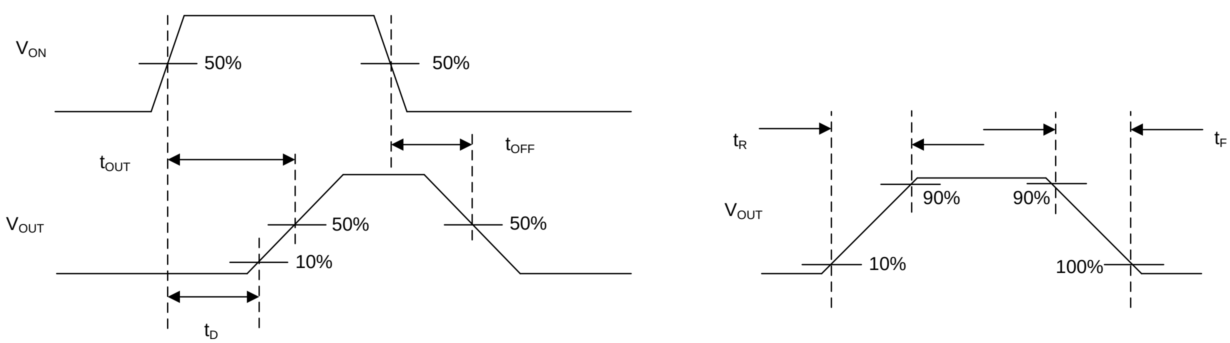


図 17. Timing Waveforms

8 Detailed Description

8.1 Overview

The TPS22810-Q1 is a 6-pin, 2.7-18-V load switch with thermal protection. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. When VIN rises, the internal MOSFET of the device starts conducting and allow current to flow from VIN to VOUT. When EN/UVLO is held low (below V_{ENF}), internal MOSFET is turned off.

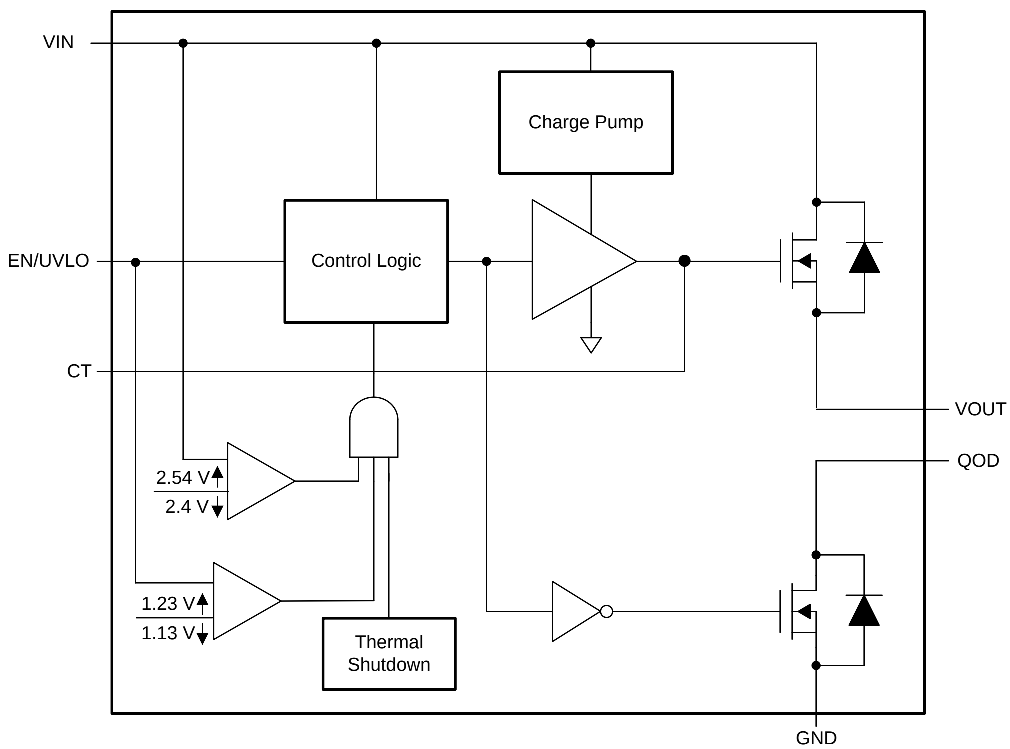
A voltage $V_{EN/UVLO} < V_{ENF}$ on this pin turns off the internal FET, thus disconnecting VIN from VOUT, while voltage below V_{SHUTF} takes the device into shutdown mode, with I_Q less than 1 μA to ensure minimal power loss.

The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. The device also features a QOD (Quick Output Discharge) pin with an internal pull-down resistance (R_{PD}) which can be used to discharge VOUT once the switch is disabled.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The device has a thermal protection feature to protect itself against thermal damage due to overtemperature and overcurrent conditions. Safe Operating Area (SOA) requirements are thus inherently met without any special design consideration by the board designer.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The EN/UVLO pin controls the state of the switch. EN/UVLO is active high and has a low threshold that can interface with low-voltage signals. The EN/UVLO pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

8.3.2 Quick Output Discharge (QOD)

The TPS22810-Q1 includes a QOD feature. The QOD pin can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal pull-down resistance (R_{PD}). The value of this resistance is listed in the *Electrical Characteristics* table.
- QOD pin connected to VOUT pin using an external resistor R_{EXT}. After the switch becomes disabled, the discharge rate is controlled by the value of the total resistance of the QOD. To adjust the total QOD resistance, 式 1 can be used.

  $$R_{QOD} = R_{PD} + R_{EXT} \quad (1)$$

  where
  - R_{QOD} is the total output discharge resistance
  - R_{PD} is the internal pulldown resistance
  - R_{EXT} is the external resistance placed between the VOUT and QOD pin.
- QOD pin is unused and left floating. Using this method, there is no quick output discharge functionality, and the output remains floating after the switch is disabled.

Note that during thermal shutdown, the QOD functionality is not available. The device does not discharge the load because R_{PD} does not become engaged.

The fall times of the device depend on many factors including the total resistance of the QOD, V_{IN}, and the output capacitance. When QOD is connected to VOUT, the fall time changes over V_{IN} because the internal R_{PD} varies over V_{IN}. To calculate the approximate fall time of V_{OUT} for a given R_{QOD}, use 式 2 and 表 1.

$$V_{CAP} = V_{IN} \times e^{-t/\tau} \quad (2)$$

where
- V_{CAP} is the voltage across the capacitor (V)
- t is the time since power supply removal (s)
- τ is the time constant equal to $R_{QOD} \times C_L$

The fall time's dependency on V_{IN} becomes minimal because the QOD value increases with additional external resistance. See 表 1 for QOD fall times.

表 1. QOD Fall Times

V_{IN} (V)	FALL TIME (µs) 90% - 10%, C_{IN} = 1 µF, I_{OUT} = 0 A , V_{IN} = 0 V, ON = 0 V (1)					
	T_A = 25°C			T_A = 85°C		
	C_L = 1 µF	C_L = 10 µF	C_L = 100 µF	C_L = 1 µF	C_L = 10 µF	C_L = 100 µF
18	470	4700	47000	470	4700	47000
12	450	4500	45000	450	4500	45000
9	440	4400	44000	440	4400	44000
5	500	5000	50000	480	4800	48000
3.3	600	6000	60000	570	5700	57000

(1) TYPICAL VALUES WITH QOD SHORTED TO VOUT

8.3.2.1 QOD when System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor, C_{IN}, discharges at VIN. Past the set UVLO level, the pull-down resistance R_{PD} becomes disabled and the output no longer becomes discharged. If there is still remaining charge on the output capacitor, this results in longer fall times. Care must be taken such that C_{IN} is large enough to meet the device UVLO settings.

8.3.2.2 Internal QOD Considerations

Special considerations must be taken when using the internal R_{PD} by shorting the QOD pin to the VOUT pin. The internal R_{PD} is a pull-down resistance designed to quickly discharge a load after the switch has been disabled. Care must be used to ensure that excessive current does not flow through R_{PD} during discharge so that the maximum T_J of 125°C is not exceeded. When using only the internal R_{PD} to discharge a load, the total capacitive load must not exceed 200 uF. Otherwise, an external resistor, R_{EXT} must be used to ensure the amount of current flowing through R_{PD} is properly limited and the maximum T_J is not exceeded. To ensure the device is not damaged, the remaining charge from C_L must decay naturally through the internal QOD resistance and must not be driven.

8.3.3 EN/UVLO

EN/UVLO controls the ON and OFF state of the internal MOSFET, as an input pin. In its high state, the internal MOSFET is enabled. A low on this pin turns off the internal MOSFET. High and Low levels are specified in the parametric table of the datasheet.

A voltage $V_{EN/UVLO} < V_{ENF}$ on this pin turns off the internal FET, thus disconnecting VIN from VOUT, while voltage below V_{SHUTF} takes the device into shutdown mode, with I_Q less than 1 μA to ensure minimal power loss.

The EN/UVLO pin can be directly driven by a 1.8 V, 3.3 V or 5 V general purpose output pin.

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (2.5 μs typical) for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

The undervoltage lock out (UVLO) threshold can be programmed by using an external resistor divider from supply VIN terminal to EN/UVLO terminal to GND shown in 図 18. When an undervoltage or input power fail event is detected, the internal FET is quickly turned off. If the programmable UVLO function is not needed, the EN/UVLO terminal must be connected to the VIN terminal. EN/UVLO terminal must not be left floating.

The device also implements internal UVLO circuitry on the VIN terminal. The device disables when the VIN terminal voltage falls below internal UVLO Threshold (V_{UVF}). The internal UVLO threshold has a hysteresis ($V_{UVRhyst}$). See 図 19 and 図 20.

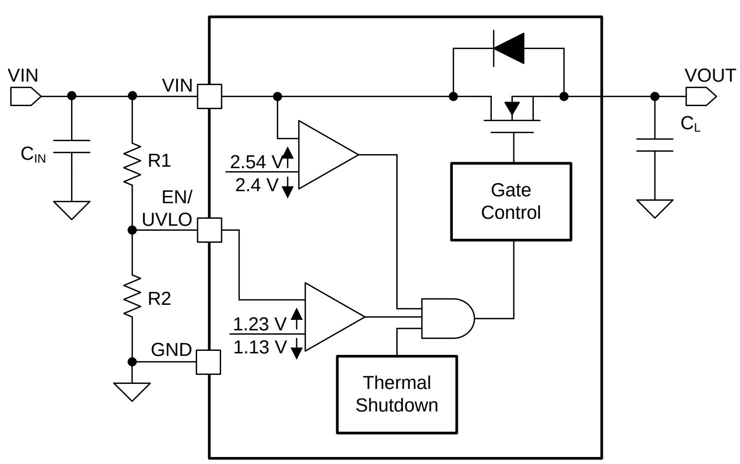


図 18. Configuring UVLO with External Resistor Network

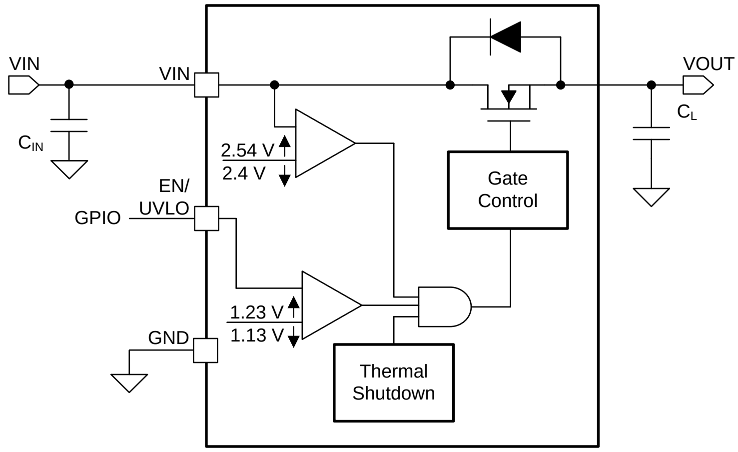


図 19. Using 1.8 V/3.3 V GPIO Signal Directly from Processor

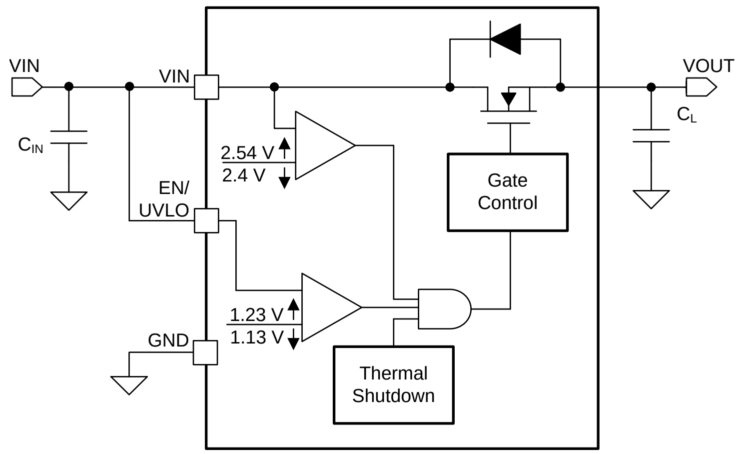


図 20. Default UVLO Threshold V_{UVR} Using No Additional External Components

8.3.4 Adjustable Rise Time (CT)

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 2.5 V. An approximate formula for the relationship between CT and slew rate is shown in 式 3. This equation accounts for 10% to 90% measurement on VOUT and does NOT apply for CT < 1 nF.

Use 表 2 to determine rise times for when CT ≥ 1 nF.

$$SR = 46.62 / CT$$

where

- SR is the slew rate (in V/µs)
- CT is the the capacitance value on the CT pin (in pF) (3)

Rise time can be calculated by dividing the input voltage by the slew rate. 表 2 describes rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN is already in steady state condition before the EN/UVLO pin is asserted high.

表 2. Rise Time Table

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω				
	VIN = 18 V	VIN = 12 V	VIN = 9 V	VIN = 5 V	VIN = 3.3 V
0	115	91	78	60	98
470	136	94	80	63	98
1000	310	209	158	91	102
2200	688	464	345	198	135
4700	1430	957	704	397	265
10000	3115	2085	1540	864	550
27000	8230	5460	4010	2245	1430

8.3.5 Thermal Shutdown

The switch disables when the junction temperature (T_J) rises above the thermal shutdown threshold, T_{SD}. The switch re-enables once the temperature drops below the T_{SD} – $T_{SD,HYS}$ value.

8.4 Device Functional Modes

The features of the TPS22810-Q1 depend on the operating mode. 表 3 summarizes the Device Functional Modes.

表 3. Function Table

EN/UVLO	Device State
L	Disabled
H	Enabled

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com (See the Device Support section for more information).

9.1.1 ON and OFF Control

The EN/UVLO pin controls the state of the switch. Asserting EN/UVLO high enables the switch. EN/UVLO is active high and has a low threshold that can interface with low-voltage signals. The EN/UVLO pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

9.1.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor must be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.1.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause VOUT to exceed VIN when the system supply is removed. This can result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) can cause slightly more VIN dip upon turnon due to inrush currents.

This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

9.2 Typical Application

This typical application demonstrates how the TPS22810-Q1 can be used to power downstream modules.

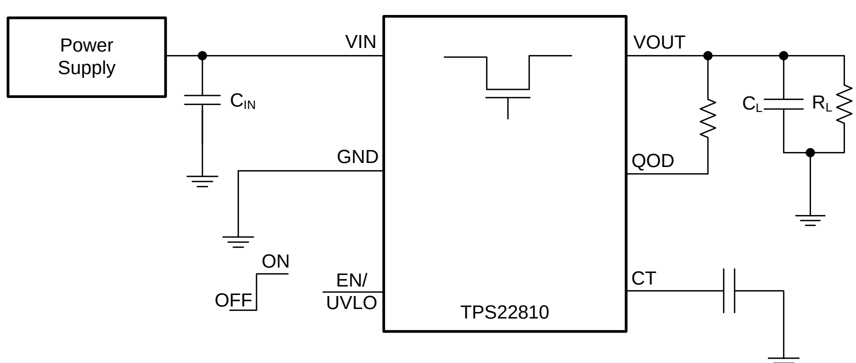


図 21. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the values listed in 表 4:

表 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	12 V
Load current	2 A
C_L	22 µF
Desired fall time	20 ms
Maximum acceptable inrush current	400 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Shutdown Sequencing During Unexpected Power Loss

Using the adjustable Quick Output Discharge function of the TPS22810-Q1, adding a load switch to each power rail can be used to manage the power down sequencing in the event of an unexpected power loss (for example, battery removal). To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down. Next, consult 表 1 to determine appropriate C_L and R_{QOD} values for each power rail's load switch so that the load switches' fall times correspond to the order in which they need to be powered down. In the above example, we must have this power rail's fall time to be 4 ms. Using 式 2, we can determine the appropriate R_{QOD} to achieve our desired fall time.

Since fall times are measured from 90% of V_{OUT} to 10% of V_{OUT}, using 式 2, we get 式 4 and 式 5.

$$1.2V = 10.8V \times e^{-(20ms)/(R_{QOD} \times (22\mu F))} \quad (4)$$

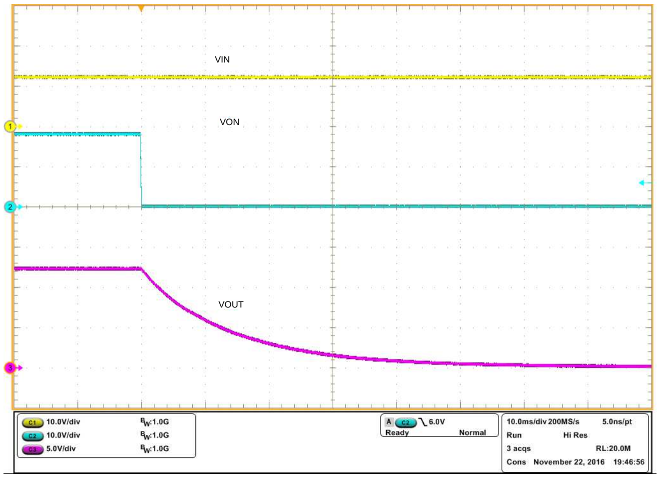
$$R_{QOD} = 413.7\ \Omega \quad (5)$$

Consulting 図 6, R_{PD} at V_{IN} = 12 V is approximately 250 Ω. Using 式 1, the required external QOD resistance can be calculated shown in 式 6 and 式 7.

$$413.7\ \Omega = 250\ \Omega + R_{EXT} \quad (6)$$

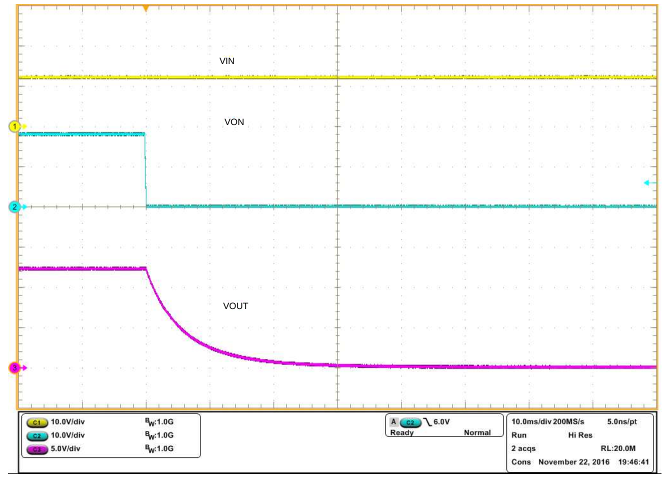
$$R_{EXT} = 163.7\ \Omega \quad (7)$$

図 22 through 図 25 are scope shots demonstrating an example of the QOD functionality when power is removed from the device (both ON and VIN are disconnected simultaneously). In the scope shots, the V_{IN} = 12 V and correspond to when R_{QOD} = 1000 Ω, R_{QOD}= 500 Ω, and QOD = VOUT with two values of C_L = 10 µF and 22 µF.



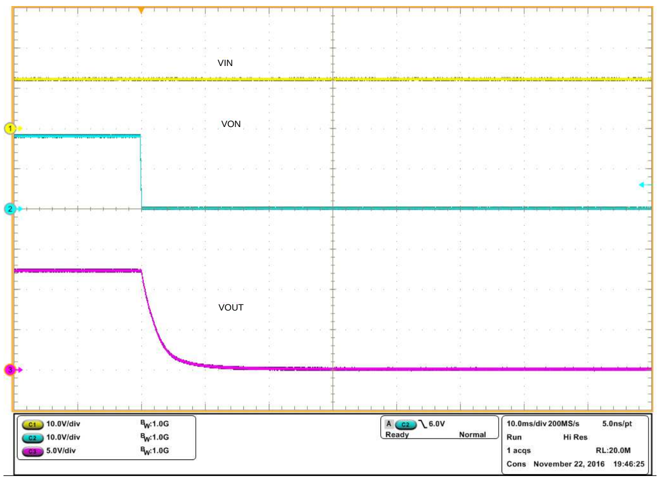
V_{IN} = 12 V C_{IN} = 1 µF C_L = 10 µF

図 22. Fall Time t_F at V_{IN} = 12 V, R_{QOD} = 1000 Ω



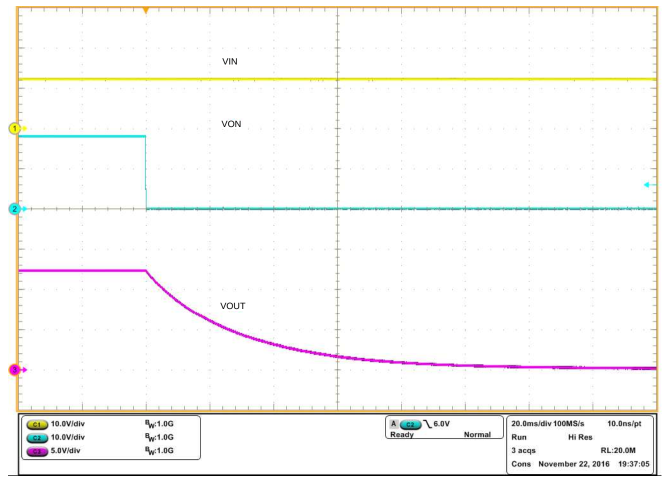
V_{IN} = 12 V C_{IN} = 1 µF C_L = 10 µF

図 23. Fall Time t_F at V_{IN} = 12 V, R_{QOD} = 500 Ω



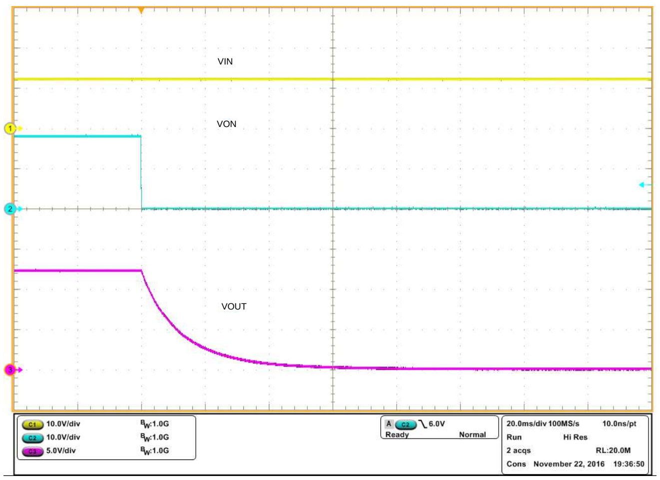
V_{IN} = 12 V C_{IN} = 1 µF C_L = 10 µF

図 24. t_F at V_{IN} = 12 V , QOD = V_{OUT}



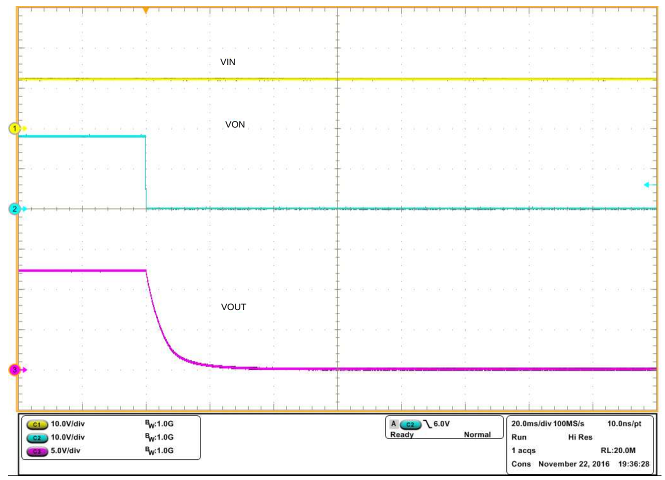
V_{IN} = 12 V C_{IN} = 1 µF C_L = 22 µF

図 25. t_F at V_{IN} = 12 V, R_{QOD} = 1000 Ω



V_{IN} = 12 V C_{IN} = 1 µF C_L = 22 µF

図 26. t_F at V_{IN} = 12 V, R_{QOD} = 500 Ω



V_{IN} = 12 V C_{IN} = 1 µF C_L = 22 µF

図 27. t_F at V_{IN} = 12 V, QOD = V_{OUT}

9.2.2.2 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use 式 8 to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \quad (8)$$

where

- ΔV is the voltage drop from VIN to VOUT
- I_{LOAD} is the load current
- R_{ON} is the On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.2.2.3 Inrush Current

To determine how much inrush current is caused by the C_L capacitor, use 式 9.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (9)$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the capacitance on VOUT
- dt is the Output Voltage rise time during the ramp up of VOUT when the device is enabled
- dV_{OUT} is the change in V_{OUT} during the ramp up of VOUT when the device is enabled

The appropriate rise time can be calculated using the design requirements and the inrush current equation. When we calculate the rise time (measured from 10% to 90% of V_{OUT}), we account for this in our d_{VOUT} parameter (80% of V_{OUT} = 9.6 V) shown in 式 10 and 式 11.

$$400 \text{ mA} = 22 \text{ µF} \times 9.6 \text{ V/dt} \quad (10)$$

$$dt = 528 \text{ µs} \quad (11)$$

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 528 µs. Consulting 表 2 at V_{IN} = 12 V, CT = 4700 pF provides a typical rise time of 957 µs. Using this rise time and voltage into 式 9, yields 式 12 and 式 13.

$$I_{Inrush} = 22 \text{ µF} \times 9.6 \text{ V/ } 957 \text{ µs} \quad (12)$$

$$_{Inrush} = 220 \text{ mA} \quad (13)$$

An appropriate C_L value must be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

9.2.3 Application Curves

See the oscilloscope captures below for an example of how the CT capacitor can be used to reduce inrush current for V_{IN} = 12 V. See the *Adjustable Rise Time (CT)* section for rise times for corresponding CT values.

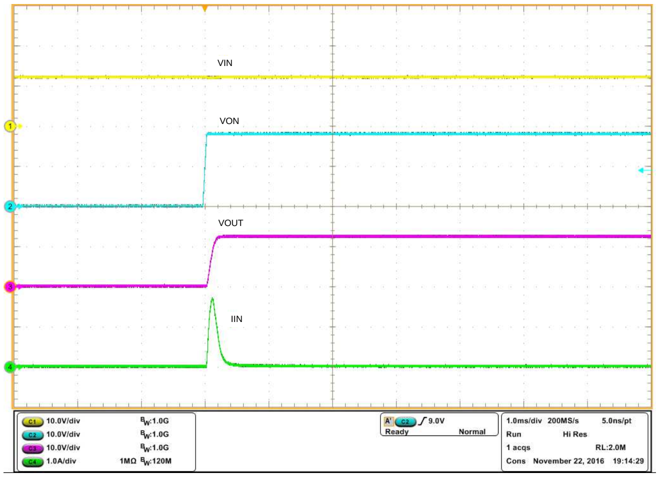


図 28. TPS22810-Q1 Inrush Current With C_L = 22 µF, CT = 0 pF

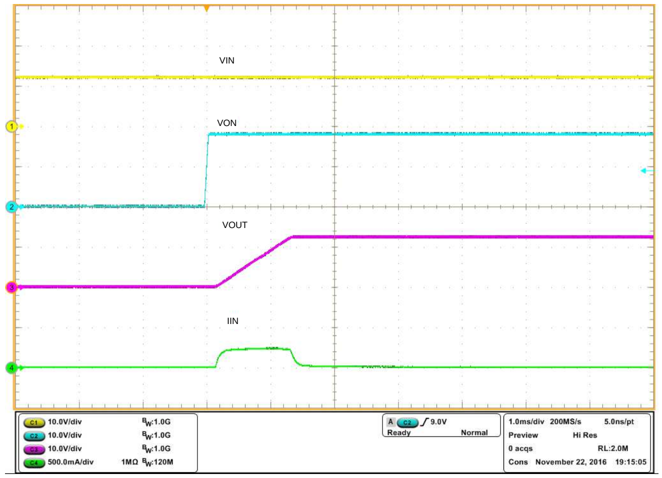


図 29. TPS22810-Q1 Inrush Current with C_L = 22 µF, CT = 4700 pF

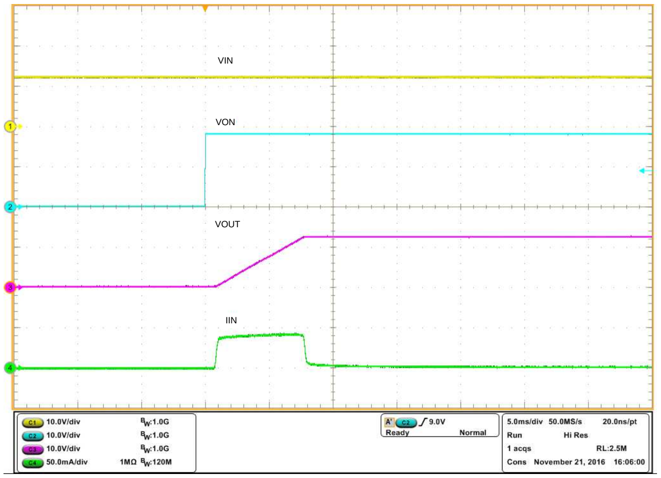


図 30. TPS22810-Q1 Inrush Current With C_L = 22 µF, CT = 27000 pF

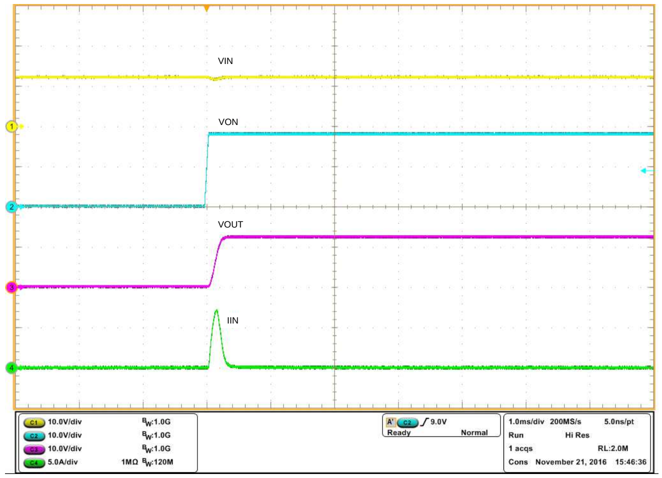


図 31. TPS22810-Q1 Inrush Current With C_L = 100 µF, CT = 0 pF

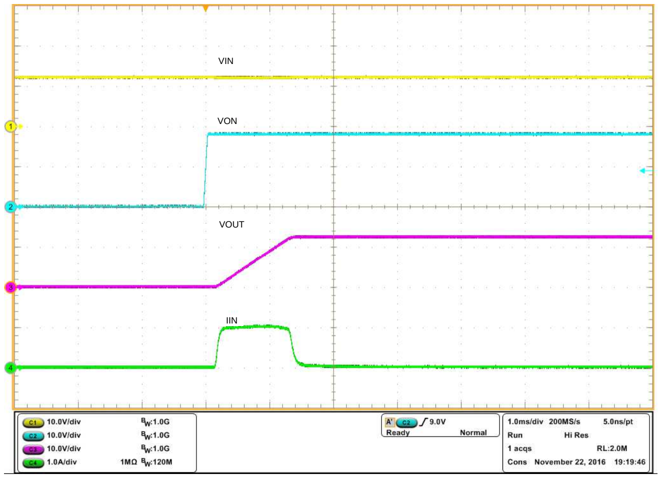


図 32. TPS22810-Q1 Inrush Current With C_L = 100 µF, CT = 4700 pF

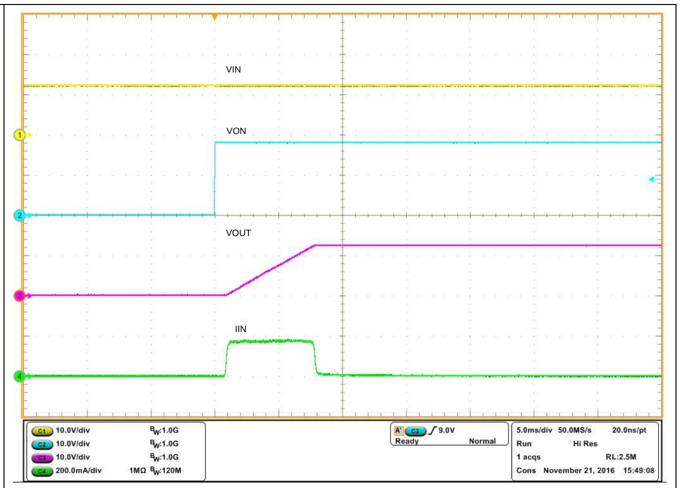


図 33. TPS22810-Q1 Inrush Current With C_L = 100 µF, CT = 27000 pF

10 Power Supply Recommendations

The device is designed to operate from a VIN range of 2.7 V to 18 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1-µF may be sufficient.

The TPS22810-Q1 operates regardless of power sequencing order. The order in which voltages are applied to VIN and EN/UVLO does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions.

11 Layout

11.1 Layout Guidelines

1. VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
2. The VIN pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.

11.2 Layout Example

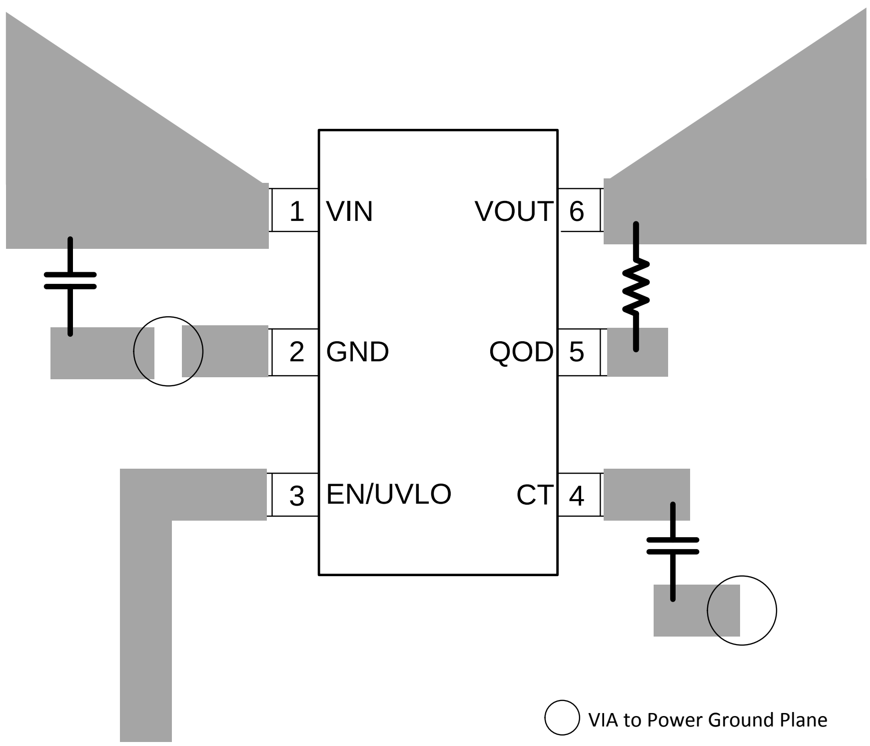


図 34. Recommended Board Layout

11.3 Thermal Considerations

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use 式 14.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (14)$$

where

- $P_{D(MAX)}$ is the maximum allowable power dissipation
- $T_{J(MAX)}$ is the maximum allowable junction temperature (150°C for the TPS22810-Q1)
- T_A is the ambient temperature of the device
- θ_{JA} is the junction to air thermal impedance. Refer to the *Thermal Information* table. This parameter highly depends on the board layout.

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

TPS22810 PSpiceトランジェント・モデルについては、『*TPS22810 PSpiceトランジェント・モデル*』を参照してください。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- 『*TPS22810負荷スイッチ評価モジュール*』
- 『*ディスクリート・ソリューションに置き換わる負荷スイッチの選択*』
- 『*負荷スイッチのタイミング*』

12.3 ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでお使いの製品のフォルダへ移動します。右上の隅にある「*通知を受け取る*」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.5 商標

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12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22810TDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1EFF	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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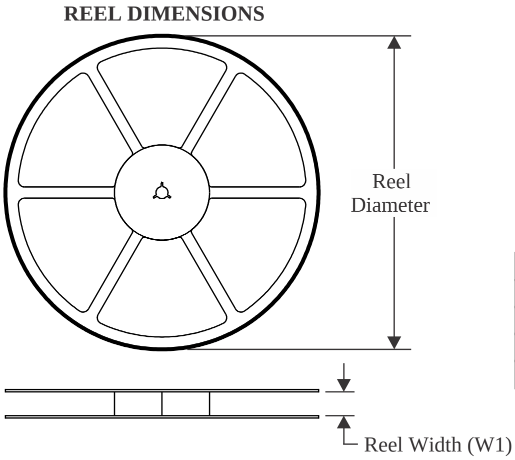
OTHER QUALIFIED VERSIONS OF TPS22810-Q1 :

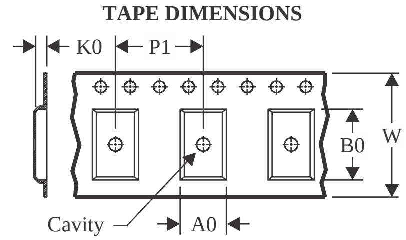
- Catalog : TPS22810

NOTE: Qualified Version Definitions:

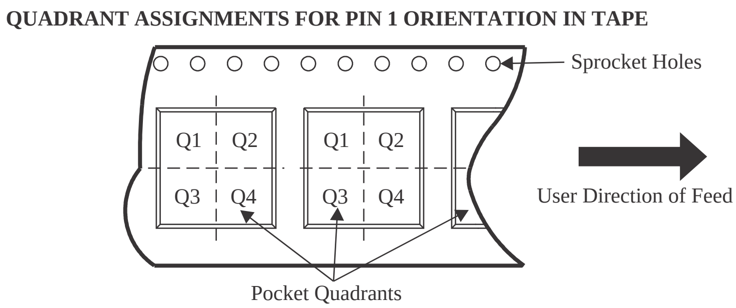
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





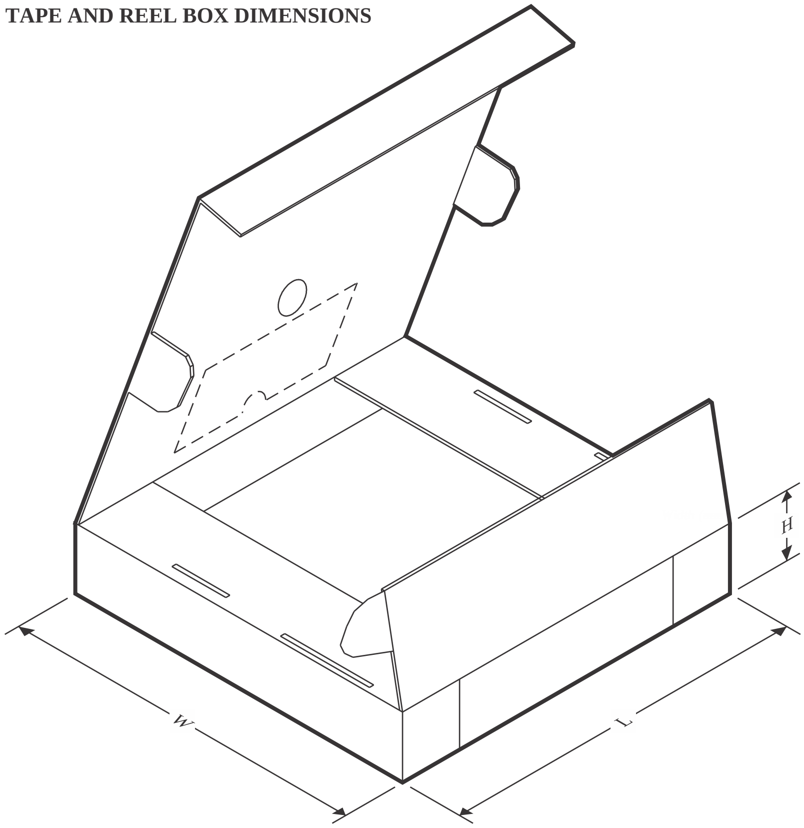
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

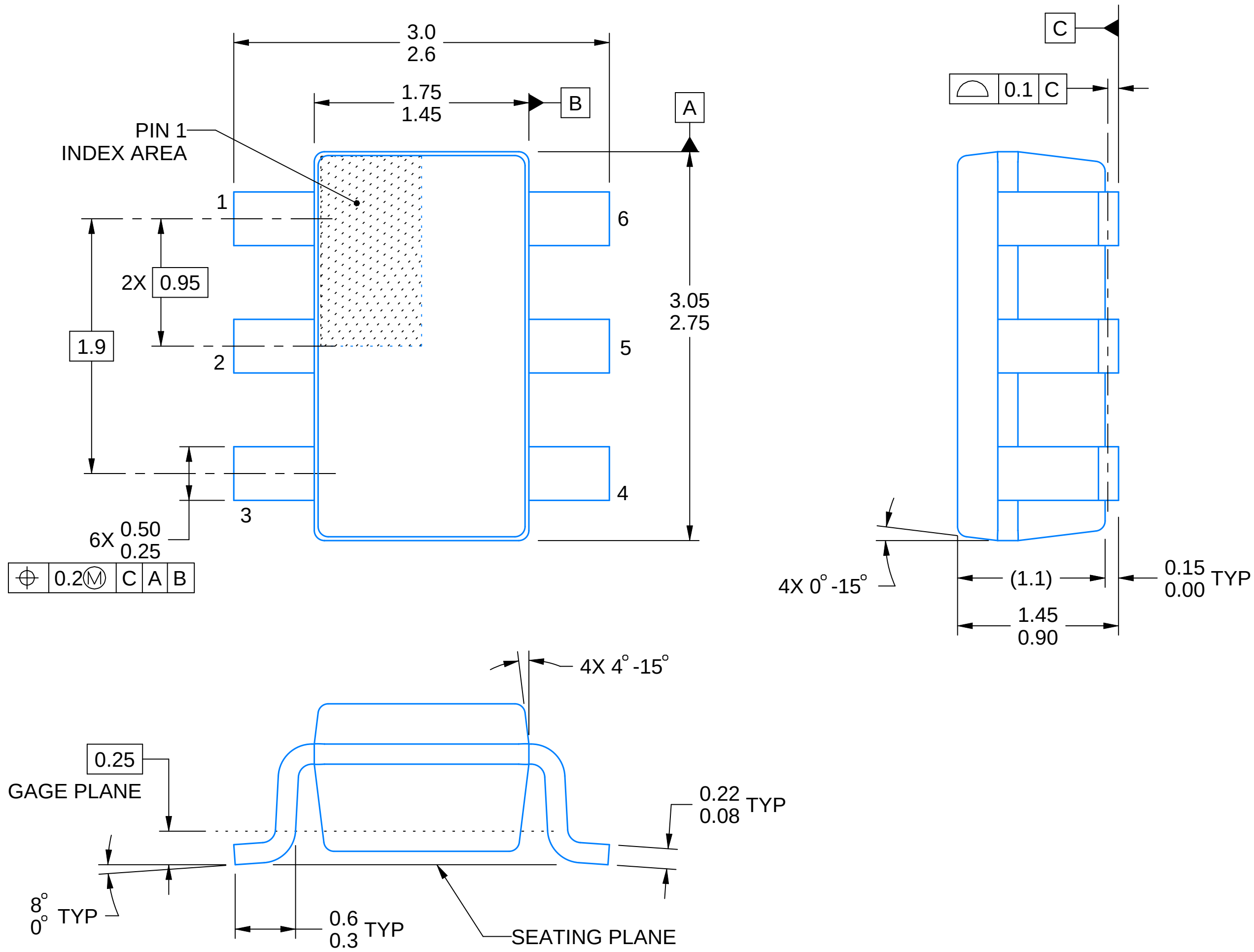
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22810TDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22810TDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0



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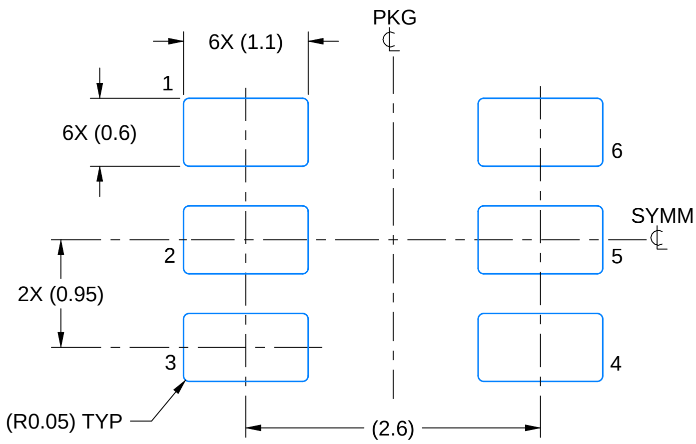
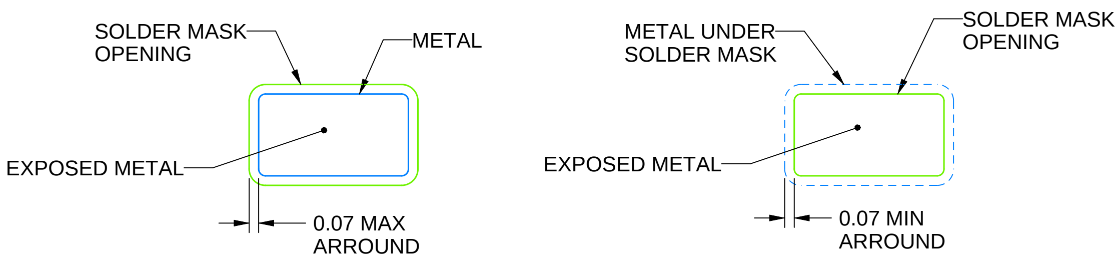
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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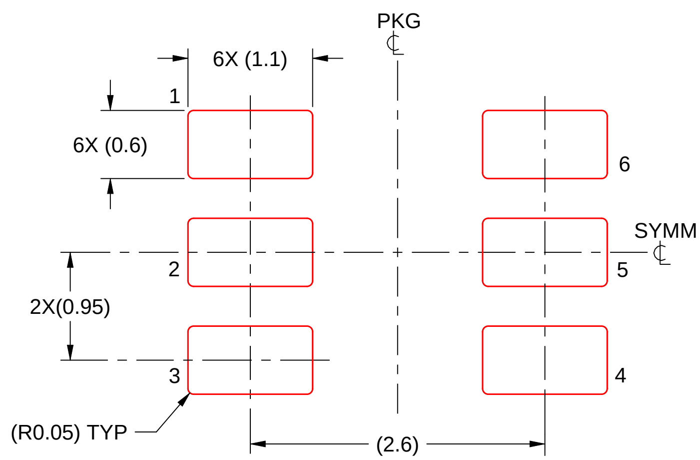
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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