

TPS2372 自動MPSおよび自動クラスを搭載した大電力PoE PDインターフェイス

1 特長

- IEEE 802.3bt (ドラフト) タイプ3またはタイプ4 PoE用のPDソリューション
- タイプ4 (TPS2372-4) 90Wおよびタイプ3 (TPS2372-3) 60W動作の電力レベルをサポート
- 堅牢な100VのホットスワップMOSFET
 - TPS2372-4 (標準値): 0.1Ω、2.2A電流制限
 - TPS2372-3 (標準値): 0.3Ω、1.85A電流制限
- 電源インジケータ出力を割り当て済み
- 突入電流完了遅延付きのPG出力
 - PSE突入電流に準拠
- 自動電源シグネチャ保持(MPS)
 - タイプ1-2または3-4 PSEに合わせてMPSを自動調整
 - 超低消費電力のスタンバイ・モードをサポート
- 自動クラス動作をサポート
- PoE++ PSEをサポート
- 接合部温度範囲: -40°C ~ 125°C
- 20リードのVQFNパッケージ

2 アプリケーション

- IEEE 802.3bt (ドラフト) 準拠のデバイス
- 照明
- パワー・モジュール
- デュアル・シグネチャPD/強制UPOE
- 4PPOE
- パススルー・システム
- 防犯カメラ
- マルチバンドのアクセス・ポイント
- Pico基地局

3 概要

TPS2372には、IEEE802.3atまたはIEEE802.3bt (ドラフト) (タイプ1-4)受電機器(PD)を実装するために必要な、すべての機能が含まれています。内部スイッチ抵抗が低いため、TPS2372-4およびTPS2372-3は、それぞれ最大90Wおよび60Wの大電力アプリケーションをサポートできます。100mのCAT5ケーブルを想定した場合、これはPD入力の71.3Wおよび51Wに相当します。

TPS2372は拡張機能付きで動作します。

自動MPS機能により、非常に消費電力の低いスタンバイ・モードが必要なアプリケーションにも使用可能です。

TPS2372は、PSE電力を維持するため必要な、パルス化された電流を自動的に生成します。外付けの抵抗を使用して、この機能を有効化し、MPSのパルス化された電流の振幅をプログラムできます。

また、TPS2372には遅延機能が実装されており、リモートPSEは突入フェーズを完了してから、パワー・グッド(PG)出力を解除できます。これによって、IEEE802.3bt (ドラフト)のスタートアップ要件を満たすことができます。

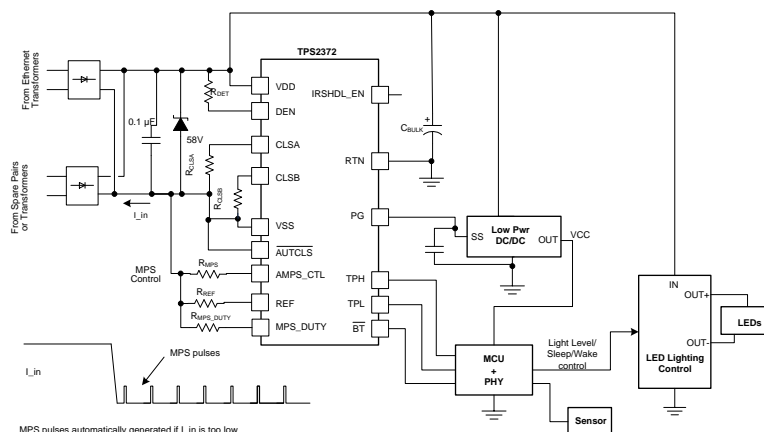
また、自動クラスのイネーブル入力により、IEEE802.3bt (ドラフト)標準に準拠した、高度なシステム電力最適化モードも可能になります。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS2372	VQFN (20)	5.00mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



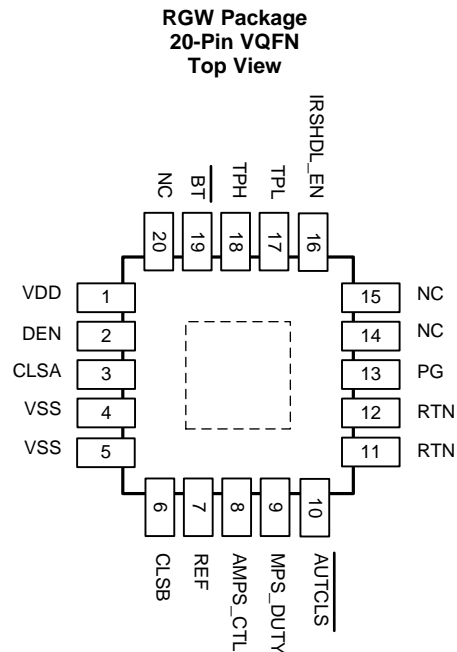
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			12	メカニカル、パッケージ、および注文情報	36

4 改訂履歴

Revision A (February 2018) から Revision B に変更	Page
• Added TableNote to	15
• Added dashed box with optional on it in Figure 22	27
• Added PSE and POE information to Opto-isolators for TPH, TPL and \overline{BT}	29
2017年10月発行のものから更新	Page
• TPS2372-2の標準電流制限を1.85Aに 変更	1
• TPS2372-3デバイスを量産データに 変更	1
• 事前情報表の注記 削除	1
• Changed current limit nominal value to 1.85 and maximum value to 2.2	6
• Changed minimum value of inrush termination to 65%	6
• Changed typical shutdown temperature to 158°C	8
• Added TPS2372-4 to the title of Figure 10	10
• Changed "current limit is changed to 1.8 A" to "current limit is changed to 1.85 A" in <i>Internal Pass MOSFET and Inrush Delay Enable, IRSHDL_EN</i> subsection	15
• Changed "~" to "approximately" and "1.8 A" to "1.85 A" in the <i>Advanced Startup and Converter Operation</i> subsection	24
• Changed equation 3 and equation 4 values in <i>Automatic MPS and MPS Duty Cycle, R_{MPS} and R_{MPS_DUTY}</i>	30
• 変更 TPS2372-3RGWRおよびTPS2372-3RGWTデバイスをアクティブに	36

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	Connect to positive PoE input power rail. Bypass with 0.1 μ F to VSS.
DEN	2	I/O	Connect a 24.9 k Ω resistor from DEN to VDD to provide the PoE detection signature. Pull DEN to VSS to disable the pass MOSFET during powered operation.
CLSA	3	O	Connect a resistor from CLSA to VSS to program the first classification current.
VSS	4, 5	—	Connect to negative power rail derived from PoE source.
CLSB	6	O	Connect a resistor from CLSB to VSS to program the second classification current.
REF	7	O	Internal 1.5 V voltage reference. Connect a 49.9k Ω _1% resistor from REF to VSS.
AMPS_CTL	8	O	Automatic MPS control. Connect a resistor with appropriate power rating (to support the MPS current) from AMPS_CTL to VSS to program the MPS current amplitude. Leave AMPS_CTL open to disable the automatic MPS function.
MPS_DUTY	9	I	MPS duty cycle select input, referenced to VSS, internally driven by a precision current source with voltage limited to less than \sim 5.5V. A resistor connected to VSS determines if the MPS duty cycle selected is either 5.4% (open), 8.1% (\sim 60.4 k Ω) or 12.5% (short).
AUTCLS	10	I	Autoclass enable input. Internally pulled-up to 5.5 V internal rail during classification only, pulled down in other circumstances to minimize consumption. Pull low (to VSS) to enable the Autoclass function during classification. Leave open otherwise.
RTN	11, 12	—	Drain of PoE pass MOSFET. Return line from the load to the controller.
PG	13	O	Power Good output. Open-drain, active-high output referenced to RTN.
NC	14, 15	—	No connect
IRSHDL_EN	16	I	PSE inrush delay (\sim 81.5 ms) enable, referenced to RTN, internally pulled-up to 5.5 V internal rail. Leave open to enable the inrush delay.
TPL	17	O	PSE allocated power outputs, binary coded. Open-drain, active-low outputs referenced to RTN.
TPH	18	O	
BT	19	O	Indicates that a PSE applying an IEEE802.3bt (Type 3 or 4) mutual identification scheme has been identified. Open-drain, active-low output referenced to RTN.
NC	20	—	No connect pin. Leave open.
Pad	—	—	The exposed thermal pad must be connected to VSS. A large fill area is required to assist in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over recommended T_J range; voltages with respect to V_{VSS} (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VDD, DEN	−0.3	100	V
	RTN ⁽²⁾	−0.6	100	
	IRSHDL_EN to RTN	−0.3	6.5	
	\overline{AUTCLS}	−0.3	6.5	
Output voltage	CLSA, CLSB, REF, MPS_DUTY ⁽³⁾	−0.3	6.5	V
	AMPS_CTL ⁽³⁾	−0.3	30	
Voltage	PG to RTN	−0.3	100	V
	TPH, TPL, \overline{BT} to RTN	−0.3	100	
Sinking current	RTN ⁽⁴⁾	Internally limited		mA
	PG, TPH, TPL, \overline{BT}	10		
	DEN	1		
Sourcing current	CLSA, CLSB	65		mA
	REF	Internally limited		
	AMPS_CTL	50		
T _{J(max)}	Maximum junction temperature	Internally limited		°C
T _{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) With $I_{RTN} = 0$

(3) Do not apply voltages to these pins

(4) SOA limited to RTN = 80 V at 2.5 A.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	
	IEC 61000-4-2 contact discharge ⁽³⁾	±8000	
	IEC 61000-4-2 air-gap discharge ⁽³⁾	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(3) Discharges applied to circuit of [Figure 22](#) between RJ-45, adapter, and output voltage rails, on TPS2372- 4EVM-006 Evaluation Module.

6.3 Recommended Operating Conditions

over operating free-air temperature range and voltages with respect to V_{SS} (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	RTN, VDD	0		57	V
Voltage range	TPH, TPL, \overline{BT} to RTN	0		57	V
	PG to RTN	0		57	
Sinking current	RTN (TPS2372-3)			1.2	A
	RTN (TPS2372-4)			1.85	
	PG, TPH, TPL, \overline{BT}			3	mA
Resistance	CLSA, CLSB ⁽¹⁾	60			Ω
	AMPS_CTL ⁽¹⁾	1			k Ω
	REF ⁽¹⁾	48.9	49.9	50.9	
Junction temperature		–40		125	°C

(1) Voltage should not be externally applied to this pin.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS2372-3	TPS2372-4	UNIT
		RGW (VQFN)	RGW (VQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.2	38.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.6	28.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	16.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.8	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Unless otherwise noted, $40\text{ V} \leq V_{DD} \leq 57\text{ V}$; $R_{DEN} = 24.9\text{ k}\Omega$; PG, CLSA, CLSB, MPS_DUTY, AMPS_CTL, IRSHDL_EN, TPH, TPL and BT open; $V_{AUTCLS} = V_{VSS}$; $R_{REF} = 49.9\text{ k}\Omega$; $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$. Positive currents are into pins. Typical values are at 25°C . All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DETECTION (DEN)						
Bias current		DEN open, $V_{DD} = 10.1\text{ V}$, Measure $I_{SUPPLY}(V_{DD}, RTN, DEN)$, Not in mark	3	4.8	14	μA
DEN leakage current		$V_{DEN} = V_{DD} = 57\text{ V}$		0.5	5	μA
Detection current		Measure $I_{SUPPLY}(V_{DD}, RTN, DEN)$, $V_{DD} = 1.4\text{ V}$	53.8	56.5	58.3	μA
		Measure $I_{SUPPLY}(V_{DD}, RTN, DEN)$, $V_{DD} = 10.1\text{ V}$, Not in mark	395	410	417	
V_{PD_DIS}	Disable threshold	DEN falling	3	3.7	5	V
	Hysteresis		75	150	250	mV
CLASSIFICATION (CLS)						
I_{CLS}	Classification A,B signature current	$13\text{ V} \leq V_{DD} \leq 21\text{ V}$, Measure $I_{VDD} + I_{DEN} + I_{RTN}$				mA
		R_{CLSA} or $R_{CLSB} = 1210\text{ }\Omega$	2.1	2.5	2.9	
		R_{CLSA} or $R_{CLSB} = 249\text{ }\Omega$	9.9	10.6	11.2	
		R_{CLSA} or $R_{CLSB} = 140\text{ }\Omega$	17.6	18.6	19.4	
		R_{CLSA} or $R_{CLSB} = 90.9\text{ }\Omega$	26.5	27.9	29.3	
		R_{CLSA} or $R_{CLSB} = 63.4\text{ }\Omega$	38	39.9	42	
I_{AUTCLS}	Autoclass signature current	After t_{ACS} during 1st Class event	1		4	mA
V_{CL_ON}	Class lower threshold	V_{DD} rising, $I_{CLS} \uparrow$	11.9	12.5	13	V
V_{CL_H}		Hysteresis	1.4	1.6	1.7	
V_{CU_ON}	Class upper threshold	V_{DD} rising, $I_{CLS} \downarrow$	21	22	23	V
V_{CU_H}		Hysteresis	0.5	0.78	0.9	
V_{MSR}	Mark reset threshold	V_{DD} falling	3	3.9	5	V
	Mark state resistance	2-point measurement at 5 V and 10.1 V	6	10	12	k Ω
	Leakage current	$V_{DD} = 57\text{ V}$, $V_{CLS} = 0\text{ V}$, measure I_{CLS}			1	μA
t_{LCF_PD}	Long first class event timing	Class 1 st event time duration for new MPS	76	81.5	86	ms
t_{ACS}	Autoclass signature timing	AUTCLS During Class 1 st event	76	81.5	87	ms
	AUTCLS pullup current	$13\text{ V} \leq V_{DD} \leq 21\text{ V}$	30	34	38	μA
PASS DEVICE (RTN)						
$r_{DS(on)}$	On resistance	TPS2372-3		0.3	0.55	Ω
		TPS2372-4		0.1	0.2	
	Input bias current	$V_{DD} = V_{RTN} = 30\text{ V}$, measure I_{RTN}			50	μA
	RTN leakage current	$V_{DD} = V_{RTN} = 100\text{ V}$, $V_{DEN} = V_{VSS}$, measure I_{RTN}			80	
	Current limit	$V_{RTN} = 1.5\text{ V}$, TPS2372-3	1.55	1.85	2.2	A
		$V_{RTN} = 1.5\text{ V}$, TPS2372-4	1.9	2.2	2.5	
	Inrush current limit	$V_{RTN} = 2\text{ V}$, $V_{DD}: 20\text{ V} \rightarrow 48\text{ V}$, TPS2372-3	165	200	237	mA
		$V_{RTN} = 2\text{ V}$, $V_{DD}: 20\text{ V} \rightarrow 48\text{ V}$, TPS2372-4	275	335	395	
t_{INR_DEL}	Inrush termination	Percentage of inrush current	65%	90%	99%	ms
		Inrush delay	78	81.5	87	
	Foldback threshold	V_{RTN} rising	12.5	14.5	15.5	V
	Foldback deglitch time	V_{RTN} rising to when current limit changes to inrush current limit	1.35	1.65	1.95	ms
POWER GOOD (PG)						

Electrical Characteristics (continued)

Unless otherwise noted, $40\text{ V} \leq V_{DD} \leq 57\text{ V}$; $R_{DEN} = 24.9\text{ k}\Omega$; PG, CLSA, CLSB, MPS_DUTY, AMPS_CTL, IRSHDL_EN, TPH, TPL and $\overline{\text{BT}}$ open; $V_{AUTCLS} = V_{VSS}$; $R_{REF} = 49.9\text{ k}\Omega$; $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$. Positive currents are into pins. Typical values are at 25°C . All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output low voltage			Measure $V_{PG} - V_{RTN}$, $I_{PG} = 2\text{ mA}$, $V_{RTN} = 2\text{ V}$, V_{DD} : $20\text{ V} \rightarrow 48\text{ V}$			0.27	0.5	V
Leakage current			$V_{PG} = 57\text{ V}$, $V_{RTN} = 0\text{ V}$				10	μA
			$V_{PG} = 10\text{ V}$, $V_{RTN} = 0\text{ V}$				1	
PSE TYPE INDICATION (T _{PL} , T _{PH} , $\overline{\text{BT}}$)								
V _{TPL}	Output low voltage		I _{TPL} = 2 mA, after 2-, 3- or 5-event classification, startup has completed, $V_{RTN} = 0\text{ V}$			0.27	0.5	V
V _{TPH}	Output low voltage		I _{TPH} = 2 mA, after 4- or 5-event classification, startup has completed, $V_{RTN} = 0\text{ V}$			0.27	0.5	
V _{BT}	Output low voltage		I _{BT} = 2 mA, after IEEE802.3bt classification, startup has completed, $V_{RTN} = 0\text{ V}$			0.27	0.5	
Leakage current			V_{TPL} or V_{TPH} or $V_{BT} = 7\text{ V}$, $V_{RTN} = 0\text{ V}$				1	μA
t _{TPLHBT}	T _{PL} , T _{PH} , $\overline{\text{BT}}$ delay		From PG: Low \rightarrow open during startup to T _{PH} and/or T _{PL} and/or $\overline{\text{BT}}$ active		20	24	28	ms
UVLO								
V _{UVLO_R}	UVLO rising threshold		V _{VDD} rising		36.3	38.1	40	V
V _{UVLO_F}	UVLO falling threshold		V _{VDD} falling		30.5	32	33.6	
V _{UVLO_H}	UVLO hysteresis					6.1		V
BIAS CURRENT								
Operating current			40 V \leq V _{VDD} \leq 57 V, startup has completed			550	800	μA
MPS								
MPS DC supply current			Startup has completed, I _{RTN} = 0 mA				0.8	mA
AMPS_CTL pulsed voltage			Startup has completed, I _{RTN} < 20 mA, R _{MPS} = 1 k Ω to 12 k Ω		23.1	24	24.9	V
Automatic MPS falling current threshold			Startup has completed, I _{RTN} threshold to generate AMPS_CTL pulses		18	28	38	mA
			Hysteresis on RTN current		1			
MPS pulsed mode duty cycle for Type 1-2 PSE			MPS pulsed current duty cycle		25.8%	26.1%	26.4%	ms
			MPS pulsed current ON time		76	81.5	87	
			MPS pulsed current OFF time		230 250			
MPS pulsed mode duty cycle for Type 3-4 PSE			MPS pulsed current duty cycle, R _{MPS_DUTY} > 230 k Ω		5.2%	5.43%	5.6%	ms
			MPS pulsed current ON time, R _{MPS_DUTY} > 230 k Ω		14.5	15.0	15.7	
			MPS pulsed current duty cycle, R _{MPS_DUTY} < 8 k Ω		12.3%	12.5%	12.7%	ms
			MPS pulsed current ON time, R _{MPS_DUTY} < 8 k Ω		36	37.5	39	
			MPS pulsed current duty cycle, 43 k Ω < R _{MPS_DUTY} < 77 k Ω		7.9%	8.1%	8.3%	ms
			MPS pulsed current ON time, 43 k Ω < R _{MPS_DUTY} < 77 k Ω		22.2	23.1	24	
			MPS pulsed current OFF time, R _{MPS_DUTY} from 0 Ω to open circuit		250	263.5	277	ms
MPS_DUTY pullup current					14	17	20	μA

Electrical Characteristics (continued)

Unless otherwise noted, $40\text{ V} \leq V_{\text{DD}} \leq 57\text{ V}$; $R_{\text{DEN}} = 24.9\text{ k}\Omega$; PG, CLSA, CLSB, MPS_DUTY, AMPS_CTL, IRSHDL_EN, TPH, TPL and $\overline{\text{BT}}$ open; $V_{\text{AUTCLS}} = V_{\text{VSS}}$; $R_{\text{REF}} = 49.9\text{ k}\Omega$; $-40^\circ\text{C} \leq T_{\text{J}} \leq 125^\circ\text{C}$. Positive currents are into pins. Typical values are at 25°C . All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Shutdown	$T_{\text{J}} \uparrow$	140	158		$^\circ\text{C}$
Hysteresis ⁽¹⁾			20		$^\circ\text{C}$

(1) Parameters provided for reference only, and do not constitute part of TI published specifications for purposes of TI product warranty.

6.6 Typical Characteristics

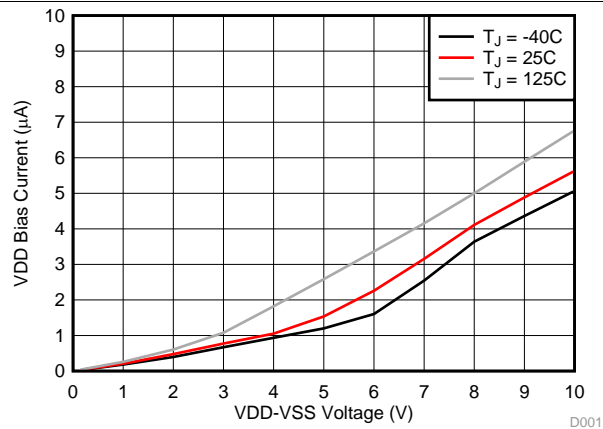


Figure 1. Detection Bias Current vs PoE Voltage

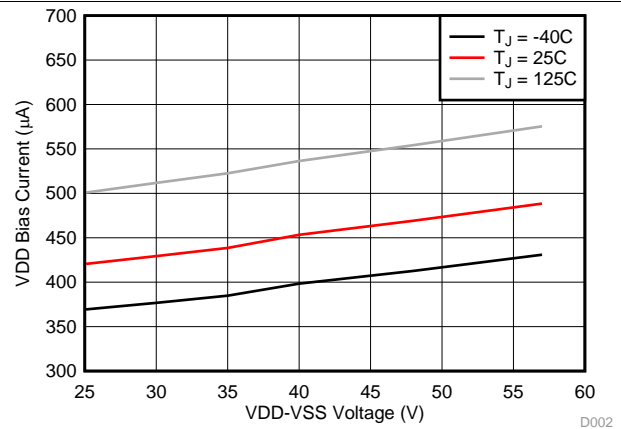


Figure 2. I_{VDD} Bias Current vs Voltage

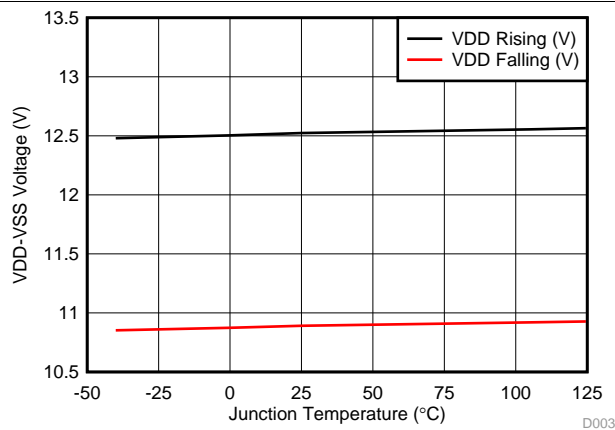


Figure 3. Classification Lower Threshold vs Temperature

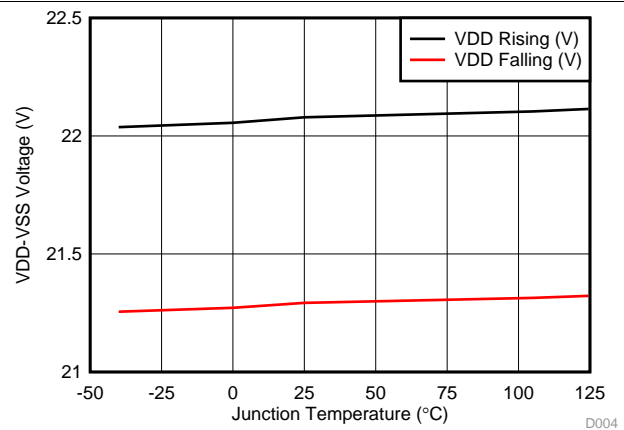


Figure 4. Classification Upper Threshold vs Temperature

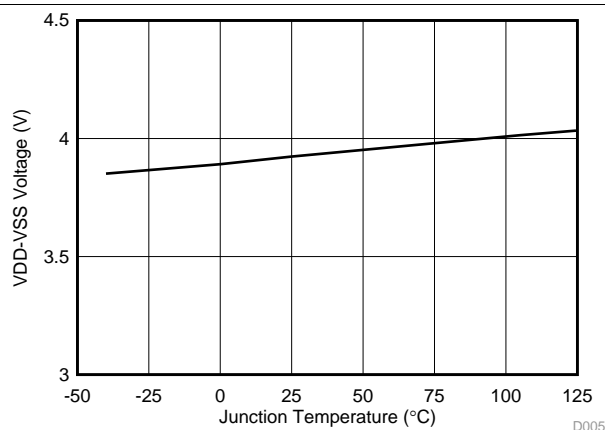


Figure 5. Mark Reset Threshold vs Temperature

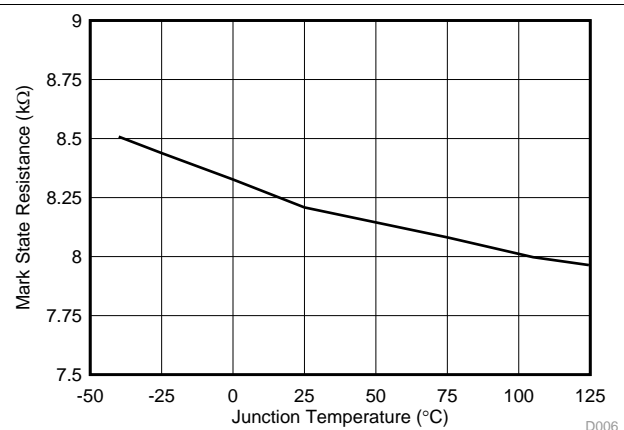


Figure 6. Mark Resistance vs Temperature

Typical Characteristics (continued)

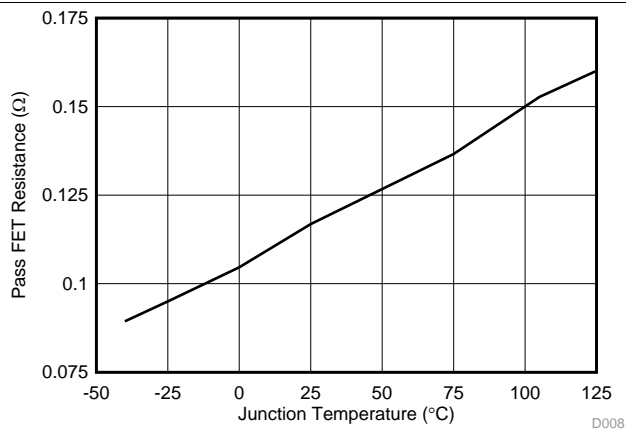


Figure 7. Pass FET Resistance vs Temperature, TPS2372-4

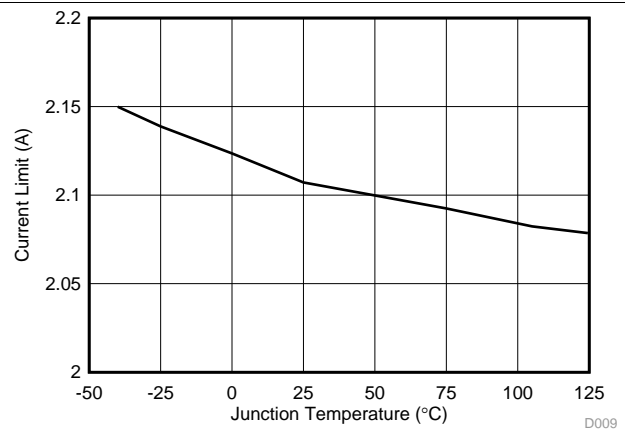


Figure 8. PoE Current Limit vs Temperature, TPS2372-4

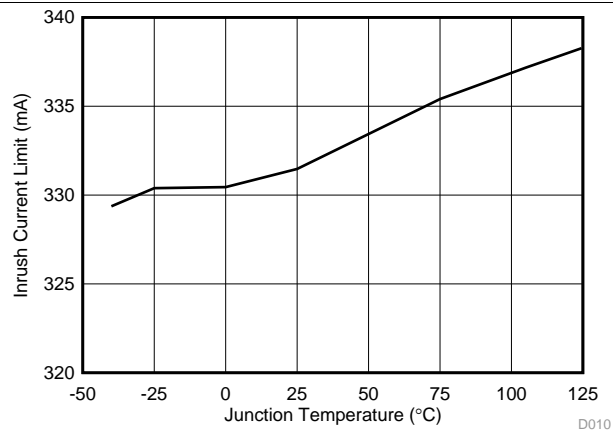


Figure 9. PoE Inrush Current Limit vs Temperature, TPS2372-4

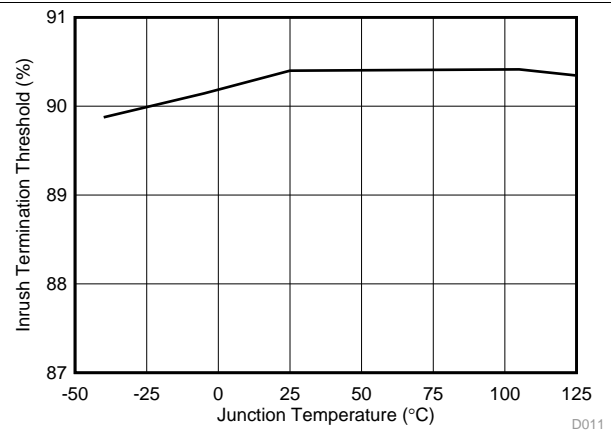


Figure 10. Inrush Termination Threshold vs Temperature, TPS2372-4

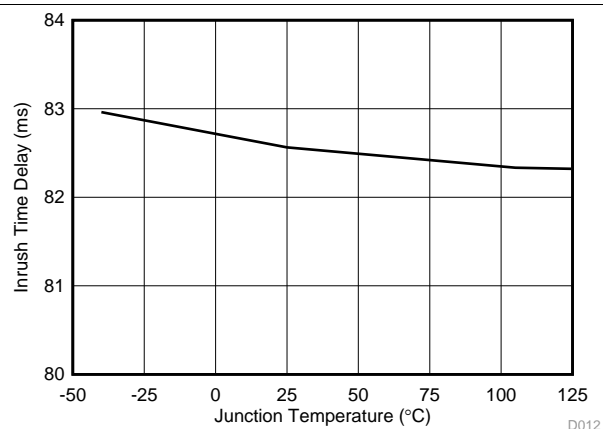


Figure 11. Inrush Time Delay vs Temperature

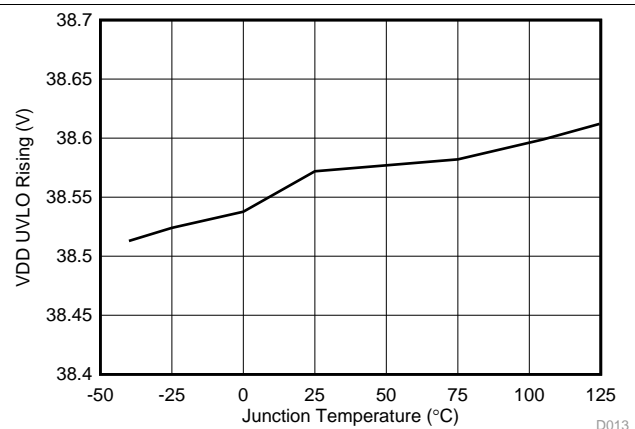


Figure 12. UVLO Rising Threshold vs Temperature

Typical Characteristics (continued)

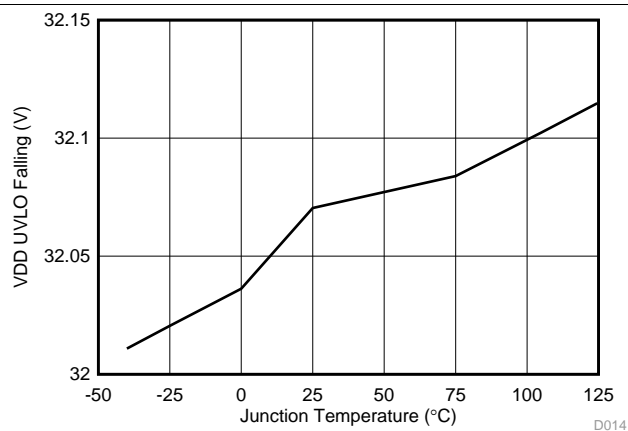


Figure 13. UVLO Falling Threshold vs Temperature

7 Detailed Description

7.1 Overview

The TPS2372 device is a 20-pin integrated circuit that contains all of the features needed to implement a single interface IEEE802.3bt Type-3 (TPS2372-3) and Type-4 (TPS2372-4) powered device (PD). Basic functionality supported includes Detection, Hardware Classification, and inrush current limit (200-mA for TPS2372-3 and 335-mA for TPS2372-4) during startup. Enhanced features include the automatic maintain power signature (MPS).

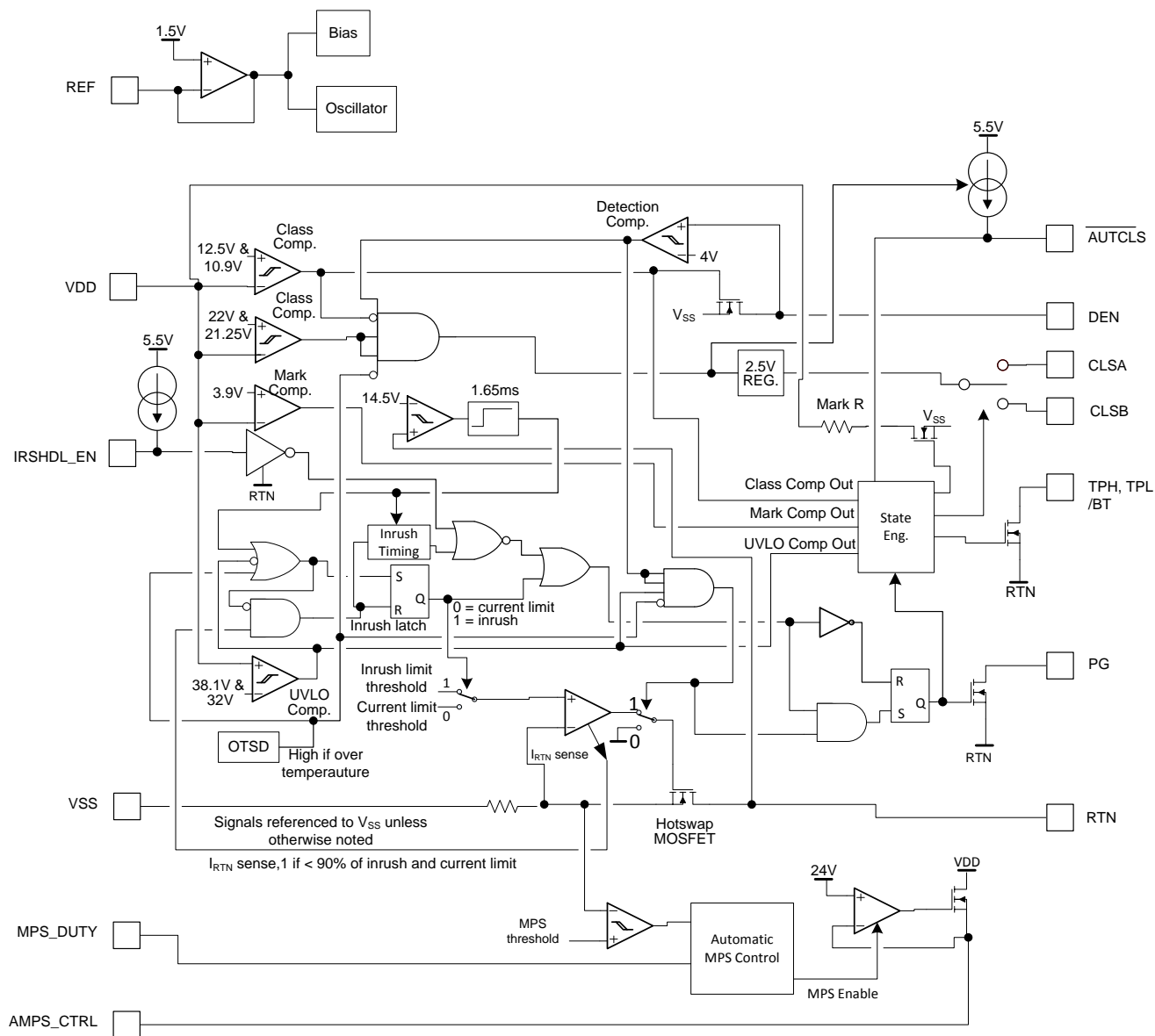
The TPS2372-3 integrates a low 0.3- Ω internal switch to support Type-3 applications up to 60 W of continuous power sourced by the PSE, allowing beyond 1.2 A (1.55 A minimum current limit) through the PD during normal operation.

Likewise, the TPS2372-4 integrates a low 0.1- Ω internal switch to support Type-4 applications up to 90 W of continuous power sourced by the PSE, allowing up to 1.9 A through the PD during normal operation.

The TPS2372 has a built-in inrush time delay period, for a simple solution to meet the IEEE802.3bt startup requirement.

The TPS2372 contains several protection features such as thermal shutdown, current limit foldback, and a robust 100-V internal switch.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PG Power Good (Converter Enable) Pin Interface

PG is an active high output that is pulled to RTN when the device is in inrush phase. It remains in a high impedance state at all other times. This pin is an open-drain output, and it may require a pullup resistor or other interface to the downstream load. PG may be left open if it is not used.

The PG pin can be used to inhibit downstream converter startup by keeping the soft-start pin low. [Figure 14](#) shows an example where PG connects to the SS pin of a DC-DC controller. Because PG is an open drain output, it will not affect the soft-start capacitor charge time when it deasserts. Another common use of the PG pin is to enable a converter with an active-high enable input. In this case, PG may require a pullup resistor to either VDD, or to a bias supply, depending on the requirements of the controller enable pin.

Feature Description (continued)

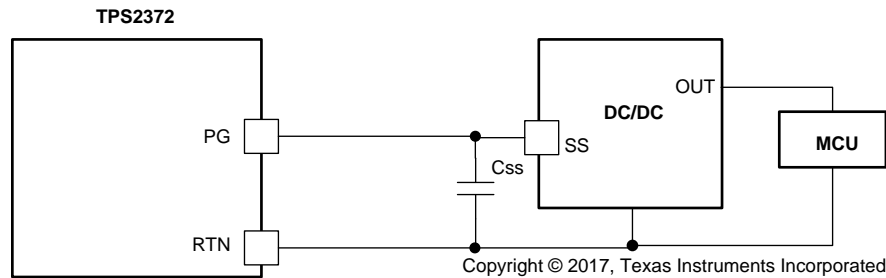


Figure 14. PG Interface

7.3.2 CLSA and CLSB Classification, AUTCLS

Each of the two external resistors (R_{CLSA} and R_{CLSB} in Figure 22) connected between the CLSA (first and second class event) and CLSB (third and any subsequent class event) pins and VSS provide a distinct classification signature to the PSE, and are used to define the power class requested by the PD. The controller places a voltage of approximately 2.5 V across CLSA (first or second class event) or CLSB (all additional class events) external resistor whenever the voltage differential between VDD and VSS lies from about 10.9 V to 22 V. The current drawn by each resistor, combined with the internal current drain of the controller and any leakage through the internal pass MOSFET, creates the classification signature current. Table 1 lists the external resistor values required for each of the PD power ranges defined by IEEE802.3bt. The number of classification cycles then determines how much power is allocated by the PSE. The maximum average power drawn by the PD, plus the power supplied to the downstream load, should not exceed the maximum power indicated in Table 1, as well as the maximum power allocated by the PSE based on the number of classification cycles.

Type 2 and Type 3 PSEs may perform two classification cycles if Class 4 signature is presented on the first cycle. Likewise, Type 3 and Type 4 PSEs may perform four classification cycles if Class 4 signature is presented on the first two cycles and Class 0 or 1 signature is presented on the third cycle. Also, Type 4 PSEs may perform five classification cycles if Class 4 signature is presented on the first two cycles and Class 2 or 3 signature is presented on the third cycle.

Table 1. Class Resistor Selection

PD Class	CLASS SIGNATURE A	CLASS SIGNATURE B	MINIMUM POWER AT PD (W)	MAXIMUM POWER AT PD (W)	NUMBER OF CLASS CYCLES @ MAX POWER	RESISTOR CLSA (Ω)	RESISTOR CLSB (Ω)
0	0	0	0.44	12.95	1	1210	1210
1	1	1	0.44	3.84	1	249	249
2	2	2	3.84	6.49	1	140	140
3	3	3	6.49	12.95	1	90.9	90.9
4	4	4	12.95	25.5	2,3	63.4	63.4
5	4	0	25.5	40	4	63.4	1210
6	4	1	40	51	4	63.4	249
7	4	2	51	62	5	63.4	140
8	4	3	62	71	5	63.4	90.9

The AUTCLS input is used to enable the Autoclass function during classification. When enabled, the class signature during the first class event drops to class 0 current level after a time t_{ACS} of the first class event, indicating to a Type 3 or 4 PSE that it supports Autoclass.

7.3.3 DEN Detection and Enable

DEN pin implements two separate functions. A resistor (R_{DEN} in Figure 22) connected between VDD and DEN generates a detection signature whenever the voltage differential between VDD and VSS lies from approximately 1.4 to 10.9 V. Beyond this range, the controller disconnects this resistor to save power. The IEEE 802.3bt standard specifies a detection signature resistance, R_{DEN} from 23.75 k Ω to 26.25 k Ω , or 25 k $\Omega \pm 5\%$. TI recommends a resistor of 24.9 k $\Omega \pm 1\%$ for R_{DEN} .

Pulling DEN to VSS during powered operation causes the internal hotswap MOSFET and class regulator to turn off. If the resistance connected between VDD and DEN is divided into two roughly equal portions, then the application circuit can disable the PD by grounding the tap point between the two resistances, while simultaneously spoiling the detection signature which prevents the PD from properly re-detecting.

7.3.4 Internal Pass MOSFET and Inrush Delay Enable, IRSHDL_EN

RTN pin provides the negative power return path for the load. Once V_{VDD} exceeds the UVLO threshold, the internal pass MOSFET pulls RTN to VSS. Inrush limiting prevents the RTN current from exceeding a nominal value of about 200 mA and 335 mA for the TPS2372-3 and TPS2372-4 respectively until the bulk capacitance (C_{BULK} in Figure 22) is fully charged. Two conditions must be met to reach the end of inrush phase. The first one is when the RTN current drops below about 90% of nominal inrush current at which point the current limit is changed to 1.85 A for TPS2372-3 and 2.2 A for TPS2372-4, while the second one, if IRSHDL_EN is open, is to ensure a minimum inrush delay period of ~81.5 ms (t_{INR_DEL}) from beginning of the inrush phase. The PG output becomes high impedance to signal the downstream load that the bulk capacitance is fully charged and the inrush period has been completed. Connecting IRSHDL_EN input to RTN pin disables the inrush delay, in which case only the first condition applies to reach the end of inrush phase.

If RTN ever exceeds about 14.5 V for longer than ~1.65 ms, then the TPS2372 returns to inrush phase; note that in this particular case, the second condition described above about inrush phase duration (81.5 ms) is not applicable.

7.3.5 TPH, TPL and \overline{BT} PSE Type Indicators

The state of \overline{BT} , TPH and TPL is used to provide information relative to the PSE Type (1-2 or 3-4) and its allocated power. Table 2 lists the encoding corresponding to various combinations of PSE Type, PD Class and allocated power. Table 3 also corresponds to cases where the PSE allocated power is lower than what the PD is requesting. The allocated power is determined by the number of classification cycles having been received. During startup, the TPH, TPL and \overline{BT} outputs are enabled typically 24 ms after PG went from low to open, to allow the power supply to reach a stable state first. These 3 outputs will return to a high-impedance state if the part enters thermal shutdown, or if VDD-to-VSS voltage falls below ~32 V. Note that in all these cases, as long as VDD-to-VSS voltage remains above the mark reset threshold, the internal logic state of these 3 signals is remembered such that these outputs will be activated accordingly after the startup has completed. This circuit resets when the VDD-to-VSS voltage drops below the mark reset threshold. The TPH, TPL and \overline{BT} pins can be left unconnected if not used.

Table 2. TPH, TPL, \overline{BT} and Allocated Power Truth Table

PSE Type	PD Class	NUMBER OF CLASS CYCLES	PSE ALLOCATED POWER AT PD (W)	TPH	TPL	$\overline{BT}^{(1)}$
1-2	0	1	12.95	HIGH	HIGH	HIGH
1-2	1	1	3.84	HIGH	HIGH	HIGH
1-2	2	1	6.49	HIGH	HIGH	HIGH
1-2	3	1	12.95	HIGH	HIGH	HIGH
2	4	2	25.5	HIGH	LOW	HIGH

(1) The BT output is not required to indicate how much power is allocated to the PD by a IEEE802.3bt compliant PSE. Additional information may be provided depending on the application described in the Application *Detailed Design Requirements* section [Opto-isolators for TPH, TPL and BT](#)

Table 2. TPH, TPL, \overline{BT} and Allocated Power Truth Table (continued)

PSE Type	PD Class	NUMBER OF CLASS CYCLES	PSE ALLOCATED POWER AT PD (W)	TPH	TPL	$\overline{BT}^{(1)}$
3-4	0	1	12.95	HIGH	HIGH	LOW
3-4	1	1	3.84	HIGH	HIGH	LOW
3-4	2	1	6.49	HIGH	HIGH	LOW
3-4	3	1	12.95	HIGH	HIGH	LOW
3-4	4	2-3	25.5	HIGH	LOW	LOW
3-4	5	4	40	LOW	HIGH	LOW
3-4	6	4	51	LOW	HIGH	LOW
4	7	5	62	LOW	LOW	LOW
4	8	5	71	LOW	LOW	LOW

Table 3. Power Demotion Cases

PSE Type	PD Class	NUMBER OF CLASS CYCLES	PSE ALLOCATED POWER AT PD (W)	TPH	TPL	\overline{BT}
3-4	4-8	1	12.95	HIGH	HIGH	LOW
3-4	5-8	2,3	25.5	HIGH	LOW	LOW
3-4	7-8	4	51	LOW	HIGH	LOW

7.3.6 AMPS_CTL, MPS_DUTY and Automatic MPS

To maintain PSE power, the AMPS_CTL output generates voltage pulses. This is translated into current pulses by connecting a resistor between AMPS_CTL and VSS. These pulses are automatically generated as long as the current through the RTN-to-VSS path is not high enough ($< \sim 28$ mA). Typical resistor value of 1.3 k Ω is recommended, in applications where the load current may go below ~ 20 mA and the PSE power has to be maintained.

If a Type 3 or 4 PSE is detected, the MPS_DUTY input can be used to select one out of three duty-cycles (5.4%, 8.1%, 12.5%). The selection is based on various system parameters, which include the amount of bulk capacitance, the input cable impedance and the type of input bridge. Also, inserting a blocking diode (or MOSFET) between the bulk capacitor and the TPS2372 allows the selection of a shorter MPS duty-cycle. [Table 4](#) should be used to select a proper MPS Duty Cycle.

Table 4. MPS Duty-Cycle Selection

PSE Type	MPS_DUTY	MPS Duty-Cycle
1,2	-	26%
3,4	Short to VSS	12.5%
3,4	Resistance (60.4K typ.) to VSS	8.1%
3,4	Open	5.4%

Table 5. System Conditions and MPS Duty-Cycle

Expected PoE PD System Conditions			MPS_DUTY Selection		
C_{BULK} Blocking Diode	C_{BULK}	Cable Length	MPS Duty-cycle	Pin Termination	I_{MPS} (mA)
Yes	Any	0 -100m	5.4% or longer	Open	18.5
No	$\leq 60 \mu F$		8.1% or longer	60 k Ω to VSS	18.5
No	$> 60 \mu F, \leq 120 \mu F$		12.5%	Short to VSS	18.5
No	$\leq 120 \mu F$		5.4% or longer ⁽¹⁾	Open	18.5
No	$> 120 \mu F, \leq 300 \mu F$		8.1% or longer ⁽¹⁾	60 k Ω to VSS	18.5

(1) Applicable when PSE voltage step-down events are unlikely or are not expected to exceed -0.4 V.

7.3.7 VDD Supply Voltage

VDD pin connects to the positive side of the input supply. It provides operating power to the PD controller and allows monitoring of the input line voltage. If V_{VDD} falls below its UVLO threshold and goes back above it, or if a thermal shutdown resumes while V_{VDD} is already above its UVLO threshold, the TPS2372 returns to inrush phase.

7.3.8 VSS

VSS pin is the input supply negative rail that serves as a local ground. The exposed thermal PAD must be connected to this pin to ensure proper operation.

7.3.9 Exposed Thermal PAD

The exposed thermal PAD is internally connected to VSS pin. It should be tied to a large VSS copper area on the PCB to provide a low resistance thermal path to the circuit board. TI recommends maintaining a clearance of 0.025" between VSS and high-voltage signals such as VDD.

7.4 Device Functional Modes

7.4.1 PoE Overview

The following text is intended as an aid in understanding the operation of the TPS2372 but not as a substitute for the IEEE 802.3bt standard. The pending IEEE 802.3bt standard is an update to IEEE 802.3-2012 clause 33 (PoE), adding 4-pair power, high-power options, additional features and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2012 is referred to as a Type 1 (Class 0-3) or 2 (Class 4) device, and devices with higher power and enhanced classification will be referred to as Type 3 (Class 5,6) or 4 (Class 7,8) devices. Type 3 devices will also include Class 0-4 devices that are 4-pair capable. Standards change and should always be referenced when making design decisions.

The IEEE 802.3bt standard defines a method of safely powering a PD (powered device) over a cable by power sourcing equipment (PSE), and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. There is also a fourth operational state used by Type 3 and 4 PSEs, called "connection check", to determine if the PD has same (single interface) or independent (dual interface or commonly referred to "dual-signature" in the IEEE802.3bt standard) classification signature on each pairset. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection, and also includes connection check if Type 3 or 4 PSE. The low power levels used during detection and connection check are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE may inquire how much power the PD requires; this is referred to as classification. The PSE may then power the PD if it has adequate capacity.

Device Functional Modes (continued)

Type 3 or Type 4 PSEs are required to do an enhanced hardware classification of Type 3 or 4 respectively. Type 2 PSEs are required to do Type 1 hardware classification plus a data-layer classification, or an enhanced Type 2 hardware classification. Type 1 PSEs are not required to do hardware or data link layer (DLL) classification. A Type 3 or Type 4 PD must do respectively Type 3 or Type 4 hardware classification as well as DLL classification. A Type 2 PD must do Type 2 hardware classification as well as DLL classification. The PD may return the default, 13-W current-encoded class, or one of four other choices if Type 2, one of six other choices if Type 3, and one of eight other choices if Type 4. DLL classification occurs after power-on and the Ethernet data link has been established.

The Autoclass function is optional for both the PSE and the PD.

Once started, the PD must present a maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 15 shows the operational states as a function of PD input voltage.

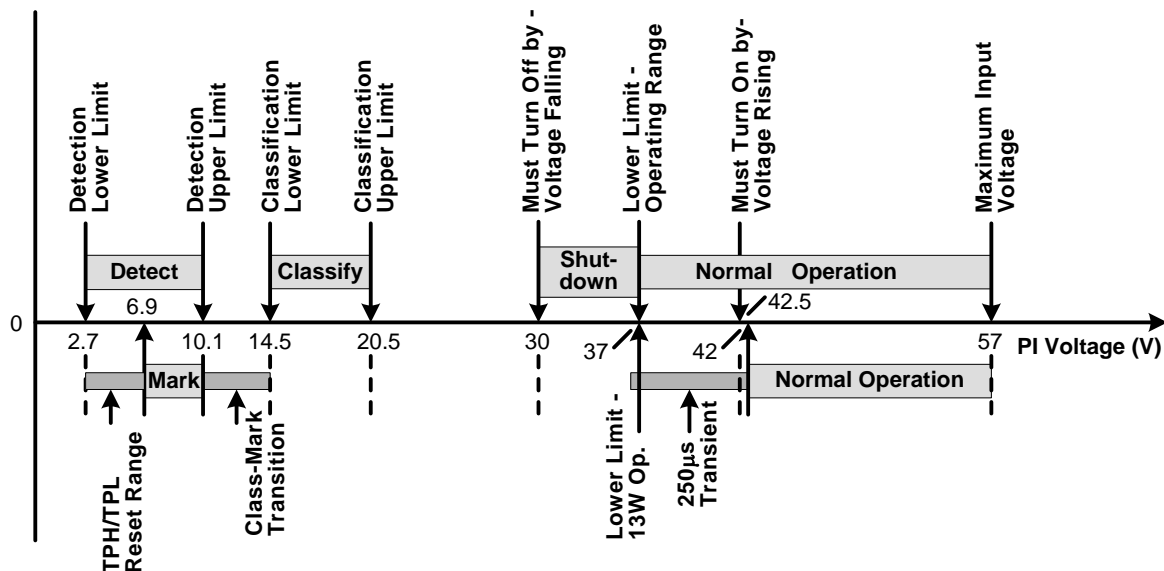


Figure 15. Operational States

The PD input, typically an RJ-45 eight-lead connector, is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops and operating margin. The standard allots the maximum loss to the cable regardless of the actual installation to simplify implementation. IEEE 802.3-2008 was designed to run over infrastructure including ISO/IEC 11801 class C (CAT3 per TIA/EIA-568) that may have had AWG 26 conductors. IEEE 802.3at Type 2 and IEEE 802.3bt Type 3 cabling power loss allotments and voltage drops have been adjusted for 12.5-Ω power loops per ISO/IEC11801 class D (CAT5 or higher per TIA/EIA-568, typically AWG 24 conductors). Table 6 shows key operational limits broken out for the two revisions of the standard.

Table 6. Comparison of Operational Limits

STANDARD	POWER LOOP RESISTANCE (MAX)	PSE OUTPUT POWER (MIN)	PSE STATIC OUTPUT VOLTAGE (MIN)	PD INPUT POWER (MAX)	STATIC PD INPUT VOLTAGE	
					POWER ≤ 13 W	POWER > 13 W
IEEE802.3-2012 802.3at (Type 1)	20 Ω	15.4 W	44 V	13 W	37 V – 57 V	N/A
802.3bt (Type 3)	12.5 Ω		50 V			
802.3at (Type 2) 802.3bt (Type 3)	12.5 Ω	30 W	50 V	25.5 W	37 V – 57 V	42.5 V – 57 V
802.3bt (Type 3)	6.25 Ω (4-pair)	60 W	50 V	51 W	N/A	42.5 V – 57 V
802.3bt (Type 4)	6.25 Ω (4-pair)	90 W	52 V	71.3 W	N/A	41.2 V – 57 V

The PSE can apply voltage either between the RX and TX pairs (pins 1–2 and 3–6 for 10baseT or 100baseT), or between the two spare pairs (4–5 and 7–8). Power application to the same pin combinations in 1000/2.5G/5G/10GbaseT systems is recognized in IEEE 802.3bt. 1000/2.5G/5G/10GbaseT systems can handle data on all pairs, eliminating the spare pair terminology. Type 1 and 2 PSEs are allowed to apply voltage to only one set of pairs at a time, while Type 3 and 4 PSEs may apply power to one or both sets of pairs at a time. The PD uses input diode or active bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS2372 specifications.

A compliant Type 2, 3 or 4 PD has power management requirements not present with a Type 1 PD. These requirements include the following:

1. Must interpret respectively Type 2, 3 or 4 hardware classification.
2. Must present hardware Class 4 during the first two classification events, applicable to Type 2 and 4 PDs, as well as to Type 3 PD with Class level 4 or higher.
3. If Type 3 or 4 single interface PD, it must present hardware Class in the range of 0 to 3 during the third and any subsequent classification events.
4. Must implement DLL negotiation.
5. Must behave like a Type 1 PD for 50 ms then must draw less than 400 mA until 80 ms after the PSE applies operation voltage (power up), if Type 2 or 3 single interface PD. This covers the PSE inrush period, which is 75 ms maximum.
6. Should behave like a Type 1 PD for 50 ms then must draw less than 400 mA until 80 ms after the PSE applies operation voltage (power up), if Type 4 single interface PD.
7. Must not draw more than 60 mA and 5 mA any time the input voltage falls below respectively 30 V and 10 V.
8. Must not draw more than 13 W if it has not received at least a Type 2 hardware classification or received permission through DLL.
9. Must not draw more than 25.5 W if it has not received at least 4 classification events or received permission through DLL.
10. Must not draw more than 51 W if it has not received at least 5 classification events or received permission through DLL.
11. Must meet various operating and transient templates.
12. Optionally monitor for the presence or absence of an adapter (assume high power).

As a result of these requirements, the PD must be able to dynamically control its loading, and monitor TPL and TPH for changes. In cases where the design needs to know specifically if an adapter is plugged in and operational, the adapter should be individually monitored, typically with an optocoupler.

7.4.2 Threshold Voltages

The TPS2372 has a number of internal comparators with hysteresis for stable switching between the various states. [Figure 16](#) relates the parameters in [Electrical Characteristics](#) to the PoE states. The mode labeled Idle between Classification and Operation implies that the DEN, CLSA, CLSB, and RTN pins are all high impedance. The state labeled Mark, which is drawn in dashed lines, is part of the Type 2-3-4 hardware class state machine.

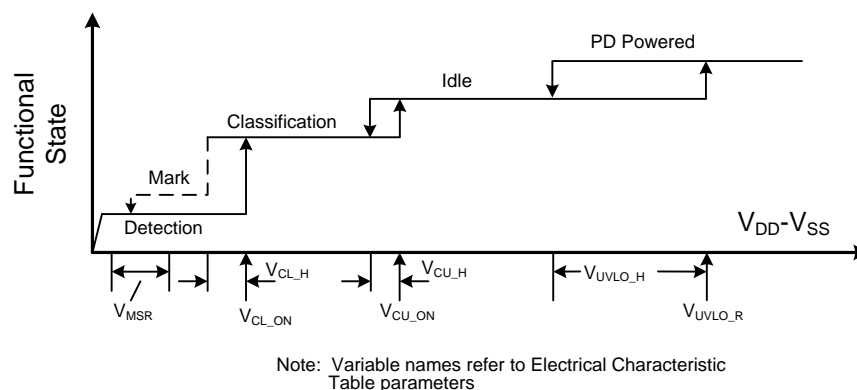


Figure 16. Threshold Voltages

7.4.3 PoE Startup Sequence

The waveforms of [Figure 17](#) demonstrate detection, classification including Autoclass during the first class event, and startup from a PSE with Type 3 Class 6 hardware classification. The key waveforms shown are $V_{(VDD-VSS)}$, $V_{(RTN-VSS)}$ and I_{PI} . IEEE 802.3bt requires a PSE allocating Class 6 level of power to generate a minimum of two detection levels, four class and mark cycles, and startup from the fourth mark event. As shown below, the required minimum duration of the first class event has been extended for Type 3 and 4 PSEs. V_{RTN} to V_{SS} falls as the TPS2372 charges C_{BULK} following application of full voltage. In [Figure 19](#), assertion of the PG signal is delayed and used to enable load current as seen in the I_{PI} waveform.

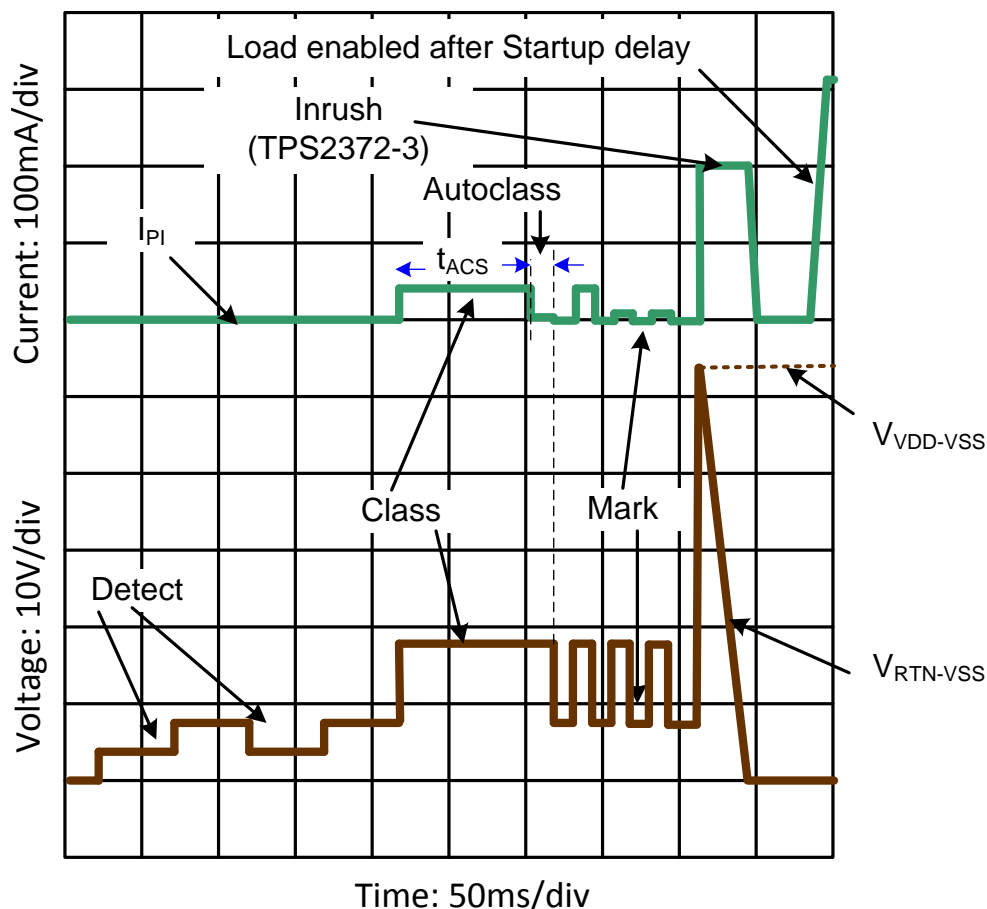


Figure 17. Startup of Class 6 PD

7.4.4 Detection

The TPS2372 pulls DEN to V_{SS} whenever $V_{(VDD-VSS)}$ is below the lower classification threshold. When the input voltage rises above V_{CL_ON} , the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, and almost all the internal circuits are disabled. An R_{DEN} of 24.9 k Ω ($\pm 1\%$), presents the correct signature. It may be a small, low-power resistor because it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance ($\Delta V / \Delta I$) from 23.7 k Ω to 26.3 k Ω at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and internal V_{DD} loading. The input diode bridge's incremental resistance may be hundreds of Ω at the low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially compensated by the TPS2372 effective resistance during detection.

The hardware classification protocol of IEEE 802.3bt specifies that a Type 2, 3 or 4 PSE drops its output voltage into the detection range during the classification sequence. The PD is required to have an incorrect detection signature in this condition, which is referred to as a mark event (see [Figure 17](#)). After the first mark event, the TPS2372 will present a signature less than 12 k Ω until it has experienced a $V_{(VDD-VSS)}$ voltage below the mark reset threshold (V_{MSR}). This is explained more fully under [Hardware Classification](#).

7.4.5 Hardware Classification

Hardware classification allows a PSE to determine a PD's power requirements before powering, and helps with power management once power is applied. Type 2, 3, and 4 hardware classification permits high power PDs to determine whether the PSE can support its high-power operation. The number of class cycles generated by the PSE prior to turn on indicates to the PD if it allots the power requested or if the allocated power is less than requested, in which case there is power demotion as shown in

Table 3. A Type 2 PD always presents Class 4 in hardware to indicate that it is a 25.5W device. A Class 5 or 6 Type 3 PD presents Class 4 in hardware during the first two class events and it presents Class 0 or 1, respectively, for all subsequent class events. A Class 7 or 8 Type 4 PD presents Class 4 in hardware during the first two class events and it presents Class 2 or 3, respectively, for all subsequent class events. A Type 1 PSE will treat a Class 4 to 8 device like a Class 0 device, allotting 13 W if it chooses to power the PD. A Type 2 PSE will treat a Class 5 to 8 device like a Class 4 device, allotting 25.5W if it chooses to power the PD. A Class 4 PD that receives a 2-event class, a Class 5 or 6 PD that receives a 4-event class, or a Class 7 or 8 PD that receives a 5-event class, understands that the PSE has agreed to allocate the PD requested power. In the case where there is power demotion, the PD may choose to not start, or to start while not drawing more power than initially allocated, and request more power through the DLL after startup. The standard requires a Type 2, 3 or 4 PD to indicate that it is underpowered if this occurs. Startup of a high-power PD at lower power than requested implicitly requires some form of powering down sections of the application circuits.

The maximum power entries in [Table 1](#) determine the class the PD must advertise. The PSE may disconnect a PD if it draws more than its stated class power, which may be the hardware class or a DLL-derived power level. The standard permits the PD to draw limited current peaks that increase the instantaneous power above the [Table 1](#) limit; however, the average power requirement always applies.

The TPS2372 implements one- to five-event classification. R_{CLSA} and R_{CLSB} resistor values define the class of the PD. DLL communication is implemented by the Ethernet communication system in the PD and is not implemented by the TPS2372.

The TPS2372 disables classification above V_{CU_ON} to avoid excessive power dissipation. CLSA/B voltage is turned off during PD thermal limiting or when DEN is active. The CLSA and CLSB outputs are inherently current-limited, but should not be shorted to V_{SS} for long periods of time.

Figure 18 shows how classification works for the TPS2372. Transition from state-to-state occurs when comparator thresholds are crossed (see [Figure 15](#) and [Figure 16](#)). These comparators have hysteresis, which adds inherent memory to the machine. Operation begins at idle (unpowered by PSE) and proceeds with increasing voltage from left to right. A 2- to 5-event classification follows the (heavy lined) path towards the bottom, ending up with a latched TPL/TPH decode along the lower branch that is highlighted. Once the valid path to the PSE detection is broken, the input voltage must transition below the mark reset threshold to start anew.

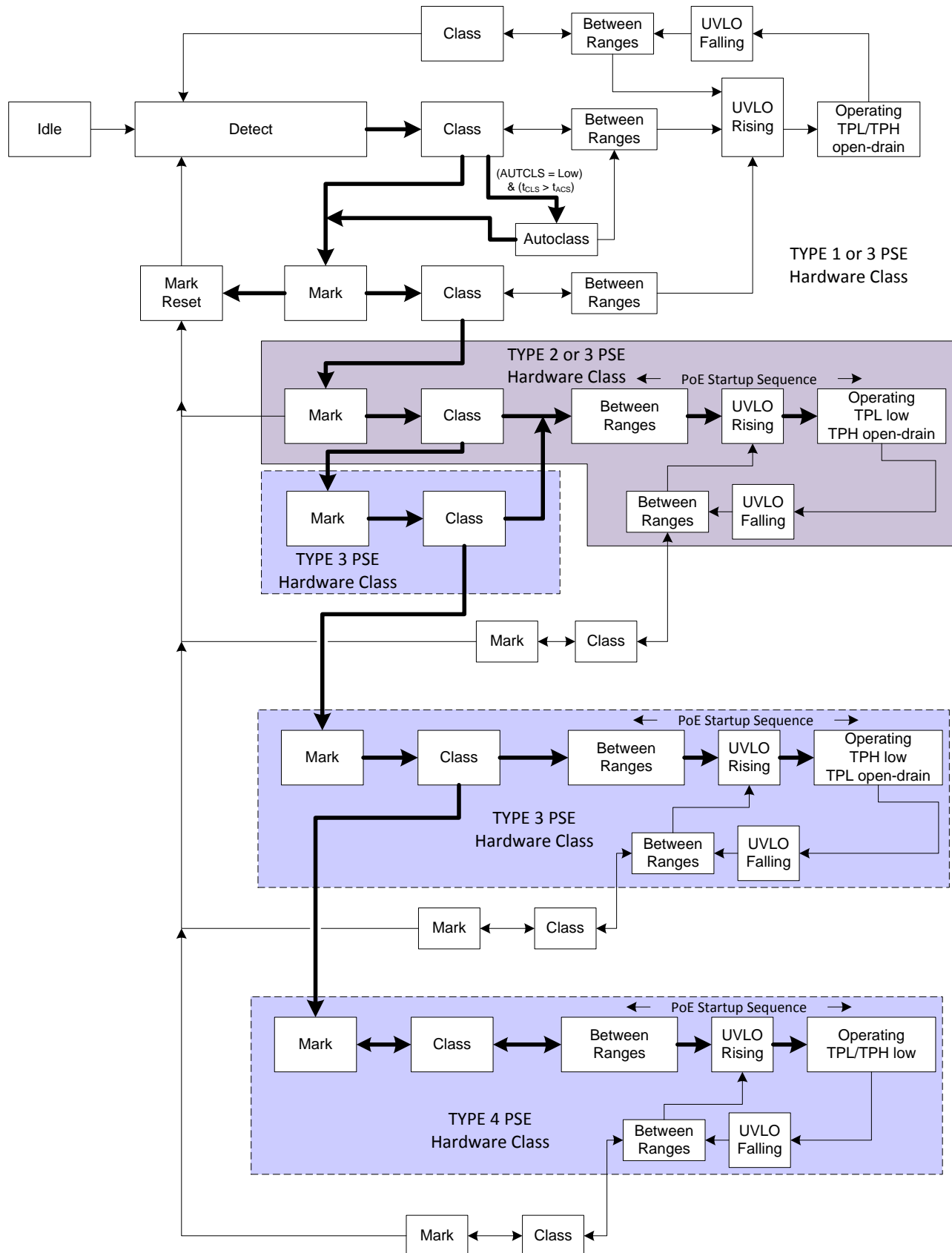


Figure 18. Up to Five-Event Class Internal States

7.4.6 Autoclass

Autoclass is a classification mechanism that allows a PD to communicate its effective maximum power consumption to the PSE. This happens in such a way that the PSE will be able to set the power budget to the effective maximum PD power including the effective channel losses and additional margin. This new feature was introduced in the IEEE802.3bt standard to allow a more efficient use of the available power since only the effectively used power needs to be budgeted.

A Type 3 or Type 4 PD may optionally support Autoclass whereas a Type 3 or Type 4 PSE may make use of it to optimize its power management.

A PSE implementing Autoclass uses the first class event to inquire if the PD supports Autoclass, looking for the class current to fall to class 0 current level after a time t_{ACS} , as shown in [Figure 17](#). If it is the case, the PSE can then proceed to Autoclass measurement immediately after power up, the PD being required to draw its highest power throughout the period bounded by the next 1.35 second to 3.65 seconds. Note that the average power is calculated using any sliding window with a width in the range of 150 to 300 ms.

7.4.7 Inrush and Startup

IEEE 802.3bt has a startup current and time limitation, providing compatibility between a PSE of any Type and a PD of any Type. The PSE inrush limit varies according to the allotted power. If Class 0 to 4, Class 5 to 6 or Class 7 to 8, the inrush limit is respectively from 400 mA to 450 mA, 400 mA to 900 mA or 800 mA to 900 mA. PSE inrush limit applies for up to 75 ms after power up (applying "48 V" to the PI), after which the Type 2, 3, or 4 PSE will support a higher output current in accordance with the allocated class. The TPS2372-3 and TPS2372-4 respectively implement a 200-mA and 335-mA inrush current, which is compatible with all PSE Types. A high-power PD must limit its converter startup peak current. The operational current for Type 2 and 3, and preferably Type 4, cannot exceed 400 mA for a period of 80 ms.

7.4.8 Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. For a Type 1 or Type 2 PD, a valid MPS consists of a minimum dc current of 10 mA, or a 10-mA pulsed current for at least 75 ms every 325 ms, and an AC impedance lower than 26.3 k Ω in parallel with 0.05 μ F. Only Type 1 and Type 2 PSEs monitor the AC MPS. A Type 1 or Type 2 PSE that monitors only the AC MPS may remove power from the PD.

To enable applications with stringent standby requirements, IEEE802.3bt introduced a significant change regarding the minimum pulsed current duration to assure the PSE will maintain power. This applies to all Type 3 and Type 4 PSEs, and the pulse duration is ~10% of what is required for Type 1 and 2 PSEs. The MPS current amplitude requirement for Class 5-8 PDs have also increased to 16 mA at the PSE end of the ethernet cable.

If the current through the RTN-to-VSS path is below ~28 mA, the TPS2372 automatically generates the MPS pulsed current through the AMPS_CTL output pin, the current amplitude being adjustable with an external resistor. The TPS2372 is also able to determine if the PSE is of Type 1-2 or Type 3-4, automatically adjusting the MPS pulse duration and duty-cycle. Note that the IEEE802.3bt requirement for the PD is applicable at the PSE end of the cable. That means that depending on the cable length and other parameters including the bulk capacitance, a longer MPS duration may be required to ensure a valid MPS. For that purpose, the TPS2372 has 3 different selections of MPS pulse duration and duty-cycle, selectable through the MPS_DUTY input pin.

When DEN is used to force the hotswap switch off, the DC MPS will not be met. A PSE that monitors the DC MPS will remove power from the PD when this occurs.

7.4.9 Startup and Converter Operation

The internal PoE UVLO (Undervoltage Lock Out) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the downstream converter circuits from loading the PoE input during detection and classification. The converter circuits will discharge C_{BULK} while the PD is unpowered. Thus $V_{(VDD-RTN)}$ will be a small voltage just after full voltage is applied to the PD, as seen in [Figure 17](#). The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{VDD} rises above the UVLO turn-on threshold (V_{UVLO_R} , approximately 38 V) with RTN high, the TPS2372-3 and TPS2372-4 enables the hotswap MOSFET with inrush current limit (~200 mA for TPS2372-3 and ~335 mA for TPS2372-4) as seen in [Figure 19](#). The PG

pin is in low state while C_{BULK} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS} . PG output is maintained low during that time, to avoid additional loading between V_{VDD} and V_{RTN} that could prevent successful PD and subsequent converter start up. Once the inrush current falls about 10% below the inrush current limit, the PD current limit switches to the operational level (approximately 1.85 A for TPS2372-3 and approximately 2.2 A for TPS2372-4).

Additionally, as seen in [Figure 19](#) once the inrush period duration has also exceeded ~81.5 ms, if IRSHDL_EN is open (this delay does not apply if connect to RTN), PG output becomes high impedance, allowing the downstream converter circuitry to start. In typical lighting applications, this allows a low power converter to start powering a microcontroller, which subsequently turns ON a high power LED driver. As seen in [Figure 20](#), the converter soft-start introduces a slight additional delay before the transition to a higher power mode. TPH, TPL and BT outputs are enabled within t_{TPLHBT} following PG going from low to open.

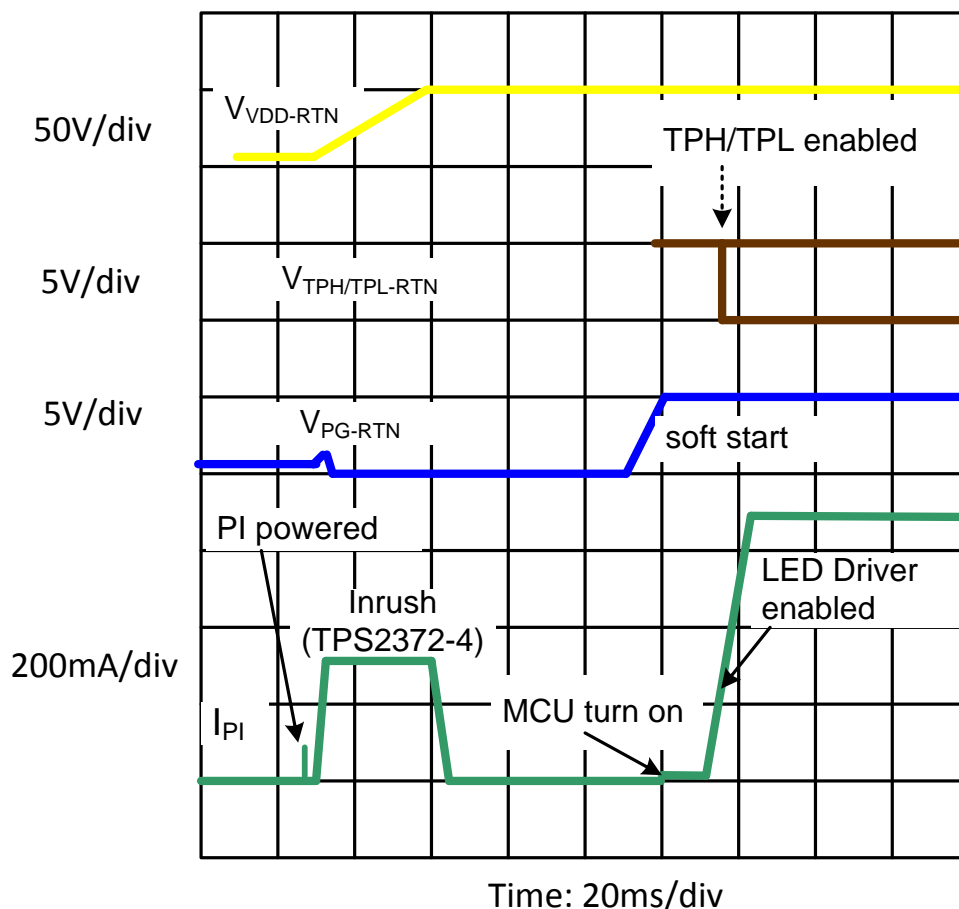


Figure 19. Power Up and Start

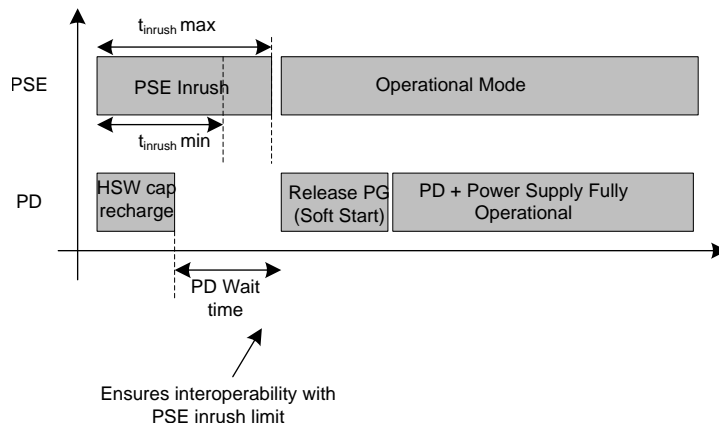


Figure 20. Power Up and Start

If $V_{DD}-V_{SS}$ drops below the lower PoE UVLO (V_{UVLO_F} , ~32 V), the hotswap switch is turned off, but the PG output remains high impedance allowing the converter to continue operating until the converter's UVLO threshold is reached.

7.4.10 PD Hotswap Operation

IEEE802.3bt includes new PSE output limiting requirements for Type 3 and 4 operation to cover higher power and 4-pair applications. Type 2, 3 and 4 PSEs must meet an output current vs time template with specified minimum and maximum sourcing boundaries. The peak output current per each 2-pair may be as high as 50 A for 10 μ s or 1.75 A for 75 ms, and the total peak current becomes twice these values when power is delivered over 4 pairs. This makes robust protection of the PD device even more important than it was in IEEE 802.3-2012.

The internal hotswap MOSFET is protected against output faults and input voltage steps with a current limit and deglitched (time-delay filtered) foldback. An overload on the pass MOSFET engages the current limit, with $V_{(RTN-VSS)}$ rising as a result. If $V_{(RTN-VSS)}$ rises above approximately 14.5 V for longer than approximately 1.65 ms, the current limit reverts to the inrush value and PG output is forced low which turns off the converter, although there is no minimum inrush delay period (81.5-ms) applicable in this case. The 1.65-ms deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 21 shows an example of the RTN current profile during V_{DD} to RTN short circuit, using 5-ohm load impedance. The hotswap MOSFET goes into current limit, causing the RTN voltage to increase. Once V_{RTN} exceeds 14.5 V, I_{RTN} , which was clamped to the current limit drops to the level of inrush current limit after 1.65 ms.

The inrush current limit is also reestablished when $V_{(VDD-VSS)}$ drops below UVLO then rises above it.

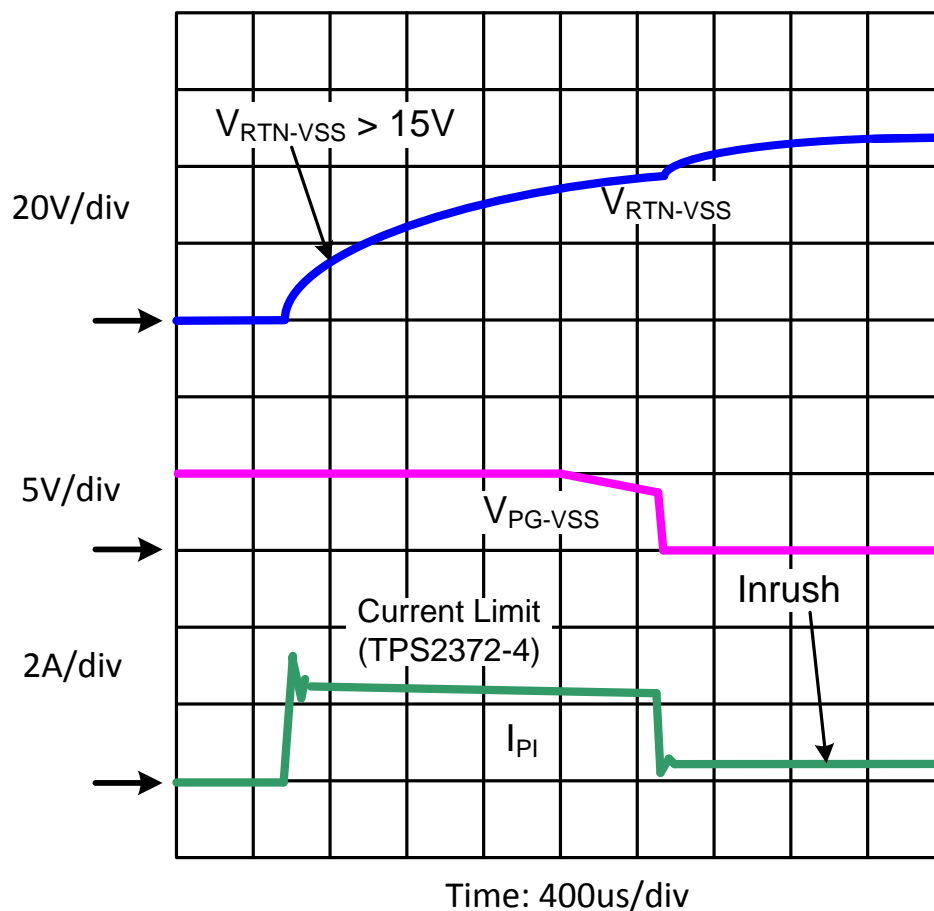


Figure 21. Response to PD Output Short Circuit

The PD control has thermal sensors that protect the internal hotswap MOSFET and the MPS pulsed current driver. Conditions like startup or operation into a V_{DD} -to-RTN short cause high power dissipation in the MOSFET. An over-temperature shutdown (OTSD) turns off the hotswap MOSFET, the class regulator, and the MPS driver, which are restarted after the device cools. The hotswap MOSFET will be re-enabled and the TPS2372 will return to inrush phase when exiting from an overtemperature event. Pulling DEN to VSS during powered operation causes the internal hotswap MOSFET to turn off.

The hotswap switch will be forced off under the following conditions:

1. $V_{(DEN-VSS)} < V_{PD-DIS}$ when $V_{(VDD-VSS)}$ is in the operational range,
2. PD is over-temperature, or
3. $V_{(VDD-VSS)} < \text{PoE UVLO falling threshold (approximately 32 V)}$.

7.4.11 Startup and Power Management, PG and TPH, TPL, \overline{BT}

PG (power good or converter enable) is a pin that when at low level indicates when the internal hotswap MOSFET is in inrush phase. PG goes high impedance when inrush phase is over and can be used to enable a downstream converter to start up. Common interfaces to the converter controller include the soft-start or enable pins.

TPH, TPL and \overline{BT} provide information relative to the PSE Type (1-2 or 3-4) and its allocated power.

The usage of TPH/TPL/ \overline{BT} is demonstrated in [Figure 22](#).

The TPS2372 is also able to interoperate with non standard PoE++ PSE controllers. If powered from a PoE++ PSE controller, the TPH/TPL/ \overline{BT} 3-bit code becomes "Low-Low-High". This also indicates that the PoE++PSE agreed to deliver the power requested by the TPS2372.

7.4.12 Using DEN to Disable PoE

The DEN pin may be used to turn the PoE hotswap switch off by pulling it to V_{SS} while in the operational state, or to prevent detection when in the idle state. A low voltage on DEN forces the hotswap MOSFET off during normal operation. Additional information is available in the *Advanced Adapter ORing Solutions* using the TPS23753 (SLVA306) application report.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS2372 has the flexibility to be implemented in IEEE802.3bt and PoE++ PDs. Therefore, it can be used in a wide range applications such as video and VoIP telephones, multiband access points, security cameras, power modules, LED lighting converters, and pico-base stations.

8.2 Typical Application

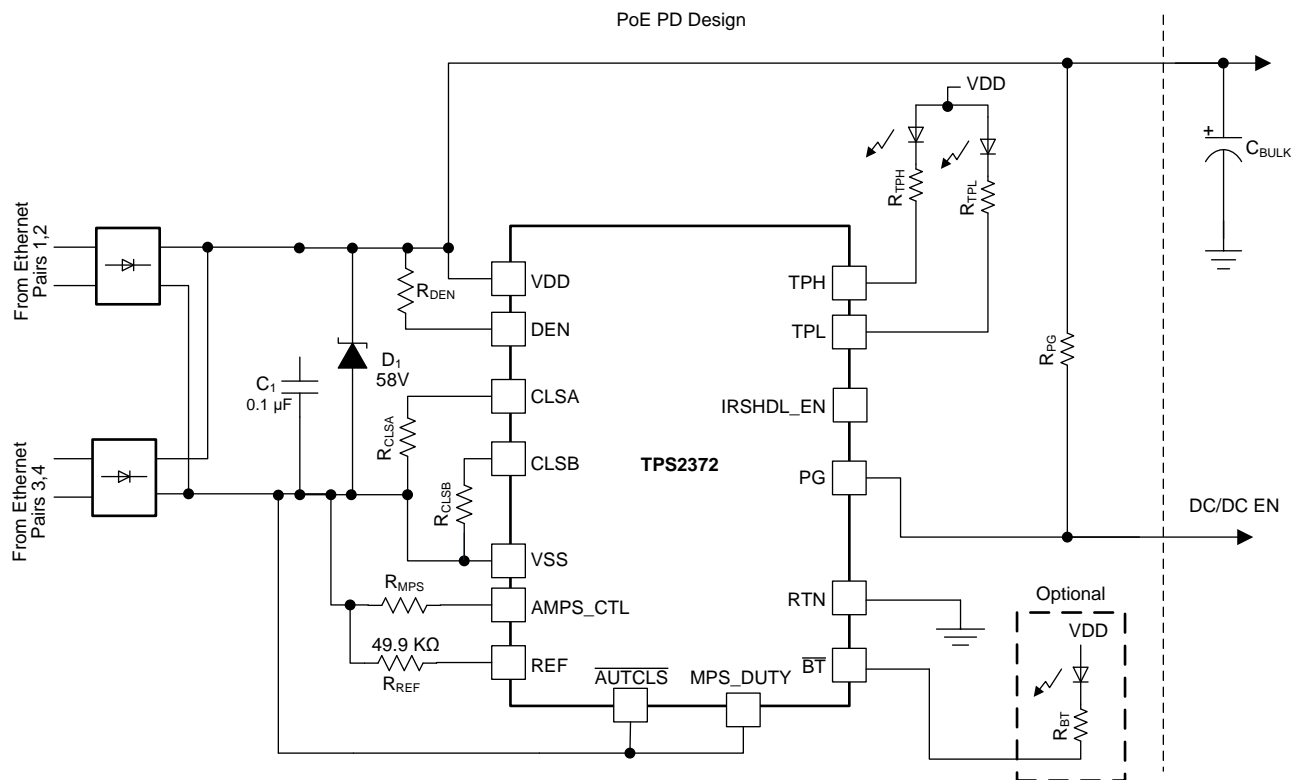


Figure 22. Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters in [Table 7](#) for a PD Class 8 application.

Table 7. Design Parameters

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
POWER INTERFACE				
Input voltage	Power applied through PoE or adapter	0	57	V
Operating voltage	After startup	30	57	V
Input UVLO	Rising input voltage at device terminals	—	40	V
	Falling input voltage	30.5	—	
Detection voltage	At device terminals	1.4	10.1	V
Classification voltage	At device terminals	11.9	23	V
PD class 8	Class signature A	38	42	mA
PD class 8	Class signature B	26.5	29.3	mA
Inrush current limit		275	395	mA
Operating current-limit		1.9	2.5	A
Autoclass		Yes		
Automatic MPS	12.5% Duty Cycle at no load			
Inrush delay		Yes	Yes	

8.2.2 Detailed Design Requirements

8.2.2.1 Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges will reduce the power dissipation in these devices by about 30%. There are, however, some things to consider when using them. The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100-k Ω resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. To compensate, use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges.

Schottky diode leakage currents and lower dynamic resistances can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing R_{DET} slightly may also help meet the requirement.

Schottky diodes have proven less robust to the stresses of ESD transients than PN junction diodes. After exposure to ESD, Schottky diodes may become shorted or leak. Take care to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

As a general recommendation, use 3-A to 5-A, 100-V rated discrete or bridge diodes for the input rectifiers.

Many high power PoE PD designs require the need for an active FET bridge rectifier in high efficiency applications. An example of an active FET bridge rectifier design can be found in the TPS2372-4EVM-006 User's Guide.

8.2.2.2 Protection, D_1

A TVS, D_1 , across the rectified PoE voltage per [Figure 22](#) must be used. TI recommends a SMAJ58A, or equivalent, is recommended for general indoor applications. If an adapter is connected from V_{DD} to RTN, as in ORing option 2 above, then voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

8.2.2.3 Capacitor, C_I

The IEEE 802.3at standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 μF to 0.12 μF . Typically a 0.1 μF , 100 V, 10% ceramic capacitor is used.

8.2.2.4 Detection Resistor, R_{DEN}

The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} between 23.7 k Ω and 26.3 k Ω , or 25 k $\Omega \pm 5\%$. A resistor of 24.9 k $\Omega \pm 1\%$ is recommended for R_{DEN} .

8.2.2.5 Classification Resistors, R_{CLSA} and R_{CLSB}

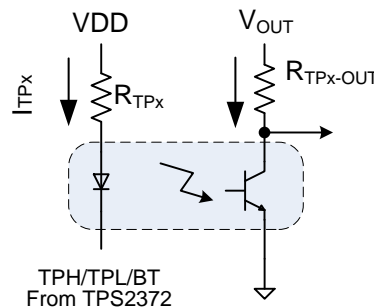
Connect a resistor from CLSA and CLSB to V_{SS} to program the classification current according to the IEEE 802.3bt standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLSA} and R_{CLSB} according to Table 1.

Choose Class 4 for $R_{CLSA} = 63.4 \Omega$.

Choose Class 3 for $R_{CLSB} = 90.9 \Omega$.

8.2.2.6 Opto-isolators for TPH, TPL and \overline{BT}

The TPH, TPL and \overline{BT} pin are active-low, open-drain outputs, which give an indication about the PSE allocated power along with its Type. Optocouplers can interface these pins to circuitry on the secondary side of the converter. A high-gain optocoupler and a high-impedance (for example, CMOS) receiver are recommended. Design of the optocoupler interface can be accomplished as follows:



See Table 2 to decode PSE Type

Figure 23. TPH, TPL, and \overline{BT} Interface

- A. As shown in Figure 23, let $V_{DD} = 48 \text{ V}$, $V_{OUT} = 5 \text{ V}$, $R_{TPx-OUT} = 10 \text{ k}\Omega$, $V_{TPx} = 260 \text{ mV}$, $V_{TPx-OUT} = 400 \text{ mV}$.

$$I_{TPx-OUT} = \frac{V_{OUT} - V_{TPx-OUT}}{R_{TPx-OUT}} = \frac{5 - 0.4}{10000} = 0.46 \text{ mA} \quad (1)$$

- B. The optocoupler current transfer ratio, CTR, is needed to determine R_{TPx} . A device with a minimum CTR of 100% at 1 mA LED bias current, I_{TPx} , is selected. In practice, CTR will vary with temperature, LED bias current, and aging. These variations may require some iteration using the CTR-versus- I_{DIODE} curve on the optocoupler data sheet.

- The approximate forward voltage of the optocoupler diode, V_{FWLED} , is 1.1 V from the data sheet.
- Use .

$$I_{TPx-MIN} = \frac{I_{TPx-OUT}}{CTR} = \frac{0.46 \text{ mA}}{1.00} = 0.46 \text{ mA}, \text{ Select } I_{TPx} = 1 \text{ mA}$$

$$R_{TPx} = \frac{V_C - V_T - V_{FWLED}}{I_{TPx}} = \frac{48 \text{ V} - 0.26 \text{ V} - 1.1 \text{ V}}{1 \text{ mA}} = 46.6 \text{ k}\Omega \quad (2)$$

- Choose a 46.4 k Ω resistor.

Most applications require that only the PSE's allocated power information (TPH and TPL) is needed for the MCU or PD load. In this case, the circuitry needed to drive the BT signal is not necessary and the BT pin can be left floating.

Some applications such as PoE lighting can benefit from the BT signal to show that the power consumption in standby operation may not meet regulatory requirements. In non-standard PoE applications, BT is used with TPH and TPL to indicate a PoE++ PSE.

8.2.2.7 Automatic MPS and MPS Duty Cycle, R_{MPS} and R_{MPS_DUTY}

MPS_DUTY should be short circuited to VSS for 12.5% duty cycle

$$R_{MPS} = \frac{V_{AMPS_CTL}}{I_{MPS}} = \frac{24\text{ V}}{18.5\text{ mA}} = 1.3\text{ k}\Omega \quad (3)$$

$$P_{RMPS} = \frac{V_{MPS}^2 \times \text{MPS Duty Cycle}}{R_{MPS}} = \frac{24\text{ V}^2 \times 26.4\%}{1.3\text{ k}\Omega} = 115\text{ mW} \quad (4)$$

Choose 1.3 k Ω rated for 1/8 W

26.4% duty cycle is chosen to take into account if the PD is connected to a IEEE802.3at PSE with a longer MPS timing specification.

For applications that require ultra-low power consumption, such as PoE Lighting, a shorter MPS duty-cycle can be used. For example, a 5.4% MPS duty cycle can be selected by leaving the MPS_DUTY pin open. Refer to Table 4 for MPS duty-cycle selection.

8.2.2.8 Internal Voltage Reference, R_{REF}

Per Recommended Operating Conditions,

Choose $R_{REF} = 49.9\text{ k}\Omega$

8.2.2.9 Autoclass

To enable Autoclass, AUTOCLS pin should be connected to VSS.

8.2.2.10 Inrush Delay

To enable the 80-ms inrush delay, IRSHDL_EN pin should be open

8.2.3 Application Curves

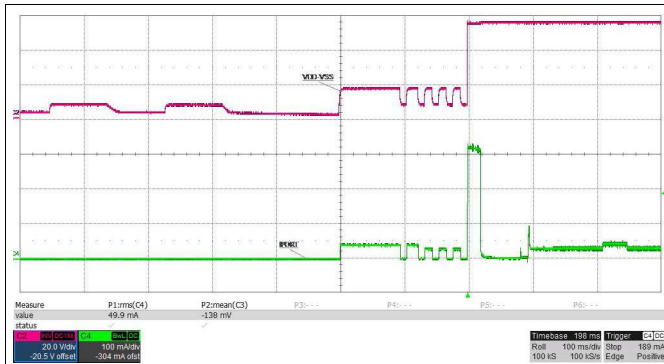


Figure 24. Startup

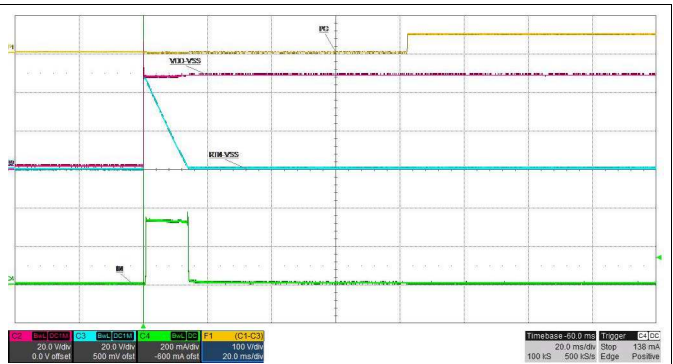


Figure 25. Startup and PG Delay

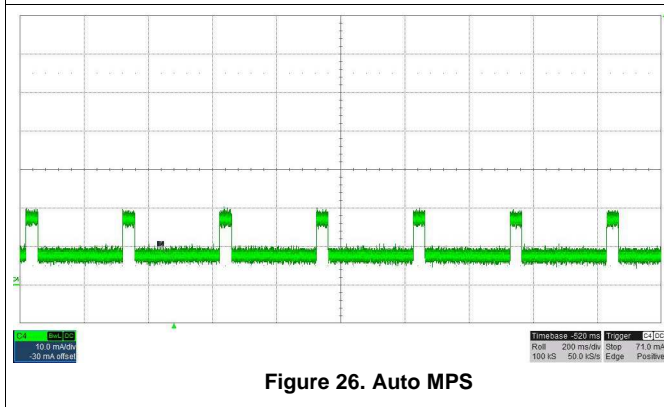


Figure 26. Auto MPS

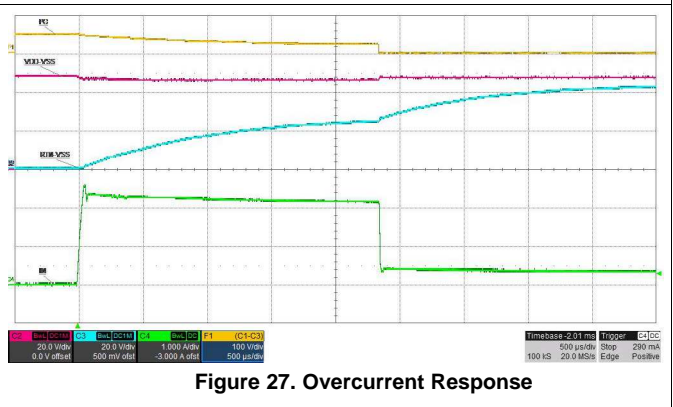


Figure 27. Overcurrent Response

9 Power Supply Recommendations

The TPS2372 device will typically be followed by a power supply such as an isolated flyback or active clamp forward converter or a non-isolated buck converter. The input voltage of the converter should be capable of operating within the IEEE802.3bt recommended input voltage as shown in [Table 6](#).

10 Layout

10.1 Layout Guidelines

The layout of the PoE front end should follow power and EMI/ESD best practice guidelines. A basic set of recommendations include:

- Parts placement must be driven by power flow in a point-to-point manner; RJ-45, Ethernet transformer, diode bridges, TVS and 0.1- μ F capacitor, and TPS2372.
- All leads should be as short as possible with wide power traces and paired signal and return.
- There should not be any crossovers of signals from one part of the flow to another.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS2372 should be located over split, local ground planes referenced to VSS for the PoE input and to RTN for the switched output.
- Large copper fills and traces should be used on SMT power-dissipating devices, and wide traces or overlay copper fills should be used in the power path.
- Nine vias are recommended on the Exposed Thermal Pad of the TPS2372. These should connect to all layers of a copper plane on the PCB. Ensure 80% printed solder coverage by area.

10.2 Layout Example

[Figure 28](#) and [Figure 29](#) show the top and bottom layer and assemblies of the TPS2372-4EVM-006 as a reference for optimum parts placement. A detailed PCB layout can be found in the user's guide of the *TPS2372-4EVM-006 Evaluation Module* (SLVUB75).

Layout Example (continued)

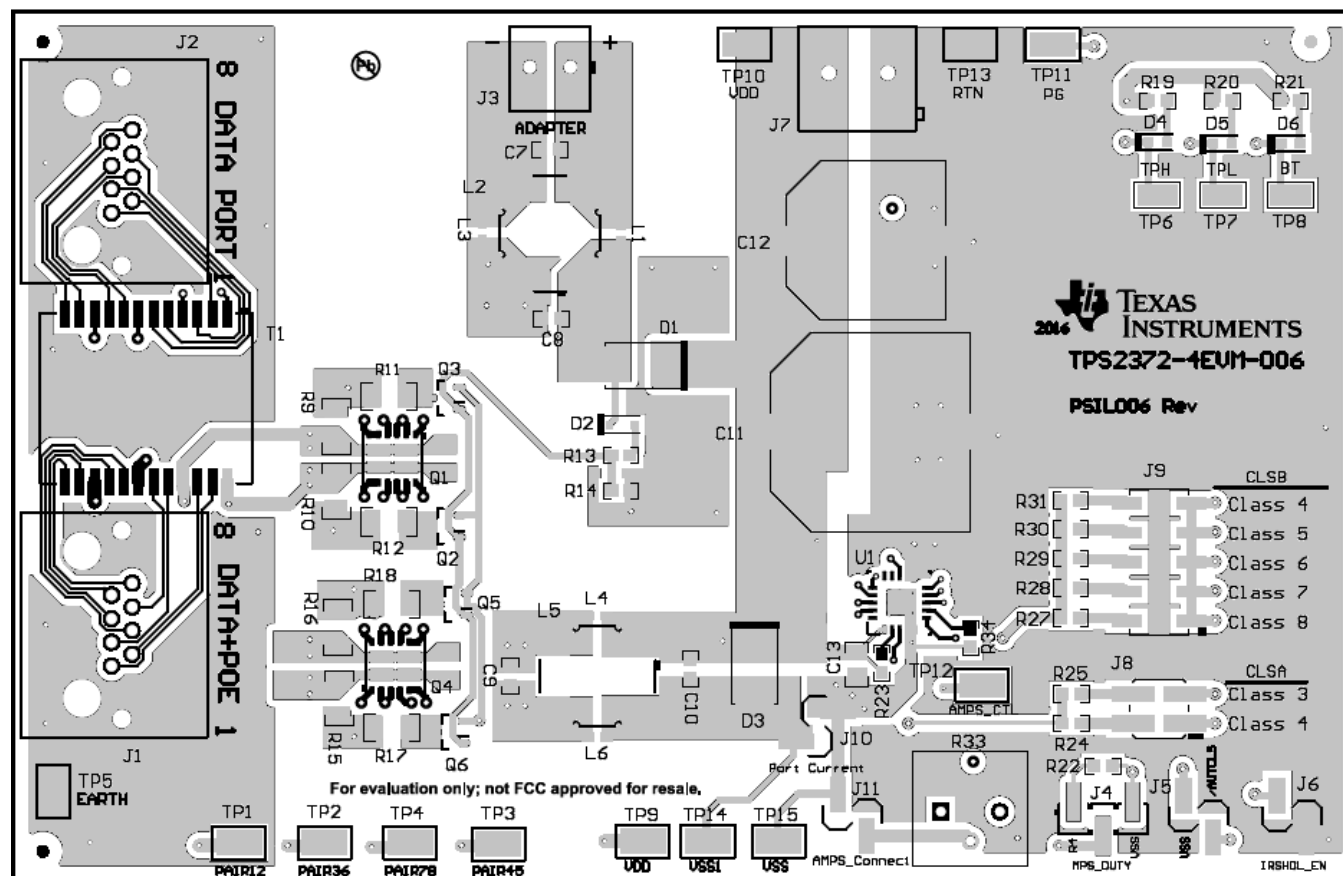


Figure 28. TPS2372-4EVM-006 Top Side Layout and Component Placement

Layout Example (continued)

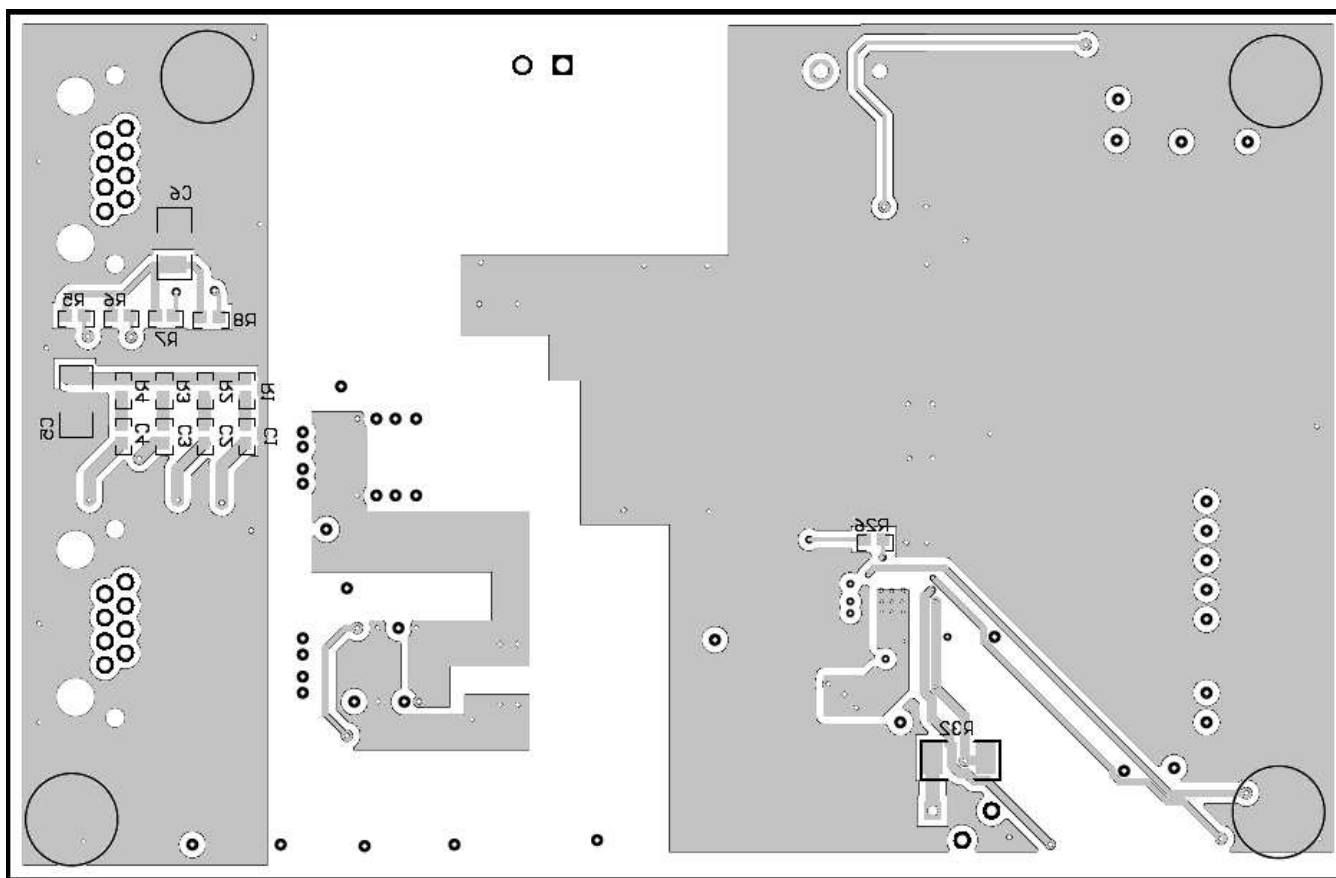


Figure 29. TPS2372-4EVM-006 Bottom Side Layout and Component Placement

10.3 EMI Containment

- Use compact loops for dv/dt and di/dt circuit paths (power loops and gate drives).
- Use minimal, yet thermally adequate, copper areas for heat sinking of components tied to switching nodes (minimize exposed radiating surface).
- Use copper ground planes (possible stitching) and top layer copper floods (surround circuitry with ground floods).
- Use 4 layer PCB if economically feasible (for better grounding).
- Minimize the amount of copper area associated with input traces (to minimize radiated pickup).
- Use Bob Smith terminations, Bob Smith EFT capacitor, and Bob Smith plane.
- Use Bob Smith plane as ground shield on input side of PCB (creating a phantom or literal earth ground).
- Use of ferrite beads on input (allow for possible use of beads or 0- Ω resistors).
- Maintain physical separation between input-related circuitry and power circuitry (use ferrite beads as boundary line).
- Possible use of common-mode inductors.
- Possible use of integrated RJ-45 jacks (shielded with internal transformer and Bob Smith terminations).
- End-product enclosure considerations (shielding).

10.4 Thermal Considerations and OTSD

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS2372 is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating TPS2372 device to experience an OTSD event if it is excessively heated by a nearby device.

10.5 ESD

ESD requirements for a unit that incorporates the TPS2372 have a much broader scope and operational implications than are used in TI's testing. Unit-level requirements should not be confused with reference design testing that only validates the ruggedness of the TPS2372.

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS2372-3	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS2372-4	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.1.2 関連資料

関連資料については、以下を参照してください。

- 『TPS23753を使用する高度なアダプタORソリューション』、[SLVA306](#)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

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11.5 静電気放電に関する注意事項



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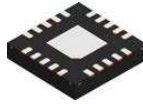
11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

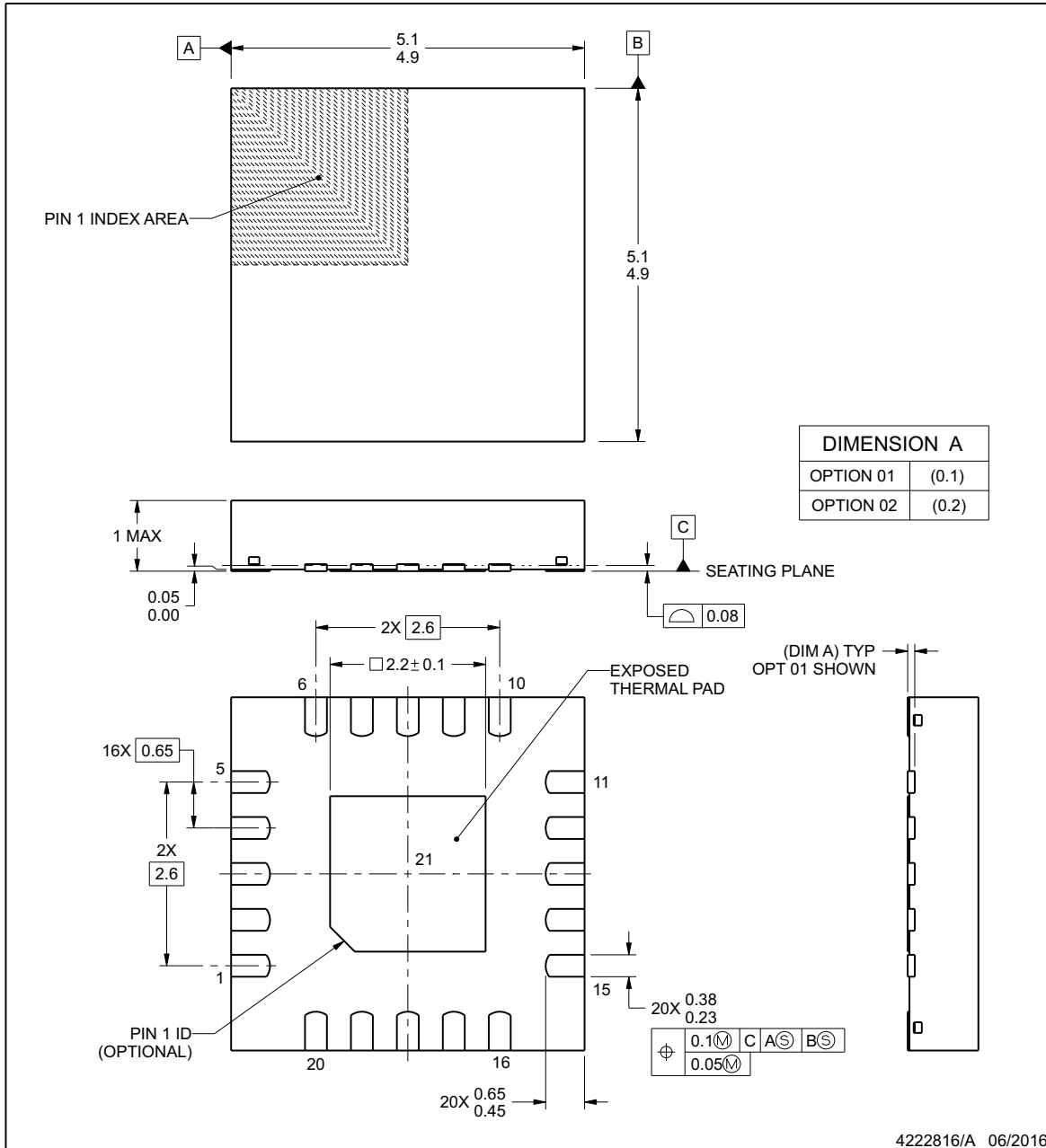


RGW0020B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



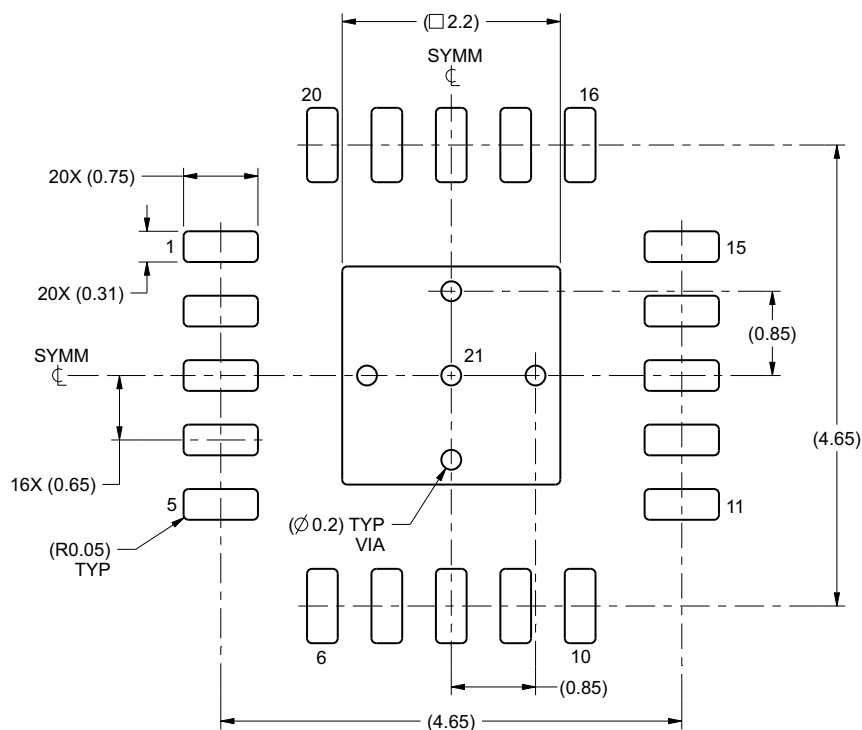
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

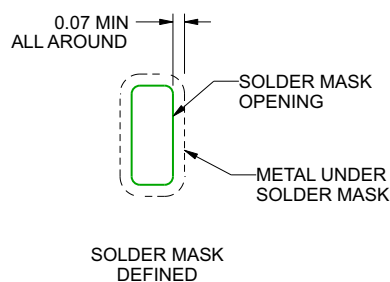
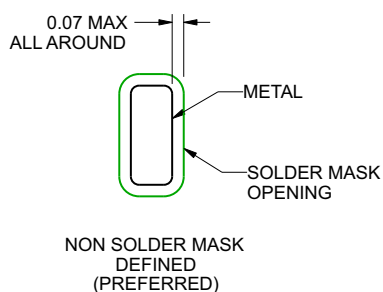
EXAMPLE BOARD LAYOUT

RGW0020B
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4222816/A 06/2016

NOTES: (continued)

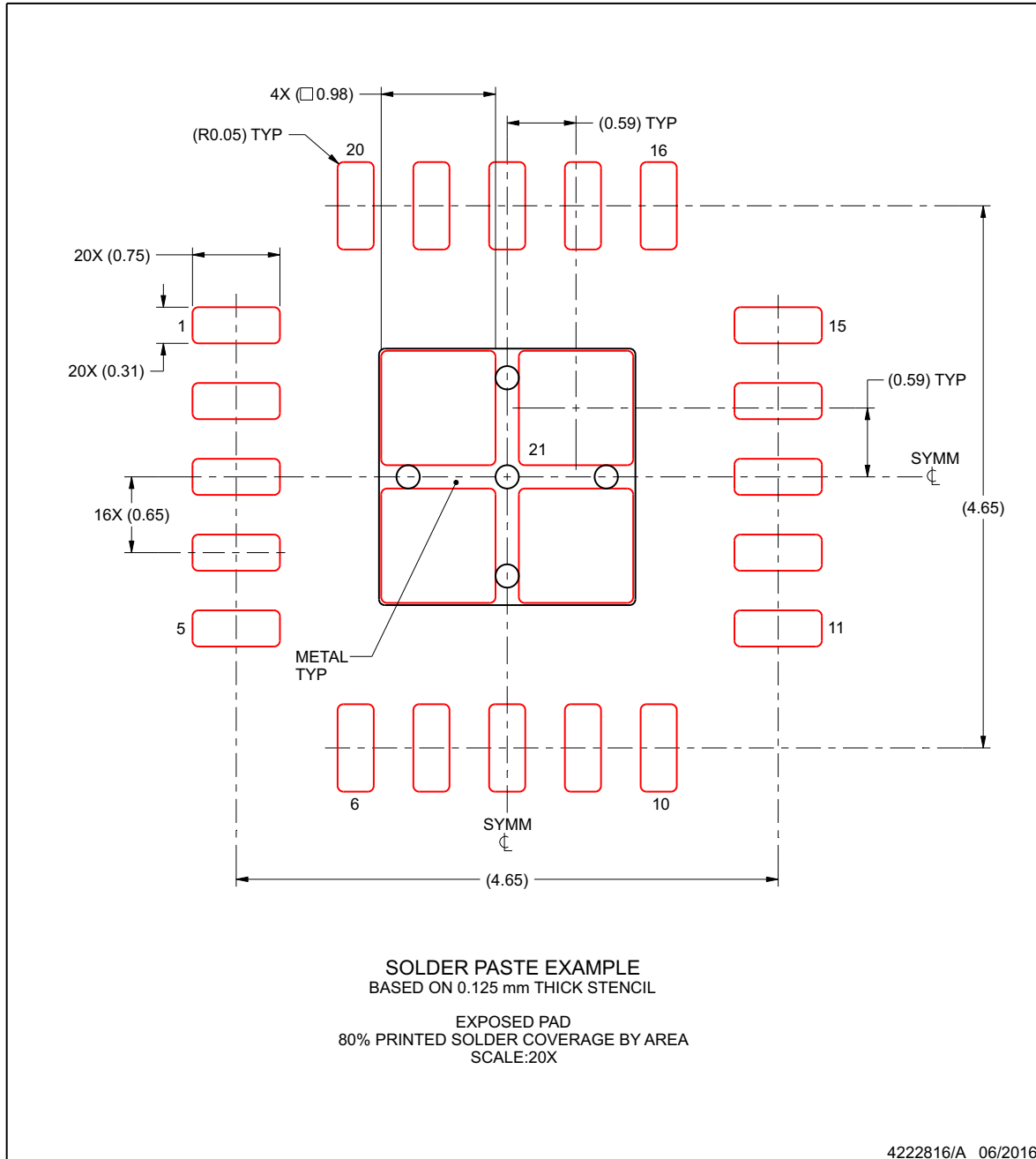
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGW0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2372-3RGWR	Active	Production	VQFN (RGW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-3
TPS2372-3RGWR.A	Active	Production	VQFN (RGW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-3
TPS2372-3RGWT	Active	Production	VQFN (RGW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-3
TPS2372-3RGWT.A	Active	Production	VQFN (RGW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-3
TPS2372-4RGWR	Active	Production	VQFN (RGW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-4
TPS2372-4RGWR.A	Active	Production	VQFN (RGW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-4
TPS2372-4RGWT	Active	Production	VQFN (RGW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-4
TPS2372-4RGWT.A	Active	Production	VQFN (RGW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 2372-4

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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