TEXAS INSTRUMENTS

TPS2597xx 2.7V～23V、7A、9.8mΩ eFuse、高精度電流モニタおよび過渡過電流ブランキング搭載

1 特長

- 広い動作時入力電圧範囲：2.7V ～ 23V
  - 絶対最大電圧 28V
- 低いオン抵抗の FET を内蔵：R_{ON} = 9.8mΩ (標準値)
- 高速過電圧保護
  - 過電圧クランプ (OVC) (ピンで選択可能なスレッショルド (3.89V、5.76V、13.88V)、5μs (標準値) の応答時間) または
  - 調整可能な過電圧誤動作防止 (OVLO) 1.2μs (標準値) の応答時間
- 負荷電流監視出力 (ILM) を備えた過電流保護
  - アクティブ電流制限またはサーキット ブレーカを選択可能
  - 調整可能なスレッショルド (I_{LIM}) 0.87A～7.7A
    - 精度：±10% (I_{LIM} > 1.74A)
  - 可変の過渡ブランキング タイマ (ITIMER)、最大 2 × I_{LIM} のピーク電流を許容
  - 出力負荷電流監視精度：±8% (最大値)
- 高速トリップ応答による短絡保護
  - 550ns の立ち上がり時間 (標準値)
  - 可変 (2 × I_{LIM}) および固定のスレッショルド
- アクティブ High のイネーブル入力、低電圧誤動作防止 (UVLO) スレッショルドを設定可能
- 可変の出力スルー レート (dVdt) 制御
- 過熱保護
- デジタル出力
  - フォルト通知 ($\overline{FLT}$) または
  - 可変スレッショルド (PGTH) 付きのパワー グッド表示 (PG)
- UL 2367 認定
  - ファイル番号 E339631
  - R_{ILM} ≥ 750Ω
- IEC 62368-1 CB 認証
- 小さい占有面積：QFN 2mm × 2mm (0.45mm ピッチ)

2 アプリケーション

- サーバー、PC マザーボード、アドイン カード
- エンタープライズ ストレージ：RAID/HBA/SAN/eSSD
- 患者モニタ
- 家電製品と電動工具
- 小売用 POS 端末
- スマートフォンとタブレット

3 説明

TPS2597xx デバイス ファミリの eFuse は、小さなパッケージに搭載され、高集積な回路保護および電力管理ソリューションです。このデバイスは、非常に少ない数の外付け部品で複数の保護モードを提供し、過負荷、短絡、電圧サージ、および過剰な突入電流に対して堅牢な保護を行います。

出力のスルー レートと突入電流は、単一の外付けコンデンサを使用して調整できます。固定の安全な最大電圧 (ピンで選択可能) に出力をクランプする方法と、可変の過電圧スレッショルドを入力が超えた際に出力を遮断する方法のどちらかで、入力過電圧状態から負荷を保護します。このデバイスは、電流をアクティブに制限するか、または回路を遮断することにより、出力過負荷に対応します。出力電流制限スレッショルドおよび過渡過電流ブランキング タイマは、ユーザーが調整可能です。電流制限制御ピンは、アナログ負荷電流モニタとしても機能します。
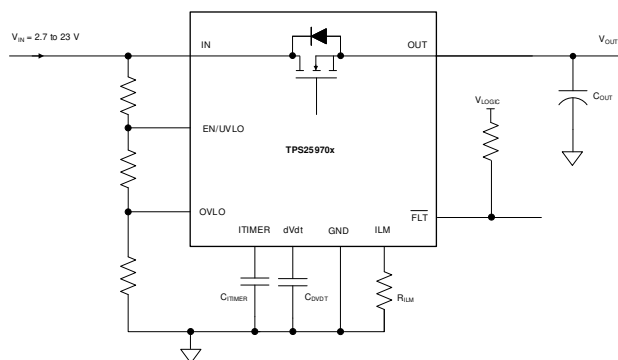
これらのデバイスは、2mm × 2mm、10 ピンの HotRod™ QFN パッケージで供給され、放熱性能の向上とシステムのフットプリント削減に役立ちます。

これらのデバイスは、-40℃～+125℃の接合部温度範囲で動作が規定されています。

パッケージ情報

部品番号	パッケージ[1]	パッケージ サイズ[2]
TPS2597xxRPW	RPW (QFN、10)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

概略回路図

Table of Contents

4 Device Comparison Table

PART NUMBER	OVERVOLTAGE RESPONSE	OVERCURRENT RESPONSE	PG and PGTH	$\overline{FLT}$	RESPONSE TO FAULT
TPS25970ARPW	Adjustable OVLO	Active Current Limit	N	Y	Auto-Retry
TPS25970LRPW					Latch-Off
TPS25972ARPW	Pin Selectable OVC (3.89 V/5.76 V/13.88 V)		Y	N	Auto-Retry
TPS25972LRPW					Latch-Off
TPS25974ARPW	Adjustable OVLO	Circuit Breaker			Auto-Retry
TPS25974LRPW					Latch-Off

5 Pin Configuration and Functions
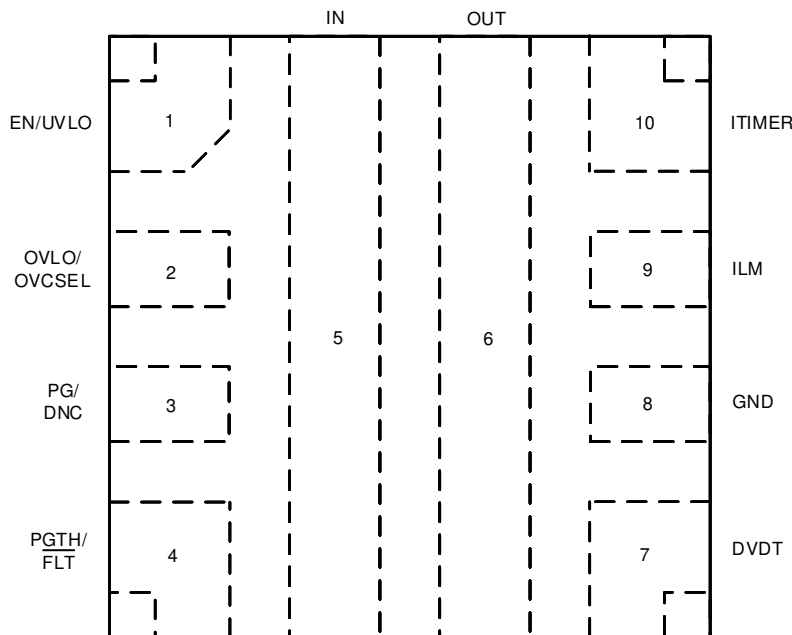
図 5-1. TPS2597xx RPW Package 10-Pin QFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active high enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the undervoltage lockout threshold. *Do not leave floating.* Refer to *Undervoltage Lockout (UVLO and UVP)* for details.
OVLO	2	Analog Input	*TPS25970x and TPS25974x:* A resistor divider on this pin from supply to GND can be used to adjust the overvoltage lockout threshold. This pin can also be used as an active low enable for the device. *Do not leave floating.* Refer to *Overvoltage Lockout (OVLO)* for details.
OVCSEL		Analog Input	*TPS25972x:* Overvoltage clamp threshold select pin. Refer to *Overvoltage Clamp (OVC)* for details.
PG	3	Digital Output	*TPS25972x and TPS25974x:* Power-good indication. This is an open-drain signal, which is asserted high when the internal powerpath is fully turned ON and the PGTH input exceeds a certain threshold. Refer to *Power Good Indication (PG)* for more details.
DNC		Digital Output	*TPS25970x:* Can be left floating
FLT	4	Digital Output	*TPS25970x:* Active low fault event indicator. This pin is an open-drain signal that is pulled low when a fault is detected. Refer to *Fault Response and Indication (FLT)* for more details.
PGTH		Analog Input	*TPS25972x and TPS25974x:* Power-good threshold. Refer to *Power Good Indication (PG)* for more details.
IN	5	Power	Power input
OUT	6	Power	Power output
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to *Slew Rate (dVdt) and Inrush Current Control* for details.
GND	8	Ground	This pin is the ground reference for all internal circuits and must be connected to system GND.
ILM	9	Analog Output	This pin is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit threshold during start-up as well as steady state. The pin voltage can also be used as analog output load current monitor signal. *Do not leave floating.* Refer to *Circuit-Breaker* or *Active Current Limiting* for more details.
ITIMER	10	Analog Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for the fastest response to overcurrent events. Refer to *Circuit-Breaker* or *Active Current Limiting* for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	Parameter	Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40 ℃ ≤ T_J ≤ 125 ℃	IN	–0.3	28	V
$SR_{IN(R)}$	Maximum input voltage rising slew rate	IN		100	V/µs
$SR_{IN(F)}$	Maximum input voltage falling slew rate	IN		10	V/µs
V_{OUT}	Maximum output voltage range, –40 ℃ ≤ T_J ≤ 125 ℃	OUT	–0.3	V_{IN} + 0.3	
$V_{OUT,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable pin voltage range	EN/UVLO	–0.3	6.5	V
V_{OV}	Maximum OVCSEL/OVLO pin voltage range	OVCSEL/OVLO	–0.3	6.5	V
V_{dVdT}	Maximum dVdT pin voltage range	dVdt	Internally limited		V
V_{ITIMER}	Maximum ITIMER pin voltage range	ITIMER	Internally limited		V
V_{PGTH}	Maximum PGTH pin voltage range	PGTH	–0.3	6.5	V
V_{PG}	Maximum PG pin voltage range	PG	–0.3	6.5	V
V_{FLTB}	Maximum $\overline{FLT}$ pin voltage range	$\overline{FLT}$	–0.3	6.5	V
V_{ILM}	Maximum ILM pin voltage range	ILM	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	Parameter	Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	23[1]	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5[2]	V
V_{OV}	OVLO pin voltage range (TPS25970x and TPS25974x variants only)	OVLO	0.5	1.5	V
V_{dVdT}	dVdT pin capacitor voltage rating	dVdt	V_{IN} + 5 V		V
V_{PGTH}	PGTH pin voltage range	PGTH		5	V
V_{FLTB}	$\overline{FLT}$ pin voltage range	$\overline{FLT}$		5	V
V_{PG}	PG pin voltage range	PG		5	V

6.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{ITIMER}	ITIMER pin capacitor voltage rating	ITIMER	4		V
R_{ILM}	ILM pin resistance to GND	ILM	715	6650	Ω
I_{MAX}	Continuous switch current, $T_J \le 125\ ℃$	IN to OUT		7	A
T_J	Junction temperature		−40	125	°C

(1) For TPS25972x OVC variants, the input operating voltage should be limited to the selected Output Voltage Clamp Option as listed in the Electrical Characteristics section

(2) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V , it is recommended to use a resistor divider with minimum pull-up resistor value of 350 kΩ.

6.4 Thermal Information

THERMAL METRIC [1]		TPS2597xx	UNIT
		RPW (QFN)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7[2]	°C/W
		71.8[3]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1[2]	°C/W
	Junction-to-top characterization parameter	1.3[3]	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23 [2]	°C/W
		14.5 [3]	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device

(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V for TPS25970x/4x, OVCSEL = 390 kΩ to GND for TPS25972x, R_{ILM} = 715 Ω , dVdT = Open, ITIMER = Open, $\overline{FLT}$ = Open for TPS25970x, PGTH = Open for TPS25972x/4x, PG = Open for TPS25972x/4x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current (TPS25970x)		413	650	µA
	IN supply quiescent current (TPS25972x)		407	650	µA
	IN supply quiescent current (TPS25974x)		413	650	µA
	IN supply quiescent current during OVC (TPS25972x)		429	650	µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		67	131	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		2.3	25	µA
$V_{UVP(R)}$	IN supply UVP rising threshold	2.44	2.54	2.64	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.35	2.45	2.55	V
OUTPUT VOLTAGE CLAMP (OUT) - TPS25972x					
V_{OVC}	Overvoltage Clamp threshold, OVCSEL = Shorted to GND	3.65	3.89	4.1	V
	Overvoltage Clamp threshold, OVCSEL = Open	5.25	5.76	6.2	V
	Overvoltage Clamp threshold, OVCSEL = 390 kΩ to GND	13.2	13.88	14.5	V
V_{CLAMP}	Output voltage during clamping, OVCSEL = Shorted to GND, I_{OUT} = 10 mA	3.2	3.82	4.2	V
	Output voltage during clamping, OVCSEL = Open, I_{OUT} = 10 mA	5	5.68	6.12	V
	Output voltage during clamping, OVCSEL = 390 kΩ to GND, I_{OUT} = 10 mA	13	13.79	14.6	V
OUTPUT LOAD CURRENT MONITOR (ILM)					
G_{IMON}	Analog load current monitor gain (I_{MON} : I_{OUT}), 1 A ≤ I_{OUT} ≤ 7.7 A, I_{OUT} < I_{LIM}	98	105.5	114	µA/A
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent threshold, R_{ILM} = 6.65 KΩ	0.745	0.87	0.97	A
	Overcurrent threshold, R_{ILM} = 3.32 KΩ	1.55	1.73	1.905	A
	Overcurrent threshold, R_{ILM} = 1.65 KΩ	3.2	3.48	3.715	A
	Overcurrent threshold, R_{ILM} = 750 Ω	7.03	7.67	8.15	A
I_{SPFLT}	Circuit-Breaker threshold, ILM pin open (Single point failure)			0.1	A
I_{SPFLT}	Circuit-Breaker threshold, ILM pin shorted to GND (Single point failure)		2	3.1	A
I_{SCGain}	Scalable fast-trip threshold (I_{SC}) : I_{LIM} ratio	170	201	240	%
VFB	V_{OUT} threshold to exit current limit foldback	1.55	1.88	2.23	V
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} ≤ 4 V, I_{OUT} = 3 A, T_J = 25 °C		10	18.3	mΩ
	4 < V_{IN} ≤ 23 V, I_{OUT} = 3 A, T_J = 25 °C		9.8	18.3	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.183	1.2	1.228	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.076	1.1	1.12	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.45	0.75	0.95	V
I_{ENLKG}	EN/UVLO pin leakage current	-0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO) - TPS25970x/4x					
$V_{OV(R)}$	OVLO rising threshold	1.183	1.2	1.228	V

資料に関するフィードバック(ご意見やお問い合わせ)を送信

English Data Sheet: SLVSGG5

6.5 Electrical Characteristics (続き)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V for TPS25970x/4x, OVCSEL = 390 kΩ to GND for TPS25972x, R_{ILM} = 715 Ω , dVdT = Open, ITIMER = Open, $\overline{FLT}$ = Open for TPS25970x, PGTH = Open for TPS25972x/4x, PG = Open for TPS25972x/4x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
$V_{OV(F)}$	OVLO falling threshold	1.076	1.1	1.12	V
I_{OVLKG}	OVLO pin leakage current (0.5 V < V_{OVLO} < 1.5 V)	-0.1		0.1	µA
OVERCURRENT FAULT TIMER (ITIMER)					
I_{ITIMER}	ITIMER pin internal discharge current, I_{OUT} > I_{LIM}	1.5	2	2.72	µA
R_{ITIMER}	ITIMER pin internal pull-up resistance		13.8	35	kΩ
V_{INT}	ITIMER pin internal pull-up voltage	2.1	2.57	2.74	V
$V_{ITIMER(F)}$	ITIMER comparator threshold, I_{OUT} > I_{LIM}	0.609	1.05	1.37	V
ΔV_{ITIMER}	ITIMER discharge differential voltage threshold, I_{OUT} > I_{LIM}	1.286	1.52	1.741	V
POWER GOOD INDICATION (PG) - TPS25972x/4x					
V_{PGD}	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pull-up (I_{PG} = 26 µA)		663	1000	mV
	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pull-up (I_{PG} = 242 µA)		782	1000	mV
	PG pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0	600	mV
I_{PGLKG}	PG pin leakage current, PG asserted			3	µA
POWERGOOD THRESHOLD (PGTH)					
$V_{PGTH(R)}$	PGTH rising threshold	1.178	1.2	1.23	V
$V_{PGTH(F)}$	PGTH falling threshold	1.071	1.1	1.13	V
$I_{PGTHLKG}$	PGTH pin leakage current	-1		1	µA
FAULT INDICATION (FLTB) - TPS25970x					
I_{FLTLKG}	$\overline{FLT}$ pin leakage current	-1		1	µA
R_{FLTB}	$\overline{FLT}$ pin internal pull-down resistance		12.4		Ω
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J ↑		154		°C
TSD_{HYS}	Thermal Shutdown hysteresis, T_J ↓		10		°C
DVDT					
I_{dVdt}	dVdt pin internal charging current	1.4	3.4	5.7	µA

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	TPS25970x and TPS25974x, V_{OVLO} > $V_{OV(R)}$ to V_{OUT} ↓		1.2		µs
t_{OVC}	Overvoltage clamp response time	TPS25972x, V_{IN} > V_{OVC} to V_{OUT} ↓		5		µs
t_{CB}	Circuit-Breaker response time	TPS25974x, I_{OUT} > I_{LIM} + 30% to V_{OUT} ↓		2		µs
t_{LIM}	Current limit response time	TPS25970x and TPS25972x, I_{OUT} > I_{LIM} + 30% to I_{OUT} settling to within 5% of I_{LIM}		465		µs
t_{SC}	Short-circuit response time	I_{OUT} > 3x I_{LIM} to output current cut off		550		ns
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT} ↓		550		ns
$t_{TSD,RST}$	Thermal Shutdown auto-retry Interval	Device enabled and T_J < TSD - TSD_{HYS}		110		ms
t_{PGA}	PG assertion de-glitch time	V_{PGTH} > $V_{PGTH(R)}$ to PG ↑		14		µs

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PGD}	PG de-assertion de-glitch time	$V_{PGTH} < V_{PGTH(F)}$ to PG ↓		14		µs

6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNITS
SR_{ON}	Output rising slew rate	2.7 V	8.922	1.218	0.72	V/ms
		12 V	21.45	1.562	0.901	
		23 V	34.16	1.761	1.003	
$t_{D,ON}$	Turn on delay	2.7 V	0.138	0.505	0.79	ms
		12 V	0.145	0.979	1.659	
		23 V	0.15	1.478	2.562	
t_R	Rise time	2.7 V	0.242	1.771	2.993	ms
		12 V	0.446	6.131	10.63	
		23 V	0.538	10.43	18.31	
t_{ON}	Turn on time	2.7 V	0.379	2.277	3.783	ms
		12 V	0.582	7.11	12.29	
		23 V	0.668	11.91	20.87	
$t_{D,OFF}$	Turn off delay	2.7 V	22.1	22.1	22.1	µs
		12 V	18.9	18.9	18.9	
		23 V	16.5	16.5	16.5	

6.8 Typical Characteristics
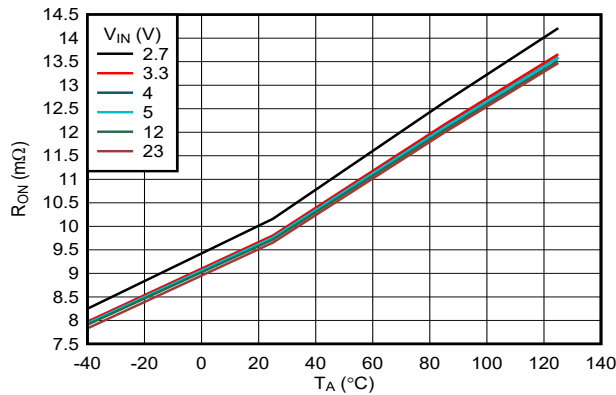
図 6-1. ON-Resistance vs Supply Voltage
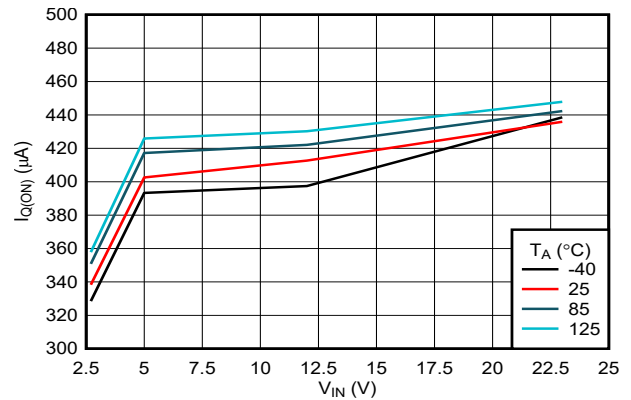
図 6-2. IN Quiescent Current vs Temperature (TPS25970x, TPS25974x Variants)
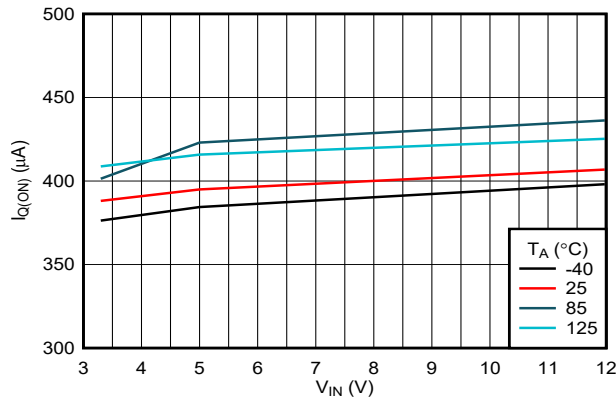
図 6-3. IN Quiescent Current vs Temperature (TPS25972x Variant)
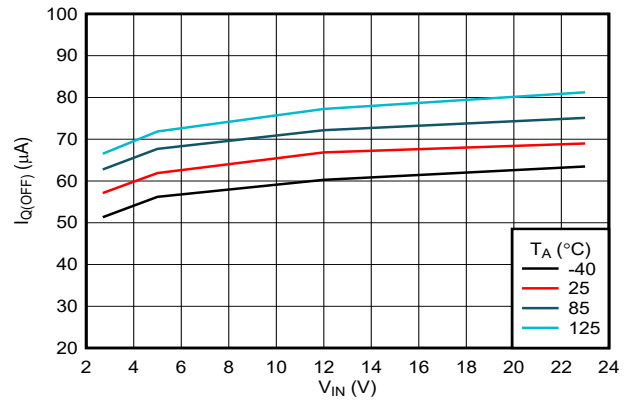
図 6-4. IN OFF State (UVLO) Current vs Temperature
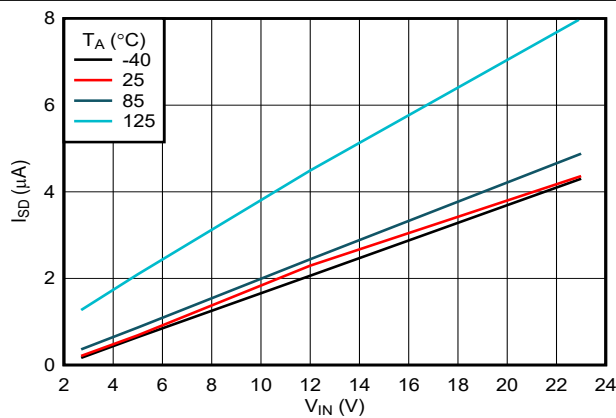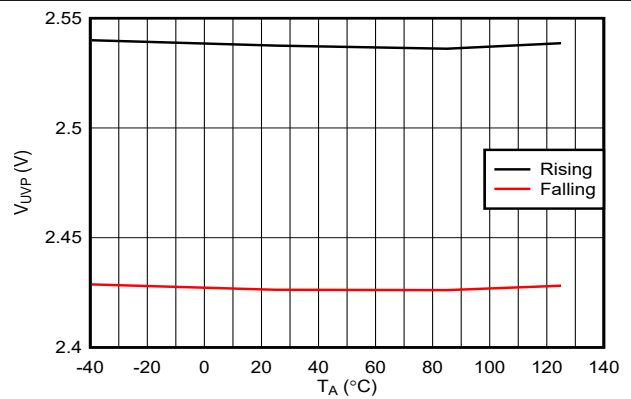

図 6-5. IN Shutdown Current vs Temperature

図 6-6. IN Undervoltage Threshold vs Temperature
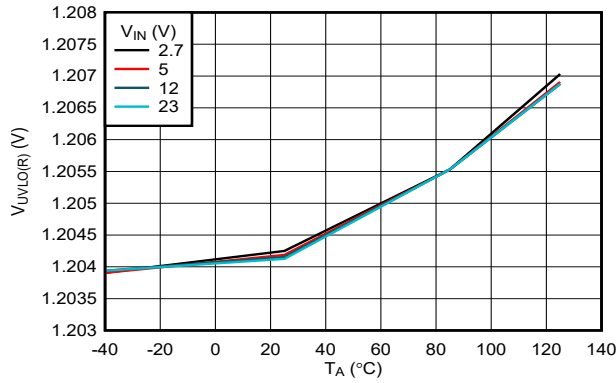
6.8 Typical Characteristics (continued)
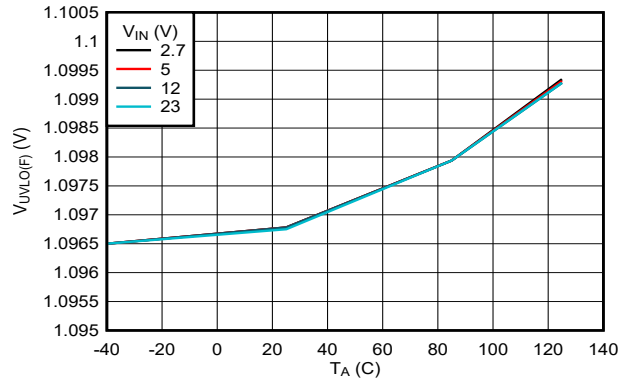

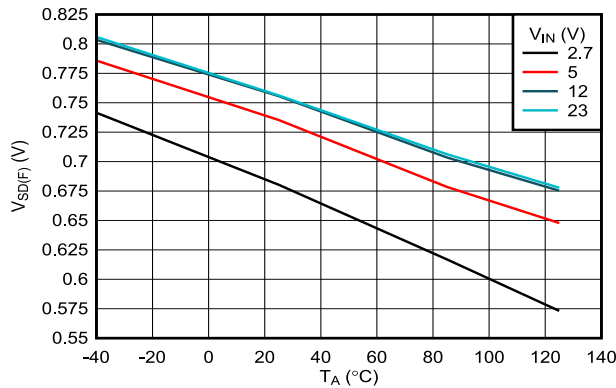図 6-7. EN/UVLO Rising Threshold vs Temperature

図 6-8. EN/UVLO Falling Threshold vs Temperature

図 6-9. EN/UVLO Shutdown Falling Threshold vs Temperature
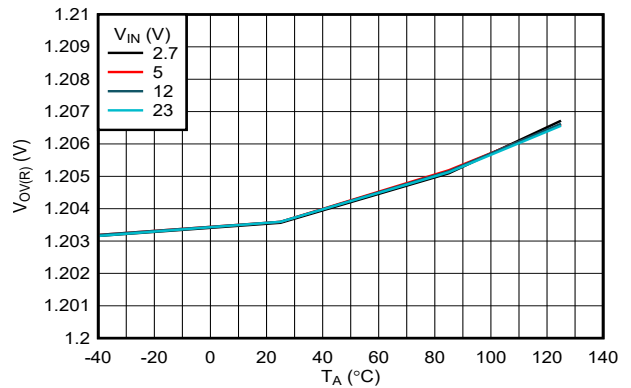
図 6-10. OVLO Rising Threshold vs Temperature (TPS25970x, TPS25974x Variants)
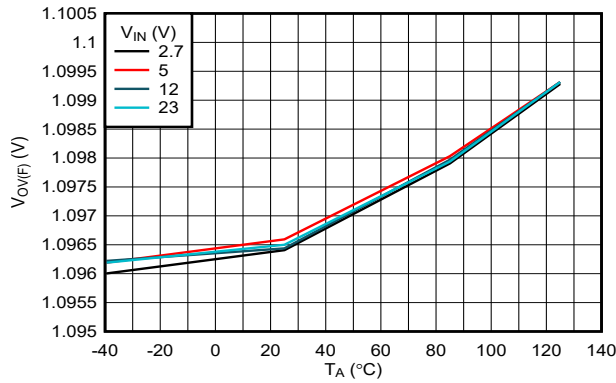
図 6-11. OVLO Falling Threshold vs Temperature (TPS25970x, TPS25974x Variants)
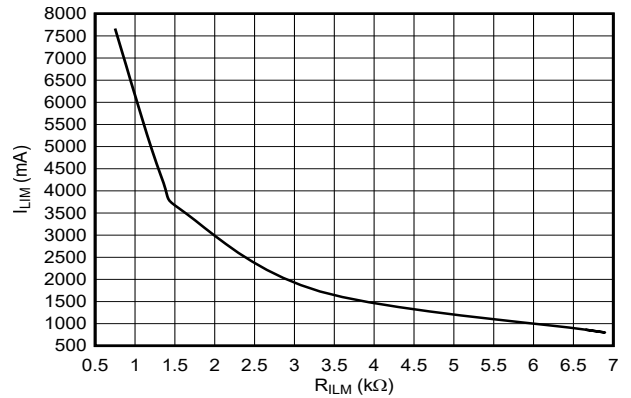
図 6-12. Overcurrent Threshold vs ILM Resistor

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5

6.8 Typical Characteristics (continued)
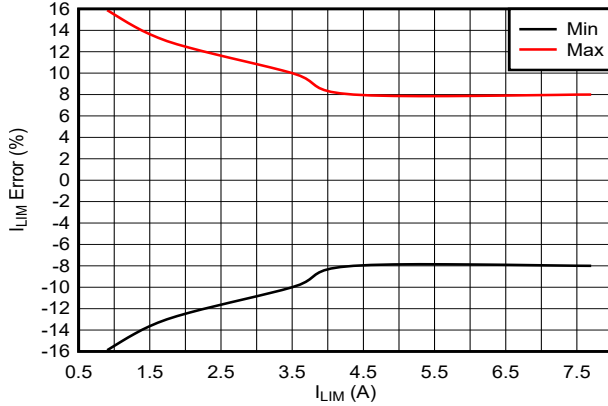
図 6-13. Overcurrent Threshold Accuracy (Across Process, Voltage and Temperature)
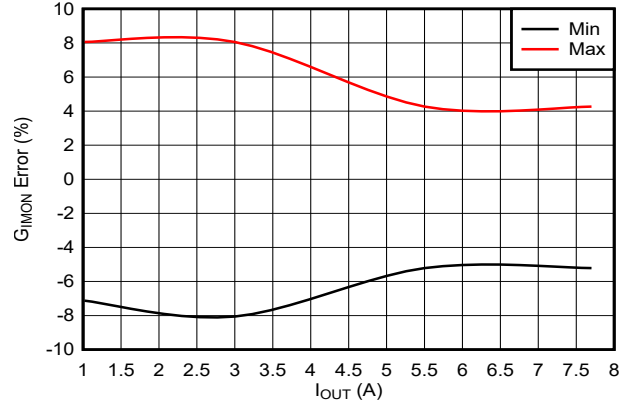
図 6-14. Analog Current Monitor Gain Accuracy
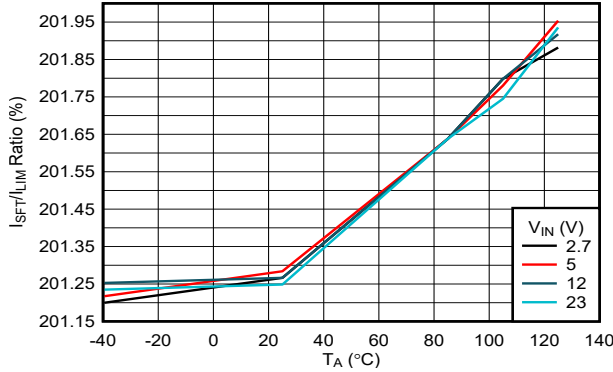
図 6-15. Scalable Fast-Trip Threshold: Current Limit Threshold (I_LIM) Ratio vs Temperature
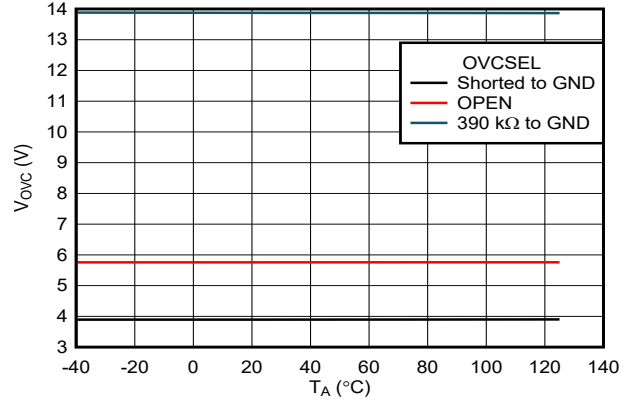

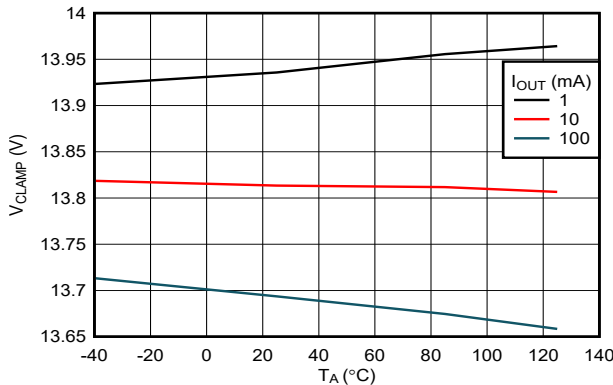図 6-16. OVC Threshold vs Temperature (TPS25972x Variant)

図 6-17. OVC Clamping Voltage (OVCSEL = 390 kΩ to GND) vs Load Current (TPS25972x Variant)
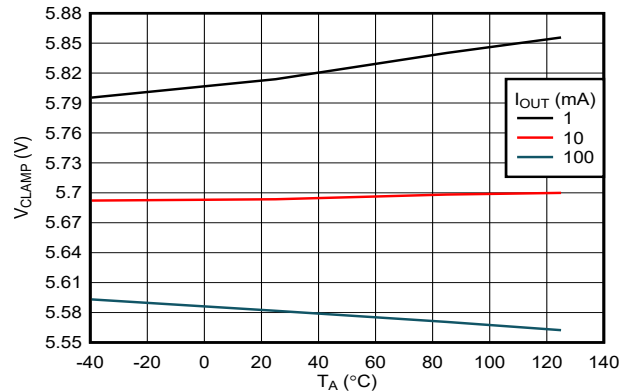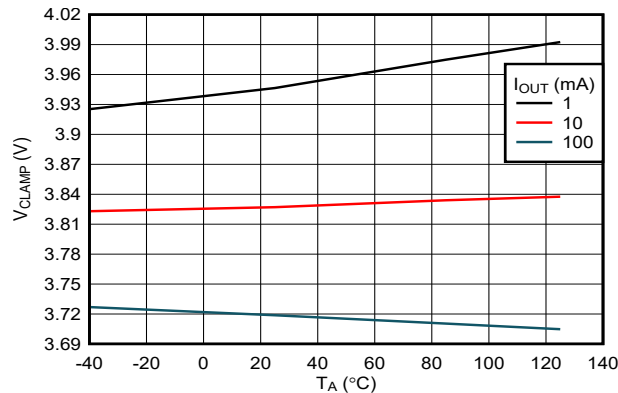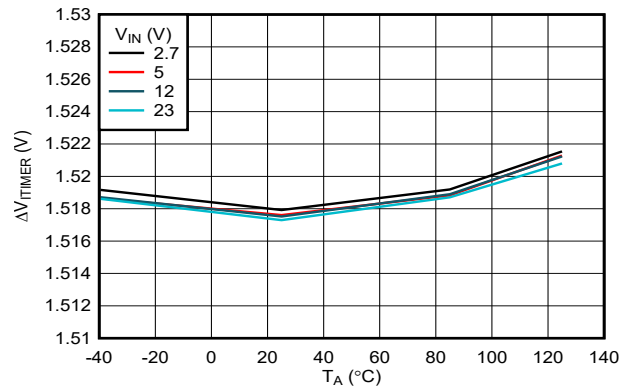

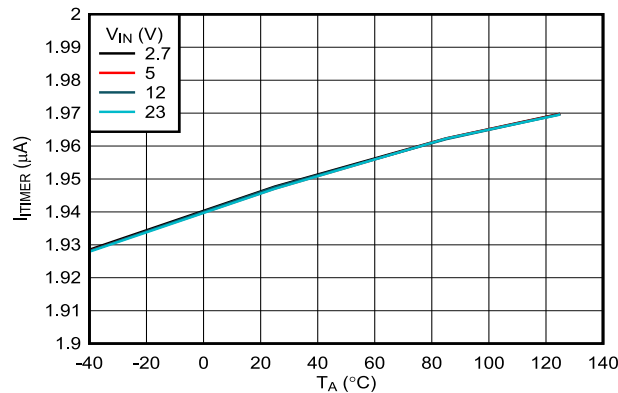図 6-18. OVC Clamping Voltage (OVCSEL = OPEN) vs Load Current (TPS25972x Variant)
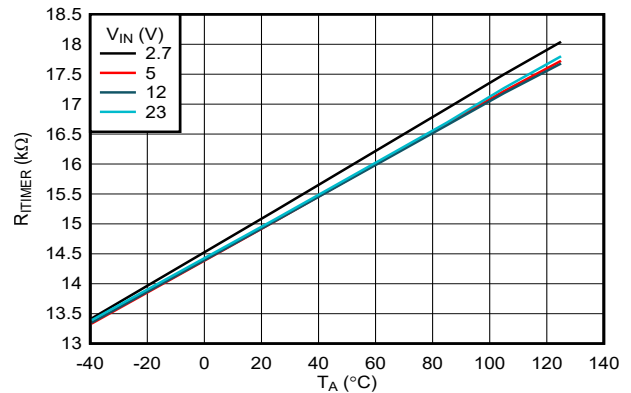
6.8 Typical Characteristics (continued)

図 6-19. OVC Clamping Voltage (OVCSEL = GND) vs Load Current (TPS25972x Variant)
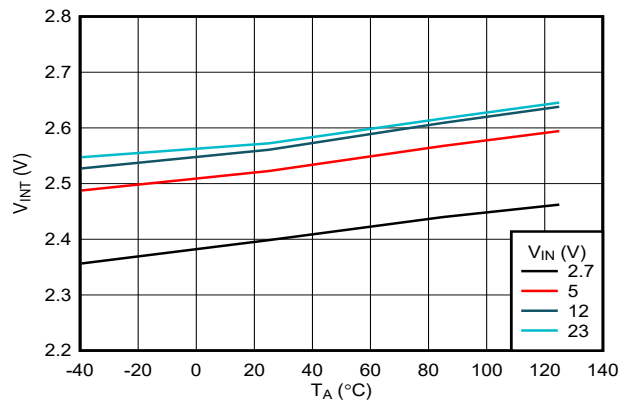
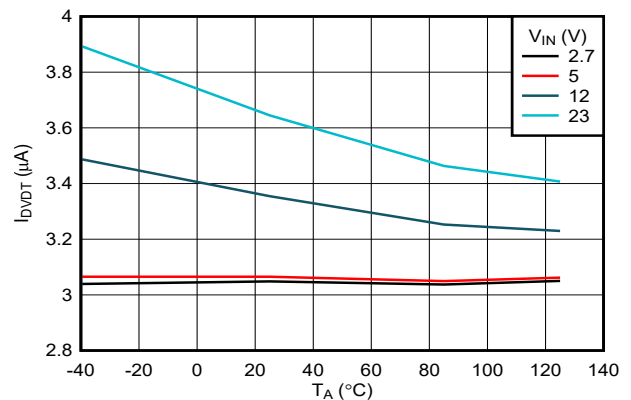図 6-20. ITIMER Discharge Differential Voltage Threshold vs Temperature

図 6-21. ITIMER Discharge Current vs Temperature

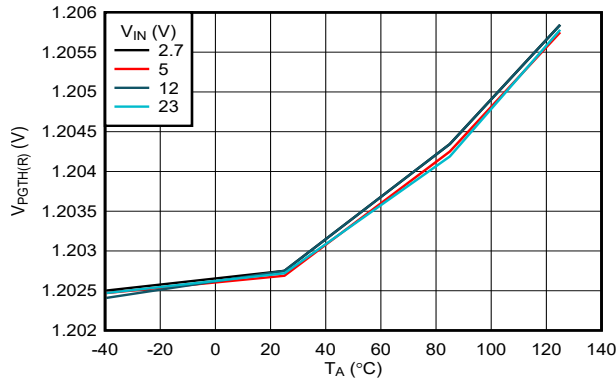図 6-22. ITIMER Internal Pullup Resistance vs Temperature

図 6-23. ITIMER internal Pullup Voltage vs Temperature

図 6-24. DVDT Charging Current vs Temperature

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5

6.8 Typical Characteristics (continued)

図 6-25. PGTH Threshold (Rising) vs Temperature (TPS25972x, TPS25974x Variants)
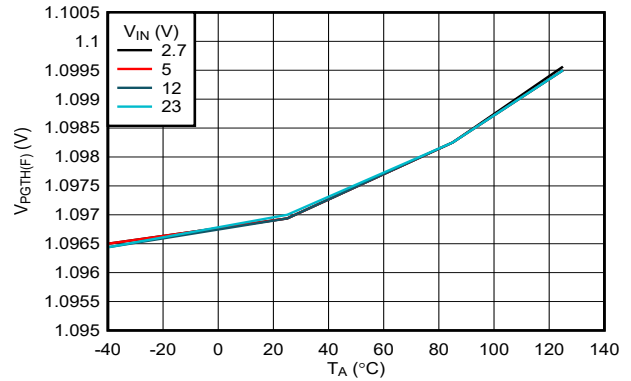
図 6-26. PGTH Threshold (Falling) vs Temperature (TPS25972x, TPS25974x Variants)
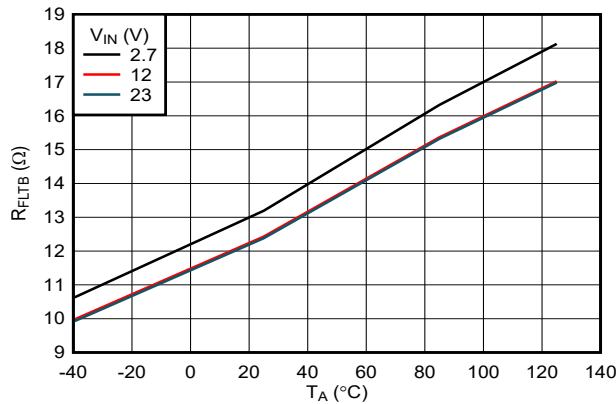
図 6-27. FLT Pin Pulldown Resistance vs Temperature
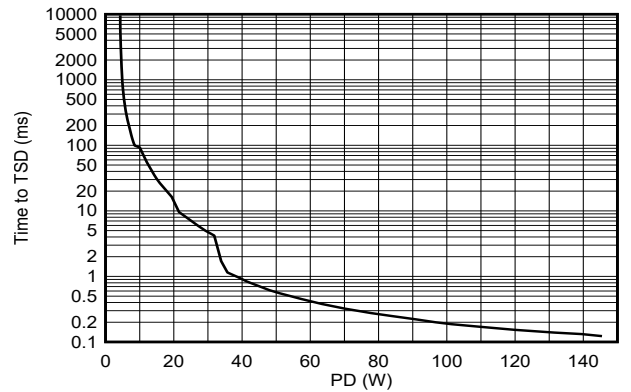
図 6-28. Time to Thermal Shut-Down During Inrush State

図 6-29. Time to Thermal Shut-Down During Steady State

V_{IN} = 12 V, C_{OUT} = 22 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ ramped from 0 V → 1.4 V → 0 V

図 6-30. Power Up and Down With EN/UVLO Control

6.8 Typical Characteristics (continued)
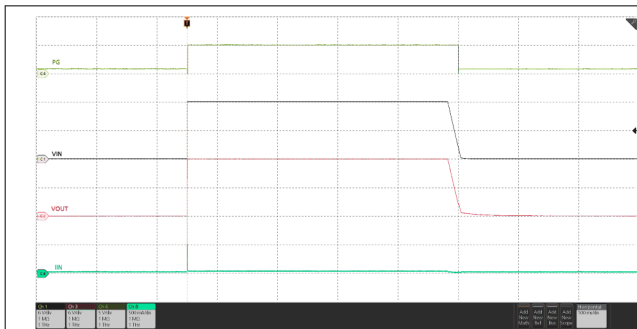
$V_{EN/UVLO}$ = 2 V, C_{OUT} = 22 µF, C_{dVdt} = Open, V_{IN} ramped from 0 V → 12 V → 0 V

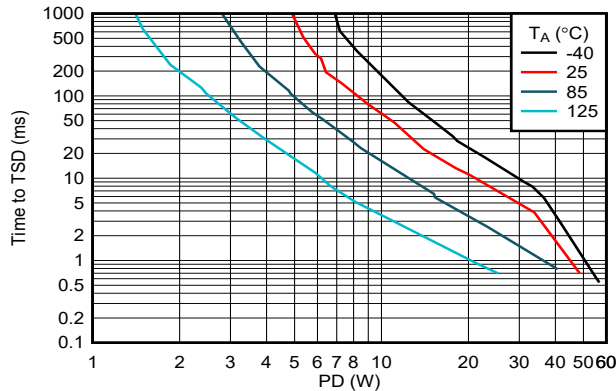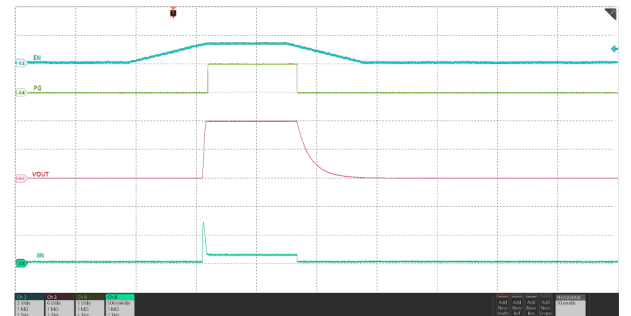**図 6-31. Power Up and Down With Input Supply**
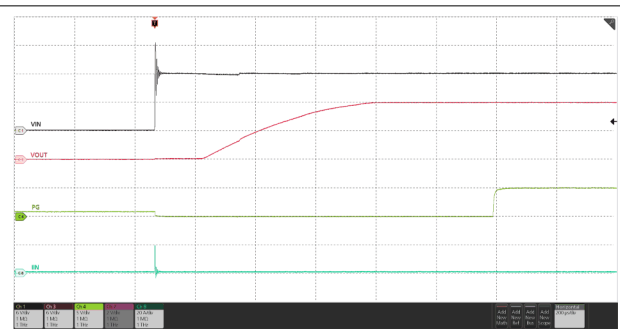
C_{OUT} = 22 µF, C_{dVdt} = Open, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

図 6-32. Input Hot-Plug
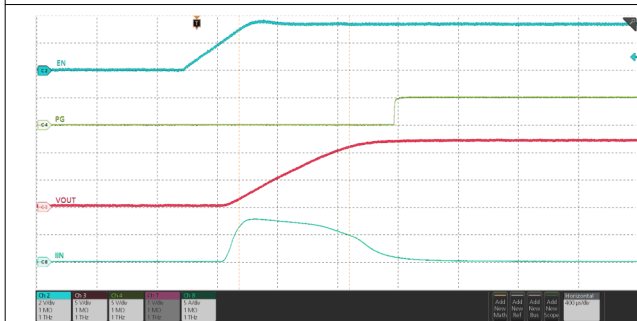
V_{IN} = 12 V, C_{OUT} = 470 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 3.3 V

図 6-33. Inrush Current Without Slew Rate Control – Capacitive Load
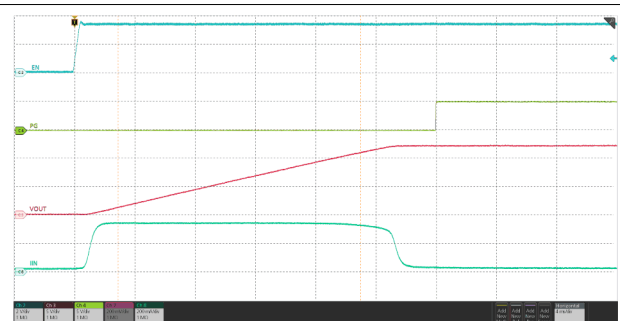
V_{IN} = 12 V, C_{OUT} = 470 µF, C_{dVdt} = 5100 pF, $V_{EN/UVLO}$ stepped up to 3.3 V

図 6-34. Inrush Current With Slew Rate Control – Capacitive Load
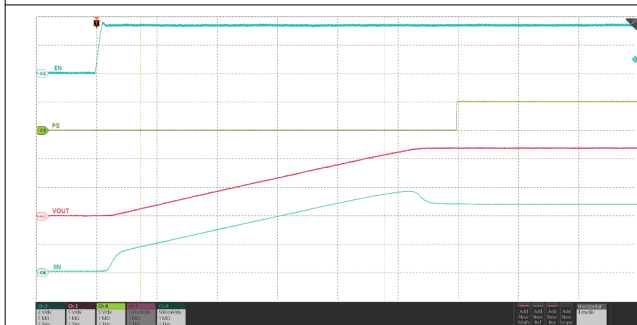
V_{IN} = 12 V, C_{OUT} = 470 µF, R_{OUT} = 10 Ω, C_{dVdt} = 5100 pF, $V_{EN/UVLO}$ stepped up to 3.3 V

図 6-35. Inrush Current With Slew Rate Control – Resistive and Capacitive Load
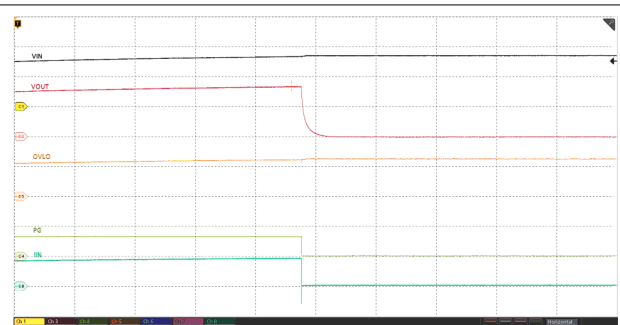
OV threshold set to 16.7 V, V_{IN} ramped up from 12 V to 17 V

図 6-36. Overvoltage Lockout Response – TPS25970x and TPS25974x

Product Folder Links: *TPS2597*

English Data Sheet: *SLVSGG5*

6.8 Typical Characteristics (continued)
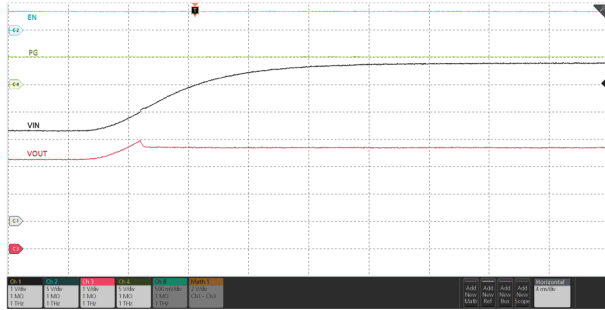
R_{OVCSEL} = GND, C_{OUT} = 220 µF, I_{OUT} = 200 mA, V_{IN} ramped up from 3.3 V to 5.8 V

図 6-37. Overvoltage Clamp Response – TPS25972x
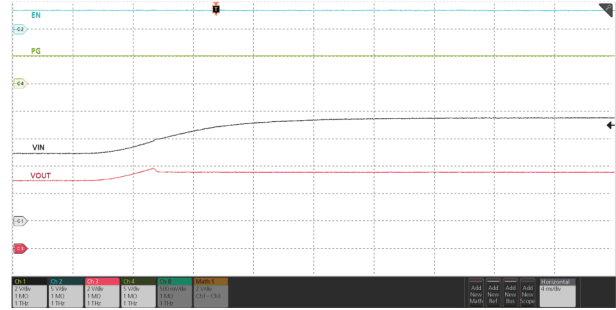
R_{OVCSEL} = Open, C_{OUT} = 220 µF, I_{OUT} = 200 mA, V_{IN} ramped up from 5 V to 7.5 V

図 6-38. Overvoltage Clamp Response – TPS25972x
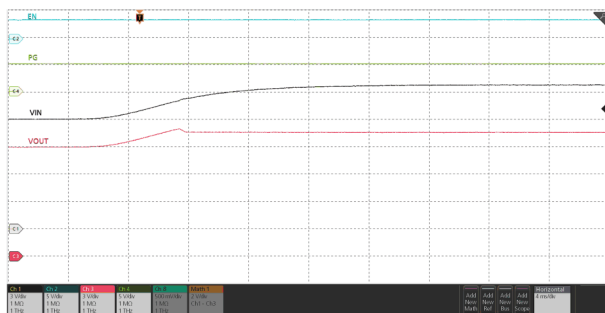
R_{OVCSEL} = 390 kΩ, C_{OUT} = 220 µF, I_{OUT} = 200 mA, V_{IN} ramped up from 12 V to 16.5 V

図 6-39. Overvoltage Clamp Response – TPS25972x
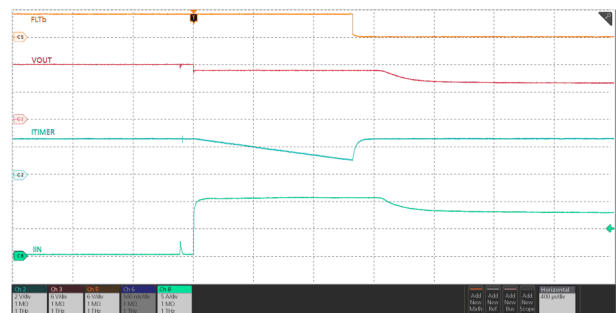
V_{IN} = 12 V, C_{ITIMER} = 1.3 nF, C_{OUT} = 220 µF, R_{ILM} = 715 Ω, I_{OUT} stepped from 0 A → 11 A

図 6-40. Active Current Limit Response – TPS25970x
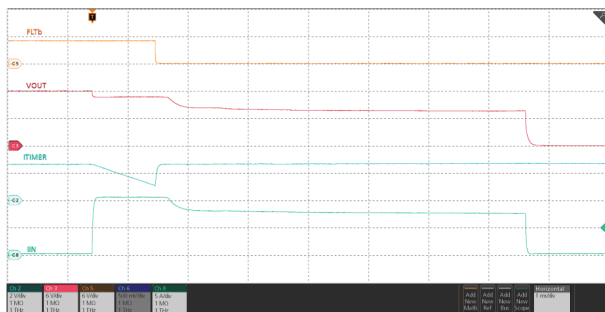
V_{IN} = 12 V, C_{ITIMER} = 1.3 nF, C_{OUT} = 220 µF, R_{ILM} = 715 Ω, I_{OUT} stepped from 0 A → 11 A

図 6-41. Active Current Limit Response Followed by TSD – TPS25970x
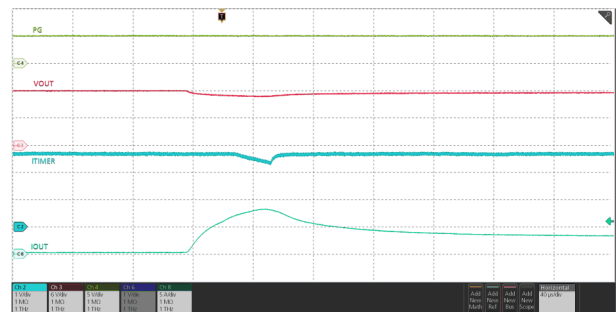
V_{IN} = 12 V, C_{ITIMER} = 120 pF, C_{OUT} = 470 µF, R_{ILM} = 715 Ω, I_{OUT} ramped from 0 A → 8 A → 4 A within 100 µs

図 6-42. Transient Overcurrent Blanking Timer Response

6.8 Typical Characteristics (continued)
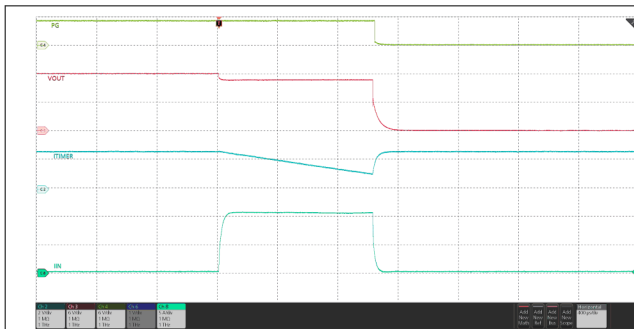
V_{IN} = 12 V, C_{ITIMER} = 1.3 nF, C_{OUT} = 470 µF, R_{ILM} = 715 Ω, I_{OUT} stepped from 0 A → 11 A

図 6-43. Circuit-Breaker Response TPS25974x
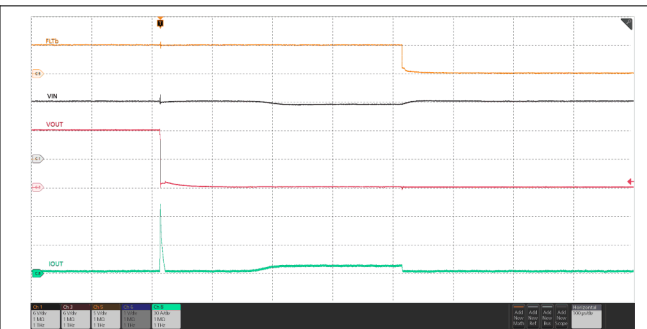
V_{IN} = 12 V, R_{ILM} = 715 Ω, OUT stepped from Open → Short-circuit to GND

図 6-44. Output Short-Circuit During Steady State
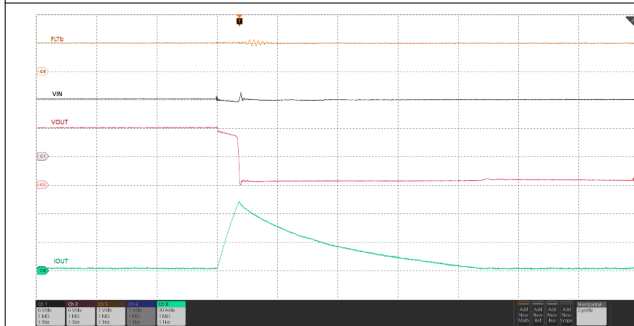
V_{IN} = 12 V, R_{ILM} = 715 Ω, OUT stepped from Open → Short-circuit to GND

図 6-45. Output Short-Circuit During Steady State (Zoomed In)
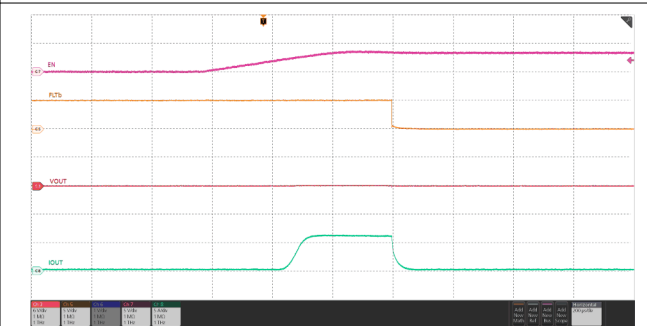
V_{IN} = 12 V, C_{OUT} = Open, OUT short-circuit to GND, R_{ILM} = 715 Ω, $V_{EN/UVLO}$ stepped from 0 V to 3.3 V

図 6-46. Power Up into Short-Circuit

Product Folder Links: *TPS2597*

English Data Sheet: *SLVSGG5*

7 Detailed Description

7.1 Overview

The TPS2597xx is an eFuse with an integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the undervoltage protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path (HFET) to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal HFET to ensure that the user adjustable overcurrent limit threshold (I_{LIM}) is not exceeded and overvoltage spikes are either safely clamped to the selected threshold voltage (V_{OVC}) or cut-off after they cross the user-adjustable overvoltage lockout threshold (V_{OVLO}). The device also provides fast protection against severe overcurrent during short-circuit events. This feature keeps the system safe from harmful levels of voltage and current. At the same time, a user-adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This action ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

7.2 Functional Block Diagram
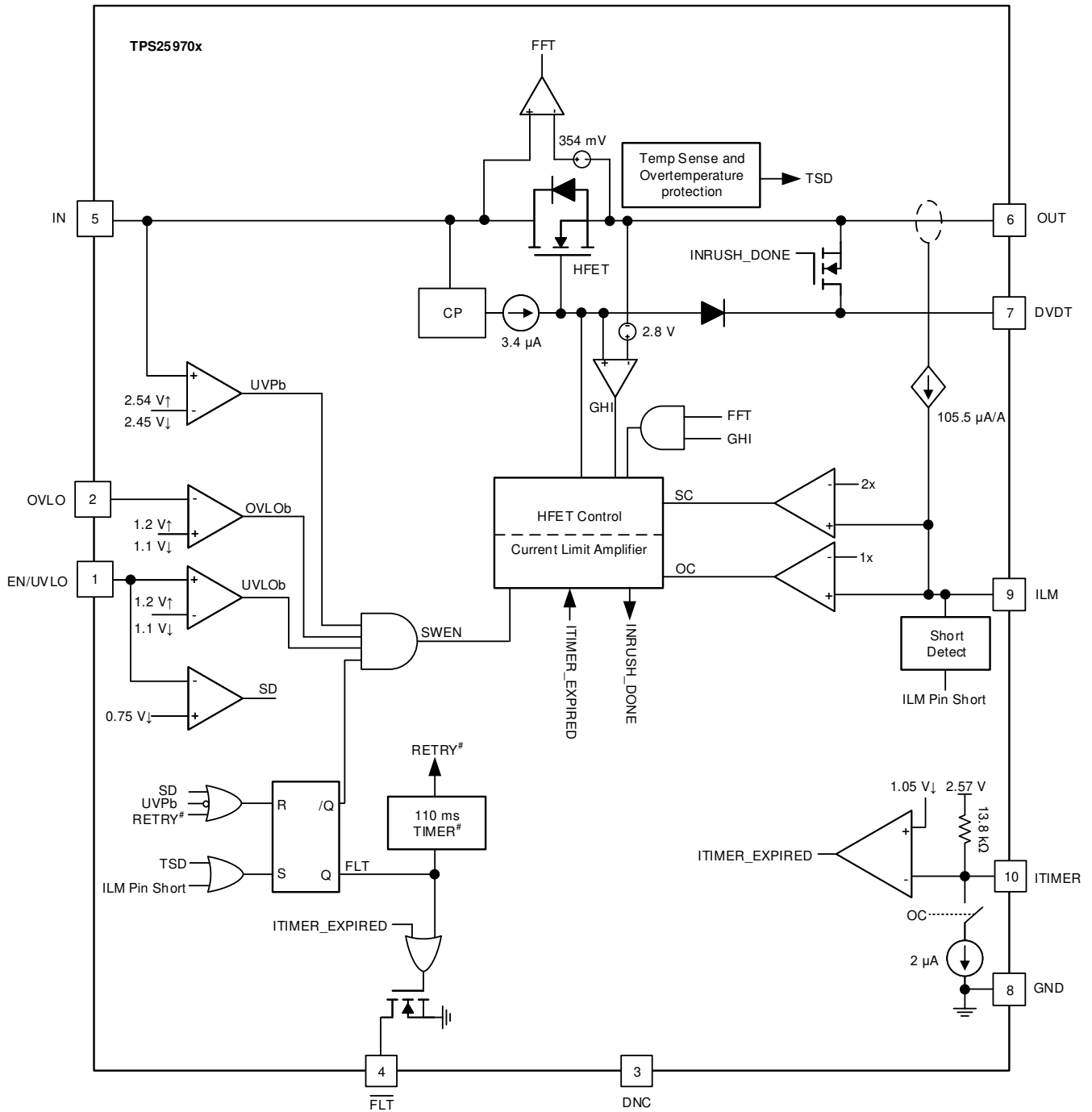
Not applicable to Latch-off variants (TPS25970L)

図 7-1. TPS25970x Block Diagram
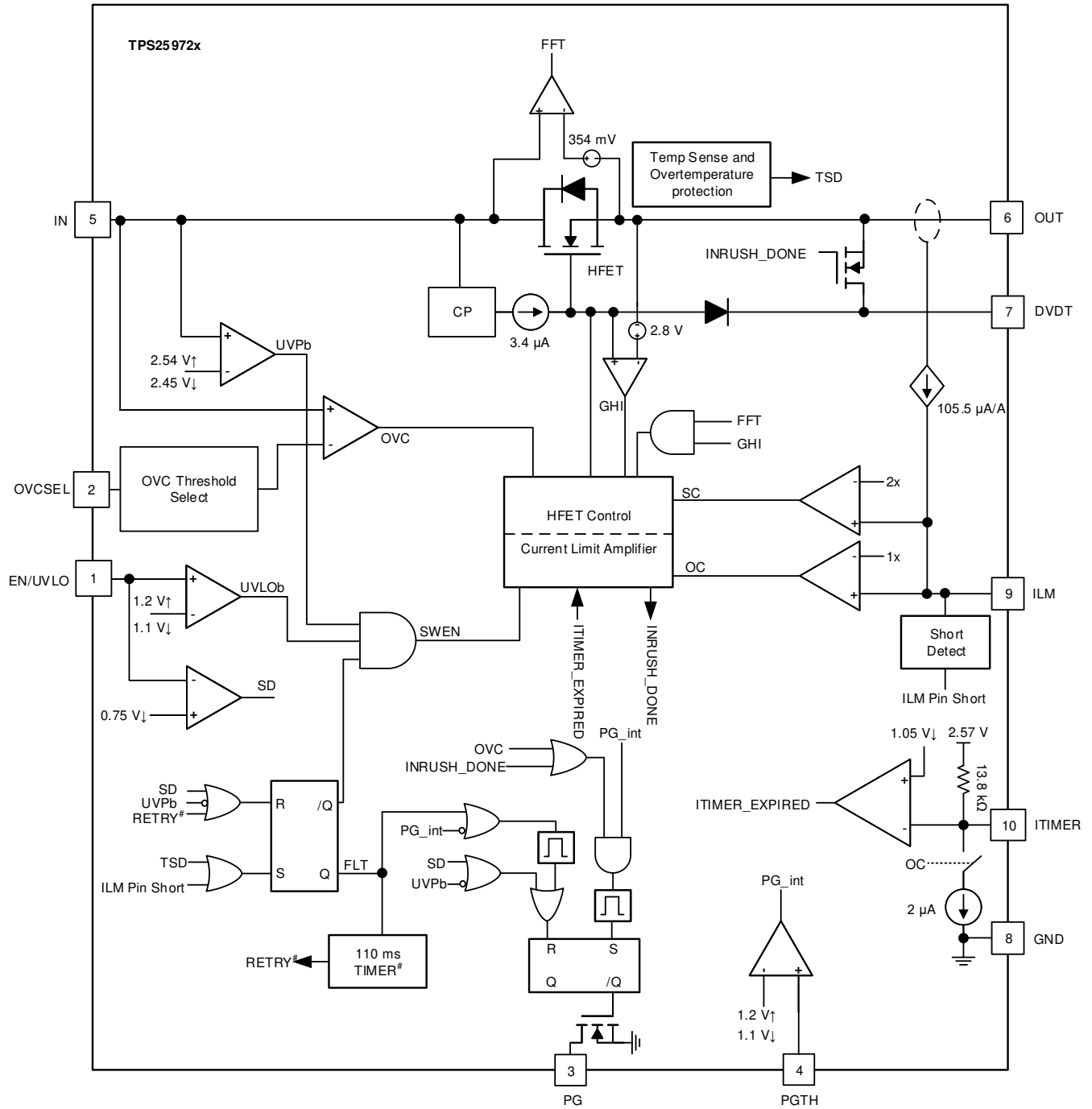
図 7-2. TPS25972x Block Diagram
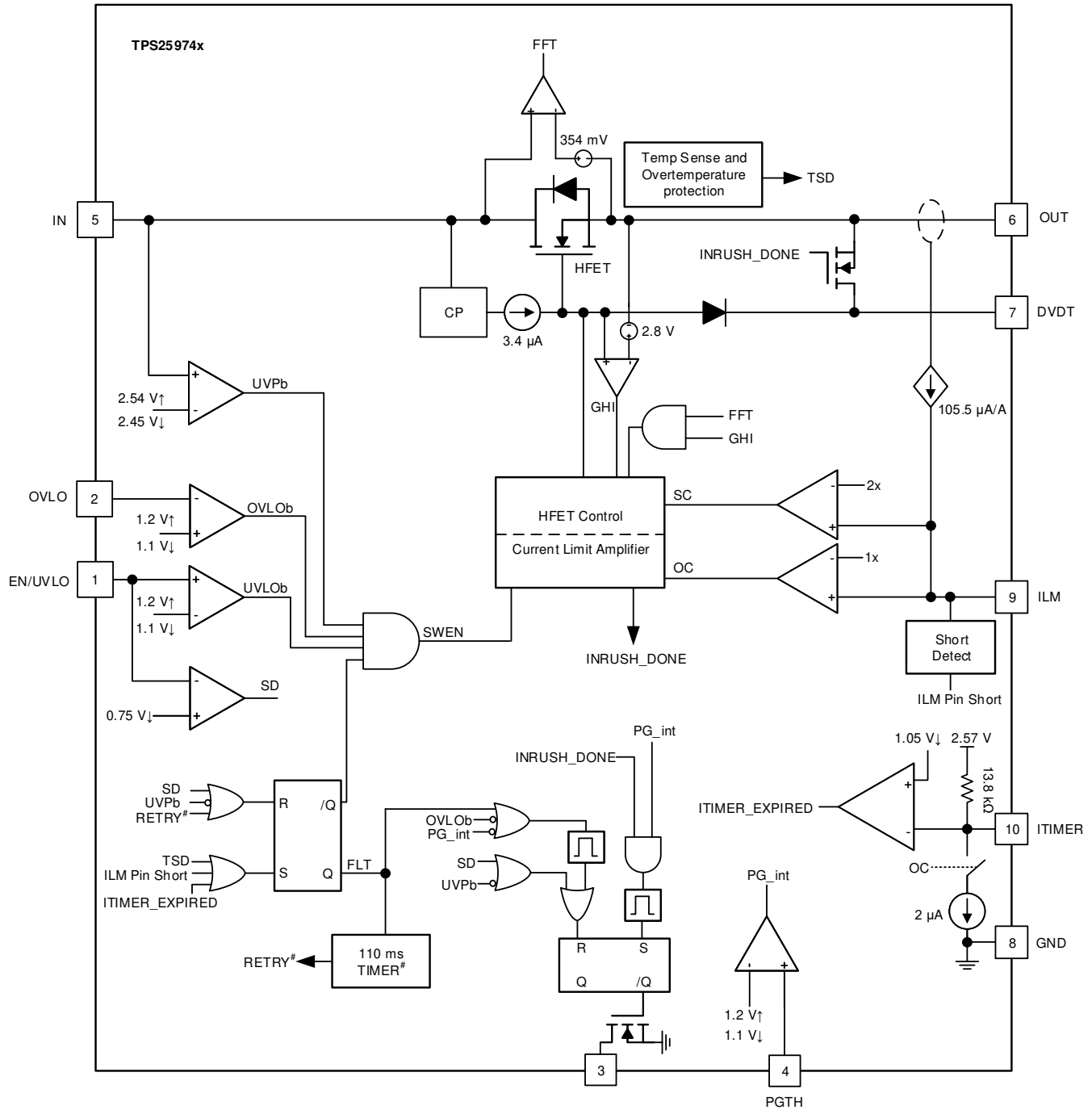
Not applicable to Latch-off variants (TPS25972L)

図 7-3. TPS25974x Block Diagram

Not applicable to Latch-off variants (TPS25974L)

7.3 Feature Description

The TPS2597xx eFuse is a compact, feature-rich power management device that provides detection, protection, and indication in the event of system faults.

7.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS2597xx implements undervoltage protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user-defined value. 図 7-4 and 式 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.
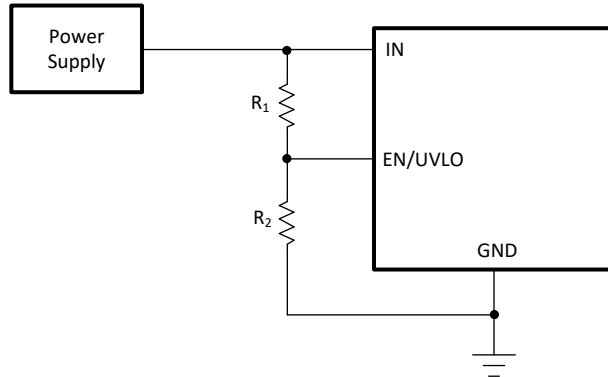
図 7-4. Adjustable Undervoltage Protection

$$VIN(UV) = \frac{VUVLO \times (R1 + R2)}{R2} \tag{1}$$

7.3.2 Overvoltage Lockout (OVLO)

The TPS25970x and TPS25974x variants allow the user to implement overvoltage lockout to protect the load from input overvoltage conditions. The OVLO comparator on the OVLO pin allows the overvoltage protection threshold to be adjusted to a user-defined value. After the voltage at the OVLO pin crosses the OVLO rising threshold, $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the OVLO pin to fall below the OVLO falling threshold, $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysteresis. 図 7-5 and 式 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.
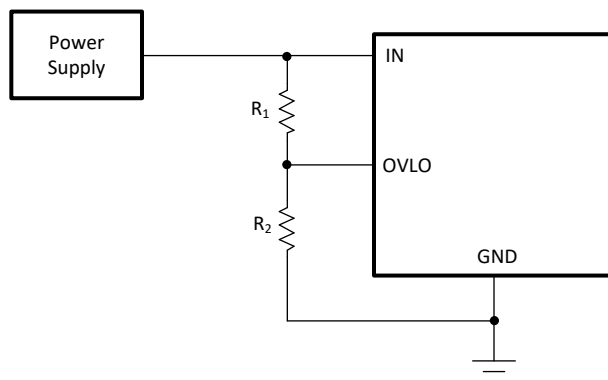
図 7-5. Adjustable Overvoltage Protection

$$VIN(OV) = \frac{VOV \times (R1 + R2)}{R2} \tag{2}$$

While recovering from a OVLO event, the TPS25970x variants start up with inrush control (dVdt).
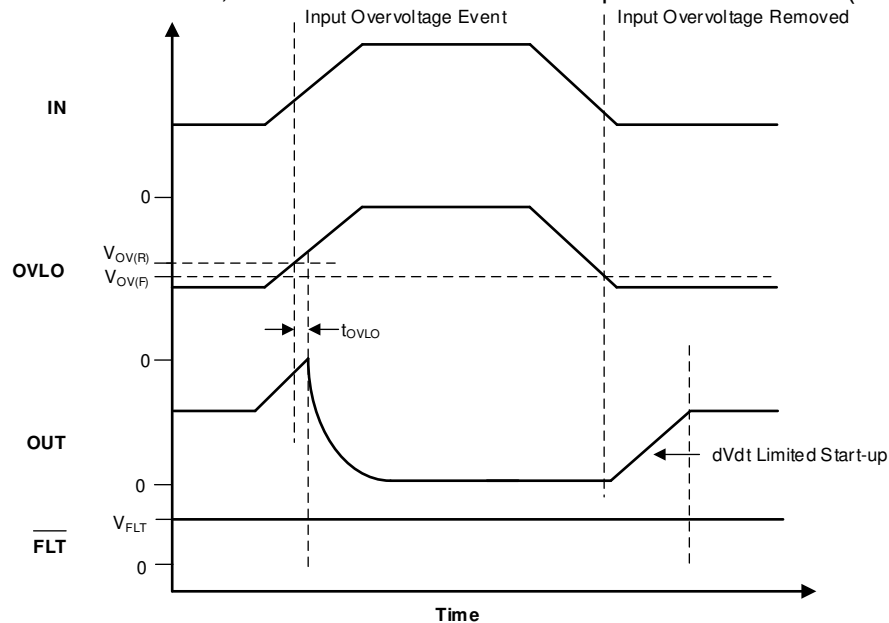
図 7-6. TPS25970x Overvoltage Lockout and Recovery

While recovering from an OVLO event, the TPS25974x variants start up with inrush control (dVdt).
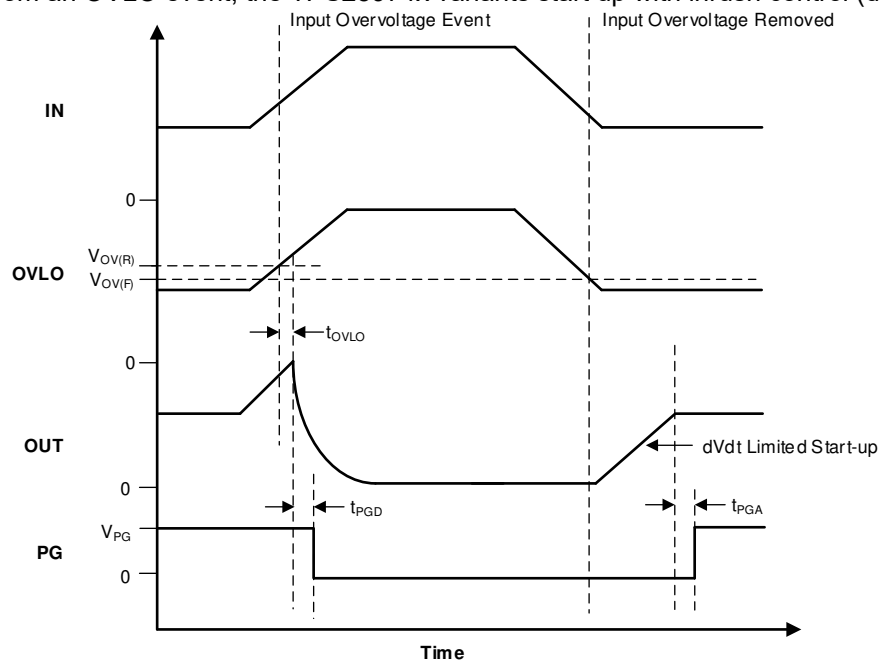
図 7-7. TPS25974x Overvoltage Lockout and Recovery

7.3.3 Overvoltage Clamp (OVC)

The TPS25972x variants implement a voltage clamp on the output to protect the system in the event of input overvoltage. When the device detects the input has exceeded the overvoltage clamp threshold (V_{OVC}), it quickly responds within t_{OVC} and stops the output from rising further. the device then regulates the HFET linearly to clamp the output voltage below V_{CLAMP} as long as an overvoltage condition is present on the input.

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5

If the part stays in clamping state for an extended period of time, there is higher power dissipation inside the part which can eventually lead to thermal shutdown (TSD). After the part shuts down due to TSD fault, it either stays latched off (TPS25972L variant) or restart automatically after a fixed delay (TPS25972A variant). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.
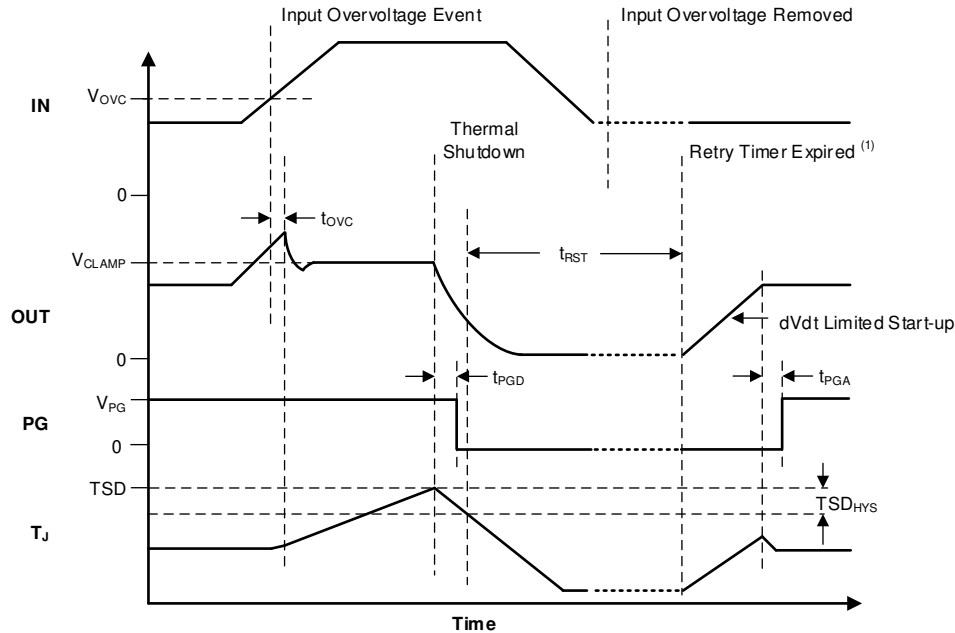
図 7-8. TPS25972x Overvoltage Response (Auto-Retry)

There are three available overvoltage clamp threshold options, which can be configured using the OVCSEL pin.

表 7-1. TPS25972x Overvoltage Clamp Threshold Selection

OVCSEL PIN CONNECTION	OVERVOLTAGE CLAMP THRESHOLD
Shorted to GND	3.89 V
Open	5.76 V
Connected to GND through a 390-kΩ resistor	13.88 V

7.3.4 Inrush Current, Overcurrent, and Short Circuit Protection

TPS2597xx incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
4. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short-circuits during steady-state

7.3.4.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors or cause the system power supply to droop leading to unexpected restarts elsewhere in the system or both. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. Use 式 3 to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$\text{SR (V/ms)} = \frac{\text{IINRUSH (mA)}}{\text{COUT (µF)}} \tag{3}$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. Use 式 4 to calculate the required C_{dVdt} capacitance to produce a given slew rate.

$$\text{CdVdt}\left(\text{pF}\right) = \frac{3300}{\text{SR (V/ms)}} \tag{4}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

注

For C_{dVdt} > 10nF, TI recommends to add a 100Ω resistor in series with the capacitor on the dVdt pin.

7.3.4.2 Circuit-Breaker

The circuit-breaker variants (TPS25974x) respond to output overcurrent conditions by turning off the output after a user-adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the fast-trip threshold (2 × I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal 2-µA pulldown current. If the load current drops below I_{LIM} before the ITIMER pin capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit breaker action is not engaged. This action allows short load transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and after it discharges by ΔV_{ITIMER}, the circuit breaker action turns off the HFET immediately. At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This action ensures the full blanking timer interval is provided for every overcurrent event. Use 式 5 to calculate the R_{ILM} value for an overcurrent threshold.

$$\text{RILM }(\Omega) = \frac{5747}{\text{ILIM (A)}} \tag{5}$$

注

1. Leaving the ILM pin Open sets the current limit to nearly zero and results in the part breaking the circuit with the slightest amount of loading at the output.
2. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There is a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. Use 式 6 to calculate the C_{ITIMER} value needed to set the desired transient overcurrent blanking interval.

$$\text{tITIMER (ms)} = \frac{\Delta \text{VITIMER (V)} \times \text{CITIMER (nF)}}{\text{IITIMER (µA)}} \tag{6}$$
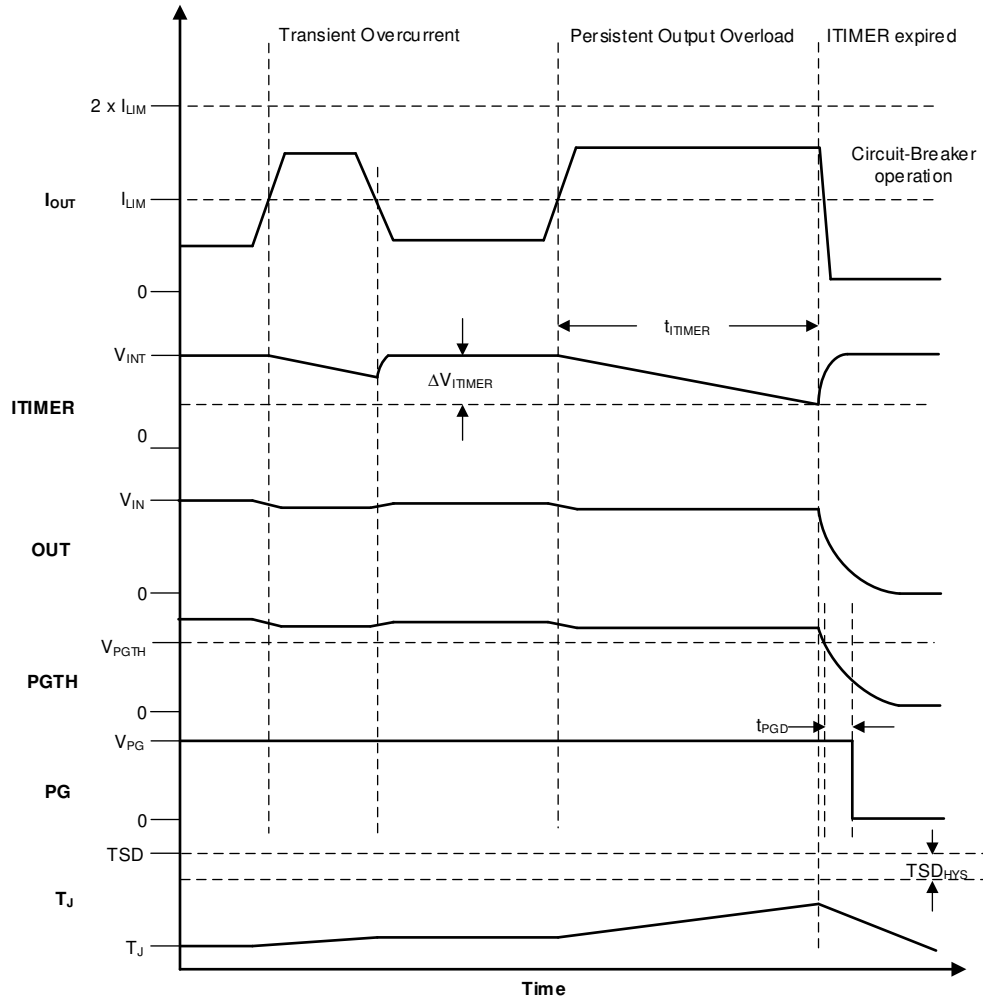
図 7-9. TPS25974x Overcurrent Response

注

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This action is not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval, but it also extends the time needed for the ITIMER cap to recharge up to V_{INT}. If the next overcurrent event occurs before the ITIMER cap is recharged fully, it takes less time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

After the part shuts down due to a circuit-breaker fault, it either stays latched off (TPS25974L variant) or restart automatically after a fixed delay (TPS25974A variant).

7.3.4.3 Active Current Limiting

The active current limit variants (TPS25970x and TPS25972x) respond to output overcurrent conditions by actively limiting the current after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold ($2 \times I_{LIM}$), the device starts discharging the ITIMER pin capacitor using an internal 2-µA pulldown current. If the load current drops below the overcurrent threshold before the ITIMER capacitor (C_{ITIMER})

discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the current limit action is not engaged. This event allows short load transient pulses to pass through the device without getting current limited. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and after it discharges by ΔV_{ITIMER}, the current limit starts regulating the HFET to actively limit the current to the set overcurrent threshold (I_{LIM}). At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This event ensures the full blanking timer interval is provided for every overcurrent event. Use 式 7 to calculate the R_{ILM} value for a desired overcurrent threshold.

$$RILM\ (\Omega) = \frac{5747}{ILIM\ (A)} \tag{7}$$

<div align="center">注</div>

1. Leaving the ILM pin open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
2. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the steady state current limit threshold (I_{LIM}).
3. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There's a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. Use 式 8 to calculate the C_{ITIMER} value needed to set the desired transient overcurrent blanking interval.

$$tITIMER\ (ms) = \frac{\Delta VITIMER\ (V) \times CITIMER\ (nF)}{IITIMER\ (\mu A)} \tag{8}$$

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5
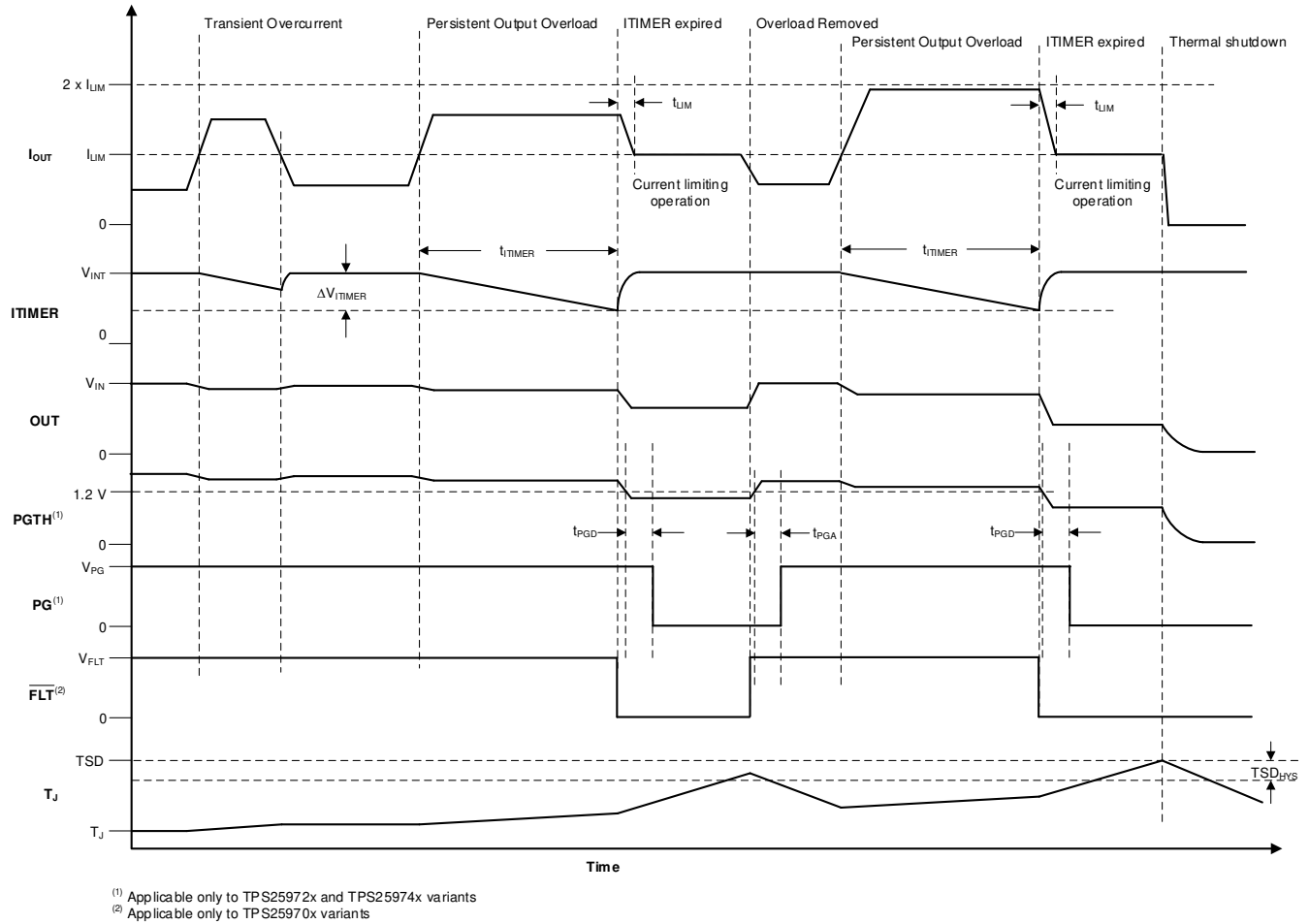
図 7-10. TPS25970x and TPS25972x Active Current Limit Response

---

注

1. Leave the ITIMER pin open to allow the part to limit the current with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This action is not a recommended mode of operation.
3. Active current limiting based on R_{ILM} is active during start-up for TPS25970x, TPS25972x (active current limit) as well as TPS25974x (circuit-breaker) variants. In case the start-up current exceeds I_{LIM}, the device regulates the current to the set limit. However, during start-up the current limit is engaged without waiting for the ITIMER delay.
4. For the TPS25972x variants, during overvoltage clamp condition, if an overcurrent event occurs, the current limit is engaged without waiting for the ITIMER delay.
5. Increasing the C_{ITIMER} value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it takes lesser time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

During active current limit, the output voltage drops, resulting in increased device power dissipation across the HFET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the HFET is turned off. After the part shuts down due to TSD fault, it either stays latched off (TPS2597xL variants) or restarts

automatically after a fixed delay (TPS2597xA variants). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

7.3.4.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the device triggers a fast-trip response to limit the current to a safe level. The internal fast-trip comparator employs a scalable threshold (I_{SC}) which is equal to 2 × I_{LIM}. This action enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short-circuits during steady state. The fixed fast-trip threshold is higher than the maximum recommended user adjustable scalable fast-trip threshold. After the current exceeds I_{SC} or I_{FT}, the HFET is turned off completely within t_{FT}. Thereafter, the devices tries to turn the HFET back on after a short de-glitch interval (30 µs) in a current limited manner instead of a dVdt limited manner. This action ensures that the HFET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device stays in current limit causing the junction temperature to rise and eventually enter thermal shutdown. For details on the device response to overtemperature, see *Overtemperature Protection (OTP)*.
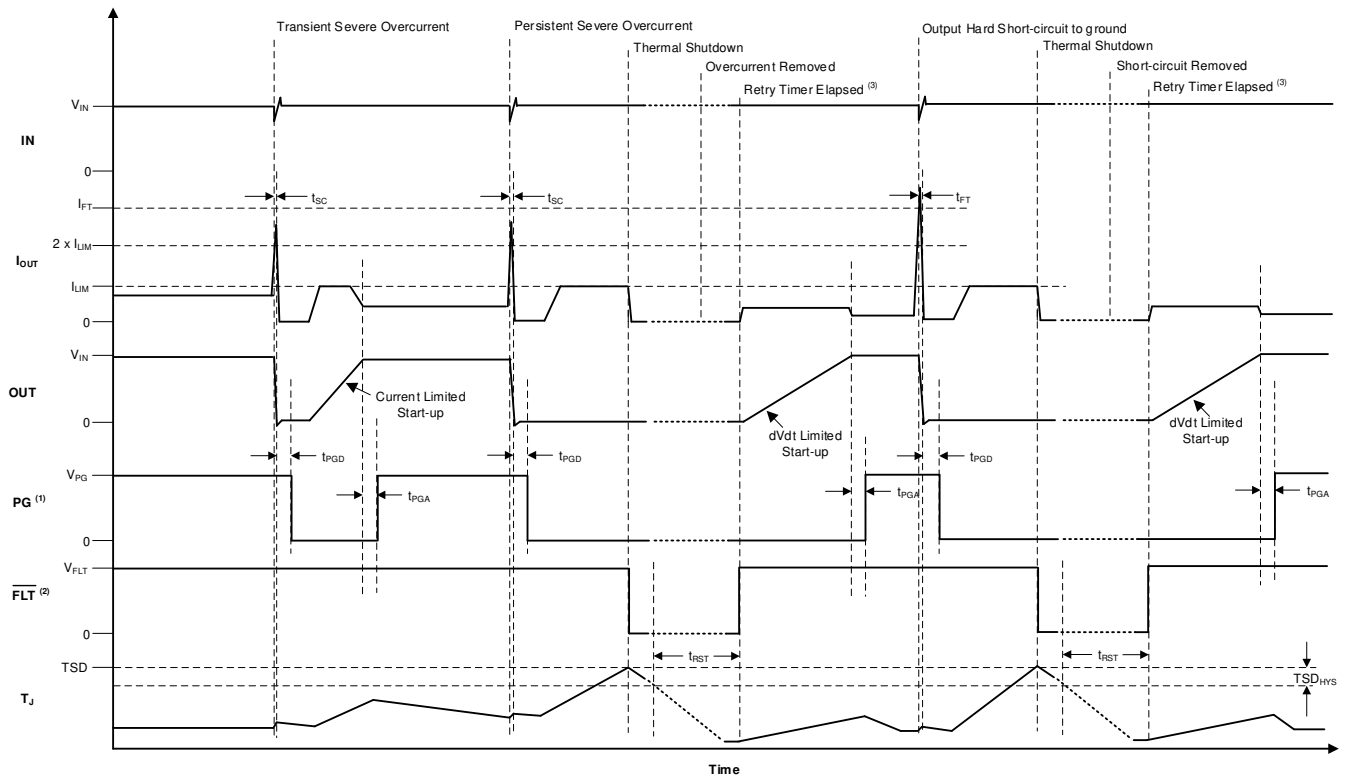
(1) Applicable only to TPS25972x and TPS25974x variants
(2) Applicable only to TPS25970x variants
(3) Applicable only to TPS2597xA variants

図 7-11. TPS2597xx Short-Circuit Response

7.3.5 Analog Load Current Monitor

The device allows the system to accurately monitor the output load current by providing an analog current sense output on the ILM pin, which is proportional to the current through the FET. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$IOUT\ (A) = \frac{VILM\ (\mu V)}{RILM\ (\Omega) \times GIMON\ (\mu A/A)} \tag{9}$$

The waveform below shows the ILM signal response to a load step at the output.
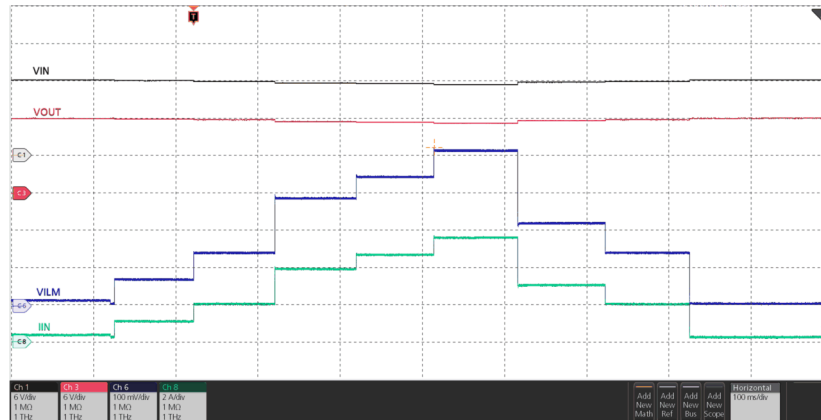
V_{IN} = 12 V, R_{ILM} = 715 Ω, I_{OUT} varied dynamically between 0 A and 5.5 A

図 7-12. Analog Load Current Monitor Response

注

The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50 pF for stable operation.

7.3.6 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD), thereby protecting the device from damage. The device does not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS2597xL (latch-off variant) detects thermal overload, it shuts down and remains latched-off until the device is power cycled or re-enabled. When the TPS2597xA (auto-retry variant) detects thermal overload, it remains off until it has cooled down by TSD_{HYS}. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

表 7-2. Thermal Shutdown

DEVICE	ENTER TSD	EXIT TSD
TPS2597xL (Latch-Off)	T_J ≥ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$
TPS2597xA (Auto-Retry)	T_J ≥ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$ or t_{RST} timer expired

7.3.7 Fault Response and Indication ($\overline{FLT}$)

表 7-3 summarizes the device response to various fault conditions. Additionally, an active low external fault indication ($\overline{FLT}$) pin is available on the TPS25970x variants.

表 7-3. Fault Summary

EVENT	PROTECTION RESPONSE	FAULT LATCHED INTERNALLY	$\overline{FLT}$ PIN STATUS [1]	$\overline{FLT}$ ASSERTION DELAY[1]
Overtemperature	Shutdown	Y	L	

表 7-3. Fault Summary (続き)

EVENT	PROTECTION RESPONSE	FAULT LATCHED INTERNALLY	$\overline{\text{FLT}}$ PIN STATUS [1]	$\overline{\text{FLT}}$ ASSERTION DELAY[1]
Undervoltage (UVP or UVLO)	Shutdown	N	H	
Input Overvoltage	Shutdown[1] [2]	N	H	
	Voltage Clamp[2]	N	N/A	
Transient Overcurrent (I_{LIM} < I_{OUT} < 2 × I_{LIM})	None	N	N	
Persistent Overcurrent	Circuit Breaker[3]	Y	N/A	
Persistent Overcurrent	Current Limit[4]	N	L	t_{ITIMER}
Output Short-Circuit to GND	Circuit Breaker followed by Current Limit	N	H	
ILM Pin Open (During Steady State)	Shutdown	N	L	t_{ITIMER}
ILM Pin Shorted to GND	Shutdown	Y	L	t_{ITIMER}

(1)   Applicable to TPS25970x variants only.
(2)   Applicable to TPS25972x variants only.
(3)   Applicable to TPS25974x variants only.
(4)   Applicable to TPS25970x and TPS25972x variants only.

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}. This action also releases the $\overline{\text{FLT}}$ pin for the TPS25970x variants and resets the t_{RST} timer for the TPS2597xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This fact is true for both TPS2597xL (latch-off) and TPS2597xA (auto-retry) variants.

For TPS2597xA (auto-retry) variants, on expiry of the t_{RST} timer after a fault, the device restarts automatically and the $\overline{\text{FLT}}$ pin is de-asserted (TPS25970A variant).

7.3.8 Power-Good Indication (PG)

The TPS25972x and TPS25974x variants provide an active high digital output (PG) which serves as a power-good indication signal and is asserted high depending on the voltage at the PGTH pin along with the device state information. The PG is an open-drain pin and must be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the HFET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the voltage at PGTH is above $V_{PGTH(R)}$, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation, the voltage at PGTH falls below $V_{PGTH(F)}$, or the device detects a fault (except overcurrent). The PG de-assertion de-glitch time is t_{PGD}.
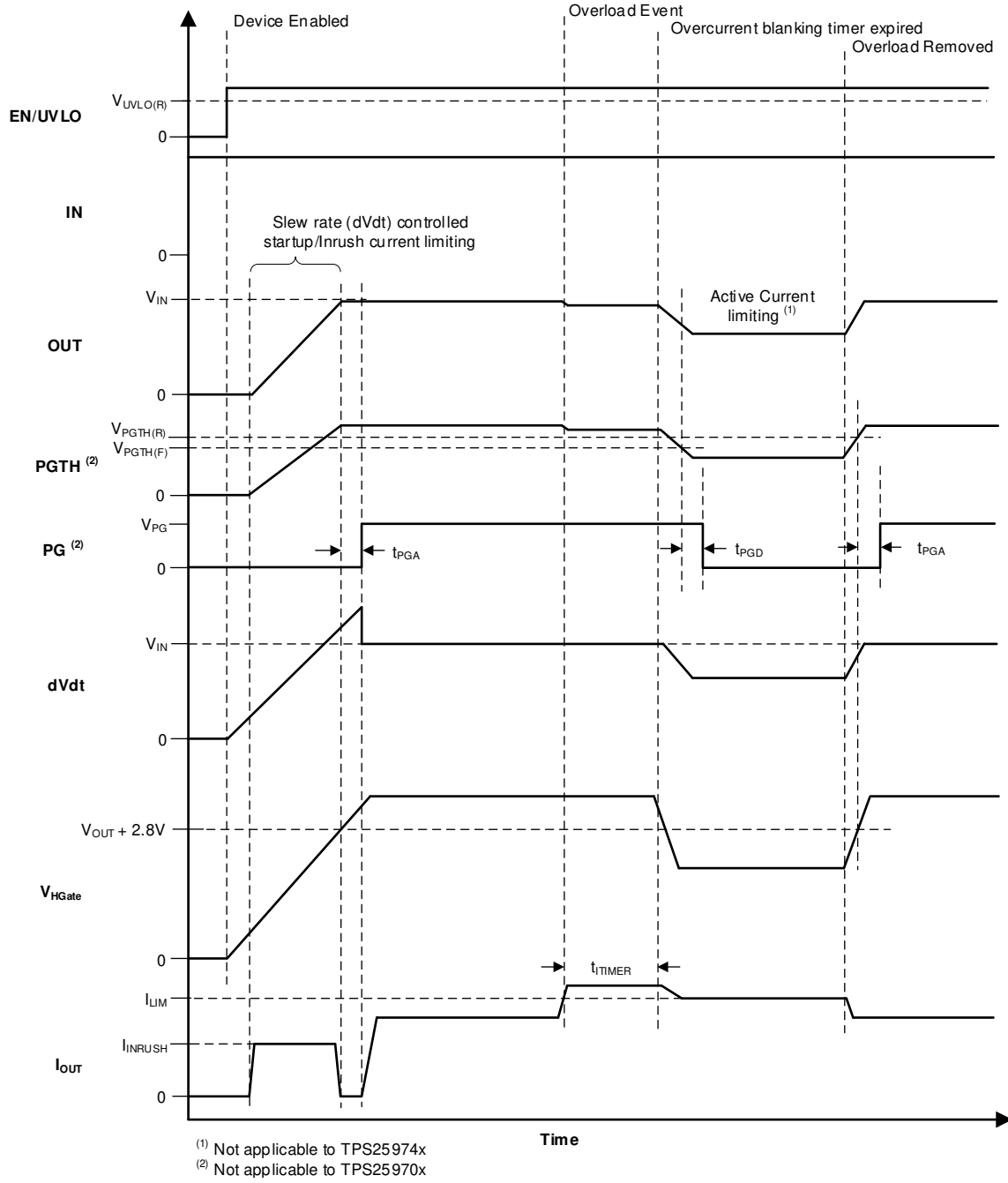
図 7-13. TPS25972x, TPS25974x PG Timing Diagram

表 7-4. TPS25972x and TPS25974x PG Indication Summary

EVENT	DEVICE STATUS	PG PIN STATUS	PG PIN TOGGLE DELAY
Undervoltage (UVP or UVLO)	OFF	L	
Overvoltage (TPS25972x only)	ON (Clamping)	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Overvoltage (TPS25974x only)	OFF	L	t_{PGD}
Steady state	ON	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Transient overcurrent	ON	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Persistent overload (TPS25972x only)	ON (Current Limiting)	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Persistent overload (TPS25974x only)	OFF (Circuit-Breaker)	L	t_{PGD}
Output short-circuit to GND	Fast-trip followed by Current Limit	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
ILM pin open	OFF	L (If PGTH < 1.1 V)	t_{PGD} + t_{ITIMER}
ILM pin shorted to GND	OFF	L	t_{PGD}
Overtemperature	OFF	L	t_{PGD}

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

7.4 Device Functional Modes

The TPS25970x and TPS25974x variants have only one functional mode that applies when operated within the recommended operating conditions.

The TPS25972x variants have three different functional modes depending on the OVCSEL pin connection.

表 7-5. TPS25972x Overvoltage Clamp Threshold Selection

OVCSEL PIN CONNECTION	OVERVOLTAGE CLAMP THRESHOLD
Shorted to GND	3.89 V
Open	5.76 V
Connected to GND through a 390-kΩ resistor	13.88 V

8 Application and Implementation

8.1 Application Information

The TPS2597xx is a 2.7-V to 23-V, 7-A eFuse that is typically used for power rail protection applications. The device operates from 2.7 V to 23 V with adjustable overvoltage and undervoltage protection. The device provides ability to control inrush current and protection against overcurrent conditions. The device can be used in a variety of systems such as adapter input protection, server, PC motherboard, add-on cards, enterprise storage – RAID/HBA/SAN/eSSD, retail point-of-sale terminals, smartphones, and tablets. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, *TPS2597xx Design Calculator*, is available in the web product folder.

8.1.1 Single Device, Self-Controlled
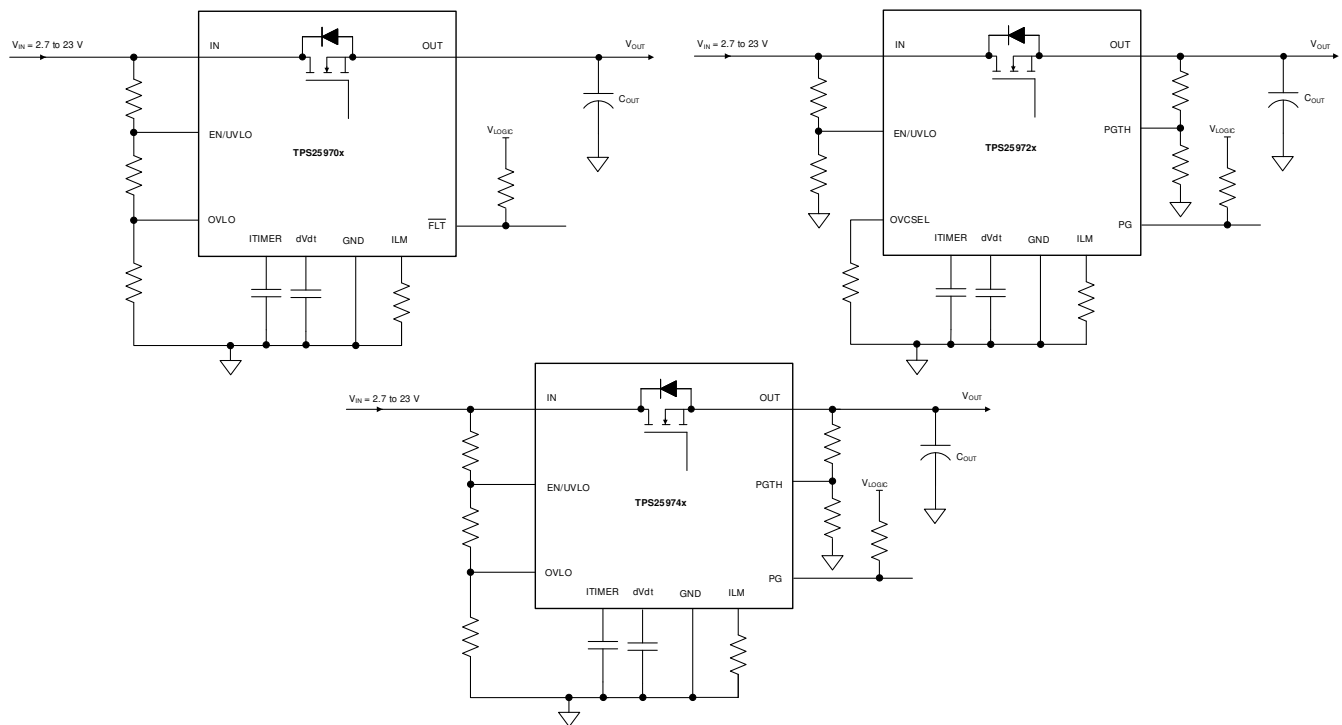
図 8-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

ILM pin can be connected to the MCU ADC input for current monitoring purpose.

注

TI recommends to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation.

For the TPS25972x and TPS25974x variants, either V_{IN} or V_{OUT} can be used to drive the PGTH resistor divider depending on which supply must be monitored for Power Good indication.

8.2 Typical Application

TPS2597xx can be used for server add-on card input power protection. During overcurrent or short-circuit event at load side, TPS2597xx can quickly respond to this fault event by turning off the device and thus protect the load from damage as well as prevent input supply from drooping. The ITIMER feature allows short duration peak currents to pass through without tripping the eFuse, thereby meeting the transient load current profile of these cards.
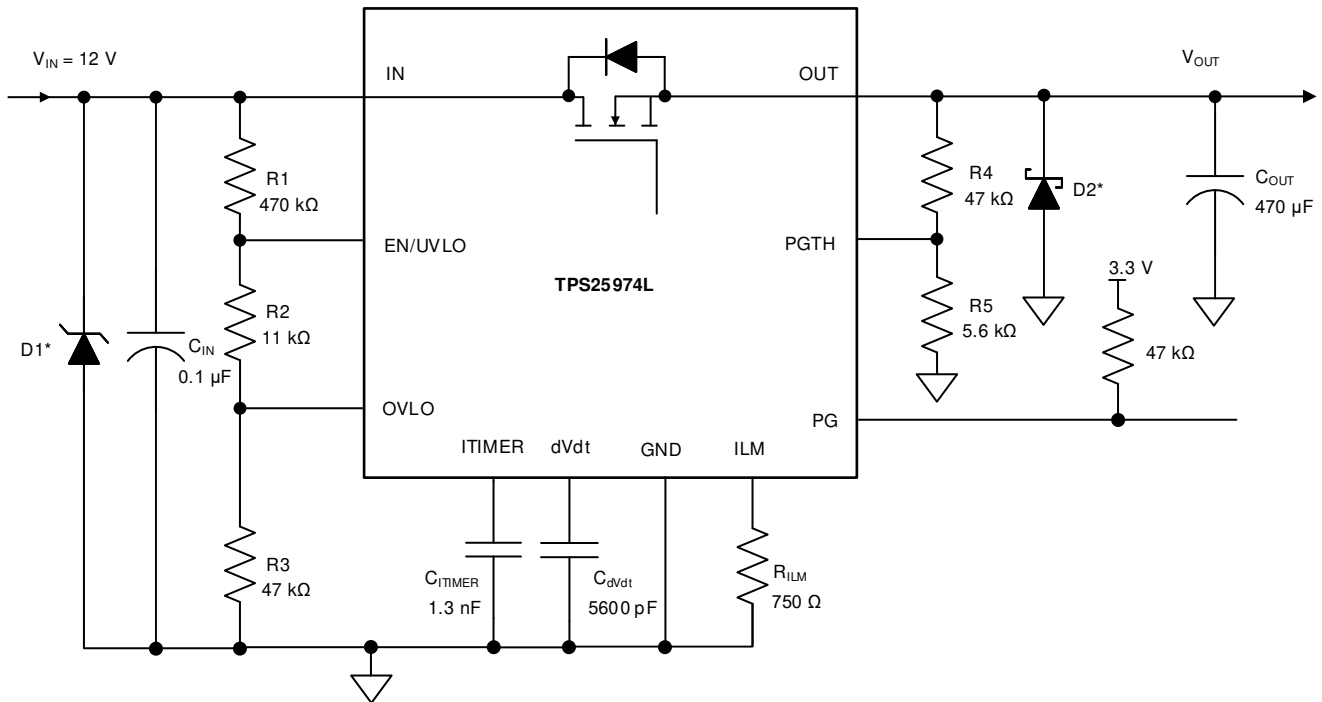
* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

図 8-2. Server Add-on Card Input Power Protection

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Input supply voltage (V_{IN})	12 V
Undervoltage threshold ($V_{IN(UV)}$)	10.8 V
Overvoltage threshold ($V_{IN(OV)}$)	13.2 V
Output Power Good threshold (V_{PG})	11.4 V
Maximum continuous current	7 A
Load transient blanking interval (t_{ITIMER})	1 ms
Output capacitance (C_{OUT})	470 µF
Output rise time (t_R)	20 ms
Overcurrent threshold (I_{LIM})	7.7 A
Overcurrent response	Circuit breaker
Fault response	Latch-off

8.2.2 Detailed Design Procedure

8.2.2.1 Device Selection

Because the application requires circuit-breaker response to overcurrent with latch-off response after a fault, the TPS25974L variant is selected after referring to the *Device Comparison Table*.

8.2.2.2 Setting Undervoltage and Overvoltage Thresholds

The supply undervoltage and overvoltage thresholds are set using the resistors R1, R2, and R3, whose values can be calculated using 式 10 and 式 11:

$$VIN(UV) = \frac{VUVLO(R) \times (R1 + R2 + R3)}{R2 + R3} \tag{10}$$

$$VIN(OV) = \frac{VOV(R) \times (R1 + R2 + R3)}{R3} \tag{11}$$

Where $V_{UVLO(R)}$ is the UVLO rising threshold and $V_{OV(R)}$ is the OVLO rising threshold. Because R1, R2, and R3 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1, R2, and R3 from the power supply is IR123 = V_{IN} / (R1 + R2 + R3). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the leakage current expected on the EN/UVLO and OVLO pins.

From the device electrical specifications, both the EN/UVLO and OVLO leakage currents are 0.1 µA (maximum), $V_{OV(R)}$ = 1.2 V and $V_{UVLO(R)}$ = 1.2 V. From design requirements, $V_{IN(OV)}$ = 13.2 V and $V_{IN(UV)}$ = 10.8 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equations to solve for R2 = 10.7 kΩ and R3 = 48 kΩ.

Using the closest standard 1% resistor values, we get R1 = 470 kΩ, R2 = 11 kΩ, and R3 = 47 kΩ.

8.2.2.3 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of the device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR\ (V/ms) = \frac{VIN\ (V)}{tR\ (ms)} = \frac{12\ V}{20\ ms} = 0.6\ V/ms \tag{12}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$CdVdt\ (pF) = \frac{3300}{SR\ (V/ms)} = \frac{3300}{0.6} = 5500\ pF \tag{13}$$

Choose the nearest standard capacitor value as 5600 pF.

For this slew rate, the inrush current can be calculated as:

$$IINRUSH\ (mA) = SR\ (V/ms) \times COUT\ (\mu F) = 0.6 \times 470 = 282\ mA \tag{14}$$

The average power dissipation inside the part during inrush can be calculated as:

$$PDINRUSH\ (W) = \frac{IINRUSH\ (A) \times VIN\ (V)}{2} = \frac{0.282 \times 12}{2} = 1.69\ W \tag{15}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. 図 8-3 shows the thermal shutdown limit. For 1.69 W of power, the shutdown time is more than 10 s, which is very large as compared to t_R = 20 ms. Therefore, it is safe to use 20 ms as the start-up time for this application.
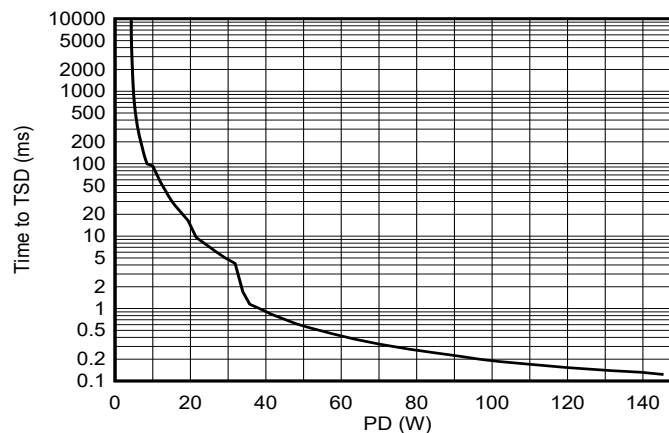
図 8-3. Thermal Shut-Down Plot During Inrush

注

In some systems, there can be active load circuits (for example, DC-DC converters) with low turn-on threshold voltages which can start drawing power before the eFuse has completed the inrush sequence. This action can cause additional power dissipation inside the eFuse during start-up and can lead to thermal shutdown. TI recommends to use the Power Good (PG) pin of the eFuse to enable and disable the load circuit. This action ensures that the load is turned on only when the eFuse has completed its start-up and is ready to deliver full power without the risk of hitting thermal shutdown.

8.2.2.4 Setting Power-Good Assertion Threshold

The Power Good assertion threshold can be set using the resistors R4 and R5 connected to the PGTH pin, whose values can be calculated as:

$$VPG = \frac{VPGTH(R) \times (R4 + R5)}{R5} \tag{16}$$

Because R4 and R5 leak the current from the output rail V_{OUT}, these resistors must be selected to minimize the leakage current. The current drawn by R4 and R5 from the power supply is IR45 = V_{OUT} / (R4 + R5). However, leakage currents due to external active components connected to the resistor string can add error to these

calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the PGTH leakage current expected.

From the device electrical specifications, PGTH leakage current is 1 µA (maximum), $V_{PGTH(R)}$ = 1.2 V and from design requirements, V_{PG} = 11.4 V. To solve the equation, first choose the value of R4 = 47 kΩ and calculate R5 = 5.52 kΩ. Choose the nearest 1% standard resistor value as R5 = 5.6 kΩ.

8.2.2.5 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection (Circuit Breaker) threshold can be set using the R_{ILM} resistor whose value can be calculated as:

$$\text{RILM} \ (\Omega) = \frac{5747}{\text{ILIM (A)}} = \frac{5747}{7.7 \text{ A}} = 746.4 \ \Omega \tag{17}$$

Choose nearest 1% standard resistor value as 715 Ω.

8.2.2.6 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

$$\text{CITIMER (nF)} = \frac{\text{tITIMER (ms)} \times \text{IITIMER (}\mu\text{A)}}{\Delta \text{ VITIMER (V)}} = \frac{1 \times 2}{1.52} = 1.32 \text{ nF} \tag{18}$$

Choose nearest standard capacitor value as 1.3 nF.

8.2.3 Application Curves

図 8-4. Power Up

図 8-5. Transient Overload

図 8-6. Circuit Breaker Response
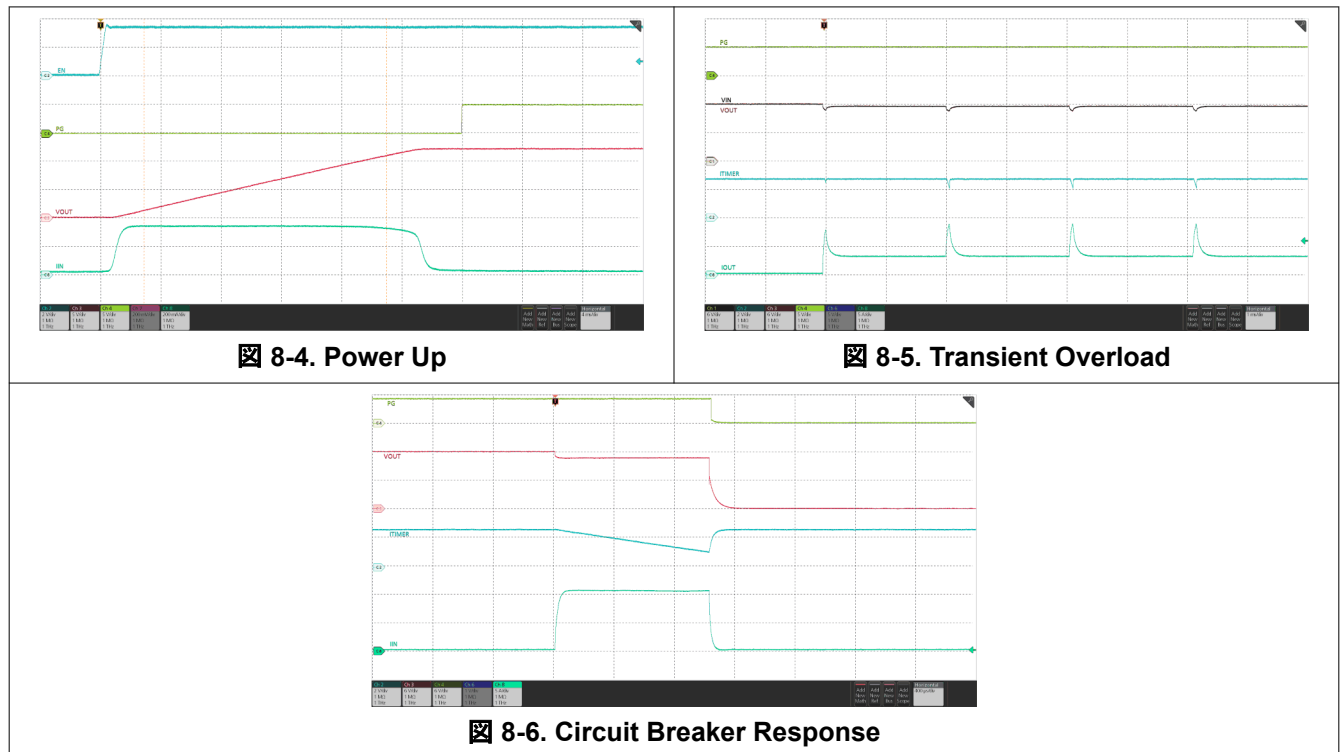
8.3 Parallel Operation

Applications that need higher steady current can use two TPS25974x devices connected in parallel as shown in 図 8-7. In this configuration, the first device turns on initially to provide the inrush current control. The second device is held in an OFF state by driving its EN/UVLO pin low using the PG signal of the first device. After the inrush sequence is complete, the first device asserts its PG pin high and turns on the second device. The

second device asserts its PG signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady state current.

After in steady state, both devices share current nearly equally. There can be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

図 8-7. Two Devices Connected in Parallel for Higher Steady State Current Capability

The waveforms below illustrate the behavior of the parallel configuration during start-up as well as during steady state.

Product Folder Links: *TPS2597*

English Data Sheet: *SLVSGG5*

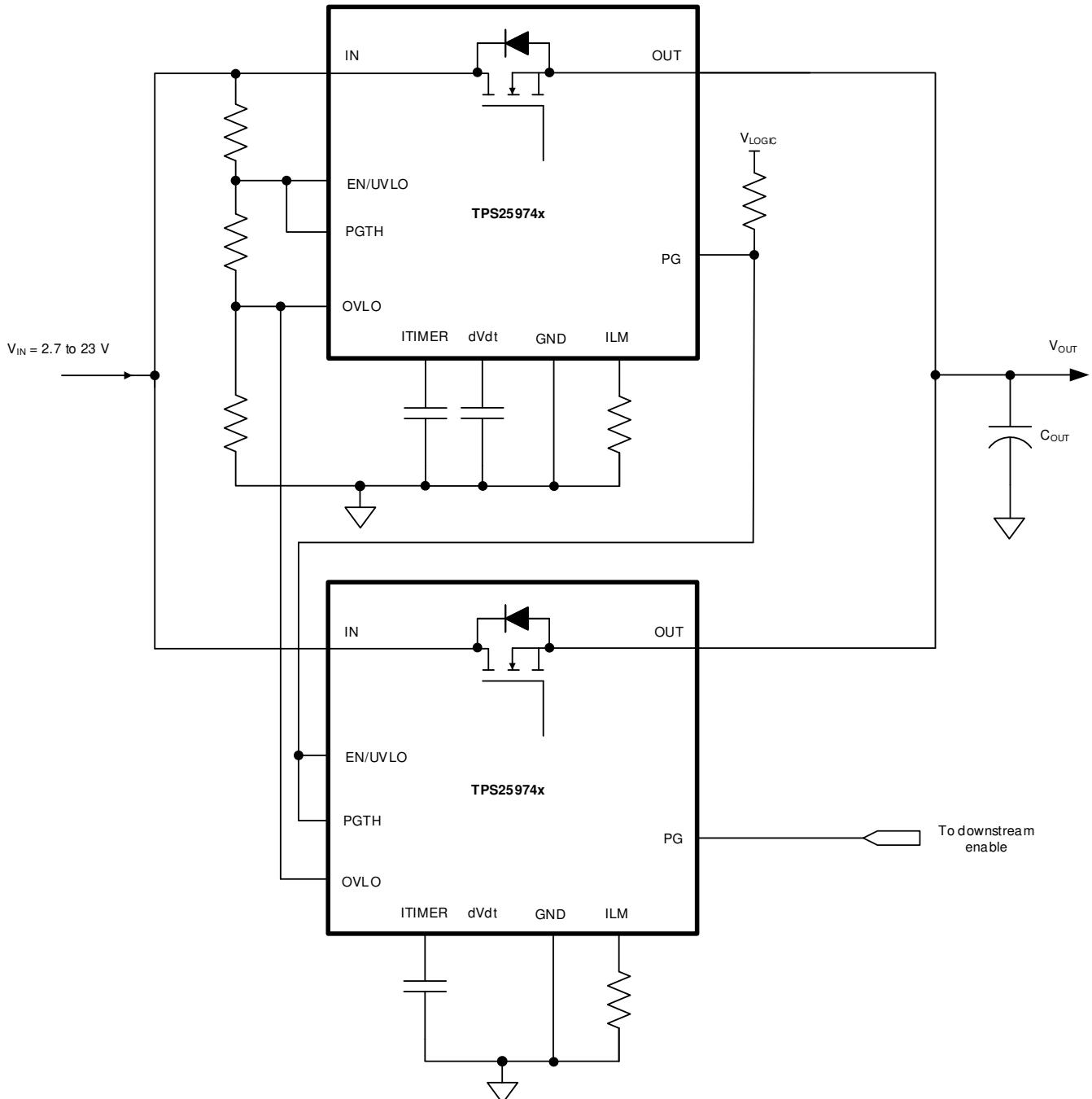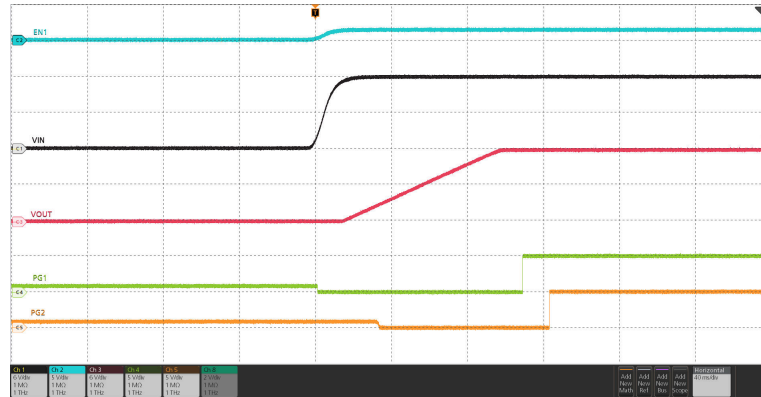**図 8-8. Parallel Devices Sequencing During Start-Up**
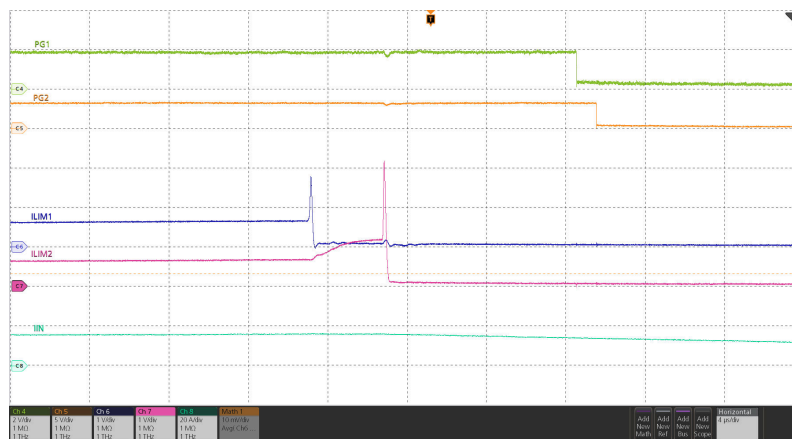
図 8-9. Parallel Devices Load Current During Steady State and Overload

8.4 Power Supply Recommendations

The TPS2597xx devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 23 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

8.4.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

Use 式 19 to estimate the approximate value of input capacitance:

$$VSPIKE(Absolute) \ = VIN + ILOAD \times \sqrt{\frac{LIN}{CIN}} \tag{19}$$

where

- – V_{IN} is the nominal supply voltage.
- – I_{LOAD} is the load current.
- – L_{IN} equals the effective inductance seen looking into the source.
- – C_{IN} is the capacitance present at the input.
- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

図 8-10 shows the circuit implementation with optional protection components.

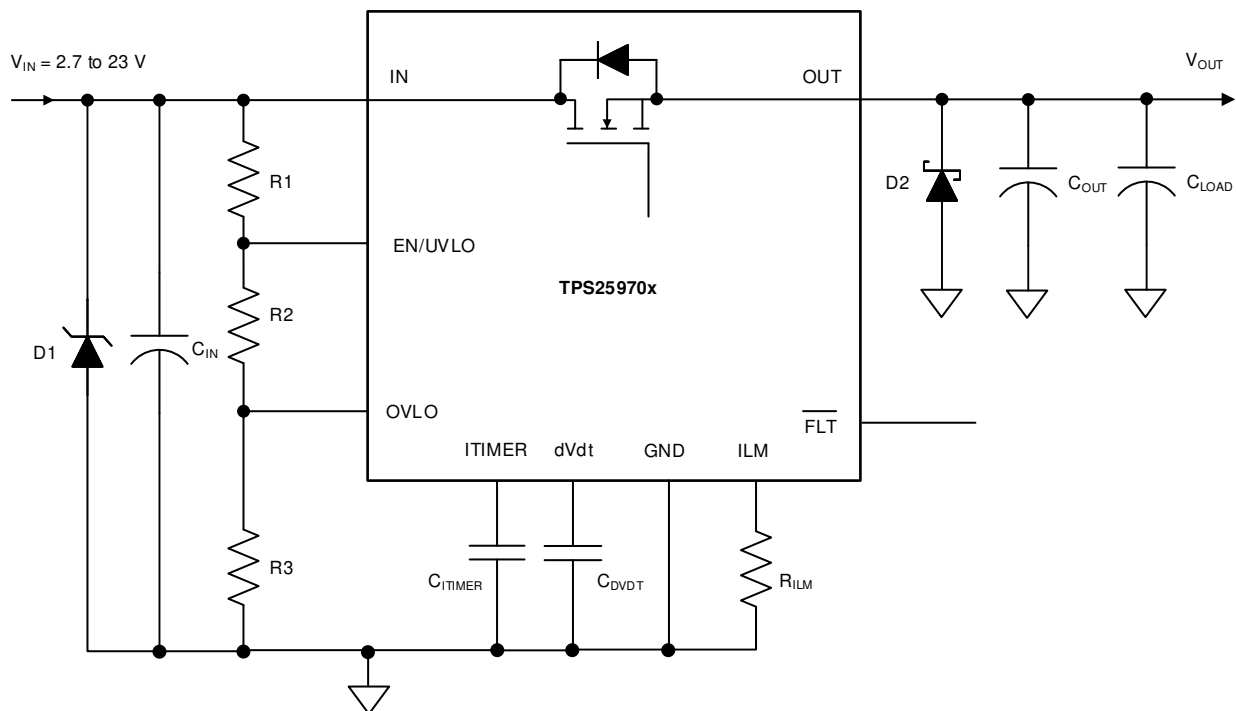図 **8-10. Circuit Implementation With Optional Protection Components**

8.4.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.5 Layout

8.5.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - C_{ITIMER}
  - Resistors for the EN/UVLO, OVLO/OVCSEL, and PGTH pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the RILM, CITIMER and CdVdt components to the device must be as short as possible to reduce parasitic effects on the current limit, overcurrent blanking interval and soft start timing. It's recommended to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation. These traces must not have any coupling to switching signals on the board.
- Because the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads. TI also recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin, and the GND terminal of the IC.
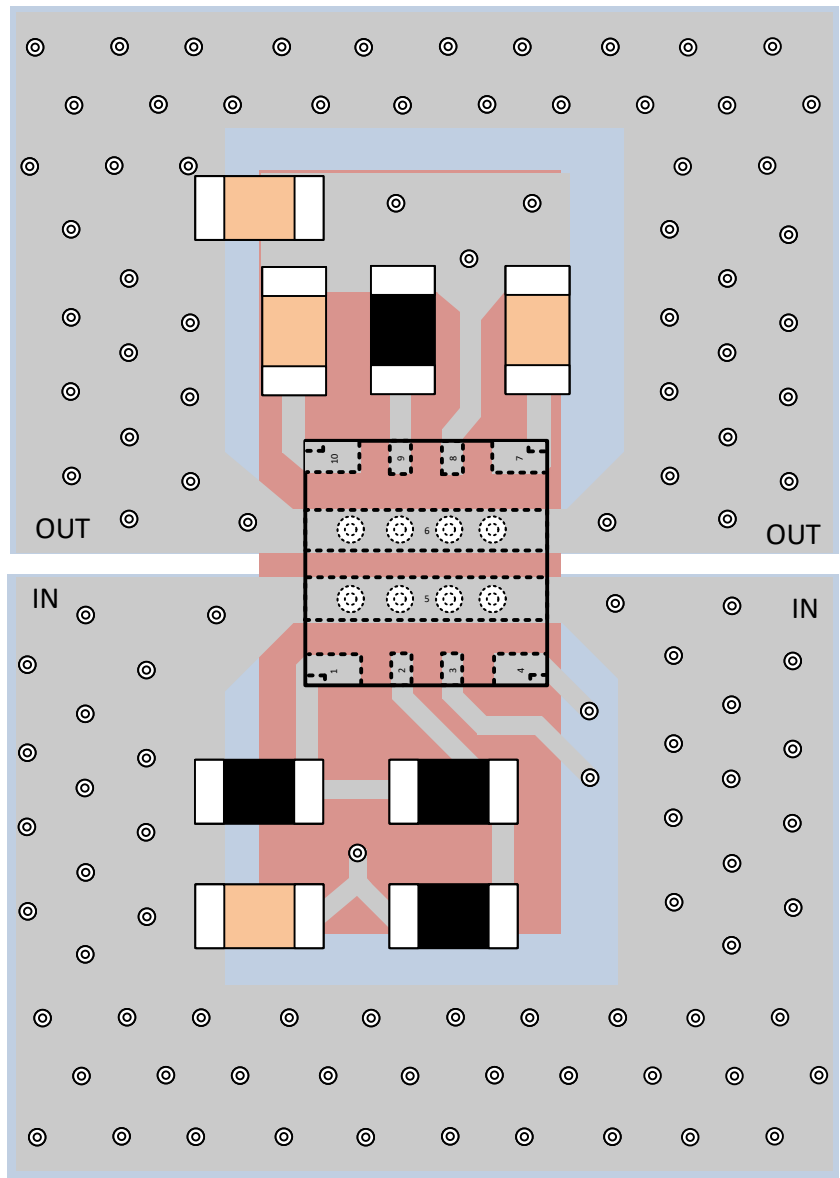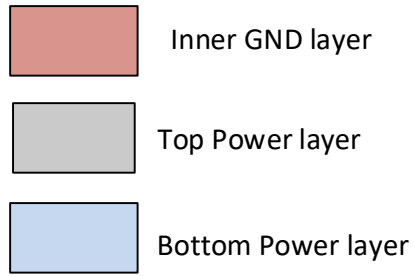
8.5.2 Layout Example

図 8-11. Layout Example - Single TPS25974x With PGTH Referred to OUT

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:
- Texas Instruments, *TPS2597EVM eFuse Evaluation Board* user's guide
- Texas Instruments, *TPS2597xx Design Calculator*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

HotRod™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (April 2023) to Revision D (May 2025)   **Page**
- Added maximum input voltage rising slew rate = 100V/µs to *Absolute Maximum Ratings* section....................5
- Added maximum input voltage falling slew rate = 10V/µs to *Absolute Maximum Ratings* section.....................5

Changes from Revision B (January 2022) to Revision C (April 2023) **Page**

Product Folder Links: *TPS2597*

English Data Sheet: SLVSGG5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25970ARPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KNH
TPS25970ARPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KNH
TPS25970LRPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KOH
TPS25970LRPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KOH
TPS25972ARPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KPH
TPS25972ARPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KPH
TPS25972LRPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KQH
TPS25972LRPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KQH
TPS25974ARPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KRH
TPS25974ARPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KRH
TPS25974LRPWR	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KSH
TPS25974LRPWR.A	Active	Production	VQFN-HR (RPW) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2KSH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

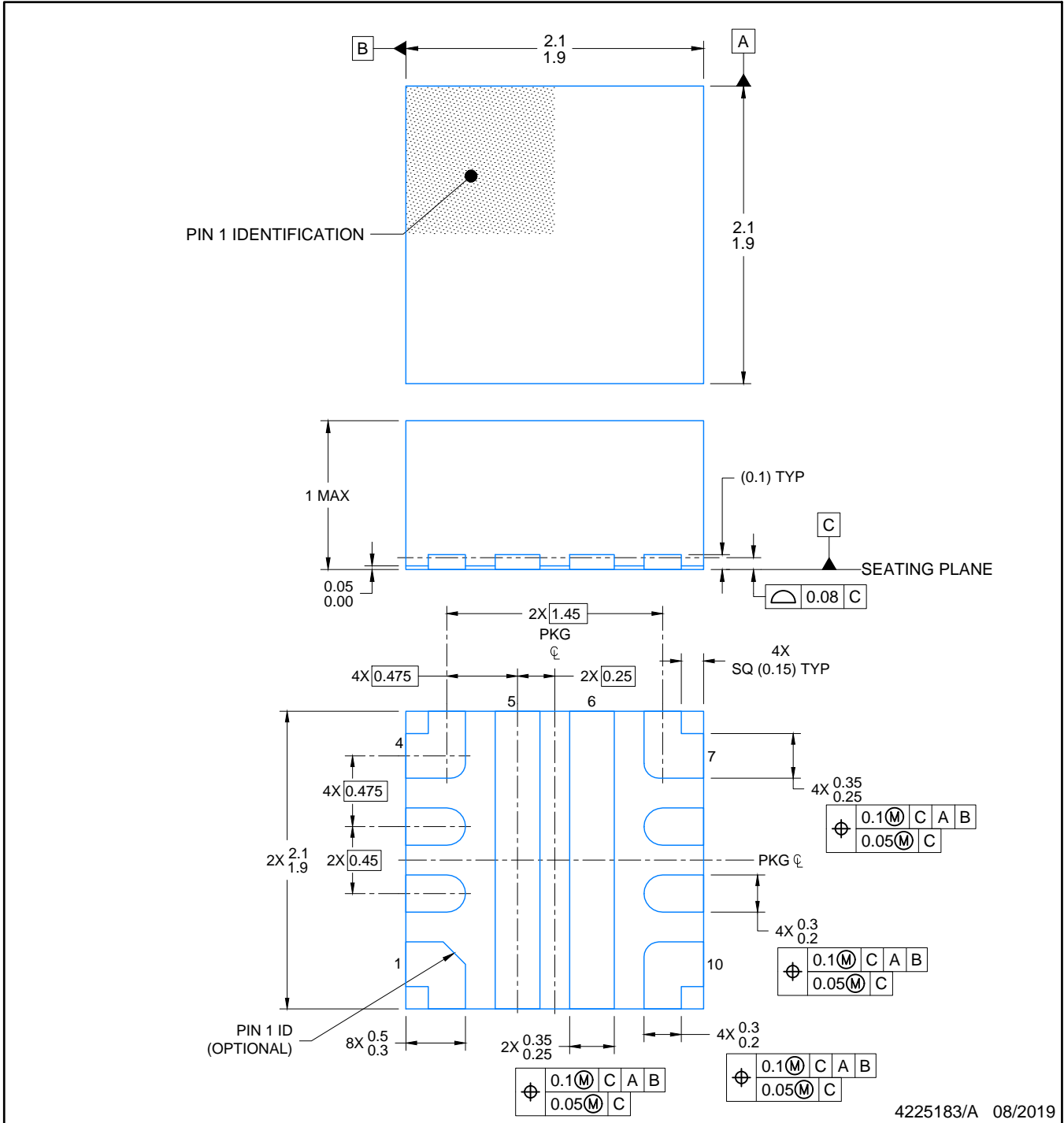Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25970ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25970LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25972ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25972LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25974ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25974LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25970ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS25970LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS25972ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS25972LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS25974ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS25974LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0

B | 2.1 / 1.9 | A

PIN 1 IDENTIFICATION

2.1
1.9

1 MAX

(0.1) TYP

0.05
0.00

C

SEATING PLANE

⌒ 0.08 C

2X 1.45
PKG ℄

4X 0.475

2X 0.25

4X
SQ (0.15) TYP

5   6

4

7

4X 0.475

4X 0.35
0.25

⊕ | 0.1 Ⓜ C A B
    | 0.05 Ⓜ C

2X 2.1
1.9

2X 0.45

PKG ℄

4X 0.3
0.2

1

10

⊕ | 0.1 Ⓜ C A B
    | 0.05 Ⓜ C

PIN 1 ID
(OPTIONAL)

8X 0.5
0.3

2X 0.35
0.25

4X 0.3
0.2

⊕ | 0.1 Ⓜ C A B
    | 0.05 Ⓜ C

⊕ | 0.1 Ⓜ C A B
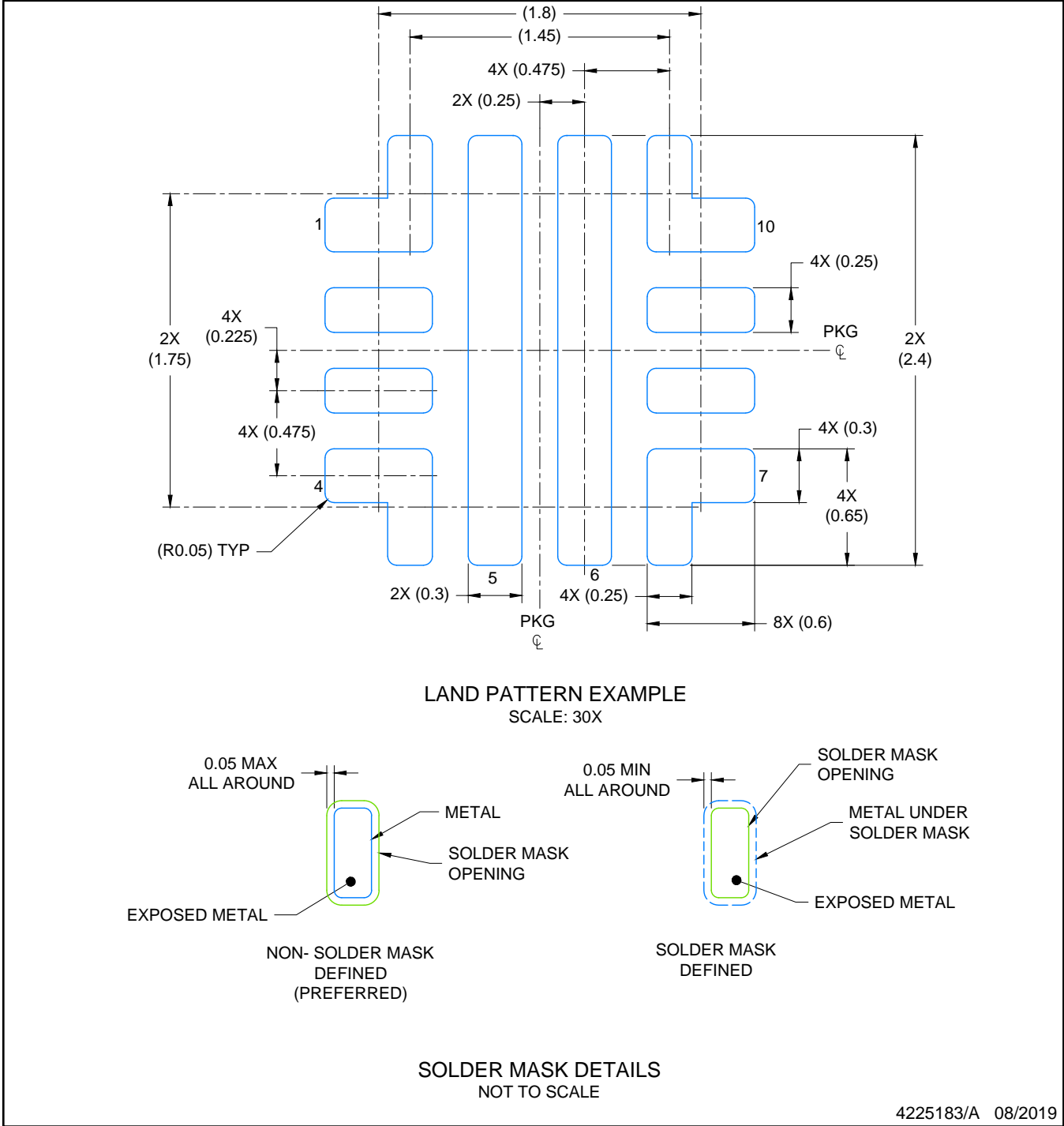 | 0.05 Ⓜ C

4225183/A   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

LAND PATTERN EXAMPLE
SCALE: 30X

SOLDER MASK DETAILS
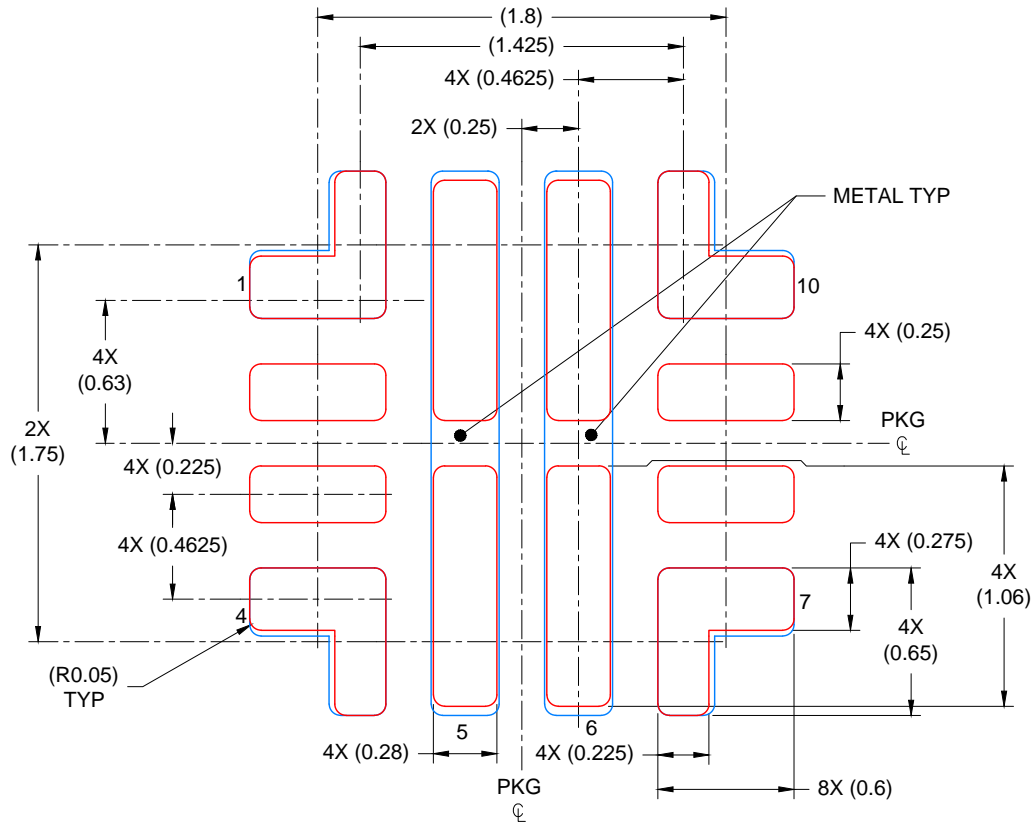NOT TO SCALE

4225183/A   08/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A   08/2019

NOTES: (continued)

5.   Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。