TPS3423、TPS3424、Nano-Power プッシュボタン コントローラ、バッテリ フレッシュネス シールのための遅延設定が可能

1 特長

- 動作電圧範囲:1V～6V
- ナノアンペア単位の電源電流:18nA (標準値)
- プッシュボタン ピンの HBM ESD 定格:±8kV
- プログラム可能な短押しおよび長押し時間
  - TPS3423、TPS3424 固定タイミング オプション:
    - 短押し時間:50msec～13sec
    - 長押し時間:1sec～30sec
    - タイマ精度 (最大値):±10%
  - TPS3424:外付けコンデンサを使ってユーザーによるプログラムが可能 (50msec～50sec)
- 出力構成:
  - リセット構成:
    - プッシュプル / オープン ドレイン、アクティブ High / Low
    - ラッチあり / ラッチなし
    - ラッチなしバージョンでは、100msec～1sec のパルス オプション
  - $\overline{\text{INT}}$ 設定:
    - オープン ドレイン、アクティブ Low
    - ラッチなし (100msec～1sec のパルス幅)
- KILL 機能:ホストがリセット出力を制御可能
- ピン互換の 8 ピンおよび 6 ピンの DRL パッケージで供給

2 アプリケーション

- ウェアラブル
- ゲーム機
- ホーム シアター エンターテインメント
- プリンタ
- ヘルスケア
- ポータブル エレクトロニクス
- ファクトリ オートメーション / 制御

3 概要

TPS3423 および TPS3424 はプッシュボタン コントローラであり、短押しと長押しをさまざまな条件で独立して検出できます。これらのデバイスは、プッシュボタンごとに最大 2 つの出力 (RESET と $\overline{\text{INT}}$) を備えており、電圧レギュレータやサーキット ブレーカのイネーブル、指定された押下期間に対するワンショットの生成、マイクロコントローラへの割り込みの送信など、さまざまな使用事例に使用できます。このデバイスは、短押しと長押しの両方に対して割り込みパルスを生成し、マイクロコントローラに通知します。RESET 出力は、デバイス構成に基づいて状態が変化します。

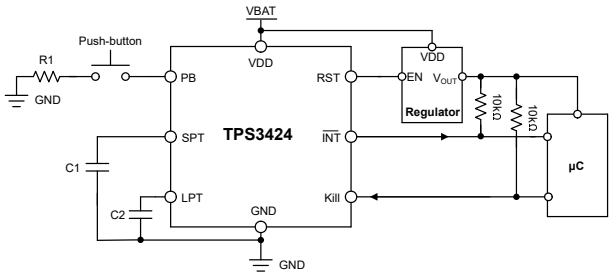
18nA の非常に低い消費電力により、バッテリ駆動デバイスの製品保管期間の延長に貢献します。このデバイスは、必要なボタンの押下が検出されるまで、電源ツリーが無効の状態を維持します。この機能は、バッテリー フレッシュネス シールと呼ばれています。

TPS3423/4 は、短押しおよび長押しの時間について固定タイミング オプションで供給されます。設計者にフレキシビリティを提供するため、TPS3424 は、外付けコンデンサにより短押しおよび長押しの時間をユーザーがプログラムすることも可能です。TPS3424 の KILL ピンを使用すると、マイクロコントローラからのフィードバックによる RESET のデアサートが可能になります。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ (3)
TPS3423	DRL (SOT-5X3)	2.10mm × 1.60mm
	DRL (SOT-5X3) (2)	1.60mm × 1.20mm
TPS3424	DRL (SOT-5X3)	2.10mm × 1.60mm
	DRL (SOT-5X3) (2)	1.60mm × 1.20mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) プレビュー版パッケージ
(3) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます



TPS3424 代表的なアプリケーションの図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison

図 4-1 and 図 4-3 shows the device nomenclature of the TPS3423 and TPS3424, for output / push-button input, short press and long press, interrupt, reset and kill timing options. 図 4-2 extends nomenclature of TPS3423 to provide 2 different timing option for channels. Refer セクション 7 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.

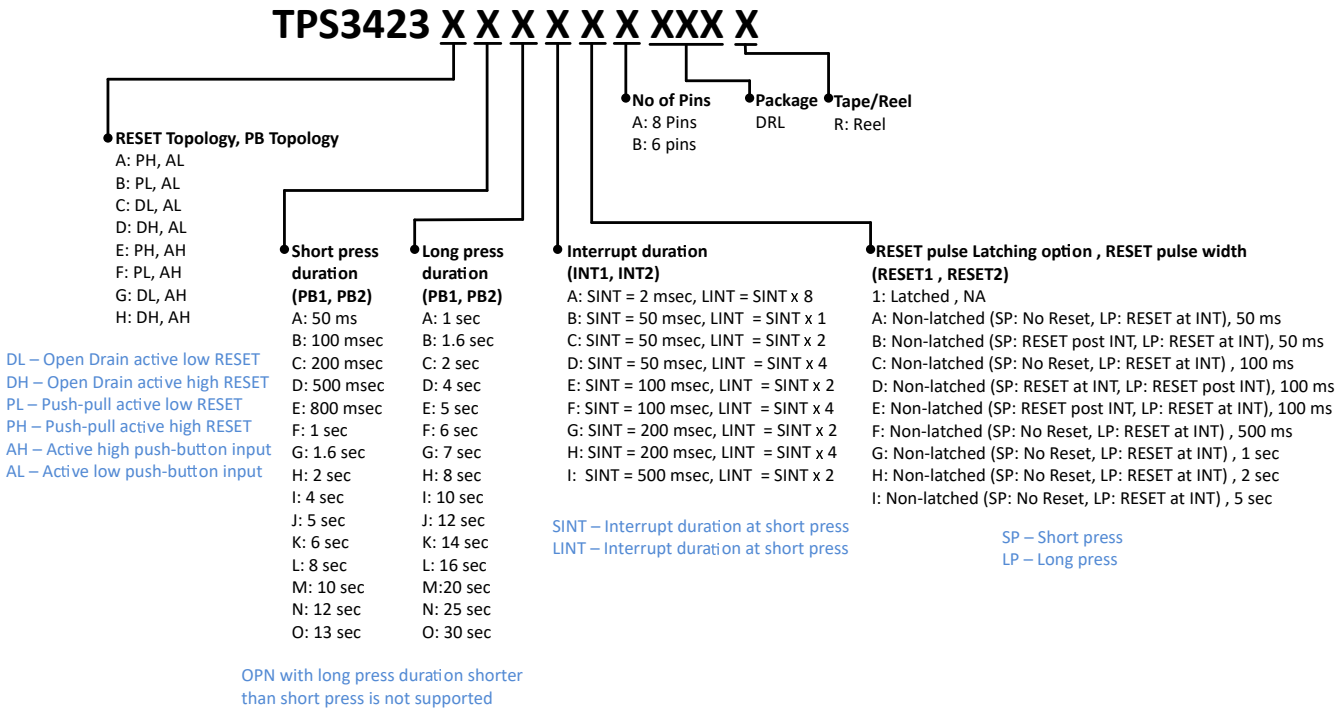

図 4-1. Dual Push-Button Nomenclature

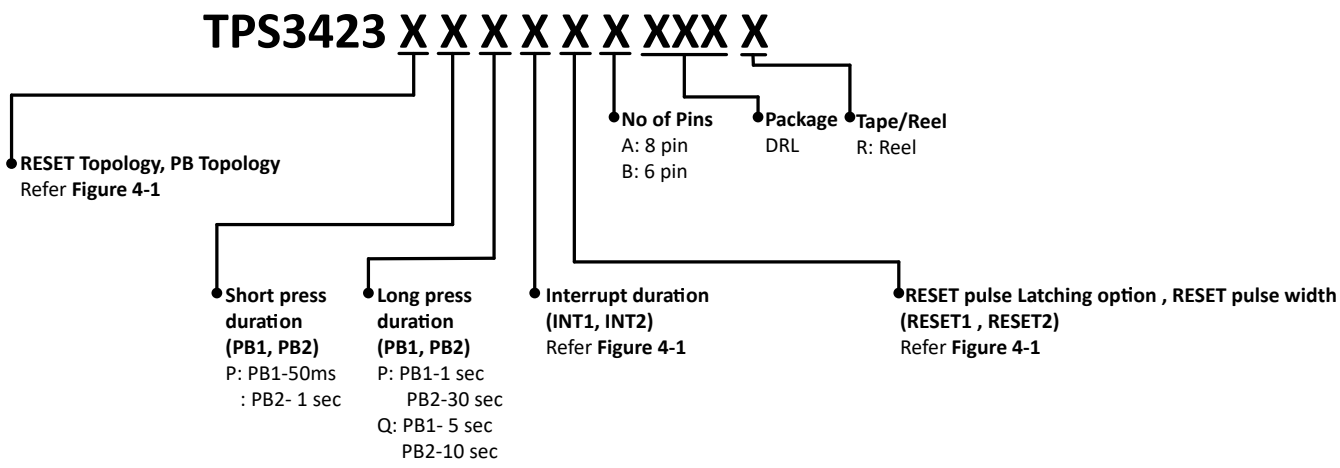

図 4-2. Dual Push-Button Extended Nomenclature

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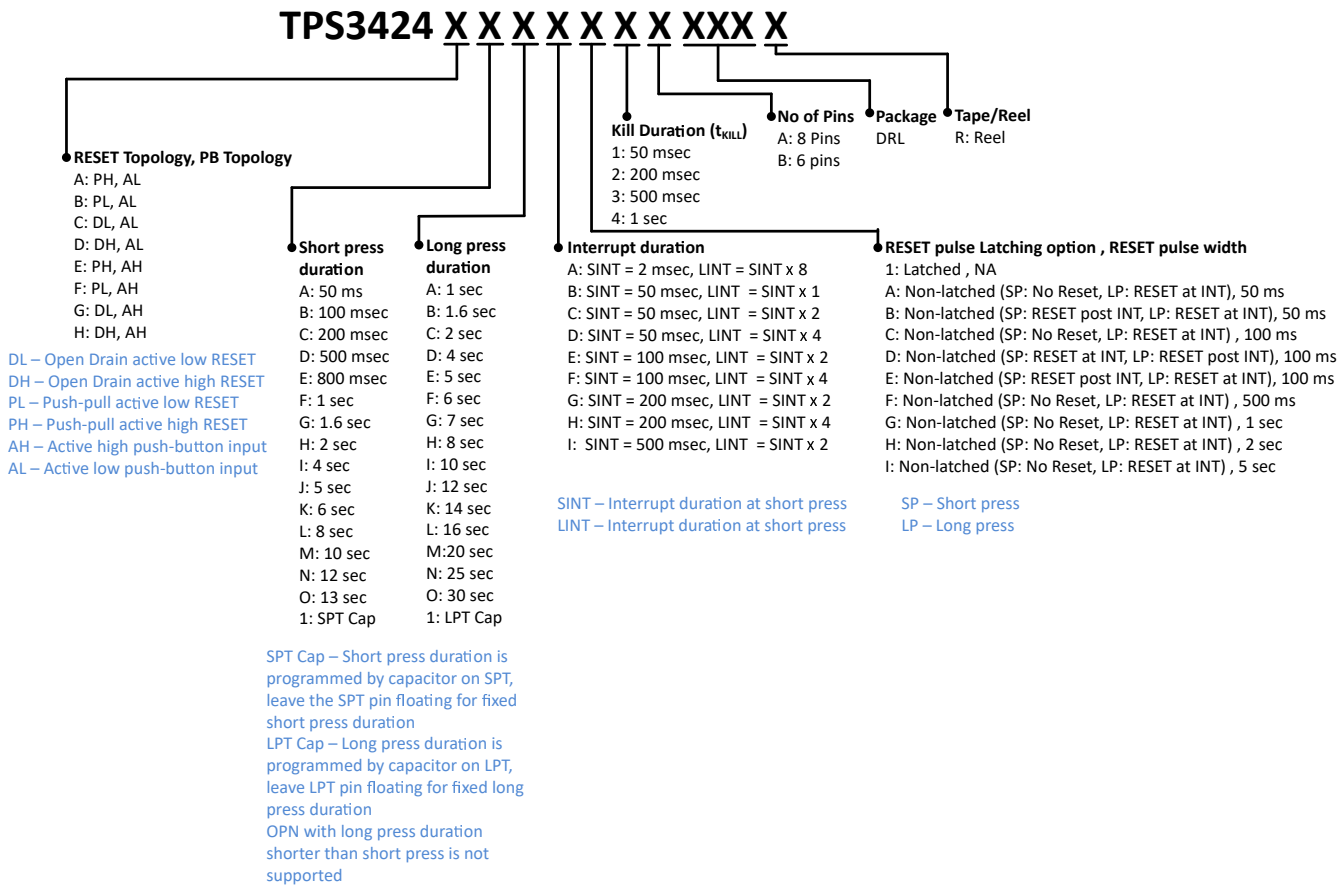

図 4-3. Single Push-Button Nomenclature

TPS3423/4 belongs to family of devices offering different feature sets as highlighted in Device Information.

Device Information

PART NUMBER	NO. OF PUSH-BUTTONS	PUSH-BUTTON TIMING OPTION	KILL FEATURE
TPS3423	2	Fixed	No
TPS3424	1	Fixed , programmable with external capacitor	Yes

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5 Pin Configuration and Functions

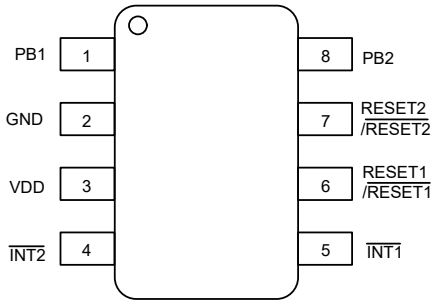

図 5-1. Pin Configuration Option: TPS3423
DRL Package
8-Pin SOT-5X3
Top View

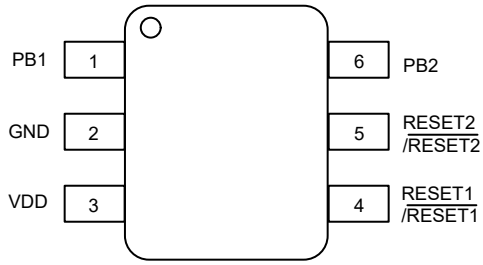

図 5-2. Pin Configuration Option TPS3423
DRL Package
6-Pin SOT-5X3
Top View

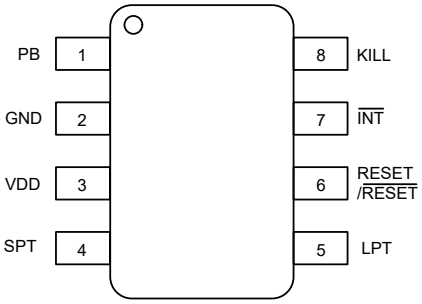

図 5-3. Pin Configuration Option TPS3424
DRL Package
8-Pin SOT-5X3
Top View

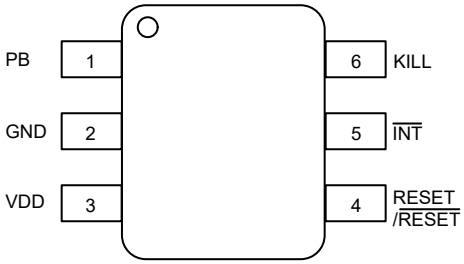

図 5-4. Pin Configuration Option TPS3424
DRL Package
6-Pin SOT-5X3
Top View

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表 5-1. TPS3423 - Pin Functions

TPS3423			I/O	DESCRIPTION
PIN NAME	8 PIN SOT-5X3	6 PIN SOT-5X3		
PB1	1	1	I	Push-button input 1, refer セクション 7.3.1.1 for additional details.
GND	2	2	-	Ground connection for IC.
V_{DD}	3	3	I	Supply connection, connect a 0.1µF capacitor near the pin for best performance.
$\overline{INT2}$	4		O	Interrupt output for push-button input 2, $\overline{INT2}$ is open drain active low output which toggles from every short press and long press on push-button input 2 as described in セクション 7.3.2.1
$\overline{INT1}$	5		O	Interrupt output for push-button input 1, $\overline{INT1}$ is open drain active low output which toggles from every short press and long press on push-button input 1 as described in セクション 7.3.2.1
RESET1/ $\overline{RESET1}$	6	4	O	RESET output for push-button input 1. The response of RESET to short press and long press is described in セクション 7.3.2.2.
RESET2/ $\overline{RESET2}$	7	5	O	RESET output for push-button input 2. The response of RESET to short press and long press is described in セクション 7.3.2.2.
PB2	8	6	I	Push-button input 2, refer セクション 7.3.1.1 for additional details.

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表 5-2. TPS3424 - Pin Functions

TPS3424			I/O	DESCRIPTION
PIN NAME	8 PIN SOT-5X3	6 PIN SOT-5X3		
PB	1	1	I	Push-button input, refer セクション 7.3.1.1 for additional details.
GND	2	2	-	Ground connection for IC.
V_{DD}	3	3	I	Supply connection, connect a 0.1µF capacitor near the pin for best performance.
SPT	4			Connect capacitor to program short press time as described in セクション 7.3.1.1 for SPT Cap version.
LPT	5		O	Connect capacitor to program long press time as described in セクション 7.3.1.1 for LPT Cap version.
RESET/ $\overline{\text{RESET}}$	6	4	O	RESET output for the device. The response of RESET to short press and long press is described in セクション 7.3.2.2.
$\overline{\text{INT}}$	7	5	O	Interrupt output. $\overline{\text{INT}}$ is open drain active low output which toggles from every short press and long press on push-button input as described in セクション 7.3.2.1
KILL	8	6	I	Kill is feedback from the host. RESET can be de-asserted in the latched version by pulling KILL low. Connect this pin to V_{DD} if not used. Please refer セクション 7.3.1.3 for additional details.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	6.5	V
	V_{PB} (1)	–0.3	V_{DD} + 0.3	V
	V_{KILL} (1)	–0.3	V_{DD} + 0.3	V
Current	$I_{RESET/\overline{RESET}}$	-6	6	mA
Temperature(2)	Operating free-air temperature, T_A	-40	125	°C
Storage temperature range	T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (PB pin only)	±8000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101	±750	

(1) HBM for all the pins except PB

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1		6	V
V_{PB}	Push-button pin input voltage	0		V_{DD}	V
V_{KILL}	KILL pin Voltage	0		V_{DD}	V
$V_{\overline{INT}}$	Interrupt pin voltage	0		V_{DD}	V
$V_{RESET/\overline{RESET}}$	Output pin voltage	0		V_{DD}	V
$I_{RESET/\overline{RESET}}$	Output pin current	0		5	mA
T_A	Ambient temperature	-40		125	℃
C_{SPT}	SPT capacitor (1)			125	nF
C_{LPT}	LPT capacitor			125	nF

(1) SPT capacitor value must be lower than LPT capacitor value

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6.4 Thermal Information

THERMAL METRIC(1)		TPS3423 / TPS3424 DRL (SOT-583) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At 1V <V_{DD} <6V, SPT = LPT = Open, KILL = VDD, C_{RESET} = 50pF, $\overline{INT}$ = 10KΩ pull up to V_{DD} and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{DD}	Supply Voltage			1		6	V
$I_{DD(Standby)}$	Standby supply current(1)	V_{DD} = 3V	T_A = 25°C		18	24	nA
			T_A = –40°C to 85°C			90	
		V_{DD} = 6V	T_A = –40°C to 85°C		23	100	
		V_{DD} = 6V				350	
Push-button PIN							
$I_{DD(Active)}$	Supply current when V $\overline{PB}$ = 0V (two push-button is pressed)(2)	V_{DD} = 3V				12	µA
	Supply current when V $\overline{PB}$ = 0V (one push-button is pressed)(2)					7	
	Supply current when V_{PB} = VDD (both-push buttons are pressed)(3)					1.5	
$V_{IH(\overline{PB} / PB)}$	PB Logic high input(2)	V_{DD} = 3V		0.8*V_{DD}			
$V_{IL(\overline{PB} / PB)}$	PB Logic low Input(2)					0.3*VDD	
R_{PB}	PB pin internal pull-up / pull-down resistance(2) (3)				1000		kΩ
$\overline{INT}$ and RESET							
$V_{OL(\overline{INT})}$	Low level output voltage	V_{DD} = 1V, $\overline{INT}$ = 100µA				200	mV
	Low level output voltage	V_{DD} = 3V, $\overline{INT}$ = 1mA				300	
$I_{LKG(\overline{INT})}$	Open drain output leakage current for $\overline{INT}$	V_{DD} = $V_{\overline{Pullup}}$ = 6V				70	nA

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6.5 Electrical Characteristics (続き)

At 1V <V_{DD} <6V, SPT = LPT = Open, KILL = VDD, C_{RESET} = 50pF, $\overline{INT}$ = 10KΩ pull up to V_{DD} and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OL(RESET/\overline{RESET})}$	Low level output voltage (Open Drain)	V_{DD} = 1V, $I_{(RESET/\overline{RESET})}$ = 300µA			200	mV
	Low level output voltage (Push-Pull)(4)	V_{DD} = 1V, $I_{(RESET/\overline{RESET})}$ = 300µA			200	
	Low level output voltage (Open Drain)	V_{DD} = 3V, $I_{(RESET/\overline{RESET})}$ = 5mA			300	
	Low level output voltage (Push-Pull)(4)	V_{DD} = 3V, $I_{(RESET/\overline{RESET})}$ = 5mA			300	
$V_{OH(RESET/\overline{RESET})}$	High level output voltage (Push-Pull)(4)	V_{DD} = 1V, $I_{(RESET/\overline{RESET})}$ = 200µA	0.7*V_{DD}			
	High level output voltage (Push-Pull)(4)	V_{DD} = 3V, $I_{(RESET/\overline{RESET})}$ = 5mA	0.7*$_{VDD}$			
$I_{LKG\ (RESET/\overline{RESET})}$	Open drain output leakage current for (RESET)	V_{DD} = $V_{\overline{Pullup}}$ = 6V, R_{Pullup} = 10kΩ			70	nA
KILL , SPT , LPT						
I_{KILL}	Kill Input current			25		nA
V_{KILL_L}	KILL logic low input				0.3*V_{DD}	
V_{KILL_H}	KILL logic high input		0.7*V_{DD}			

(1) PB pin is floating.
(2) PB pin as active low.
(3) PB pin as active high.
(4) This spec holds true both for active high RESET and active low RESET.

6.6 Timing Requirements

At 1V <V_{DD} <6V, SPT = LPT = Open, KILL = VDD, C_{RESET} = 50pF, $\overline{INT}$ = 10KΩ pull up to V_{DD} and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

Parameter		Test Condition	MIN	TYP	MAX	UNIT
t_{SP} Accuracy	Short press duration accuracy for fixed version(1)		-10		10	%
	Short press duration accuracy for adjutable version(1)	SPT = 330pF, LPT = 4.7nF	-20		20	%
t_{LP} Accuracy	Long press duration accuracy for fixed version		-10		10	%
	Long press duration accuracy for adjutable version	SPT = 330pF, LPT = 4.7nF	-20		-20	%
t_{SINT} Accuracy	Interrupt pulse width accuracy for PB long press		-10		10	%
t_{LINT} Accuracy	Interrupt pulse width accuracy for PB short press		-10		10	%
t_{KILL} Accuracy	PB/KILL debounce accuracy when RESET deaaserts in latched version		-10		10	%
t_{RESET}	Reset pulse duration (non latched) - Accuracy		-10		10	%
$t_{GI(KILL)}$	Glitch Immunity at KILL pin			250		ns
$t_{PD(KILL)}$	KILL falling edge to RESET assert delay			300		ns

(1) t_{SPD} should always be less than t_{LPD}.

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6.7 Timing Diagrams

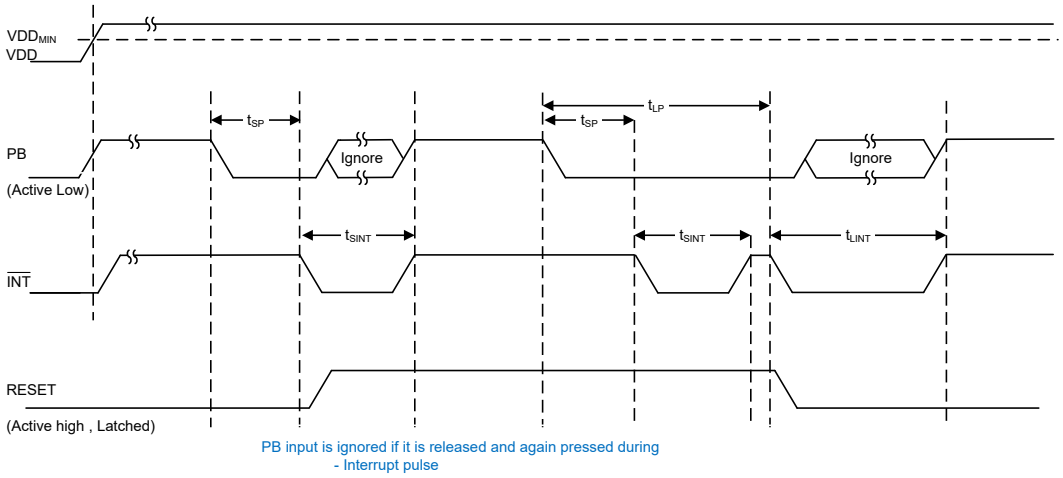

図 6-1. Timing Diagram: Latched RESET

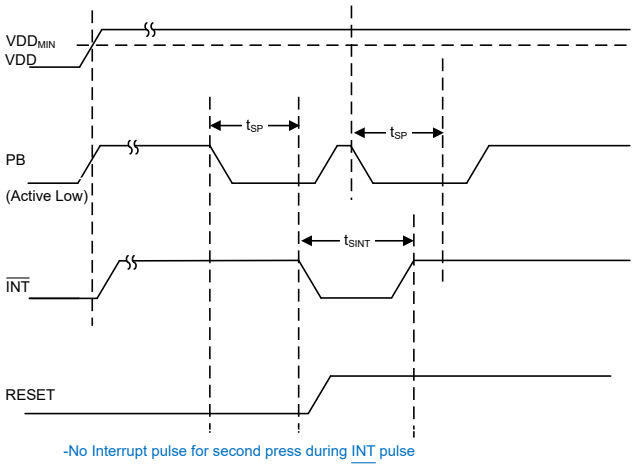

図 6-2. Timing Diagram: Example of PB Input Ignore

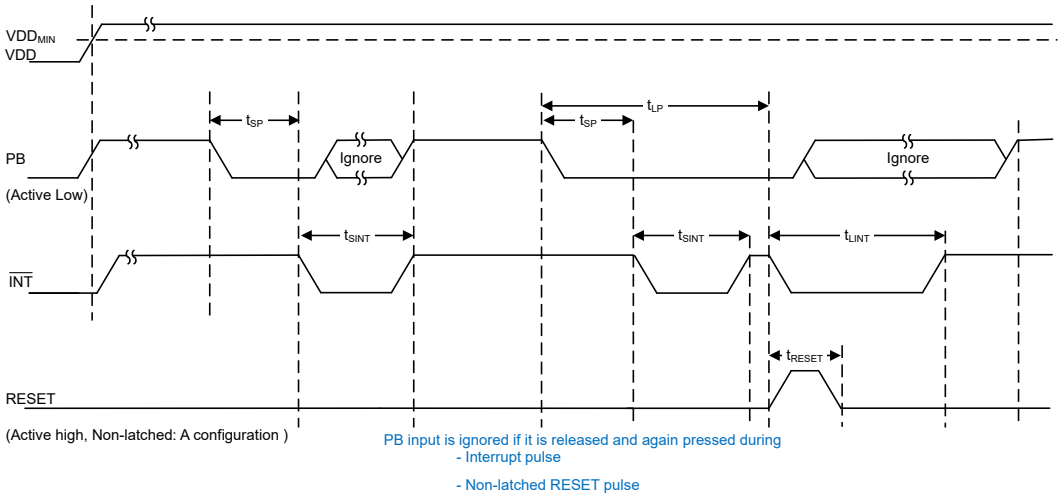

図 6-3. Timing Diagram: Non-Latched RESET

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(SP: No Reset, LP: RESET at INT)

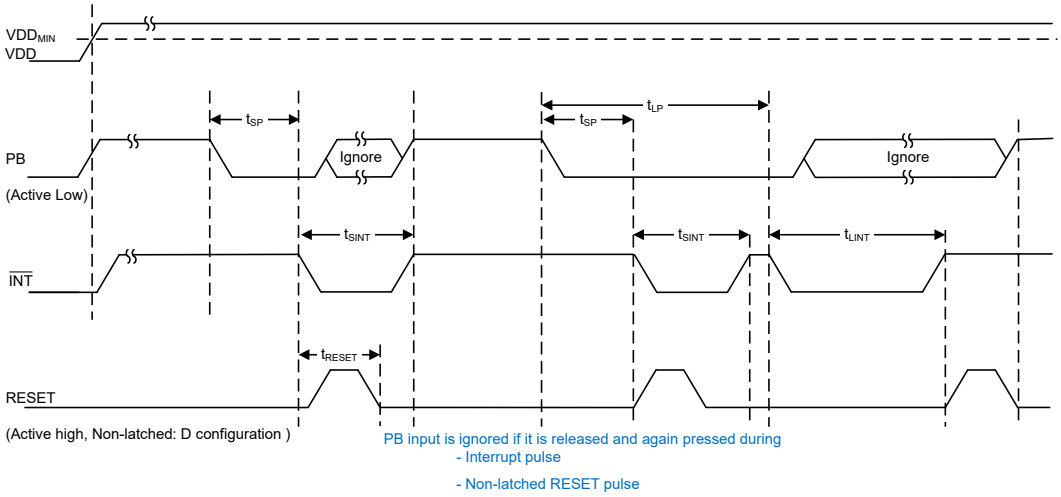

図 6-4. Timing Diagram: Non-Latched RESET

(SP: RESET at INT, LP: RESET post INT)

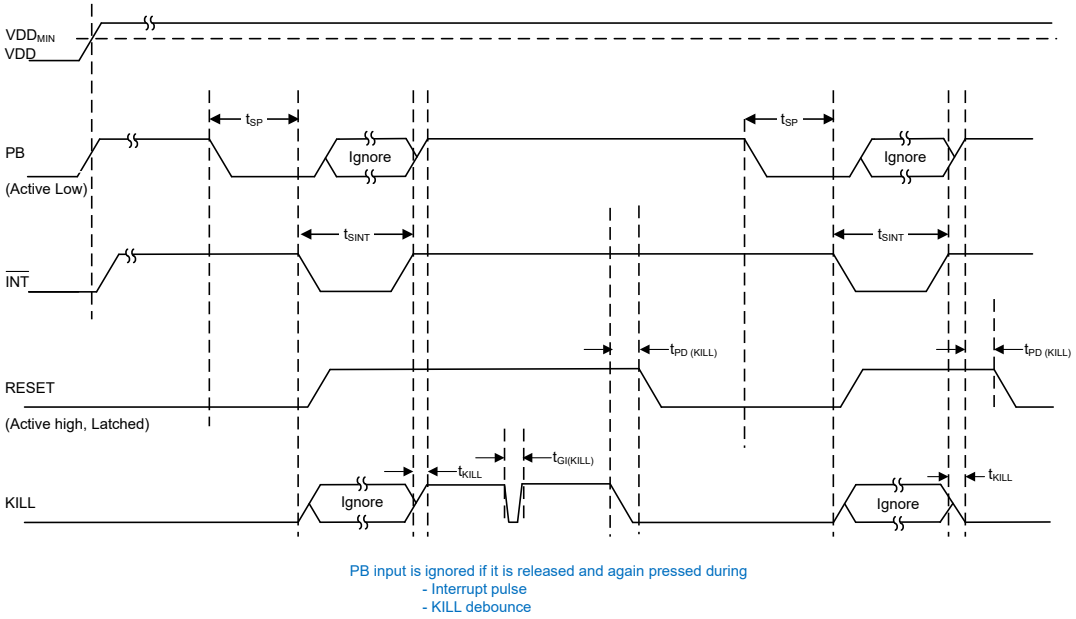

図 6-5. Timing Diagram: KILL

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6.8 Typical Characteristics

At V_{DD} = 6V, SPT = LPT = Open, KILL = VDD, C_{RESET} = 50pF, INT = 10K pull up to V_{DD} and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted.

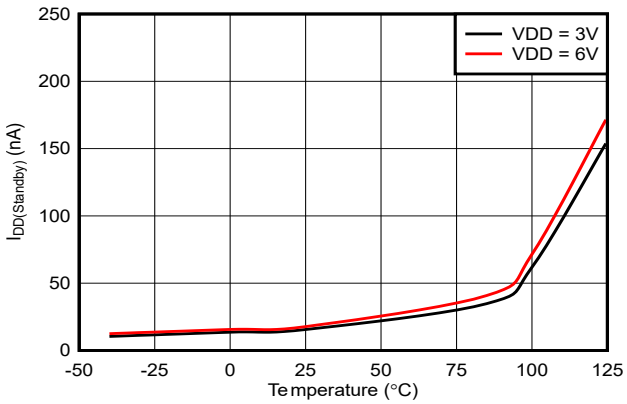

図 6-6. Standby Supply Current vs Temperature

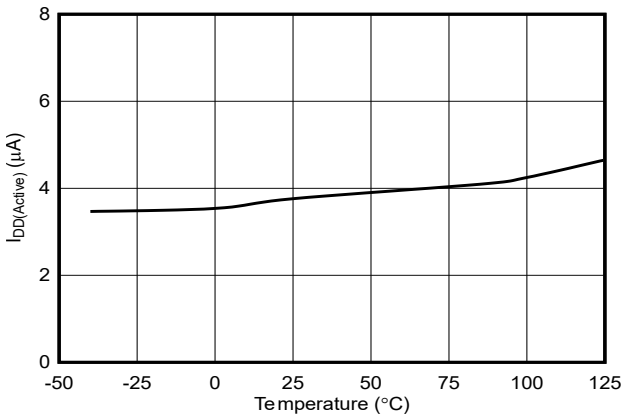

図 6-7. Active Current vs Temperature (Active Low Push Button Input)

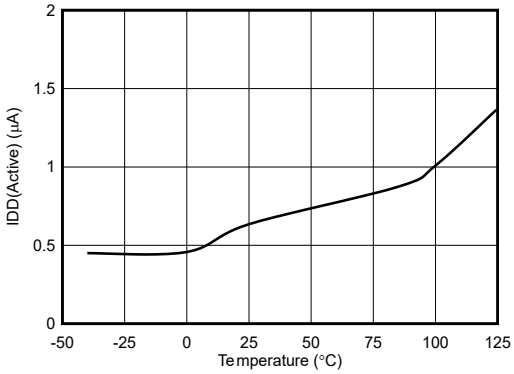

図 6-8. Active Current vs Temperature (Active High Push Button Input)

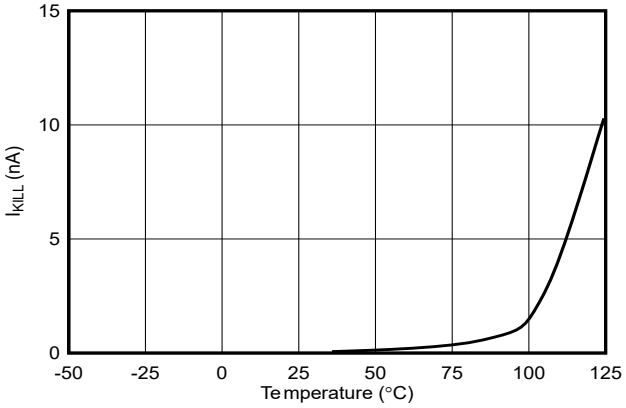

図 6-9. Kill Current vs Temperature

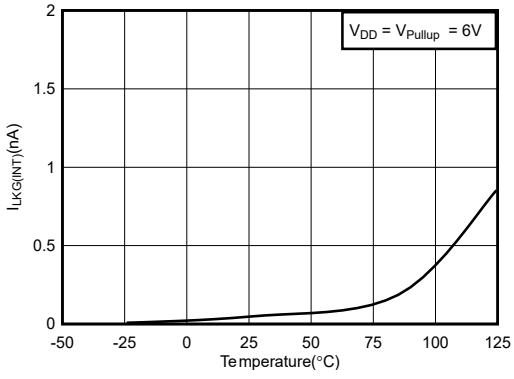

図 6-10. INT Leakage vs Temperature

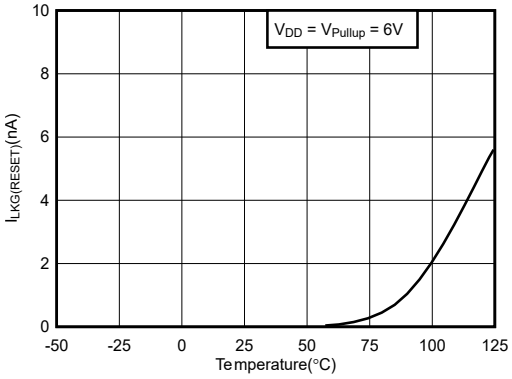

図 6-11. Open Drain RESET Leakage vs Temperature

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6.8 Typical Characteristics (continued)

At V_{DD} = 6V, SPT = LPT = Open, KILL = VDD, C_{RESET} = 50pF, INT = 10K pull up to V_{DD} and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted.

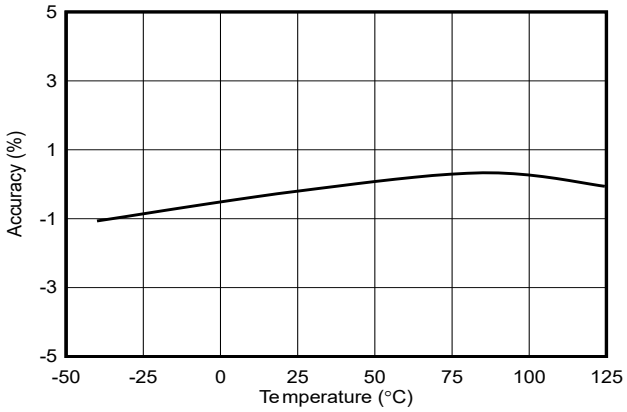

図 6-12. Timing Accuracy vs Temperature (Short Press, Long Press, Kill Blanking time)

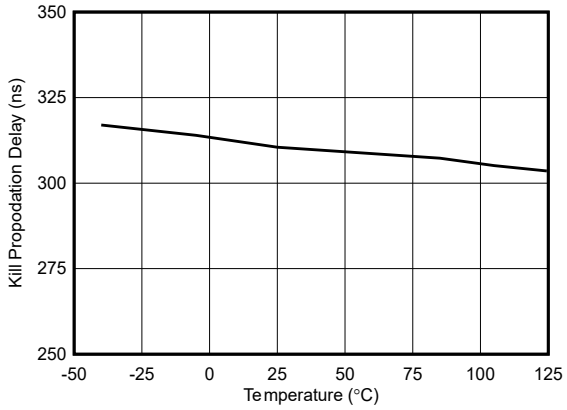

図 6-13. Kill Propagation Delay vs Temperature

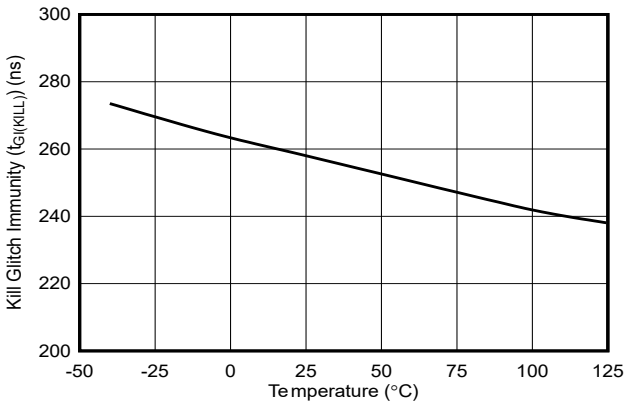

図 6-14. Kill Glitch Immunity vs Temperature

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7 Detailed Description

7.1 Overview

The TPS3423 & TPS3424 are nano power push-button family which offer wide range of timing option for input (PB, KILL) and output (RESET, $\overline{INT}$) pins. This device family is available in two different pinout with 8 and 6 pin DRL package and various output and input configuration as per Device Comparison to support various applications. The pin placement enables use of either 6 pin or 8 pin device for a single 8 pin layout.

7.2 Functional Block Diagrams

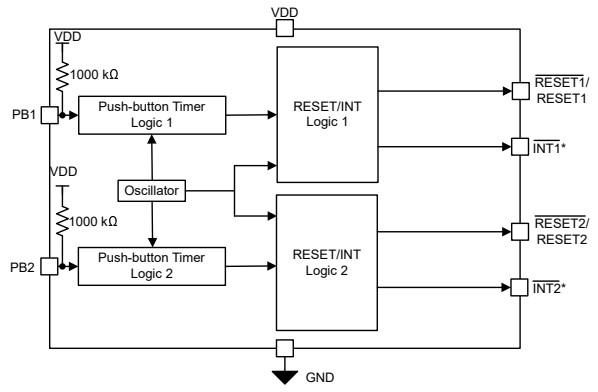

図 7-1. TPS3423 Block Diagram (Active Low Push-Button Input)

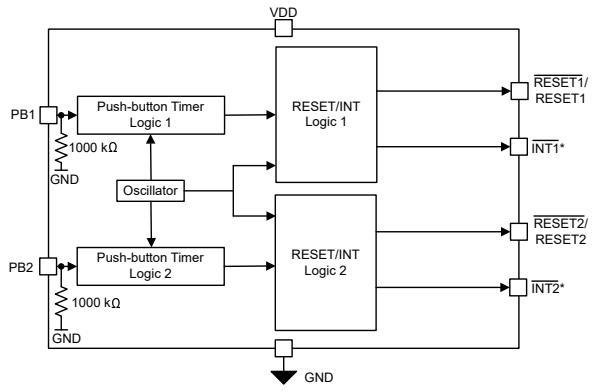

図 7-2. TPS3423 Block Diagram (Active High Push-Button Input)

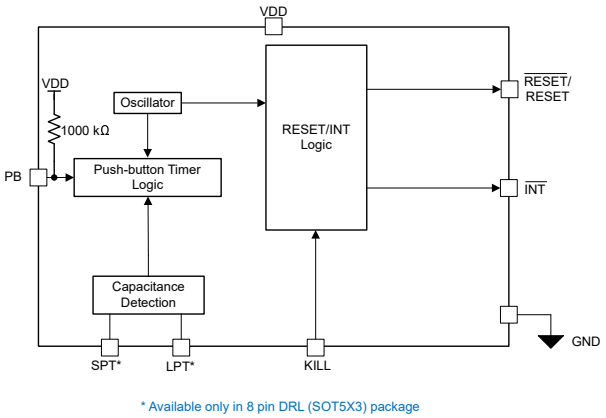

図 7-3. TPS3424 Block Diagram (Active Low Push-Button Input)

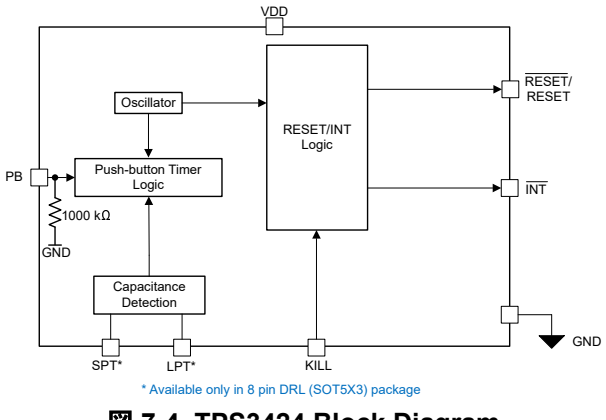

図 7-4. TPS3424 Block Diagram (Active High Push-Button Input)

7.3 Feature Description

7.3.1 Inputs

This section discusses the inputs of the TPS3423 & TPS3424 devices.

7.3.1.1 Push-Button Input (PB)

Push-button input (PB) for TPS3423 and TPS3424 is available in active low and active high configuration as per 表 7-1 as shown from 図 7-1 to 図 7-4.

表 7-1. Push-Button Configuration

PUSH-BUTTON CONFIGURATION	INTERNAL RESISTOR ORIENTATION	PB TRIGGER STATE
Active low	1000kΩ , pulled up to VDD	Falling edge on PB pin if INT is not asserted.
Active High	1000kΩ , pulled down to GND	Rising edge on PB pin if INT is not asserted.

PB pin should be connected to a switch with ON resistance less than 20% of the pull-up / pull-down resistance to provide the correct PB input trigger for the device.

A precise timer gets started once PB pin is triggered by rising or falling edge for active high or active low configuration respectively. The device generates the output corresponding to short press, once PB pin is kept low (for active low PB) or kept high (for active high PB) for more than short press (t_{SP}) duration. The device generates output corresponding to long press if the PB pin is held in the same state for long press (t_{LP}) duration. The timer stops and gets reset when PB pin is released. If PB is released during interrupt pulse (図 7-5), non-latched RESET pulse or KILL debounce time then next PB input is ignored as described in セクション 6.7 and 図 7-6.

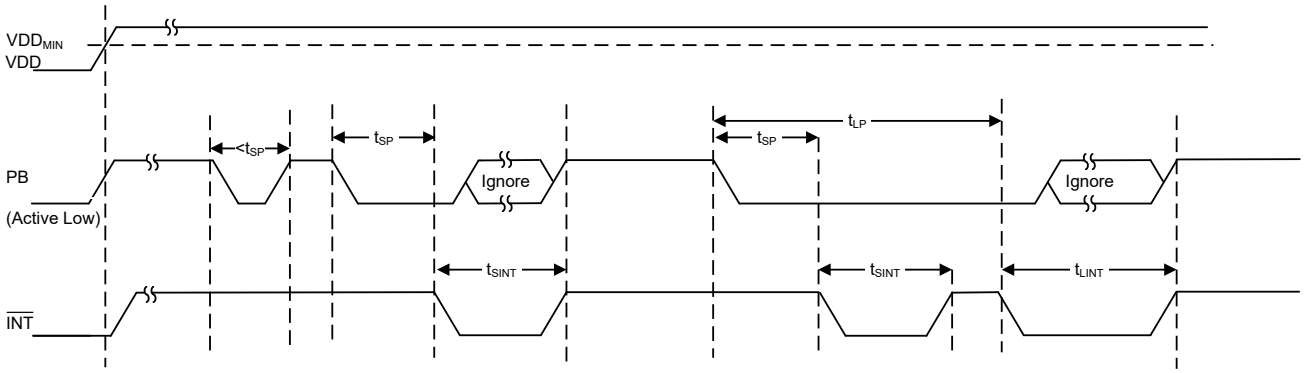

図 7-5. Push Button Functionality

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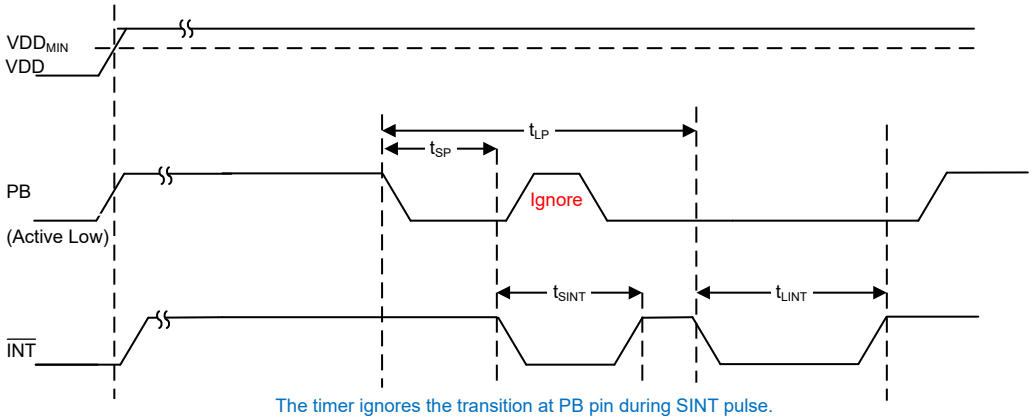

図 7-6. Push Button Transition Behavior at INT Pulse

TPS3423 has two independent push-button pins PB1 and PB2. These pins are factory programmed for short press (t_{SP}) and long press (t_{LP}) duration. TPS3424 has single PB pin. PB pin in TPS3424 is available both in fixed timing and user programmable option (8-pin DRL package) through capacitor connection on SPT and LPT pins. SPT and LPT pins must be floating for fixed timing option of TPS3424.

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7.3.1.2 Push-Button Timing Programmability

TPS3424x11xxx8DRLR has options to program short press duration (t_{SP}) and long press duration (t_{LP}) with capacitor on SPT pin and LPT pin respectively. Equation 1 shows the relation between the press duration and the capacitance. If the pin is left floating, the device defaults to fixed timer of 50msec. Connecting a capacitor which provides less than 50msec press duration as per, programs to 50msec press duration. Make sure t_{LP} is greater than t_{SP} for proper device operation.

$$t_{SP} \text{ or } t_{LP}(\text{sec}) = 0.422 \times C(\text{nF}) \quad (1)$$

where

- Press duration is t_{SP} for SPT capacitor and t_{LP} for LPT capacitor.
- C is the value capacitance connected on SPT or LPT pin.

The device samples the value of capacitor at SPT and LPT at the time of power-up and stores that value. Changing the capacitor after power-up does not change the value of short press (t_{SP}) and long press (t_{LP})

7.3.1.3 KILL

KILL pin is used as a control input from the host for the latched RESET version of push-button device. A short press on PB pin asserts the RESET output of push-button in latched version. The host pulls KILL high once all the expected action from short press is completed like power tree start-up. The device ignores the KILL input for t_{SINT} + t_{KILL} after short press time (t_{SP}), this allows sufficient time for host to monitor the expected tasks for short press.

The host doesn't pull KILL high if short press doesn't perform all expected actions and the push-button device de-asserts RESET output when KILL is low after the debounce time as shown in 図 6-5. Host can pull KILL low at any time to de-assert RESET without any long press on PB pin. KILL input is ignored for non-latched RESET configuration. Connect KILL pin to VDD if KILL feature is not used.

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7.3.2 Outputs

This section discusses the outputs of the TPS3423/4 devices.

7.3.2.1 Interrupt ($\overline{INT}$)

$\overline{INT}$ is open drain active low output. This pin generates low pulse for short press and long press as shown in 図 6-1. Pulse duration for short press t_{INTS} and long press t_{INTL} is factory programmed. Please refer セクション 4 section for the available option for the interrupt duration.

7.3.2.2 RESET / $\overline{RESET}$

RESET output of the device supports multiple configurations as described in 表 7-2. This device is available in all combination as described in セクション 4.

表 7-2. Reset Configurations

PARAMETER	VALUE
Latching option	Latched, Non-latched
Logic	Active High (AH), Active Low (AL)
Output configuration	Open Drain (OD), Push-Pull (PP)

RESET is asserted for short press and de-asserted for long press on PB pin for latched version as shown in 図 6-1. Pulling KILL pin low also de-asserts the RESET in latched version as described in 図 6-5. Non-latched RESET helps in achieving complex logic function with push-button. Non-latched RESET version of device supports multiple pattern as described in セクション 4. RESET pattern is always different for short press and long press. One of the non-latched RESET pattern is shown in 図 6-4.

7.4 Device Functional Modes

Device Functional Modes summarizes the functional modes of the push-button device.

Device Functional Modes

VDD	PB (Active Low)	INT	RESET (Latched, Active high)
VDD< 1V	Not Applicable	Undefined	Undefined
1V ≤ VDD <6V	Low <t_{SP}	No Pulse	No State change
	Low >t_{SP}	Single pulse (SINT)	High
	Low >t_{LP}	Two pulse (SINT, LINT)	Low

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8 Application and Implementation

注

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8.1 Application Information

Push-button controllers play an important role in any human-machine interface (HMI) design. They decode user inputs from single or multiple button presses, control system power or reset, and perform other essential user interface functions. TPS3423 and TPS3424 devices are designed to extend the shelf life of battery powered applications.

8.2 Typical Applications

8.2.1 Power Button Control with TPS3424

TPS3424 is designed for power button applications which need to put the system in deep sleep mode with very small standby power. TPS3424 controls enable for load switch or DC-DC converter in latched mode of RST pin.

An application diagram is shown in 図 8-1 with load switch TPS22919, where TPS3424 is used to control the power from HMI.

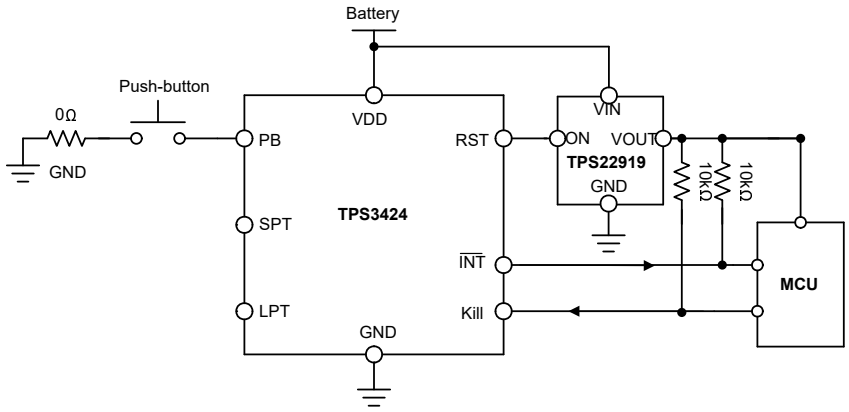

図 8-1. TPS3424 Application Diagram

8.2.1.1 Design Requirements

表 8-1 lists the design requirements for 図 8-1.

表 8-1. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT
HMI Button	PB
Supply = 3V	VDD = 3V
T_{ON} = 50ms	t_{SP}= 50ms
T_{OFF} = 2sec	t_{LP}= 2sec
MCU IO pin current rating < 500uA	$\overline{INT}$ & KILL pull up = 10kΩ

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8.2.1.2 Detailed Design Procedure

8.2.1.2.1 PB and RESET Topology

Selection of push-button input topology depends on the HMI. The button press in this application shorts PB pin to GND with a low resistor, hence active low PB topology is chosen here. Selection of RESET pin topology depends on the ON pin behaviour of the load switch or the voltage regulator in power control applications. Active high latched REST is chosen topology is chosen here to turn-on the load switch at short press and turn-off at long press.

8.2.1.2.2 Short Press Time (t_{SP}) and Long Press Time (t_{LP}) selection

t_{SP}= 50ms and t_{LP}= 2sec can be selected through the factory programmed option or placing capacitor at the SPT and LPT pin for programable option. Leave the SPT and LPT pin open as shown in 図 8-1 for factory programmed timing option. Equation 1 and Equation 2 shows the value for capacitor at SPT and LPT pin respectively for programming t_{SP}= 50ms and t_{LP}= 2sec in cap programable option.

$$C_{SPT}(\text{nF}) = \text{Open} \tag{2}$$

$$C_{LPT}(\text{nF}) = \frac{2\ \text{sec}}{0.422} = 4.7 \tag{3}$$

8.2.1.2.3 Interrupt and Kill Feature

TPS3424 generated a pulse on $\overline{\text{INT}}$ pin for every valid short press and long press. This feature can be used as feature traverser (eg. showing different value on screen).

KILL feature enables host to control the RESET output of TPS3424 as described in セクション 7.3.1.3. KILL pin enables the host to put the system in deep sleep when unused for given time. Short KILL to V_{DD} pin if KILL feature is not used.

8.2.1.3 Application Curve

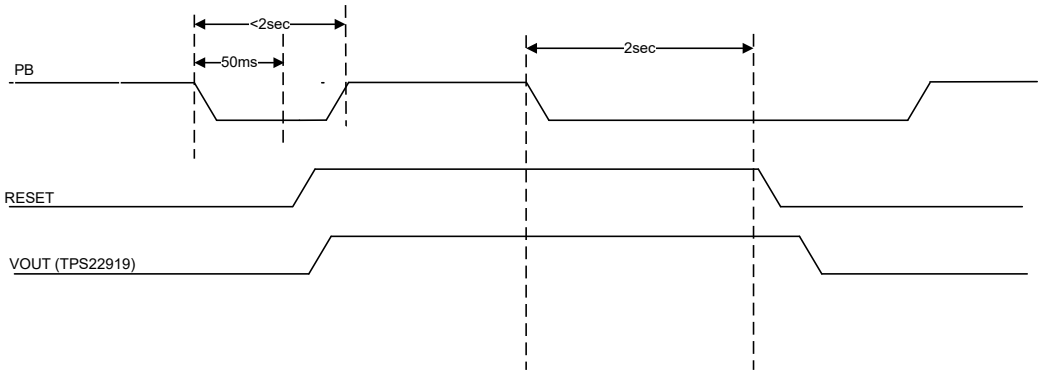

図 8-2. Power Control Through Load Switch

8.2.2 High Voltage Connection

Low current shunt regulator ATL431 enables the push-button to be used with 12V/24V battery powered application as shown in 図 8-3.

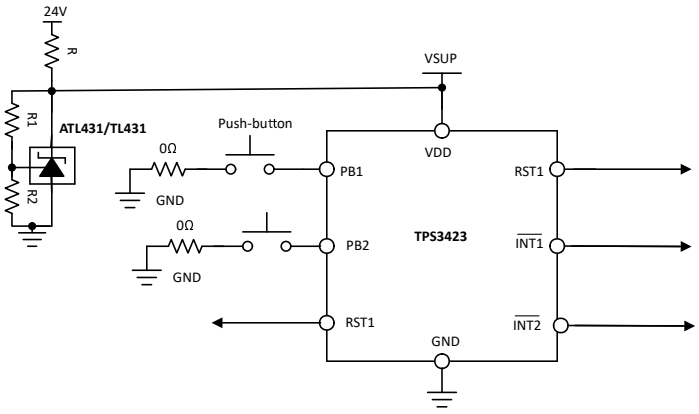

図 8-3. High voltage support with ATL431

8.3 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1V and 6V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1µF capacitor between the VDD pin and the GND pin.

8.4 Layout

8.4.1 Layout Guidelines

Follow these guidelines for laying out the printed circuit board (PCB) that is used for the TPS3423 and TPS3424.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1µF ceramic capacitor as near as possible to the VDD pin.
- Place the external capacitor on close to LPT and SPT pin for TPS3424.
- Parasitic on LPT and SPT must be less than 50pF when these pins are floating for TPS3424.

8.4.2 Layout Example

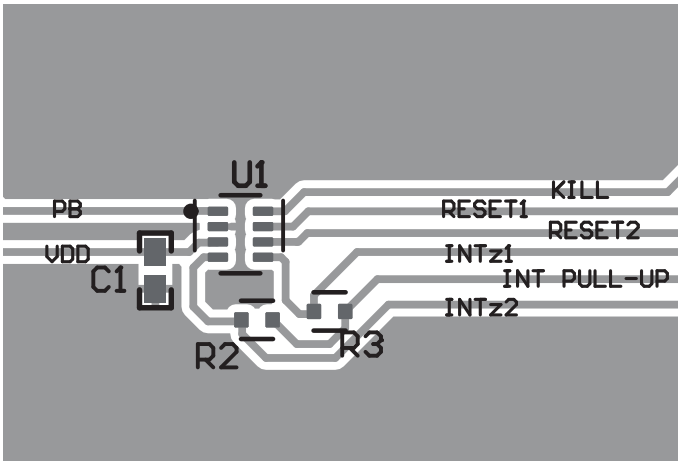

図 8-4. TPS3423: Layout Example (8-Pin DRL Package)

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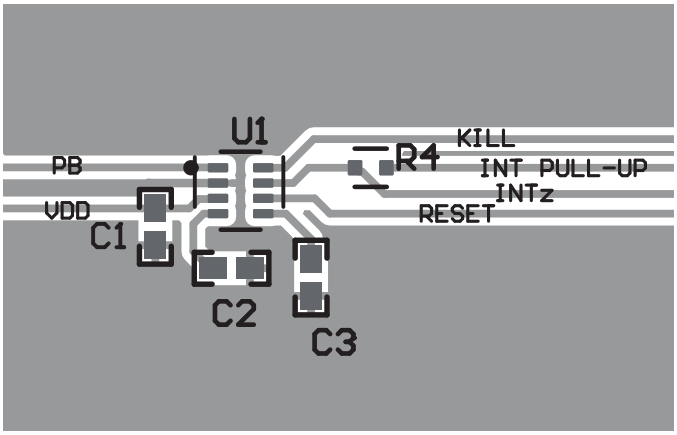

図 8-5. TPS3423: Layout Example (8-Pin DRL Package)

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2024) to Revision A (December 2024)	Page
• 量産データのリリース	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PPS3423DAHGFADRLR	ACTIVE	SOT-5X3	DRL	8	4000	TBD	Call TI	Call TI	-40 to 125		Samples
PPS3424A11C13ADRLR	ACTIVE	SOT-5X3	DRL	8	4000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS3423GAMDHADRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	D0001	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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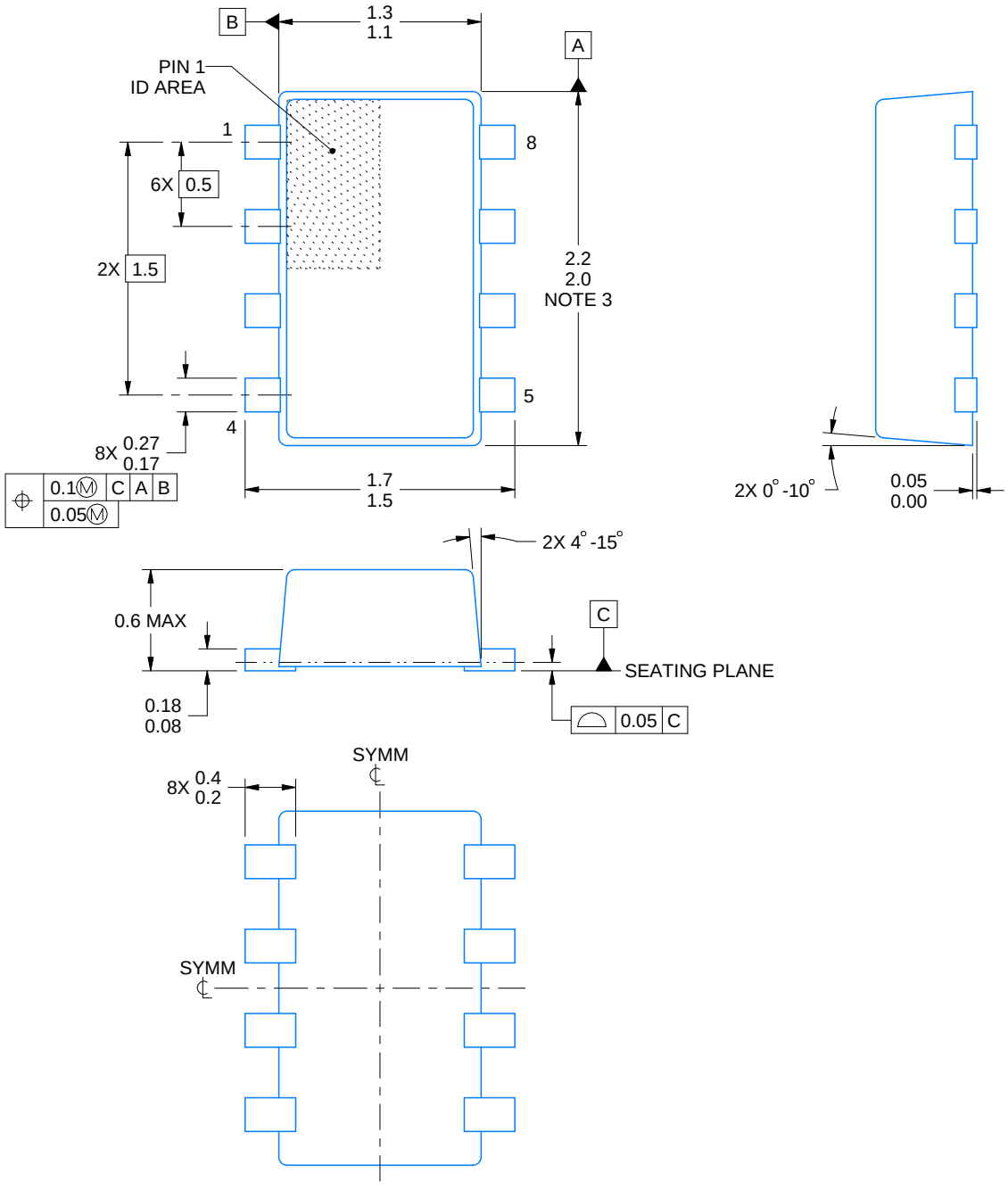
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

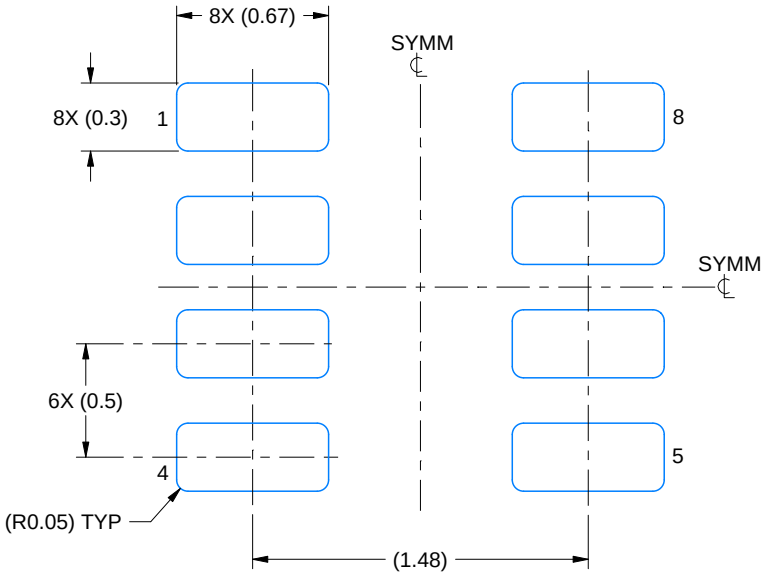
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

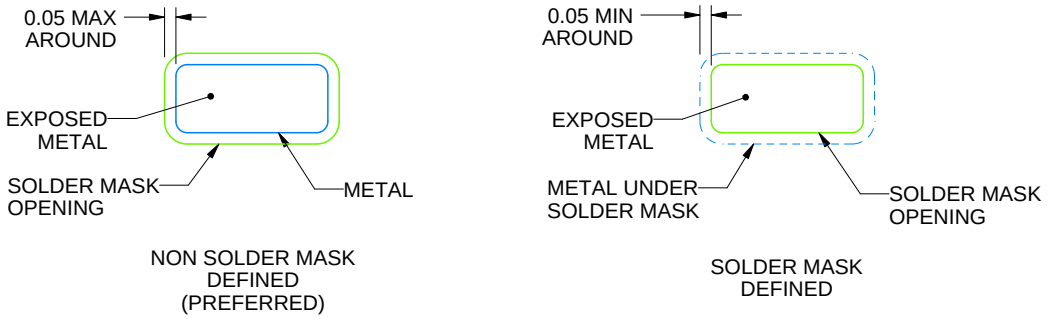
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

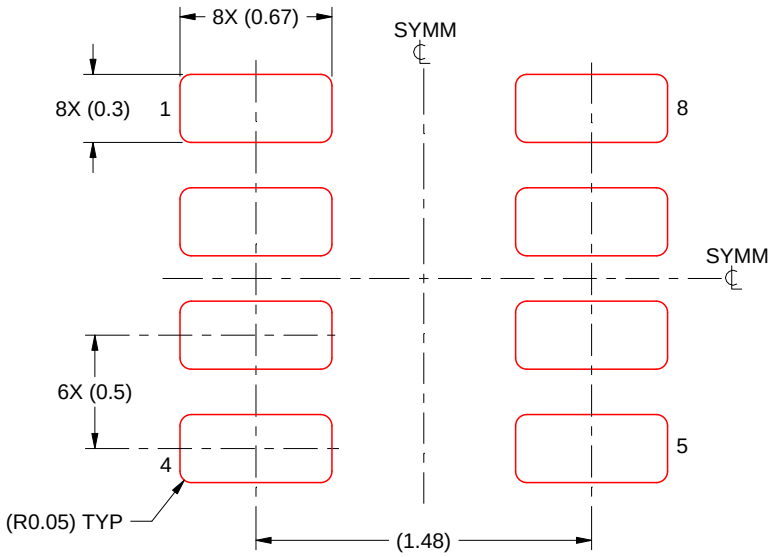
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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