参考資料

TPS3762-Q1 車載用 65V ウィンドウ (OV & UV) スーパーバイザ、セルフテストおよびラッチ機能内蔵

1 特長

- ASIL-D 機能安全準拠
  - ISO 26262 システムの設計に役立つ資料
  - ASIL-D までの決定論的対応能力
  - ASIL-D までのハードウェア機能
- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度グレード 1:-40℃～+125℃
- 設計要件を満たすデバイスの柔軟性
  - 幅広い電圧スレッショルド範囲:2.7V～60V
  - 800mV オプション - スレッショルドを設定するには、外付け分割抵抗と併用
  - ヒステリシス内蔵 (2%、5%、10% のオプション)
  - 固定またはプログラム可能なリセット時間遅延
  - 固定およびプログラム可能な検出遅延
- 高電圧電源レールを監視
  - 幅広い入力電圧範囲:2.7V～65V
  - センス ピン -65V の逆極性保護
- 12/24/48V システムでの高速 UV/OV 保護
  - 出力リセット・ラッチ機能
  - 超高速検出時間遅延オプション (5μs)
  - 内蔵セルフ・テスト

2 アプリケーション

- センサ フュージョンおよびカメラ
- デジタル コックピット処理装置
- オンボード チャージャ
- ADAS ドメイン コントローラ

3 概要

TPS3762-Q1 は、4μA I_{DD}、0.9% 精度、高速検出時間 (5μs)、内蔵セルフテスト機能を備えた 65V 入力電圧スーパーバイザです。このデバイスは 12V/24V 車載用バッテリ システムに直接接続し、過電圧 (OV) および低電圧 (UV) 状態を継続的に監視できます。また、分割抵抗を内蔵しているため、TPS3762-Q1 はソリューション全体のサイズを最小化できます。多くのヒステリシス電圧オプションを利用することで、大きな電圧過渡を無視することができ、さらに誤リセット信号を防止できます。

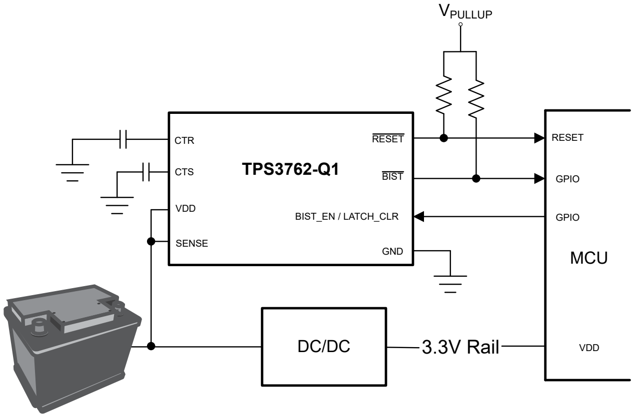
VDD ピンと SENSE ピンが独立しているため、信頼性が高いシステムが求める冗長性を実現できます。また、SENSE は VDD よりも高い電圧と低い電圧を監視できます。SENSE ピンは高インピーダンス入力なので外付け抵抗を使うこともできます。CTS ピンおよび CTR ピンを使うことで、RESET 信号の立ち下がり / 立ち上がりエッジの遅延を調整できます。CTS は、監視対象の電圧レールの電圧グリッチを無視することで、デバウンシング機能として機能します。

TPS3762-Q1 は、2.9mm × 1.6mm の SOT23 8 ピン パッケージで供給されます。

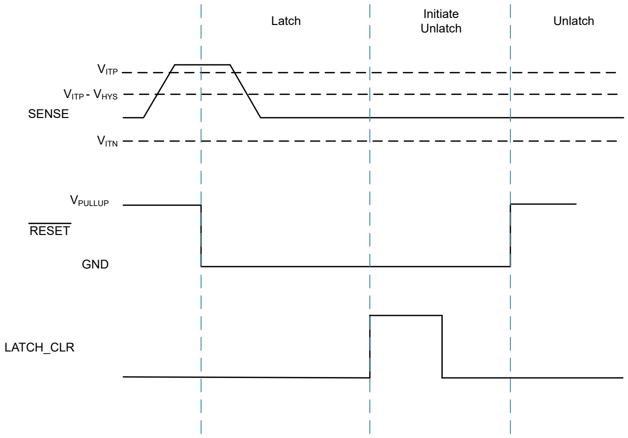
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
TPS3762-Q1	SOT-23 (8) (DDF)	2.9mm x 1.6mm

(1) パッケージの詳細については、このデータシートの末尾の外形図を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路



ラッチ機能の波形

Table of Contents

4 Device Nomenclature

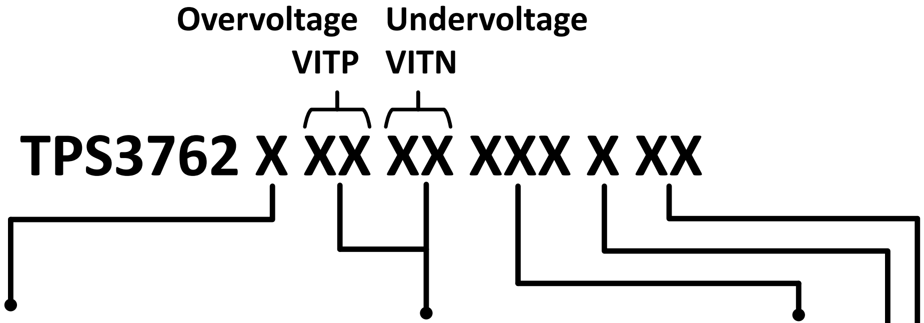
Device Decoder in セクション 5 describe how to decode certain device function of the device based on its part number. Not all part numbers follow this nomenclature. Use 表 4-1 as the part number decoding table for all devices.

表 4-1. Device Configuration Table

ORDERABLE PART NAME	Overvoltage (V_{ITP})	Overvoltage Hysteresis	Undervoltage (V_{ITN})	Undervoltage Hysteresis	CTR / CTS	Latch / UVbypass	BIST RESET Trigger
TPS3762D02OVDDFRQ1	800mV	2%	N/A	N/A	ADJ / ADJ	Both	Yes

5 Device Comparison

Device Decoder shows some of the device naming nomenclature of the TPS3762-Q1. Not all device namings follow this nomenclature table. For a detailed breakdown of every device part number by threshold voltage options, BIST configurations, Latch configurations, CTR options, CTS options, and UV bypass, see セクション 4 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.



Topology

Suffix	CTR	CTS	Latch / UV Bypass	BIST RESET Trigger
A	ADJ	ADJ	Disabled	Yes
B	ADJ	ADJ	Latch	Yes
C	ADJ	ADJ	UVBypass	Yes
D	ADJ	ADJ	Both	Yes
E	ADJ	5 µs	Disabled	Yes
F	ADJ	5 µs	Latch	Yes
G	ADJ	5 µs	UVBypass	Yes
H	ADJ	5 µs	Both	Yes
I	ADJ	ADJ	Disabled	No
J	ADJ	ADJ	Latch	No
K	ADJ	ADJ	UVBypass	No
L	ADJ	ADJ	Both	No
M	ADJ	5 µs	Disabled	No
N	ADJ	5 µs	Latch	No
O	ADJ	5 µs	UVBypass	No
P	ADJ	5 µs	Both	No
Q	200ms	5 µs	Disabled	Yes
R	200ms	5 µs	Latch	Yes

Threshold Voltage

2% Hysteresis Option

Suffix	VIT	Suffix	VIT
02	800mV	**D7**	8.5V
A7	2.7V	**D8**	9V
A8	2.8V	**D9**	9.5V
A9	2.9V	**E0**	10V
B0	3V	**E1**	11V
B1	3.1V	**E2**	12V
B2	3.2V	**E3**	13V
B3	3.3V	**E4**	14V
B4	3.4V	**E5**	15V
B5	3.5V	**E6**	16V
B6	3.6V	**E7**	17V
B7	3.7V	**E8**	18V
B8	3.8V	**E9**	20V
B9	3.9V	**F0**	22V
C0	4V	**F1**	24V
C1	4.1V	**F2**	26V
C2	4.2V	**F3**	28V
C3	4.3V	**F4**	30V
C4	4.4V	**F5**	32V
C5	4.5V	**F6**	34V
C6	4.6V	**F7**	36V
C7	4.7V	**F8**	38V
C8	4.8V	**F9**	40V
C9	4.9V	**G0**	42V
D0	5V	**G1**	46V
D1	5.5V	**G2**	48V
D2	6V	**G3**	50V
D3	6.5V	**G4**	54V
D4	7V	**G5**	57V
D5	7.5V	**G6**	58V
D6	8V	**G7**	60V
W7	+/-7%		
UV	UV Only	**OV**	OV Only

5% Hysteresis Option

Suffix	VIT	Suffix	VIT
05	800mV	**K7**	8.5V
H7	2.7V	**K8**	9V
H8	2.8V	**K9**	9.5V
H9	2.9V	**L0**	10V
I0	3V	**L1**	11V
I1	3.1V	**L2**	12V
I2	3.2V	**L3**	13V
I3	3.3V	**L4**	14V
I4	3.4V	**L5**	15V
I5	3.5V	**L6**	16V
I6	3.6V	**L7**	17V
I7	3.7V	**L8**	18V
I8	3.8V	**L9**	20V
I9	3.9V	**M0**	22V
J0	4V	**M1**	24V
J1	4.1V	**M2**	26V
J2	4.2V	**M3**	28V
J3	4.3V	**M4**	30V
J4	4.4V	**M5**	32V
J5	4.5V	**M6**	34V
J6	4.6V	**M7**	36V
J7	4.7V	**M8**	38V
J8	4.8V	**M9**	40V
J9	4.9V	**N0**	42V
K0	5V	**N1**	46V
K1	5.5V	**N2**	48V
K2	6V	**N3**	50V
K3	6.5V	**N4**	54V
K4	7V	**N5**	57V
K5	7.5V	**N6**	58V
K6	8V	**N7**	60V

10% Hysteresis Option

Suffix	VIT	Suffix	VIT
10	800mV	**Q1**	4.1V
O7	2.7V	**Q2**	4.2V
O8	2.8V	**Q3**	4.3V
O9	2.9V	**Q4**	4.4V
P0	3V	**Q5**	4.5V
P1	3.1V	**Q6**	4.6V
P2	3.2V	**Q7**	4.7V
P3	3.3V	**Q8**	4.8V
P4	3.4V	**Q9**	4.9V
P5	3.5V	**R0**	5V
P6	3.6V	**R1**	5.5V
P7	3.7V	**R2**	6V
P8	3.8V	**R3**	6.5V
P9	3.9V	**R4**	7V
Q0	4V	**R5**	7.5V

10% Hysteresis Option

Suffix	VIT	Suffix	VIT
R6	8V	**T2**	26V
R7	8.5V	**T3**	28V
R8	9V	**T4**	30V
R9	9.5V	**T5**	32V
S0	10V	**T6**	34V
S1	11V	**T7**	36V
S2	12V	**T8**	38V
S3	13V	**T9**	40V
S4	14V	**U0**	42V
S5	15V	**U1**	46V
S6	16V	**U2**	48V
S7	17V	**U3**	50V
S8	18V	**U4**	54V
S9	20V	**U5**	57V
T0	22V	**U6**	58V
T1	24V	**U7**	60V

Package

Suffix	Name
DDF	SOT-23

Reel

Suffix	Name
R	Large

Rating

Suffix	Name
Q1	AUTO

1. Suffix 02, 05, and 10 with VIT of 800mV corresponds to the adjustable variant, do not have internal voltage divider
2. Not all TPS3762-Q1 devices can be decoded by this table. Refer to セクション 4 for a decoding table by part number.

6 Pin Configuration and Functions

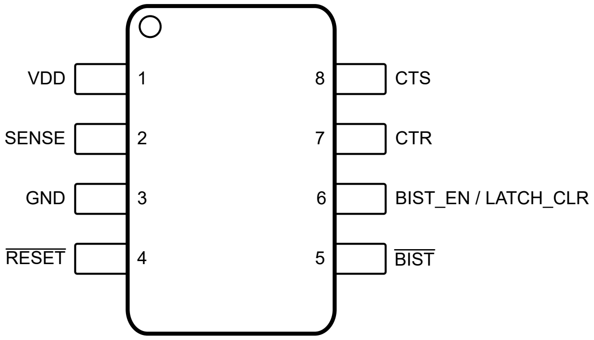


図 6-1. DDF Package,
8-Pin SOT-23,
TPS3762-Q1 (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	**Input Supply Voltage:** Supply voltage pin. For noisy systems, bypass with a 0.1µF capacitor to GND.
SENSE	2	I	**Sense Voltage:** Connect this pin to the supply rail that must be monitored. See Section 8.3.2 for more details. Sensing Topology: **Overvoltage (OV) or Undervoltage (UV) or Window (OV + UV)**
GND	3	-	**Ground.** Ground pin. All GND pins must be electrically connected to the board ground.
$\overline{\text{RESET}}$	4	O	**Output Reset Signal:** $\overline{\text{RESET}}$ asserts when SENSE crosses the voltage threshold after the sense time delay, set by CTS, and remains asserted for the reset time delay period, set by CTR, after SENSE transitions out of a fault condition. For latch variants $\overline{\text{RESET}}$ remains asserted until the latch is cleared. The active low open-drain reset output requires an external pullup resistor. See Section 8.3.3.2 for more details. Output topology: **Open-Drain Active-Low**
$\overline{\text{BIST}}$	5	O	**Built-In Self-Test:** $\overline{\text{BIST}}$ asserts when a logic high input occurs on the BIST_EN / LATCH_CLR or BIST_EN pin, this initiates the internal BIST testing. $\overline{\text{BIST}}$ recovers after $t_{\overline{\text{BIST}}}$ to signify BIST completed successfully. $\overline{\text{BIST}}$ remains asserted for a time period longer than $t_{\overline{\text{BIST}}}$ if there is a failure during BIST. $\overline{\text{BIST}}$ active-low open-drain output requires an external pullup resistor. See Section 8.3.6 for more details.
BIST_EN / LATCH_CLR	6	I	**Built-in Self-test Enable and Latch Clear:** A logic high input must occur on the BIST_EN / LATCH_CLR to initate BIST and clear a latched $\overline{\text{OV}}$/$\overline{\text{UV}}$ fault. See Section 8.3.6 for more details.
CTR	7	O	**RESET Time Delay:** User-programmable reset time delay for $\overline{\text{RESET}}$. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section8.3.4 for more details.
CTS	8	O	**SENSE Time Delay:** User-programmable sense time delay for SENSE. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 8.3.5 for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted (1)

		MIN	MAX	UNIT
Voltage	V_{DD}, $V_{SENSE(Adjustable)}$, $V_{\overline{RESET}}$	–0.3	70	V
Voltage	$V_{SENSE(Fixed)}$	–65	70	V
Voltage	V_{CTS}, V_{CTR}	–0.3	6	V
Voltage	V_{BIST}, V_{BIST_EN}, $V_{BIST\_EN/LATCH\_CLR}$	–0.3	6	V
Current	I_{RESET}, I_{BIST}		10	mA
Temperature (2)	Operating junction temperature, T_J	–40	150	°C
Temperature (2)	Operating Ambient temperature, T_A	–40	150	°C
Temperature (2)	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	2.7		65	V
Voltage	V_{SENSE}, $V_{\overline{RESET}}$	0		65	V
Voltage	V_{CTS}, V_{CTR}	0		5.5	V
Voltage	$V_{\overline{BIST}}$, V_{BIST_EN}, $V_{BIST\_EN/LATCH\_CLR}$	0		5.5	V
Current	$I_{\overline{RESET}}$, $I_{\overline{BIST}}$	0		5	mA
T_J (1)	Junction temperature (free air temperature)	–40		125	°C

(1) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.4 Thermal Information

THERMAL METRIC [1]		TPS3762-Q1	UNIT
		DDF	
		8-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	72.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open, output $\overline{\text{RESET}}$ pull-up resistor R_{PU} = 10kΩ, voltage V_{PU} = 5.5V, output $\overline{\text{BIST}}$ pull-up resistor $R_{PU\_\overline{BIST}}$ = 10kΩ, voltage $V_{PU\_\overline{BIST}}$= 5.5V, and load C_{LOAD} = 10pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12V and V_{IT} = 6.5V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{DD}	Supply Voltage		2.7		65	V
UVLO (1)	Undervoltage Lockout	V_{DD} rising above $V_{DD\ (MIN)}$			2.6	V
UVLO(HYS) (1)	Undervoltage Lockout Hysteresis	V_{DD} falling below $V_{DD\ (MIN)}$		500		mV
$V_{POR(\overline{RESET})}$	Power on Reset Voltage (2) $\overline{\text{RESET}}$, Active Low (Open-Drain)	$V_{OL(MAX)}$ = 300mV $I_{OUT\ (Sink)}$ = 15µA			1.4	V
$V_{POR(\overline{BIST})}$	Power on Reset Voltage (2) $\overline{\text{BIST}}$, Active Low (Open-Drain)	$V_{OL(MAX)}$ = 300mV $I_{OUT\ (Sink)}$ = 15µA			1.4	V
I_{DD}	Supply current into V_{DD} pin	V_{IT} = 800mV $V_{DD\ (MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$		4	8.1	µA
SENSE (Input)						
I_{SENSE}	Input current	V_{IT} = 800mV			200	nA
V_{ITN}	Input Threshold Negative (Undervoltage)	V_{IT} = 800mV (3)	-0.9		0.9	%
V_{ITP}	Input Threshold Positive (Overvoltage)	V_{IT} = 800mV (3)	-0.9		0.9	%
V_{HYS}	Hysteresis Accuracy (4)	V_{IT} = 0.8V V_{HYS} Range = 2%	1.5	2	2.5	%
$\overline{\text{RESET}}$ (Output)						
$I_{lkg(OD)}$	Open-Drain leakage	$V_{\overline{RESET}}$ = 5.5V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$I_{lkg(OD)}$	Open-Drain leakage	$V_{\overline{RESET}}$ = 65V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
V_{OL} (5)	Low level output voltage	2.7V ≤ VDD ≤ 65V $I_{\overline{RESET}}$ = 2.7mA			350	mV

7.5 Electrical Characteristics (続き)

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, output $\overline{\text{RESET}}$ pull-up resistor R_{PU} = 10kΩ, voltage V_{PU} = 5.5V, output $\overline{\text{BIST}}$ pull-up resistor $R_{PU\_\overline{BIST}}$ = 10kΩ, voltage $V_{PU\_\overline{BIST}}$= 5.5V, and load C_{LOAD} = 10pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12V and V_{IT} = 6.5V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR)		2.96	3.7	4.44	MΩ
R_{CTS}	Internal resistance (CTS)		2.96	3.7	4.44	MΩ
Built-in Self-test						
$I_{lkg(\overline{BIST})}$	Open-Drain leakage	$V_{\overline{BIST}}$ = 5.5V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$I_{lkg(\overline{BIST})}$	Open-Drain leakage	$V_{\overline{BIST}}$ = 3.3V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$V_{\overline{BIST}\_OL}$	Low level output voltage	2.7V ≤ VDD ≤ 65V $I_{\overline{BIST}}$ = 5mA			300	mV
V_{BIST_EN}	BIST_EN pin logic low input				500	mV
V_{BIST_EN}	BIST_EN pin logic high input		1300			mV
$V_{BIST\_EN/LATCH\_CLR}$	LATCH_CLR pin logic low input				500	mV
$V_{BIST\_EN/LATCH\_CLR}$	LATCH_CLR pin logic high input		1300			mV

(1) When V_{DD} voltage falls below UVLO, $\overline{\text{RESET}}$ is asserted. V_{DD} slew rate ≤ 100mV / µs

(2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below V_{POR}, the output cannot be determined. V_{DD} slew rate ≤ 100mV/µs

(3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**

(4) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.

(5) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**

7.6 Switching Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open and enabled, output $\overline{\text{RESET}}$ pull-up resistor R_{PU} = 10kΩ, voltage V_{PU} = 5.5V, output $\overline{\text{BIST}}$ pull-up resistor $R_{PU\_\overline{BIST}}$ = 10kΩ, voltage $V_{PU\_\overline{BIST}}$= 5.5V, and load C_{LOAD} = 10pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12V and V_{IT} = 6.5V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Switching Requirements						
$t_{CTR(No\ Cap)}$	$\overline{\text{RESET}}$ release time delay (CTR)[1]	VIT = 800mV C_{CTR} = Open 20% Overdrive from Hysteresis		350	600	µs
$t_{CTS(No\ Cap)}$	Sense detect time delay (CTS)[2]	VIT = 800mV C_{CTS} = Open 20% Overdrive from V_{IT}		85	100	µs
t_{SD}	Startup Delay [3]	C_{CTR} = Open		1		ms
BIST Switching Requirements						
$t_{BIST\_en\_pd}$	Rising edge of BIST_EN to BIST asserting			2.3		µs
$t_{BIST\_en\_pd}$	Rising edge of BIST_EN to RESET asserting			2.3		µs
$t_{\overline{BIST}\_recover}$	Rising edge of $\overline{\text{BIST}}$ to SENSE input valid	C_{CTR} = Open, BIST = Enabled		350	600	µs
$t_{\overline{BIST}}$	BIST run time				3.5	ms
$t_{SD+\overline{BIST}}$	Startup time with BIST run time				4.5	ms
LATCH Switching Requirements						
$t_{BIST\_EN/LATCH\_CLR\_Recover}$	Rising edge of $\overline{\text{BIST}}$ to SENSE input valid	C_{CTR} = Open, BIST = Disabled		10		µs

(1) **CTR Reset detect time delay:**
Overvoltage active-low output is measure from $V_{ITP\ -\ HYS}$ to V_{OH}
Undervoltage active-low output is measure from $V_{ITN\ +\ HYS}$ to V_{OH}

(2) **CTS Sense detect time delay:**
Overvoltage active-low output is measure from V_{ITP} to V_{OL}
Undervoltage active-low output is measure from V_{ITN} to V_{OL}

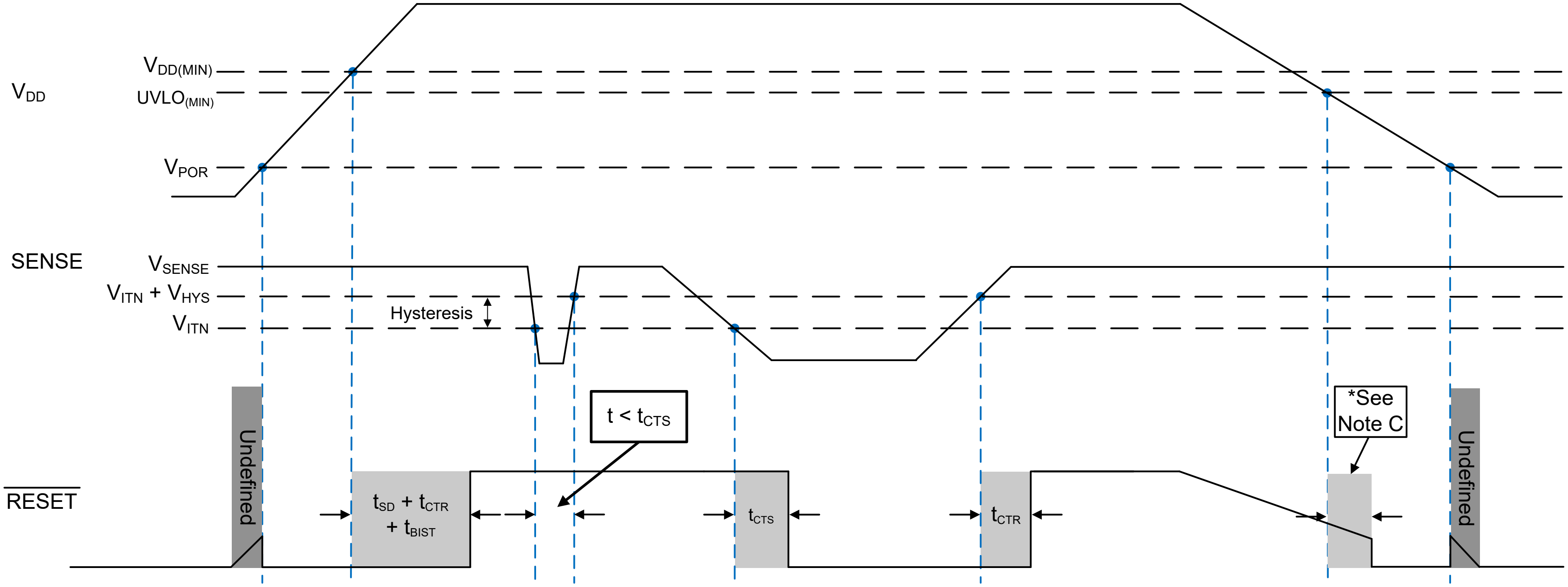
(3) During the power-on sequence, V_{DD} must be at or above $V_{DD\ (MIN)}$ for at least $t_{SD+\overline{BIST}}$ + t_{CTR} before the output is in the correct state based on V_{SENSE}.
t_{SD} time includes the propagation delay (C_{CTR} = Open). Capacitor on CTR will add time to t_{SD}.

7.7 Timing Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open and enabled, output $\overline{\text{RESET}}$ pull-up resistor R_{PU} = 10kΩ, voltage V_{PU} = 5.5V, output $\overline{\text{BIST}}$ pull-up resistor $R_{PU\_\overline{BIST}}$ = 10kΩ, voltage $V_{PU\_\overline{BIST}}$= 5.5V, and load C_{LOAD} = 10pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12V and V_{IT} = 6.5V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters						
BIST timing parameters						
$t_{BIST\_en\ Glitch}$	BIST_EN Glitch immunity			1.1		µs
t_{BIST_en}	Minimum BIST_EN input width to initate BIST			1.2	8	µs
LATCH timing parameters						
$t_{BIST\_EN/LATCH\_CLR\ Glitch}$	Latch Glitch immunity			1.5		µs
$t_{BIST\_EN/LATCH\_CLR}$	Latch input width to clear latch			1.6		µs

8 Timing Diagrams

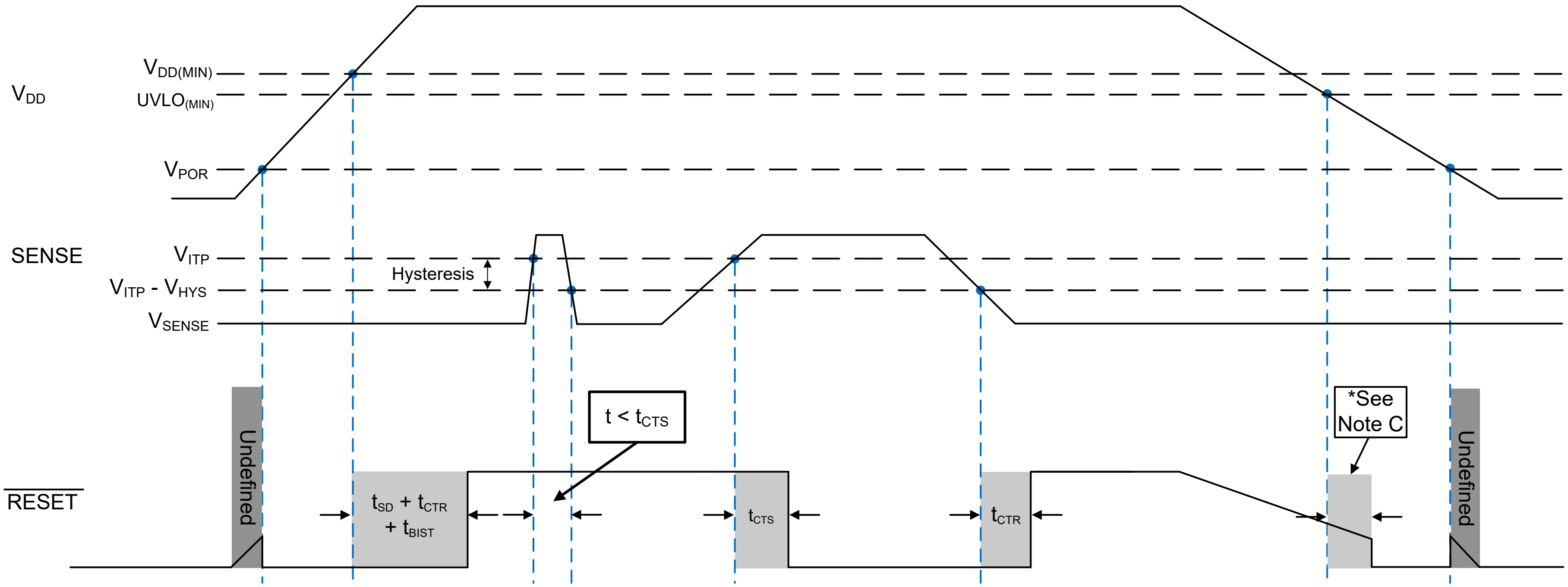


A. The timing diagram assumes the open-drain output $\overline{\text{RESET}}$ pin is connected via an external pull-up resistor to V_{DD}.

B. Be advised that 図 8-1 shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay (t_{CTR}) time.

C. $\overline{\text{RESET}}$ is asserted when V_{DD} goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTR}, is reached.

図 8-1. SENSE Undervoltage (UV) Timing Diagram



A. The timing diagram assumes the open-drain output $\overline{\text{RESET}}$ pin is connected via an external pull-up resistor to V_{DD}.

B. Be advised that 図 8-2 shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay (t_{CTR}) time.

C. $\overline{\text{RESET}}$ is asserted when V_{DD} goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTR}, is reached.

図 8-2. SENSE Overvoltage (OV) Timing Diagram

9 Typical Characteristics

Typical characteristics show the typical performance of the TPS3762-Q1 device. Test conditions are taken at T_A = 25°C, unless otherwise noted.

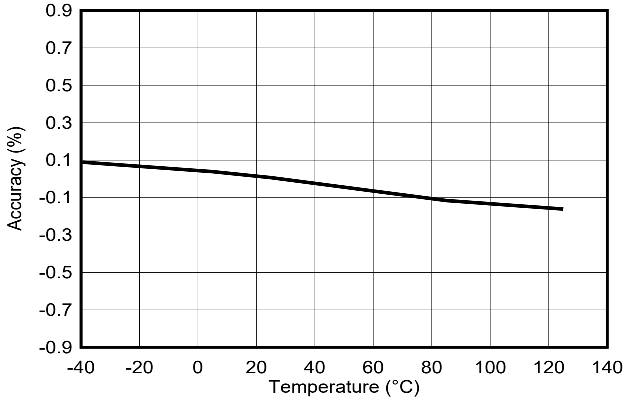


図 9-1. Undervoltage Accuracy vs Temperature (V_{IT} = 0.8V)

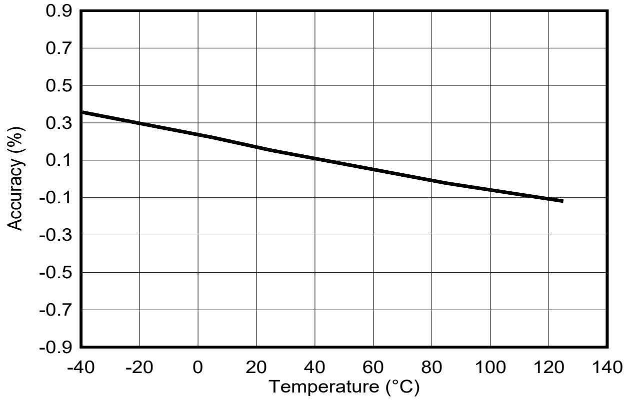


図 9-2. Overvoltage Accuracy vs Temperature (V_{IT} = 0.8V)

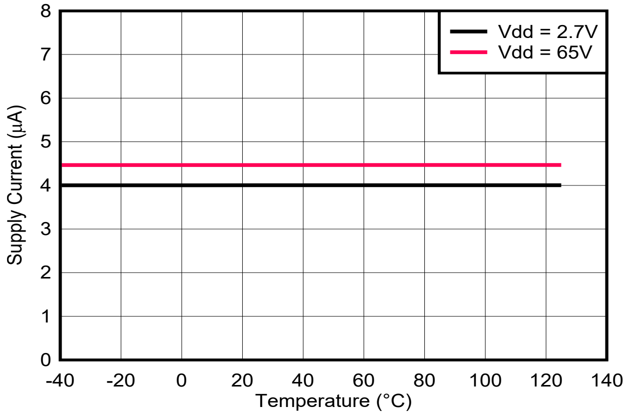


図 9-3. I_{DD} vs Temperature ($\overline{RESET}$ = High, V_{IT} = 0.8V)

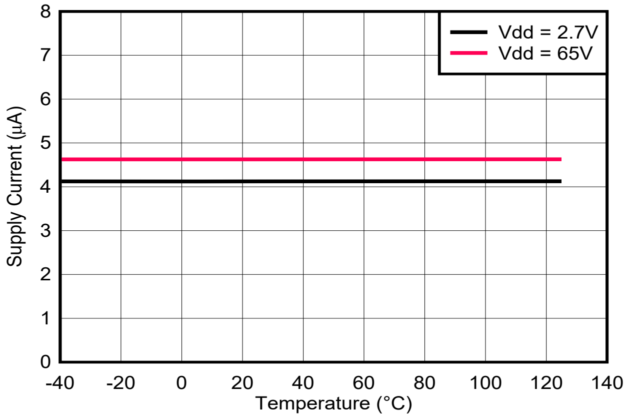


図 9-4. I_{DD} vs V_{DD} ($\overline{RESET}$ = Low, V_{IT} = 0.8V)

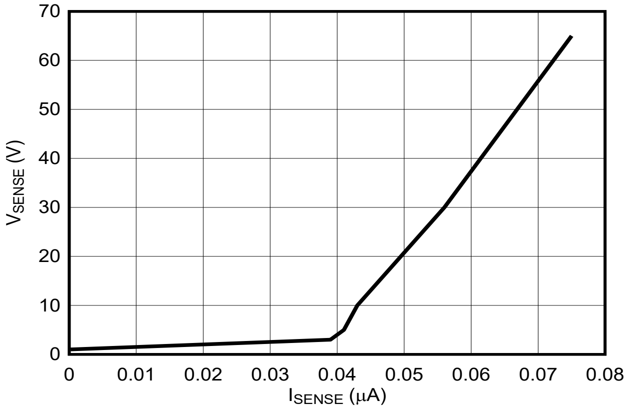


図 9-5. V_{SENSE} vs I_{SENSE} (V_{DD} = 2.7V)

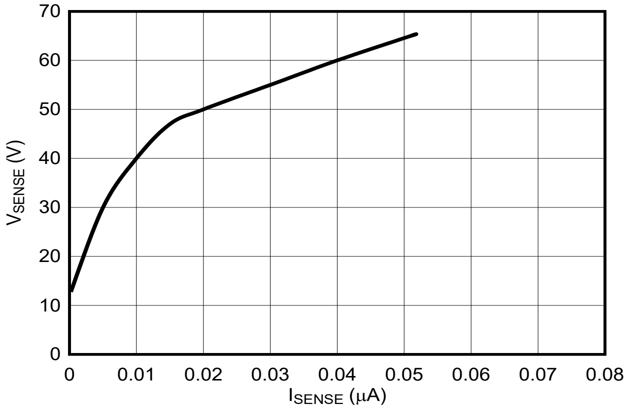


図 9-6. V_{SENSE} vs I_{SENSE} (V_{DD} = 65V)

9 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3762-Q1 device. Test conditions are taken at T_A = 25°C, unless otherwise noted.

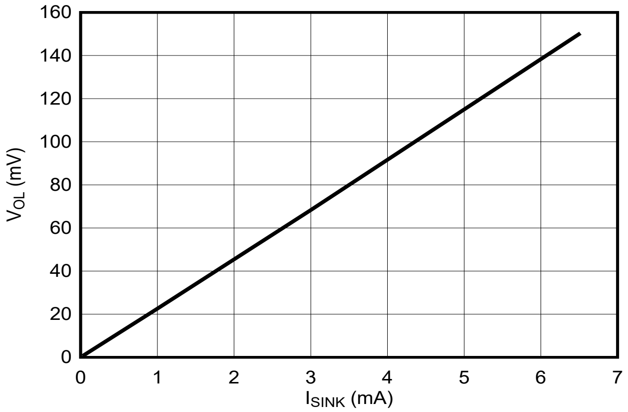


図 9-7. Open-Drain Active Low V_{OL} vs $I_{\overline{RESET}}$ (V_{DD} = 2.7V)

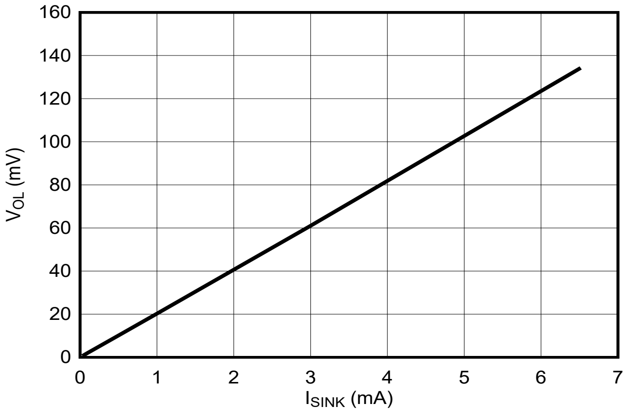


図 9-8. Open-Drain Active Low V_{OL} vs $I_{\overline{RESET}}$ (V_{DD} = 65V)

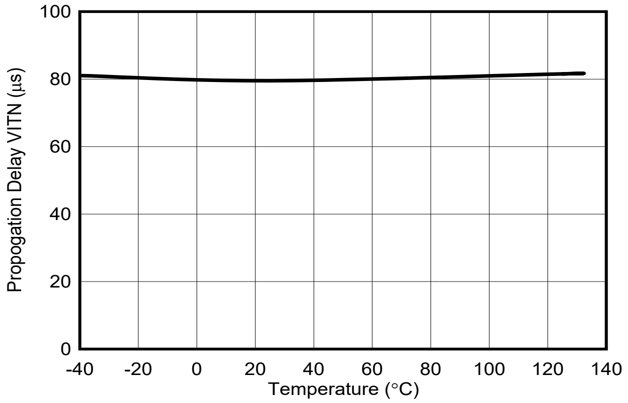


図 9-9. Propogation Delay (Undervoltage) vs Temperature (V_{IT} = 0.8V, CTS = Enabled = 50pF)

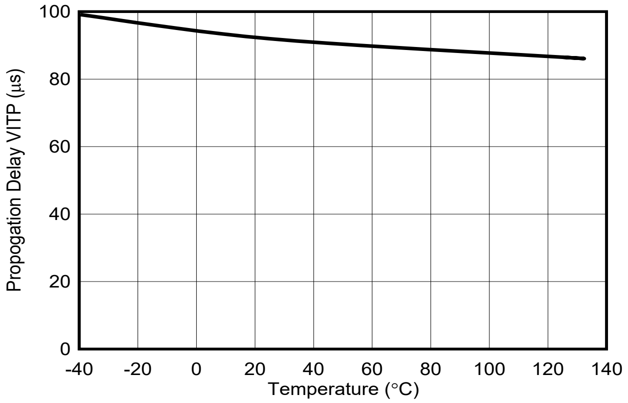


図 9-10. Propogation Delay (Overvoltage) vs Temperature (V_{IT} = 0.8V, CTS = Enabled = 50pF)

10 Detailed Description

10.1 Overview

The TPS3762-Q1 is a family of high voltage and low quiescent current voltage supervisors with overvoltage and undervoltage threshold voltage options, delay timings, Built-In Self-Test, and latch. The TPS3762-Q1 over and undervoltage thresholds are device specific and are offered in either adjustable thresholds or fixed threholds. The adjustable threshold option uses an external resistor ladder to make a voltage divider on SENSE pin which uses the internal 800mV threshold to trigger overvoltage and undervoltage faults. The benefit of using an adjustable option with external resistors is the faster reaction speed compared to a fixed internal threshold variant. The TPS3762-Q1 fixed threshold option utilizes an integrated voltage divider to eliminate the need for external resistors and provides a lower system leakage current.

VDD, SENSE and $\overline{\text{RESET}}$ pins can support 65V continuous operation. SENSE has -65V reverse polarity protection. VDD, SENSE, and $\overline{\text{RESET}}$ voltage levels can be independent of each other. TPS3762-Q1 includes a reset output latching feature that holds the output active to help system achieve safe state. Fixed and programmable sense and reset delay are available to avoid false resets and false reset releases.

10.2 Functional Block Diagram

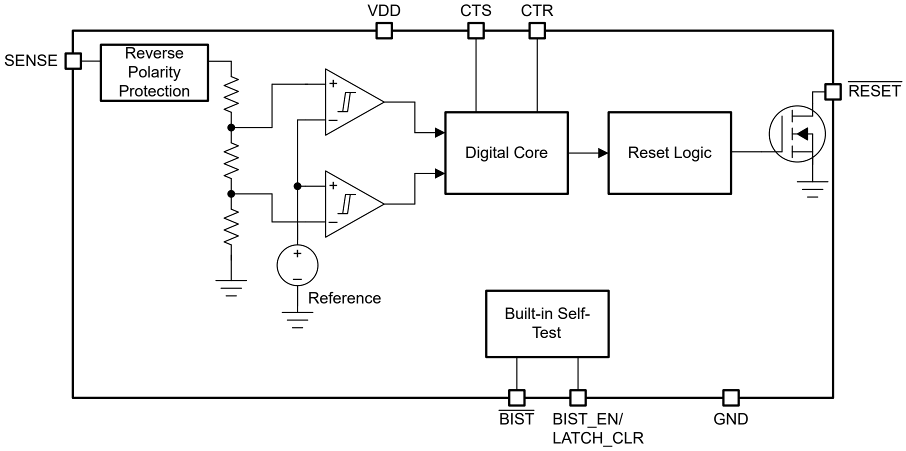


図 10-1. Fixed Threshold Functional Block Diagram

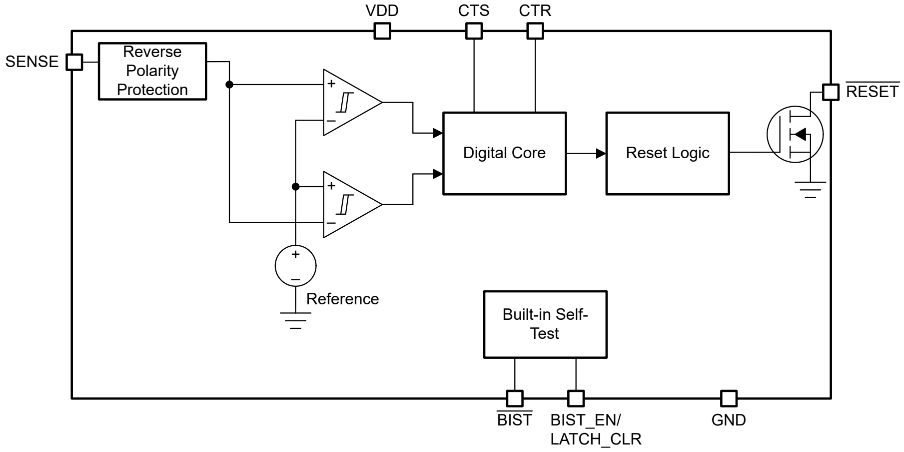


図 10-2. Adjustable Threshold Functional Block Diagram

10.3 Feature Description

10.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7V to 65V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1µF capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET}, meaning that VDD can be higher or lower than the other pins.

10.3.1.1 Undervoltage Lockout ($V_{POR} < V_{DD} <$ UVLO)

When the voltage on V_{DD} is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the $\overline{\text{RESET}}$ and $\overline{\text{BIST}}$ pins will be asserted, regardless of the voltage at SENSE pin.

10.3.1.2 Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

Note: 図 10-3 and 図 10-4 assume an external pull-up resistor is connecting the $\overline{\text{RESET}}$ pin to VDD.

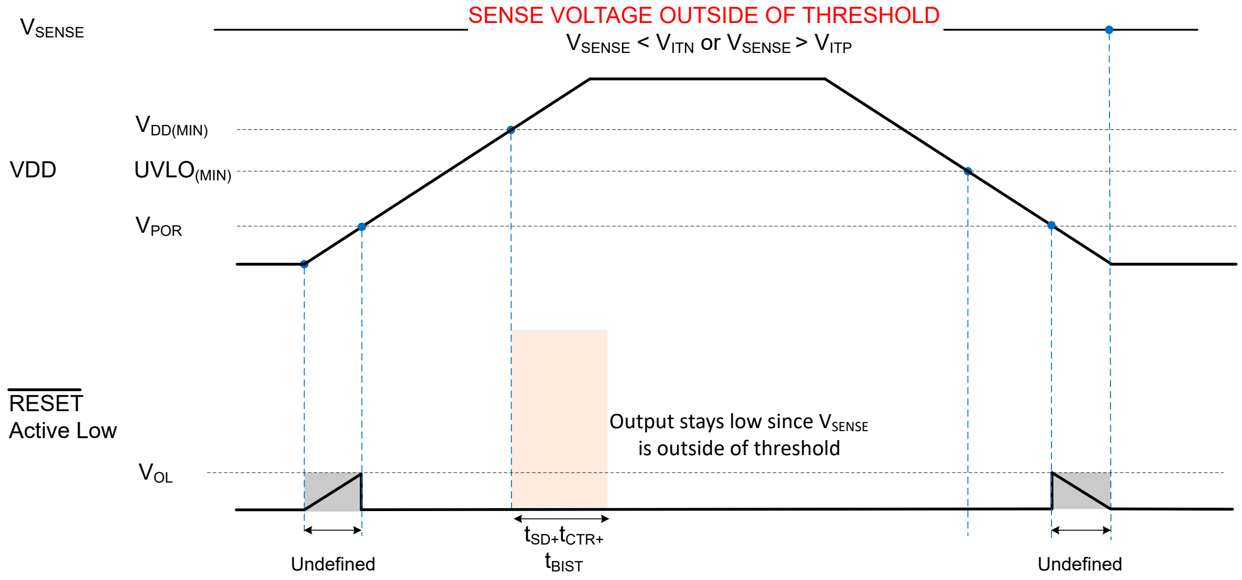


図 10-3. Power Cycle (SENSE Outside of Nominal Voltage)

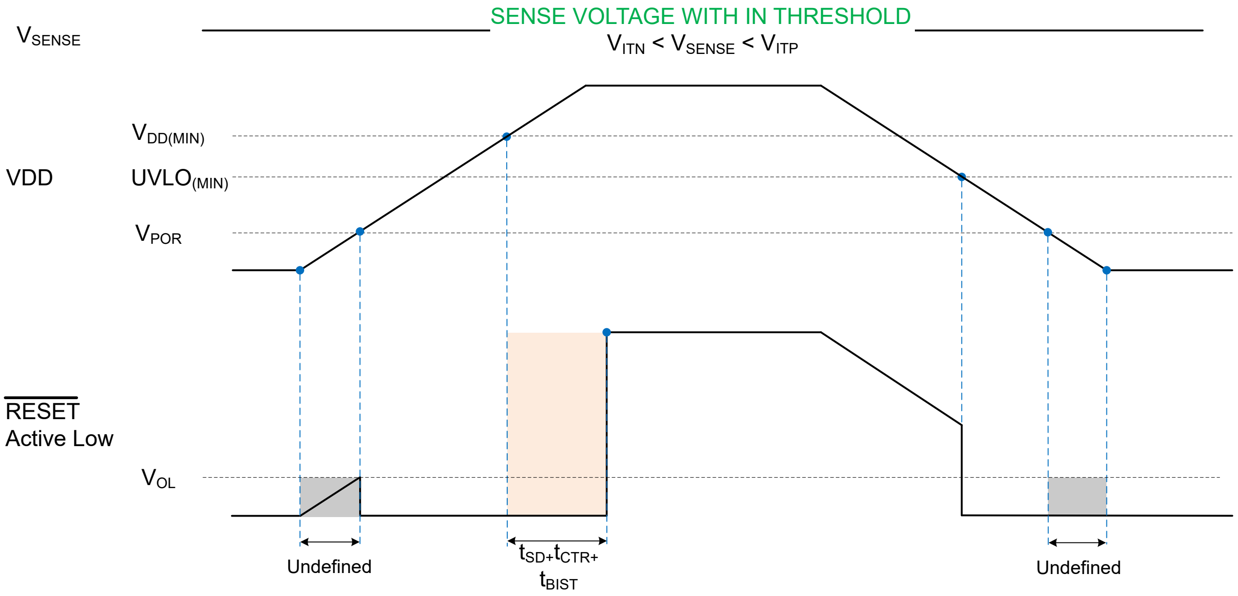


図 10-4. Power Cycle (SENSE Within Nominal Voltage)

10.3.2 SENSE

The SENSE pin connects to the supply rail that is to be monitored. The sense pin on each device is configured to monitor either overvoltage (OV), undervoltage (UV), or window (OV&UV) conditions. TPS3762-Q1 device offers built-in hysteresis that provides noise immunity and maintains stable operation.

Although not required in most cases, for noisy applications where t_{CTS} is not sufficient glitch rejection, good analog design practice is to place a 10nF to 100nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal. SENSE can be connected directly to VDD pin.

10.3.2.1 Reverse Polarity Protection

The TPS3762-Q1 has reverse polarity protection on the sense pin up to -65V. This allows the TPS3762-Q1 to support accidental or test simulated reverse connections without damaging the device. This protection permits the TPS3762-Q1 to connect directly off of the supply prior to any reverse polarity protection diodes for accurate voltage measurement.

10.3.2.2 SENSE Hysteresis

TPS3762-Q1 device offers built-in hysteresis around the UV and OV thresholds to avoid erroneous $\overline{\text{RESET}}$ deassertions. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

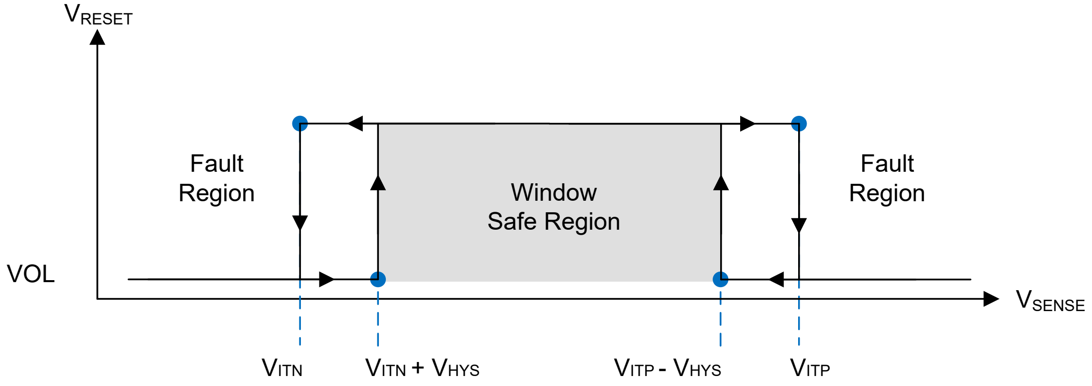


図 10-5. Hysteresis (Undervoltage & Overvoltage Active-Low)

表 10-1. Common Adjustable Hysteresis Lookup Table

TARGET			DEVICE HYSTERESIS OPTION
ADJUSTABLE THRESHOLD	**TOPOLOGY**	**RELEASE VOLTAGE (V)**	
800mV	Overvoltage	784mV	-2%
800mV	Overvoltage	760mV	-5%
800mV	Overvoltage	720mV	-10%
800mV	Undervoltage	816mV	2%
800mV	Undervoltage	840mV	5%
800mV	Undervoltage	880mV	10%

表 10-1 shows a sample of hysteresis for the 800mV adjustable variant of TPS3762-Q1.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is (V_{ITN} + V_{HYS}) and for the overvoltage (OV) channel is (V_{ITP} - V_{HYS}).

Undervoltage (UV)

V_{ITN} = 800mV

Voltage Hysteresis (V_{HYS}) = 2% = 16mV

Hysteresis Accuracy = +1.5% to +2.5% = 16.24mV to 16.4mV

Release Voltage = V_{ITN} + V_{HYS} = 816.24mV to 816.4mV

Overvoltage (OV)

V_{ITP} = 800mV

Voltage Hysteresis (V_{HYS}) = 2% = 16mV

Hysteresis Accuracy = +1.5% to +2.5% = 16.24mV to 16.4mV

Release Voltage = V_{ITP} - V_{HYS} = 783.6mV to 783.76mV

10.3.3 Output Logic Configurations

TPS3762-Q1 is a single channel device that has a single input SENSE pin and a single $\overline{\text{RESET}}$ pin. The single $\overline{\text{RESET}}$ is available only with open drain topology.

10.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system V_{OH} and the Open-Drain Leakage Current (I_{lkg}) provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS3762-Q1 open-drain output pin.

10.3.3.2 Active-Low ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ (active low) denoted with a bar above the pin label. $\overline{\text{RESET}}$ remains high voltage (V_{OH}, deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage the SENSE voltage needs to cross the upper boundary (V_{ITP}).

10.3.3.3 Latching

The TPS3762-Q1 comes with the optional output reset latching feature, check the セクション 5 to verify variant specific latch functionality. When using a variant with latch enabled ($V_{BIST\_EN/LATCH\_CLR}$ <0.5V), whenever a fault, OV or UV, occurs $\overline{\text{RESET}}$ asserts and goes low and remains low until cleared by a logic high input ($V_{BIST\_EN/LATCH\_CLR}$ > 1.3V) on the BIST_EN / LATCH_CLR pin. If the SENSE pin is in a safe region and latch is disabled, the $\overline{\text{RESET}}$ deasserts after a delay. This delay is dependent on BIST and CTR timing. See セクション 10.3.6 for more details. While $V_{BIST\_EN/LATCH\_CLR}$ > 1.3V, the device is in latch disabled mode and the $\overline{\text{RESET}}$ does not latch for OV and UV on SENSE pin. While the device is in latch disabled mode the $\overline{\text{RESET}}$ asserts for OV and UV faults. When $V_{BIST\_EN/LATCH\_CLR}$ < 0.5V, latch mode is enabled.

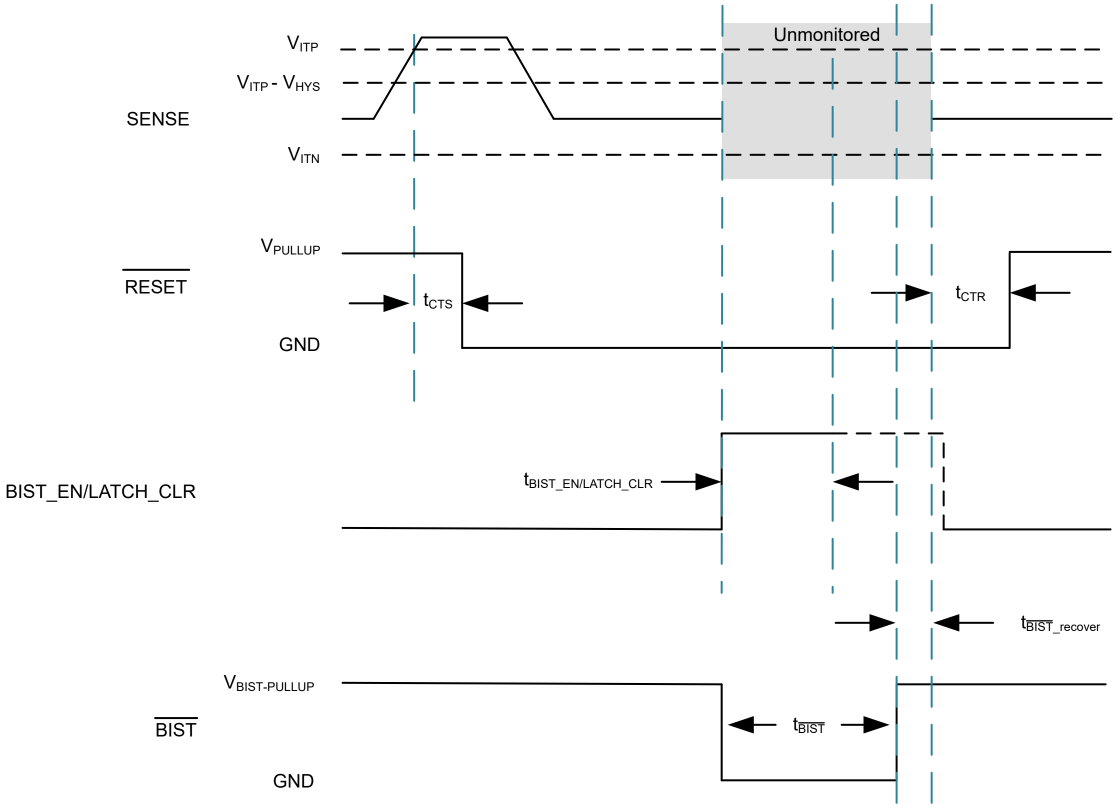


図 10-6. $\overline{\text{RESET}}$ Latch & Unlatch

10.3.3.4 UVBypass

The TPS3762-Q1 comes with the optional undervoltage bypass (UVbypass) feature, check セクション 5 to verify variant specific UVbypass functionality. When using a variant with UVbypass enabled, the first undervoltage event after V_{DD} > V_{POR} is ignored. In cases where an undervoltage event has not occurred UVbypass can be cleared by running BIST.

UVbypass is targeted at specific applications in which the TPS3762-Q1 is powered Off-battery and is monitoring the Off-battery DC-DC output, as shown in 図 10-7. If the Off-battery DCDC output is outside of threshold the TPS3762-Q1 resets this device. See 図 10-8 and 図 10-9 for more details.

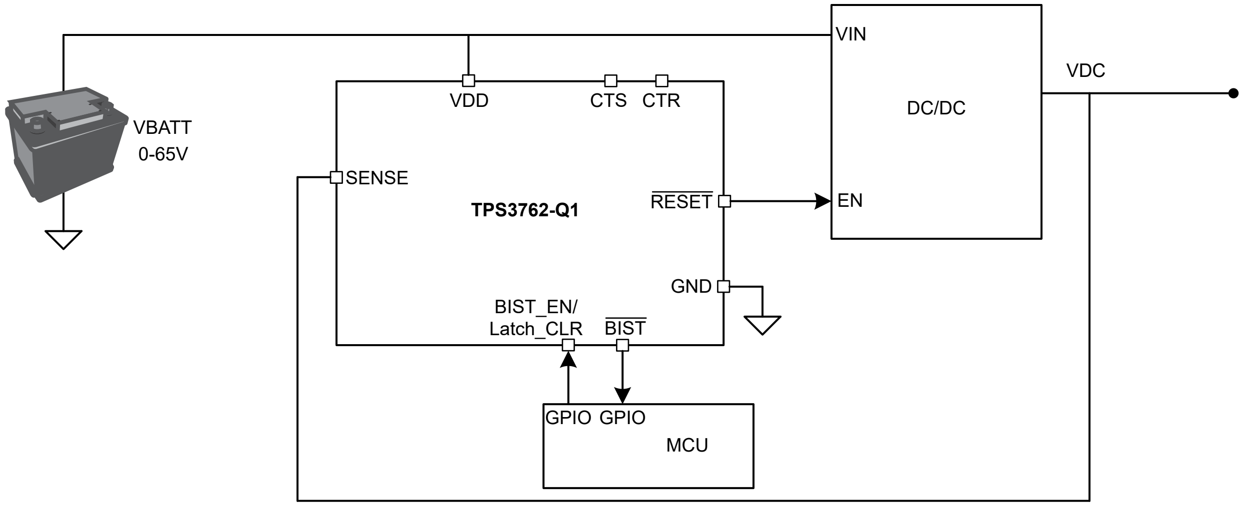


図 10-7. UVbypass Schematic

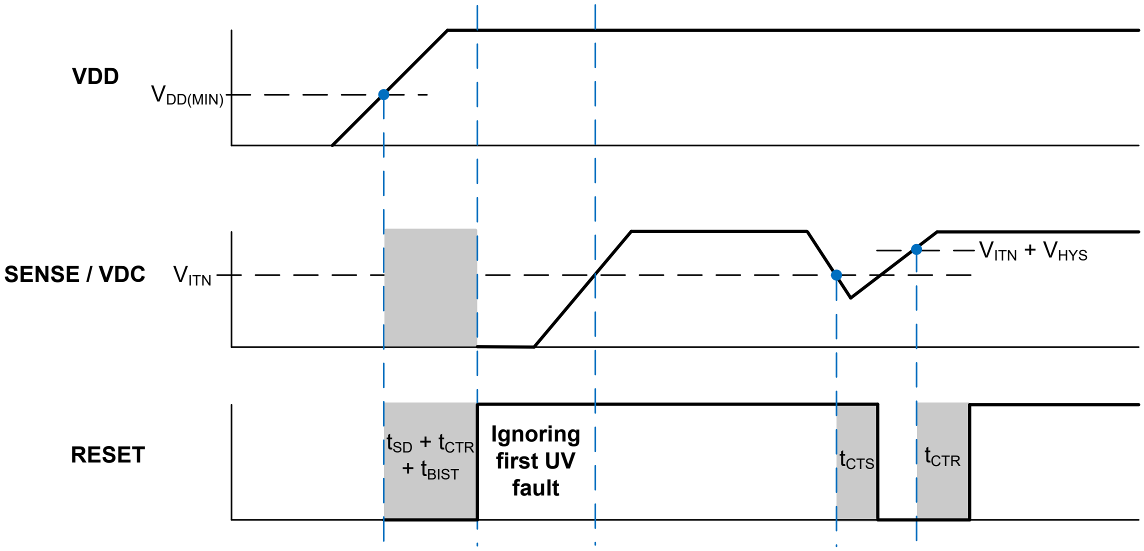


図 10-8. UVbypass Enabled

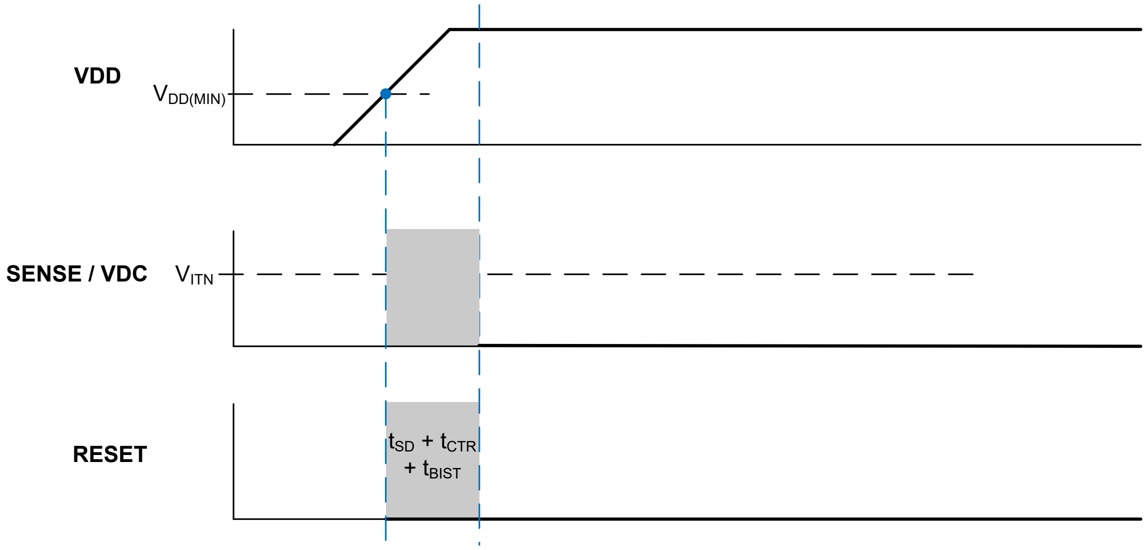


図 10-9. UVbypass Disabled

10.3.4 User-Programmable Reset Time Delay

TPS3762-Q1 has adjustable reset release time delay with external capacitors.

- A capacitor on CTR programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time indicated by t_{CTR} in セクション 7.6.
- Variants such as TPS3762Q use a fixed internal time delay. check the セクション 5 to verify variant specific timing.

10.3.4.1 Reset Time Delay Configuration

RESET time delay (t_{CTR}) occurs when the $\overline{\text{RESET}}$ is transitioning from a fault state (V_{OL}) to a non-fault state (V_{OH}). The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND. For situations with a fault on SENSE after $\overline{\text{RESET}}$ recovers, the TPS3762-Q1 makes sure that the CTR capacitor is fully discharged before starting the recovery sequence. This makes sure that the programmed CTR time is maintained for consecutive faults.

The relationship between external capacitor $C_{CTR\_EXT\ (typ)}$ and the time delay $t_{CTR\ (typ)}$ is given by 式 1.

$$t_{CTR\ (typ)} = R_{CTR\ (typ)} \text{ x } C_{CTR\_EXT\ (typ)} + t_{CTR\ (no\ cap)} \text{ x } 10^{-6} \tag{1}$$

$R_{CTR\ (typ)}$ = is in mega ohms (MΩ)

$C_{CTR\_EXT\ (typ)}$ = is given in microfarads (µF)

$t_{CTR\ (typ)}$ = is the reset time delay/delays

The reset delay varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in セクション 7.5, and the constant ($t_{CTR\ (no\ cap)}$) provided in セクション 7.6. The minimum and maximum variance due to the constant is show in 式 2 and 式 3:

$$t_{CTR\ (min)} = R_{CTR\ (min)} \text{ x } C_{CTR\_EXT\ (min)} + t_{CTR\ (no\ cap\ (min))} \text{ x } 10^{-6} \tag{2}$$

$$t_{CTR\ (max)} = R_{CTR\ (max)} \text{ x } C_{CTR\_EXT\ (max)} + t_{CTR\ (no\ cap\ (max))} \text{ x } 10^{-6} \tag{3}$$

There is no limit to the capacitor on CTR pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold $\overline{\text{RESET}}$ active.

* Leakages on the capacitor can effect accuracy of reset time delay.

10.3.5 User-Programmable Sense Delay

TPS3762-Q1 has adjustable sense release time delay with external capacitors.

- A capacitor on CTS programs the sense time delay of the input.
- No capacitor on this pin gives the fastest sense delay time indicated by t_{CTS} in セクション 7.7.
- The TPS3762-Q1 comes with an optional fixed internal time delay that ignores the capacitor value at the CTS pin, check the セクション 5 to verify variant specific functionality.

10.3.5.1 Sense Time Delay Configuration

SENSE time delay (t_{CTS}) occurs when the $\overline{\text{RESET}}$ is transitioning from a non-fault state (V_{OH}) to a fault state (V_{OL}). The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS\_EXT\ (typ)}$ and the time delay $t_{CTS\ (typ)}$ is given by 式 4.

$$t_{CTS\ (typ)} = R_{CTS\ (typ)} \text{ x } C_{CTS\_EXT\ (typ)} + t_{CTS\ (no\ cap)} \text{ x } 10^{-6} \tag{4}$$

$R_{CTS\ (typ)}$ = is in mega ohms (MΩ)

$C_{CTS\_EXT\ (typ)}$ = is given in microfarads (μF)

$t_{CTS\ (typ)}$ = is the sense time delay/delays

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTS}) provided in セクション 7.5, and the constant ($t_{CTS\ (no\ cap)}$) provided in セクション 7.6. The minimum and maximum variance due to the constant is show in 式 5 and 式 6:

$$t_{CTS\ (min)} = R_{CTS\ (min)} \text{ x } C_{CTS\_EXT\ (min)} + t_{CTS\ (no\ cap\ (min))} \text{ x } 10^{-6} \tag{5}$$

$$t_{CTR\ (max)} = R_{CTS\ (max)} \text{ x } C_{CTS\_EXT\ (max)} + t_{CTSx\ (no\ cap\ (max))} \text{ x } 10^{-6} \tag{6}$$

The recommended maximum sense delay capacitor for the TPS3762-Q1 is 10μF as this makes sure there is enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip unpredictably. This leads to a variation in time delay where the delay accuracy can be worse in the presence of system noise.

* Leakages on the capacitor can effect accuracy of sense time delay.

10.3.6 Built-In Self-Test

The TPS3762-Q1 has a Built-In Self-Test (BIST) feature that runs diagnostics internally in the device. During power-up BIST is initiated automatically after crossing $V_{DD(min)}$. During BIST the $\overline{BIST}$ pin and $\overline{RESET}$ output asserts low and deasserts if the $\overline{BIST}$ test completes successfully indicating no internal faults in the device. The length of the BIST and $\overline{BIST}$ assertion is specified by $t_{\overline{BIST}}$. If BIST is not successful, the $\overline{BIST}$ pin will say asserted low signifying an internal fault. The $\overline{RESET}$ output will stay assert on $\overline{BIST}$ failure. During BIST, the device is not monitoring the SENSE pin for faults and the $\overline{RESET}$ is not dependent on the SENSE pin voltage. The $\overline{BIST}$ sequence of internal tests verifies the internal signal chain of the device by checking for faults on the internal comparators on the SENSE pin, bandgap voltage, and the $\overline{RESET}$ output. See 図 10-10 for more details.

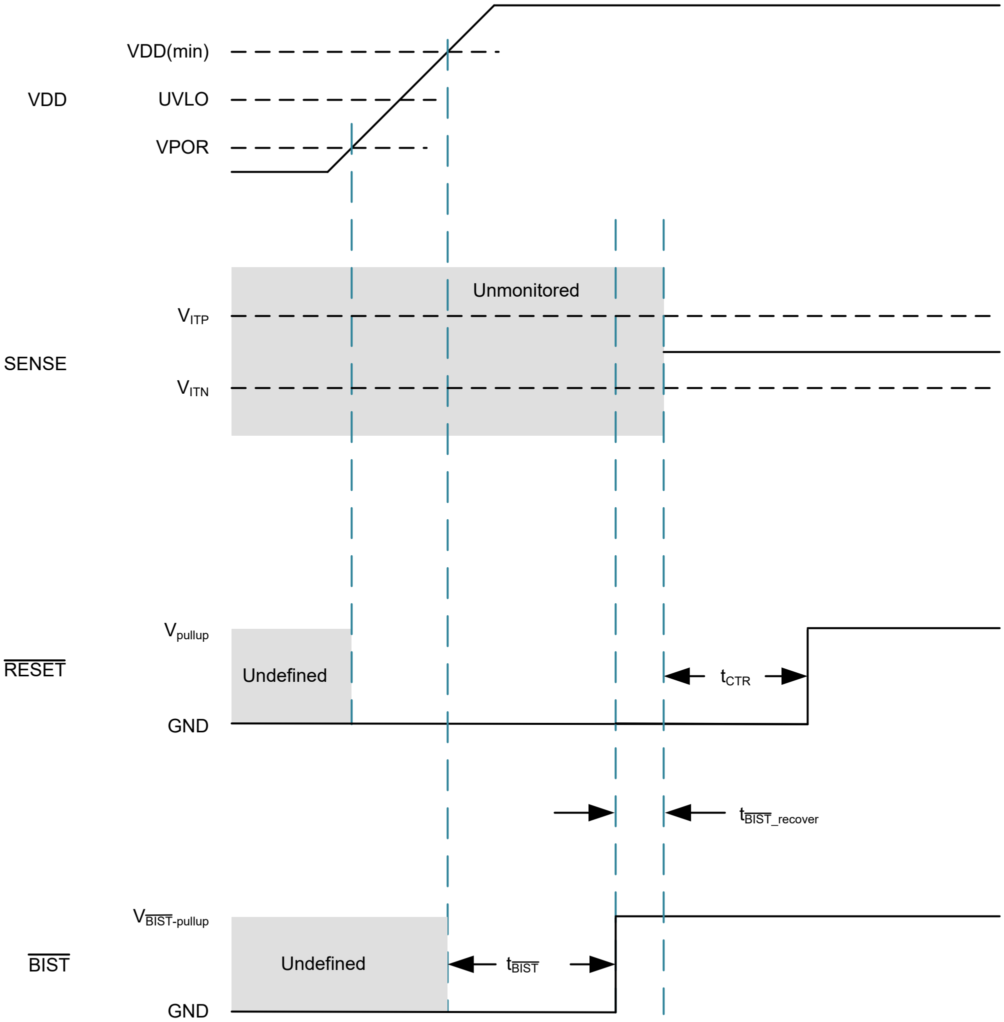


図 10-10. TPS3762-Q1 Start-Up Sequence

After a successful power-up sequence, BIST can be initiated any time with a logic high input (V_{BIST_EN} or $V_{BIST\_EN/LATCH\_CLR}$ > 1.3V) on the BIST_EN / LATCH_CLR pin. BIST initiates and the $\overline{BIST}$ pin asserts only if the SENSE pin is not in a overvoltage or undervoltage fault mode. During this BIST test time period, $t_{\overline{BIST}}$, $\overline{BIST}$ pin asserts low to signify that $\overline{BIST}$ has started and $\overline{RESET}$ assertion is dependent on the device variant. Upon a successful BIST the $\overline{BIST}$ pin and $\overline{RESET}$ pin are deasserted. If BIST is not successful due to an internal device not working properly, the $\overline{RESET}$ pin and $\overline{BIST}$ pin remain asserted low signifying a fault internal to the device. See 図 10-11 and 図 10-12 for more details.

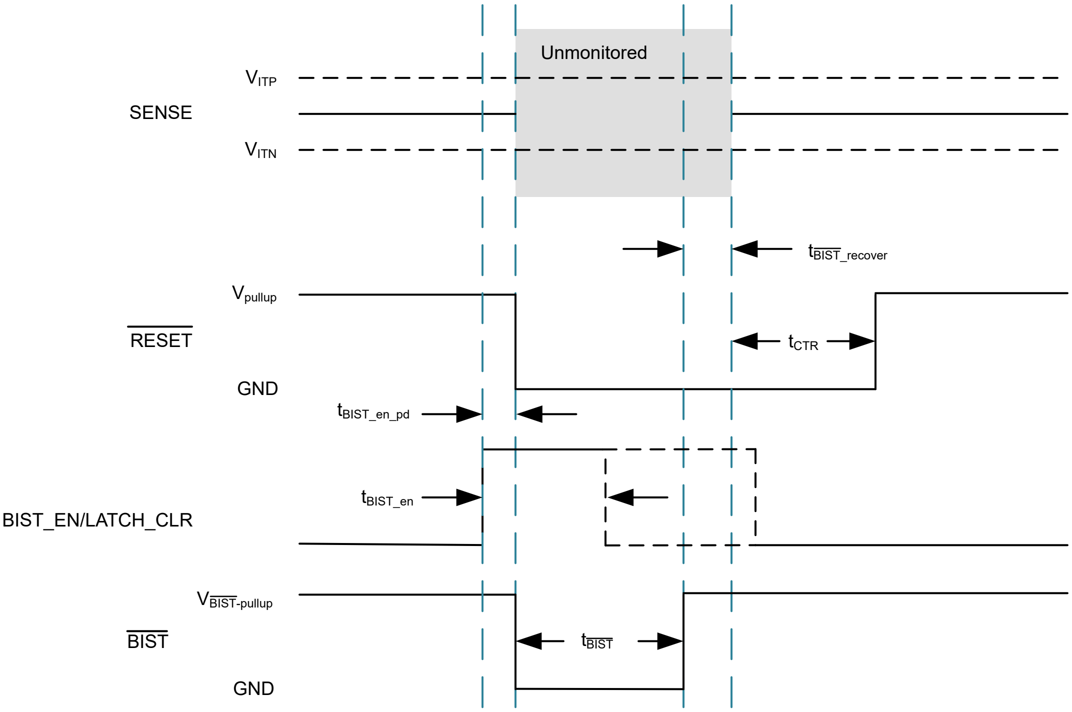


図 10-11. $\overline{\text{BIST}}$ With $\overline{\text{RESET}}$ Assertion

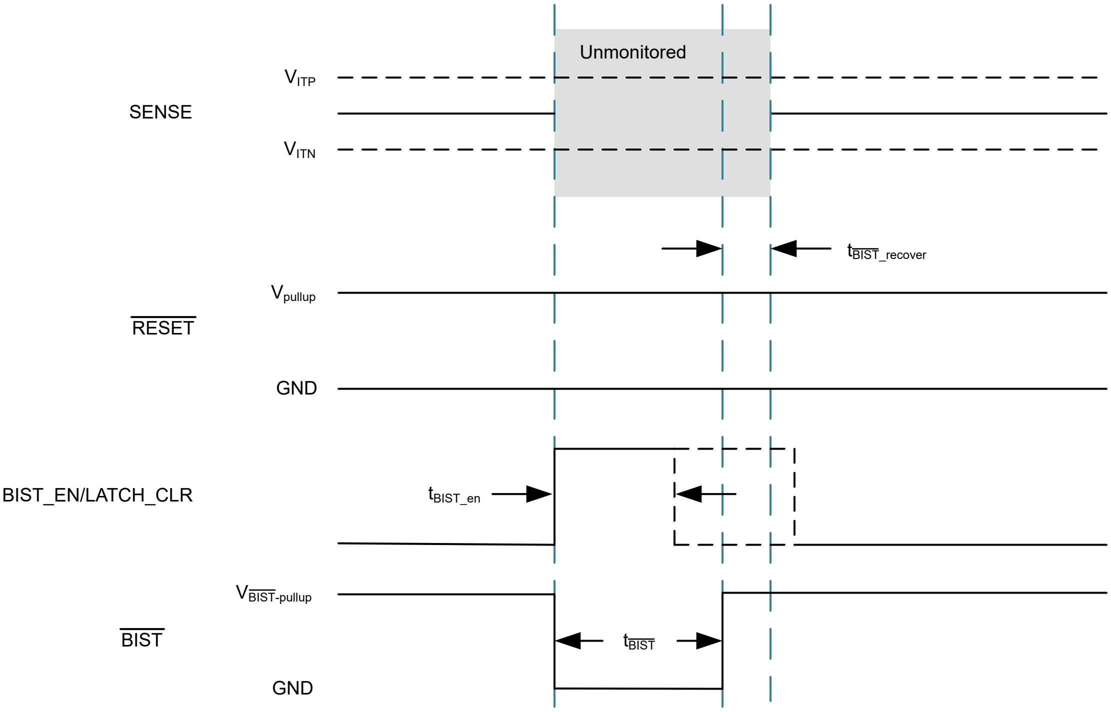


図 10-12. $\overline{\text{BIST}}$ With No $\overline{\text{RESET}}$ Assertion

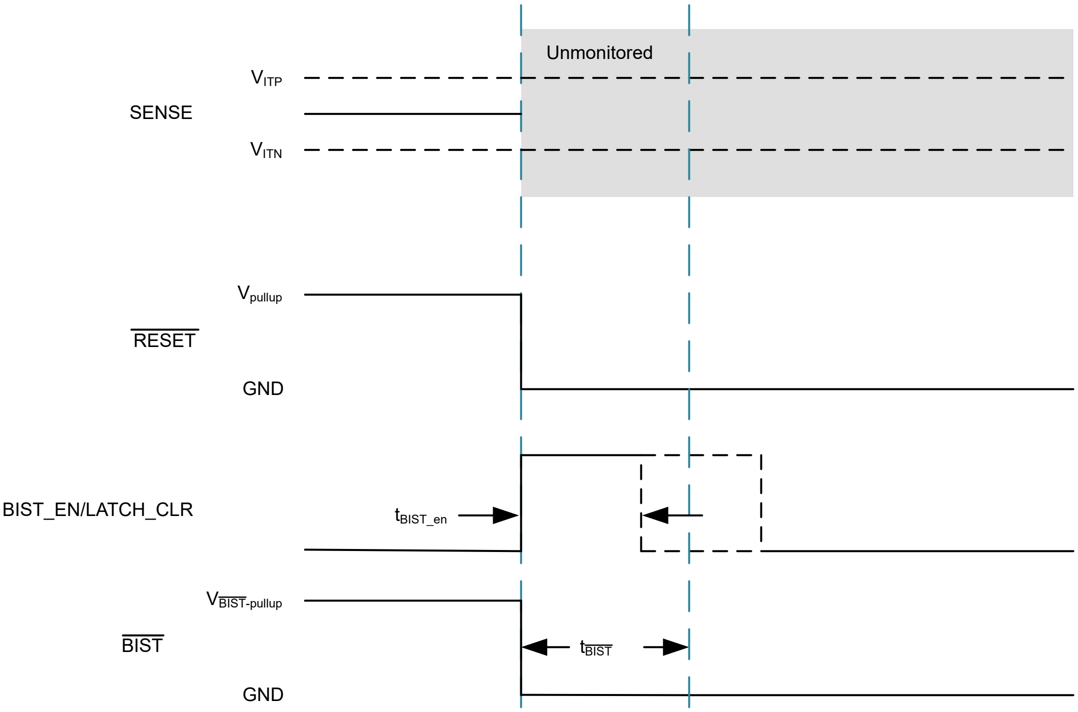


図 10-13. $\overline{\text{BIST}}$ Fail With $\overline{\text{RESET}}$ Assertion

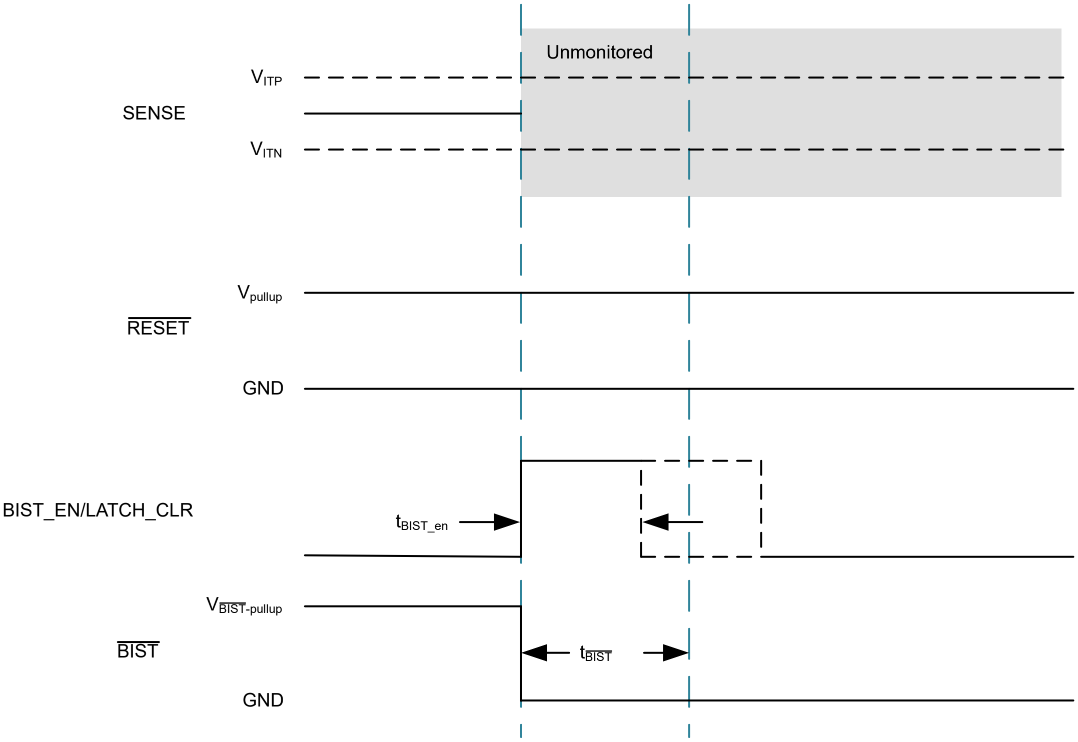


図 10-14. $\overline{\text{BIST}}$ Fail With No $\overline{\text{RESET}}$ Assertion

10.4 Device Functional Modes

表 10-2. Undervoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR [(1)] / $\overline{\text{MR}}$ PIN	V_{DD} PIN	OUTPUT [(2)] ($\overline{\text{RESET}}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE > V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Undervoltage Detection	SENSE > V_{ITN}	SENSE < V_{ITN}	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Undervoltage Detection	SENSE < V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	SENSE < V_{ITN}	SENSE > V_{ITN} + HYS	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
UVLO Engaged	SENSE > V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	$V_{POR} < V_{DD} < V_{DD(MIN)}$	Low
Below V_{POR}, Undefined Output	SENSE > V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

表 10-3. Overvoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR [(1)] / $\overline{\text{MR}}$ PIN	V_{DD} PIN	OUTPUT [(2)] ($\overline{\text{RESET}}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE < V_{ITN}	SENSE < V_{ITN}	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Overvoltage Detection	SENSE < V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Overvoltage Detection	SENSE > V_{ITN}	SENSE < V_{ITN}	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	SENSE > V_{ITN}	SENSE < V_{ITN} - HYS	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
UVLO Engaged	SENSE < V_{ITN}	SENSE < V_{ITN}	Open or capacitor connected	$V_{POR} < V_{DD}$ < UVLO	Low
Below V_{POR}, Undefined Output	SENSE < V_{ITN}	SENSE < V_{ITN}	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

11 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

11.2 Adjustable Voltage Thresholds

図 11-1 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the adjustable (0.8V voltage threshold device) when setting adjustable voltage thresholds. This variant bypasses the internal resistor ladder.

For example, consider a 12V rail, V_{MON}, being monitored for overvoltage (OV) using of the TPS3762D02OVDDFRQ1 variant, as shown in 図 11-1. The monitored OV threshold, denoted as V_{MON+}, is the desired voltage where the device asserts the reset. For this example V_{MON+} = 35V. To assert an overvoltage reset the voltage at the sense pin, V_{SENSE}, needs to be equal to the input threshold positive, V_{ITP}. For this example variant $V_{SENSE} = V_{ITP}$ = 0.8V. Using R_1 and R_2 the correlation between V_{MON+} and V_{SENSE} can be seen in 式 8. Assuming R_2 = 10kΩ, and R_1 can be calculated as R_1 = 427.5kΩ.

$$V_{SENSE} = V_{MON+} \times (R_2 \div (R_1 + R_2)) \tag{7}$$

The TPS3762D02OVDDFRQ1 comes with variant specific 2%, 5%, or 10% voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} must go below $V_{ITP} - V_{HYS}$. For this example variant a 2% voltage threshold hysteresis was selected. Therefore, V_{MON} equals 34.3V when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is the internal resistance of the SENSE pin that can affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance (R_{SENSE}) can be calculated by the SENSE voltage (V_{SENSE}) divided by the SENSE current (I_{SENSE}) as shown in 式 9. V_{SENSE} can be calculated using 式 7 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using 式 8.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \tag{8}$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \tag{9}$$

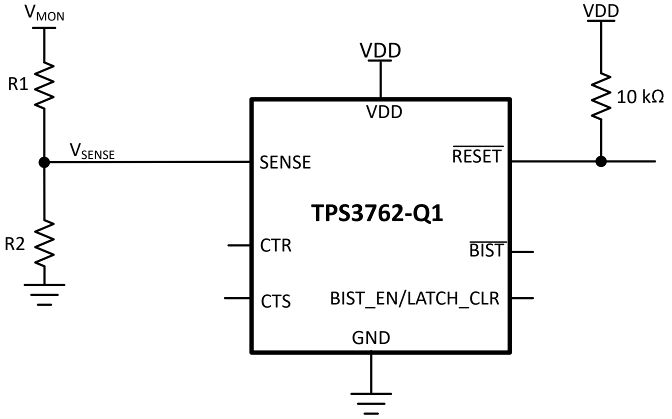


図 11-1. Adjustable Voltage Threshold with External Resistor Dividers

11.3 Typical Application

11.3.1 Design 1: Off-Battery Monitoring

This application is intended for the initial power stage in applications with the 12V batteries. The TPS3762-Q1 utilizes high-voltage SENSE and V_{DD} inputs to monitor an automotive battery.

図 11-6 illustrates an example of how the TPS3762-Q1 is monitoring the battery voltage while being powered by it, as well.

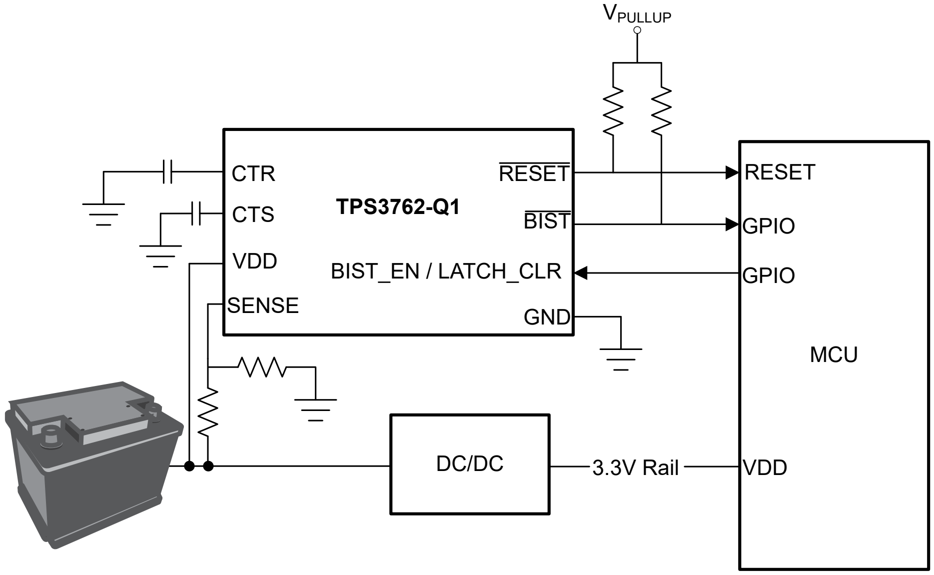


図 11-2. Off-Battery Monitoring

11.3.1.1 Design Requirements

表 11-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Voltage Threshold	Typical OV voltage threshold 30V.
Maximum Input Power	Operate with power supply input up to 65V
Output Logic	Open-Drain
SENSE Delay	>100ms
$\overline{\text{RESET}}$ Delay	>300ms
Output Features	Output latching and built-in self-test

11.3.1.2 Detailed Design Procedure

The TPS3762-Q1 utilizes high-voltage SENSE and V_{DD} inputs to monitor an automotive battery. In this design example TPS3762D02OVDDFRQ1 is used.

11.3.1.2.1 Setting Voltage Threshold

The positive-going threshold voltage, V_{ITP}, is set by the device variant. In this example, the nominal supply voltage from the battery is 12V. Setting a overvoltage threshold of 30V makes sure that the device resets before supply voltage violates the allowed boundary. The adjustable voltage variant is chosen and R_1 and R_2 are adjusted to meet the threshold. Assuming R_2 equal to 10kΩ and R_1 is calculated as 365kΩ. For additional information on selecting resistor values see セクション 11.2. TPS3762-Q1 also supports fixed voltage threshold variants. Threshold voltage decoding can be found in Device Decoder.

11.3.1.2.2 Meeting the Sense and Reset Delay

The TPS3762-Q1 features both reset assertion (sense) delay, t_{CTS}, and reset deassertion (reset) delay, t_{CTR}. The TPS3762-Q1 features two options for selecting sense and reset delays: fixed delays and capacitor-programmable delays. For the device variant used in this design, TPS3762D02OVDDFRQ1, the capacitor programmable delay is chosen. セクション 10.3.5 and セクション 10.3.4 show how to set the timings for the capacitor-programmable delays. The application requires greater than 100 ms sense delay, thus a 0.033 μF capacitor is used. The application requires greater than 300 ms reset delay, thus a 0.1 μF capacitor is used.

11.3.1.2.3 Setting Supply Voltage

Setting the supply voltage is done by connecting the V_{DD} input directly to the battery rail without the need for external circuitry. The device being able to handle 65V on V_{DD} means the monitored voltage rail can handle any voltage transience up to 65V. Good analog design practice recommends using a 0.1 μF capacitor on the V_{DD} pin.

11.3.1.2.4 Initiating Built-In Self-Test and Clearing Latch

Built-In Self-Test (BIST) is asserted on device power-up, as outlined in 図 10-10. BIST can also be initiated any time by a rising edge that crosses the voltage logic high input (V_{BIST_EN} or $V_{BIST\_EN/LATCH\_CLR}$ > 1.3V) on the BIST_EN / LATCH_CLR pin, as outlined in 図 10-11. Output reset latching is set by the device variant. For the device variant used in this design, TPS3762D02OVDDFRQ1, the output has latch. Device specific output reset latching feature can be found in Device Decoder. To clear the latch a logic high input on the BIST_EN / LATCH_CLR pin is required. When clearing latch, BIST is initiated and the $\overline{\text{RESET}}$ returns logic level high once t_{BIST} + $t_{BIST\_recover}$ + t_{CTR} has expired, outlined in 図 10-6. While $V_{BIST\_EN/LATCH\_CLR}$ > 1.3V, the device is in latch disabled mode and the $\overline{\text{RESET}}$ does not latch for OV and UV on SENSE pin. While the device is in latch disabled mode the $\overline{\text{RESET}}$ still asserts for OV and UV faults.

11.3.1.3 Application Curves

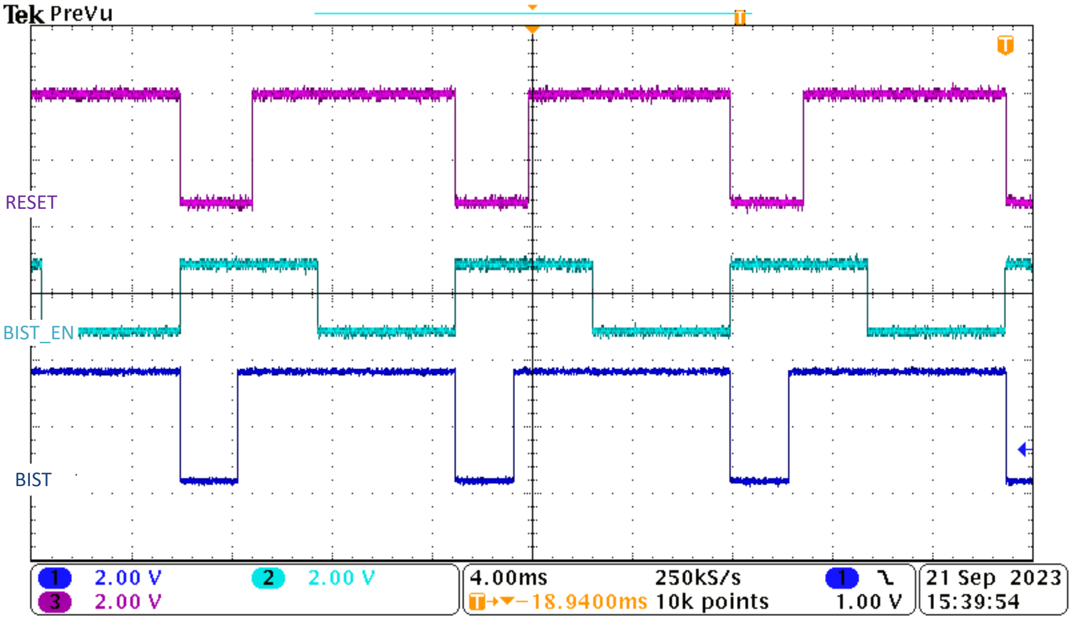


図 11-3. BIST with $\overline{\text{RESET}}$ Assertion Waveform

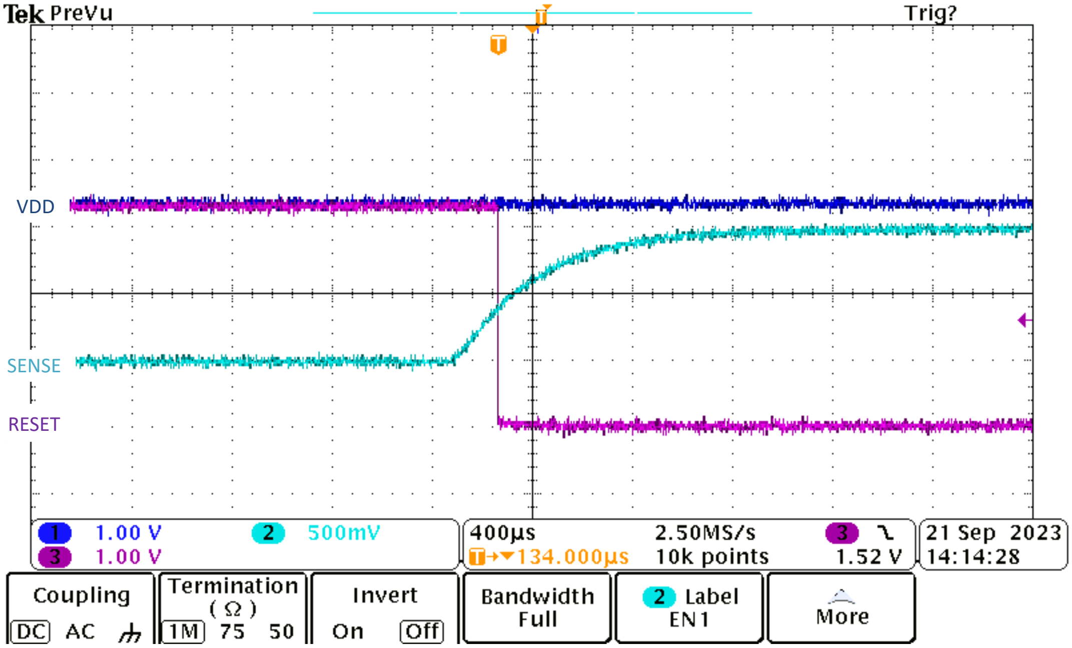


図 11-4. Overvoltage $\overline{\text{RESET}}$ Latching Waveform

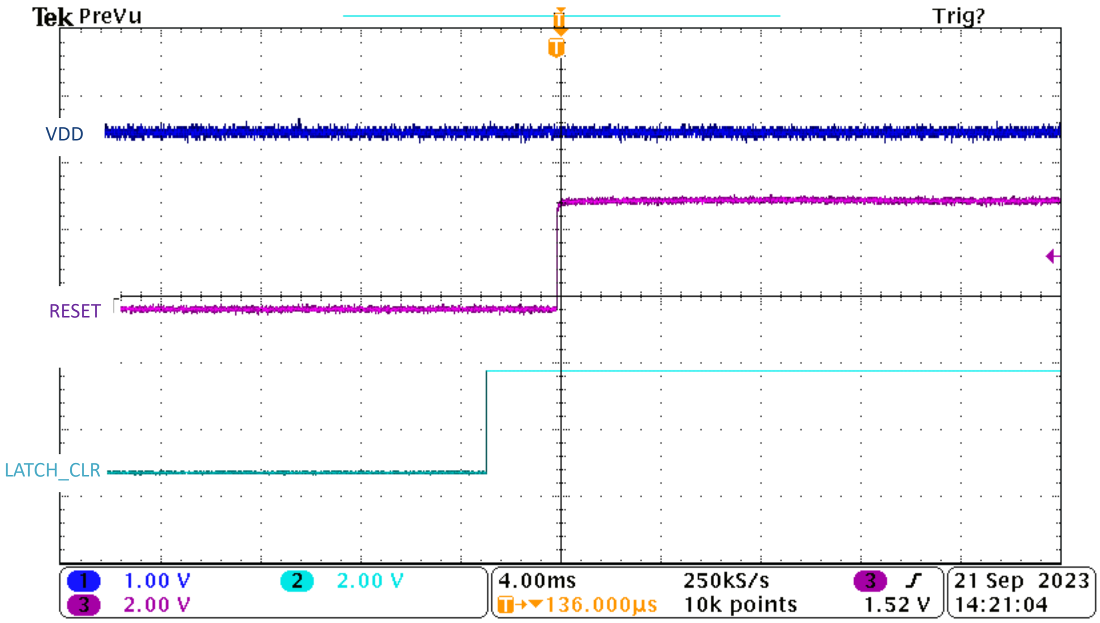


図 11-5. Overvoltage $\overline{\text{RESET}}$ Unlatching Waveform

11.4 Power Supply Recommendations

TPS3762-Q1 is designed to operate from an input supply with a V_{DD} voltage between 2.7V (minimum operation) to 65V (maximum operation). Good analog design practice recommends placing a minimum 0.1µF ceramic capacitor as near as possible to the V_{DD} pin.

11.4.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using 式 10:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \tag{10}$$

The actual power being dissipated in the device can be represented by 式 11:

$$P_D = V_{DD} \times I_{DD} + p_{RESET} \tag{11}$$

p_{RESET} is calculated by 式 12 or 式 13

$$p_{RESET\ (PUSHPULL)} = V_{DD} - V_{RESET} \times I_{RESET} \tag{12}$$

$$p_{RESET\ (OPEN\text{-}DRAIN)} = V_{RESET} \times I_{RESET} \tag{13}$$

式 10 and 式 11 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations must be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be de-rated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by 式 14:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \tag{14}$$

11.5 Layout

11.5.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1µF ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSE pins, placing a 10nF to 100nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces must be greater than 20mils (0.5mm).

- Do not have high voltage metal pads or traces closer than 20 mils (0.5mm) to the low voltage metal pads or traces.

11.5.2 Layout Example

The layout example in 図 11-6 shows how the TPS3762-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.

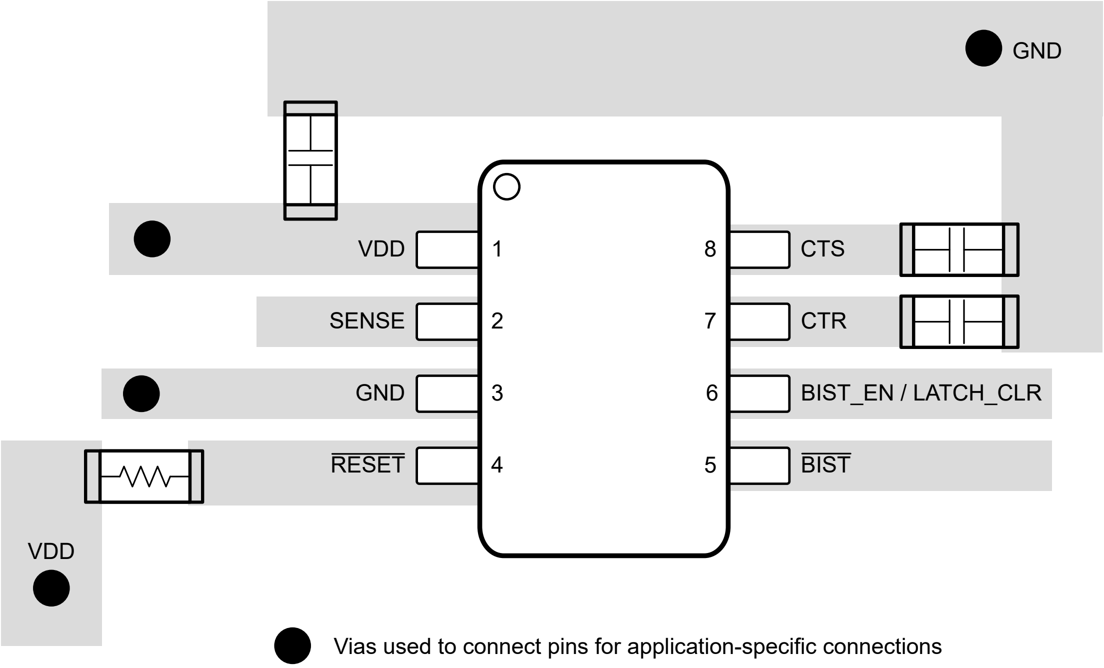


図 11-6. TPS3762-Q1 Recommended Layout

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

12.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2023) to Revision A (May 2024) **Page**

- 量産データのリリース..1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3762D02OVDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62D02
TPS3762D02OVDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62D02
TPS3762D02OVDDFRQ1.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3762-Q1 :

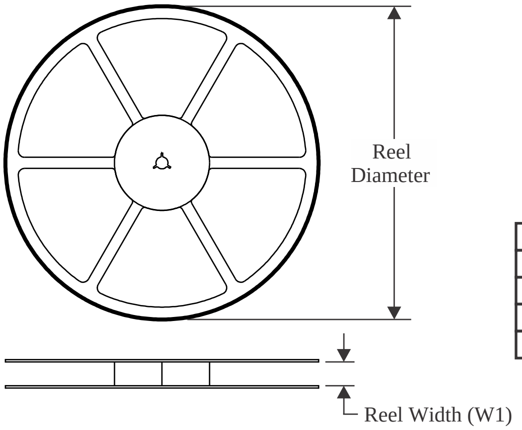
- Catalog : TPS3762

NOTE: Qualified Version Definitions:

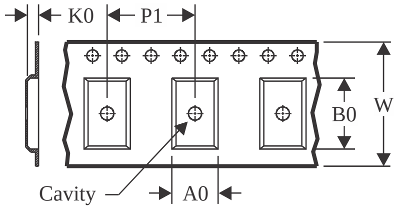
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

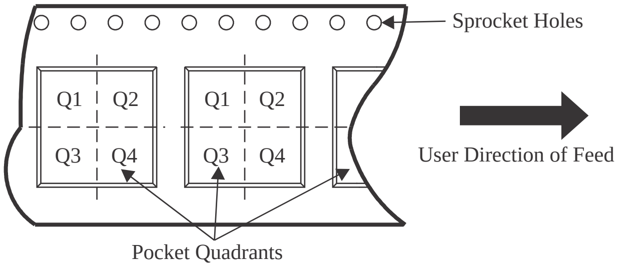


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

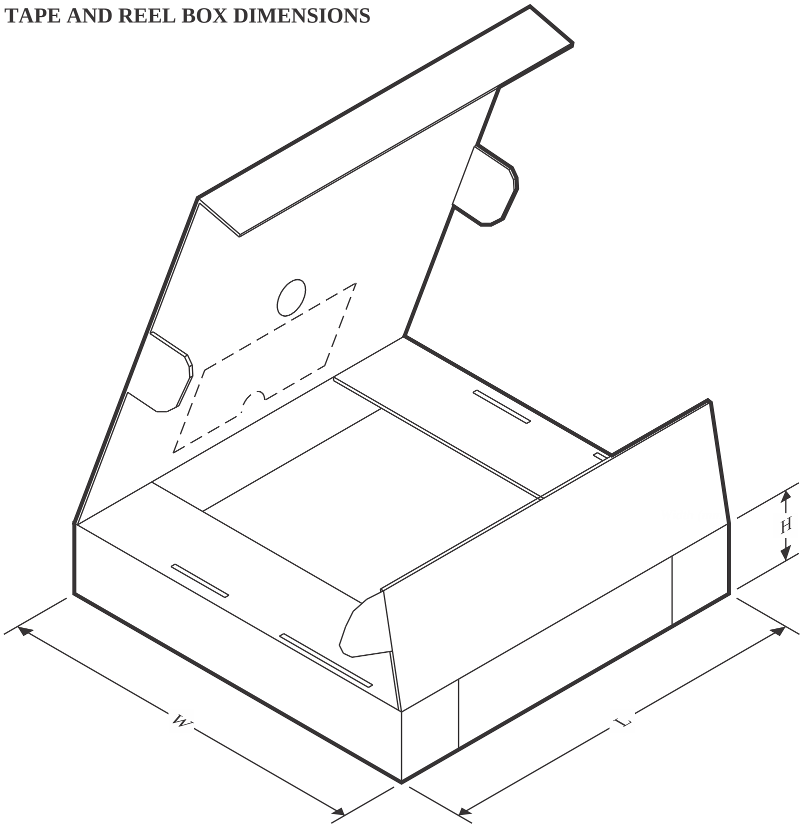
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

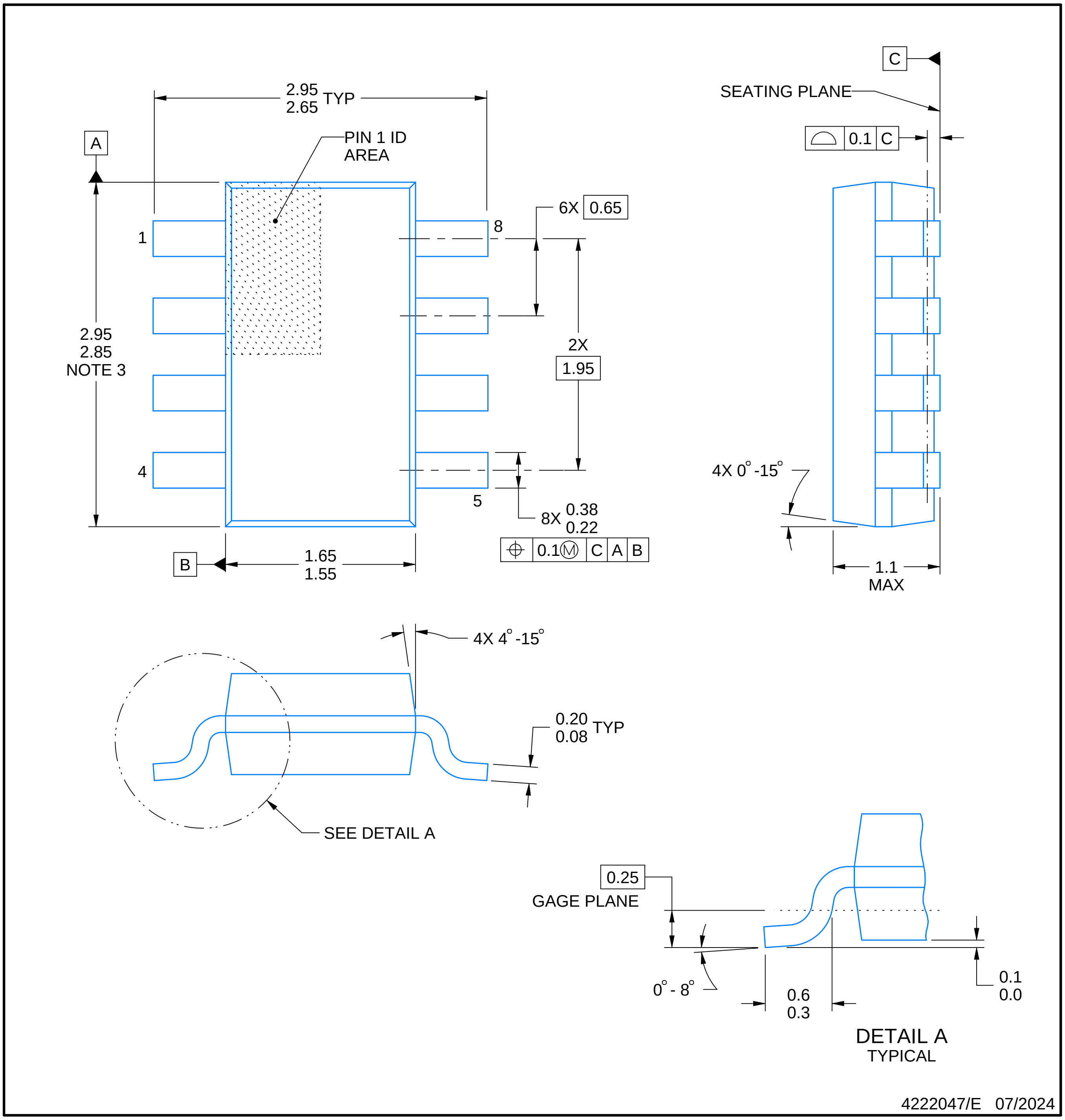
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3762D02OVDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



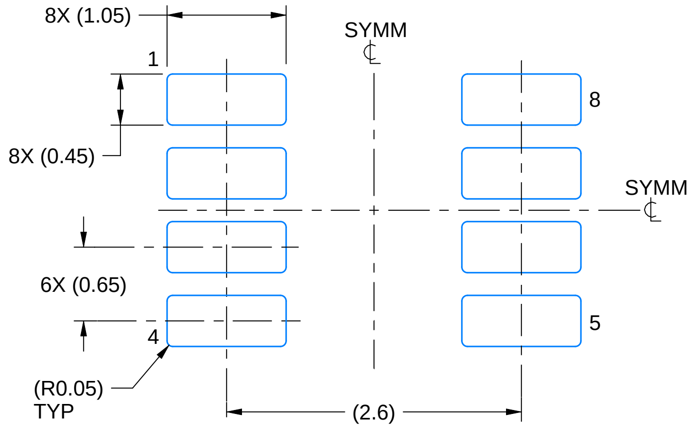
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3762D02OVDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

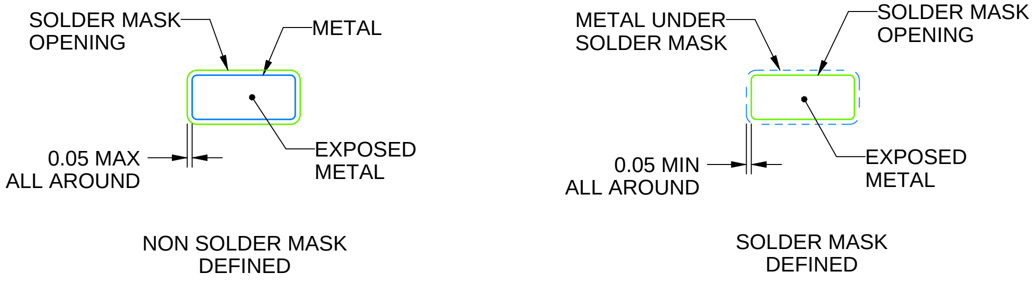


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



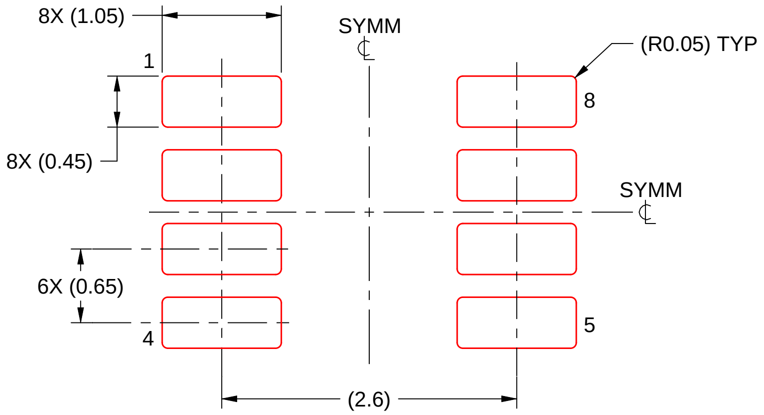
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

最終更新日：2025 年 10 月