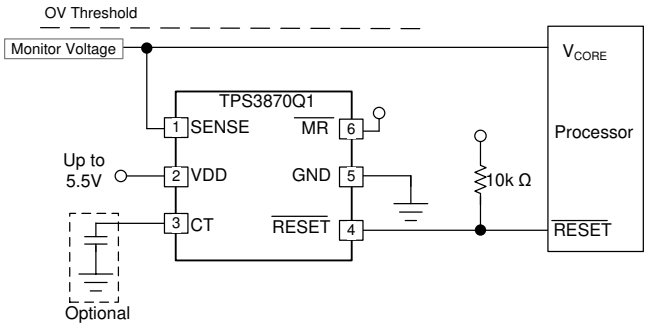
# TPS3870-Q1 時間遅延および手動リセット搭載の過電圧リセット IC

## 1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度 -40°C～+125°C
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C7B
- 入力電圧範囲：1.7V～5.5V
- 低電圧誤動作防止 (UVLO)：1.7V
- 低い静止電流：7µA (最大値)
- スレッショルドの高い精度
  - ± 0.25% (標準値)
  - ± 0.7% (-40°C～+125°C)
- 固定スレッショルド・レベル
  - 50mV 刻みで 500mV～1.3V
  - 1.5V、1.8V、2.5V、2.8V、2.9V、3.3V、5V
- 電圧スレッショルド・レベルをユーザーが変更可能
- 内部的なグリッチ耐性およびヒステリシス
- 3% から 7% まで 1% 刻みの許容値が利用可能
- 固定時間遅延オプション：50µs、1ms、5ms、10ms、20ms、100ms、200ms
- 単一の外付けコンデンサで時間遅延をプログラム可能なオプション
- オープン・ドレイン、アクティブ LOW の OV モニタ
- $\overline{\text{RESET}}$ 電圧のラッチ出力モード

過電圧検出機能を内蔵




## 2 アプリケーション

- 先進運転支援システム (ADAS)
- カメラ
- センサ・フュージョン
- HEV/EV
- FPGA、ASIC、DSP ベースのシステム

## 3 概要

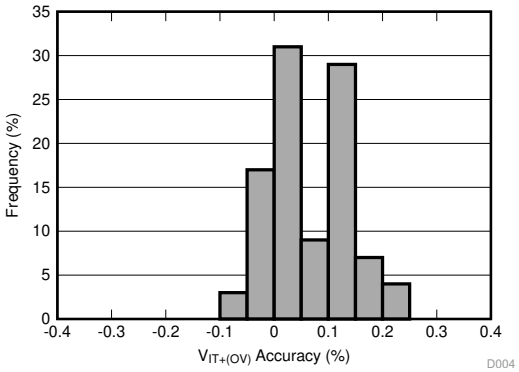
TPS3870-Q1 は統合された過電圧 (OV) モニタまたはリセット IC で、業界でも最も小さい 6 ピンの DSE パッケージに搭載されています。この高精度の電圧スーパーバイザは、低電圧電源レールで動作する、電源誤差の余地が小さいシステムに理想的です。低いスレッショルドのヒステリシスにより、監視対象の電源電圧が通常の動作範囲内であるときに誤ってリセット信号が発生するのを防止します。内部的なグリッチ耐性およびノイズ・フィルタにより、信号エラーによる誤ったリセットも回避されます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| TPS3870-Q1 | WSON (6) | 1.50mm×1.50mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

過電圧精度の標準的な分散



# 目次



## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**2019年7月発行のものから更新** **Page**

- 事前情報を量産データのリリースに ... 1

## 5 概要（続き）

TPS3870-Q1 は、外付け抵抗なしで過電圧リセットのスレッショルドを設定できるため、総合的な精度、コスト、ソリューション・サイズをさらに最適化でき、安全性システムの信頼性も向上します。各デバイスの設計には2つのリセット遅延時間が設定されており、コンデンサ時間(CT)ピンを使用してどちらかを選択できるほか、コンデンサを接続してリセット遅延を調整することもできます。SENSE入力ピンとVDDピンが別になっていることで、高信頼性システムで求められる冗長性を実現できます。

このデバイスは、静止電流仕様がわずか 4.5µA です (標準値)。TPS3870-Q1 は車載用アプリケーションに適しており、AEC-Q100 グレード 1 に認定済みです。

# 6 Device Comparison Table

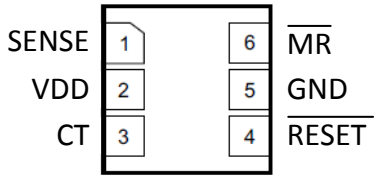
Table 1 shows the released versions of the TPS3870-Q1, including the nominal overvoltage thresholds. For all possible voltages, threshold tolerance, time delays, and threshold options, see 表 6. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

**Table 1. Device Comparison Table**

| PART NUMBER | $V_{MON}$ | TIME DELAY (ms) | | | THRESHOLD TOLERANCE |
|---|---|---|---|---|---|
| | | CT Pin = Capacitor | CT Pin = Open | CT Pin = VDD | |
| TPS3870J4080DSERQ1 | 0.80 V | Programmable | 10 ms | 200 ms | 4% |
| TPS3870J4330DSERQ1 | 3.30 V | Programmable | 10 ms | 200 ms | 4% |

# 7 Pin Configuration and Functions

**DSE Package**
**6-Pin WSON**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | SENSE | I | Input for the monitored supply voltage rail. When the SENSE voltage goes above the overvoltage threshold, the $\overline{\text{RESET}}$ pin is driven low. Connect to VDD pin if monitoring VDD supply voltage. |
| 2 | VDD | I | Supply voltage input pin. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin. |
| 3 | CT | I | Capacitor time delay pin. The CT pin offers two fixed time delays by connecting CT pin to VDD or leaving it floating. Delay time can be programmed by connecting an external capacitor reference to ground. |
| 4 | $\overline{\text{RESET}}$ | O | Active-low, open-drain output. This pin goes low when the SENSE voltage rises above the internally overvoltage threshold ($V_{IT+}$). See the timing diagram in 図 19 for more details. Connect this pin to a pull-up resistor terminated to the desired pull-up voltage. |
| 5 | GND | — | Ground |
| 6 | $\overline{\text{MR}}$ | I | Manual reset (MR), pull this pin to a logic low ($V_{\overline{MR}\_L}$) to assert a reset signal . After the $\overline{\text{MR}}$ pin is deasserted the output goes high after the reset delay time($t_D$) expires. $\overline{\text{MR}}$ can be left floating when not in use. |

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{DD}$ | –0.3 | 6 | V |
| Voltage | $V_{\overline{RESET}}$ | –0.3 | 6 | V |
| Voltage | $V_{CT}$ | –0.3 | 6 | V |
| Voltage | $V_{SENSE}$ | –0.3 | 6 | V |
| Voltage | $V_{\overline{MR}}$ | –0.3 | 6 | V |
| Current | $I_{\overline{RESET}}$ | | ±40 | mA |
| Temperature (2) | Continuous total power dissipation | See the Thermal Information | | |
| | Operating junction temperature, $T_J$ | -40 | 150 | °C |
| | Operating free-air temperature, $T_A$ | -40 | 150 | °C |
| | Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

## 8.2 ESD ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

## 8.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply pin voltage | 1.7 | | 5.5 | V |
| $V_{SENSE}$ | Input pin voltage | 0 | | 5.5 | V |
| $V_{CT}$ | CT pin voltage (1) (2) | | | $V_{DD}$ | V |
| $V_{\overline{RESET}}$ | Output pin voltage | 0 | | 5.5 | V |
| $V_{\overline{MR}}$ | $\overline{MR}$ pin Voltage (3) | 0 | | 5.5 | V |
| $I_{\overline{RESET}}$ | Output pin current | 0.3 | | 10 | mA |
| $T_J$ | Junction temperature (free-air temperature) | -40 | | 125 | ℃ |

(1) CT pin connected to VDD pin requires a pullup resistor; 10 kΩ is recommended.
(2) The maximum rating is $V_{DD}$ or 5.5 V, whichever is smaller.
(3) If the logic signal driving $\overline{MR}$ is less than $V_{DD}$, then additional current flows into $V_{DD}$ and out of $\overline{MR}$.

## 8.4 Thermal Information

| THERMAL METRIC(1) | | TPS3870-Q1 DSE (WSON) PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 184.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 30.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 86.4 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 13.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 86.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 8.5 Electrical Characteristics

At 1.7 V ≤ $V_{DD}$ ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to $V_{DD}$, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at $V_{DD}$ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 1.7 | | 5.5 | V |
| UVLO | Under Voltage Lockout(1) | $V_{DD}$ falling below 1.7 V | 1.2 | | 1.7 | V |
| $V_{POR}$ | Power on reset voltage(2) | $V_{OL}$(max) = 0.25 V, $I_{OUT}$ = 15 µA | | | 1 | V |
| $V_{IT+(OV)}$ | Positive- going threshold accuracy | | -0.7 | ±0.25 | 0.7 | % |
| $V_{HYS}$ | Hysteresis Voltage(3) | | 0.3 | 0.55 | 0.8 | % |
| $I_{DD}$ | Supply current | $V_{DD}$ ≤ 5.5 V | | 4.5 | 7 | µA |
| $I_{SENSE}$ | Input current, SENSE pin | $V_{SENSE}$ = 5 V | | 1 | 1.5 | µA |
| $V_{OL}$ | Low level output voltage | $V_{DD}$ = 1.7 V, $I_{OUT}$ = 0.4 mA | | | 250 | mV |
| | | $V_{DD}$ = 2 V, $I_{OUT}$ = 3 mA | | | 250 | mV |
| | | $V_{DD}$ = 5 V, $I_{OUT}$ = 5 mA | | | 250 | mV |
| $I_{LKG}$ | Open drain output leakage current | $V_{DD}$ = $V_{\overline{RESET}}$ = 5.5 V | | | 300 | nA |
| $V_{\overline{MR}\_L}$ | $\overline{MR}$ logic low input | | | | 0.3 | V |
| $V_{\overline{MR}\_H}$ | $\overline{MR}$ logic high input | | 1.4 | | | V |
| $V_{CT\_H}$ | High level CT pin voltage | | 1.4 | | | V |
| $R_{\overline{MR}}$ | Manual reset Internal pullup resistance | | | 100 | | KΩ |
| $I_{CT}$ | CT pin charge current | | 337 | 375 | 413 | nA |
| $V_{CT}$ | CT pin comparator threshold voltage(4) | | 1.133 | 1.15 | 1.167 | V |

(1) $\overline{RESET}$ pin is driven low when $V_{DD}$ falls below UVLO.
(2) $V_{POR}$ is the minimum $V_{DD}$ voltage level for a controlled output state.
(3) Hysteresis is with respect of the trip point ($V_{IT+(OV)}$)
(4) $V_{CT}$ voltage refers to the comparator threshold voltage that measures the voltage level of the external capacitor at CT pin.

## 8.6 Timing Requirements

At 1.7 V ≤ $V_{DD}$ ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to $V_{DD}$, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at $V_{DD}$ = 3.3 V.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_D$ | Reset time delay, TPS3870J | CT = Open | 7 | 10 | 13 | ms |
| $t_D$ | Reset time delay, TPS3870J | CT = 10 kΩ to $V_{DD}$ | 140 | 200 | 260 | ms |
| $t_D$ | Reset time delay, TPS3870K | CT = Open | 0.7 | 1 | 1.3 | ms |
| $t_D$ | Reset time delay, TPS3870K | CT = 10 kΩ to $V_{DD}$ | 14 | 20 | 26 | ms |
| $t_D$ | Reset time delay, TPS3870L | CT = Open | 3.5 | 5 | 6.5 | ms |
| $t_D$ | Reset time delay, TPS3870L | CT = 10 kΩ to $V_{DD}$ | 70 | 100 | 130 | ms |

## Timing Requirements (continued)

At 1.7 V ≤ $V_{DD}$ ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to $V_{DD}$, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at $V_{DD}$ = 3.3 V.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_D$ | Reset time delay, TPS3870M | CT = 10 kΩ to $V_{DD}$<br>CT = Open | | 50 | | µs |
| $t_{PD}$ | Propagation detect delay(1)(2) | | | 15 | 30 | µs |
| $t_R$ | Output rise time(1)(3) | | | 2.2 | | µs |
| $t_F$ | Output fall time(1)(3) | | | 0.2 | | µs |
| $t_{SD}$ | Startup delay(4) | | | 300 | | µs |
| $t_{GI\ (VIT+)}$ | Glitch Immunity overvoltage $V_{IT+(OV)}$, 5% Overdrive(1) | | | 3.5 | | µs |
| $t_{GI\ (\overline{MR})}$ | Glitch Immunity $\overline{MR}$ pin | | | | 25 | ns |
| $t_{PD\ (\overline{MR})}$ | Propagation delay from $\overline{MR}$ low to assert $\overline{RESET}$ | | | 500 | | ns |
| $t_{\overline{MR}\_W}$ | $\overline{MR}$ pin pulse width duration to assert $\overline{RESET}$ | | 1 | | | µs |
| $t_{D\ (\overline{MR})}$ | $\overline{MR}$ reset time delay | | | $t_D$ | | ms |

(1) 5% Overdrive from threshold. Overdrive % = [$V_{SENSE}$ - $V_{IT+(OV)}$] / $V_{IT+(OV)}$
(2) $t_{PD}$ measured from threshold trip point $V_{IT+(OV)}$ to $\overline{RESET}$ $V_{OL}$ voltage
(3) Output transitions from $V_{OL}$ to 90% for rise times and 90% to $V_{OL}$ for fall times.
(4) During the power-on sequence, $V_{DD}$ must be at or above $V_{DD\ (MIN)}$ for at least $t_{SD}$ + $t_D$ before the output is in the correct state.

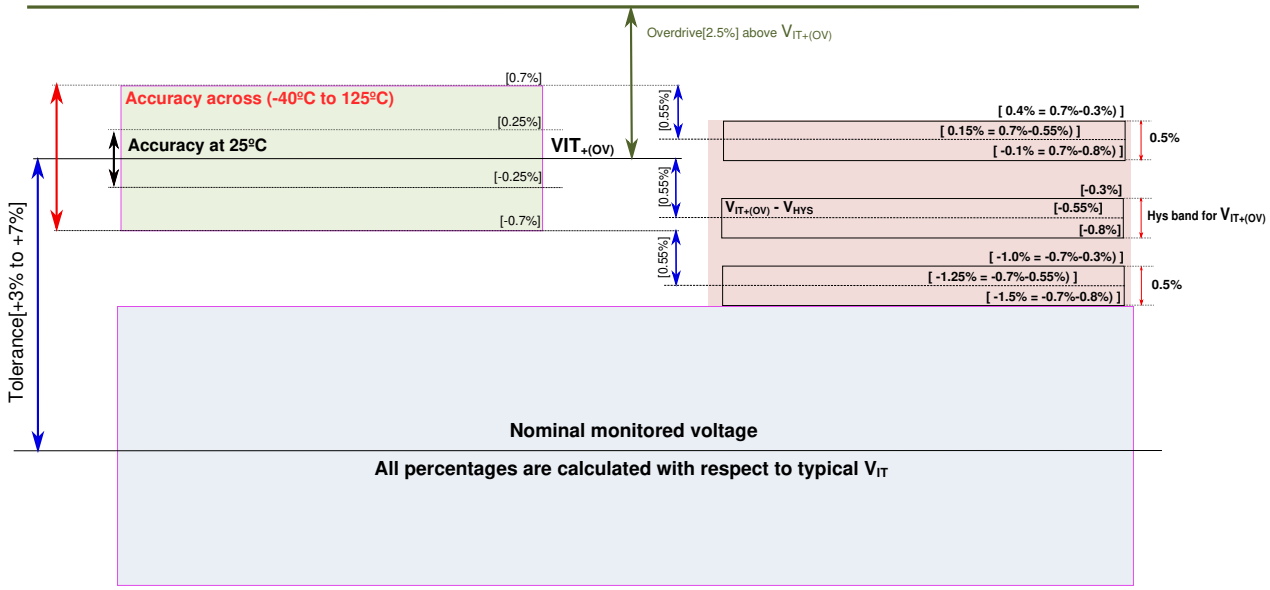
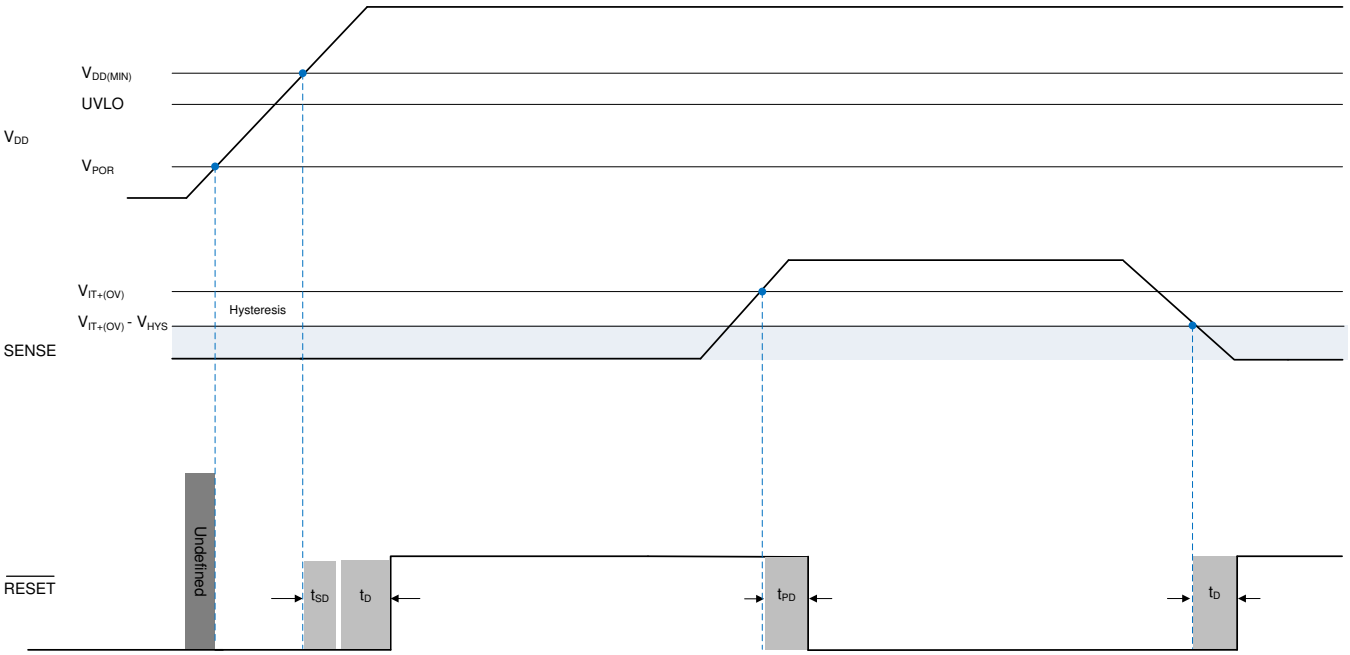



**図 1. Voltage Threshold and Hysteresis Accuracy**



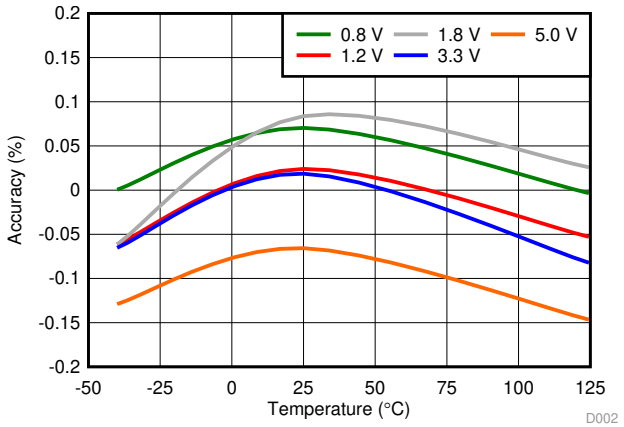

(1) $V_{DD}$ = 2 V, $R_{PU}$ = 10 kΩ to $V_{DD}$

(2) Variant M (time delay bypass) has a ~40 µs pulse at $\overline{\text{RESET}}$ pin during power up window, this is present only when the power cycle off time is longer than 10 seconds, this behavior will not occur if SENSE pin is within window of operation during $V_{DD}$ power up.

**図 2. SENSE Timing Diagram**

## 8.7 Typical Characteristics

At $T_J$ = 25°C, $V_{DD}$ = 3.3 V, and $R_{PU}$ = 10 kΩ, unless otherwise noted.




Tested across multiple voltage options

**図 3. Overvoltage Accuracy vs Temperature**

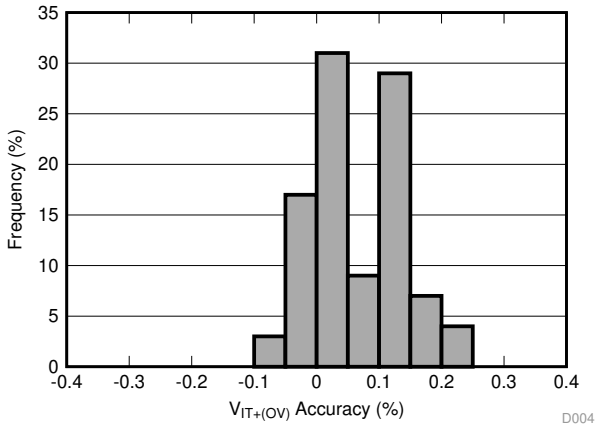
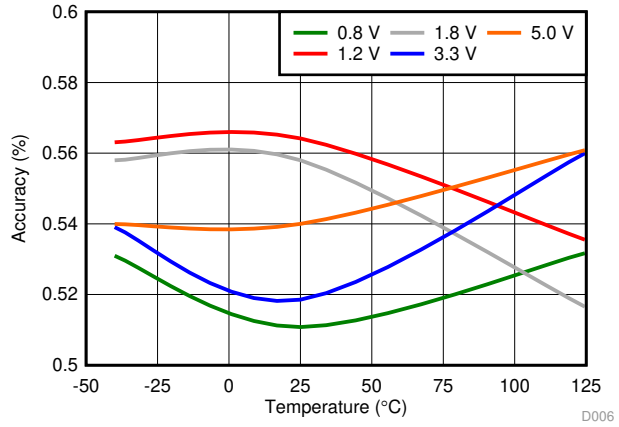
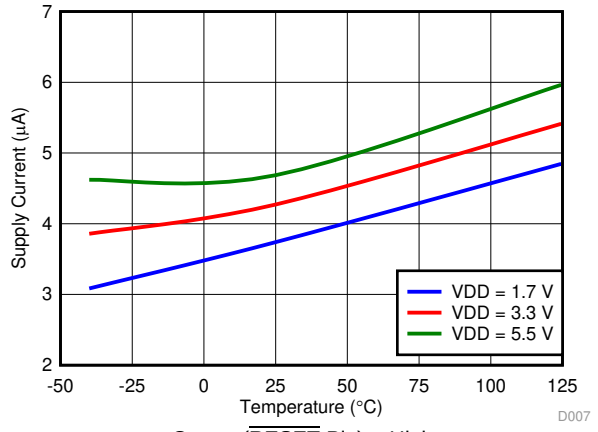



**図 4. Overvoltage Accuracy Distribution**



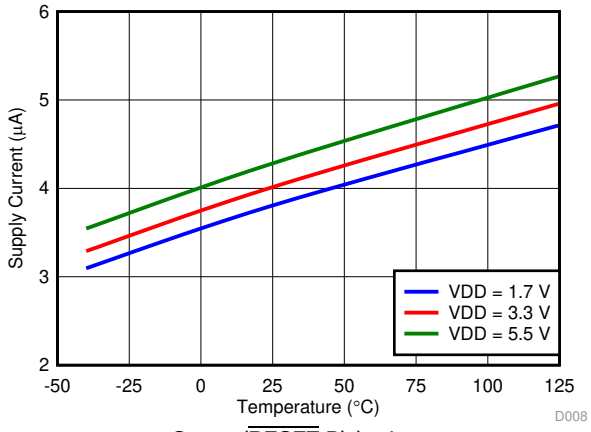

Tested across multiple voltage options

**図 5. Overvoltage Hysteresis Voltage Accuracy vs Temperature**



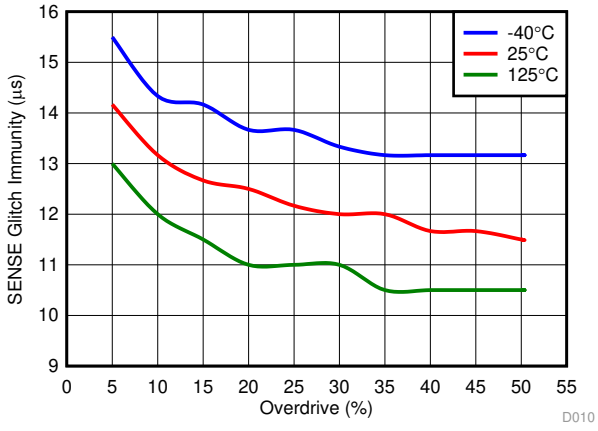

Output ($\overline{\text{RESET}}$ Pin) = High

**図 6. Supply Current vs Temperature**




Output ($\overline{\text{RESET}}$ Pin) = Low

**図 7. Supply Current vs Temperature**

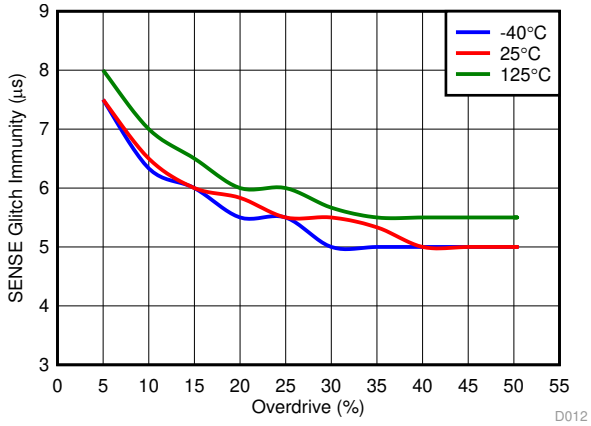



VDD = 1.7 V

**図 8. SENSE Glitch Immunity (VIT+) vs Overdrive**

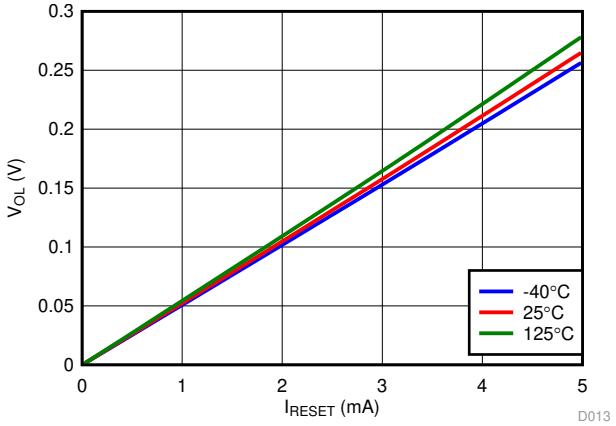
## Typical Characteristics (continued)

At $T_J$ = 25°C, $V_{DD}$ = 3.3 V, and $R_{PU}$ = 10 kΩ, unless otherwise noted.



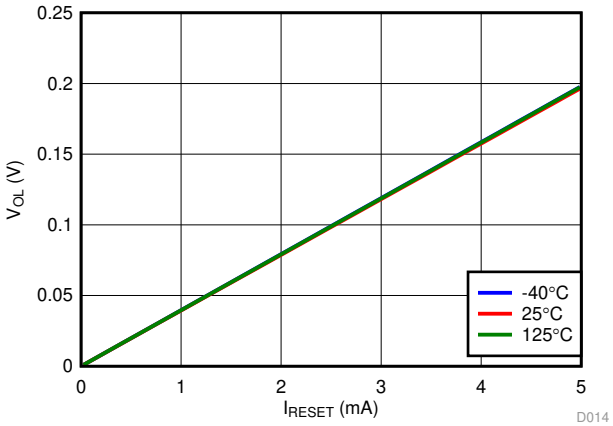

VDD = 5.5 V

**図 9. SENSE Glitch Immunity (VIT+) vs Overdrive**



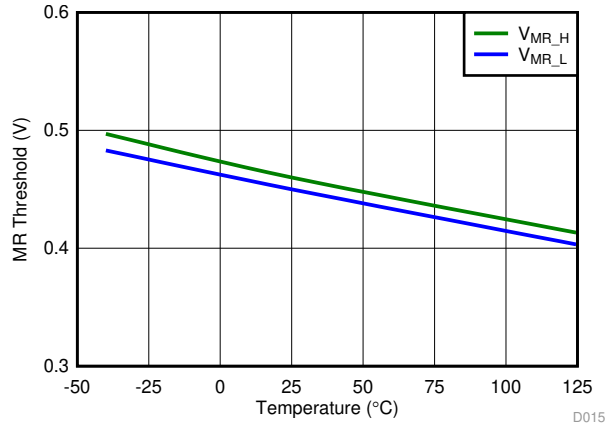

VDD = 1.7 V

**図 10. Low-Level Output Voltage vs RESET current**



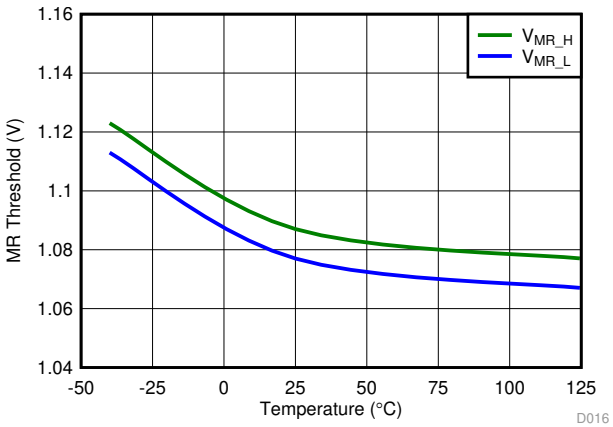

VDD = 5.5 V

**図 11. Low-Level Output Voltage vs RESET current**




VDD = 1.7 V

**図 12. SET Threshold vs Temperature**




VDD = 5.5 V

**図 13. SET Threshold vs Temperature**

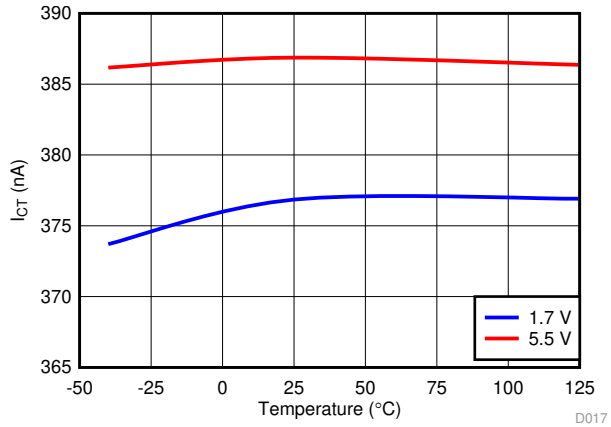



**図 14. CT Current vs CT value**

## Typical Characteristics (continued)

At $T_J$ = 25°C, $V_{DD}$ = 3.3 V, and $R_{PU}$ = 10 kΩ, unless otherwise noted.

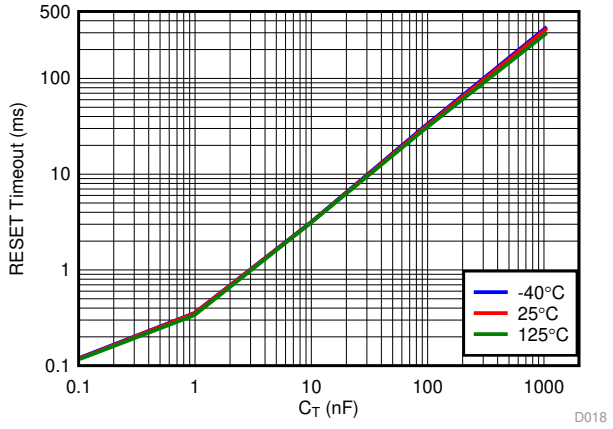



図 15. $\overline{\text{RESET}}$ Timeout vs CT Capacitor

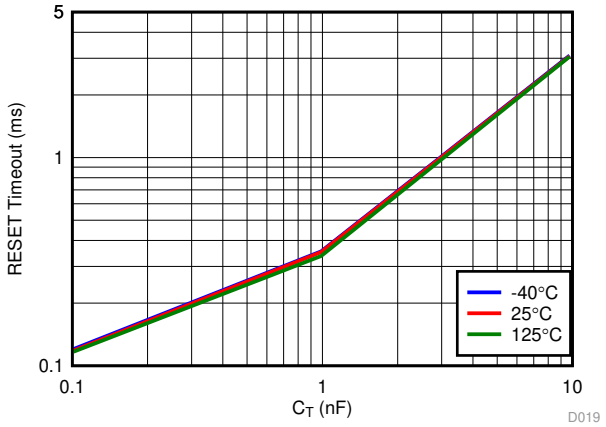



図 16. Timeout vs CT Capacitor (0.1 to 10 nF)

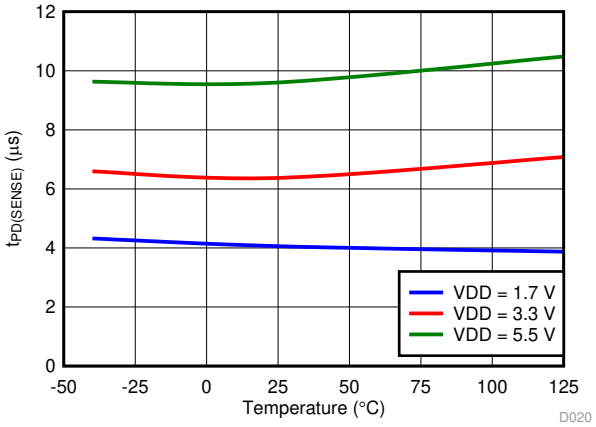



図 17. Detect Propagation Delay vs Temperature

# 9 Detailed Description

## 9.1 Overview

The TPS3870-Q1 family of devices uses a voltage comparator and a precision voltage reference for overvoltage detection. The TPS3870-Q1 features a highly accurate threshold voltage (±0.7% over temperature) and a variety of voltage threshold variants.

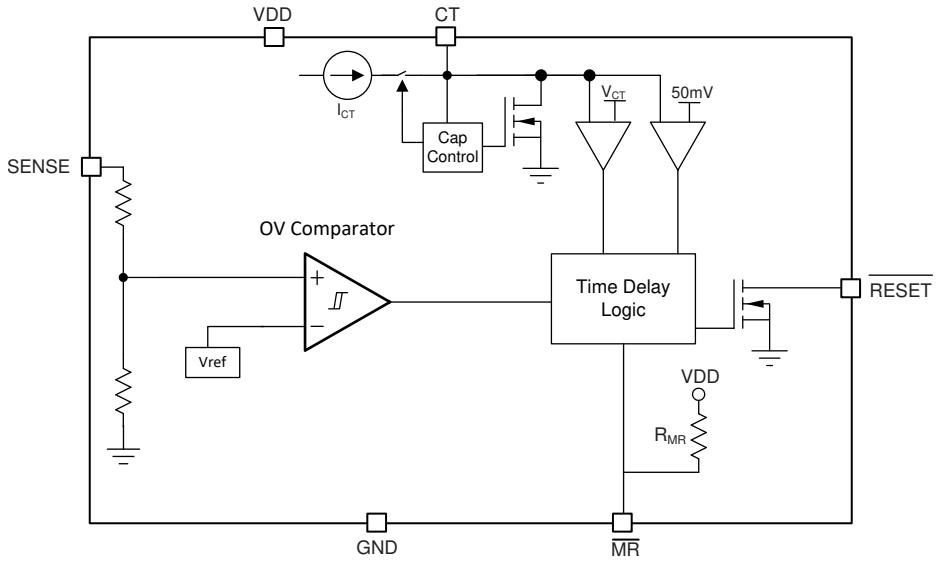
The TPS3870-Q1 includes the resistors used to set the overvoltage threshold internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

TPS3870-Q1 versions J, K and L have three time delay settings, two fixed by connecting CT pin to VDD through a resistor and leaving CT floating and a programmable time delay setting that only requires a single capacitor connected from CT pin to ground.

Manual Reset ($\overline{MR}$) allows for sequencing or hard reset by driving the $\overline{MR}$ pin below $V_{\overline{MR}\_L}$.

The TPS3870-Q1 is designed to assert active low output signals when the monitored voltage is outside the safe window. The relationship between the monitored voltage and the states of the outputs is shown in 表 2.

## 9.2 Functional Block Diagram




*For all possible voltages, threshold tolerance, time delays, and threshold options, see 表 6.

## 9.3 Feature Description

### 9.3.1 VDD

The TPS3870-Q1 is designed to operate from an input voltage supply range between 1.7 V to 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 1-µF capacitor between the VDD pin and the GND pin.

$V_{DD}$ needs to be at or above $V_{DD(MIN)}$ for at least the start-up delay ($t_{SD}$+ $t_D$) for the device to be fully functional.

### 9.3.2 SENSE

The TPS3870-Q1 uses a comparator with a precision reference voltage and a trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. The comparator also includes built-in hysteresis that provides noise immunity and ensures stable operation.

## Feature Description (continued)

Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE input in order to reduce sensitivity to transient voltages on the monitored signal.

When monitoring VDD supply voltage, the SENSE pin can be connected directly to VDD. The output ($\overline{\text{RESET}}$) is high impedance when voltage at the SENSE pin is lower than the upper boundary of the threshold.

### 9.3.3 $\overline{\text{RESET}}$

In a typical TPS3870-Q1 application, the $\overline{\text{RESET}}$ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the enable input of a voltage regulator [such as a DC-DC converter or low-dropout regulator (LDO)].

The TPS3870-Q1 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by $V_{OL}$, output capacitive loading, and output leakage current. These values are specified in *Specifications*. The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS3870-Q1 $\overline{\text{RESET}}$ pin.

表 2 describes the scenarios when the output ($\overline{\text{RESET}}$) is either asserted low or high impedance.

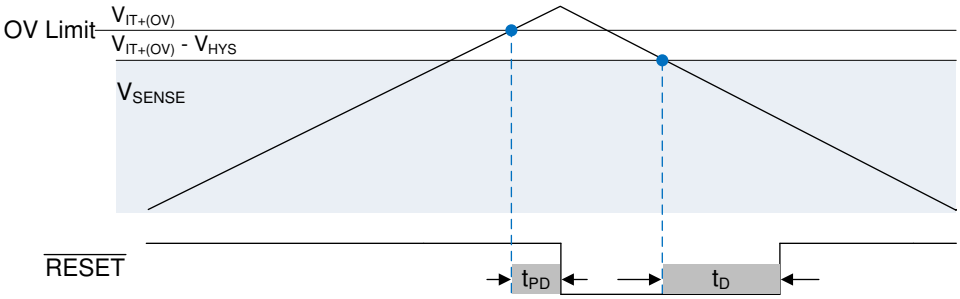



**図 18. RESET output**

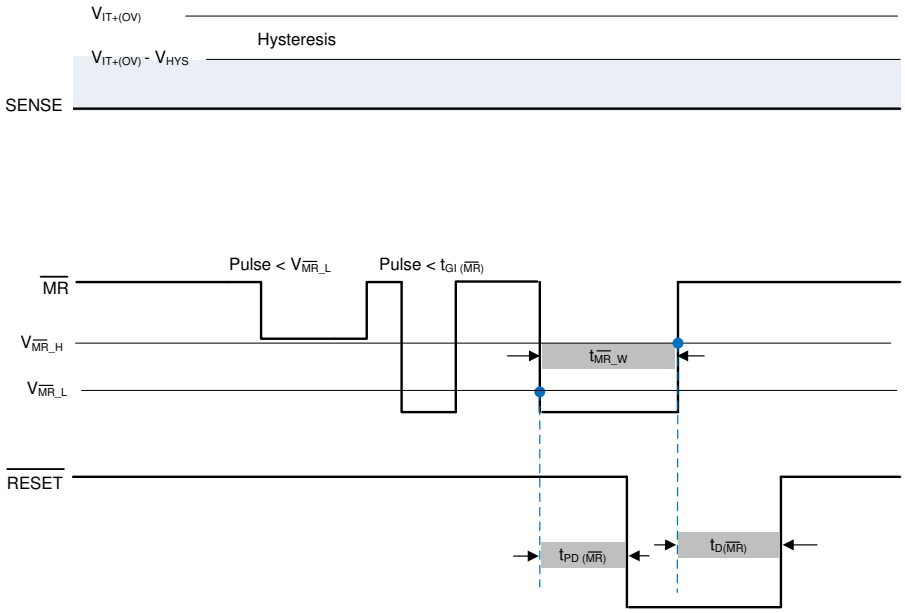
### 9.3.4 Capacitor Time (CT)

The CT pin provides the user the functionality of both high-precision, factory-programmed, reset delay timing options and user-programmable, reset delay timing. The CT pin can be pulled up to $V_{DD}$ through a resistor, have an external capacitor to ground, or can be left unconnected. The configuration of the CT pin is re-evaluated by the device every time the voltage on the SENSE line enters the valid window ($V_{SENSE} < V_{IT+(OV)}$). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CT pin. The sequence of events takes 450 µs to determine if the CT pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CT pin is being pulled up to $V_{DD}$, then a pull-up resistor is required, 10 kΩ is recommended.

### 9.3.5 Manual Reset ($\overline{\text{MR}}$)

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and the SENSE pin voltage is within a valid condition ($V_{SENSE} < V_{IT+(OV)}$) , $\overline{\text{RESET}}$ is deasserted after the reset delay time ($t_D$). If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ can either be connected to $V_{DD}$ or left floating because the $\overline{\text{MR}}$ pin is internally pulled up to $V_{DD}$. Figure 図 19 shows the relation between $\overline{\text{MR}}$ and $\overline{\text{RESET}}$.

## Feature Description (continued)




(1) $\overline{RESET}$ pulls up to VDD with 10 kΩ.

(2) To initiate and continue time reset counter both conditions must be met $\overline{MR}$ pin above $V_{\overline{MR}\_H}$ or floating and $V_{SENSE}$ below $V_{IT+(OV)}$ - $V_{HYS}$

(3) $\overline{MR}$ is ignored during output $\overline{RESET}$ low event

**図 19. Manual Reset Timing Diagram**

## 9.4 Device Functional Modes

**表 2. Functional Mode Truth Table**

| DESCRIPTION | CONDITION | $\overline{MR}$ PIN | VDD PIN | OUTPUT ($\overline{RESET}$ PIN) |
|---|---|---|---|---|
| Normal Operation | SENSE < $V_{IT+(OV)}$ | Open or above $V_{\overline{MR}\_H}$ | $V_{DD}$ > $V_{DD(MIN)}$ | High |
| Over Voltage detection | SENSE > $V_{IT+(OV)}$ | Open or above $V_{\overline{MR}\_H}$ | $V_{DD}$ > $V_{DD(MIN)}$ | Low |
| Manual reset | SENSE < $V_{IT+(OV)}$ | Below $V_{\overline{MR}\_L}$ | $V_{DD}$ > $V_{DD(MIN)}$ | Low |
| UVLO engaged | SENSE < $V_{IT+(OV)}$ | Open or above $V_{\overline{MR}\_H}$ | $V_{POR}$ < $V_{DD}$ < UVLO | Low |

### 9.4.1 Normal Operation ($V_{DD}$ > $V_{DD(MIN)}$)

When the voltage on $V_{DD}$ is greater than $V_{DD(MIN)}$ for approximately ($t_{SD}$+ $t_D$), the $\overline{RESET}$ output state will correspond to the SENSE pin voltage with respect to the threshold limits, when SENSE voltage is outside of threshold limits the $\overline{RESET}$ voltage will be low ($V_{OL}$).

### 9.4.2 Undervoltage Lockout ($V_{POR}$ < $V_{DD}$ < UVLO)

When the voltage on $V_{DD}$ is less than the device UVLO voltage but greater than the power-on reset voltage ($V_{POR}$), the $\overline{RESET}$ pin will be held low , regardless of the voltage on SENSE pin.

### 9.4.3 Power-On Reset ($V_{DD}$ < $V_{POR}$)

When the voltage on $V_{DD}$ is lower than the required voltage ($V_{POR}$) to internally pull the asserted output to GND, $\overline{RESET}$ signal is undefined and is not to be relied upon for proper device function.

# 10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

### 10.1.1 Voltage Threshold Accuracy

Voltage monitoring requirements vary depending on the voltage supply tolerance of the device being powered. Due to the high precision of the TPS3870-Q1 (±0.7% Max), the device allows for a wider supply voltage margins and threshold headroom for tight tolerance applications.

For example, take a DC/DC regulator providing power to a core voltage rail of an MCU. The MCU has a tolerance of ±5% of the nominal output voltage of the DC/DC. The user sets an ideal voltage threshold of 4% which allows for ±1% of threshold accuracy. Since the TPS3870-Q1 threshold accuracy is higher than ±1%, the user has more supply voltage margin which can allow for a relaxed power supply design. This gives flexibility to the DC/DC to use a smaller output capacitor or inductor because of a larger voltage window for voltage ripple and transients. There is also headroom between the minimum system voltage and voltage tolerance of the MCU to ensure that the voltage supply will never be in the region of potential failure of malfunction without the TPS3870-Q1 asserting a reset signal.

図 20 illustrates the supply overvoltage margin and accuracy of the TPS3870-Q1 for the example explained above. Using a low accuracy supervisor will eat into the available budget for the power supply ripple and transient response. This gives less flexibility to the user and a more stringent DC/DC converter design.

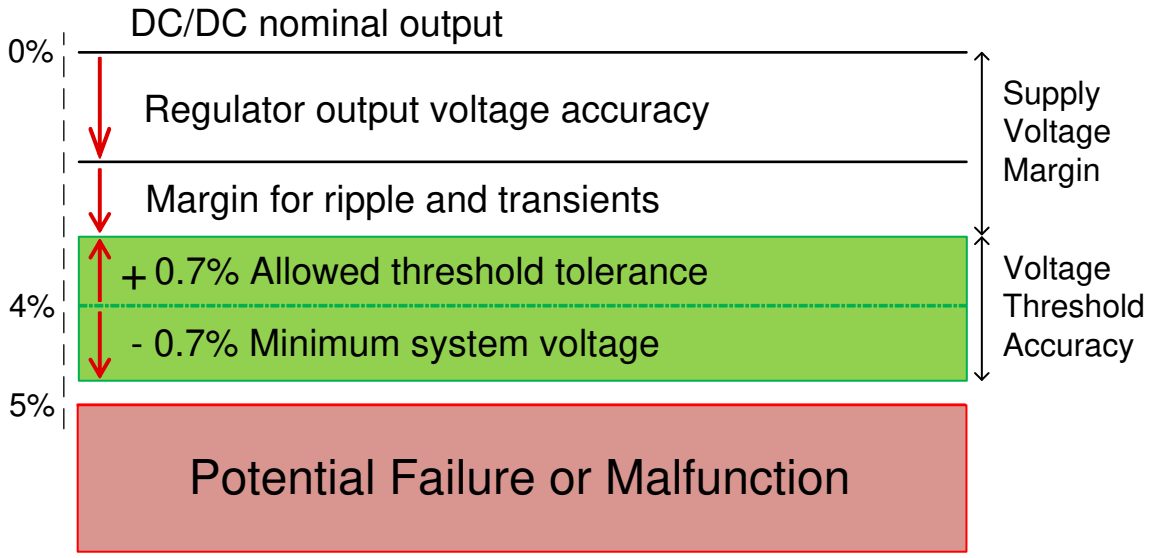



**図 20. TPS3870-Q1 Voltage Threshold Accuracy**

## Application Information (continued)

### 10.1.2 CT Reset Time Delay

The TPS3870-Q1 features three options for setting the reset delay ($t_D$): connecting a capacitor to the CT pin, connecting a pull-up resistor to VDD, and leaving the CT pin unconnected. 図 21 shows a schematic drawing of all three options. To determine which option is connected to the CT pin, an internal state machine controls the internal pulldown device and measures the pin voltage. This sequence of events takes 450 µs to determine which timing option is used. Every time the voltage on the SENSE line enters the valid window ($V_{SENSE} < V_{IT+(OV)} - V_{HYS}$, the state machine determines the CT option.

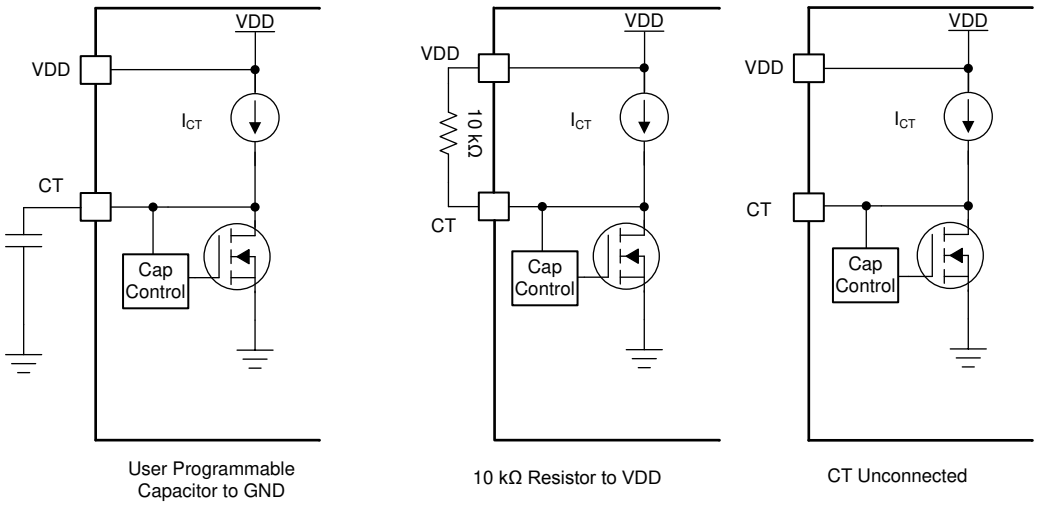



**図 21. CT Charging Circuit**

#### *10.1.2.1 Factory-Programmed Reset Delay Timing*

To use the factory-programmed timing options, the CT pin must either be left unconnected or pulled up to VDD through a 10 kΩ pull-up resistor. Using these options enables a high-precision reset delay timing, as shown in 表 3.

**表 3. Reset Delay Time for Factory-Programmed Reset Delay Timing**

| VARIANT | $\overline{\text{RESET}}$ DELAY TIME ($t_D$) | | | VALUE |
|---|---|---|---|---|
| | CT = Capacitor to GND | CT = Floating | CT = 10 kΩ to VDD | |
| TPS3870J | Programmable $t_D$ | 10 | 200 | ms |
| TPS3870K | Programmable $t_D$ | 1 | 20 | ms |
| TPS3870L | Programmable $t_D$ | 5 | 100 | ms |
| TPS3870M | N/A | 50 | 50 | µs |

#### *10.1.2.2 Programmable Reset Delay-Timing*

The TPS3870 reset time delay is based on internal current source ($I_{CT}$) to charge external capacitor ($C_{CT}$) and read capacitor voltage with the internal comparator. The minimum value capacitor is 250 pF. There is no limitation on maximum capacitor the only constrain is imposed by the initial voltage of the capacitor, if CT cap is zero or near to zero then ideally there is no other constraint on the max capacitor. The typical ideal capacitor value needed for a given delay time can be calculated using 式 1, where $C_{CT}$ is in nanofarads (nF) and $t_D$ is in ms:

$$t_D = 3.066 \times C_{CT} + 0.5 \text{ ms} \quad (1)$$

To calculate the minimum and maximum-reset delay time use 式 2 and 式 3, respectively.

$$t_{D(min)} = 2.7427 \times C_{CT} + 0.3 \text{ ms} \quad (2)$$

$$t_{D(max)} = 3.4636 \times C_{CT} + 0.7 \text{ ms} \quad (3)$$

The slope of the equation is determined by the time the CT charging current ($I_{CT}$) takes to charge the external capacitor up to the CT comparator threshold voltage ($V_{CT}$). When $\overline{\text{RESET}}$ is asserted, the capacitor is discharged through the internal CT pulldown resistor. When the $\overline{\text{RESET}}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor; when $V_{CT}$ = 1.15 V, $\overline{\text{RESET}}$ is unasserted. Note that in order to minimize the difference between the calculated $\overline{\text{RESET}}$ delay time and the actual $\overline{\text{RESET}}$ delay time, use a use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. 表 4 lists the reset delay time ideal capacitor values for $C_{CT}$.

**表 4. Reset Delay Time for Ideal Capacitor Values**

| $C_{CT}$ | $\overline{\text{RESET}}$ DELAY TIME ($t_D$), TYPICAL |
|---|---|
| 250 pF | 1.27 ms |
| 1 nF | 3.57 ms |
| 3.26 nF | 10.5 ms |
| 32.6 nF | 100.45 ms |
| 65.2 nF | 200.40 ms |
| 1uF | 3066.50 ms |

### 10.1.3 $\overline{\text{RESET}}$ Latch Mode

The TPS3870-Q1 features a voltage latch mode on the $\overline{\text{RESET}}$ pin when connecting the CT pin to common ground . A pull-down resistor is recommended to limit current consumption of the system. In latch mode, if the $\overline{\text{RESET}}$ pin is low or triggers low, the pin will stay low regardless if $V_{SENSE}$ is within the acceptable voltage boundaries ($V_{SENSE}$ < $V_{IT+(OV)}$). To unlatch the device provide a voltage to the CT pin that is greater than the CT pin comparator threshold voltage, $V_{CT}$. The $\overline{\text{RESET}}$ pin will trigger high instantaneously without any reset delay. A voltage greater than 1.2 V to recommended to ensure a proper unlatch. Use a series resistance to limit current when an unlatch voltage is applied. For more information, Design 1: $\overline{\text{RESET}}$ Latch Mode gives an example of a typical latch application.

**注**

At power up, the TPS3870-Q1 will be latched when CT is connected to GND. To ensure correct power up when using $\overline{\text{RESET}}$ latch mode, send a pulse to the CT pin greater than 1.2 V after $t_{SD}$ and SENSE is within the correct window of operation.

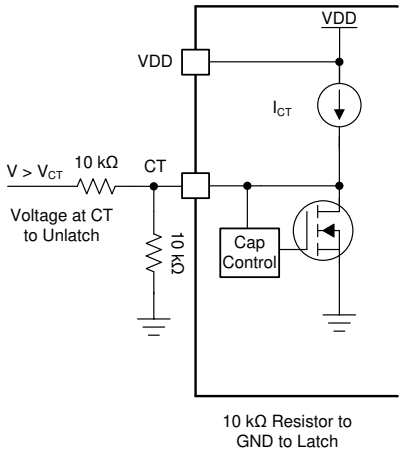



**図 22. $\overline{\text{RESET}}$ Latch Circuit**

### 10.1.4 Adjustable Voltage Thresholds

The TPS3870-Q1 0.7% maximum accuracy allows for adjustable voltage thresholds using external resistors without adding major inaccuracies to the device. In case that the desired monitored voltage is not available, external resistor dividers can be used to set the desired voltage thresholds. 図 23 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8V voltage threshold device such as the TPS3870J4080 because of the bypass mode of internal resistor ladder.

For example, consider a 2.0 V rail being monitored ($V_{MON}$) using the TPS3870J4080 variant. Using 式 4, R1 = 15 kΩ given that R2 = 10 kΩ, $V_{MON}$ = 2 V , and $V_{SENSE}$ = 0.8 V. This device is typically meant to monitor a 0.8 V rail with a +4% voltage threshold. This means that the device overvoltage threshold ($V_{IT+(OV)}$) is 0.832 V. Using 式 4, the monitored overvoltage threshold ($V_{MON+}$) = 2.08 V when $V_{SENSE}$ = $V_{IT+(OV)}$. If a wider tolerance threshold is desired, use a device variant shown on 表 6 to determine what device part number matches your application.

$$V_{SENSE} = V_{MON} \times (R_2 \div (R_1 + R_2)) \quad (4)$$

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for design specifications. The internal sense resistance ($R_{SENSE}$) can be calculated by the sense voltage ($V_{SENSE}$) divided by the sense current ($I_{SENSE}$) as shown in 式 6. $V_{SENSE}$ can be calculated using 式 4 depending on the resistor divider and monitored voltage. $I_{SENSE}$ can be calculated using 式 5.

$$I_{SENSE} = (V_{MON} - V_{SENSE}) \div R_1 - (V_{SENSE} \div R_2) \quad (5)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (6)$$

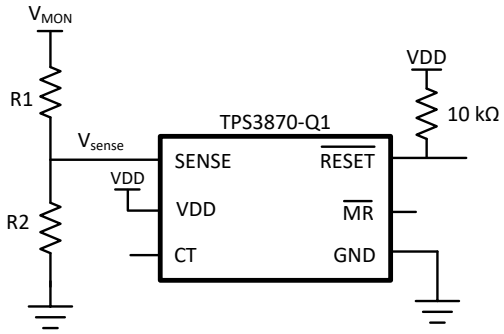



**図 23. Adjustable Voltage Threshold with External Resistor Dividers**

Although 式 4 solves for $V_{SENSE}$, inaccuracies for leakage need to be taken into consideration when understanding the overall threshold accuracy of the device. To calculate the threshold with this inaccuracy taken into account, use 式 7

$$V_{IT\_Actual} = V_{SENSE} + R_1 \times ((V_{SENSE} \div R_2) + I_{SENSE}) \quad (7)$$

To calculate the worst case values through the resistor divider, $I_{SENSE}$ should be taken from the Electrical Characteristics table. While these equations provide a summary of what you need to correctly account for factors that go into determining your resistor divider with inaccuracy, you should use the Application Report Optimizing Resistor Dividers at a Comparator Input to further understand this and to design your implementation. This report explains how to optimize the resistor divider at the SENSE input for an adjustable voltage threshold version of the device. You should follow this Application Report using 0.8 V as the $V_{REF}$ value for the TPS3870-Q1.

### 10.1.5 Immunity to SENSE Pin Voltage Transients

The TPS3870-Q1 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient.

Overdrive is defined by how much the $V_{SENSE}$ exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs ($\overline{RESET}$). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 8:

$$\text{Overdrive \%} = | (V_{SENSE} - (V_{IT+(OV)})) / V_{IT} \text{ (Nominal)} \times 100\% | \quad (8)$$

where:

- $V_{SENSE}$ is the voltage at the SENSE pin
- $V_{IT}$ (Nominal) is the nominal threshold voltage
- $V_{IT+(OV)}$ represents the actual overvoltage tripping voltage

#### *10.1.5.1 Hysteresis*

The overvoltage comparator includes built-in hysteresis that provides noise immunity and ensures stable operation. For example if the voltage on the SENSE pin goes above $V_{IT+(OV)}$ and $\overline{RESET}$ is asserted (driven low), then when the voltage on the SENSE pin is below the positive threshold voltage, $\overline{RESET}$ deasserts after the user-defined $\overline{RESET}$ delay time. Figure 図 24 shows the relation between $V_{IT+(OV)}$ and hysteresis voltage ($V_{HYS}$).

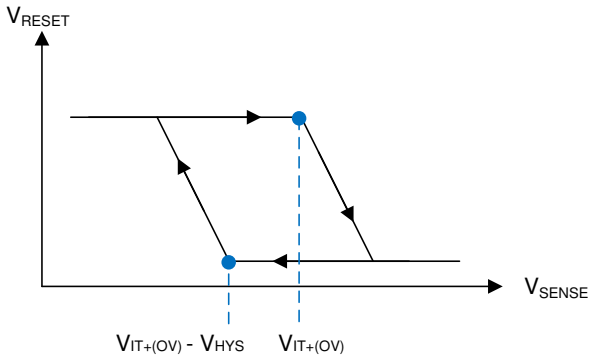



**図 24. SENSE Pin Hysteresis**

## 10.2 Typical Application

### 10.2.1 Design 1: $\overline{\text{RESET}}$ Latch Mode

Another typical application for the TPS3870-Q1 is shown in 図 25. The TPS3870-Q1 is used in a $\overline{\text{RESET}}$ latch output mode. In latch mode, once $\overline{\text{RESET}}$ driven logic low, it will stay low regardless of the sense voltage. If the $\overline{\text{RESET}}$ pin is low on start up, it will also stay low regardless of sense voltage.

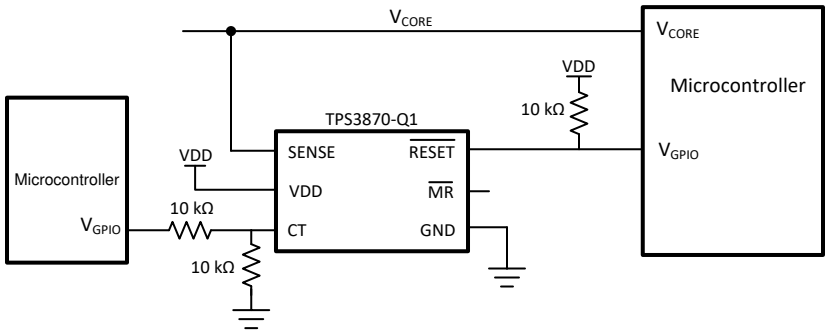



**図 25. Window Voltage Monitoring with $\overline{\text{RESET}}$ Latch**

#### *10.2.1.1 Design Requirements*

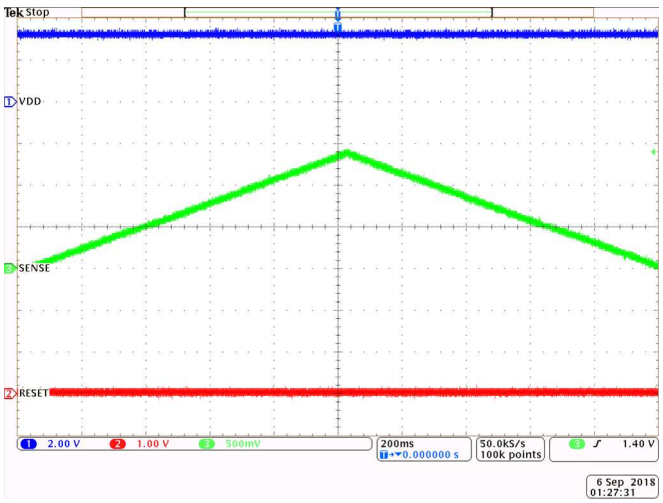
**表 5. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT | DESIGN RESULT |
|---|---|---|
| Monitored Rail | 1.2-$V_{CORE}$ nominal, with alerts if outside of 5% of 1.2 V (including device accuracy), Latch when $\overline{\text{RESET}}$ is low, until voltage is applied on CT pin. | Worst case $V_{IT+(OV)}$ = 1.256 V (4.7%), |
| Output logic voltage | 5-V CMOS | 5-V CMOS |
| Maximum device current consumption | 15 µA | 4.5 µA (Typ), 7 µA (Max) |

#### *10.2.1.2 Detailed Design Procedure*

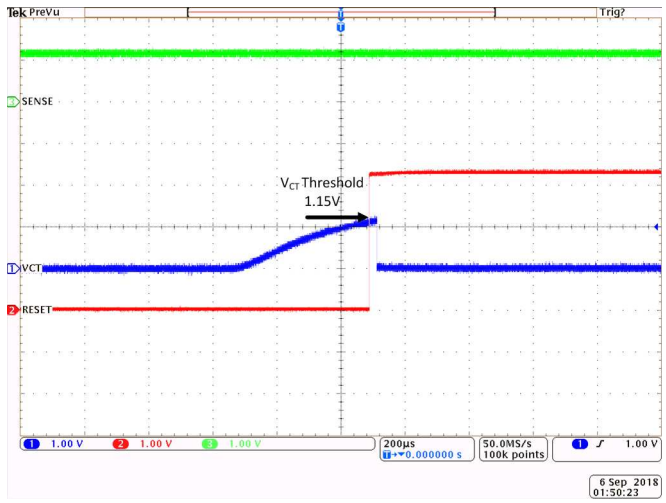
The $\overline{\text{RESET}}$ pin can be latched when the CT pin is connected to a common ground with a pull-down resistor. A 10 kΩ resistors is recommended to limit current consumption. To unlatch the device provide a voltage to the CT pin that is greater than the CT pin comparator threshold voltage, $V_{CT}$. A voltage greater than 1.15 V to recommended to ensure a proper unlatch. Use a series resistance to limit current when an unlatch voltage is applied. To go back into latch operation, disconnect the voltage on the CT pin. The $\overline{\text{RESET}}$ pin will trigger high instantaneously without any reset delay.

### 10.2.1.3 Application Curves



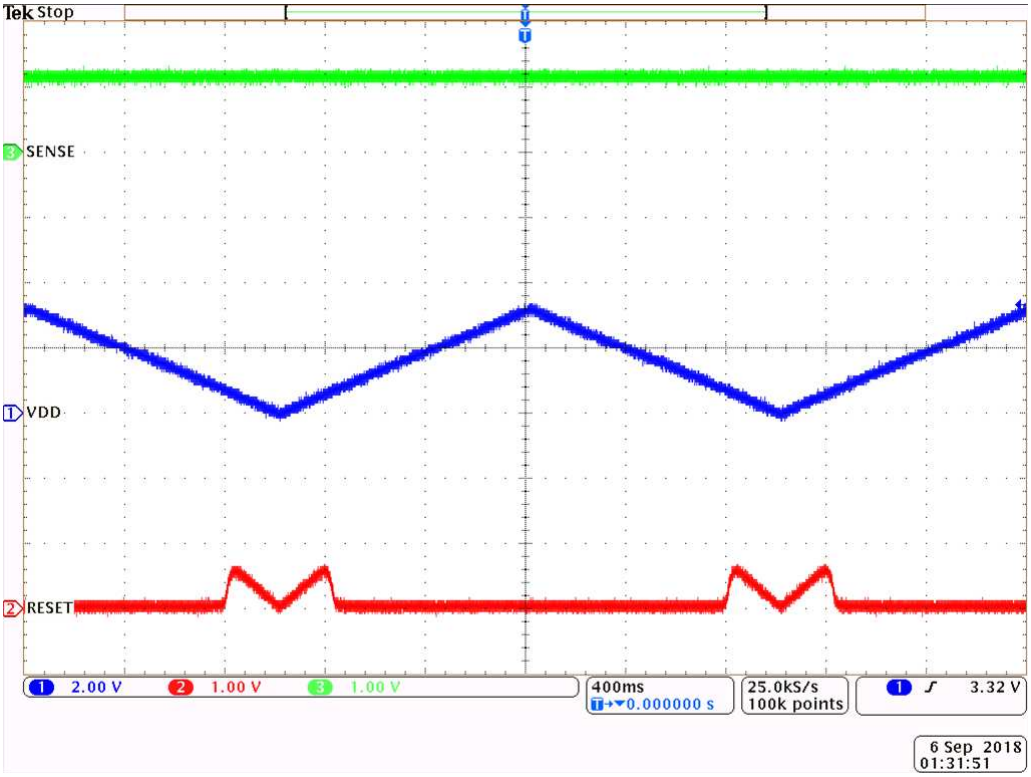

$V_{SENSE}$ ramp from 0 V to 1.4V, $V_{DD}$ = 3.3 V, $V_{CT}$ = 0 V
$V_{\overline{RESET}}$ = VDD = 3.3 V

**図 26. TPS3870-Q1 SENSE Ramp Latch Function**




$V_{CT}$ biased at least to 1.15 V , $V_{SENSE}$ = 1.2 V
$V_{\overline{RESET}}$ = VDD = 3.3 V

**図 27. TPS3870-Q1 CT Bias Unlatch Function**




$V_{DD}$ ramp up from 0 V to 3.3 V , $V_{SENSE}$ = 1.2 V, CT = 0 V
$V_{\overline{RESET}}$ = VDD = 3.3 V

**図 28. TPS3870-Q1 VDD Ramp Latch Function**

# 11 Power Supply Recommendations

## 11.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 1.7 V to 5.5 V. It has a 6-V absolute maximum rating on the VDD pin. It is good analog practice to place a 0.1-µF to 1-µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

# 12 Layout

## 12.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the sense pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

## 12.2 Layout Example

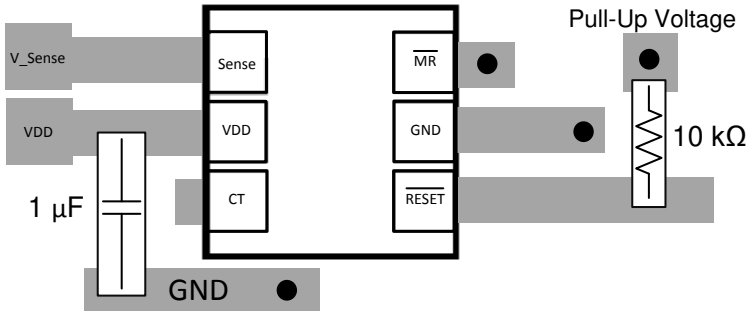



**図 29. Recommended Layout**

# 13 デバイスおよびドキュメントのサポート

## 13.1 デバイスの項目表記

デバイスの型番から機能を解読する方法を、表 6に示します。

**表 6. デバイスの命名規則**

| 説明 | | 項目表記 | 値 |
|---|---|---|---|
| | | TPS3870 | TPS3870 |
| **時間遅延オプション:** すべての部品には 2 つの固定時間遅延と、外付けコンデンサによる可変遅延のオプションがあります。 | OV のみ | J | CT ピンがオープン = 10ms、CT ピンが VDD に接続 = 200ms<br>CT は外付けコンデンサでプログラム可能 |
| | | K | CT ピンがオープン = 1ms、CT ピンが VDD に接続 = 20ms<br>CT は外付けコンデンサでプログラム可能 |
| | | L | CT ピンがオープン = 5ms、CT ピンが VDD に接続 = 100ms<br>CT は外付けコンデンサでプログラム可能 |
| | | M | CTピンがオープン = 50µs、CTピンがVDDに接続 = 50µs<br>CTはプログラム不能 |
| **許容値オプション:** トリガーまたはスレッショルド電圧の、監視対象スレッショルド電圧に対する割合（パーセンテージ）。 | | 3 | 公称値からの過電圧スレッショルド = OV : 3% |
| | | 4 | 公称値からの過電圧スレッショルド = OV : 4% |
| | | 5 | 公称値からの過電圧スレッショルド = OV : 5% |
| | | 6 | 公称値からの過電圧スレッショルド = OV : 6% |
| | | 7 | 公称値からの過電圧スレッショルド = OV : 7% |
| 公称モニタ・スレッショルド電圧のオプション | | 050 | 0.50V |
| | | 055 | 0.55V |
| | | 060 | 0.60V |
| | | 065 | 0.65V |
| | | 070 | 0.70V |
| | | 075 | 0.75V |
| | | 080 | 0.80V |
| | | 085 | 0.85V |
| | | 090 | 0.90V |
| | | 095 | 0.95V |
| | | 100 | 1.00V |
| | | 105 | 1.05V |
| | | 110 | 1.10V |
| | | 115 | 1.15V |
| | | 120 | 1.20V |
| | | 125 | 1.25V |
| | | 130 | 1.30V |
| | | 150 | 1.50V |
| | | 180 | 1.80V |
| | | 250 | 2.50V |
| | | 280 | 2.80V |
| | | 290 | 2.90V |
| | | 330 | 3.30V |
| | | 500 | 5.00V |
| パッケージ | | DSE | WSON - 6ピン(1.5mm×1.5mm) |
| リール | | R | 大型リール |
| 車載用バージョン | | Q1 | Q100 AEC |

## 13.2 ドキュメントのサポート

### 13.2.1 評価基板

TPS3870-Q1 を使用する回路の性能の初期評価に役立てるため、評価基板 (EVM) を利用可能です。TPS3703-Q1 の EVM は、TPS3870-Q1 の過電圧検出機能の評価のみに使用できます。*TPS3703-Q1 評価基板* (および*関連するユーザー・ガイド*) は、テキサス・インスツルメンツの Web サイトのプロダクト・フォルダから請求するか、TI eStore から直接お求めになれます。

## 13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 13.4 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 13.5 商標

E2E is a trademark of Texas Instruments.
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## 13.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS3870J4080DSERQ1 | Active | Production | WSON (DSE) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | H5 |
| TPS3870J4080DSERQ1.A | Active | Production | WSON (DSE) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | H5 |
| TPS3870J4330DSERQ1 | Active | Production | WSON (DSE) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | H4 |
| TPS3870J4330DSERQ1.A | Active | Production | WSON (DSE) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | H4 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

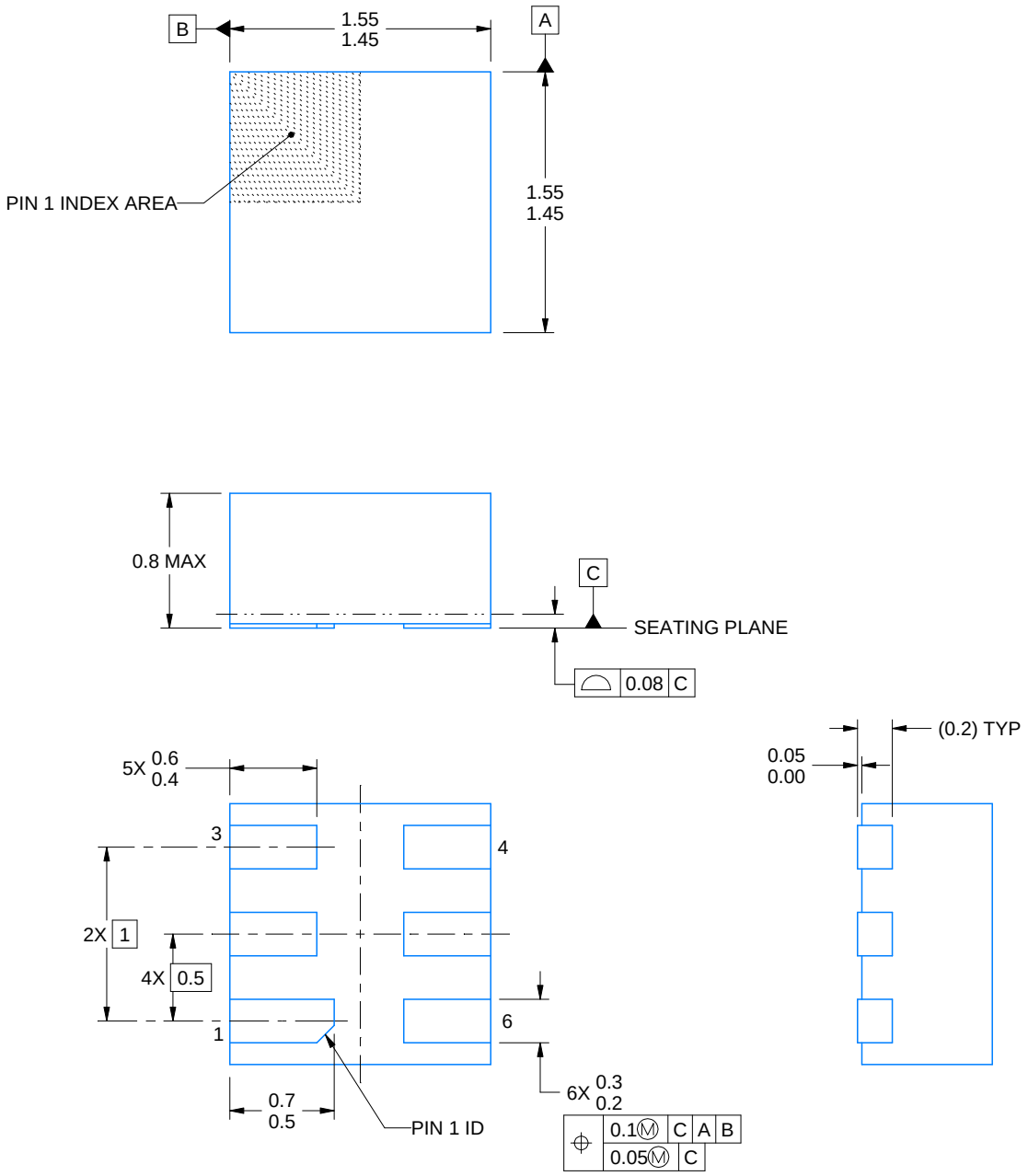
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# DSE0006A

# PACKAGE OUTLINE

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

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NOTES:

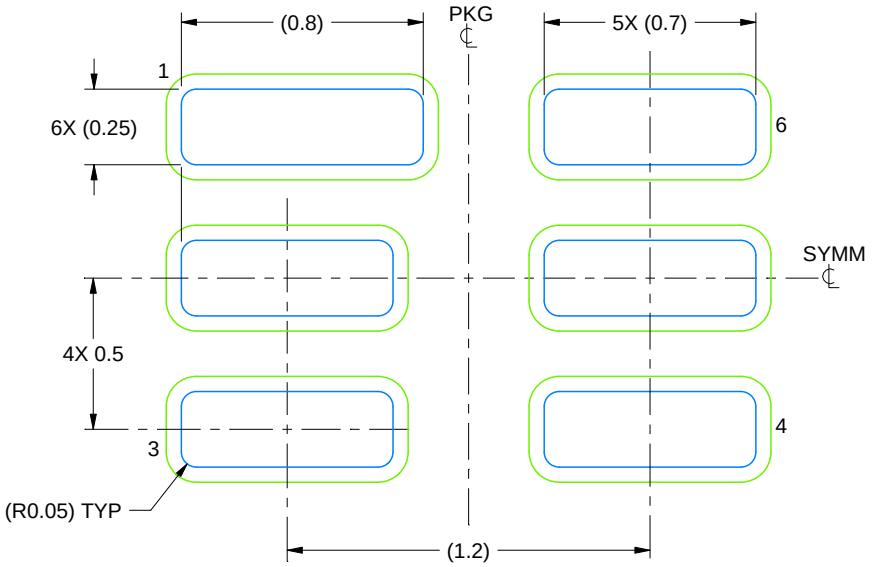
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

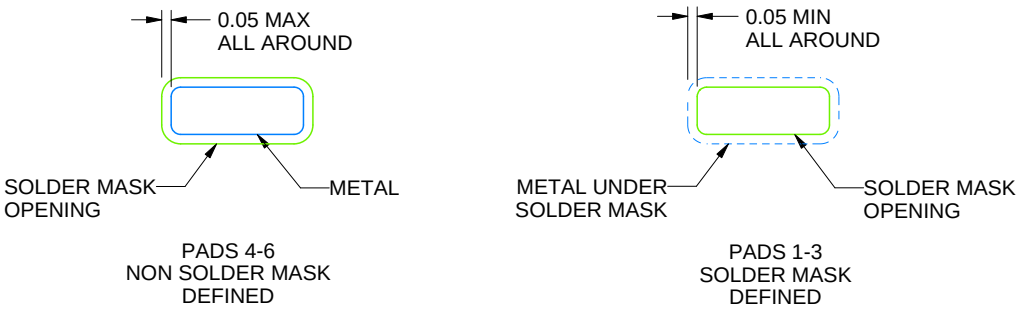
## DSE0006A

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SCALE:40X




SOLDER MASK DETAILS

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NOTES: (continued)

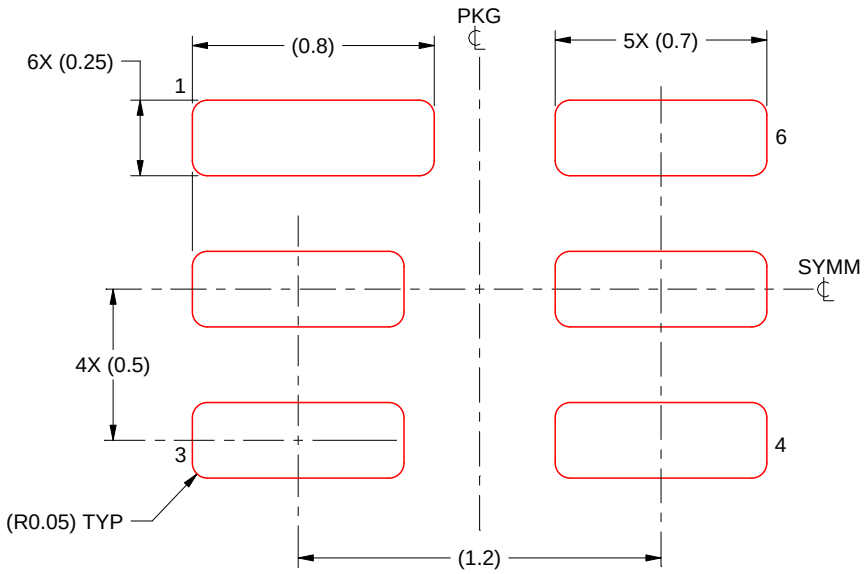
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSE0006A

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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