TPS38800/TPS388R0 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor

1 Features

- Monitor state-of-the art SOCs
  - ± 6mV threshold accuracy (–40°C to +125°C)
  - Input voltage range: 2.5V to 5.5V
  - Undervoltage lockout (UVLO): 2.48V
  - Low quiescent current (maximum): 200µA in idle mode
  - Configuration of 2 to 8 channels available
  - Fixed window threshold levels
    - 5mV steps from 0.2V to 1.475V
    - 20mV steps from 0.8V to 5.5V
- Miniature package and minimal component cost
  - 3mm x 3mm QFN package
  - User adjustable glitch immunity via I²C
  - User adjustable voltage threshold levels via I²C
- Designed for safety applications
  - Active-low open-drain NIRQ output (Latched)
  - Active-low open-drain NRST output (Reset Delay)
  - Cyclic Redundancy Checking (CRC)
  - Packet Error Checking (PEC)

2 Applications

- Medical robotics
- Industrial robotics

3 Description

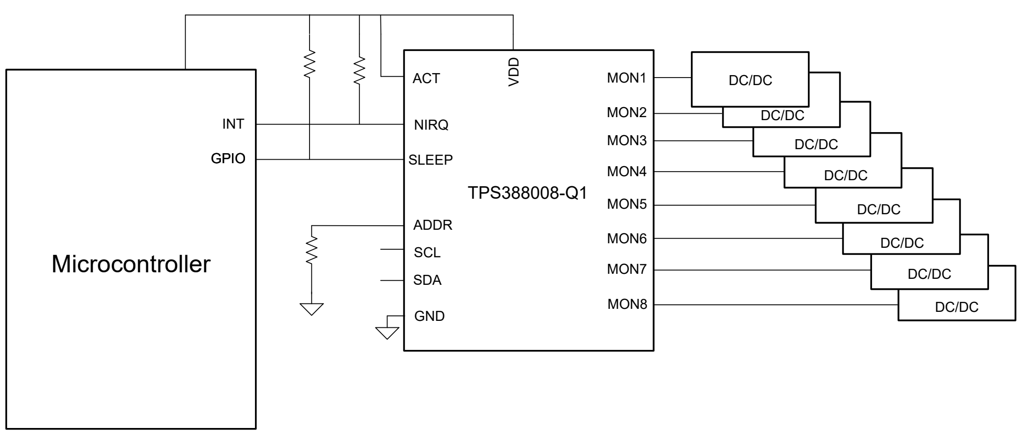
The TPS38800/TPS388R0 device is an ASIL-B device for a 2 to 8 channel window supervisor IC available in a 16-pin 3mm x 3mm QFN package. This high accuracy multichannel voltage supervisor is designed for systems that operate on low-voltage supply rails and have narrow margin supply tolerances.

I²C functionality gives flexibility in selecting thresholds, reset delays, glitch filters, and pin functionality. The internal glitch immunity and noise filters eliminate the need for external RC components to reduce false resets resulting from power transients. TPS38800/TPS388R0 does not require any external resistors for setting overvoltage and undervoltage reset thresholds, which further optimizes overall accuracy, cost, size, and improves reliability for safety systems.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS38800/ TPS388R0	WQFN (16)	3mm x 3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS38800 Typical Circuit

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4 Device Comparison

Figure 4-1 and Figure 4-2 shows the device nomenclature of TPS38800 and TPS388R0 respectively. Table 4-1 provides a summary of available device functions and corresponding part number. Contact TI sales representatives or go online to TI's E2E forum for details and availability of other options; minimum order quantities apply.

See Section 11.1 for more information regarding the device ordering codes. Table 11-1 and Table 11-2 show how to decode the function of the device based on part number.

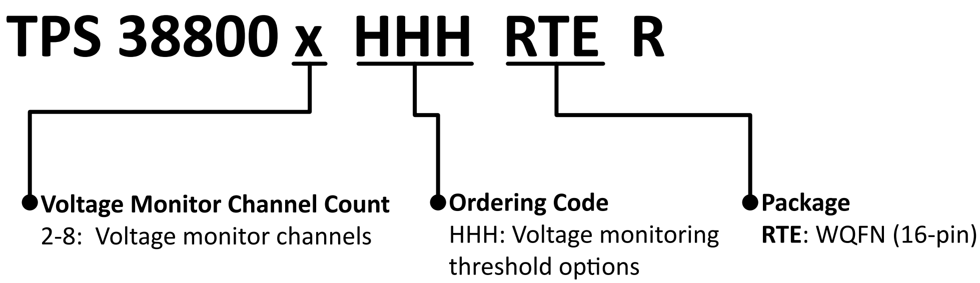

Figure 4-1. TPS38800 Device Nomenclature

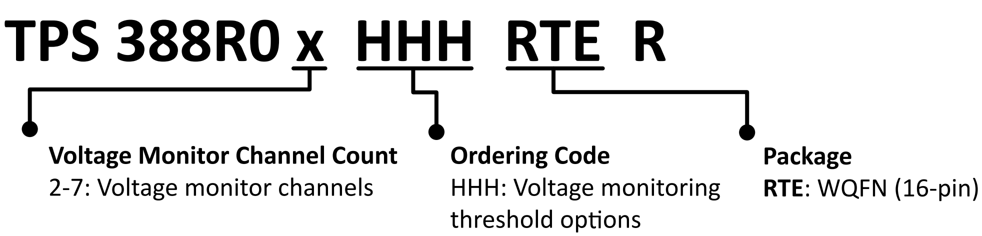

Figure 4-2. TPS388R0Device Nomenclature

Table 4-1. Multichannel Supervisor Summary Table

Specification	TPS38900x-Q1	TPS389R0x-Q1 [(1)]	TPS38800x-Q1 [(1)]	TPS388R0x-Q1 [(1)]	TPS389C0x-Q1	TPS388C0x-Q1 [(1)]
Hardware ASIL Rating	D	D	B	B	D	B
Monitoring Channel Count	2 to 8	2 to 7	2 to 8	2 to 7	2 to 6	2 to 6
Monitoring Range	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V
Comparator Monitoring (HF Faults)	✓	✓	✓	✓	✓	✓
ADC Monitoring (LF Faults)	✓	✓	x	x	✓	x
Watchdog	x	x	x	x	Q&A	Window
Voltage Telemetry	✓	✓	x	x	✓	x
Monitor Glitch Filtering	✓	✓	✓	✓	✓	✓

Table 4-1. Multichannel Supervisor Summary Table (continued)

Specification	TPS38900x-Q1	TPS389R0x-Q1 (1)	TPS38800x-Q1 (1)	TPS388R0x-Q1 (1)	TPS389C0x-Q1	TPS388C0x-Q1 (1)
Sequence Logging	✓	✓	✓	✓	x	✓
NIRQ PIN	✓	✓	✓	✓	✓	✓
NRST PIN	x	✓	x	✓	✓	✓
SYNC PIN	✓	x	x	x	x	x
WDO PIN	x	x	x	x	✓	✓
WDI PIN	x	x	x	x	x	✓
ESM PIN	x	x	x	x	✓	x

(1) Preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options

5 Pin Configuration and Functions

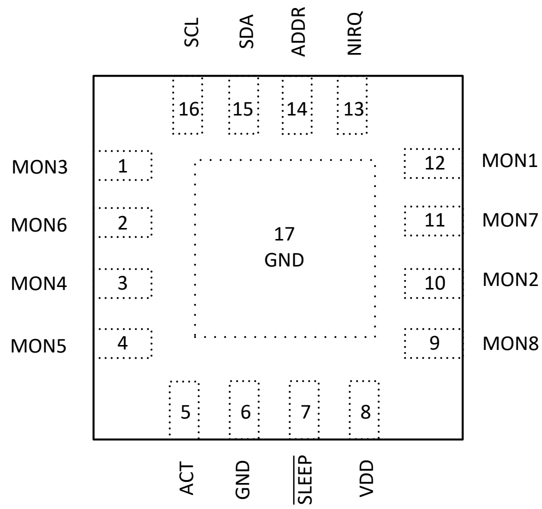

Figure 5-1. RTE Package 16-Pin WQFN TPS388008 Top View

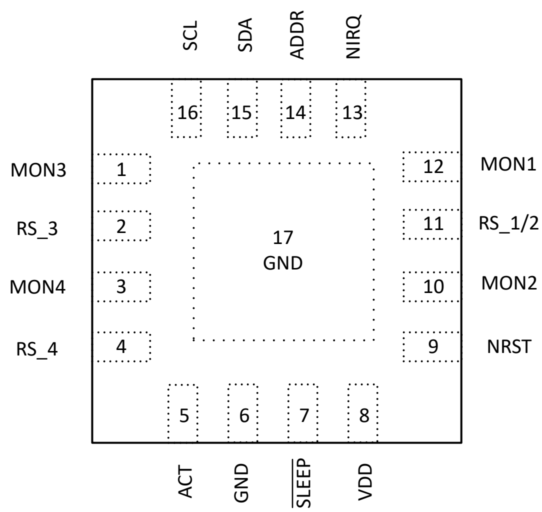

Figure 5-2. RTE Package 16-Pin WQFN TPS388R04 Top View

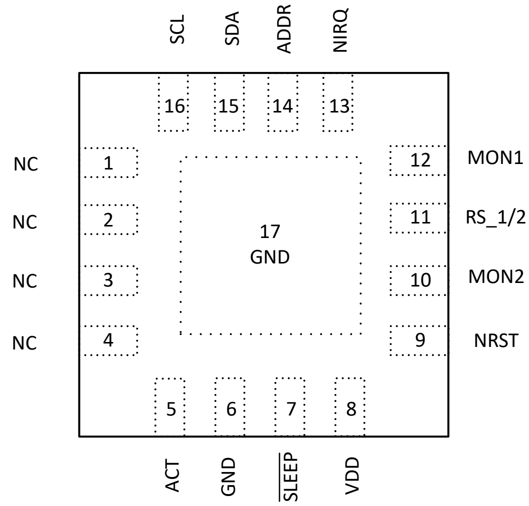

Figure 5-3. RTE Package 16-Pin WQFN TPS388R02Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NO.	TPS388008 NAME	TPS388R04 NAME		
1	MON3	MON3	I	Voltage monitor channel 3
2	MON6	RS_3	I	Voltage monitor channel 6 / Remote sense for channel 3
3	MON4	MON4	I	Voltage monitor channel 4
4	MON5	RS_4	I	Voltage monitor channel 5 / Remote sense for channel 4
5	ACT	ACT	I	Main enable
6	GND	GND	-	Power ground
7	$\overline{\text{SLEEP}}$	$\overline{\text{SLEEP}}$	I	Active low sleep enable
8	VDD	VDD	-	Power supply rail
9	MON8	NRST	I	Voltage monitor channel 8 / Open drain Reset pin
10	MON2	MON2	I	Voltage monitor channel 2
11	MON7	RS_1/2	I	Voltage monitor channel 7 / Remote sense for channel 1/2
12	MON1	MON1	I	Voltage monitor channel 1
13	NIRQ	NIRQ	O	Active-low open-drain interrupt output
14	ADDR	ADDR	I	I^2C address select pin
15	SDA	SDA	I/O	I^2C data pin
16	SCL	SCL	I	I^2C clock pin
17	GND	GND	-	Exposed power ground pad

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	6	V
Voltage	NIRQ, NRST	–0.3	6	V
Voltage	ACT, $\overline{SLEEP}$, SCL, SDA	–0.3	6	V
Voltage	ADDR	–0.3	2	V
Voltage	MONx	–0.3	6	V
Current	NIRQ, NRST		±10	mA
Temperature (2)	Continuous total power dissipation	See the Thermal Information		
	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	125	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) As a result of the low dissipated power in this device, $T_J = T_A$.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)		±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 (2)		±750	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	2.5		5.5	V
NIRQ, NRST	Pin voltage	0		5.5	V
$I_{NIRQ,NRST}$	Pin Currents	0		±5	mA
ADDR	Address pin voltage	0		1.8	V
MONx	Monitor Pins	0		5.5	V
ACT, $\overline{SLEEP}$, SCL, SDA	Pin Voltage	0		5.5	V
R_{UP} (1)	Pull-up resistor (Open Drain config)	10		100	kΩ

6.4 Thermal Information

THERMAL METRIC[1]		TPS38800/TPS388R0 RTE (WQFN) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At 2.6V <= VDD <= 5.5V, NIRQ,NRST Voltage = 10kΩ to V_{DD}, NIRQ,NRST load = 10pF, and over the operating free-air temp range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD= 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
VDD	Input supply voltage		2.6		5.5	V
VDD_{UVLO}	Rising Threshold		2.67		2.81	V
	Falling Threshold		2.48		2.60	V
V_{POR}	Power on Reset Voltage [2]				1.65	V
I_{DD_Active}	Supply current into VDD pin (MON = HF active) ACT = High, Sleep = High	VDD <= 5.5V		1.55	2	mA
I_{DD_Sleep}	Supply current into VDD pin (MON = HF active) ACT = High ,Sleep = Low,I2C = Sleep power bit set to 1	VDD <= 5.5V		1.55	2	mA
I_{DD_Idle}	Supply current into VDD pin ACT = Low, Idle state-I2C active and OVLF mon	VDD <= 5.5V >10ms BIST		200	280	µA
$I_{DD\_Deep\ Sleep}$	Supply current into VDD pin (MON = HF active), ACT = High,Sleep = Low,I2C = Sleep power bit set to 0	VDD <= 5.5V		275	380	µA
V_{MONX}	MON voltage range		0.2		5.5	V
I_{MONX}	Input current MONx pins	V_{MON} = 5V			20	µA
I_{MONX_ADJ}	Input current for ADJ version (1x)	V_{MON} = 5V			0.1	µA
VMON_HF	1x mode (No scaling)		0.2		1.475	V
	with 4x scaling		0.8		5.5	V
Threshold granularity_HF	1x mode (No scaling) LSB			5		mV
	4x mode (With scaling) LSB			20		mV
Accuracy_HF	VMON	0.2V≤V_{MONX}≤1.0V	–6		6	mV
		1.0V<V_{MONX}≤1.475V	-7.5		7.5	mV
		1.475V<V_{MONX}≤2.95V	-0.6		0.6	%
		VMONX>2.95V	-0.5		0.5	%
V_{HYS_HF}	Hysteresis on UV,OV pin(Hysteresis is with respect of the tripoint ((UV),(OV)) [1]	0.2V≤V_{MONX}≤1.475V		5	11	mV
		1.475V<V_{MONX}≤2.95V		9	16	
		VMONX>2.95V		17	28	mV

6.5 Electrical Characteristics (continued)

At 2.6V <= VDD <= 5.5V, NIRQ,NRST Voltage = 10kΩ to V_{DD}, NIRQ,NRST load = 10pF, and over the operating free-air temp range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD= 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS_HF}	Hysteresis on UV,OV pin(Hysteresis is with respect of the tripoint ((UV),(OV)) (1)	Hysteresis disabled orderable		0		mV
MON_OFF	OFF Voltage threshold	Monitored falling edge of V_{MON}	140		215	mV
I_{LKG}	Output leakage current -NIRQ	VDD=V_{NIRQ}=5.5V			300	nA
ACT_L	Logic Low input	DEV_CONFIG.SOC_IF1=1			0.36	V
ACT_H	Logic high input	DEV_CONFIG.SOC_IF1=1	0.84			V
$\overline{SLEEP}$_L	Logic Low input	DEV_CONFIG.SOC_IF1=1			0.36	V
$\overline{SLEEP}$_H	Logic high input	DEV_CONFIG.SOC_IF1=1	0.84			V
ACT	Internal Pull down			100		kΩ
$\overline{SLEEP}$	Internal Pull down			100		kΩ
UV,OV	Steps/Resolution	0.2V<V_{MONX}≤1.475V		5		mV
		0.8V<V_{MONX}<5.5V		20		
V_{OL}	Low level output voltage-NIRQ	NIRQ ,5.5V/5mA			100	mV
$I_{lkg(OD)}$	Open-Drain output leakage current-NIRQ	NIRQ pin in High Impedance,V_{NIRQ} = 5.5, Not asserted state			90	nA
V_{OL}	Low level output voltage-NRST	NRST ,5.5V/5mA			100	mV
$I_{lkg(OD)}$	Open-Drain output leakage current-NRST	NRST pin in High Impedance,V_{NRST} = 5.5, Not asserted state			90	nA
I_{ADDR}	ADDR pin current			20		µA
I^2C ADDR	(Hex format)	R=5.36k		0x30		
		R=16.2k		0x31		
		R=26.7k		0x32		
		R=37.4k		0x33		
		R=47.5k		0x34		
		R=59.0k		0x35		
		R=69.8k		0x36		
		R=80.6k		0x37		
TSD	Thermal Shutdown			155		℃
TSD Hys	Thernal Shutdown Hysterisis			20		℃
RS	Remote sense range		-100		100	mV
I2C ELECTRICAL SPECIFICATIONS						
C_B	Capacitive load for SDA and SCL				400	pF
SDA,SCL	Low Threshold	1.2V config orderable			0.36	V
SDA,SCL	High Threshold	1.2V config orderable	0.84			V
SDA,SCL	Low Threshold	3.3V config orderable			0.99	V
SDA,SCL	High Threshold	3.3V config orderable	2.31			V
SDA,SCL	Low Threshold	1.8V config orderable			0.54	V
SDA,SCL	High Threshold	1.8V config orderable	1.26			V
SDA	VOL	I_{OL}=5mA			0.4	V

(1) Hysteresis is with respect of the tripoint ($V_{IT-(UV)}$, $V_{IT+(OV)}$).
(2) V_{POR} is the minimum V_{DDX} voltage level for a controlled output state.

6.6 Timing Requirements

At 2.6V ≤ VDD ≤ 5.5V, NIRQ,NRST Voltage = 10kΩ to VDD, NIRQ,NRST load = 10pF, and over the operating free-air temp range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
COMMON PARAMETERS						
t_{BIST}	POR to ready with BIST, TEST_CFG.AT_POR=1	includes OTP load			12	ms
t_{NBIST}	POR to ready without BIST, TEST_CFG.AT_POR=0	includes OTP load			2	ms
BIST	BIST time,TEST_CFG.AT_POR=1 or TEST_CFG.AT_SHDN=1				10	ms
t_{I2C_ACT}	I^{2}C active from BIST complete				0	µs
t_{SEQ_Range}	Sequence timestamp range, ACT or $\overline{\text{SLEEP}}$ edge to max counter				4	s
t_{SEQ_LSB}	Sequence timestamp resolution			50		µs
t_{MON_ACT}	Monitoring active from ACT rising edge				10	µs
t_{NIRQ}	Fault detection to NIRQ assertion latency (except OV/UV faults)				25	µs
$t_{PD\_NIRQ\_1X}$	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 100mV			650	ns
$t_{PD\_NIRQ\_4X}$	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 400mV			750	ns
t_{NRST}	Fault detection to NRST assertion latency (except OV/UV faults)				25	µs
$t_{PD\_NRST\_1X}$	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 100mV			650	ns
$t_{PD\_NRST\_4X}$	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 400mV			750	ns
t_{SEQ_ACC}	Accuracy of sequence timestamp		-5		5	%
t_D	RESET time delay	I2C Register time delay =000		200		µs
		I2C Register time delay =001		1		ms
		I2C Register time delay =010		10		ms
		I2C Register time delay =011		16		ms
		I2C Register time delay =100		20		ms
		I2C Register time delay =101		70		ms
		I2C Register time delay =110		100		ms
		I2C Register time delay =111		200		ms
t_{GI_R}	UV & OV debounce range via I2C	FLT_HF(N)	0.1		102.4	µs

6.6 Timing Requirements (continued)

At 2.6V ≤ VDD ≤ 5.5V, NIRQ,NRST Voltage = 10kΩ to VDD, NIRQ,NRST load = 10pF, and over the operating free-air temp range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
I2C TIMING CHARACTERISTICS						
f_{SCL}	Serial clock frequency	Standard mode			100	kHz
f_{SCL}	Serial clock frequency	Fast mode			400	kHz
f_{SCL}	Serial clock frequency	Fast mode +			1	MHz
t_{LOW}	SCL low time	Standard mode	4.7			µs
t_{LOW}	SCL low time	Fast mode	1.3			µs
t_{LOW}	SCL low time	Fast mode +	0.5			µs
t_{HIGH}	SCL high time	Standard mode	4			µs
t_{HIGH}	SCL high time	Fast mode +	0.26			µs
$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
$t_{SU;DAT}$	Data setup time	Fast mode	100			ns
$t_{SU;DAT}$	Data setup time	Fast mode +	50			ns
$t_{HD;DAT}$	Data hold time	Standard mode	10		3450	ns
$t_{HD;DAT}$	Data hold time	Fast mode	10		900	ns
$t_{HD;DAT}$	Data hold time	Fast mode +	10			ns
$t_{SU;STA}$	Setup time for a Start or Repeated Start condition	Standard mode	4.7			µs
$t_{SU;STA}$	Setup time for a Start or Repeated Start condition	Fast mode	0.6			µs
$t_{SU;STA}$	Setup time for a Start or Repeated Start condition	Fast mode +	0.26			µs
$t_{HD:STA}$	Hold time for a Start or Repeated Start condition	Standard mode	4			µs
$t_{HD:STA}$	Hold time for a Start or Repeated Start condition	Fast mode	0.6			µs
$t_{HD:STA}$	Hold time for a Start or Repeated Start condition	Fast mode +	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
t_{BUF}	Bus free time between a STOP and START condition	Fast mode	1.3			µs
t_{BUF}	Bus free time between a STOP and START condition	Fast mode +	0.5			µs
$t_{SU;STO}$	Setup time for a Stop condition	Standard mode	4			µs
$t_{SU;STO}$	Setup time for a Stop condition	Fast mode	0.6			µs
$t_{SU;STO}$	Setup time for a Stop condition	Fast mode +	0.26			µs
trDA	Rise time of SDA signal	Standard mode			1000	
trDA	Rise time of SDA signal	Fast mode	20		300	ns
trDA	Rise time of SDA signal	Fast mode +			120	ns
tfDA	Fall time of SDA signal	Standard mode			300	ns
tfDA	Fall time of SDA signal	Fast mode	1.4		300	ns
tfDA	Fall time of SDA signal	Fast mode +	6.5		120	ns
trCL	Rise time of SCL signal	Standard mode			1000	ns
trCL	Rise time of SCL signal	Fast mode	20		300	ns
trCL	Rise time of SCL signal	Fast mode +			120	ns
tfCL	Fall time of SCL signal	Standard mode			300	ns
tfCL	Fall time of SCL signal	Fast mode	6.5		300	ns
tfCL	Fall time of SCL signal	Fast mode +	6.5		120	ns
tSP	Pulse width of SCL and SDA spikes that are suppressed	Standard mode, Fast mode and Fast mode +			50	ns

7 Detailed Description

7.1 Overview

The TPS38800 family of devices has up to 8 channels that can be configured for over voltage, under voltage or both in a window configuration. Fault outputs can be selectively mapped to NIRQ pin. The TPS38800 features highly accurate window threshold voltages (up to ±6 mV) and a variety of voltage thresholds which can be factory configured or set on boot up by I2C commands.

The TPS388R0 family of devices has up to 6 channels that can be configured for over voltage, under voltage or both in a window configuration. Fault outputs can be selectively mapped to NIRQ and/or NRST pin. The TPS388R0 features highly accurate window threshold voltages (up to ±6 mV) and a variety of voltage thresholds which can be factory configured or set on boot up by I2C commands.

The TPS38800/TPS388R0 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

The TPS38800 is designed to assert active low output signals (NIRQ) when the monitored voltage is outside the safe window. The TPS388R0 is designed to assert active low output signals (NIRQ/NRST) when the monitored voltage is outside the safe windowThe factory configuration can have the interrupts disabled for over voltage and under voltage faults, sequence timeout, BIST enabled at POR, and over voltage and under voltage deglitch settings depending on the OTP

7.2 Functional Block Diagram

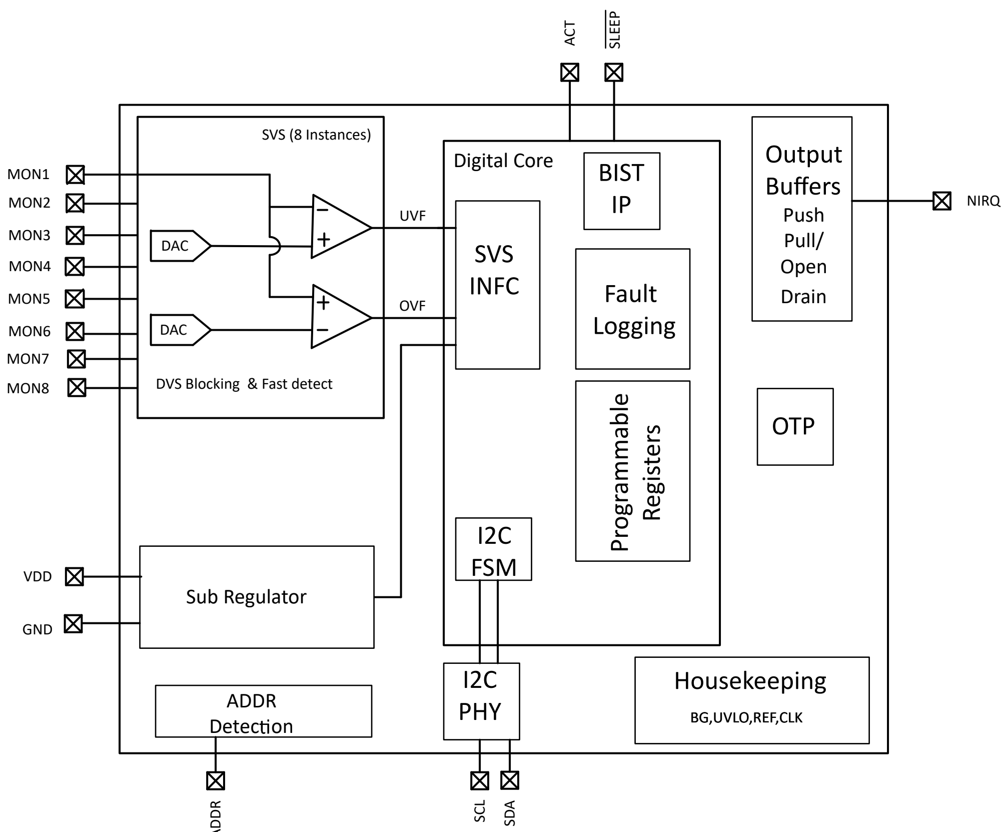

Figure 7-1. TPS388008 Block Diagram

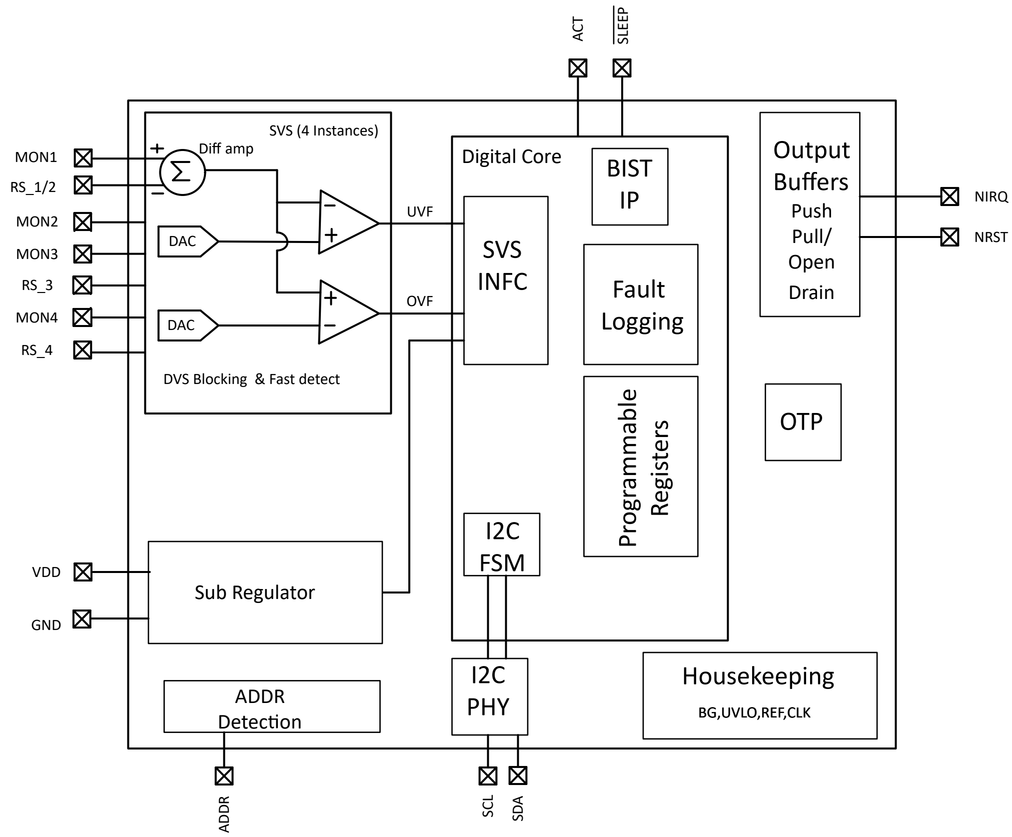

Figure 7-2. TPS388R04 Block Diagram

7.3 Feature Description

7.3.1 I²C

The TPS38800/TPS388R0device follows the I²C protocol (up to 1MHz) to manage communication with host devices such as a MCU or System on Chip (SoC). I²C is a two wire communication protocol implmented using two signals, clock (SCL) and data (SDA). The host device is the primary controller of communication. TPS38800/TPS388R0 device responds over the data line during read or write operations as defined by I²C protocol. Both SCL and SDA signals are open drain topology and can be used in a wired-OR configuration with other devices to share the communication bus. Both SCL and SDA pins need an external pull up resistor to supply voltage (10kΩ recommended).

Figure 7-3 shows the timing relationship between SCL and SDA lines to transfer 1 byte of data. SCL line is always controlled by host. To transfer 1 byte data, host needs to send 9 clocks on SCL. 8 clocks for data and 1 clock for ACK or NACK. SDA line is controlled by either the host or TPS38800/TPS388R0 device based on the read or write operation. Figure 7-4 and Figure 7-5 highlight the communication protocol flow and which device controls SDA line at various instances during active communication.

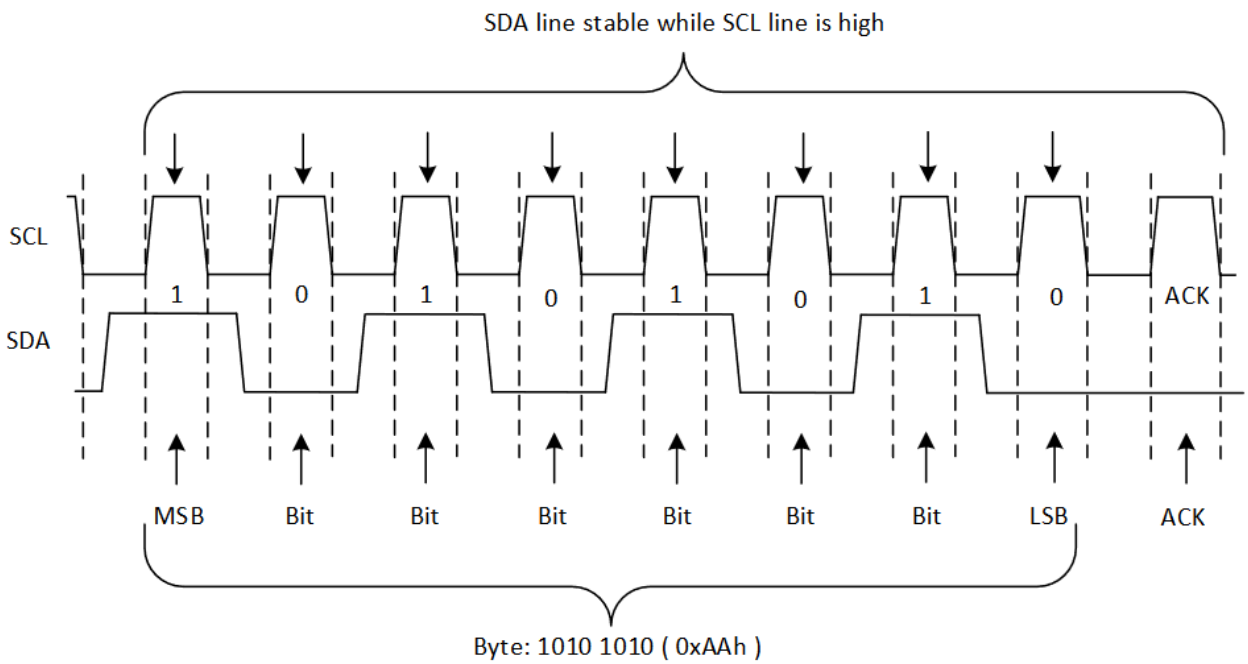

Figure 7-3. SCL to SDA Timing for 1 Byte Data Transfer

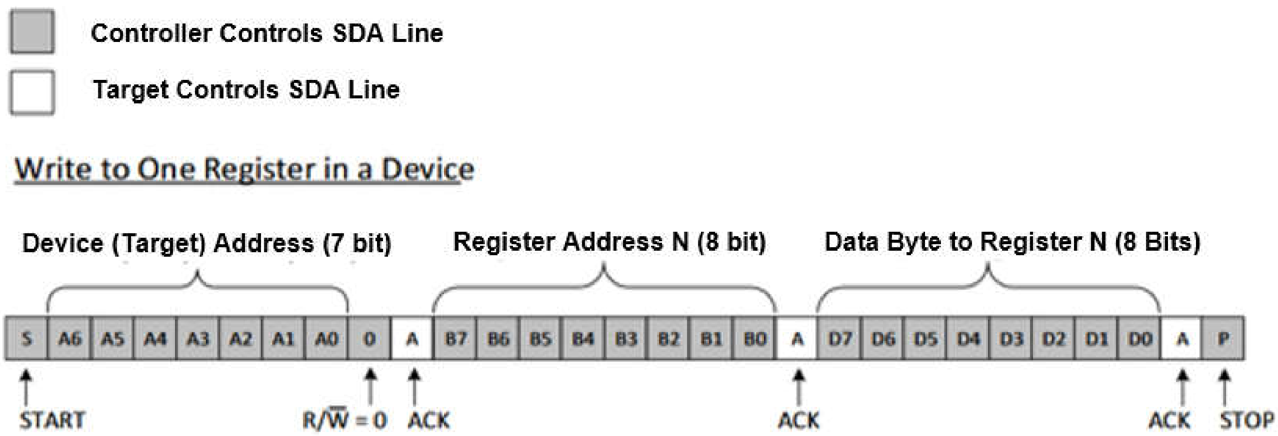

Figure 7-4. I²C Write Protocol

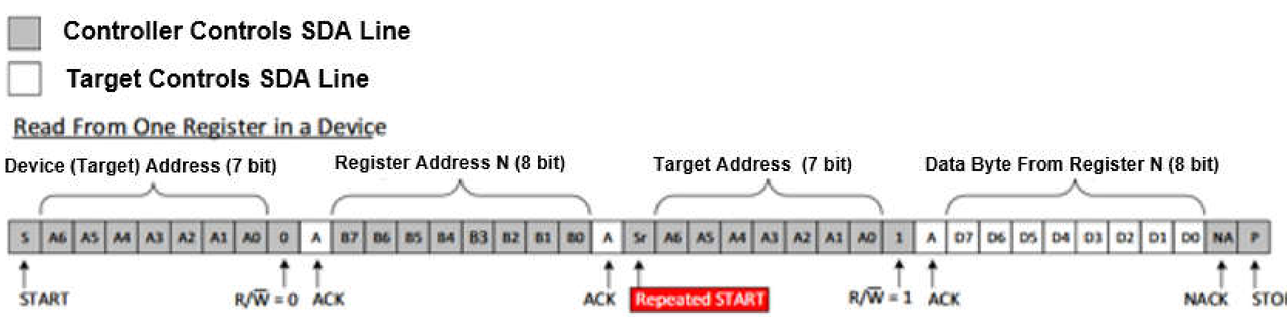

Figure 7-5. I²C Read Protocol

Before initiating communication over I²C protocol, host needs to confirm the I²C bus is available for communication. Monitor the SCL and SDA lines, if any line is pulled low, the I²C bus is occupied. Host needs to wait until the bus is available for communication. Once the bus is available for communication, the host can initiate read or write operation by issuing a START condition. Once the I²C communication is complete, release the bus by issuing STOP command. Figure 7-6 shows how to implement START and STOP condition.

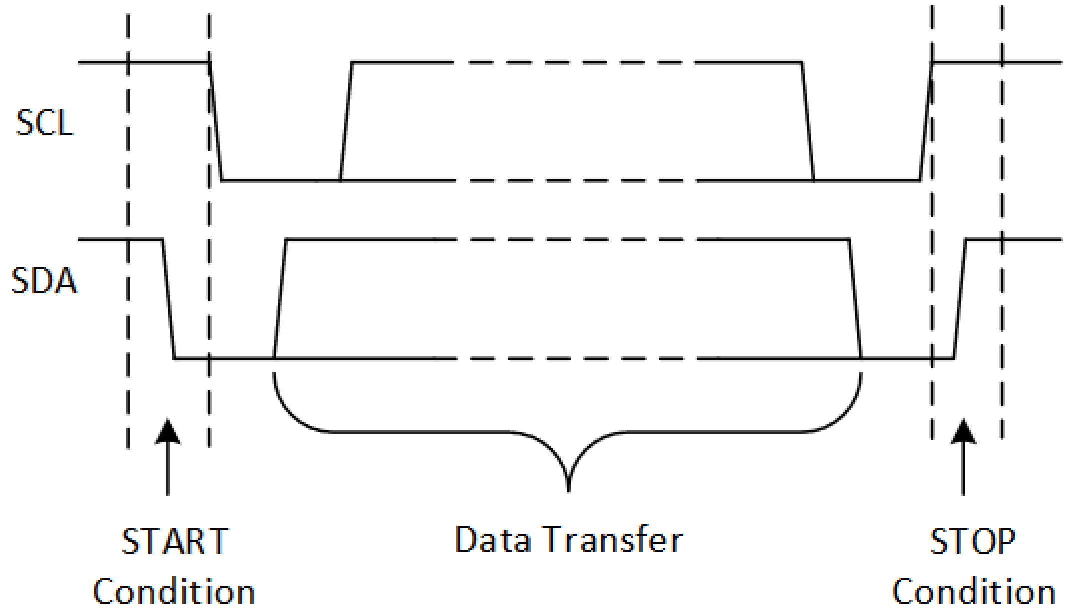

Figure 7-6. I^{2}C START and STOP Condition

Table 7-1 shows the different functionality available when programming with I^{2}C.

Table 7-1. User Programmable I^{2}C Functions

FUNCTIONS	DESCRIPTION
Thresholds for OV/UV- fast loop	Adjustable in 5mV steps from 0.2V to 1.475V and 20mV steps from 0.8V to 5.5V
Voltage Monitoring scaling	1 or 4
Glitch immunity for OV/UV-fast loop	0.1us to 102.4us
Enable sequence timeout	1ms to 4s
Sleep sequence timeout	1ms to 4s
Auto Mask OFF-ON-OFF via ACT	Selectable for each MON channel
Auto Mask OFF-ON-OFF via $\overline{\text{SLEEP}}$	Selectable for each MON channel
Packet error checking for I^{2}C	Enabling or Disabling
Force NIRQ assertion	Controlled by I^{2}C register
Individual channel MON	Enable or Disable
Interrupt disable functions	BIST, PEC, TSD, CRC

7.3.2 Auto Mask (AMSK)

In the case of power up AMSK_ON and AMSK_EXS registers apply. TPS38800/TPS388R0 masks interrupts till the MON voltage crosses the MON's OFF threshold or sequence timeout expires whichever is sooner. In the case of power down AMSK_OFF and AMSK_ENS registers apply. Interrupts are masked till the MON voltage is below the OFF threshold.

Table 7-2 summarizes the auto-mask operation for the ACT and SLEEP transitions.

Table 7-2. Transition Table

TRANSITION	AUTO-MASK APPLIED	AUTO-MASK APPLIES TO	AUTO-MASK INACTIVE	INTERRUPTS ACTIVE FOR MON CHANNELS NOT IN AUTO-MASK
ACT (Low -> High)	AMSK_ON	IEN_UVHF, IEN_OVHF	SEQ_TOUT expires or rail crosses MON's OFF threshold	At ACT=High
ACT (High -> Low)	AMSK_OFF		Auto-mask active in transition till SEQ_TOUT expires	Until SEQ_TOUT expires
SLEEP (Low -> High) ACT = High	AMSK_EXS		SEQ_TOUT expires or rail crosses MON's OFF threshold	Always active
SLEEP (High -> Low) ACT = High	AMSK_ENS		Auto-mask active	Always active

7.3.3 PEC

TPS38800/TPS388R0 supports Packet Error Checking (PEC). TPS38800/TPS388R0 uses a CRC-8 represented by the polynomial C(x)=x^8 + x^2 + x + 1, with CRC initial value set to 0x00. The PEC calculation includes all bytes in the transmission, including address, command and data. The PEC calculation does not include ACK or NACK bits or START,STOP or REPEATED START conditions. The device which acts as a peripheral and supports PEC must be prepared to perform the transfer with or without a PEC, verify the correctness of the PEC if present and only process the message if PEC is correct.

- If PEC is enabled by EN_PEC, and the PEC byte is present in the write transaction, the device reports NACK and assert NIRQ if PEC byte is incorrect.
- If PEC is enabled by EN_PEC, and the PEC byte is not present in the write transaction

-If REQ_PEC =0, missing PEC is treated as good PEC and register write succeeds. NIRQ is not asserted.

-If REQ_PEC =1, missing PEC is treated as incorrect PEC and register write fails. NIRQ is asserted.

Figure 7-7 and Figure 7-8 highlight the communication protocol flow when PEC is required and which device controls SDA line at various instances during active communication.

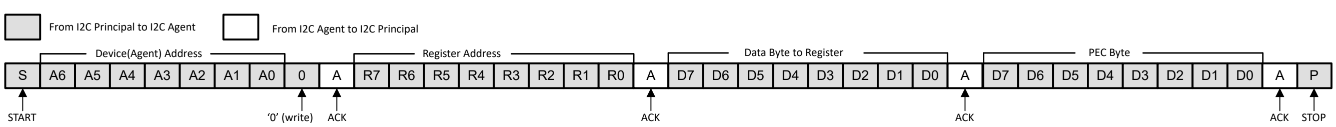

Figure 7-7. Single Byte Write with PEC

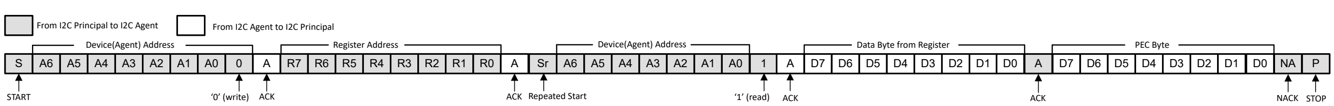

Figure 7-8. Single Byte Read with PEC

7.3.4 VDD

The TPS38800/TPS388R0is designed to operate from an input voltage supply range between 2.6V to 5.5V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 1µF capacitor between the VDD pin and the GND pin.

V_{DD} needs to be at or above $V_{DD(MIN)}$ for at least the start-up delay (t_{SD}+ t_D) for the device to be fully functional.

7.3.5 MON

The TPS38800/TPS388R0 combines two comparators with a precision reference voltage and a trimmed resistor divider per monitor (MON) channel. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides noise immunity and maintains stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 1nF to 10nF bypass capacitor at the MON input to reduce sensitivity to transient voltages on the monitored signal. Specific debounce times or deglitch times can also be set independently for each MON via I2C registers. A debounce filter for glitch immunity can be configured for each monitor using the FLT_HF registers in BANK1 associated with each MON channel.

When monitoring VDD supply voltage, the MON pin can be connected directly to VDD. The output (NIRQ/NRST) is high impedance when voltage at the MON pin is between upper and lower boundary of threshold.

7.3.6 NIRQ

In a typical TPS38800/TPS388R0 application, the NIRQ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the enable input of a voltage regulator [such as a DC-DC converter or low-dropout regulator (LDO)].NIRQ is a interrupt error ouput with latched behavior, if a monitored voltage falls or rises outside of the programmed OVHF and UVHF thresholds NIRQ is asserted. NIRQ remains in a low state until the action causing the fault is no longer present and a 1-to-clear is written to the bit signaling the fault. Un-mapping NIRQ from a fault reporting register does not de-assert the NIRQ signal

The TPS38800/TPS388R0 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To maintain proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current. These values are specified in *Section 6*. The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS38800/ TPS388R0 NIRQ pin.

7.3.7 NRST

The NRST pin features a programmable reset delay time that can be adjusted from 0.2ms to 200ms when using I2C RESET time delay register. NRST is an open-drain output, requires an external1kΩ to 100kΩ pullup resistor. When the device is powered up and POR is complete, NRST is asserted low until the BIST is complete. After the BIST, NRST remains high (not asserted) until triggered by a mappable fault condition. An NRST_MISMATCH fault asserts if the NRST pin is pulled to an unexpected state. For example, if the NRST pin is in a high-impedence state (logic high) and is externally pulled low, then an NRST_MISMATCH fault asserts. During an NRST toggle NRST mismatch is active after 2µs, NRST must exceed 0.6*VDD to be considered in a logic high state.

NRST is mappable to the OVHF and UVHF faults using the FC_LF[n] registers. If a monitored voltage falls or rises outside of the programmed OVHF and UVHF thresholds, then NRST is asserted, driving the NRST pin low. When the monitored voltage comes back into the valid window, a reset delay circuit is enabled that holds NRST low for a specified reset delay period (t_D).

The t_D period is determined by the RST_DLY[2:0] value found in the TI_CONTROL register. When the reset delay has elapsed, the NRST pin goes to a high-impedance state and uses a pullup resistor to hold NRST high. The pullup resistor must be connected to the proper voltage rail to allow other devices to be connected at the correct interface voltage. To maintain proper voltage levels, give consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (VOL), capacitive loading, and leakage current.

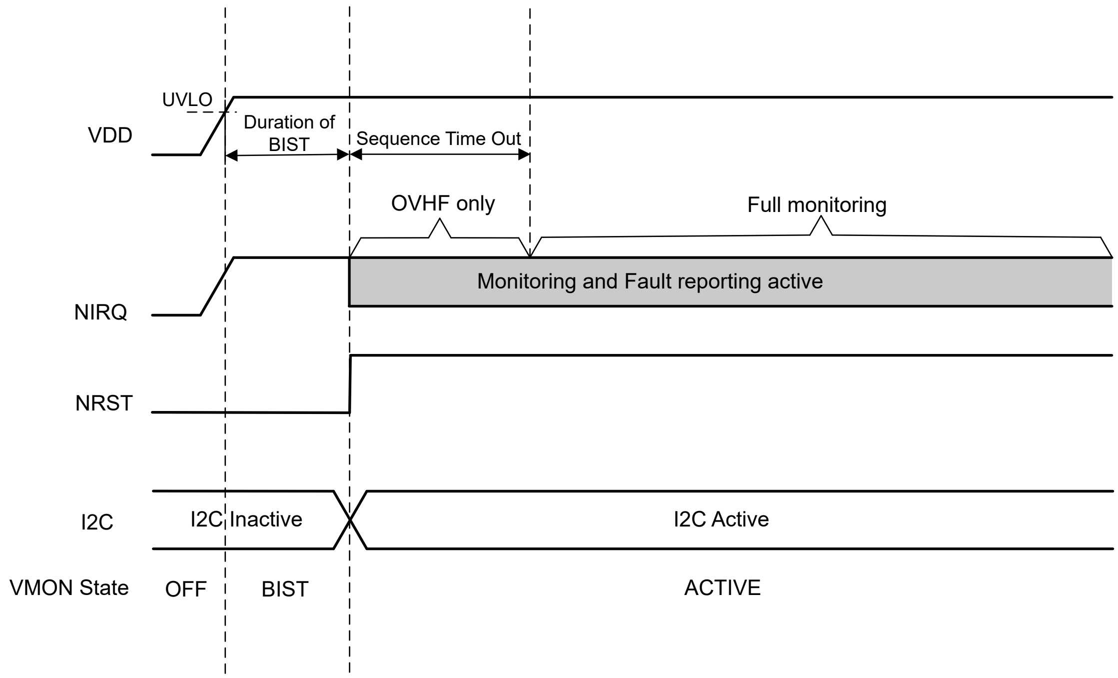

Figure 7-9. NRST Start Up Behavior

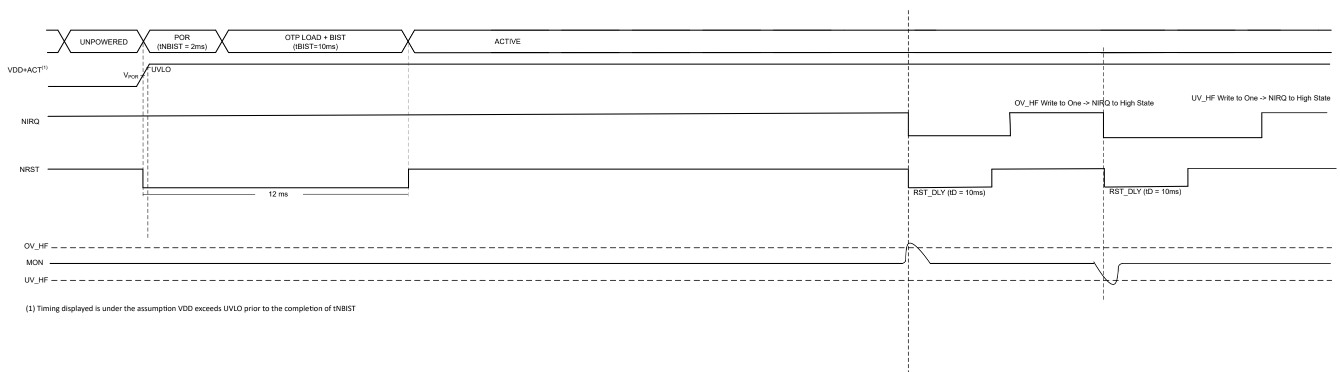

Figure 7-10. NRST Timing diagram for voltage faults

7.4 Device Functional Modes

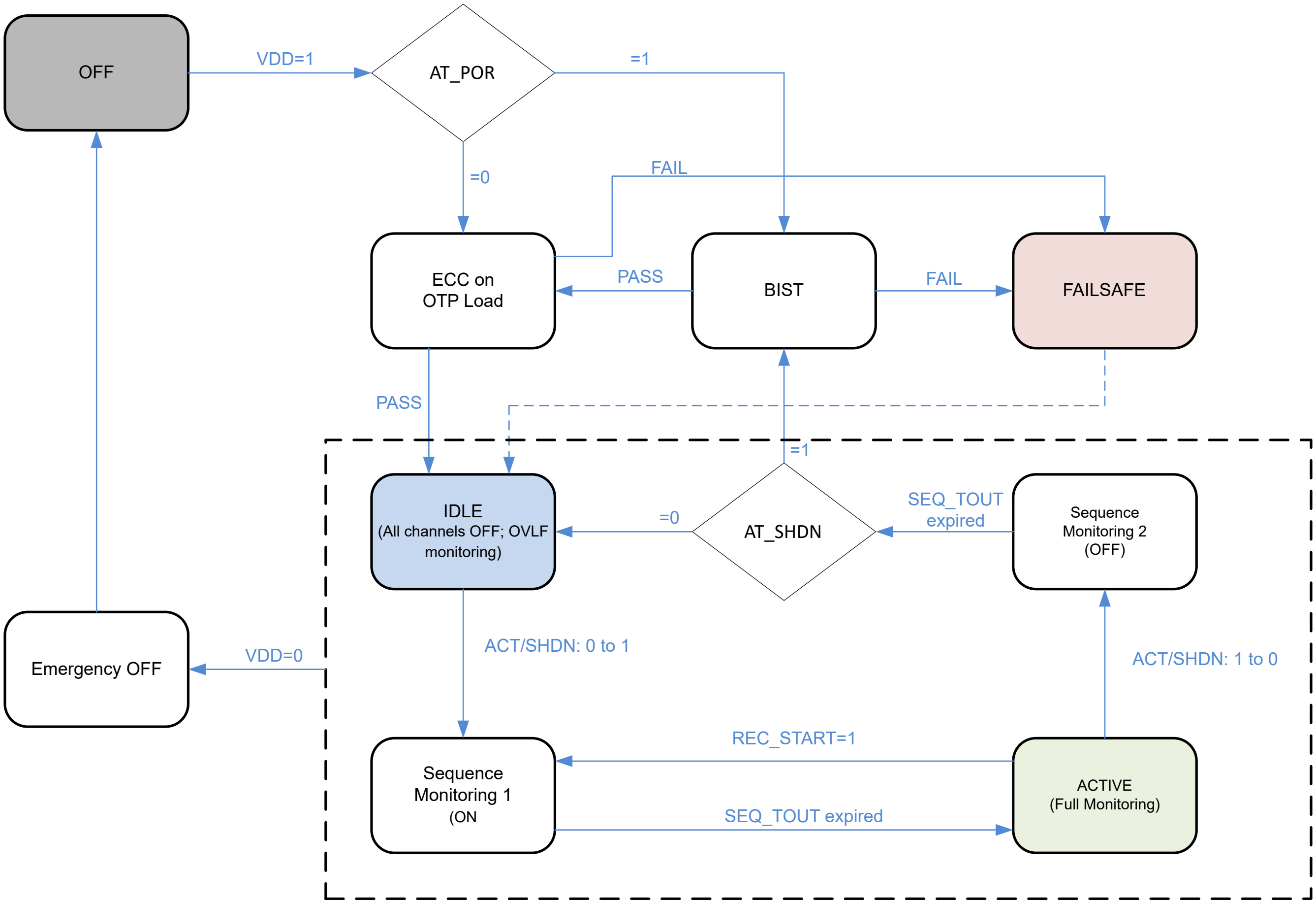

Figure 7-11. TPS38800/TPS388R0 State Diagram

7.4.1 Built-In Self Test and Configuration Load

Built-In Self Test (BIST) is performed:

1. At Power On Reset (POR), if TEST_CFG.AT_POR=1
2. When exiting ACTIVE state due to ACT transitioning from 1→0, if TEST_CFG.AT_SHDN=1

Configuration load from OTP is assisted by ECC (supporting SEC-DED). This is to protect against data integrity issues and to maximize system availability.

During BIST, NIRQ is de-asserted (asserted in case of failure), input pins are ignored, and the I^2C block is inactive with SDA and SCL de-asserted. NRST is asserted low during BIST. The BIST includes device testing to meet the Technical Safety Requirements. Once BIST is completed without failure, I^2C is immediately active and the device enters the IDLE state after loading the configuration data from OTP. If BIST fails and/or ECC reports Double-Error Detection (DED), NIRQ is asserted, the device enters FAILSAFE state, and a best effort attempt is made to active I^2C. TEST_INFO register provides additional information on the test results.

The detailed behavior upon success/failure of the BIST is controlled by INT_TEST and IEN_TEST registers. Reporting of the BIST results is carried out through:

- NIRQ pin: pulled low depending on the test result and BIST_C and BIST bits in IEN_TEST
- NRST pin: pulled low during BIST
- I_BIST_C and BIST bits in INT_TEST register depending on IEN_TEST settings
- VMON_STAT.ST_BIST_C register bit
- TEST_INFO[3:0] register bits

7.4.1.1 Notes on BIST Execution

Upon POR the TPS38800/TPS388R0 needs to make a decision whether to run BIST or not, based on the value of the TEST_CFG.AT_POR register bit. Assuming that ECC on this register is performed after BIST has checked the ECC logic, data intregitry is not verified before running BIST.

7.4.2 TPS38800 Power ON

When the TPS38800/TPS388R0 is powered ON, BIST is optionally executed (depending on TEST_CFG.AT_POR register bit); I^2C and fault reporting (through NIRQ) become active as soon as BIST is completed and configuration is loaded from OTP (assisted by ECC, supporting SEC-DED).

The details of the configuration load ECC and BIST results are reported are reported in TEST_INFO register.

Upon detection of the ACT rising edge, the TPS38800/TPS388R0 begins the sequence time out where inputs selected with auto-mask register AMSK_ON start with masked (disabled) interrupts for Under-Voltage High Frequency (UVHF) conditions. Selected inputs are masked until the input passes the MON's OFF threshold or sequence time out has expired. $\overline{\text{SLEEP}}$ is ignored until ACT is High and the sequence timeout has expired. The TPS38800/TPS388R0 then acts on $\overline{\text{SLEEP}}$ transitions to monitor/record Sleep Entry/Exit sequences.

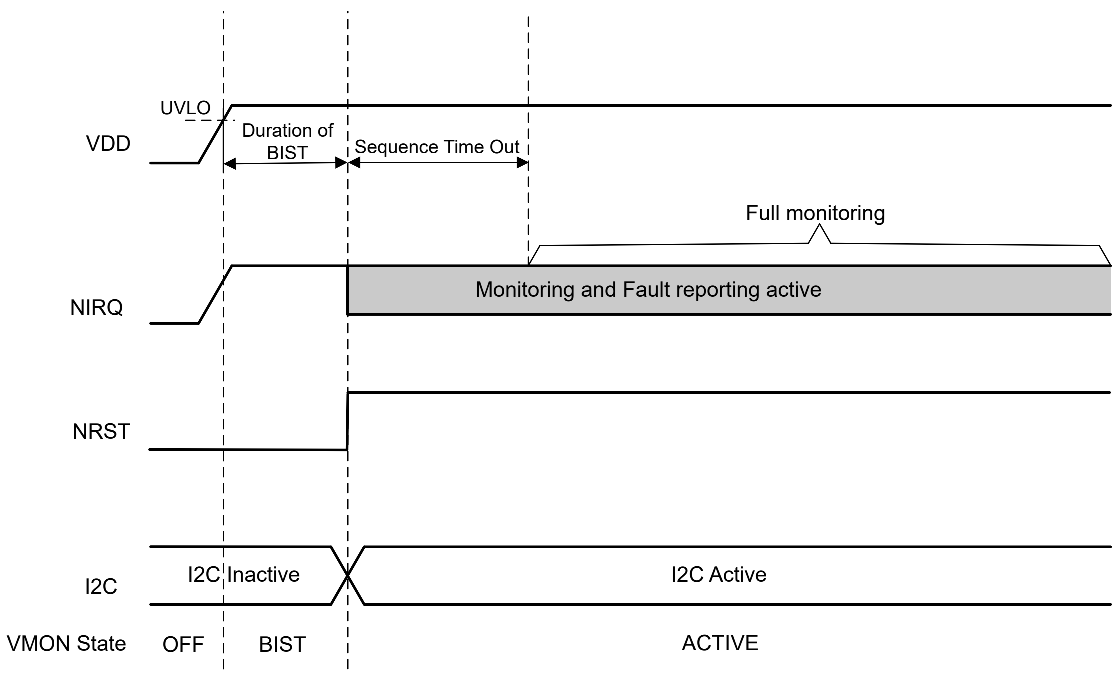

Figure 7-12. TPS38800/TPS388R0 Power ON Signaling and Internal States

BIST completion can be detected through interrupt or register polling:

- Interrupt: INT_TEST.I_BIST_C flag is set and NIRQ is asserted if IEN_TEST.BIST_C=1
- Polling: VMON_STAT register can be polled to read the ST_BIST_C bit

7.4.3 General Monitoring

7.4.3.1 IDLE Monitoring

The TPS38800/TPS388R0 is in IDLE state when ACT is Low and BIST is completed.

In this state, all monitored channels are expected to be in the OFF state (below the OFF threshold). During this state all monitoring is disabled.

7.4.3.2 ACTIVE Monitoring

The TPS38800/TPS388R0 is in ACTIVE state when ACT is High.

VMON monitors High Frequency channel levels against Under-Voltage High Frequency (UVHF) and Over-Voltage High Frequency (OVHF) thresholds.

Some channels can be connected to rails which are controlled by user software. Such channels can be in OFF state (below the OFF threshold) when the TPS38800/TPS388R0 is in ACTIVE state, and have the UVHF interrupts normally disabled. Once these rails are turned ON, the TPS38800/TPS388R0 host enables the channels UVHF interrupts to allow full monitoring. Similarly, before these rails are turned OFF, the TPS38800/TPS388R0 host disables the channels UVHF interrupts to avoid false UV violations during the ramp down. As these channels are not part of the sequencing initiated by ACT or $\overline{\text{SLEEP}}$, UVHF/OVHF interrupts cannot be automatically enabled/disabled using the auto-mask registers.

Other enabled channels can be in OFF state as a result of the $\overline{\text{SLEEP}}$ 1→0 transition sequence. Those channels are identified by the AMSK_ENS auto-mask register, used to avoid UVHF and OVHF interrupts during the transition.

Table 7-3. Modes of Operation Summary

Mode	Pin/Bit Condition	Iq	Monitored- Triggers NIRQ if CHx enabled	Status only
ACTIVE	ACT=High, Sleep=High	1.5mA	OVHF, UVHF	OFF
IDLE	ACT=Low, Sleep=X	230uA	OVHF	OFF
SLEEP ACT=High, SLEEP=Low Sleep Power bit=1	CHx not assigned to Sleep	1.5mA	OVHF, UVHF	OFF
	CHx assigned to Sleep (AMSK=1)		No monitoring	OFF
	CHx assigned to Sleep (AMSK=0)		OVHF, UVHF	OFF
DEEP SLEEP ACT=High, SLEEP=Low Sleep Power bit=0	CHx not assigned to Sleep	330uA	OVHF, UVHF	-
	CHx assigned to Sleep (AMSK=1)		No monitoring	-
	CHx assigned to Sleep (AMSK=0)		OVHF, UVHF	-

7.4.3.3 Sequence Monitoring 1

Sequence Monitoring 1 is a transitional state entered when:

1. ACT transitions 0→1
2. $\overline{\text{SLEEP}}$ transitions 0→1, if ACT=1
3. $\overline{\text{SLEEP}}$ transitions 1→0, if ACT=1

The following sections describe the actions for the three cases explicitly for clarity.

7.4.3.3.1 ACT Transitions 0→1

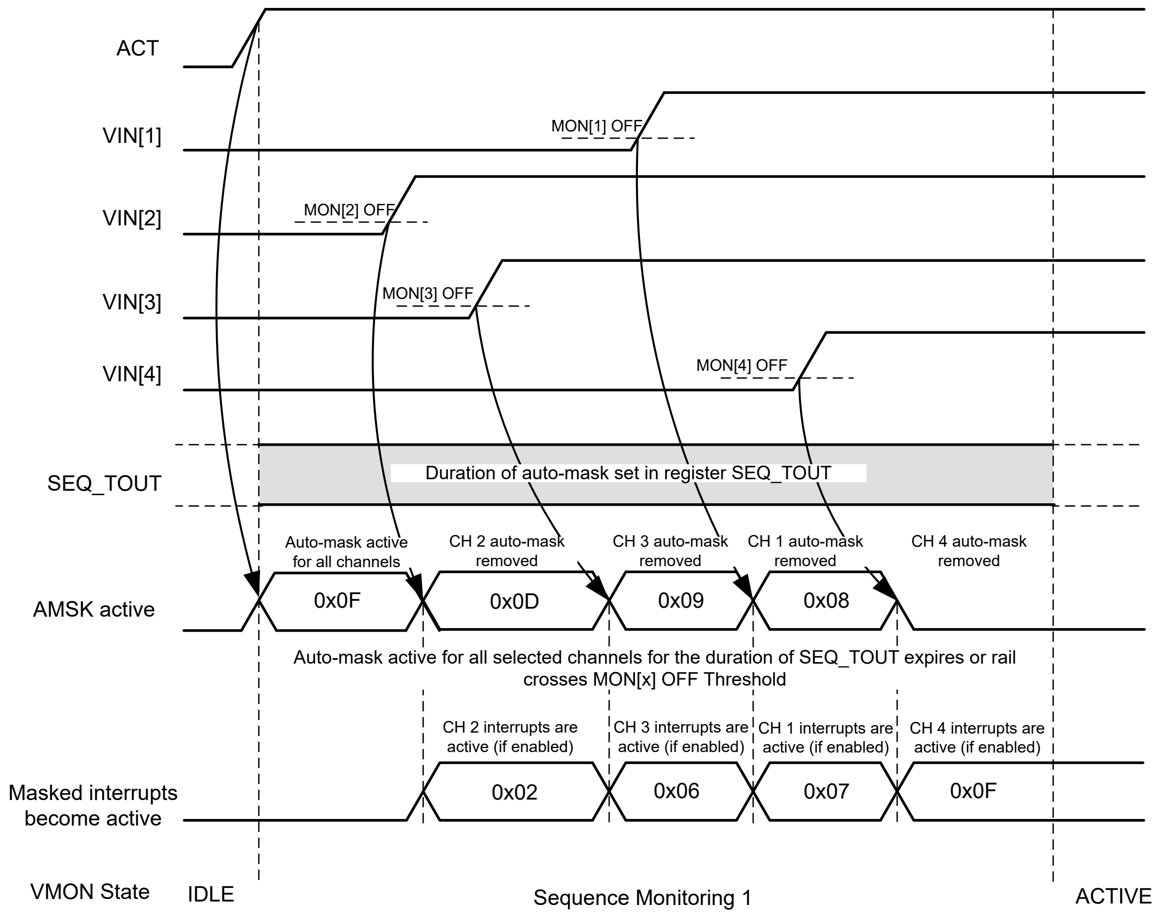

Figure 7-13. ACT 0→1 Transition

The TPS38800/TPS388R0 takes several actions on the ACT 0→1 transition:

1. After ACT 0→1 transition:
    a. All TPS38800/TPS388R0 inputs selected with auto-mask register AMSK_ON start with masked (disabled) interrupts for Under-Voltage High Frequency (UVHF) conditions.
    b. As each rail passes the MON's OFF threshold, automatically (and expected to happen within about 5-10 µs) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN_UVHF and IEN_OVHF registers.
2. After SEQ_TOUT timeout:
    a. TPS38800/TPS388R0 is in ACTIVE state and starts normal monitoring.

7.4.3.3.2 SLEEP Transition 1→0

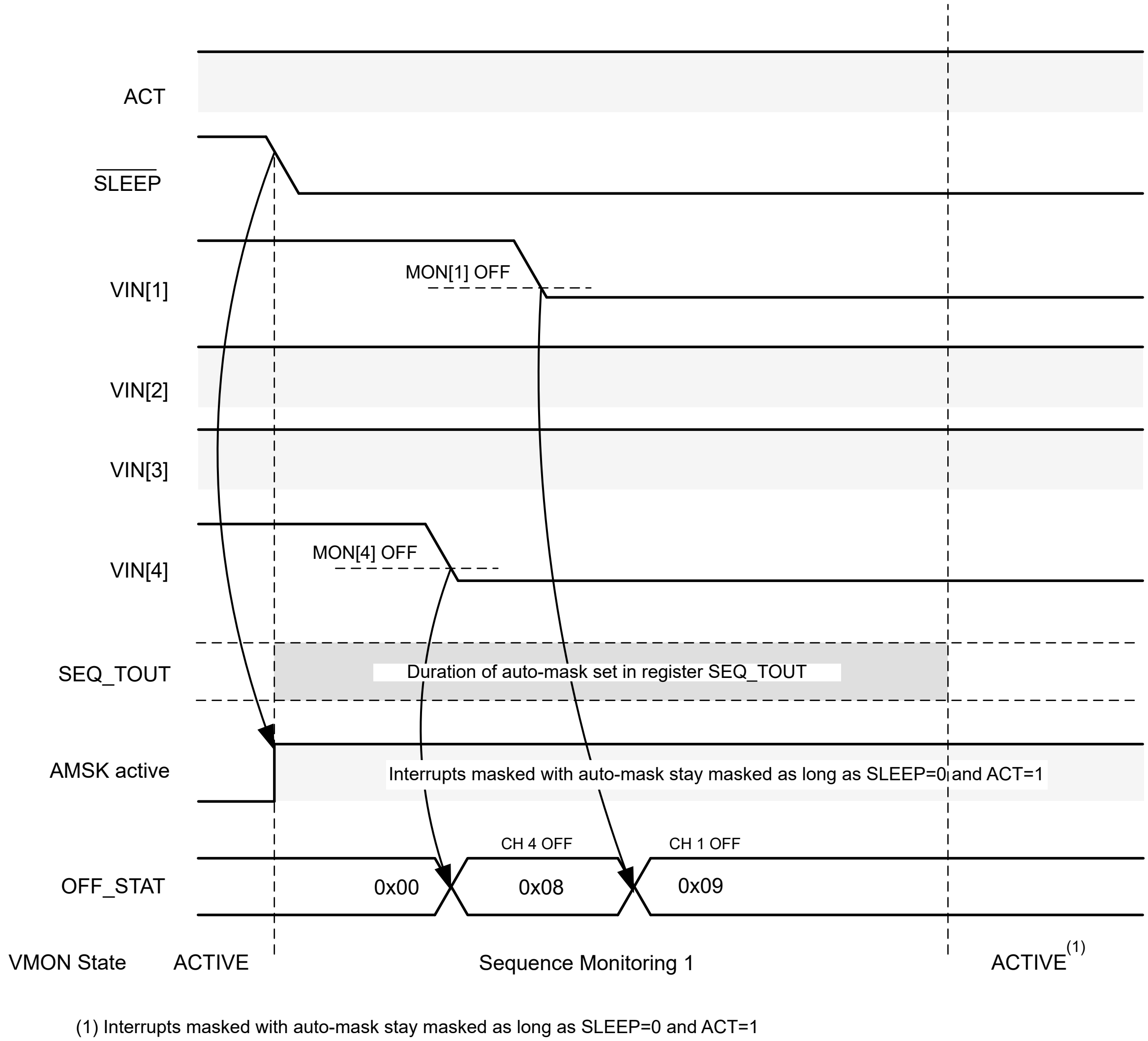

Figure 7-14. SLEEP 1→0 Transition

The TPS38800/TPS388R0 takes several actions on the SLEEP 1→0 transition:

1. After SLEEP 1→0 transition:
   a. Relevant TPS38800/TPS388R0 inputs selected with auto-mask register AMSK_ENS are set with masked interrupts for UVHF and OVHF conditions.
2. After SEQ_TOUT has expired:
   a. TPS38800/TPS388R0 is in ACTIVE state and interrupts for UVHF and OVHF conditions remain masked so long as SLEEP=0 and ACT=1.

7.4.3.3.3 SLEEP Transition 0→1

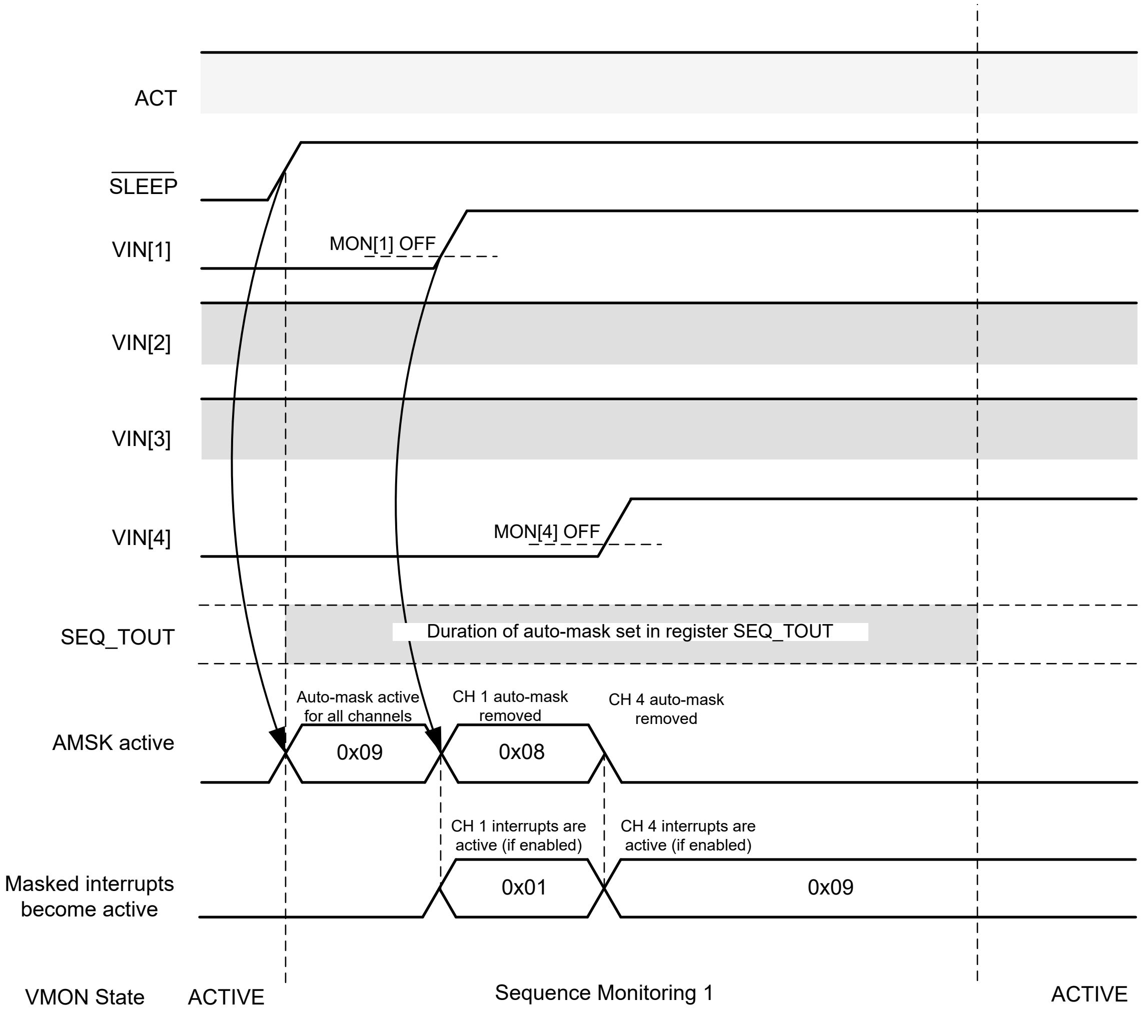

Figure 7-15. SLEEP 0→1 Transition

The TPS38800/TPS388R0 takes several actions on the SLEEP 0→1 transition:

1. After SLEEP 0→1 transition:
   a. As each rail passes the MON's OFF threshold, automatically (and expected to happen within about 5-10 µs) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN_UVHF and IEN_OVHF registers.
2. After a SEQ_TOUT has expired.
   a. TPS38800/TPS388R0 enters the ACTIVE state and TPS38800/TPS388R0 continues normal monitoring in accordance with the IEN_UVHF and IEN_OVHF registers.

7.4.3.4 Sequence Monitoring 2

Sequence Monitoring 2 is very similar to Sequence Monitoring 1, however, an extra step is taken when exiting this transitioning state depending on the TEST_CFG.AT_SHDN register bit.

Sequence Monitoring 2 is entered when ACT transitions 1→0. The actions taken are described in Section 7.4.3.4.1.

7.4.3.4.1 ACT Transition 1→0

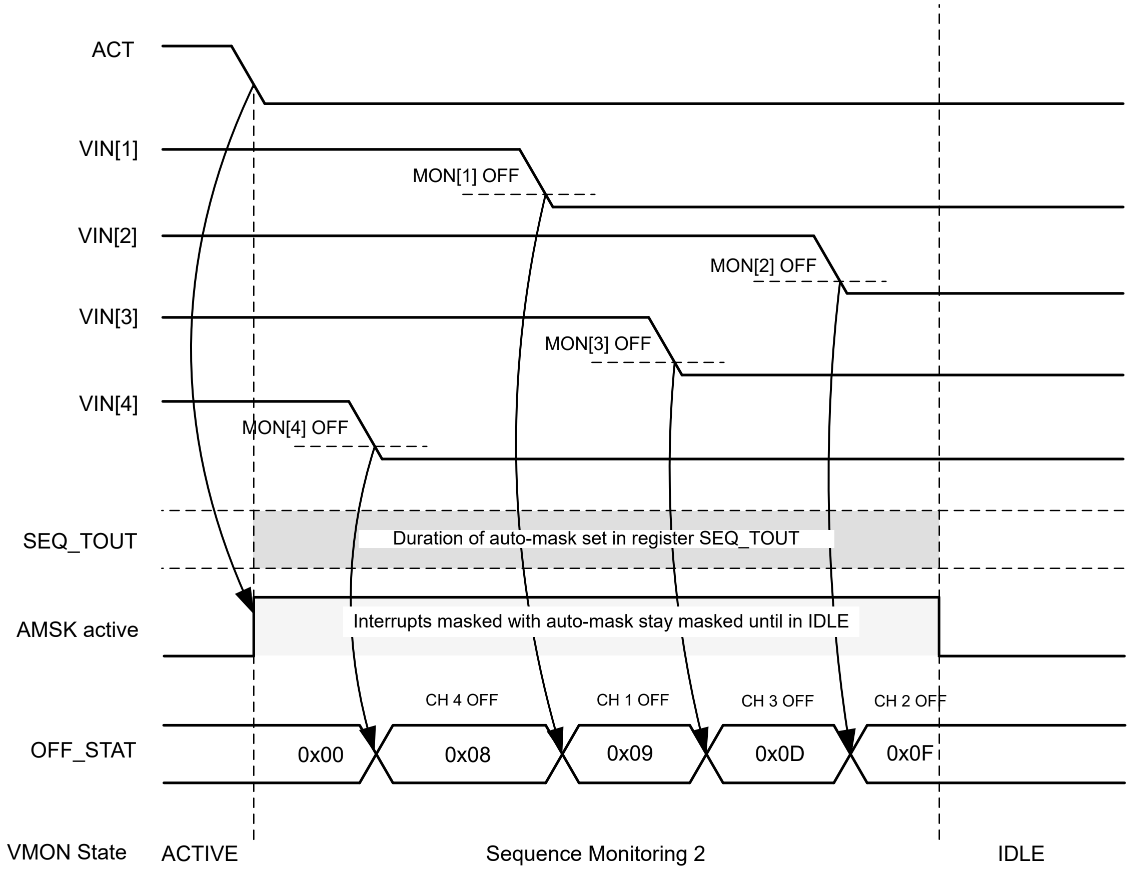

Figure 7-16. ACT 1→0 Transition

The TPS38800/TPS388R0 takes several actions on the ACT 1→0 transition:

1. After ACT 1→0 transition:
   a. All TPS38800/TPS388R0 inputs selected with auto-mask register AMSK_OFF are set with masked (disabled) interrupts for UVHF conditions.
2. After SEQ_TOUT timeout:
   a. All UVHF interrupts are masked (disabled) .
   b. If TEST_CFG.AT_SHDN register bit is set, BIST is executed (next state depends on BIST results).
   c. If TEST_CFG.AT_SHDN register bit is no set, the TPS38800/TPS388R0 enters IDLE state.

7.5 Register Maps

7.5.1 Registers Overview

The register map is designed to support up to 16 channels through register banks, with the following organization:

- Bank 0 - Status Register Set Summary:
  - Vendor info and usage registers (bank independent)
  - Interrupt registers
  - Status registers
  - Bank selection register (bank independent)
  - Protection registers (bank independent)
  - Device configuration registers (bank independent)
- Bank 1 - Channel 1-8 Configuration Register Set Summary:
  - Vendor info and usage registers (bank independent)
  - Control registers (device global registers)
  - Monitor configuration registers (channel specific registers)
  - Sequence configuration registers (both device global and channel specific registers)
  - Bank selection register (bank independent)
  - Protection registers (bank independent)
  - Device configuration registers (bank independent)

Bank independent registers are accessible at the same address irrespective of the current bank selection. Access to other registers requires the proper bank being selected.

All registers are 8-bit wide, and are loaded at boot with the default value described here or with the OTP value programmed at the factory.

Unused registers addresses are reserved for future use and support up to 16 channels.

Write accesses to protected registers (see PROT1/2 details), invalid registers, or valid registers with invalid data, are NACK'd.

7.5.1.1 BANK0 Registers

Table 7-4 lists the memory-mapped registers for the BANK0 registers. All register offset addresses not listed in Table 7-4 should be considered as reserved locations and the register contents should not be modified.

Table 7-4. BANK0 Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	INT_SRC	F_OTHER	RESERVED				TEST	CONTROL	MONITOR
11h	INT_MONITOR	RESERVED					OVHF	RESERVED	UVHF
12h	INT_UVHF	F_UVHF[8]	F_UVHF[7]	F_UVHF[6]	F_UVHF[5]	F_UVHF[4]	F_UVHF[3]	F_UVHF[2]	F_UVHF[1]
16h	INT_OVHF	F_OVHF[8]	F_OVHF[7]	F_OVHF[6]	F_OVHF[5]	F_OVHF[4]	F_OVHF[3]	F_OVHF[2]	F_OVHF[1]
22h	INT_CONTROL	RESERVED			F_CRC	F_NIRQ	F_TSD	RESERVED	F_PEC
23h	INT_TEST	RESERVED				ECC_SEC	ECC_DED	BIST_Complete_INT	BIST_Fail_INT
24h	INT_VENDOR	Self-Test_CRC	LDO_OV_Error	NRST_MISMATCH	Freq_DEV_Error	SHORT_DET	OPEN_DET	RESERVED	
30h	VMON_STAT	FAILSAFE	ST_BIST_C	ST_VDD	ST_NIRQ	RSVD	ACTIVE	RESERVED	
31h	TEST_INFO	RESERVED		ECC_SEC	ECC_DED	BIST_VM	BIST_NVM	BIST_L	BIST_A
32h	OFF_STAT	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
90h	SEQ_TIME_MSB[1]	CLOCK[7:0]							

Table 7-4. BANK0 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h	SEQ_TIME_LSB[1]	CLOCK[7:0]							
92h	SEQ_TIME_MSB[2]	CLOCK[7:0]							
93h	SEQ_TIME_LSB[2]	CLOCK[7:0]							
94h	SEQ_TIME_MSB[3]	CLOCK[7:0]							
95h	SEQ_TIME_LSB[3]	CLOCK[7:0]							
96h	SEQ_TIME_MSB[4]	CLOCK[7:0]							
97h	SEQ_TIME_LSB[4]	CLOCK[7:0]							
98h	SEQ_TIME_MSB[5]	CLOCK[7:0]							
99h	SEQ_TIME_LSB[5]	CLOCK[7:0]							
9Ah	SEQ_TIME_MSB[6]	CLOCK[7:0]							
9Bh	SEQ_TIME_LSB[6]	CLOCK[7:0]							
9Ch	SEQ_TIME_MSB[7]	CLOCK[7:0]							
9Dh	SEQ_TIME_LSB[7]	CLOCK[7:0]							
9Eh	SEQ_TIME_MSB[8]	CLOCK[7:0]							
9Fh	SEQ_TIME_LSB[8]	CLOCK[7:0]							
F0h	BANK_SEL	RESERVED							BANK_Select
F1h	PROT1	RESERVED		WRKC	RESERVED	CFG	IEN	MON	RESERVED
F2h	PROT2	RESERVED		WRKC	RESERVED	CFG	IEN	MON	RESERVED
F3h	PROT_MON	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
F9h	I2CADDR	RESERVED	ADDR_NVM[3:0]				ADDR_STRAP[2:0]		
FAh	DEV_CFG	RESERVED							RESERVED

Complex bit access types are encoded to fit into small table cells. Table 7-5 shows the codes that are used for access types in this section.

Table 7-5. BANK0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

7.5.1.1.1 INT_SRC Register (Offset = 10h) [Reset = X0h]

INT_SRC is shown in Table 7-6.

Return to the Summary Table.

Global Interrupt Source Status register.

Table 7-6. INT_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	F_OTHER	R	0h	Vendor internal defined faults. Details reported in INT_Vendor. Represents ORed value of all bits in INT_Vendor. 0 = No Vendor defined faults detected 1 = Vendor defined faults detected
6-3	RESERVED	R	0h	Reserved
2	TEST	R	Xh	Internal test or configuration load fault. Details reported in INT_TEST. Represents ORed value of all bits in INT_TEST. 0 = No test/configuration fault detected 1 = Test/configuration fault detected
1	CONTROL	R	Xh	Control status or communication fault. Details reported in INT_CONTROL. Represents ORed value of all bits in INT_CONTROL. 0 = No status or communication fault detected 1 = Status or communication fault detected
0	MONITOR	R	Xh	Voltage monitor fault. Details reported in INT_MONITOR. Represents ORed value of all bits in INT_MONITOR. 0 = No voltage fault detected 1 = Voltage fault detected

7.5.1.1.2 INT_MONITOR Register (Offset = 11h) [Reset = X0h]

INT_MONITOR is shown in Table 7-7.

Return to the Summary Table.

Voltage Monitor Interrupt Status register.

Table 7-7. INT_MONITOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	OVHF	R	Xh	Over-Voltage High Frequency Fault reported by comparator based monitoring. Details reported in INT_OVHF. Represents ORed value of all bits in INT_OVHF. 0 = No OVHF fault detected 1 = OVHF fault detected
1	RESERVED	R	0h	Reserved
0	UVHF	R	Xh	Under-Voltage High Frequency Fault reported by comparator based monitoring. Details reported in INT_UVHF. Represents ORed value of all bits in INT_UVHF. 0 = No UVHF fault detected 1 = UVHF fault detected

7.5.1.1.3 INT_UVHF Register (Offset = 12h) [Reset = X0h]

INT_UVHF is shown in Table 7-8.

Return to the Summary Table.

High Frequency channel Under-Voltage Interrupt Status register.

Table 7-8. INT_UVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	F_UVHF[8]	R/W1C	0h	Under-Voltage High Frequency Fault for MON8. Trips if MON8 High Frequency signal goes below UVHF[8]. 0 = MON8 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON8 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON8 High Frequency signal is above UVHF[8]).
6	F_UVHF[7]	R/W1C	0h	Under-Voltage High Frequency Fault for MON7. Trips if MON7 High Frequency signal goes below UVHF[7]. 0 = MON7 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON7 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON7 High Frequency signal is above UVHF[7]).
5	F_UVHF[6]	R/W1C	0h	Under-Voltage High Frequency Fault for MON6. Trips if MON6 High Frequency signal goes below UVHF[6]. 0 = MON6 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON6 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON6 High Frequency signal is above UVHF[6]).
4	F_UVHF[5]	R/W1C	0h	Under-Voltage High Frequency Fault for MON5. Trips if MON5 High Frequency signal goes below UVHF[5]. 0 = MON5 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON5 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON5 High Frequency signal is above UVHF[5]).
3	F_UVHF[4]	R/W1C	Xh	Under-Voltage High Frequency Fault for MON4. Trips if MON4 High Frequency signal goes below UVHF[4]. 0 = MON4 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON4 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON4 High Frequency signal is above UVHF[4]).
2	F_UVHF[3]	R/W1C	Xh	Under-Voltage High Frequency Fault for MON3. Trips if MON3 High Frequency signal goes below UVHF[3]. 0 = MON3 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON3 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON3 High Frequency signal is above UVHF[3]).

Table 7-8. INT_UVHF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	F_UVHF[2]	R/W1C	Xh	Under-Voltage High Frequency Fault for MON2. Trips if MON2 High Frequency signal goes below UVHF[2]. 0 = MON2 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON2 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON2 High Frequency signal is above UVHF[2]).
0	F_UVHF[1]	R/W1C	Xh	Under-Voltage High Frequency Fault for MON1. Trips if MON1 High Frequency signal goes below UVHF[1]. 0 = MON1 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON1 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON1 High Frequency signal is above UVHF[1]).

7.5.1.1.4 INT_OVHF Register (Offset = 16h) [Reset = X0h]

INT_OVHF is shown in Table 7-9.

Return to the Summary Table.

High Frequency channel Over-Voltage Interrupt Status register

Table 7-9. INT_OVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	F_OVHF[8]	R/W1C	0h	Over-Voltage High Frequency Fault for MON8. Trips if MON8 High Frequency signal goes above OVHF[8]. 0 = MON8 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON8 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON8 High Frequency signal is below OVHF[8])
6	F_OVHF[7]	R/W1C	0h	Over-Voltage High Frequency Fault for MON7. Trips if MON7 High Frequency signal goes above OVHF[7]. 0 = MON7 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON7 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON7 High Frequency signal is below OVHF[7])
5	F_OVHF[6]	R/W1C	0h	Over-Voltage High Frequency Fault for MON6. Trips if MON6 High Frequency signal goes above OVHF[6]. 0 = MON6 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON6 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON6 High Frequency signal is below OVHF[6])
4	F_OVHF[5]	R/W1C	0h	Over-Voltage High Frequency Fault for MON5. Trips if MON5 High Frequency signal goes above OVHF[5]. 0 = MON5 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON5 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON5 High Frequency signal is below OVHF[5])
3	F_OVHF[4]	R/W1C	Xh	Over-Voltage High Frequency Fault for MON4. Trips if MON4 High Frequency signal goes above OVHF[4]. 0 = MON4 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON4 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON4 High Frequency signal is below OVHF[4])
2	F_OVHF[3]	R/W1C	Xh	Over-Voltage High Frequency Fault for MON3. Trips if MON3 High Frequency signal goes above OVHF[3]. 0 = MON3 has no OVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON3 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON3 High Frequency signal is below OVHF[3])

Table 7-9. INT_OVHF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	F_OVHF[2]	R/W1C	Xh	Over-Voltage High Frequency Fault for MON2. Trips if MON2 High Frequency signal goes above OVHF[2]. 0 = MON2 has no OVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON2 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON2 High Frequency signal is below OVHF[2])
0	F_OVHF[1]	R/W1C	Xh	Over-Voltage High Frequency Fault for MON1. Trips if MON1 High Frequency signal goes above OVHF[1]. 0 = MON1 has no OVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON1 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON1 High Frequency signal is below OVHF[1])

7.5.1.1.5 INT_CONTROL Register (Offset = 22h) [Reset = X0h]

INT_CONTROL is shown in Table 7-10.

Return to the Summary Table.

Control and Communication Interrupt Status register.

Table 7-10. INT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	F_CRC	R/W1C	0h	Runtime register CRC Fault: 0 = No fault detected (or IEN_CONTROL.RT_CRC is disabled) 1 = Register CRC fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit. The bit is set again during next register CRC check if the same fault is detected
3	F_NIRQ	R/W1C	Xh	Interrupt pin fault (fault bit always enabled; no enable bit available): 0 = No fault detected on NIRQ pin 1 = Low resistance path to supply detected on NIRQ pin The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the NIRQ fault condition is also removed.
2	F_TSD	R/W1C	Xh	Thermal Shutdown fault: 0 = No TSD fault detected (or IEN_CONTROL.TSD is disabled) 1 = TSD fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the TSD fault condition is also removed
1	RESERVED	R	0h	Reserved
0	F_PEC	R/W1C	Xh	Packet Error Checking fault: 0 = PEC mismatch has not occurred (or IEN_CONTROL.PEC is disabled) 1 = PEC mismatch has occurred, or VMON_MISC.REQ_PEC=1 and PEC is missing in a write transaction The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit. The bit is set again during next I2C transaction if the same fault is detected.

7.5.1.1.6 INT_TEST Register (Offset = 23h) [Reset = X0h]

INT_TEST is shown in Table 7-11.

Return to the Summary Table.

Internal Test and Configuration Load Interrupt Status register.

Table 7-11. INT_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	ECC_SEC	R/W1C	Xh	ECC single-error corrected on OTP configuration load: 0 = No single-error corrected (or IEN_TEST.ECC_SEC is disabled) 1 = Single-error corrected Write-1-to-clear clears the bit. The bit is set again during next OTP configuration load if the same fault is detected.
2	ECC_DED	R/W1C	Xh	ECC double-error detected on OTP configuration load: 0 = No double-error detected on OTP load 1 = Double-error detected on OTP load The fault bit is always enabled (there is no associated interrupt enable bit). The device is moved to a failsafe mode on double error detection.
1	BIST_Complete_INT	R/W1C	Xh	Indication of Built-In Self-Test complete: 0 = BIST not complete (or IEN_TEST.BIST_C is disabled) 1 = BIST complete Write-1-to-clear clears the bit. The bit is set again on completion of next BIST execution
0	BIST_Fail_INT	R/W1C	Xh	Built-In Self-Test fault: 0 = No BIST fault detected (or IEN_TEST.BIST is disabled) 1 = BIST fault detected Write-1-to-clear clears the bit. The bit is set again during next BIST execution if the fault is detected

7.5.1.1.7 INT_VENDOR Register (Offset = 24h) [Reset = X0h]

INT_VENDOR is shown in Table 7-12.

Return to the Summary Table.

Vendor Specific Internal Interrupt Status register.

Table 7-12. INT_VENDOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Self-Test_CRC	R/W1C	0h	Startup register CRC self-test 0 = Self-test Pass 1 = Self-test Fail Write-1-to clear
6	LDO_OV_Error	R/W1C	0h	Internal LDO Overvoltage error. 0 = No internal LDO overvoltage fault detected 1 = Internal LDO overvoltage fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the LDO fault condition is also removed.
5	NRST_MISMATCH	R/W1C	0h	Designates error due to drive state and read back. During an NRST toggle NRST mismatch is active after 2µs, NRST must exceed 0.6*VDD to be considered in a logic high state. 0 = No fault detected on NRST pin 1 = Error due to drive state and read back. The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the NRST fault condition is also removed.
4	Freq_DEV_Error	R/W1C	0h	Designates internal frequency errors. 0 = No internal frequency fault detected 1 = Internal frequency fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the frequency fault condition is also removed.
3	SHORT_DET	R/W1C	Xh	Address pin short detect. 0 = No internal address pin short fault detected 1 = Internal address pin short fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the internal address pin short fault condition is also removed.
2	OPEN_DET	R/W1C	Xh	Address pin open detect. 0 = No internal address pin open fault detected 1 = Internal address pin open fault detected The recovery of the fault condition does NOT clear the bit. The fault is only cleared when the host performs a write-1-to-clear. Write-1-to-clear clears the bit only if the internal address pin open fault condition is also removed.
1-0	RESERVED	R	0h	Reserved

7.5.1.1.8 VMON_STAT Register (Offset = 30h) [Reset = X0h]

VMON_STAT is shown in Table 7-13.

Return to the Summary Table.

Status flags for internal operations and other non critical conditions.

Table 7-13. VMON_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAILSAFE	R	0h	1 = Device in FAILSAFE state
6	ST_BIST_C	R	0h	Built-In Self-Test state: 0 = BIST not complete 1 = BIST complete
5	ST_VDD	R	0h	Status VDD
4	ST_NIRQ	R	0h	Status NIRQ pin
3	RSVD	R	Xh	RSVD
2	ACTIVE	R	Xh	1 = Device in ACTIVE state
1-0	RESERVED	R	0h	Reserved

7.5.1.1.9 TEST_INFO Register (Offset = 31h) [Reset = X0h]

TEST_INFO is shown in Table 7-14.

Return to the Summary Table.

Internal Self-Test and ECC information.

Table 7-14. TEST_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	ECC_SEC	R	0h	Status of ECC single-error correction on OTP configuration load. 0 = no error correction applied 1 = single-error correction applied
4	ECC_DED	R	0h	Status of ECC double-error detection on OTP configuration load. 0 = no double-error detected 1 = double-error detected
3	BIST_VM	R	Xh	Status of Volatile Memory test output from BIST. 0 = Volatile Memory test pass 1 = Volatile Memory test fail
2	BIST_NVM	R	Xh	Status of Non-Volatile Memory test output from BIST. 0 = Non-Volatile Memory test pass 1 = Non-Volatile Memory test fail
1	BIST_L	R	Xh	Status of Logic test output from BIST. 0 = Logic test pass 1 = Logic test fail
0	BIST_A	R	Xh	Status of Analog test output from BIST. 0 = Analog test pass 1 = Analog test fail

7.5.1.1.10 OFF_STAT Register (Offset = 32h) [Reset = X0h]

OFF_STAT is shown in Table 7-15.

Return to the Summary Table.

Channel OFF status.

Table 7-15. OFF_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R	0h	Represents the OFF status of each channel: 0 = channel 8 is NOT OFF 1 = channel 8 is OFF (below OFF threshold)
6	MON[7]	R	0h	Represents the OFF status of each channel: 0 = channel 7 is NOT OFF 1 = channel 7 is OFF (below OFF threshold)
5	MON[6]	R	0h	Represents the OFF status of each channel: 0 = channel 6 is NOT OFF 1 = channel 6 is OFF (below OFF threshold)
4	MON[5]	R	0h	Represents the OFF status of each channel: 0 = channel 5 is NOT OFF 1 = channel 5 is OFF (below OFF threshold)
3	MON[4]	R	Xh	Represents the OFF status of each channel: 0 = channel 4 is NOT OFF 1 = channel 4 is OFF (below OFF threshold)
2	MON[3]	R	Xh	Represents the OFF status of each channel: 0 = channel 3 is NOT OFF 1 = channel 3 is OFF (below OFF threshold)
1	MON[2]	R	Xh	Represents the OFF status of each channel: 0 = channel 2 is NOT OFF 1 = channel 2 is OFF (below OFF threshold)
0	MON[1]	R	Xh	Represents the OFF status of each channel: 0 = channel 1 is NOT OFF 1 = channel 1 is OFF (below OFF threshold)

7.5.1.1.11 SEQ_TIME_MSB[1] Register (Offset = 90h) [Reset = X0h]

SEQ_TIME_MSB[1] is shown in Table 7-16.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-16. SEQ_TIME_MSB[1] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 1. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[1] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.12 SEQ_TIME_LSB[1] Register (Offset = 91h) [Reset = X0h]

SEQ_TIME_LSB[1] is shown in Table 7-17.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-17. SEQ_TIME_LSB[1] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 1. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[1] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.13 SEQ_TIME_MSB[2] Register (Offset = 92h) [Reset = X0h]

SEQ_TIME_MSB[2] is shown in Table 7-18.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-18. SEQ_TIME_MSB[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 2. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[2] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.14 SEQ_TIME_LSB[2] Register (Offset = 93h) [Reset = X0h]

SEQ_TIME_LSB[2] is shown in Table 7-19.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-19. SEQ_TIME_LSB[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 2. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[2] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.15 SEQ_TIME_MSB[3] Register (Offset = 94h) [Reset = X0h]

SEQ_TIME_MSB[3] is shown in Table 7-20.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-20. SEQ_TIME_MSB[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 3. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[3] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.16 SEQ_TIME_LSB[3] Register (Offset = 95h) [Reset = X0h]

SEQ_TIME_LSB[3] is shown in Table 7-21.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-21. SEQ_TIME_LSB[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 3. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[3] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.17 SEQ_TIME_MSB[4] Register (Offset = 96h) [Reset = X0h]

SEQ_TIME_MSB[4] is shown in Table 7-22.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-22. SEQ_TIME_MSB[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 4. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[4] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.18 SEQ_TIME_LSB[4] Register (Offset = 97h) [Reset = X0h]

SEQ_TIME_LSB[4] is shown in Table 7-23.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-23. SEQ_TIME_LSB[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 4. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[4] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50μs (equal to tSEQ_LSB).

7.5.1.1.19 SEQ_TIME_MSB[5] Register (Offset = 98h) [Reset = X0h]

SEQ_TIME_MSB[5] is shown in Table 7-24.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-24. SEQ_TIME_MSB[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 5. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[5] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.20 SEQ_TIME_LSB[5] Register (Offset = 99h) [Reset = X0h]

SEQ_TIME_LSB[5] is shown in Table 7-25.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-25. SEQ_TIME_LSB[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 5. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[5] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.21 SEQ_TIME_MSB[6] Register (Offset = 9Ah) [Reset = X0h]

SEQ_TIME_MSB[6] is shown in Table 7-26.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-26. SEQ_TIME_MSB[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 6. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[6] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.22 SEQ_TIME_LSB[6] Register (Offset = 9Bh) [Reset = X0h]

SEQ_TIME_LSB[6] is shown in Table 7-27.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-27. SEQ_TIME_LSB[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 6. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[6] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.23 SEQ_TIME_MSB[7] Register (Offset = 9Ch) [Reset = X0h]

SEQ_TIME_MSB[7] is shown in Table 7-28.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-28. SEQ_TIME_MSB[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 7. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[7] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.24 SEQ_TIME_LSB[7] Register (Offset = 9Dh) [Reset = X0h]

SEQ_TIME_LSB[7] is shown in Table 7-29.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-29. SEQ_TIME_LSB[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 7. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[7] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.25 SEQ_TIME_MSB[8] Register (Offset = 9Eh) [Reset = X0h]

SEQ_TIME_MSB[8] is shown in Table 7-30.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-30. SEQ_TIME_MSB[8] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the MSB of the sequence timestamp for channel 8. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[8] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.26 SEQ_TIME_LSB[8] Register (Offset = 9Fh) [Reset = X0h]

SEQ_TIME_LSB[8] is shown in Table 7-31.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-31. SEQ_TIME_LSB[8] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK[7:0]	R	Xh	This register stores the LSB of the sequence timestamp for channel 8. The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP. The timestamp is stored when the voltage rising level passes the UV_LF[8] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01). The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10). The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

7.5.1.1.27 BANK_SEL Register (Offset = F0h) [Reset = X0h]

BANK_SEL is shown in Table 7-32.

Return to the Summary Table.

Bank Select.

Table 7-32. BANK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	BANK_Select	R/W	Xh	Represents bank selection. 0 = Bank 0 1 = Bank 1

7.5.1.1.28 PROT1 Register (Offset = F1h) [Reset = X0h]

PROT1 is shown in Table 7-33.

Return to the Summary Table.

Locks or unlocks register changes. Must match PROT2.

Table 7-33. PROT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	WRKC	R/W	0h	Represents Protection from writes for WRKC group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
4	RESERVED	R	0h	Reserved
3	CFG	R/W	Xh	Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
2	IEN	R/W	Xh	Represents Protection from writes for IEN group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
1	MON	R/W	Xh	Represents Protection from writes for MON group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
0	RESERVED	R	0h	Reserved

7.5.1.1.29 PROT2 Register (Offset = F2h) [Reset = X0h]

PROT2 is shown in Table 7-34.

Return to the Summary Table.

Locks or unlocks register changes. Must match PROT1.

Table 7-34. PROT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	WRKC	R/W	0h	Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
4	RESERVED	R	0h	Reserved
3	CFG	R/W	Xh	Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
2	IEN	R/W	Xh	Represents Protection from writes for IEN group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
1	MON	R/W	Xh	Represents Protection from writes for MON group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
0	RESERVED	R	0h	Reserved

7.5.1.1.30 PROT_MON Register (Offset = F3h) [Reset = X0h]

PROT_MON is shown in Table 7-35.

Return to the Summary Table.

Locks MON registers in tandem with PROT1 and PROT2.

Table 7-35. PROT_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	Protects MON8 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
6	MON[7]	R/W	0h	Protects MON7 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
5	MON[6]	R/W	0h	Protects MON6 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
4	MON[5]	R/W	0h	Protects MON5 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
3	MON[4]	R/W	Xh	Protects MON4 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
2	MON[3]	R/W	Xh	Protects MON3 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
1	MON[2]	R/W	Xh	Protects MON2 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
0	MON[1]	R/W	Xh	Protects MON1 from writes along with PROT1 and PROT1. 0= Changes are possible 1= Changes are not possible

7.5.1.1.31 I2CADDR Register (Offset = F9h) [Reset = X0h]

I2CADDR is shown in Table 7-36.

Return to the Summary Table.

I2C Address

Table 7-36. I2CADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-3	ADDR_NVM[3:0]	R	Xh	Represents I2C address from internal OTP.
2-0	ADDR_STRAP[2:0]	R	Xh	Represents I2C address from resistor value on ADDR pin.

7.5.1.1.32 DEV_CFG Register (Offset = FAh) [Reset = X0h]

DEV_CFG is shown in Table 7-37.

Return to the Summary Table.

Status of I2C interface voltage levels.

Table 7-37. DEV_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.5.1.2 BANK1 Registers

Table 7-38 lists the memory-mapped registers for the BANK1 registers. All register offset addresses not listed in Table 7-38 should be considered as reserved locations and the register contents should not be modified.

Table 7-38. BANK1 Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	VMON_CTL	RESERVED				RESET_PROT	RESERVED		FORCE_NIRQ_LOW
11h	VMON_MISC	RESERVED						REQ_PEC	EN_PEC
12h	TEST_CFG	RESERVED					AT_SHDN	AT_POR[1]	AT_POR[0]
13h	IEN_UVHF	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
15h	IEN_OVHF	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
1Bh	IEN_CONTROL	RESERVED			RT_CRC_Int	RESERVED	TSD_INT	RESERVED	PEC_INT
1Ch	IEN_TEST	RESERVED				ECC_SEC	RESERVED	BIST_Complete_INT	BIST_Fail_INT
1Dh	IEN_VENDOR	Startup Self-Test_CRC	RESERVED	NRST_MISMATCH	RESERVED				
1Eh	MON_CH_EN	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
1Fh	VRANGE_MULT	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
20h	UV_HF[1]	THRESHOLD[7:0]							
21h	OV_HF[1]	THRESHOLD[7:0]							
24h	FLT_HF[1]	OV_DEB[3:0]				UV_DEB[3:0]			
25h	FC_LF[1]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
30h	UV_HF[2]	THRESHOLD[7:0]							
31h	OV_HF[2]	THRESHOLD[7:0]							
34h	FLT_HF[2]	OV_DEB[3:0]				UV_DEB[3:0]			
35h	FC_LF[2]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
40h	UV_HF[3]	THRESHOLD[7:0]							
41h	OV_HF[3]	THRESHOLD[7:0]							
44h	FLT_HF[3]	OV_DEB[3:0]				UV_DEB[3:0]			
45h	FC_LF[3]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
50h	UV_HF[4]	THRESHOLD[7:0]							
51h	OV_HF[4]	THRESHOLD[7:0]							
54h	FLT_HF[4]	OV_DEB[3:0]				UV_DEB[3:0]			
55h	FC_LF[4]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
60h	UV_HF[5]	THRESHOLD[7:0]							

Table 7-38. BANK1 Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
61h	OV_HF[5]	THRESHOLD[7:0]							
64h	FLT_HF[5]	OV_DEB[3:0]				UV_DEB[3:0]			
65h	FC_LF[5]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
70h	UV_HF[6]	THRESHOLD[7:0]							
71h	OV_HF[6]	THRESHOLD[7:0]							
74h	FLT_HF[6]	OV_DEB[3:0]				UV_DEB[3:0]			
75h	FC_LF[6]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
80h	UV_HF[7]	THRESHOLD[7:0]							
81h	OV_HF[7]	THRESHOLD[7:0]							
84h	FLT_HF[7]	OV_DEB[3:0]				UV_DEB[3:0]			
85h	FC_LF[7]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
90h	UV_HF[8]	THRESHOLD[7:0]							
91h	OV_HF[8]	THRESHOLD[7:0]							
94h	FLT_HF[8]	OV_DEB[3:0]				UV_DEB[3:0]			
95h	FC_LF[8]	RESERVED			OVHF_TO_NRST	UVHF_TO_NRST	RESERVED		
9Fh	TI_CONTROL	ENTER_BIST	RESERVED	I2C_MR	RESERVED		RST_DLY[2:0]		
A1h	AMSK_ON	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RESERVED
A2h	AMSK_OFF	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
A3h	AMSK_EXS	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
A4h	AMSK_ENS	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]
F0h	BANK_SEL	RESERVED							BANK_Select

Complex bit access types are encoded to fit into small table cells. Table 7-39 shows the codes that are used for access types in this section.

Table 7-39. BANK1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1.2.1 VMON_CTL Register (Offset = 10h) [Reset = X0h]

VMON_CTL is shown in Table 7-40.

Return to the Summary Table.

VMON device control register.

Table 7-40. VMON_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	RESET_PROT	R/W	Xh	Reset_Prot = read 0, write 1 to clear Protection registers
2-1	RESERVED	R	0h	Reserved
0	FORCE_NIRQ_LOW	R/W	Xh	Force assertion of NIRQ

7.5.1.2.2 VMON_MISC Register (Offset = 11h) [Reset = X0h]

VMON_MISC is shown in Table 7-41.

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Miscellaneous VMON configurations.

Table 7-41. VMON_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	REQ_PEC	R/W	Xh	Require PEC. 0 = PEC not required 1 = PEC required
0	EN_PEC	R/W	Xh	Enable PEC. 0 = PEC not enabled 1 = PEC enabled

7.5.1.2.3 TEST_CFG Register (Offset = 12h) [Reset = X0h]

TEST_CFG is shown in Table 7-42.

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Built-In Self Test (BIST) execution configuration.

Table 7-42. TEST_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	AT_SHDN	R/W	Xh	Run BIST at SHDN
1	AT_POR[1]	R/W	Xh	Run BIST at POR, 2nd bit for redundancy
0	AT_POR[0]	R/W	Xh	Run BIST at POR

7.5.1.2.4 IEN_UVHF Register (Offset = 13h) [Reset = X0h]

IEN_UVHF is shown in Table 7-43.

Return to the Summary Table.

High Frequency channel Under-Voltage Interrupt Enable register

Table 7-43. IEN_UVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	UVHF interrupt enable for MON8, 0 = Disable, 1 = Enable
6	MON[7]	R/W	0h	UVHF interrupt enable for MON7, 0 = Disable, 1 = Enable
5	MON[6]	R/W	0h	UVHF interrupt enable for MON6, 0 = Disable, 1 = Enable
4	MON[5]	R/W	0h	UVHF interrupt enable for MON5, 0 = Disable, 1 = Enable
3	MON[4]	R/W	Xh	UVHF interrupt enable for MON4, 0 = Disable, 1 = Enable
2	MON[3]	R/W	Xh	UVHF interrupt enable for MON3, 0 = Disable, 1 = Enable
1	MON[2]	R/W	Xh	UVHF interrupt enable for MON2, 0 = Disable, 1 = Enable
0	MON[1]	R/W	Xh	UVHF interrupt enable for MON1, 0 = Disable, 1 = Enable

7.5.1.2.5 IEN_OVHF Register (Offset = 15h) [Reset = X0h]

IEN_OVHF is shown in Table 7-44.

Return to the Summary Table.

High Frequency channel Over-Voltage Interrupt Enable register.

Table 7-44. IEN_OVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	OVHF interrupt enable for MON8, 0 = Disable, 1 = Enable
6	MON[7]	R/W	0h	OVHF interrupt enable for MON7, 0 = Disable, 1 = Enable
5	MON[6]	R/W	0h	OVHF interrupt enable for MON6, 0 = Disable, 1 = Enable
4	MON[5]	R/W	0h	OVHF interrupt enable for MON5, 0 = Disable, 1 = Enable
3	MON[4]	R/W	Xh	OVHF interrupt enable for MON4, 0 = Disable, 1 = Enable
2	MON[3]	R/W	Xh	OVHF interrupt enable for MON3, 0 = Disable, 1 = Enable
1	MON[2]	R/W	Xh	OVHF interrupt enable for MON2, 0 = Disable, 1 = Enable
0	MON[1]	R/W	Xh	OVHF interrupt enable for MON1, 0 = Disable, 1 = Enable

7.5.1.2.6 IEN_CONTROL Register (Offset = 1Bh) [Reset = X0h]

IEN_CONTROL is shown in Table 7-45.

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Control and Communication Fault Interrupt Enable register.

Table 7-45. IEN_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	RT_CRC_Int	R/W	0h	Register Run time CRC (Cyclic Redundancy Checking) error Interrupt is a static CRC perfomed on the register map content. If enabled there does not need to be any data read or write for this CRC check to occur. The puropose of this CRC is to identify if a static bit flip or random error in the register map content has occured. This is the safety mechanism is carried out using a CRC-8 polynomial, in the case of a read or write operation the register map content changes and the polynomial is re-calculated with the new value after the changes. Interrupt is reported in INT_CONTROL_F_CRC register of Bank 0. 0 = Disable Interrupt Mapping, 1 = Enable Interrupt Mapping
3	RESERVED	R	0h	Reserved
2	TSD_INT	R/W	Xh	Thermal shutdown Interrupt. 0 = Disable, 1 = Enable
1	RESERVED	R	0h	Reserved
0	PEC_INT	R/W	Xh	PEC Error Interrupt. 0 = Disable, 1 = Enable

7.5.1.2.7 IEN_TEST Register (Offset = 1Ch) [Reset = X0h]

IEN_TEST is shown in Table 7-46.

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Internal Test and Configuration Load Fault Interrupt Enable register

Table 7-46. IEN_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	ECC_SEC	R/W	Xh	SEC Error Interrupt. 0 = Disable, 1 = Enable
2	RESERVED	R	0h	Reserved
1	BIST_Complete_INT	R/W	Xh	BIST complete Interrupt. 0 = Disable, 1 = Enable
0	BIST_Fail_INT	R/W	Xh	BIST Fail Interrupt. 0 = Disable, Enable = 1

7.5.1.2.8 IEN_VENDOR Register (Offset = 1Dh) [Reset = X0h]

IEN_VENDOR is shown in Table 7-47.

Return to the Summary Table.

Vendor Specific Internal Interrupt Enable register.

Table 7-47. IEN_VENDOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Startup Self-Test_CRC	R/W	0h	Startup Self-Test_CRC Interrupt. 0 = Disable Interrupt Mapping, 1 = Enable Interrupt Mapping
6	RESERVED	R	0h	Reserved
5	NRST_MISMATCH	R/W	0h	NRST mismatch Interrupt. 0 = Disable Interrupt Mapping, 1 = Enable Interrupt Mapping
4-0	RESERVED	R	0h	Reserved

7.5.1.2.9 MON_CH_EN Register (Offset = 1Eh) [Reset = X0h]

MON_CH_EN is shown in Table 7-48.

Return to the Summary Table.

Channel Voltage Monitoring Enable.

Table 7-48. MON_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	Enables MON8 monitoring. 0 = Disabled, 1 = Enabled
6	MON[7]	R/W	0h	Enables MON7 monitoring. 0 = Disabled, 1 = Enabled
5	MON[6]	R/W	0h	Enables MON6 monitoring. 0 = Disabled, 1 = Enabled
4	MON[5]	R/W	0h	Enables MON5 monitoring. 0 = Disabled, 1 = Enabled
3	MON[4]	R/W	Xh	Enables MON4 monitoring. 0 = Disabled, 1 = Enabled
2	MON[3]	R/W	Xh	Enables MON3 monitoring. 0 = Disabled, 1 = Enabled
1	MON[2]	R/W	Xh	Enables MON2 monitoring. 0 = Disabled, 1 = Enabled
0	MON[1]	R/W	Xh	Enables MON1 monitoring. 0 = Disabled, 1 = Enabled

7.5.1.2.10 VRANGE_MULT Register (Offset = 1Fh) [Reset = X0h]

VRANGE_MULT is shown in Table 7-49.

Return to the Summary Table.

Channel Voltage Monitoring Range/Scaling.

Table 7-49. VRANGE_MULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	Scalar for MON8. 0 = 1x, 1 = 4x
6	MON[7]	R/W	0h	Scalar for MON7. 0 = 1x, 1 = 4x
5	MON[6]	R/W	0h	Scalar for MON6. 0 = 1x, 1 = 4x
4	MON[5]	R/W	0h	Scalar for MON5. 0 = 1x, 1 = 4x
3	MON[4]	R/W	Xh	Scalar for MON4. 0 = 1x, 1 = 4x
2	MON[3]	R/W	Xh	Scalar for MON3. 0 = 1x, 1 = 4x
1	MON[2]	R/W	Xh	Scalar for MON2. 0 = 1x, 1 = 4x
0	MON[1]	R/W	Xh	Scalar for MON1. 0 = 1x, 1 = 4x

7.5.1.2.11 UV_HF[1] Register (Offset = 20h) [Reset = X0h]

UV_HF[1] is shown in Table 7-50.

Return to the Summary Table.

Channel 1 High Frequency channel Under-Voltage threshold.

Table 7-50. UV_HF[1] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.12 OV_HF[1] Register (Offset = 21h) [Reset = X0h]

OV_HF[1] is shown in Table 7-51.

Return to the Summary Table.

Channel 1 High Frequency channel Over-Voltage threshold.

Table 7-51. OV_HF[1] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.13 FLT_HF[1] Register (Offset = 24h) [Reset = X0h]

FLT_HF[1] is shown in Table 7-52.

Return to the Summary Table.

Channel 1 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-52. FLT_HF[1] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.14 FC_LF[1] Register (Offset = 25h) [Reset = X0h]

FC_LF[1] is shown in Table 7-53.

Return to the Summary Table.

Channel 1 UV and OV mapping to NRST error output

Table 7-53. FC_LF[1] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON1 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON1 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.15 UV_HF[2] Register (Offset = 30h) [Reset = X0h]

UV_HF[2] is shown in Table 7-54.

Return to the Summary Table.

Channel 2 High Frequency channel Under-Voltage threshold.

Table 7-54. UV_HF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.16 OV_HF[2] Register (Offset = 31h) [Reset = X0h]

OV_HF[2] is shown in Table 7-55.

Return to the Summary Table.

Channel 2 High Frequency channel Over-Voltage threshold.

Table 7-55. OV_HF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.17 FLT_HF[2] Register (Offset = 34h) [Reset = X0h]

FLT_HF[2] is shown in Table 7-56.

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Channel 2 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-56. FLT_HF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.18 FC_LF[2] Register (Offset = 35h) [Reset = X0h]

FC_LF[2] is shown in Table 7-57.

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Channel 2 UV and OV mapping to NRST error output

Table 7-57. FC_LF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON2 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON2 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.19 UV_HF[3] Register (Offset = 40h) [Reset = X0h]

UV_HF[3] is shown in Table 7-58.

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Channel 3 High Frequency channel Under-Voltage threshold.

Table 7-58. UV_HF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.20 OV_HF[3] Register (Offset = 41h) [Reset = X0h]

OV_HF[3] is shown in Table 7-59.

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Channel 3 High Frequency channel Over-Voltage threshold.

Table 7-59. OV_HF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.21 FLT_HF[3] Register (Offset = 44h) [Reset = X0h]

FLT_HF[3] is shown in Table 7-60.

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Channel 3 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-60. FLT_HF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.22 FC_LF[3] Register (Offset = 45h) [Reset = X0h]

FC_LF[3] is shown in Table 7-61.

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Channel 3 UV and OV mapping to NRST error output

Table 7-61. FC_LF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON3 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON3 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.23 UV_HF[4] Register (Offset = 50h) [Reset = X0h]

UV_HF[4] is shown in Table 7-62.

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Channel 4 High Frequency channel Under-Voltage threshold.

Table 7-62. UV_HF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.24 OV_HF[4] Register (Offset = 51h) [Reset = X0h]

OV_HF[4] is shown in Table 7-63.

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Channel 4 High Frequency channel Over-Voltage threshold.

Table 7-63. OV_HF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.25 FLT_HF[4] Register (Offset = 54h) [Reset = X0h]

FLT_HF[4] is shown in Table 7-64.

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Channel 4 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-64. FLT_HF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1μs 1000b = 25.6μs 0001b = 0.2μs 1001b = 51.2μs 0010b = 0.4μs 1010b = 102.4μs 0011b = 0.8μs 1011b = 102.4μs 0100b = 1.6μs 1100b = 102.4μs 0101b = 3.2μs 1101b = 102.4μs 0110b = 6.4μs 1110b = 102.4μs 0111b = 12.8μs 1111b = 102.4μs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1μs 1000b = 25.6μs 0001b = 0.2μs 1001b = 51.2μs 0010b = 0.4μs 1010b = 102.4μs 0011b = 0.8μs 1011b = 102.4μs 0100b = 1.6μs 1100b = 102.4μs 0101b = 3.2μs 1101b = 102.4μs 0110b = 6.4μs 1110b = 102.4μs 0111b = 12.8μs 1111b = 102.4μs

7.5.1.2.26 FC_LF[4] Register (Offset = 55h) [Reset = X0h]

FC_LF[4] is shown in Table 7-65.

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Channel 4 UV and OV mapping to NRST error output

Table 7-65. FC_LF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON4 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON4 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.27 UV_HF[5] Register (Offset = 60h) [Reset = X0h]

UV_HF[5] is shown in Table 7-66.

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Channel 5 High Frequency channel Under-Voltage threshold.

Table 7-66. UV_HF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.28 OV_HF[5] Register (Offset = 61h) [Reset = X0h]

OV_HF[5] is shown in Table 7-67.

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Channel 5 High Frequency channel Over-Voltage threshold.

Table 7-67. OV_HF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.29 FLT_HF[5] Register (Offset = 64h) [Reset = X0h]

FLT_HF[5] is shown in Table 7-68.

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Channel 5 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-68. FLT_HF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.30 FC_LF[5] Register (Offset = 65h) [Reset = X0h]

FC_LF[5] is shown in Table 7-69.

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Channel 5 UV and OV mapping to NRST error output

Table 7-69. FC_LF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON5 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON5 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.31 UV_HF[6] Register (Offset = 70h) [Reset = X0h]

UV_HF[6] is shown in Table 7-70.

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Channel 6 High Frequency channel Under-Voltage threshold.

Table 7-70. UV_HF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.32 OV_HF[6] Register (Offset = 71h) [Reset = X0h]

OV_HF[6] is shown in Table 7-71.

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Channel 6 High Frequency channel Over-Voltage threshold.

Table 7-71. OV_HF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.33 FLT_HF[6] Register (Offset = 74h) [Reset = X0h]

FLT_HF[6] is shown in Table 7-72.

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Channel 6 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-72. FLT_HF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.34 FC_LF[6] Register (Offset = 75h) [Reset = X0h]

FC_LF[6] is shown in Table 7-73.

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Channel 6 UV and OV mapping to NRST error output

Table 7-73. FC_LF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON6 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON6 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.35 UV_HF[7] Register (Offset = 80h) [Reset = X0h]

UV_HF[7] is shown in Table 7-74.

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Channel 7 High Frequency channel Under-Voltage threshold.

Table 7-74. UV_HF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.36 OV_HF[7] Register (Offset = 81h) [Reset = X0h]

OV_HF[7] is shown in Table 7-75.

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Channel 7 High Frequency channel Over-Voltage threshold.

Table 7-75. OV_HF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.37 FLT_HF[7] Register (Offset = 84h) [Reset = X0h]

FLT_HF[7] is shown in Table 7-76.

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Channel 7 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-76. FLT_HF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.38 FC_LF[7] Register (Offset = 85h) [Reset = X0h]

FC_LF[7] is shown in Table 7-77.

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Channel 7 UV and OV mapping to NRST error output

Table 7-77. FC_LF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON7 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON7 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.39 UV_HF[8] Register (Offset = 90h) [Reset = X0h]

UV_HF[8] is shown in Table 7-78.

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Channel 8 High Frequency channel Under-Voltage threshold.

Table 7-78. UV_HF[8] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.40 OV_HF[8] Register (Offset = 91h) [Reset = X0h]

OV_HF[8] is shown in Table 7-79.

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Channel 8 High Frequency channel Over-Voltage threshold.

Table 7-79. OV_HF[8] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRESHOLD[7:0]	R/W	Xh	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475 V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.41 FLT_HF[8] Register (Offset = 94h) [Reset = X0h]

FLT_HF[8] is shown in Table 7-80.

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Channel 8 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-80. FLT_HF[8] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OV_DEB[3:0]	R/W	0h	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3-0	UV_DEB[3:0]	R/W	Xh	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.42 FC_LF[8] Register (Offset = 95h) [Reset = X0h]

FC_LF[8] is shown in Table 7-81.

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Channel 8 UV and OV mapping to NRST error output

Table 7-81. FC_LF[8] Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	OVHF_TO_NRST	R/W	0h	Maps MON8 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	Xh	Maps MON8 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2-0	RESERVED	R	0h	Reserved

7.5.1.2.43 TI_CONTROL Register (Offset = 9Fh) [Reset = X0h]

TI_CONTROL is shown in Table 7-82.

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Manual BIST/Manual Reset via I2C/Reset delay

Table 7-82. TI_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENTER_BIST	R/W	0h	Manual BIST. 1 = Enter BIST
6	RESERVED	R	0h	Reserved
5	I2C_MR	R/W	0h	Manual Reset. 1 = Assert NRST low
4-3	RESERVED	R	0h	Reserved
2-0	RST_DLY[2:0]	R/W	Xh	Reset delay 000 = 200µs 001 = 1ms 010 = 10ms 011 = 16ms 100 = 20ms 101 = 70ms 110 = 100ms 111 = 200ms

7.5.1.2.44 AMSK_ON Register (Offset = A1h) [Reset = X0h]

AMSK_ON is shown in Table 7-83.

Return to the Summary Table.

Auto-mask UVHF and OVHF interrupts on power up transitions.

Table 7-83. AMSK_ON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	Automask at power on for MON8. 0 = Disabled 1 = Enabled
6	MON[7]	R/W	0h	Automask at power on for MON7. 0 = Disabled 1 = Enabled
5	MON[6]	R/W	0h	Automask at power on for MON6. 0 = Disabled 1 = Enabled
4	MON[5]	R/W	0h	Automask at power on for MON5. 0 = Disabled 1 = Enabled
3	MON[4]	R/W	Xh	Automask at power on for MON4. 0 = Disabled 1 = Enabled
2	MON[3]	R/W	Xh	Automask at power on for MON3. 0 = Disabled 1 = Enabled
1	MON[2]	R/W	Xh	Automask at power on for MON2. 0 = Disabled 1 = Enabled
1	MON[1]	R/W	Xh	Automask at power on for MON1. 0 = Disabled 1 = Enabled
0	RESERVED	R	0h	

7.5.1.2.45 AMSK_OFF Register (Offset = A2h) [Reset = X0h]

AMSK_OFF is shown in Table 7-84.

Return to the Summary Table.

Auto-mask UVHF and OVHF interrupts on power down transitions.

Table 7-84. AMSK_OFF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	Automask at power off for MON8. 0 = Disabled 1 = Enabled
6	MON[7]	R/W	0h	Automask at power off for MON7. 0 = Disabled 1 = Enabled
5	MON[6]	R/W	0h	Automask at power off for MON6. 0 = Disabled 1 = Enabled
4	MON[5]	R/W	0h	Automask at power off for MON5. 0 = Disabled 1 = Enabled
3	MON[4]	R/W	Xh	Automask at power off for MON4. 0 = Disabled 1 = Enabled
2	MON[3]	R/W	Xh	Automask at power off for MON3. 0 = Disabled 1 = Enabled
1	MON[2]	R/W	Xh	Automask at power off for MON2. 0 = Disabled 1 = Enabled
0	MON[1]	R/W	Xh	Automask at power off for MON1. 0 = Disabled 1 = Enabled

7.5.1.2.46 AMSK_EXS Register (Offset = A3h) [Reset = X0h]

AMSK_EXS is shown in Table 7-85.

Return to the Summary Table.

Auto-mask UVHF and OVHF interrupts on exit sleep transitions.

Table 7-85. AMSK_EXS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	Automask at exit sleep for MON8. 0 = Disabled 1 = Enabled
6	MON[7]	R/W	0h	Automask at exit sleep for MON7. 0 = Disabled 1 = Enabled
5	MON[6]	R/W	0h	Automask at exit sleep for MON6. 0 = Disabled 1 = Enabled
4	MON[5]	R/W	0h	Automask at exit sleep for MON5. 0 = Disabled 1 = Enabled
3	MON[4]	R/W	Xh	Automask at exit sleep for MON4. 0 = Disabled 1 = Enabled
2	MON[3]	R/W	Xh	Automask at exit sleep for MON3. 0 = Disabled 1 = Enabled
1	MON[2]	R/W	Xh	Automask at exit sleep for MON2. 0 = Disabled 1 = Enabled
0	MON[1]	R/W	Xh	Automask at exit sleep for MON1. 0 = Disabled 1 = Enabled

7.5.1.2.47 AMSK_ENS Register (Offset = A4h) [Reset = X0h]

AMSK_ENS is shown in Table 7-86.

Return to the Summary Table.

Auto-mask UVHF and OVHF interrupts on enter sleep transitions.

Table 7-86. AMSK_ENS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MON[8]	R/W	0h	Automask at enter sleep for MON8. 0 = Disabled 1 = Enabled
6	MON[7]	R/W	0h	Automask at enter sleep for MON7. 0 = Disabled 1 = Enabled
5	MON[6]	R/W	0h	Automask at enter sleep for MON6. 0 = Disabled 1 = Enabled
4	MON[5]	R/W	0h	Automask at enter sleep for MON5. 0 = Disabled 1 = Enabled
3	MON[4]	R/W	Xh	Automask at enter sleep for MON4. 0 = Disabled 1 = Enabled
2	MON[3]	R/W	Xh	Automask at enter sleep for MON3. 0 = Disabled 1 = Enabled
1	MON[2]	R/W	Xh	Automask at enter sleep for MON2. 0 = Disabled 1 = Enabled
0	MON[1]	R/W	Xh	Automask at enter sleep for MON1. 0 = Disabled 1 = Enabled

7.5.1.2.48 BANK_SEL Register (Offset = F0h) [Reset = X0h]

BANK_SEL is shown in Table 7-87.

Return to the Summary Table.

Bank Select.

Table 7-87. BANK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	BANK_Select	R/W	Xh	Represents bank selection. 0 = Bank 0 1 = Bank 1

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the application accuracy or completeness. TI's customers are responsible for determining components for the customer's system purposes. Customers are adviced to validate and test design implementation to confirm system functionality.

8.1 Application Information

Modern SOC and FPGA devices typically have multiple power rails to provide power to the different blocks within the IC. Accurate voltage level and timing requirements are common and must be met to maintain proper operation of these devices. By utilizing TPS38800 along with a multichannel voltage sequencer, the power up and power down sequencing requirements as well as the core voltage requirements of the target SOC or FPGA device can be met. This design focuses on meeting the timing requirements for an SOC by using the TPS38800.

8.2 Typical Application

8.2.1 Multichannel Sequencer and Monitor

A typical application for the TPS38800 is shown in Figure 8-1. TPS38800 is used to provide the proper voltage monitoring for the target SOC device. A mulitchannel voltage monitor TPS38800 is used to monitor the voltage rails as these rails power up and power down to verify that the correct sequence occurs in both occasions. A safety microcontroller is also used to provide ACT, NIRQ, and I²C commands to the TPS38800 and the multichannel voltage monitor. The ACT signal from the safety microcontroller determines when the TPS38800 enters into ACTIVE or SHDN states while the NIRQ pin of the TPS38800 acts as an interrupt pin that is set when a fault has occurred. The host microcontroller can clear the fault by writing 1 to the affected register. The power rails for the safety microcontroller are not shown in Figure 8-1 for simplicity.

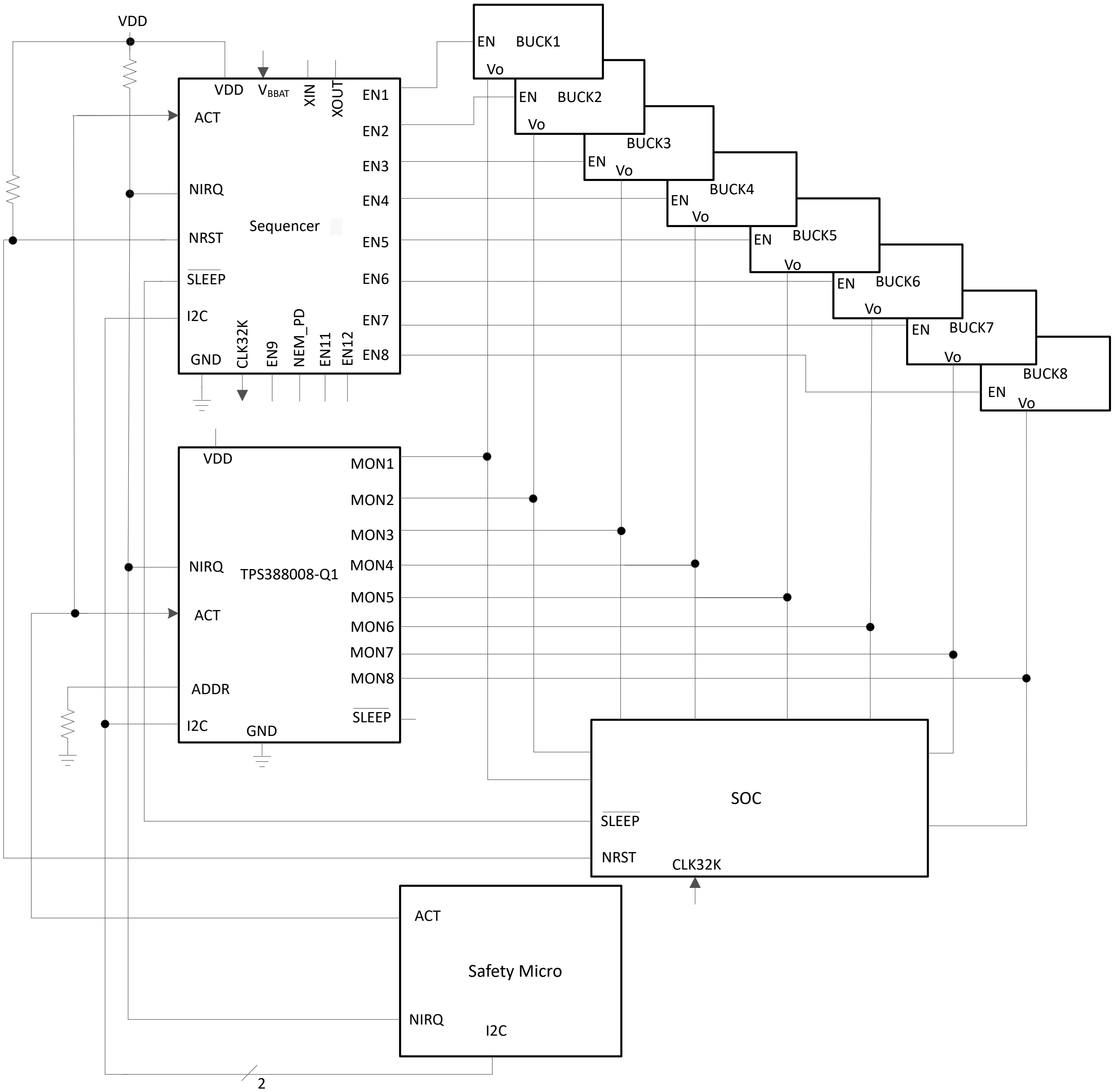


Figure 8-1. TPS38800 Voltage Monitor Design Block Diagram

8.2.2 Design Requirements

- Six different voltage rails supplied by DC/DC converters need to be properly monitored in this design.
- All detected failures in sequencing are reported via an external hardware interrupt signal.
- All detected failures are logged in internal registers and be accessible to an external processor via I^2C.

8.2.3 Detailed Design Procedure

- TPS38800/ TPS388R0 device option comes preprogrammed with default values for over voltage, under voltage, expected sequences on power up and down.
- NIRQ pin requires a pull up resistor in the range of 10kΩ to 100kΩ.
- SDA and SCL lines require pull up resistors in the range of 10kΩ.
- The ACT pin is driven by an external safety microcontroller. When the ACT pin is driven high, the device enters into ACTIVE mode. When the ACT pin is driven low, the device enters into SHDN mode.
- The safety microcontroller is used to clear fault interrupts reported through the NIRQ interrupt pin and the INT_SCR1 and INT_SCR2 registers. The interrupt flags can only be cleared by the host microcontroller with a write-1-to-clear operation; interrupt flags are not automatically cleared if the fault condition is no longer present.

8.2.4 Application Curves

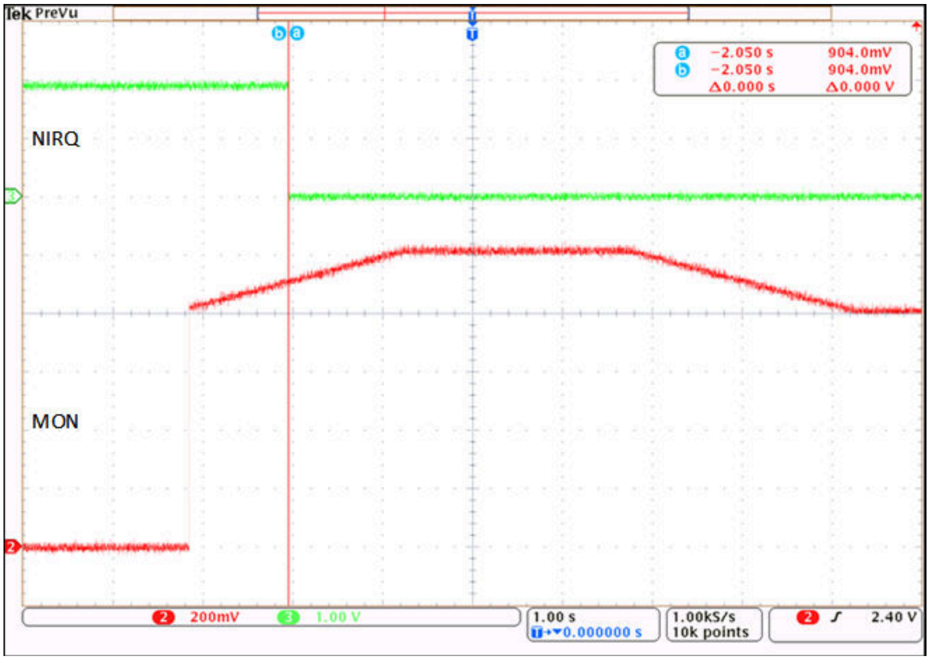


Figure 8-2. NIRQ Triggered After an Overvoltage Fault

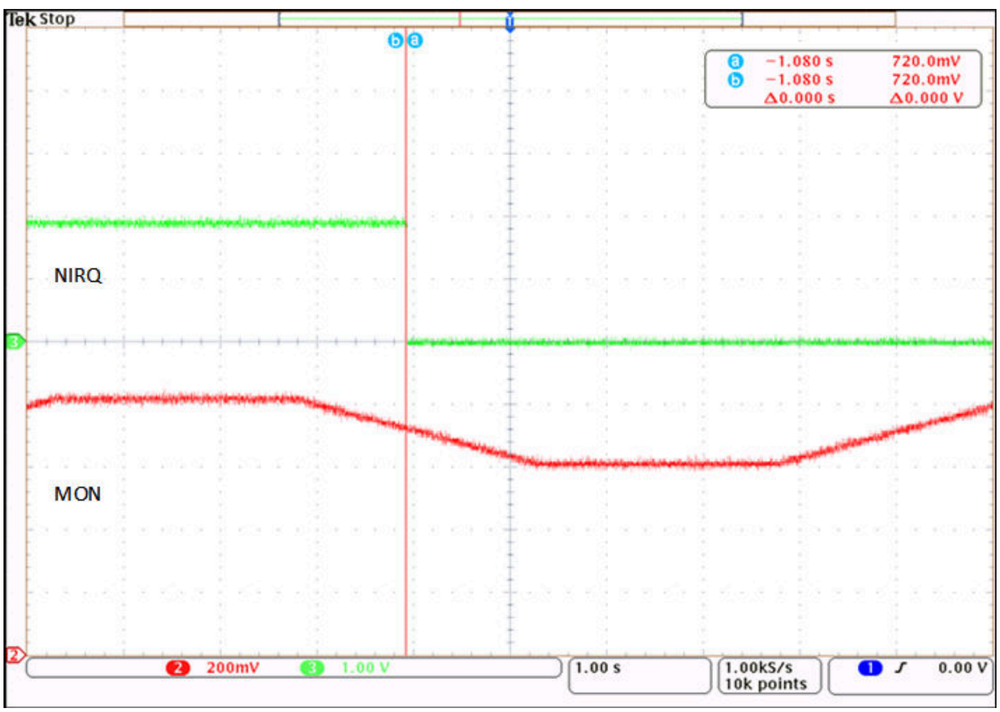


Figure 8-3. NIRQ Triggered After an Undervoltage Fault

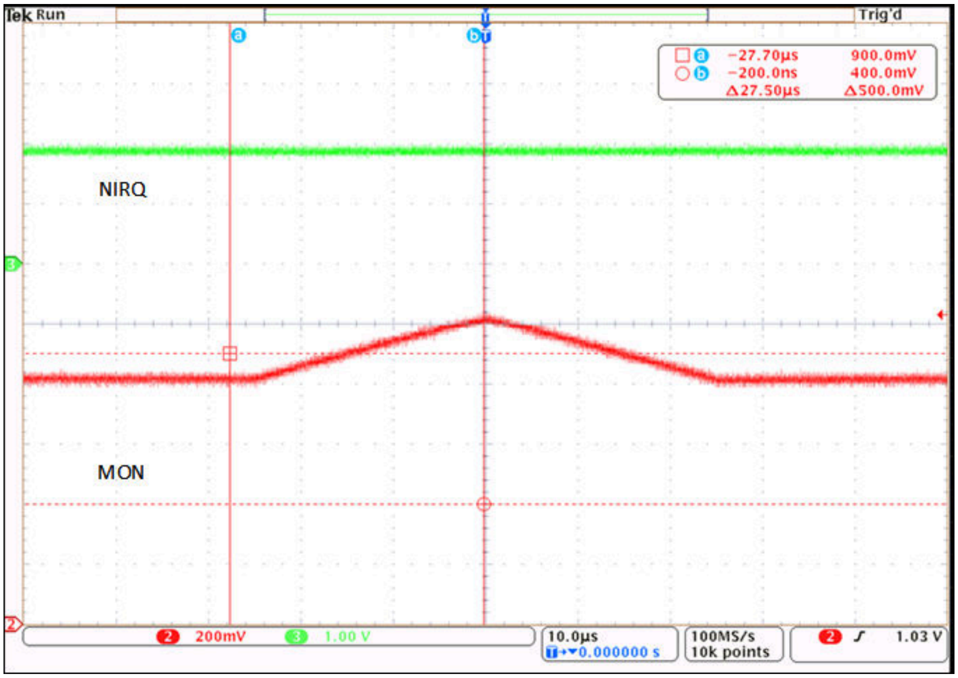


Figure 8-4. NIRQ Not Triggered on Overvoltage Fault with 51.2us OV Debounce Filter

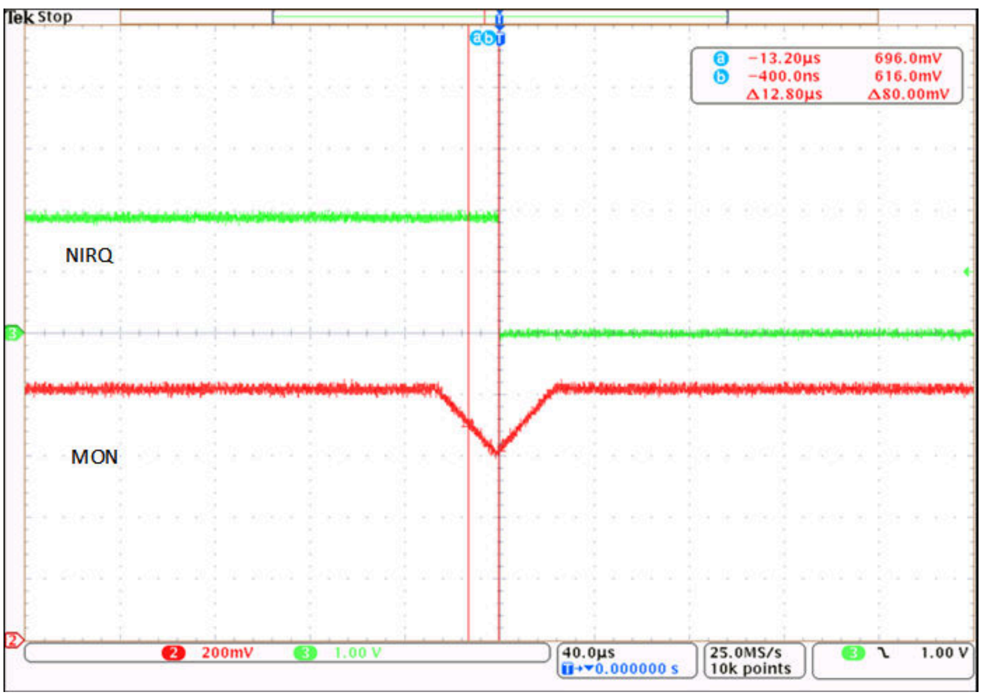


Figure 8-5. NIRQ Triggered on Undervoltage Fault with 12.8us UV Debounce Filter

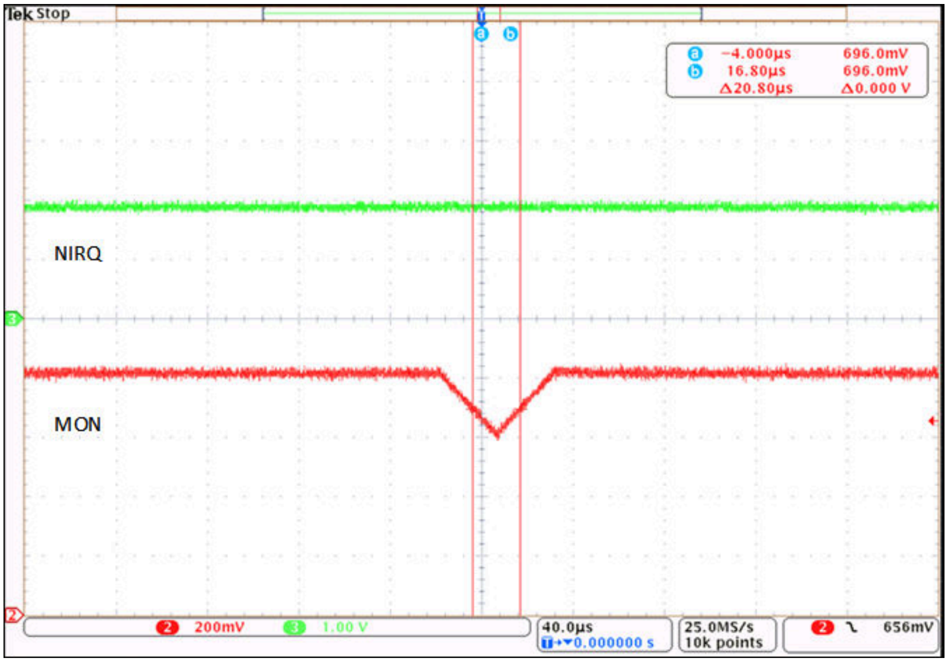


Figure 8-6. NIRQ Not Triggered on Undervoltage Fault with 25us UV Debounce Filter

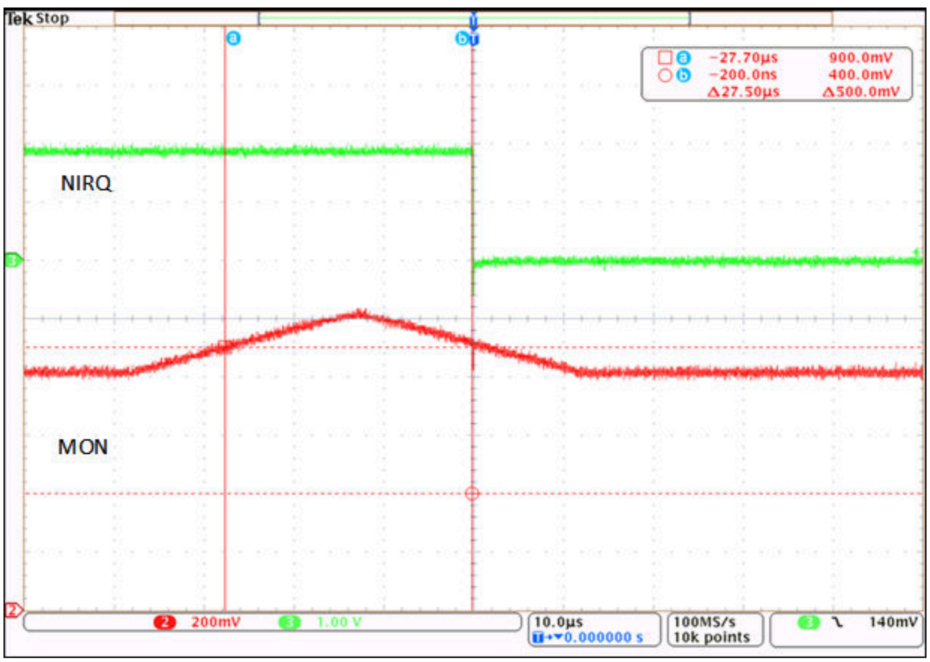


Figure 8-7. NIRQ Triggered on Overvoltage Fault with 25us OV Debounce Filter

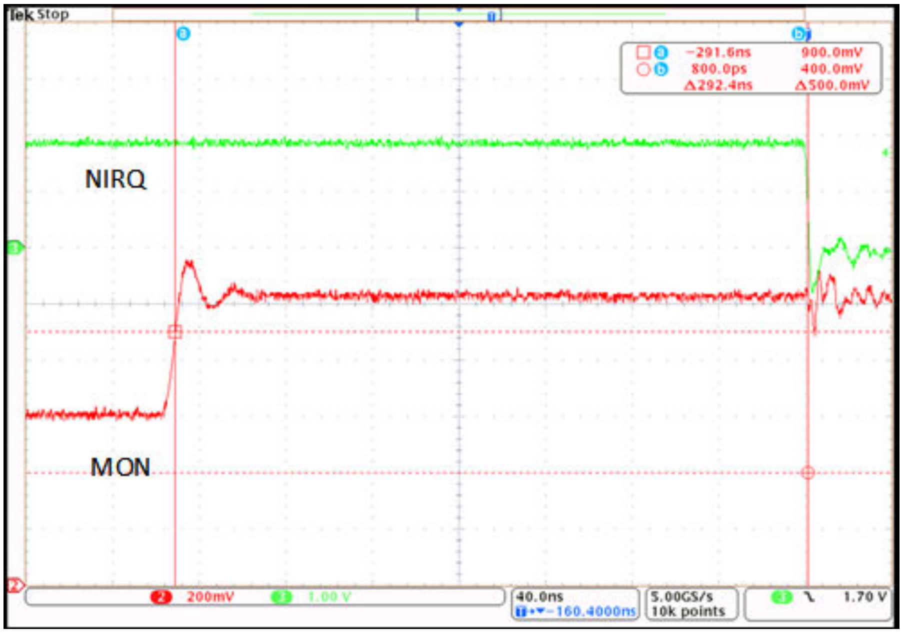


Figure 8-8. NIRQ Propagation Delay Resulting from Overvoltage Fault

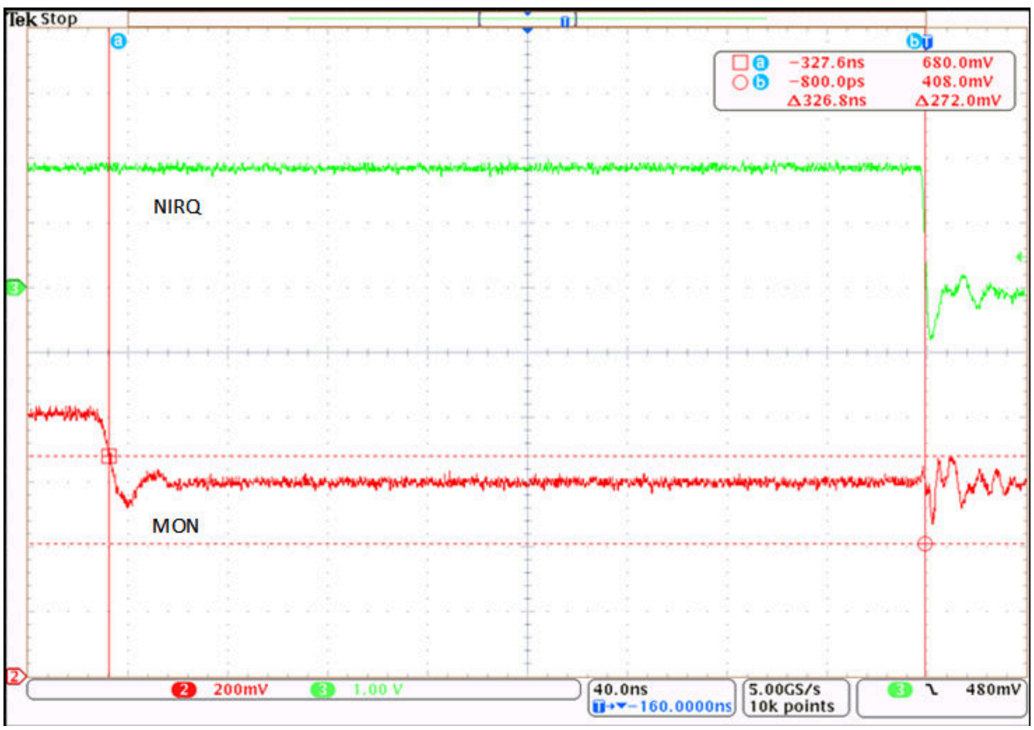


Figure 8-9. NIRQ Propagation Delay Resulting from Undervoltage Fault

9 Power Supply Recommendations

9.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 2.5V to 5.5V. TPS38800/TPS388R0 has a 6V absolute maximum rating on the VDD pin. A good analog practice is to place a 0.1μF to 1μF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See Using Voltage Supervisors in High Voltage Applications for more information.

10 Layout

10.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the MON pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- If differential voltage sensing is required for MON1 and/or MON2 route RS_1/2 pin to the point of measurement
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

10.2 Layout Example

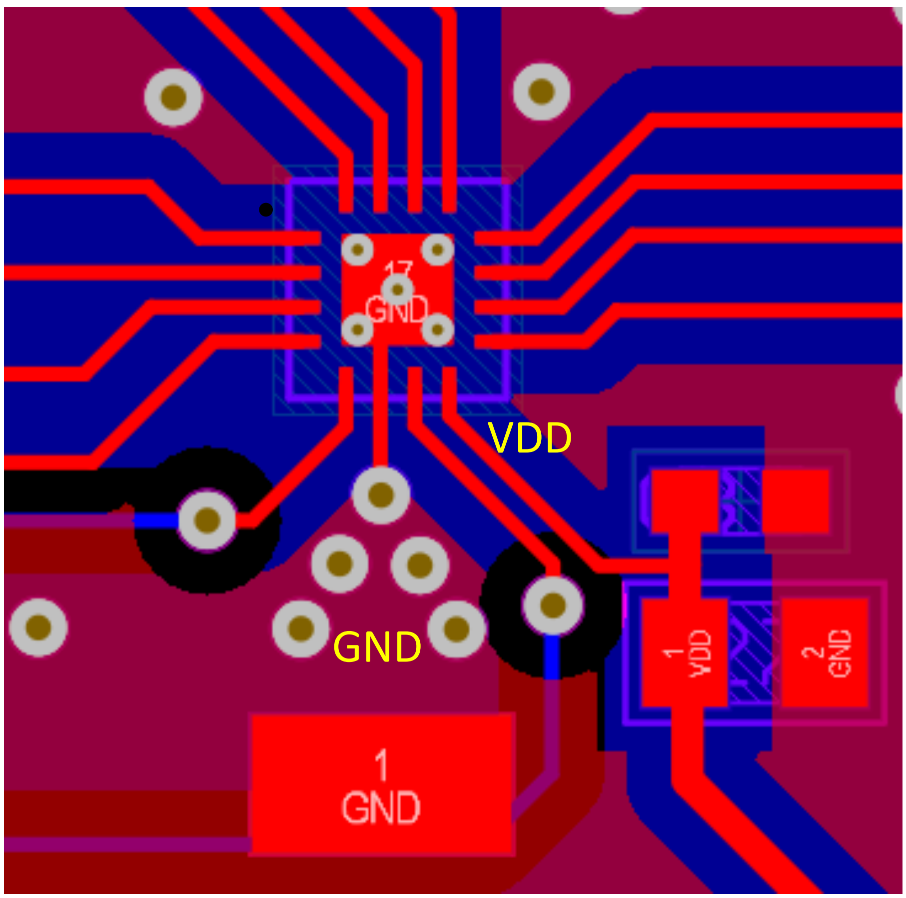


Figure 10-1. Recommended Layout

11 Device and Documentation Support

11.1 Device Nomenclature

Table 11-1 and Table 11-2 show how to decode the function of the device based on part number.

Table 11-1. Device Thresholds

ORDERING CODE	Thresholds	VMON1 (V)	VMON2 (V)	VMON3 (V)	VMON4 (V)	VMON5 (V)	VMON6 (V)	VMON7 (V)	VMON8 (V)
TPS388R02001-Q1 [1]	UV_HF/ OV_HF	1.15/1.25	3.16/3.44	N/A	N/A	N/A	N/A	N/A	N/A
TPS388R02002-Q1 [1]	UV_HF/ OV_HF	1.15/1.25	3.16/3.44	N/A	N/A	N/A	N/A	N/A	N/A
TPS388R04H01-Q1	UV_HF/ OV_HF	0.705/0.82	0.705/0.82	0.845/0.985	0.79/0.925	N/A	N/A	N/A	N/A
TPS388R04H00-Q1	UV_HF/ OV_HF	0.705/0.82	0.705/0.82	0.725/0.84	0.685/0.80	N/A	N/A	N/A	N/A
TPS388008001RTER	UV_HF/ OV_HF	0.765/0.835	1.195/1.305	1.72/1.88	1.195/1.305	N/A	1.195/1.305	3.16/3.44	N/A

1. Preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options

Table 11-2. Device Configuration Table

ORDERING CODE	FUNCTIONS	Reporting exclusions	OV/UV DEBOUNCE	Hysteresis_HF	BIST	SEQ TIMEOUT	PEC	I^{2}C PULL-UP VOLTAGE (V)
TPS388R02001RTERQ1 Preview	Monitor HF	N/A	0.1µsec	Disabled	at POR	1ms	Disable	3.3
TPS388R02002RTERQ1 Preview	Monitor HF	N/A	0.1µsec	Enabled	at POR	1ms	Disable	3.3
TPS388R04H01RTERQ1	Monitor HF	MON2	51.2µsec	Enabled	at POR	100ms	Enable	1.8
TPS388R04H00RTERQ1	Monitor HF	MON2	51.2µsec	Enabled	at POR	100ms	Enable	1.8
TPS388008001RTER	Monitor HF	MON5,MON8	51.2µsec	Enabled	at POR	200ms	Disable	1.2

11.2 Documentation Support

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2025	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

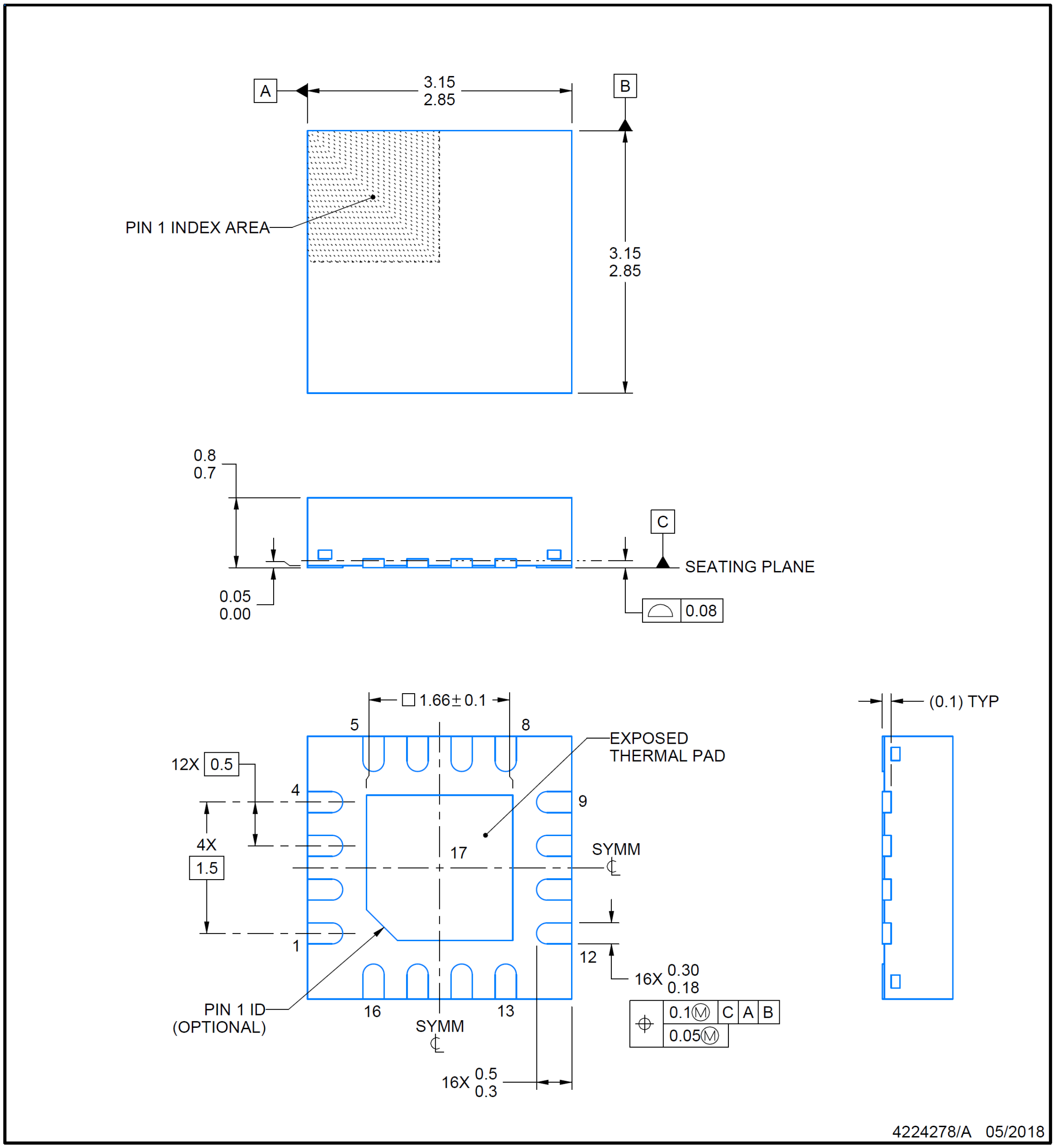
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

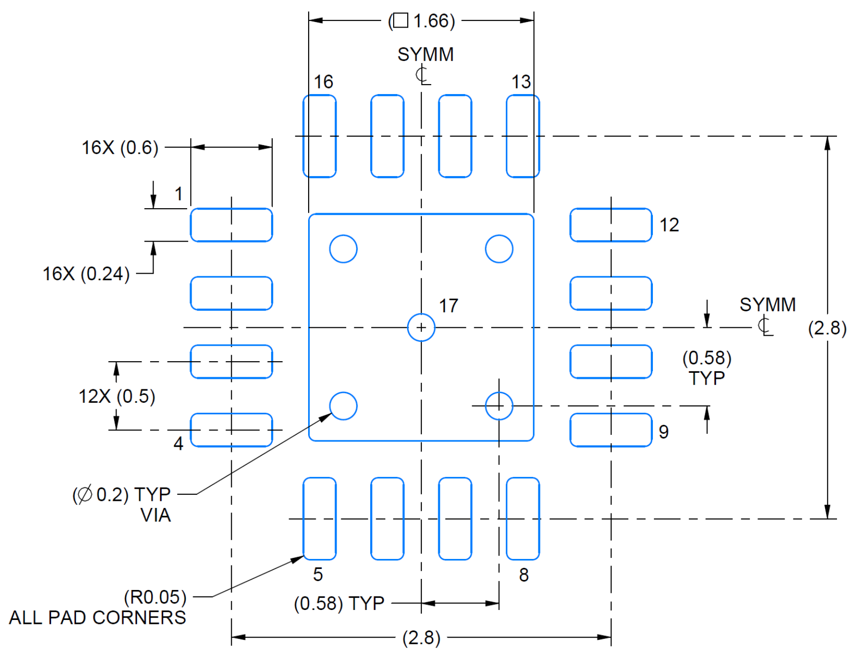
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

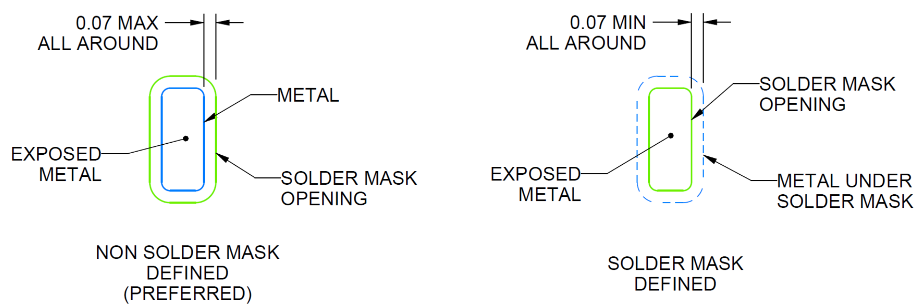
RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224278/A 05/2018

NOTES: (continued)

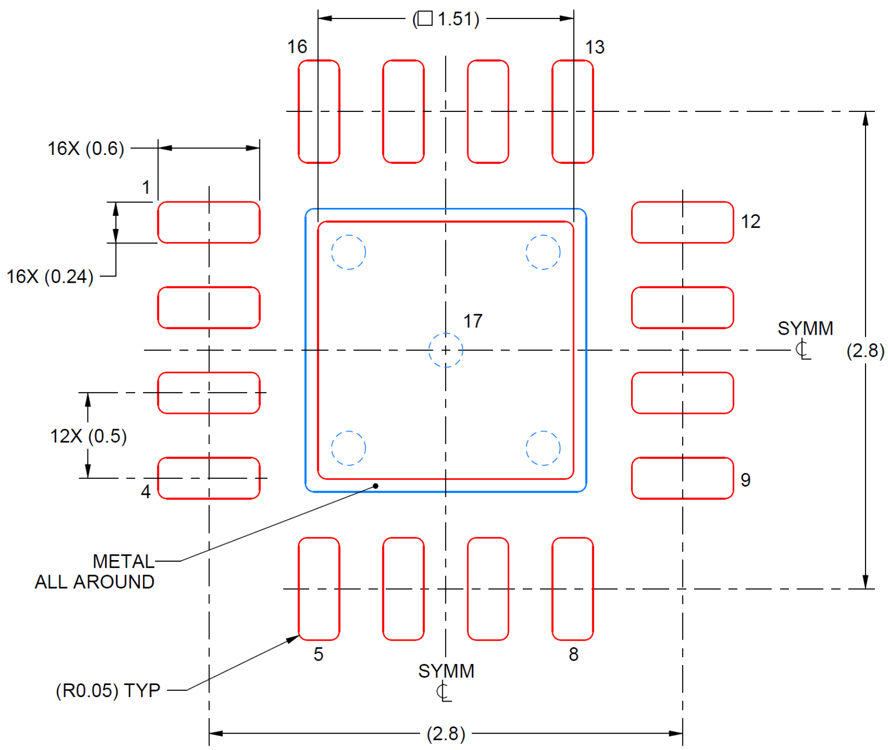
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224278/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS388008001RTER	ACTIVE	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T8001	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

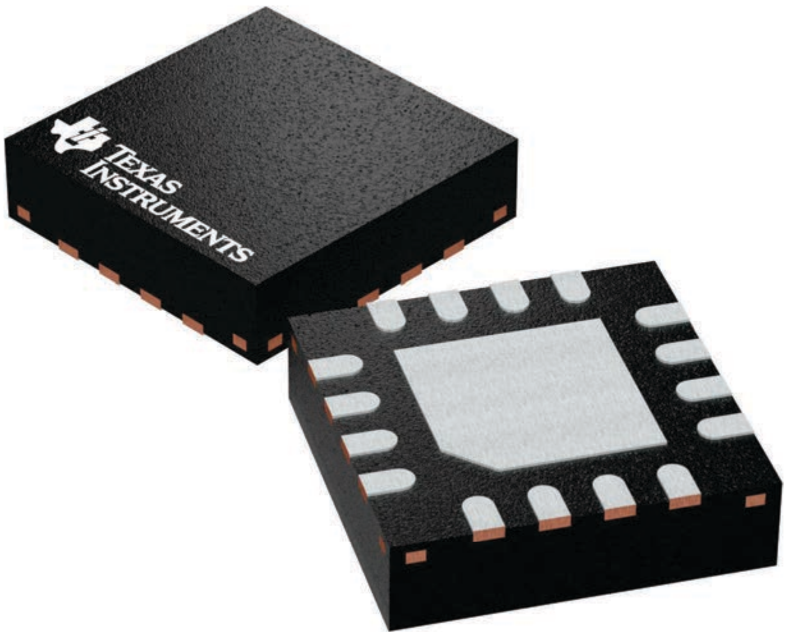
RTE 16

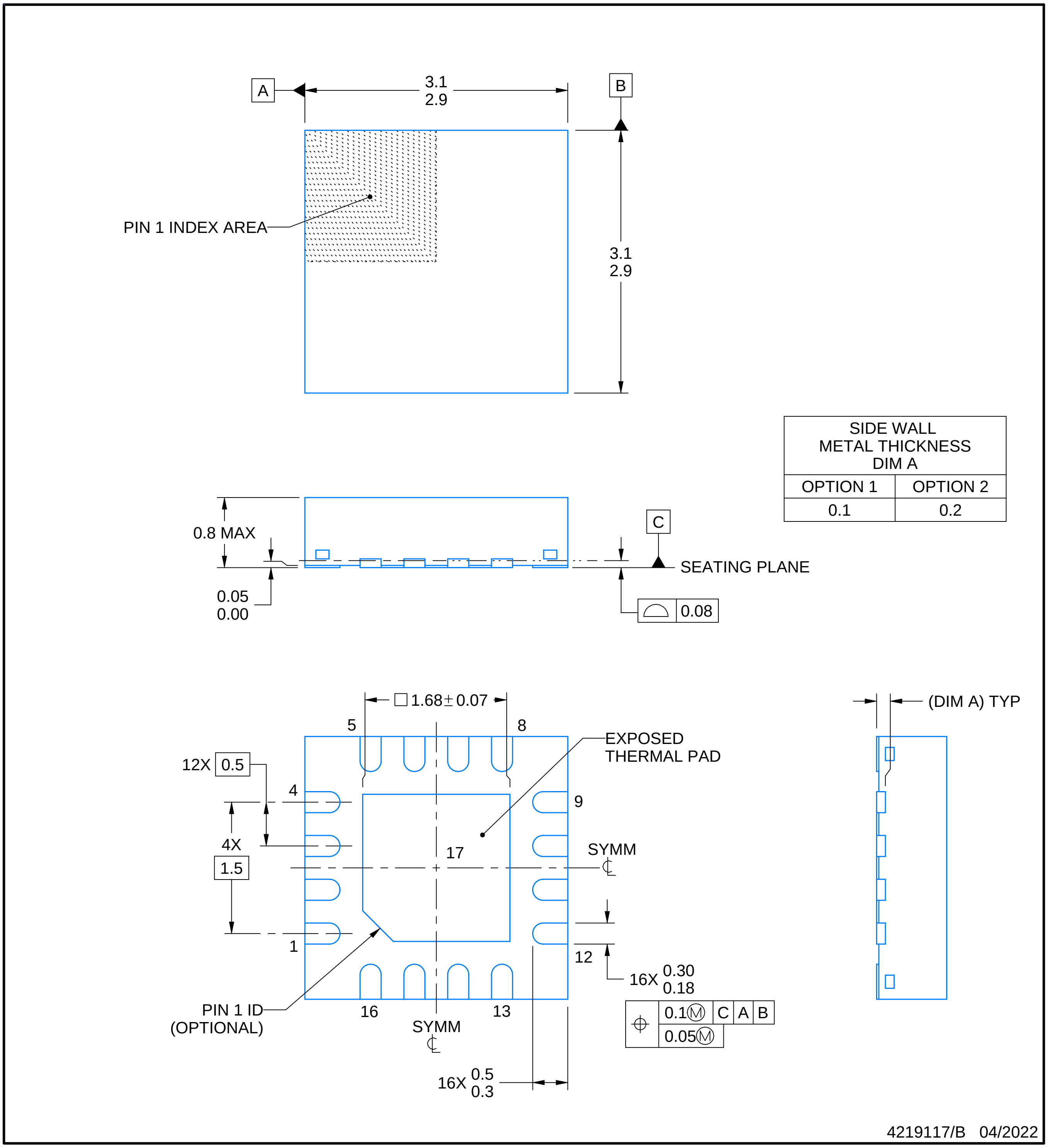
WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

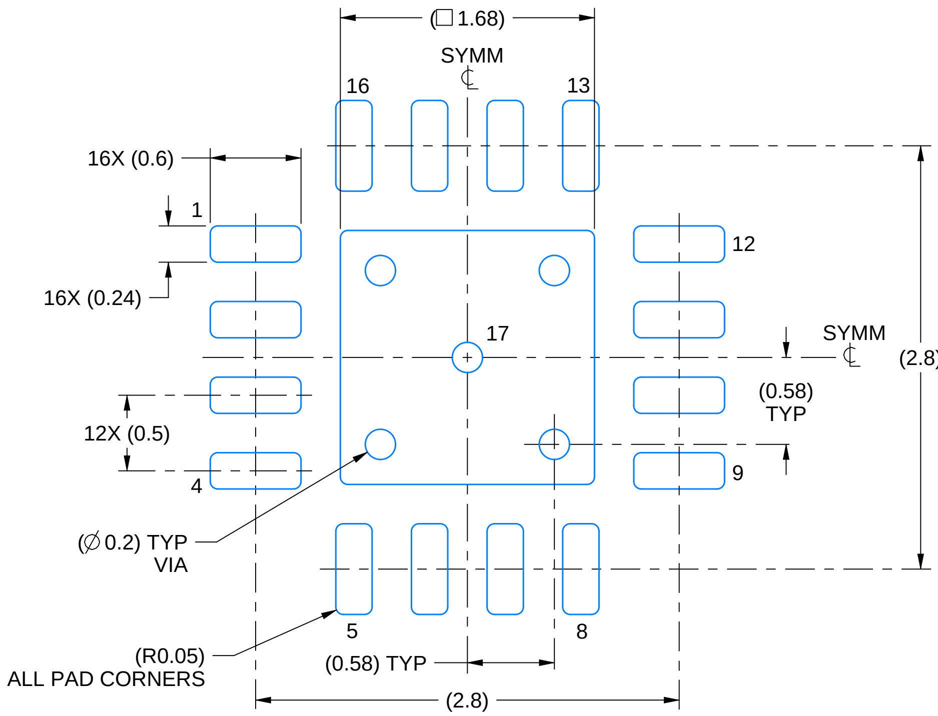




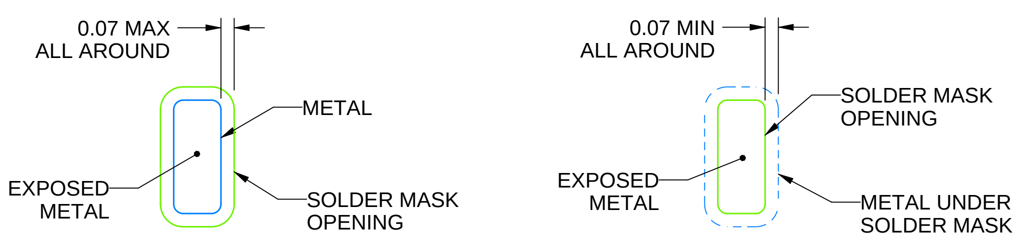
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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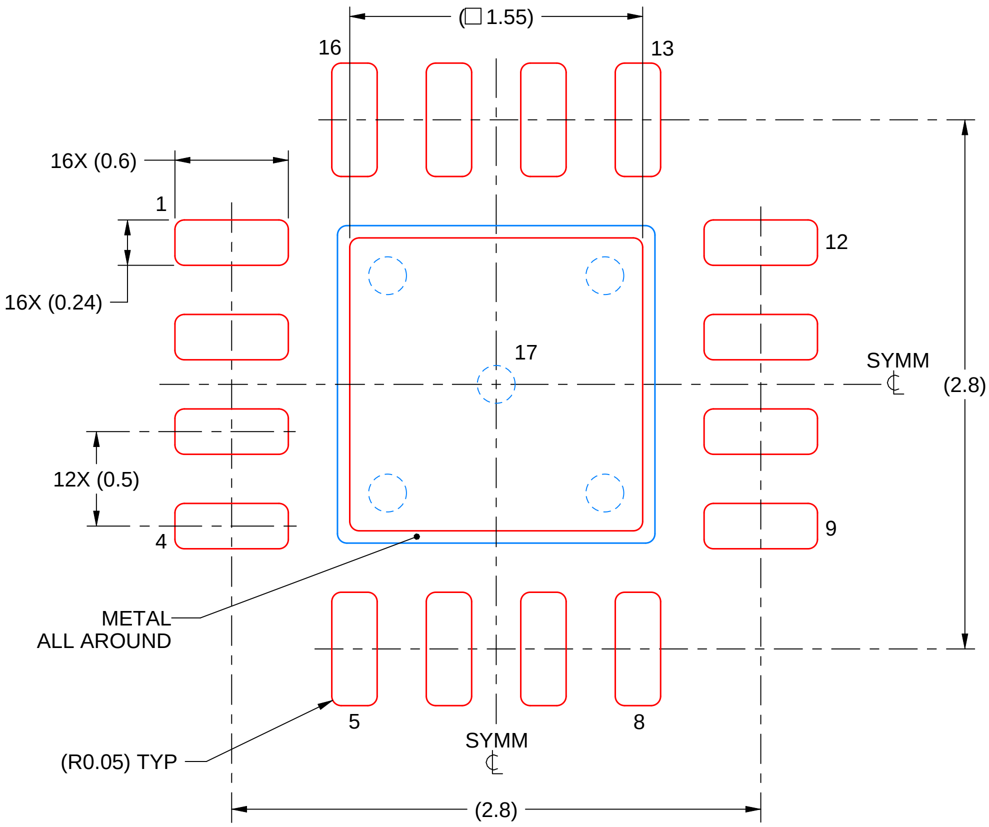

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

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