TEXAS INSTRUMENTS

TPS40303, TPS40304, TPS40305

JAJS463D – NOVEMBER 2009 – REVISED MARCH 2018

TPS4030x 3V～20V入力、電圧モードの同期整流降圧コントローラ

1 特長

- 3V～20Vの入力電圧範囲
- 300kHz (TPS40303)、600kHz (TPS40304)、1.2MHz (TPS40305)のスイッチング周波数
- ハイサイドおよびローサイドFET $R_{DS(on)}$電流センシング
- プログラミング可能な温度補償付きOCPレベル
- ソフトスタートをプログラム可能
- 基準電圧: 600mV、1%
- 電圧フィードフォワード補償
- プリバイアス出力をサポート
- 周波数スペクトラム拡散
- サーマル・シャットダウン保護: 145℃
- サーマル・パッドへのグランド接続を備えた10ピン3mm×3mm VSONパッケージ
- WEBENCH® Power Designerにより、TPS4030xを使用するカスタム設計を作成

2 アプリケーション

- POLモジュール
- プリンタ
- デジタル・テレビ
- 通信機器
- USB Type-Cレセプタクル

3 概要

TPS4030xは、3V～20Vの入力で動作する、コスト最適化された同期整流降圧コントローラのファミリです。このコントローラには電圧モード制御アーキテクチャが実装されており、入力電圧フィードフォワード補償により、入力電圧の変化に対して即座に応答します。スイッチング周波数は300kHz、600kHz、または1.2MHz固定です。

周波数スペクトラム拡散(FSS)機能により、スイッチング周波数にディザリングを付加することで、ピークEMIノイズが大幅に低減され、EMI標準への準拠が容易になります。

TPS4030xの設計には、ソフトスタート、過電流保護(OCP)レベル、ループ補償など、ユーザーによりプログラム可能な各種の機能が組み込まれています。

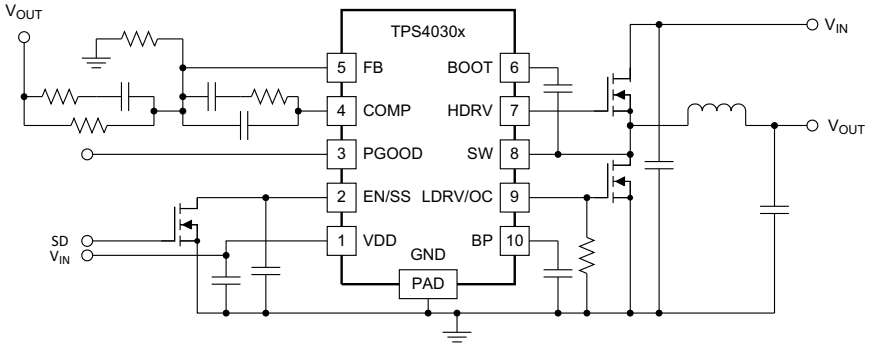
OCPレベルは、LDRVピンと回路のグランドとの間に接続する1個の外付け抵抗によってプログラムできます。最初の電源オン時に、TPS4030xは較正サイクルに移行し、LDRVピンの電圧を測定して、内部のOCP電圧レベルを設定します。動作中は、プログラムされたOCP電圧レベルが、ローサイドFETのオン時の電圧降下と比較され、過電流状態が発生しているかどうかが確認されます。過電流が発生すると、TPS4030xはその状況が解消されるまでの間、シャットダウンと再起動のサイクルを繰り返します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS40303	VSON (10)	3.00mm×3.00mm
TPS40304		
TPS40305		

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

アプリケーション概略図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (January 2018) から Revision D に変更 **Page**

- SEO用のデータシートのタイトル 変更 ... 1
- 「アプリケーション」に「USB Type-Cレセプタクル」を追加、WEBENCHへのリンクを 追加 ... 1
- Deleted redundant *Dissipation Ratings* table ... 4

Revision B (May 2015) から Revision C に変更 **Page**

- TPS40303 TI Design用の上端のナビゲーション・アイコン 追加 ... 1
- 削除 「デバイスおよびドキュメントのサポート」から関連デバイスの表を ... 32

Revision A (August 2012) から Revision B に変更 **Page**

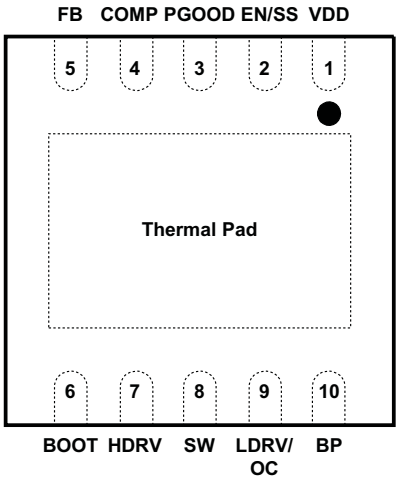
- 「*ピン構成および機能*」セクション、「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、および「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

2009年11月発行のものから更新 **Page**

- Changed minimum controllable pulse width max value from 100 to 70 ... 5

5 Pin Configuration and Functions

DRC Package
10-Pins VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	6	I	Gate drive voltage for the high-side N-channel MOSFET. A 0.1-µF capacitor (typical) must be connected between this pin and SW. For low input voltage operation, an external schottky diode from BP to BOOT is recommended to maximize the gate drive voltage for the high-side.
BP	10	O	Output bypass for the internal regulator. Connect a low ESR bypass ceramic capacitor of 1 µF or greater from this pin to GND.
COMP	4	O	Output of the error amplifier and connection node for loop feedback components.
EN/SS	2	I	Logic level input which starts or stops the controller via an external user command. Letting this pin float turns the controller on. Pulling this pin low disables the controller. This is also the soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 10 µA. The resulting voltage ramp of this pin is also used as a second non-inverting input to the error amplifier after a 0.8 V (typical) level shift downwards. Output regulation is controlled by the internal level shifted voltage ramp until that voltage reaches the internal reference voltage of 600 mV – the voltage ramp of this pin reaches 1.4 V (typical). Optionally, a 267-kΩ resistor from this pin to BP enables the FSS feature.
FB	5	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage.
HDRV	7	O	Bootstrapped gate drive output for the high-side N-channel MOSFET.
LDRV/OC	9	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET. A resistor from this pin to GND is also used to determine the voltage level for OCP. An internal current source of 10 µA flows through the resistor during initial calibration and that sets up the voltage trip point used for OCP.
PGOOD	3	O	Open-drain power good output.
SW	8	O	Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high-side FET driver.
VDD	1	I	Power input to the controller. Bypass VDD to GND with a low ESR ceramic capacitor of at least 1-µF close to the device.
GND	Thermal Pad	—	Ground connection to the controller. This is also the thermal pad used to conduct heat from the device. This connection serves a twofold purpose. The first is to provide an electrical ground connection for the device. The second is to provide a low thermal impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VDD	–0.3	22	V
SW	–3	27	V
SW (< 100-ns pulse width, 10 μJ)		–5	V
BOOT	–0.3	30	V
HDRV	–5	30	V
BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW)	–0.3	7	V
COMP, PGOOD, FB, BP, LDRV, EN/SS	–0.3	7	V
Operating junction temperature, T_J	–40	145	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	Input voltage	3		20	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS4030x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE							
V_{FB}	FB input voltage		T_J = 25°C, 3 V < V_{VDD} < 20 V	597	600	603	mV
			–40°C < T_J < 125°C, 3 V < V_{VDD} < 20 V	594	600	606	
INPUT SUPPLY							
V_{VDD}	Input supply voltage range			3		20	V
IDD_{SD}	Shutdown supply current		$V_{EN/SS}$ < 0.2 V		70	100	µA
IDD_Q	Quiescent, nonswitching		Let EN/SS float, V_{FB} = 1 V		2.5	3.5	mA
ENABLE/SOFT START							
V_{IH}	High-level input voltage, EN/SS			0.55	0.7	1	V
V_{IL}	Low-level input voltage, EN/SS			0.27	0.3	0.33	V
I_{SS}	Soft-start source current			8	10	12	µA
V_{SS}	Soft-start voltage level			0.4	0.8	1.3	V
BP REGULATOR							
V_{BP}	Output voltage		I_{BP} = 10 mA	6.2	6.5	6.8	V
V_{DO}	Regulator dropout voltage, V_{VDD} – V_{BP}		I_{BP} = 25 mA, V_{VDD} = 3 V		70	110	mV
OSCILLATOR							
f_{SW}	PWM frequency	TPS40303	3 V < V_{VDD} < 20 V	270	300	330	kHz
		TPS40304		540	600	660	kHz
		TPS40305		1.02	1.20	1.38	MHz
V_{RAMP} (1)	Ramp amplitude			V_{VDD}/6.6	V_{VDD}/6	V_{VDD}/5.4	V
f_{SWFSS}	Frequency spread-spectrum frequency deviation			12%			f_{SW}
f_{MOD}	Modulation frequency				25		kHz
PWM							
D_{MAX} (1)	Maximum duty cycle	TPS40303	V_{FB} = 0 V, 3 V < V_{VDD} < 20 V	90%			
		TPS40304		90%			
		TPS40305		85%			
$t_{ON(min)}$ (1)	Minimum controllable pulse width					70	ns
t_{DEAD}	Output driver dead time		HDRV off to LDRV on	5	25	35	ns
			LDRV off to HDRV on	5	25	30	
ERROR AMPLIFIER							
G_{BWP} (1)	Gain bandwidth product			10	24		MHz
A_{OL} (1)	Open loop gain			60			dB
I_{IB}	Input bias current (current out of FB pin)		V_{FB} = 0.6 V			75	nA
I_{EAOP}	Output source current		V_{FB} = 0 V	2			mA
I_{EAOM}	Output sink current		V_{FB} = 1 V	2			
PGOOD							
V_{OV}	Feedback upper voltage limit for PGOOD			655	675	700	mV
V_{UV}	Feedback lower voltage limit for PGOOD			500	525	550	
$V_{PGD-HYST}$	PGOOD hysteresis voltage at FB				25	40	
R_{PGD}	PGOOD pulldown resistance		V_{FB} = 0 V, I_{FB} = 5 mA		30	70	Ω
I_{PGDLK}	PGOOD leakage current		550 mV < V_{FB} < 655 mV, V_{PGOOD} = 5 V		10	20	µA

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pullup resistance	$V_{BOOT} – V_{SW}$ = 5 V, I_{HDRV} = –100 mA	0.8	1.5	2.5	Ω
R_{HDLO}	High-side driver pulldown resistance	$V_{BOOT} – V_{SW}$ = 5 V, I_{HDRV} = 100 mA	0.5	1	2.2	Ω
R_{LDHI}	Low-side driver pullup resistance	I_{LDRV} = –100 mA	0.8	1.5	2.5	Ω
R_{LDLO}	Low-side driver pulldown resistance	I_{LDRV} = 100 mA	0.35	0.6	1.2	Ω
t_{HRISE} (1)	High-side driver rise time	C_{LOAD} = 5 nF		15		ns
t_{HFALL} (1)	High-side driver fall time			12		ns
t_{LRISE} (1)	Low-side driver rise time			15		ns
t_{LFALL} (1)	Low-side driver fall time			10		ns
OVERCURRENT PROTECTION						
$t_{PSSC(min)}$ (1)	Minimum pulse time during short circuit			250		ns
t_{BLNKH} (1)	Switch leading-edge blanking pulse time			150		ns
V_{OCH}	OC threshold for high-side FET	T_J = 25°C	360	450	580	mV
I_{OCSET}	OCSET current source	T_J = 25°C	9.5	10	10.5	µA
$V_{LD-CLAMP}$	Maximum clamp voltage at LDRV		260	340	400	mV
V_{OCLOS}	OC comparator offset voltage for low-side FET	T_J = 25°C	–8		8	mV
V_{OCLPRO} (1)	Programmable OC range for low-side FET	T_J = 25°C	12		300	mV
V_{THTC} (1)	OC threshold temperature coefficient (both high-side and low-side)			3000		ppm
t_{OFF}	OC retry cycles on EN/SS pin			4		Cycle
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA		0.8		V
THERMAL SHUTDOWN						
T_{JSD} (1)	Junction shutdown temperature			145		°C
T_{JSDH} (1)	Hysteresis			20		°C

6.6 Typical Characteristics

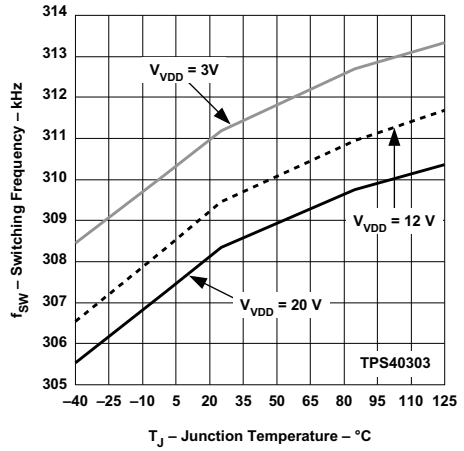


Figure 1. Switching Frequency vs Junction Temperature

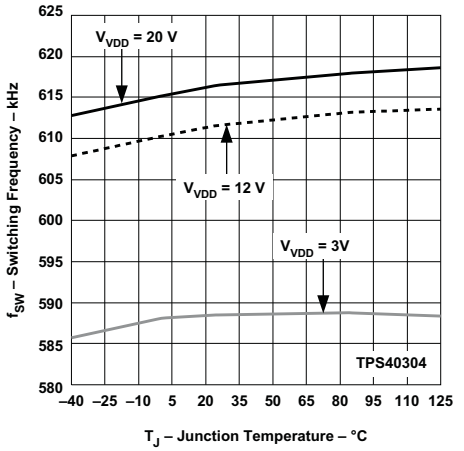


Figure 2. Switching Frequency vs Junction Temperature

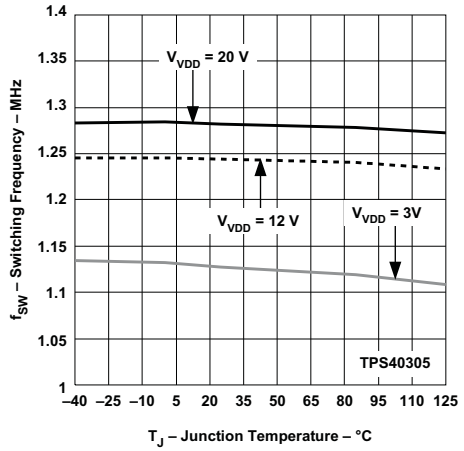


Figure 3. Switching Frequency vs Junction Temperature

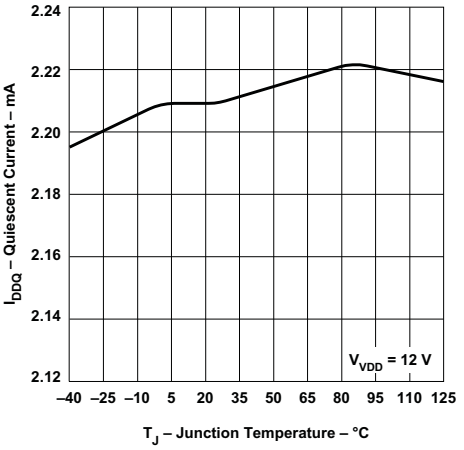


Figure 4. Quiescent Current vs Junction Temperature

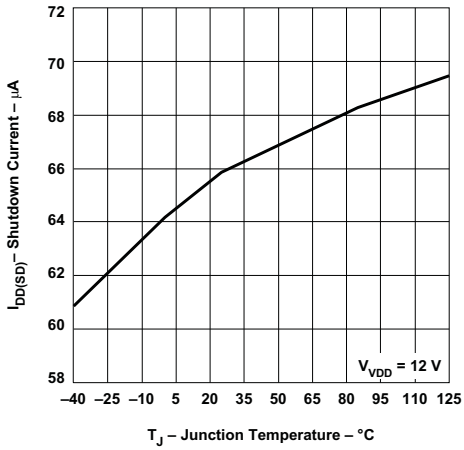


Figure 5. Shutdown Current vs Junction Temperature

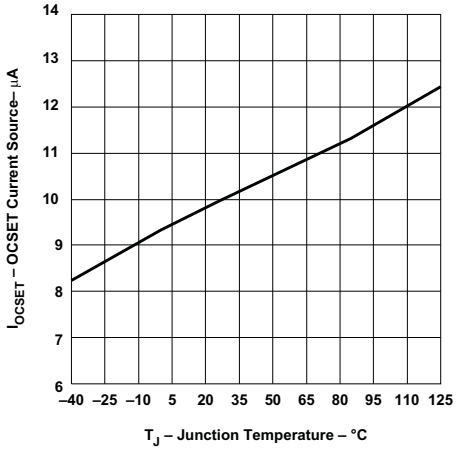


Figure 6. OCSET Current Source vs Junction Temperature

Typical Characteristics (continued)

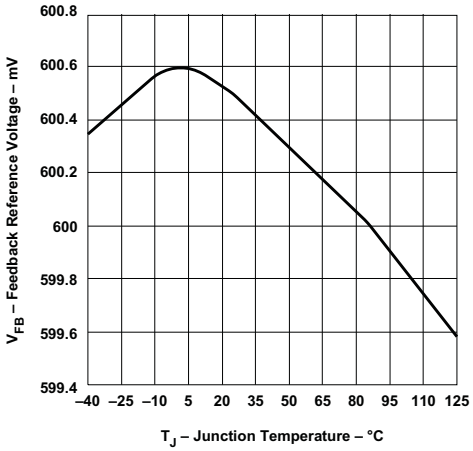


Figure 7. Feedback Reference Voltage vs Junction Temperature

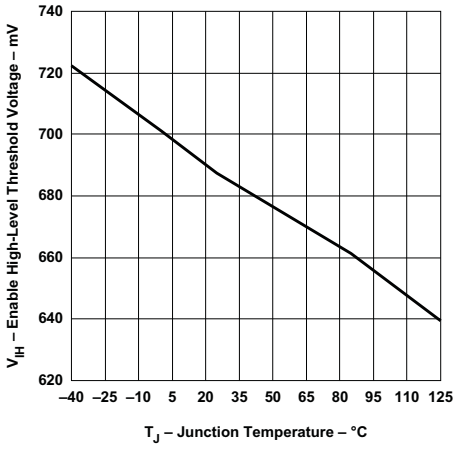


Figure 8. Enable High-Level Threshold Voltage vs Junction Temperature

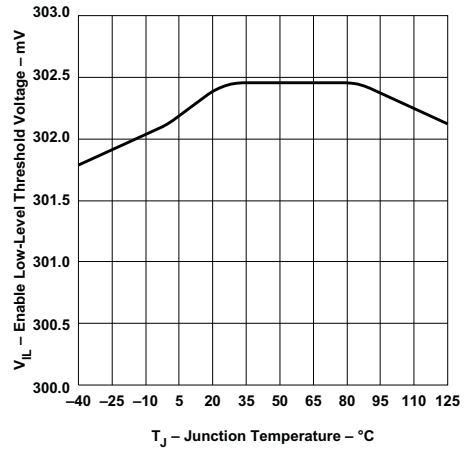


Figure 9. Enable Low-Level Threshold Voltage vs Junction Temperature

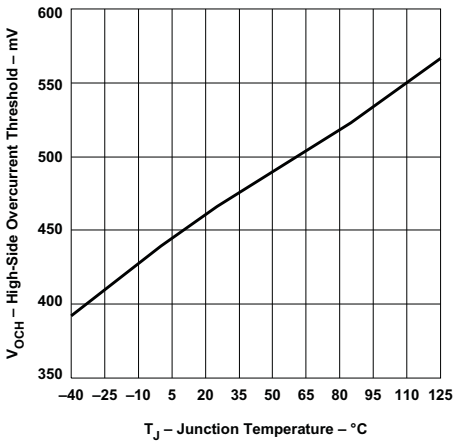


Figure 10. High-Side Overcurrent Threshold vs Junction Temperature

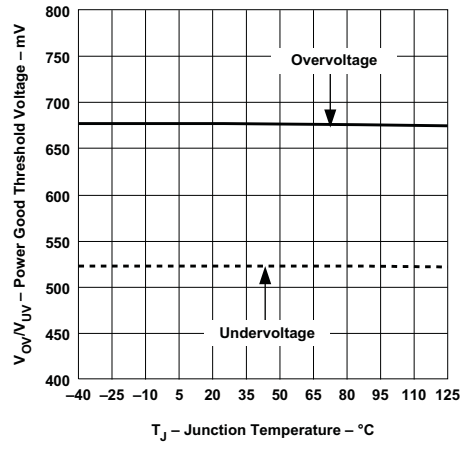


Figure 11. Power Good Threshold Voltage vs Junction Temperature

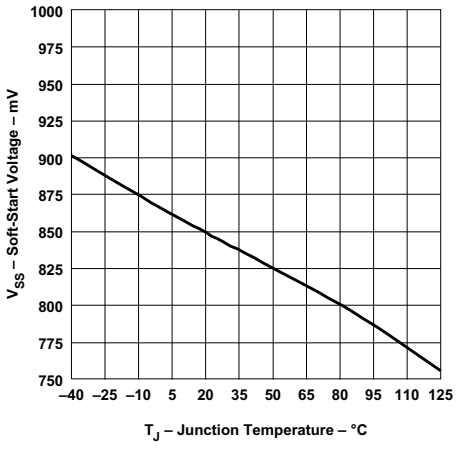


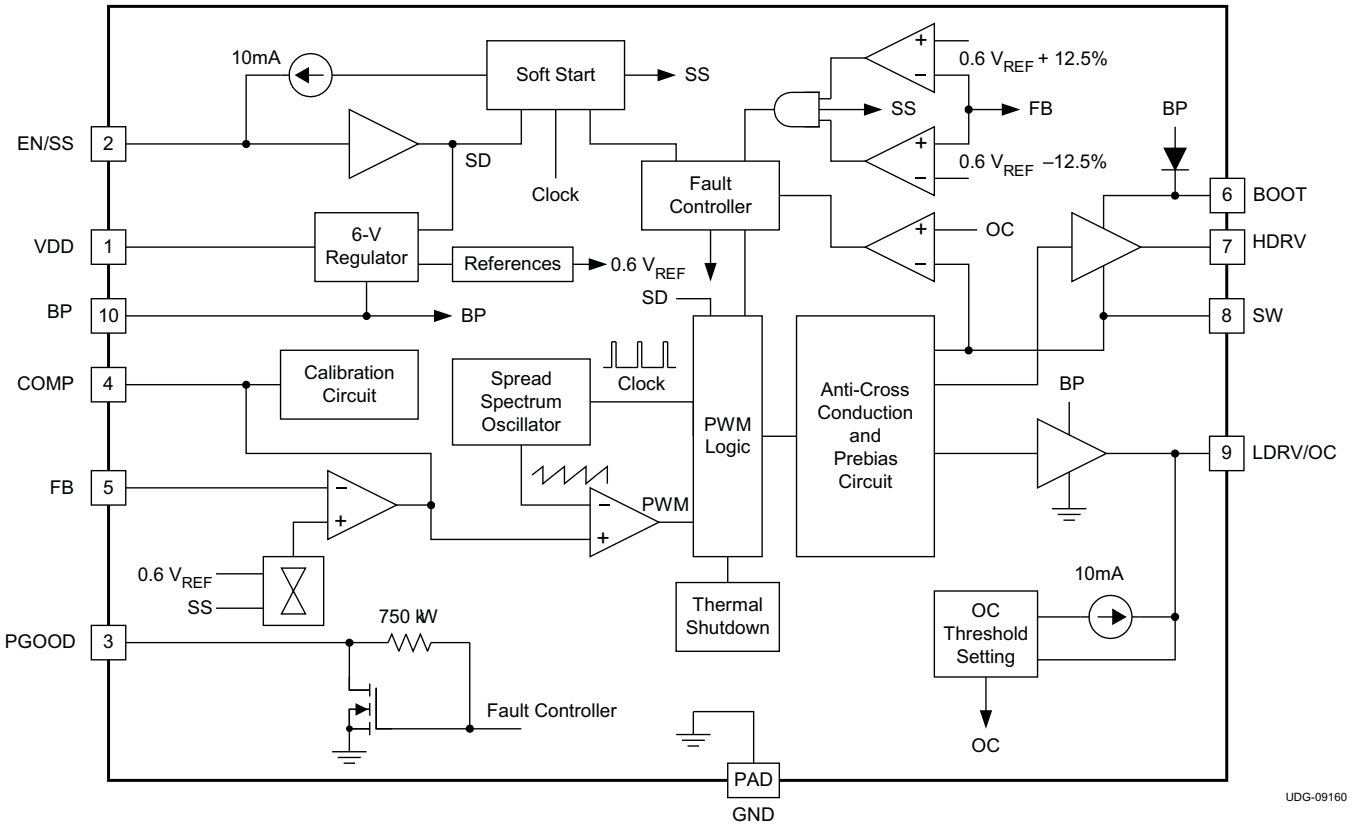
Figure 12. Soft-Start Voltage vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS4030x is a family of cost-optimized synchronous buck controllers providing high-end features to construct high-performance DC–DC converters. Prebias capability eliminates concerns about damaging sensitive loads during start-up. Programmable overcurrent protection levels and hiccup overcurrent fault recovery maximize design flexibility and minimize power dissipation in the event of a prolonged output short. The Frequency Spread Spectrum (FSS) feature reduces peak EMI noise by spreading the initial energy of each harmonic along a frequency band, thus giving a wider spectrum with lower amplitudes.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Voltage Reference

The 600-mV band gap cell is internally connected to the noninverting input of the error amplifier. The reference voltage is trimmed with the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 1% tolerance on the reference voltage allows the user to design a very accurate power supply.

7.3.2 Enable Functionality, Start-Up Sequence and Timing

After input power is applied, an internal current source of 40 µA starts to charge up the soft-start capacitor connected from EN/SS to GND. When the voltage across that capacitor increases to 0.7 V, it enables the internal BP regulator followed by a calibration. The total calibration time is about 1.9 ms. See Figure 13. During the calibration, the device performs in the following way. It disables the LDRV drive and injects an internal 10-µA current source to the resistor connected from LDRV to GND. The voltage developed across that resistor is then sampled and latched internally as the OCP trip level until one cycles the input or toggles the EN/SS.

Feature Description (continued)

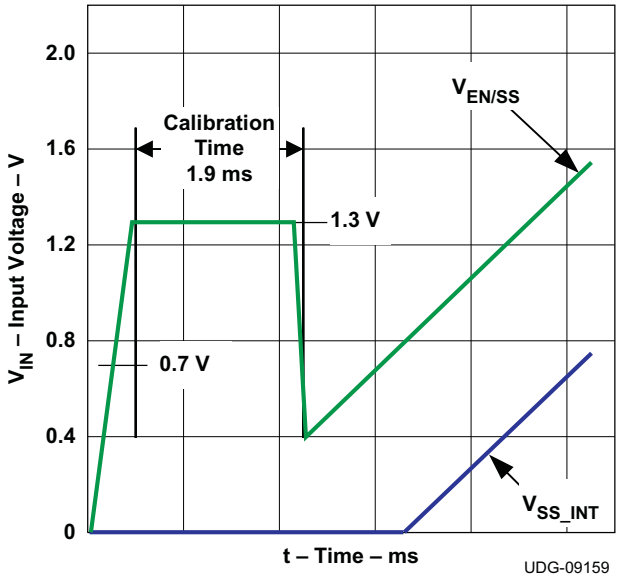


Figure 13. Start-Up Sequence and Timing

The voltage at EN/SS is internally clamped to 1.3 V before and/or during calibration to minimize the discharging time once calibration. The discharging current is from an internal current source of 140 µA and it pulls the voltage down to 0.4 V. The discharging current then initiates the soft-start by charging up the capacitor using an internal current source of 10 µA. The resulting voltage ramp on this pin is used as a second noninverting input to the error amplifier after an 800 mV (typical) downward level-shift; therefore, actual soft-start does not occur until the voltage at this pin reaches 800 mV.

If EN/SS is left floating, the controller starts automatically. EN/SS must be pulled down to less than 270 mV to ensure that the chip is in shutdown mode.

7.3.3 Soft-Start Time

The soft-start time of the TPS4030x is user programmable by selecting a single capacitor. The EN/SS pin sources 10 µA to charge this capacitor. The actual output ramp-up time is the amount of time that it takes for the 10 µA to charge the capacitor through a 600-mV range. There is some initial lag due to calibration and an offset (800 mV) from the actual EN/SS pin voltage to the voltage applied to the error amplifier.

The soft-start is done in a closed-loop fashion, meaning that the error amplifier controls the output voltage at all times during the soft-start period and the feedback loop is never open as occurs in duty cycle limit soft-start schemes. The error amplifier has two non-inverting inputs, one connected to the 600-mV reference voltage, and the other connected to the offset EN/SS pin voltage. The lower of these two voltages is what the error amplifier controls the FB pin. As the voltage on the EN/SS pin ramps up past approximately 1.4 V (800-mV offset voltage plus the 600 mV reference voltage), the 600-mV reference voltage becomes the dominant input and the converter has reached its final regulation voltage.

The capacitor required for a given soft-start ramp time for the output voltage is given by Equation 1.

$$C_{SS} = \left(\frac{I_{SS}}{V_{FB}} \right) \times t_{SS} \quad (1)$$

where

- C_{SS} is the required capacitance on the EN/SS pin. (F)
- I_{SS} is the soft-start source current (10 µA).
- V_{FB} is the feedback reference voltage (0.6 V).
- t_{SS} is the desired soft-start ramp time (s).

Feature Description (continued)

7.3.4 Oscillator and Frequency Spread Spectrum (FSS)

The oscillator frequency is internally fixed. The TPS40303 operating frequency is 300 kHz, the TPS40304 operating frequency is 600 kHz, and the TPS40305 operating frequency is 1.2 MHz.

Connecting a resistor with a value of 267 kΩ ±10% from BP to EN/SS enables the FSS feature. When the FSS is enabled, it spreads the internal oscillator frequency over a minimum 12% window using a 25-kHz modulation frequency with triangular profile. By modulating the switching frequency, side-bands are created. The emission power of the fundamental switching frequency and its harmonics is distributed into smaller pieces scattered around many sideband frequencies. The effect significantly reduces the peak EMI noise and makes it much easier for the resultant emission spectrum to pass EMI regulations.

7.3.5 Overcurrent Protection

Programmable OCP level at LDRV is from 6 mV to 150 mV at room temperature with 3000 ppm temperature coefficient to help compensate for changes in the low-side FET channel resistance as temperature increases. With a scale factor of 2, the actual trip point across the low-side FET is in the range of 12 mV to 300 mV. The accuracy of the internal current source is ±5%. Overall offset voltage, including the offset voltage of the internal comparator and the amplifier for scale factor of 2, is limited to ±8 mV.

Maximum clamp voltage at LDRV is 340 mV to avoid turning on the low-side FET during calibration and in a prebiased condition. The maximum clamp voltage is fixed and it does not change with temperature. If the voltage drop across R_{OCSET} reaches the 340-mV maximum clamp voltage during calibration (no R_{OCSET} resistor included), it disables OC protection. Once disabled, there is no low-side or high-side current sensing.

OCP level at HDRV is fixed at 450 mV with 3000-ppm temperature coefficient to help compensate for changes in the high-side FET channel resistance as temperature increases. OCP at HDRV provides pulse-by-pulse current limiting.

OCP sensing at LDRV is a true inductor valley current detection, using sample and hold. Equation 2 can be used to calculate R_{OCSET}:

$$R_{OCSET} = \left(\frac{\left(I_{OUT(max)} - \left(\frac{I_{P-P}}{2} \right) \right) \times R_{DS(on)} - V_{OCLOS}}{2 \times I_{OCSET}} \right) \quad (2)$$

where

- I_{OCSET} is the internal current source.
- V_{OCLOS} is the overall offset voltage.
- I_{P-P} is the peak-to-peak inductor current.
- $R_{DS(on)}$ is the drain to source ON-resistance of the low-side FET.
- $I_{OUT(max)}$ is the trip point for OCP.
- R_{OCSET} is the resistor used for setting the OCP level.

To avoid overcurrent tripping in normal operating load range, calculate R_{OCSET} using the equation above with:

- The maximum $R_{DS(ON)}$ at room temperature
- The lower limit of V_{OCLOS} (–8 mV) and the lower limit of I_{OCSET} (9.5 µA) from the *Electrical Characteristics* table.
- The peak-to-peak inductor current I_{P-P} at minimum input voltage

Overcurrent is sensed across both the low-side FET and the high-side FET. If the voltage drop across either FET exceeds the OC threshold, a count increments one count. If no OC is detected on either FET, the fault counter decrements by one count. If three OC pulses are summed, a fault condition is declared which cycles the soft-start function in a hiccup mode. Hiccup mode consists of four dummy soft-start timeouts followed by a real one if overcurrent condition is encountered during normal operation, or five dummy soft-start timeouts followed by a real one if overcurrent condition occurs from the beginning during start. This cycle continues indefinitely until the fault condition is removed.

Feature Description (continued)

7.3.6 Drivers

The drivers for the external high-side and low-side MOSFETs can drive a gate-to-source voltage of V_{BP}. The LDRV driver for the low-side MOSFET switches between BP and GND, while the HDRV driver for the high-side MOSFET is referenced to SW and switches between BOOT and SW. The drivers have nonoverlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier.

7.3.7 Prebias Start-Up

The TPS4030x contains a circuit to prevent current from being pulled from the output during start-up in the condition the output is prebiased. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FB pin), if the output is prebiased. Once the soft-start voltage exceeds the error amplifier input, the controller slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on time. The controller then increments that on time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This approach prevents the sinking of current from a prebiased output, and ensures the output voltage start-up and ramp to regulation is smooth and controlled.

7.3.8 Power Good

The TPS4030x provides an indication that output is good for the converter. This is an open-drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include the following:

- V_{FB} is more than ±12.5% from nominal.
- Soft-start is active.
- A short-circuit condition has been detected.

NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built-in resistor connected from drain to gate on the PGOOD pulldown device makes the PGOOD pin look approximately like a diode to GND.

7.3.9 Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 145°C, the PWM and the oscillator are turned off and HDRV and LDRV are driven low. When the junction cools to the required level (125°C typical), the PWM initiates soft-start as during a normal power-up cycle.

7.4 Device Functional Modes

7.4.1 Modes of Operation

7.4.1.1 UVLO

In UVLO, VDD is less than UVLO_ON, the BP6 regulator is off, and the HDRV and LDRV are held low by internal passive discharge resistors.

7.4.1.2 Disable

Disable is forced by holding SS/EN below 0.4 V. In disable, the BP6 regulator is off, and both HDRV and LDRV are held low by passive discharge resistors.

7.4.1.3 Calibration

Each enable of the TPS4030X3/4/5 devices requires a calibration which lasts approximately 2 ms. During calibration the TPS40303/4/5 devices LDRV and HDRV are held off by their respective pulldown drivers while the device configures as detailed in *Enable Functionality, Start-Up Sequence and Timing*.

7.4.1.4 Converting

When calibration completes, the TPS40303/4/5 devices ramp their reference voltage as described in *Soft-Start Time*, and the states of the LDRV and HDRV drivers are dictated by the COMP pin to regulate the FB pin equal to the internal reference.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS4030x is a family of cost-optimized synchronous buck controllers providing high-end features to construct high-performance DC-DC converters. Prebias capability eliminates concerns about damaging sensitive loads during start-up. Programmable overcurrent protection levels and hiccup overcurrent fault recovery maximize design flexibility and minimize power dissipation in the event of a prolonged output short. Frequency Spread Spectrum (FSS) feature reduces peak EMI noise by spreading the initial energy of each harmonic along a frequency band, thus giving a wider spectrum with lower amplitudes.

8.2 Typical Applications

8.2.1 Using the TPS40305 for a 12-V to 1.8-V Point-of-Load Synchronous Buck Regulator

Figure 14 shows 12-V to 1.8-V at 10-A synchronous buck application using the TPS40305 switching at 1200 kHz.

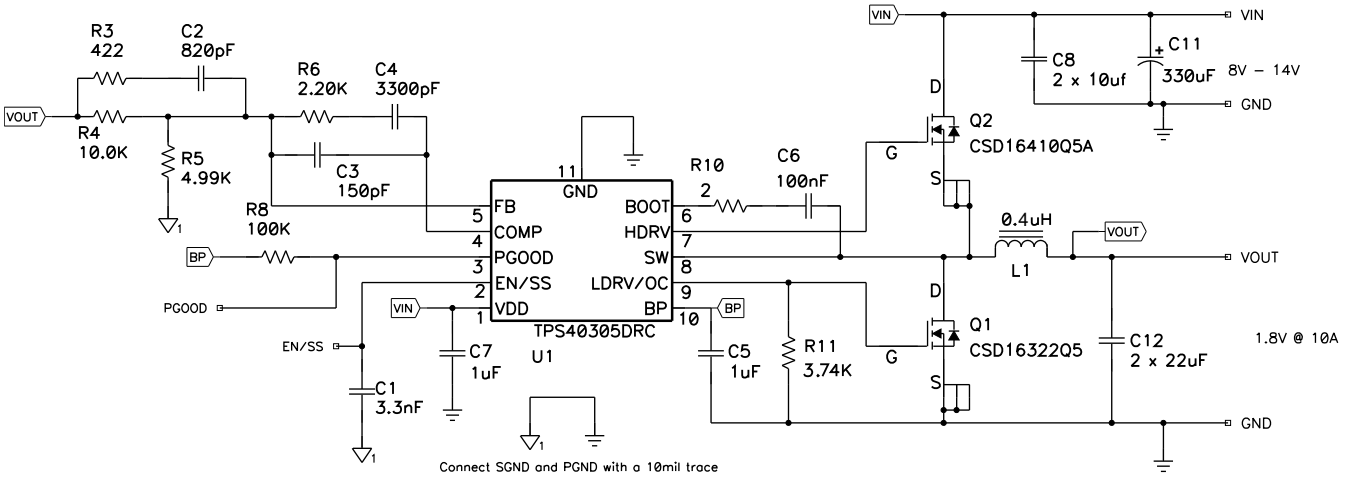


Figure 14. TPS40305 Design Example Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

For this example, follow the design parameters listed in Table 1.

Table 1. Design Example Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		8		14	V
$V_{IN(ripple)}$	Input ripple	I_{OUT} = 10 A			0.6	V
V_{OUT}	Output voltage	0 A ≤ I_{OUT} ≤ 10 A	1.764	1.800	1.836	V
	Line regulation	8 V ≤ V_{IN} ≤ 14 V			0.5%	
	Load regulation	0 A ≤ I_{OUT} ≤ 10 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT} = 10 A			36	mV
V_{OVER}	Output overshoot	I_{OUT} falling from 7 A to 3 A		100		mV
V_{UNDER}	Output undershoot	I_{OUT} rising from 3 A to 7 A		100		mV
I_{OUT}	Output current	4.5 V ≤ V_{IN} ≤ 5.5 V	0		10	A
t_{SS}	Soft-start time	V_{IN} = 12 V		1.5		ms
I_{SCP}	Short-circuit current trip point		13	15		A
f_{SW}	Switching frequency			1200		kHz
	Size			1		in^2

The bill of materials for this application is shown in Table 2. The efficiency, line, and load regulation from boards built using this design are shown in Figure 14. Gerber files and additional application information are available from the factory.

Table 2. Design Example List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1	1	3.3 nF	Capacitor, Ceramic, 10 V, X7R, 20%	0603	Std	Std
C2	1	820 pF	Capacitor, Ceramic, 25 V, X7R, 10%	0603	Std	Std
C3	1	150 pF	Capacitor, Ceramic, 25 V, X7R, 10%	0603	Std	Std
C4	1	3300 pF	Capacitor, Ceramic, 25 V, X7R, 10%	0603	Std	Std
C5	1	1.0 µF	Capacitor, Ceramic, 10 V, X7R, 20%	0805	Std	Std
C6	1	100 nF	Capacitor, Ceramic, 16 V, X7R, 20%	0603	Std	Std
C7	1	1 µF	Capacitor, Ceramic, 25 V, X7R, 20%	0805	Std	Std
C8	2	10 µf	Capacitor, Ceramic, 25 V, X7R, 10%	1210	Std	Std
C11	1	330 µF	Capacitor, Aluminum, 25 V, ±20%, 160 mΩ	0.328 × 0.390 inch	EEVFK1E331P	Panasonic
C12	2	22 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	0805	Std	Std
L1	1	0.32 µH	Inductor, SMT, 17 A	0.268 × 0.268 inch	PG0083.401	Pulse
Q1	1		MOSFET, N-Channel, 25 V, 97 A, 4.6 mΩ	QFN-8 POWER	CSD16322Q5	TI
Q2	1		MOSFET, N-Channel, 25 V, 59 A, 9.6 mΩ	QFN-8 POWER	CSD16410Q5A	TI
R3	1	422 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	1	10.0 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R5	1	4.99 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R6	1	2.20 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R8	1	100 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R10	1	2 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R11	1	3.74 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
U1	1		IC, 3-V to 20-V sync. 1.2-MHz Buck controller	DRC10	TPS40305DRC	TI

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS4030x devicse with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Selecting the Switching Frequency

To achieve the small size for this design, the TPS40305, with f_{SW} = 1200 kHz, is selected for minimal external component size.

8.2.1.2.3 Inductor Selection (L1)

Synchronous buck power inductors are typically sized for approximately 30% peak-to-peak ripple current (I_{RIPPLE})

Given this target ripple current, the required inductor size can be calculated in Equation 3.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{14\,V - 1.8\,V}{0.3 \times 10\,A} \times \frac{1.8\,V}{14\,V} \times \frac{1}{1200\,kHz} = 471\,nH \quad (3)$$

Selecting a standard 400-nH inductor value, solve for I_{RIPPLE} = 3.5 A

The RMS current through the inductor is approximated by Equation 4.

$$I_{L(rms)} = \sqrt{I_{L(avg)}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{I_{OUT}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{10^2 + \tfrac{1}{12} 3.5^2} = 10.05\,A \quad (4)$$

8.2.1.2.4 Output Capacitor Selection (C12)

The selection of the output capacitor is typically driven by the output transient response. Equation 5 and Equation 6 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{I_{TRAN}^2 \times L}{V_{OUT} \times C_{OUT}} \quad (5)$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{IN} - V_{OUT}} = \frac{I_{TRAN}^2 \times L}{(V_{IN} - V_{OUT}) \times C_{OUT}} \quad (6)$$

If $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot (Equation 5) to calculate minimum output capacitance. If $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot (Equation 6) to calculate minimum output capacitance.

$$C_{OUT(min)} = \frac{I_{TRAN(max)}^2 \times L}{(V_{OUT}) \times V_{OVER}} = \frac{4^2 \times 400\,nH}{1.8 \times 100\,mV} = 35\,\mu F \quad (7)$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 8.

$$ESR_{MAX} = \frac{V_{RIPPLE(total)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}}$$

$$= \frac{36\,mV - \left(\frac{3.5\,A}{8 \times 35\,\mu F \times 1200\,kHz}\right)}{3.5\,A} = 7\,m\Omega \quad (8)$$

Two 0805, 22-µF, 6.3-V, X5R ceramic capacitors are selected to provide more than 35 µF of minimum capacitance and less than 7 mΩ of ESR (2.5 mΩ each).

8.2.1.2.5 Peak Current Rating of Inductor

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by Equation 9.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.8\,V \times 2 \times 22\,\mu F}{1.5\,ms} = 0.053\,A \quad (9)$$

$$I_{L(peak)} = I_{OUT(max)} + \tfrac{1}{2} I_{RIPPLE} + I_{CHARGE} = 10\,A + \tfrac{1}{2} \times 3.5\,A + 0.053\,A = 11.8\,A \quad (10)$$

Table 3. Inductor Requirements

SYMBOL	PARAMETER	VALUE	UNIT
L	Inductance	400	nH
$I_{L(rms)}$	RMS current (thermal rating)	10.05	A
$I_{L(peak)}$	Peak current (saturation rating)	11.8	A

A PG0083.401, 400-nH inductor is selected for its small size, low DCR (3.0 mΩ) and high-current handling capability (17-A thermal, 27-A saturation).

8.2.1.2.6 Input Capacitor Selection (C8)

The input voltage ripple is divided between capacitance and ESR. For this design $V_{RIPPLE(cap)}$ = 150 mV and $V_{RIPPLE(esr)}$ = 150 mV. The minimum capacitance and maximum ESR are estimated by Equation 11.

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN} \times f_{SW}} = \frac{10 \times 1.8\,V}{150\,mV \times 8\,V \times 1200\,kHz} = 12.5\,\mu F \quad (11)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(esr)}}{I_{LOAD} + \tfrac{1}{2} I_{RIPPLE}} = \frac{150\,mV}{11.75\,A} = 12.7\,m\Omega \quad (12)$$

The RMS current in the input capacitors is estimated by Equation 13.

$$I_{RMS(cin)} = I_{LOAD} \times \sqrt{D \times (1 - D)} = 10\,A \times \sqrt{0.225 \times (1 - 0.225)} = 4.17\,A_{RMS} \quad (13)$$

Two 1210, 10-µF, 25-V, X5R ceramic capacitors with approximately 2-mΩ of ESR and a 2.5-A RMS current rating each are selected. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors allow sufficient capacitance at the working voltage.

8.2.1.2.7 MOSFET Switch Selection (Q1 and Q2)

Reviewing available TI NexFET MOSFETs using TI's NexFET MOSFET selection tool, the CSD16410Q5A and CSD16322Q5 5-mm × 6-mm MOSFETs are selected.

These two FETs have maximum total gate charges of 5 nC and 10 nC, respectively, which draws 18 mA at 1.2 MHz from the BP regulator, less than its 50 mA minimum rating.

8.2.1.2.8 Bootstrap Capacitor (C6)

To ensure proper charging of the high-side FET gate, limit the ripple voltage on the boost capacitor to less than 50 mV.

$$C_{BOOST} = 20 \times Q_{G2} = 20 \times 5\,nC = 100\,nF \tag{14}$$

8.2.1.2.9 VDD Bypass Capacitor (C7)

Per the TPS40305 *Electrical Characteristics* specifications, select a 1.0-µF X5R or better ceramic bypass capacitor for VDD.

8.2.1.2.10 BP Bypass Capacitor (C5)

As listed in the *Electrical Characteristics*, a minimum of 1.0-µF ceramic capacitance is required to stabilize the BP regulator. To limit regulator noise to less than 10 mV, the value of the bypass capacitor is calculated in Equation 15.

$$C_{BP} = 100 \times MAX(Q_{G1}, Q_{G2}) \tag{15}$$

Because Q1 is larger than Q2, and the total gate charge of Q1 is 10 nC, a BP capacitor of 1.0 µF is calculated. A standard value of 1.0 µF is selected to limit noise on the BP regulator.

8.2.1.2.11 Short-Circuit Protection (R11)

The TPS40305 uses the negative drop across the low-side FET at the end of the OFF time to measure the inductor current. Allowing for 30% over maximum load and 20% rise in $R_{DS(on)Q1}$ for self-heating, the voltage drop across the low-side FET at current limit is given by Equation 16.

$$V_{OC} = (1.3 \times I_{LOAD} - \tfrac{1}{2} I_{RIPPLE}) \times 1.2 \times R_{DS(on)Q1} = (1.3 \times 10\ A - \tfrac{1}{2} 3.5\ A) \times 1.2 \times 4.6\ m\Omega = 62.1\ mV \tag{16}$$

The TPS40305 internal temperature coefficient helps compensate for the $R_{DS(on)}$ temperature coefficient of the MOSFET, so the current limit programming resistor is selected by Equation 17.

$$R_{CS} = \frac{V_{OC} - V_{OCLOS(min)}}{2 \times I_{OCSET(min)}} = \frac{62.1mV - (-8mV)}{2 \times 9.5\ mA} = 3.69\ k\Omega \approx 3.74\ k\Omega \tag{17}$$

8.2.1.2.12 Feedback Divider (R4, R5)

The TPS40305 controller uses a full operational amplifier with an internally fixed 0.600-V reference. R4 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With R4 set to 10 kΩ, The output voltage is programmed with a resistor divider given by Equation 18.

$$R5 = \frac{V_{FB} \times R4}{V_{OUT} - V_{FB}} = \frac{0.600\,V \times 10.0\,k\Omega}{1.8\,V - 0.600\,V} = 5.0\,k\Omega \approx 4.99\,k\Omega \tag{18}$$

8.2.1.2.13 Compensation: (C2, C3, C4, R3, R6)

Using the TPS40k Loop Stability Tool for 100-kHz bandwidth and 60° phase margin with a R4 value of 10.0 kΩ, the following values are returned.

- C2 = C_1 = 820 pF
- C3 = C_3 = 150 pF
- C4 = C_2 = 3300 pF
- R3 = R_2 = 422 Ω
- R6 = R_3 = 2.20 kΩ

8.2.1.3 Application Curves

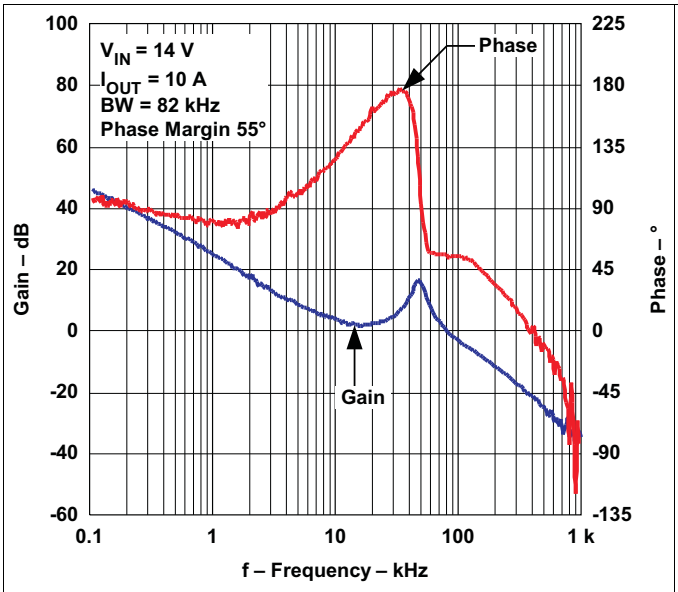


Figure 15. Gain and Phase vs Frequency

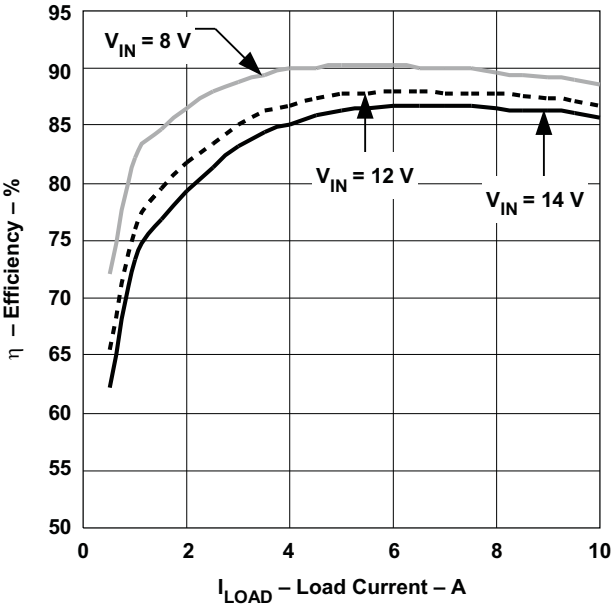


Figure 16. Efficiency vs Load Current

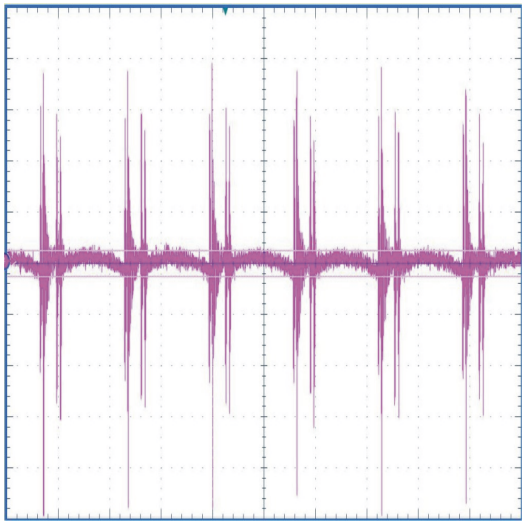


Figure 17. Output Ripple (500-MHz Bandwidth)

8.2.2 A High-Current, Low-Voltage Design Using the TPS40304

For this 20-A, 12-V to 1.2-V design, the 600-kHz TPS40304 was selected for a balance between small size and high efficiency.

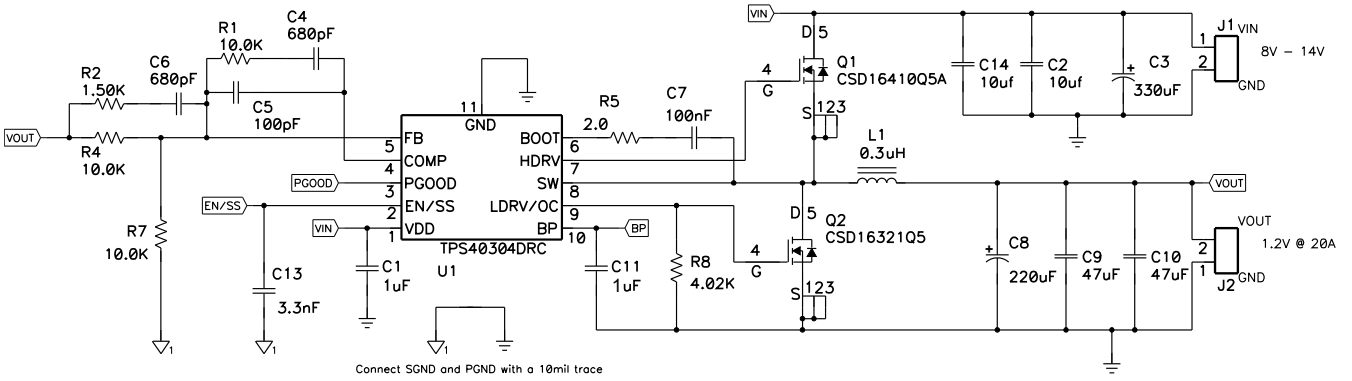


Figure 18. TPS40304 Design Example Schematic

8.2.2.1 Design Requirements

For this example, follow the design parameters listed in Table 4.

Table 4. Design Example Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		8		14	V
$V_{INripple}$	Input ripple	I_{OUT} = 20 A			0.5	V
V_{OUT}	Output voltage	0 A ≤ I_{OUT} ≤ 20 A	1.164	1.200	1.236	V
	Line regulation	8 V ≤ V_{IN} ≤ 14 V			0.5%	
	Load regulation	0 A ≤ I_{OUT} ≤ 20 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT} = 20 A			36	mV
V_{OVER}	Output overshoot	5 A ≤ I_{OUT} ≤ 15 A		100		mV
V_{UNDER}	Output undershoot	5 A ≤ I_{OUT} ≤ 15 A		100		mV
I_{OUT}	Output current	8 V ≤ V_{IN} ≤ 14 V	0		20	A
t_{SS}	Soft-start time	V_{IN} = 12 V		1.5		ms
I_{SCP}	Short-circuit current trip point		26			A
f_{SW}	Switching frequency			600		kHz
	Size				1.5	in^2

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Selecting the Switching Frequency

To achieve the small size for this design the TPS40304, with f_{SW} = 600 kHz, is selected for minimal external component size.

8.2.2.2.2 Inductor Selection (L1)

Synchronous buck power inductors are typically sized for approximately 30% peak-to-peak ripple current (I_{RIPPLE})

Given this target ripple current, the required inductor size can be calculated in Equation 19.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{F_{SW}} = \frac{14V - 1.2V}{0.3 \times 20A} \times \frac{1.2V}{14V} \times \frac{1}{600kHz} = 305nH \quad (19)$$

Selecting a standard 300-nH inductor value, solve for I_{RIPPLE} = 6 A

The RMS current through the inductor is approximated by Equation 20.

$$I_{Lrms} = \sqrt{I_{Lavg}^2 + \frac{1}{12} I_{RIPPLE}^2} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{RIPPLE}^2} = \sqrt{20^2 + \frac{1}{12} 6^2} = 20.07 \text{ A} \quad (20)$$

8.2.2.2.3 Output Capacitor Selection (C12)

The selection of the output capacitor is typically driven by the output transient response. Equation 21 and Equation 22 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{I_{TRAN}^2 \times L}{V_{OUT} \times C_{OUT}} \quad (21)$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{IN} - V_{OUT}} = \frac{I_{TRAN}^2 \times L}{(V_{IN} - V_{OUT}) \times C_{OUT}} \quad (22)$$

If $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot (Equation 21) to calculate minimum output capacitance. If $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot (Equation 22) to calculate minimum output capacitance.

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^2 \times L}{(V_{OUT}) \times V_{OVER}} = \frac{10^2 \times 300\text{nH}}{1.2 \times 100\text{mV}} = 250\mu\text{F} \quad (23)$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 24.

$$ESR_{max} = \frac{V_{RIPPLE(Total)} - V_{RIPPLE(CAP)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}\right)}{I_{RIPPLE}} = \frac{36\text{mV} - \left(\frac{6\text{A}}{8 \times 250\mu\text{F} \times 600\text{kHz}}\right)}{6\text{A}} = 5.2\text{m}\Omega \quad (24)$$

Two 47-µF and one 220-µF capacitors are selected to provide more than 250 µF of minimum capacitance and 5.2 mΩ of ESR.

8.2.2.2.4 Peak Current Rating of Inductor

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by Equation 25.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{T_{SS}} = \frac{1.2\text{ V}(2 \times 47\ \mu\text{F} + 220\ \mu\text{F})}{1.5\text{ ms}} = 0.251\text{ A} \quad (25)$$

$$I_{L\_PEAK} = I_{OUT(max)} + \frac{1}{2} I_{RIPPLE} + I_{CHARGE} = 20\text{ A} + \frac{1}{2} \times 6\text{ A} + 0.2512\text{ A} = 23.25\text{ A} \quad (26)$$

Table 5. Inductor Requirements

PARAMETER		VALUE	UNIT
L	Inductance	300	nH
$I_{L(rms)}$	RMS current (thermal rating)	20.07	A
$I_{L(peak)}$	Peak current (saturation rating)	23.25	A

8.2.2.2.5 Input Capacitor Selection (C8)

The input voltage ripple is divided between capacitance and ESR. For this design $V_{RIPPLE(cap)}$ = 150 mV and $V_{RIPPLE(esr)}$ = 150 mV. The minimum capacitance and maximum ESR are estimated by Equation 27.

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(CAP)} \times V_{IN} \times F_{SW}} = \frac{20 \times 1.2V}{150mV \times 8V \times 600kHz} = 33.3uF \quad (27)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(ESR)}}{I_{LOAD} + \frac{1}{2} I_{RIPPLE}} = \frac{150\ mV}{23A} = 6.5\ m\Omega \quad (28)$$

The RMS current in the input capacitors is estimated by Equation 29.

$$I_{RMS\_CIN} = I_{LOAD} \times \sqrt{D \times (1-D)} = 20\ A \times \sqrt{0.15 \times (1-0.15)} = 7.14\ Arms \quad (29)$$

Three 1210, 10-µF, 25-V, X5R ceramic capacitors are selected. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors allow sufficient capacitance at the working voltage.

8.2.2.2.6 MOSFET Switch Selection (Q1 and Q2)

Reviewing available TI NexFET MOSFETs using the TI NexFET MOSFET selection tool, the CSD16410Q5A and CSD16321Q5 5-mm × 6-mm MOSFETs are selected.

These two FETs have maximum total gate charges of 5 nC and 10 nC, respectively.

8.2.2.2.7 Bootstrap Capacitor (C6)

To ensure proper charging of the high-side FET gate, limit the ripple voltage on the boost capacitor to less than 50 mV.

$$C_{Boost} = 20 \times Q_{G1} = 20 \times 5\ nC = 100\ nF \quad (30)$$

8.2.2.2.8 VDD Bypass Capacitor (C7)

Per the TPS40304 data sheet, select a 1.0-uF X5R or better ceramic bypass capacitor for VDD.

8.2.2.2.9 BP Bypass Capacitor (C5)

Per the TPS40304 data sheet, a minimum 1.0-uF ceramic capacitance is required to stabilize the BP regulator. To limit regulator noise to less than 10 mV, the value of the bypass capacitor is calculated in Equation 31.

$$C_{BP} = 100 \times MAX(Q_{G1}, Q_{G2}) \quad (31)$$

Because Q2 is larger than Q1, and the total gate charge of Q2 is 10 nC, a BP capacitor of 1.0 µF is calculated. A standard value of 1.0 µF is selected to limit noise on the BP regulator.

8.2.2.2.10 Short-Circuit Protection (R11)

The TPS40304 uses the negative drop across the low-side FET at the end of the OFF time to measure the inductor current. Allowing for 30% over maximum load and 20% rise in $R_{DS(on)Q1}$ for self-heating, the voltage drop across the low-side FET at current limit is given by Equation 32.

$$V_{OC} = (1.3 \times I_{LOAD} - \frac{1}{2} I_{ripple}) \times 1.2 \times R_{DSONG2} = (1.3 \times 20\ A - \frac{1}{2}\ 6\ A) \times 1.2 \times 4.6\ m\Omega = 127\ mV \quad (32)$$

The TPS40304 internal temperature coefficient helps compensate for the MOSFET $R_{DS(on)}$ temperature coefficient, so the current limit programming resistor is selected by Equation 33.

$$R_{CS} = \frac{V_{OC} - V_{OCLOS(min)}}{2 \times I_{OCSET(min)}} = \frac{127\ mV - (-8\ mV)}{2 \times 9.5\ \mu A} = 7.1\ k\Omega \quad (33)$$

8.2.2.2.11 Feedback Divider (R4, R5)

The TPS40304 controller uses a full operational amplifier with an internally fixed 0.6-V reference. R4 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With R4 set to 10 kΩ, The output voltage is programmed with a resistor divider given by Equation 34.

$$R7 = \frac{V_{FB} \times R4}{V_{OUT} - V_{FB}} = \frac{0.600\ V \times 10.0\ k\Omega}{1.2\ V - 0.600\ V} = 10\ k\Omega \tag{34}$$

8.2.2.2.12 Compensation: (C2, C3, C4, R3, R6)

Using the TPS40k Loop Stability Tool for 100-kHz bandwidth and 60° phase margin with a R4 value of 10.0 kΩ, the following values are returned.

- C4 = 680 pF
- C5 = 100 pF
- C6 = 680 pF
- R1 = 10 kΩ
- R2 = 1.5 kΩ

8.2.2.3 Application Curves

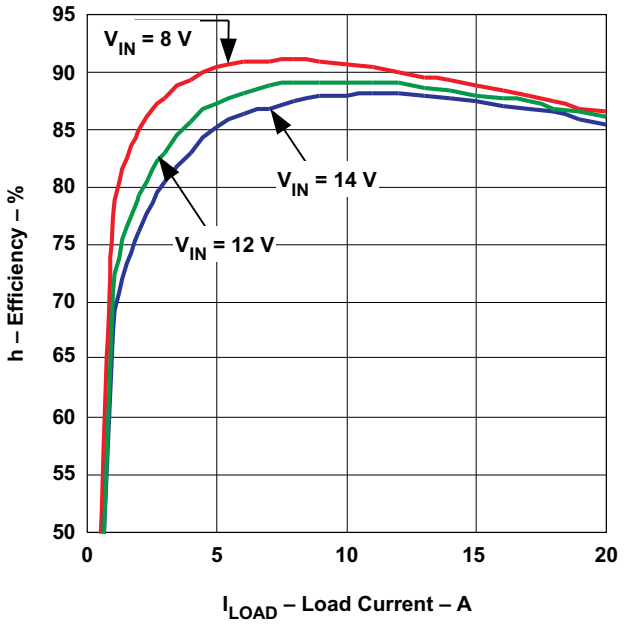


Figure 19. Efficiency vs Load Current

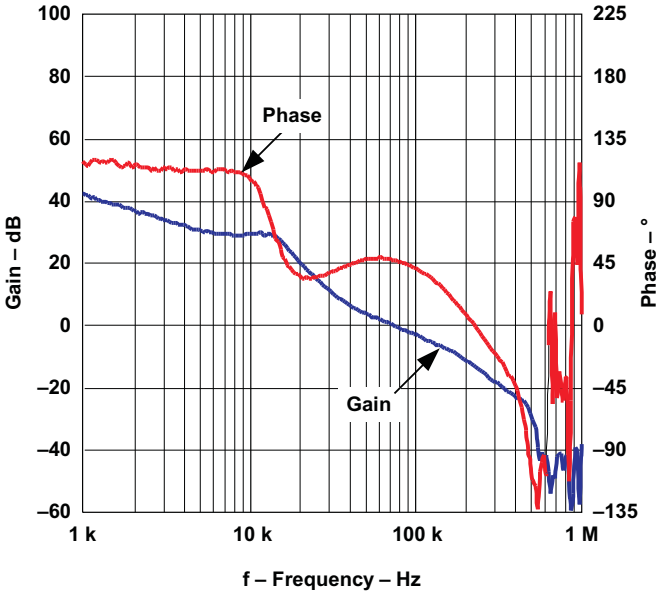


Figure 20. Gain and Phase vs Frequency

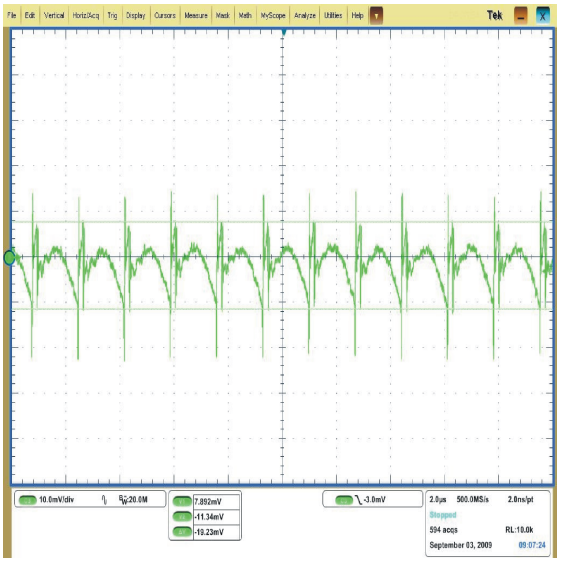


Figure 21. Output Ripple 10 mV/div, 2-µs/div, 20-MHz Bandwidth

8.2.3 A Synchronous Buck Application Using the TPS40303

Figure 22 shows a 3.3-V/5-V/12-V to 0.6-V at 10-A synchronous buck application using the TPS40303 switching at 300 kHz.

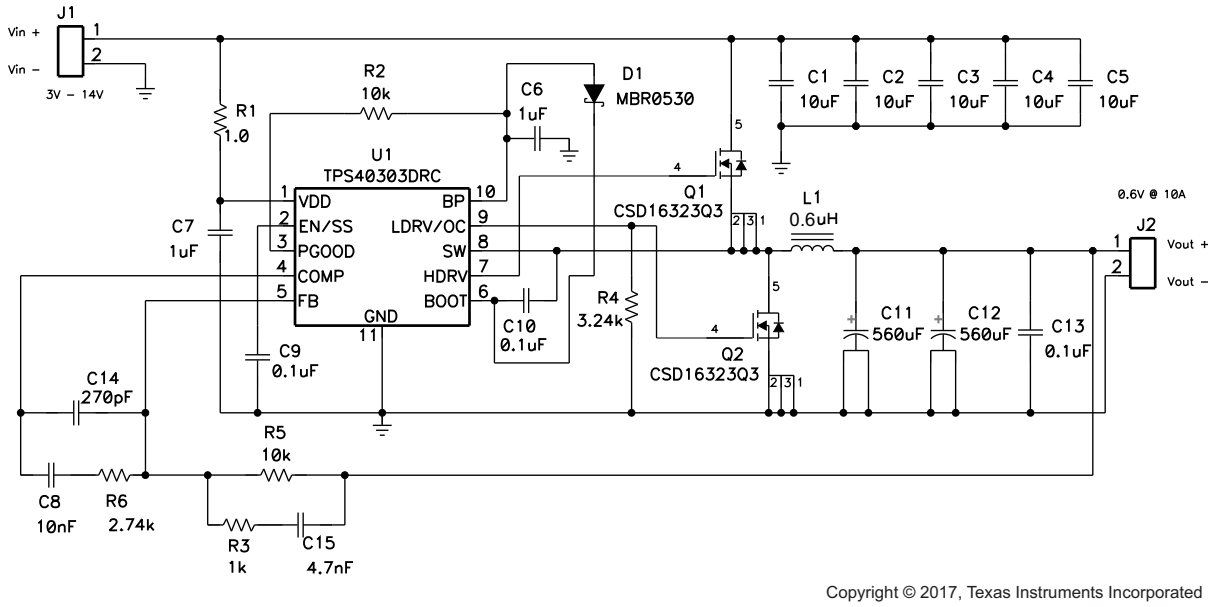


Figure 22. TPS40303 Design Example Schematic

8.2.3.1 Design Requirements

For this example, follow the design parameters listed in Table 6.

Table 6. Design Example Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		3.3		14	V
$V_{INripple}$	Input ripple	I_{OUT} = 10 A			0.6	V
V_{OUT}	Output voltage	0 A ≤I_{OUT} ≤ 10 A	0.582	0.6	0.618	V
	Line regulation	3 V ≤ V_{IN} ≤14 V			0.5%	
	Load regulation	0 A ≤I_{OUT} ≤ 10 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT} = 10 A			12	mV
V_{OVER}	Output overshoot	3 A ≤ I_{OUT} ≤ 7 A		100		mV
V_{UNDER}	Output undershoot	3 A ≤I_{OUT} ≤ 7 A		100		mV
I_{OUT}	Output current	3.3 V ≤ V_{IN} ≤ 14 V	0		10	A
t_{SS}	Soft-start time	V_{IN} = 12 V		1.5		ms
I_{SCP}	Short-circuit current trip point		13	15		A
	Efficiency	V_{IN} = 12 V, I_{OUT} = 5 A		84%		
f_{SW}	Switching frequency			300		kHz
	Size				1.5	in^2

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Selecting the Switching Frequency

To achieve the small size for this design the TPS40303, with f_{SW} = 300 kHz, is selected for minimal external component size.

8.2.3.2.2 Inductor Selection (L1)

Synchronous buck power inductors are typically sized for approximately 30% peak-to-peak ripple current (I_{RIPPLE})

Given this target ripple current, the required inductor size can be calculated in Equation 35.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{F_{SW}} = \frac{14V - 0.6V}{0.3 \times 10A} \times \frac{0.6V}{14V} \times \frac{1}{300kHz} = 638nH \quad (35)$$

Selecting a standard 600-nH inductor value, solve for I_{RIPPLE} = 3.2 A

The RMS current through the inductor is approximated by Equation 36.

$$I_{Lrms} = \sqrt{I_{Lavg}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{I_{OUT}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{10^2 + \tfrac{1}{12} 3.2^2} = 10.04A \quad (36)$$

8.2.3.2.3 Output Capacitor Selection (C12)

The selection of the output capacitor is typically driven by the output transient response. Equation 37 and Equation 38 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{I_{TRAN}^2 \times L}{V_{OUT} \times C_{OUT}} \quad (37)$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{IN} - V_{OUT}} = \frac{I_{TRAN}^2 \times L}{(V_{IN} - V_{OUT}) \times C_{OUT}} \quad (38)$$

If $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot (Equation 37) to calculate minimum output capacitance. If $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot (Equation 38) to calculate minimum output capacitance.

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^2 \times L}{(V_{OUT}) \times V_{OVER}} = \frac{4^2 \times 600\ nH}{0.6 \times 100\ mV} = 160\ \mu F \quad (39)$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 40.

$$ESR_{max} = \frac{V_{RIPPLE(Total)} - V_{RIPPLE(CAP)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}\right)}{I_{RIPPLE}} = \frac{36\ mV - \left(\frac{3.2\ A}{8 \times 160\ \mu F \times 300\ kHz}\right)}{3.2\ A} = 8.6\ m\Omega \quad (40)$$

Two 560-µF capacitors are selected to provide more than 160-µF of minimum capacitance and less than 8.6 mΩ of ESR.

8.2.3.2.4 Peak Current Rating of Inductor

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by Equation 41.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{T_{SS}} = \frac{0.6\ V(2 \times 560\,\mu F)}{1.5\ ms} = 0.448\ A \quad (41)$$

$$I_{L\_PEAK} = I_{OUT(max)} + \tfrac{1}{2} I_{RIPPLE} + I_{CHARGE} = 10A + \tfrac{1}{2} \times 3.2A + 0.448A = 12.05A \quad (42)$$

Table 7. Inductor Requirements

PARAMETER		VALUE	UNIT
L	Inductance	600	nH
$I_{L(rms)}$	RMS current (thermal rating)	10.04	A
$I_{L(peak)}$	Peak current (saturation rating)	12.05	A

8.2.3.2.5 Input Capacitor Selection (C8)

The input voltage ripple is divided between capacitance and ESR. For this design $V_{RIPPLE(cap)}$ = 150 mV and $V_{RIPPLE(esr)}$ = 150 mV. The minimum capacitance and maximum ESR are estimated by Equation 43.

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(CAP)} \times V_{IN} \times F_{SW}} = \frac{10 \times 0.6\ V}{150\ mV \times 3.3\ V \times 300\ kHz} = 40.4\ uF \quad (43)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(ESR)}}{I_{LOAD} + \tfrac{1}{2} I_{RIPPLE}} = \frac{150\ mV}{11.6\ A} = 13\ m\Omega \quad (44)$$

The RMS current in the input capacitors is estimated by Equation 45.

$$I_{RMS\_CIN} = I_{LOAD} \times \sqrt{D \times (1-D)} = 10\ A \times \sqrt{0.2 \times (1-0.2)} = 4\ Arms \quad (45)$$

Five 1210, 10-µF, 25-V, X5R ceramic capacitors with approximately 2-mΩ of ESR and a 2.5-A RMS current rating each are selected. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors allow sufficient capacitance at the working voltage.

8.2.3.2.6 MOSFET Switch Selection (Q1 and Q2)

Reviewing available TI NexFET MOSFETs using the TI NexFET MOSFET selection tool, the CSD16323Q3 and CSD16323Q3 5-mm × 6-mm MOSFETs are selected. These two FETs have maximum total gate charges of 8.4 nC.

8.2.3.2.7 Bootstrap Capacitor (C6)

To ensure proper charging of the high-side FET gate, limit the ripple voltage on the boost capacitor to less than 50 mV.

$$C_{Boost} = 20 \times Q_{G1} = 20 \times 8.4\ nC = 100\ nF \quad (46)$$

8.2.3.2.8 VDD Bypass Capacitor (C7)

Per the TPS40305 *Electrical Characteristics* specifications, select a 1.0-µF X5R or better ceramic bypass capacitor for VDD.

8.2.3.2.9 BP Bypass Capacitor (C5)

Per the TPS40303 data sheet, a minimum 1.0-uF ceramic capacitance is required to stabilize the BP regulator. To limit regulator noise to less than 10 mV, the value of the bypass capacitor is calculated in Equation 47.

$$C_{BP} = 100 \times MAX(Q_{G1}, Q_{G2}) \quad (47)$$

Because both Q1 and Q2's are the same, total gate charge is 8.4 nC, a BP capacitor of 0.84 µF is calculated. A standard value of 1.0 uF is selected to limit noise on the BP regulator.

8.2.3.2.10 Short-Circuit Protection (R11)

The TPS40305 uses the negative drop across the low-side FET at the end of the OFF time to measure the inductor current. Allowing for 30% over maximum load and 20% rise in $R_{DS(on)Q1}$ for self-heating, the voltage drop across the low-side FET at current limit is given by Equation 48.

$$V_{OC} = (1.3 \times I_{LOAD} - \frac{1}{2} I_{ripple}) \times 1.2 \times R_{DSONQ2} = (1.3 \times 10A - \frac{1}{2} 3.2A) \times 1.2 \times 4.4m\Omega = 60mV \quad (48)$$

The TPS40305 internal temperature coefficient helps compensate for the MOSFET's $R_{DS(on)}$ temperature coefficient, so the current limit programming resistor is selected by Equation 49.

$$R_{CS} = \frac{V_{OC} - V_{OCLOS(min)}}{2 \times I_{OCSET(min)}} = \frac{60\ mV - (-8\ mV)}{2 \times 9.5\ \mu A} = 3.6\ k\Omega \quad (49)$$

8.2.3.2.11 Feedback Divider (R4, R5)

The TPS40305 controller uses a full operational amplifier with an internally fixed 0.600-V reference. R5 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With R5 set to 10 kΩ, the output voltage is programmed with a resistor divider given by Equation 50. Because the feedback voltage is equal to output voltage, low-side voltage divider resistor is not needed.

$$R_{Lowside} = \frac{V_{FB} \times R5}{V_{OUT} - V_{FB}} \quad (50)$$

8.2.3.2.12 Compensation: (C2, C3, C4, R3, R6)

Using the TPS40k Loop Stability Tool for 100-kHz bandwidth and 60° phase margin with a R5 value of 10 kΩ, the following values are returned.

- C8 = 10 nF
- C14 = 270 pF
- C15 = 4.7 nF
- R6 = 2.74 kΩ
- R3 = 1 kΩ

8.2.3.3 Application Curves

A typical efficiency graph for this design example using the TPS40303 is shown in Figure 23.The typical line and load regulation this design example using the TPS40303 is shown in Figure 24

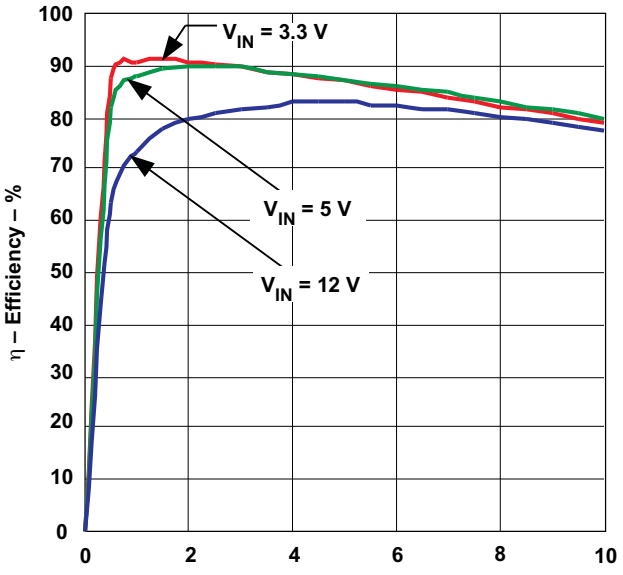


Figure 23. Efficiency vs Load Current

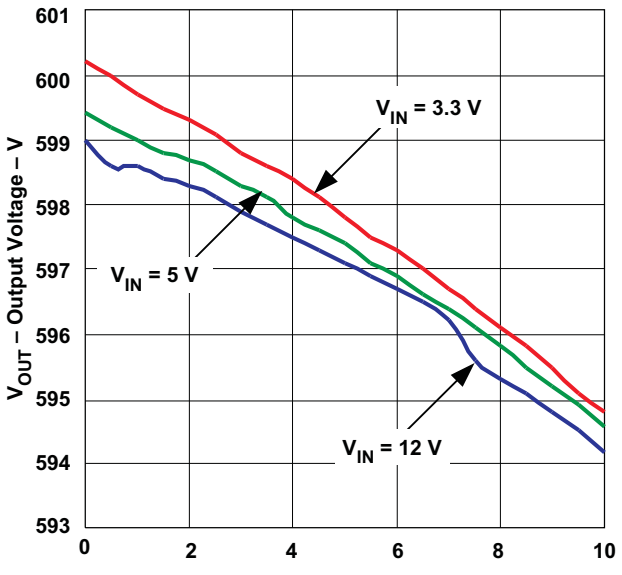


Figure 24. Line and Load Regulation

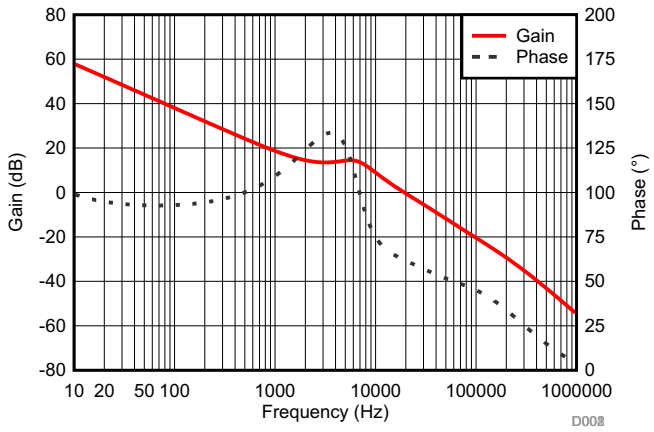


Figure 25. Total System Bode

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply between 3 V and 20 V. This input supply should remain within the input voltage supply range. This supply must be well regulated.

10 Layout

10.1 Layout Guidelines

- For MOSFET or Power Block Layout, follow the layout recommendations provided for the MOSFET or Power Block selected.
- Connect VDD to VIN as close as possible to the drain connection of the high-side FET to avoid introducing additional drop which could trigger short-circuit protection.
- Place VDD and BP to GND capacitors within 2 mm of the device and connected to the Thermal Pad (GND).
- The FB to GND resistor should connect to the thermal tab (GND) with a minimum 10-mil wide trace.
- Place VOUT to FB resistor within 2 mm of the FB pin.
- The EN/SS-to-GND capacitor must connect to the thermal tab (GND) with a minimum 10-mil-wide trace. It may share this trace with FB to GND.
- If a BJT or MOSFET is used to disable EN/SS, place it within 5 mm of the device.
- If a COMP to GND resistor is used, place it within 5 mm of the device.
- All COMP and FB traces should be kept minimum line width and as short as possible to minimize noise coupling.
- Do not route EN/SS more than 20 mm from the device.
- If multiple layers are used, extend GND under all components connected to FB, COMP and EN/SS to reduce noise sensitivity.
- HDRV and LDRV should provide short, low inductance paths of 5 mm or less to the gates of the MOSFETs or Power Block.
- No more than 1 Ω of resistance should be placed between HDRV or LDRV and their MOSFET or Power Block gate pins.
- LDRV / OC to GND Current Limit Programming resistor may be placed on the far side of the MOSFET if necessary to ensure a short connection from LDRV to the gate of the low-side MOSFET.
- The BOOT to SW resistor and capacitor should both be placed within 4 mm of the device using a minimum of 10-mil-wide trace. The full width of the component pads are preferred for trace widths if design rules allow.
- If via must be used between the HDRV, SW and LDRV pins and their respective MOSFET or Power Block connections, use a minimum of two vias to reduce parasitic inductance
- Refer to the Land Pattern Data for the preferred layout of thermal vias within the thermal pad.
- It is recommended to extend the top-layer copper area of the thermal pad (GND) beyond the package a minimum 3 mm between pins 1 and 10 and 5 and 6 to improve thermal resistance to ambient of the device.

10.2 Layout Example

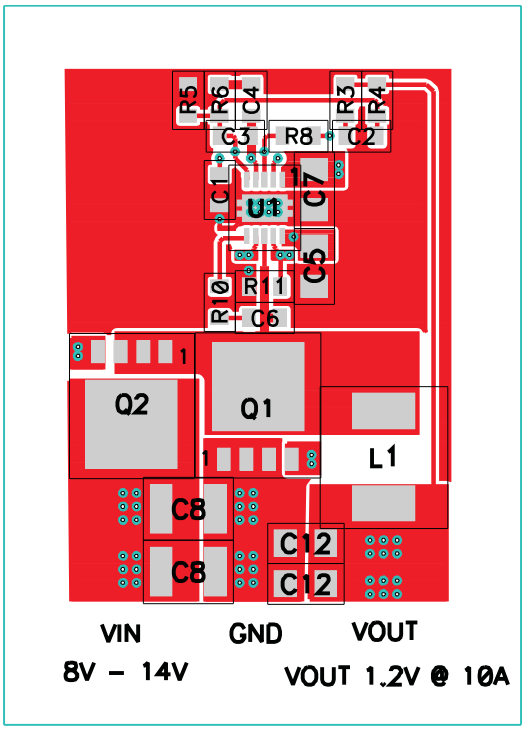


Figure 26. Top Copper With Components

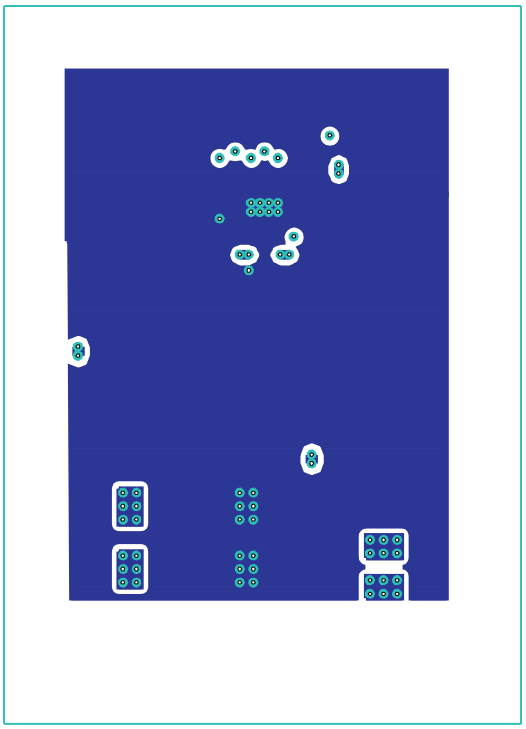


Figure 27. Top Internal Copper Layout

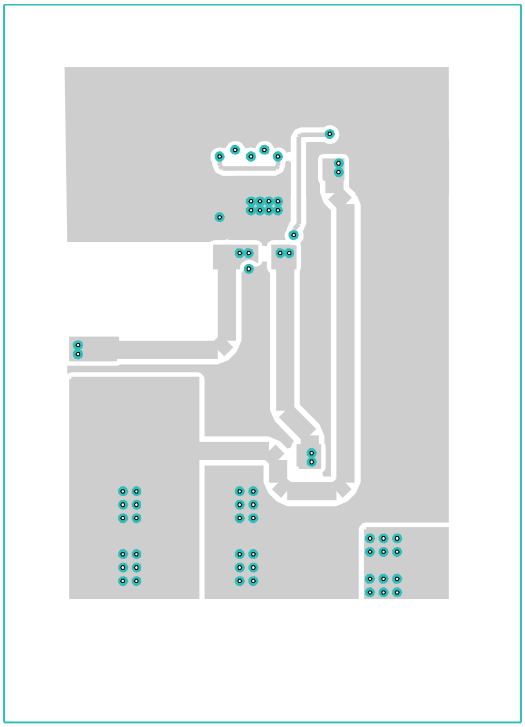


Figure 28. Bottom Internal Copper Layout

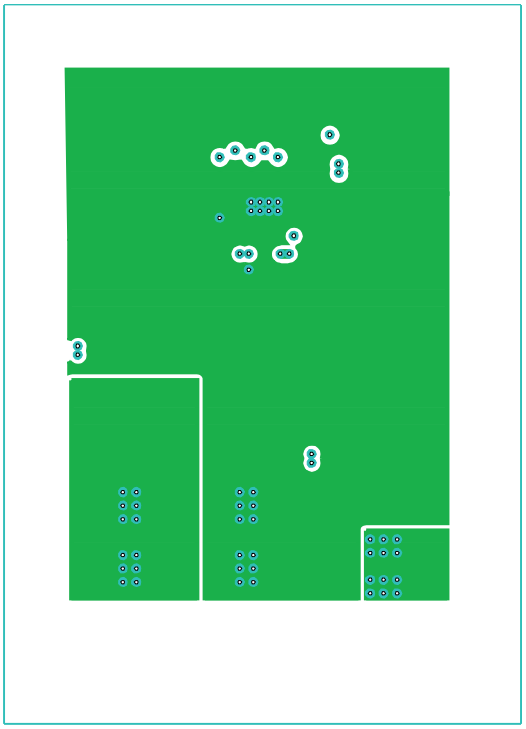


Figure 29. Bottom Copper Layer

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

11.2 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPS4030xデバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.3 ドキュメントのサポート

11.3.1 関連資料

以下の参照資料、設計ツール、および設計ソフトウェアを含む他の参考資料へのリンクは、http://power.ti.comにあります。

1. PowerPAD™に関する詳細情報はアプリケーション・ブリーフ(SLMA002およびSLMA004)に記載されています。
2. *『低電圧DC/DCコンバータの内部構造』*、2002セミナー・シリーズ、SEM1500トピック5
3. *『スイッチモード電源における降圧電力ステージについて』*、(SLVA057)、1999年3月
4. *『安定した制御ループの設計』*、2001セミナー・シリーズ、SEM1400

11.4 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS40303	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS40304	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS40305	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.5 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.6 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.7 商標

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WEBENCH is a registered trademark of Texas Instruments.
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11.8 静電気放電に関する注意事項

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11.9 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40303DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	0303
TPS40303DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0303
TPS40303DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	0303
TPS40303DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0303
TPS40304DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	0304
TPS40304DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0304
TPS40304DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	0304
TPS40304DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	0304
TPS40305DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	0305
TPS40305DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0305
TPS40305DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	0305
TPS40305DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0305

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

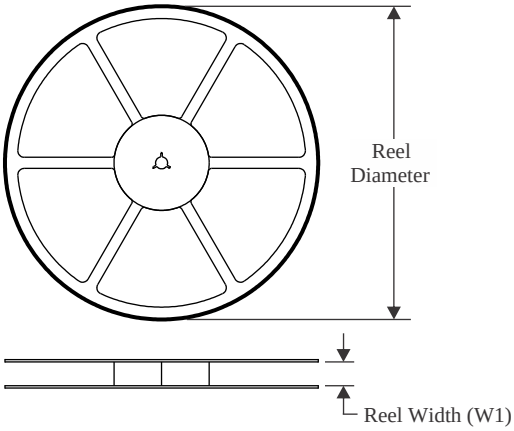
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

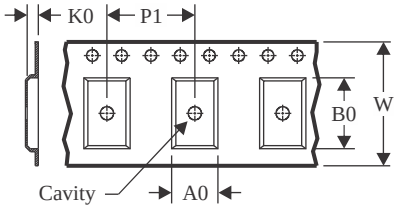
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

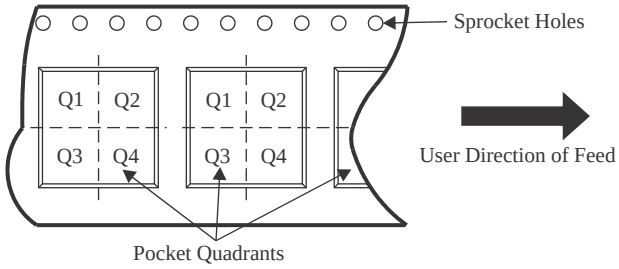


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

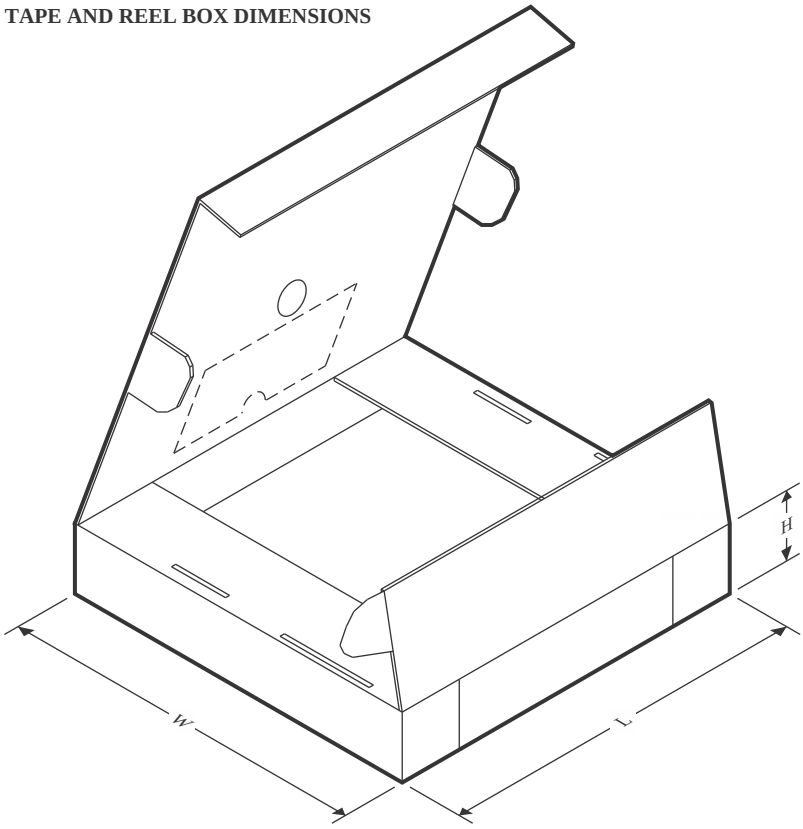
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40303DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40303DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40304DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40304DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS40305DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40305DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40303DRCR	VSON	DRC	10	3000	353.0	353.0	32.0
TPS40303DRCT	VSON	DRC	10	250	213.0	191.0	35.0
TPS40304DRCR	VSON	DRC	10	3000	338.0	355.0	35.0
TPS40304DRCT	VSON	DRC	10	250	338.0	355.0	35.0
TPS40305DRCR	VSON	DRC	10	3000	338.0	355.0	35.0
TPS40305DRCT	VSON	DRC	10	250	338.0	355.0	35.0

GENERIC PACKAGE VIEW

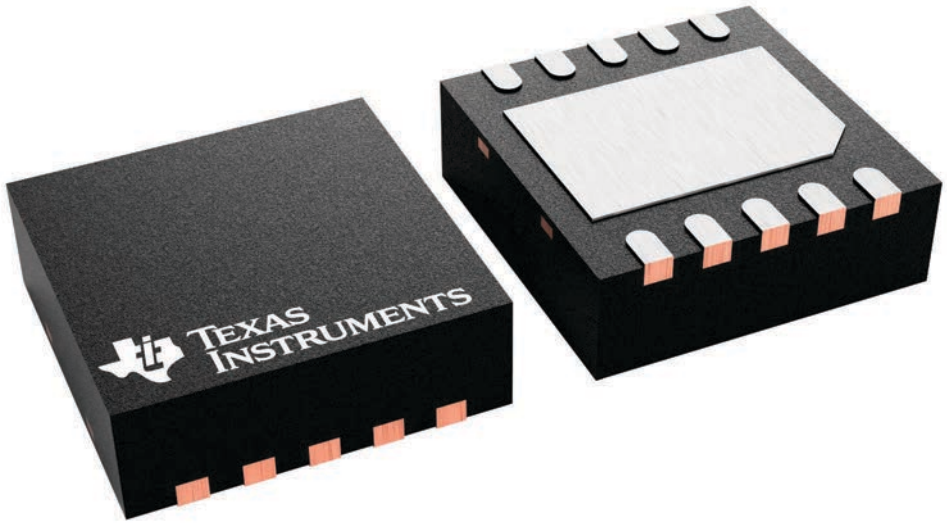
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



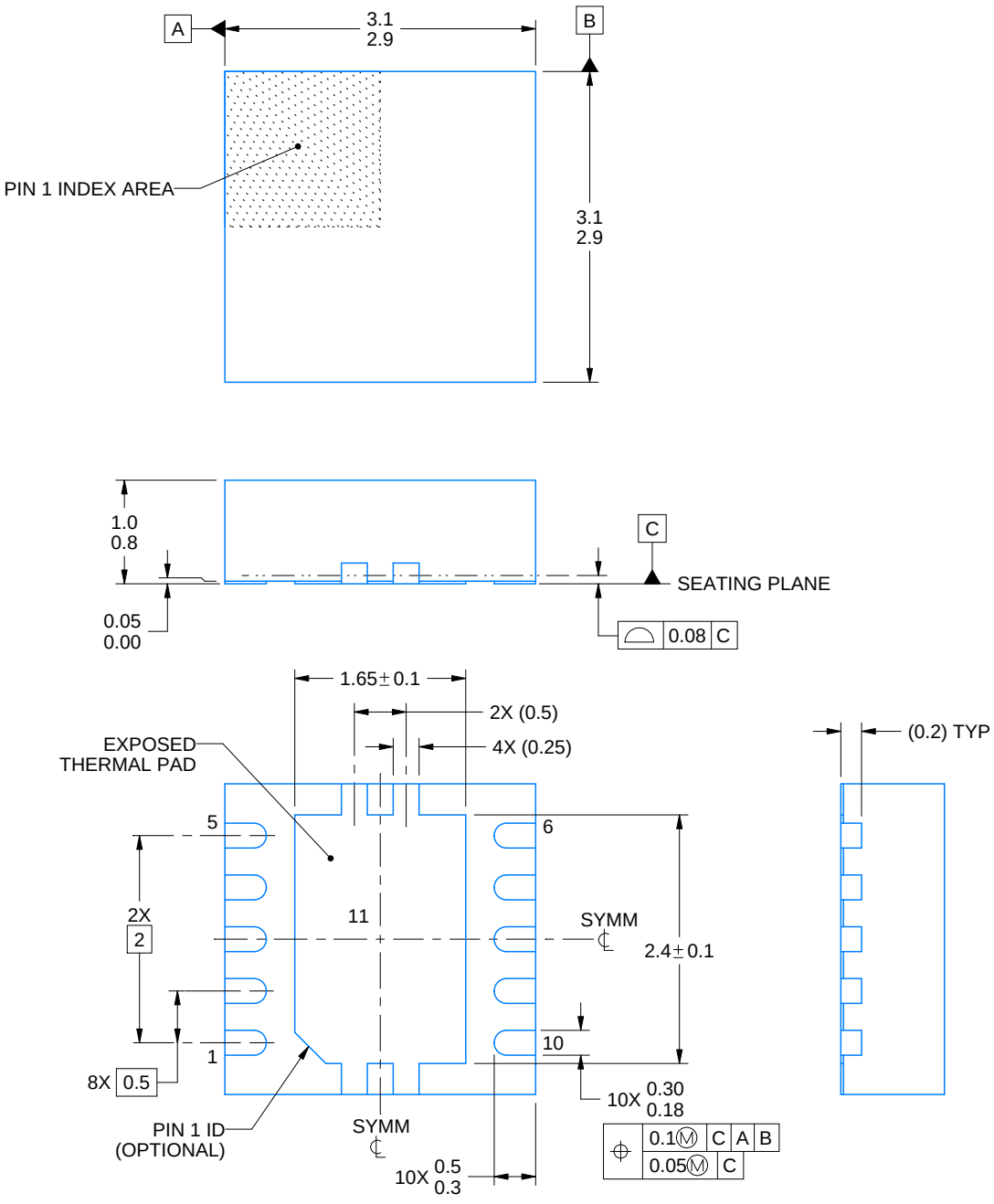
4226193/A

DRC0010J

PACKAGE OUTLINE

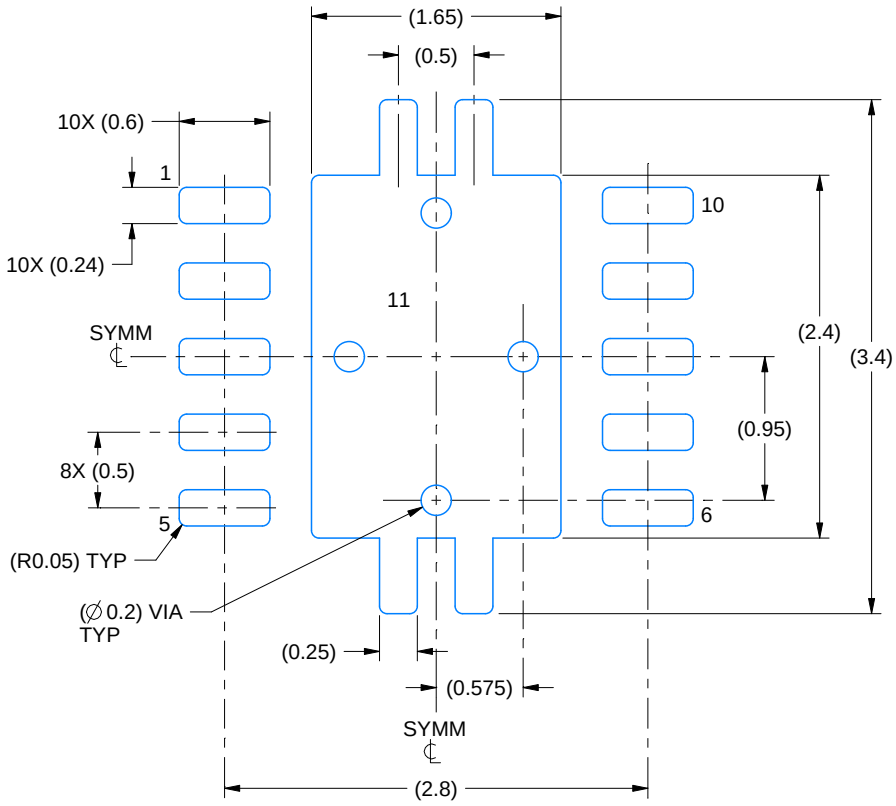
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

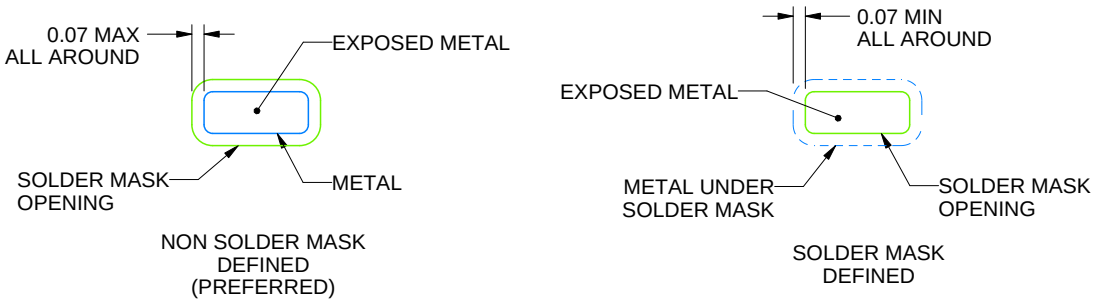


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

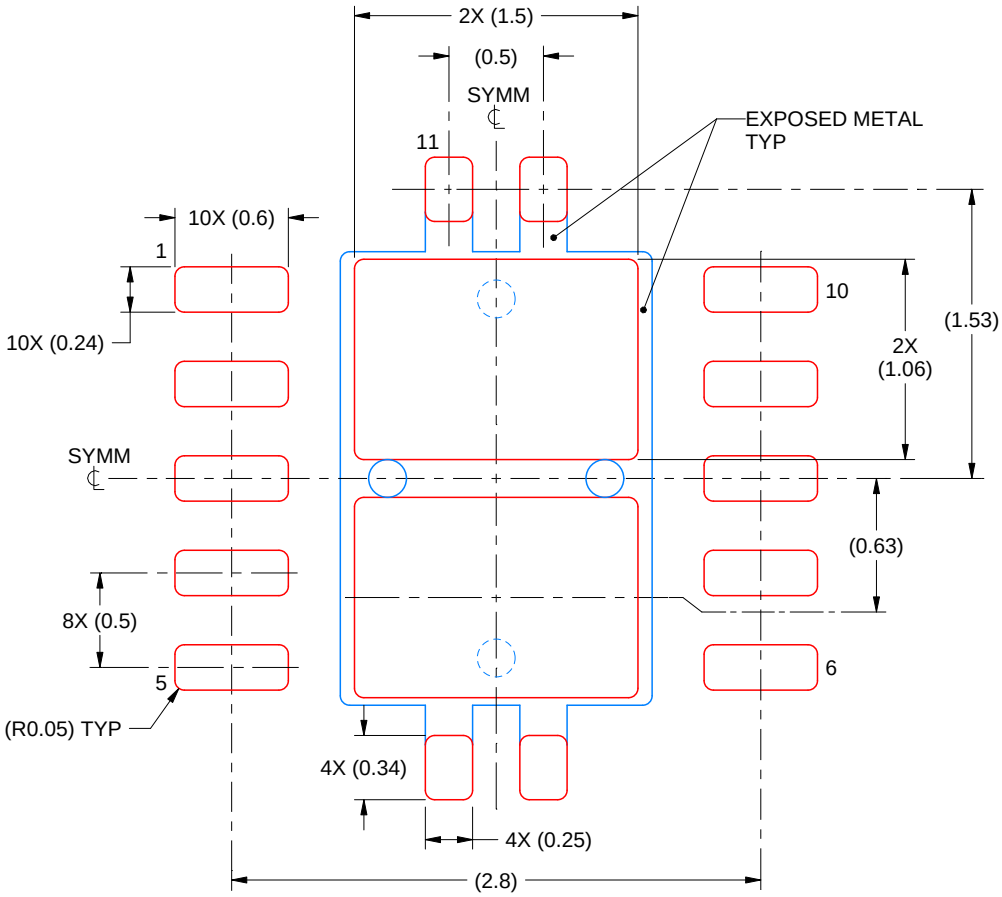
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月