TPS4141-Q1 Automotive 1200V Configurable Precision Resistor Divider With Integrated Switch

1 Features

- Qualified for automotive applications
  - AEC-Q100 grade 1: –40°C to 125°C ambient operating temperature
- Integrated high-voltage resistor divider
  - 30MΩ total resistance, precision matched divider
  - No exposed high-impedance nodes improves measurement integrity from board contaminants
- Integrated high-voltage disconnect switch
  - 1200V standoff voltage, uni-directional blocking
  - < 1.5μA leakage at T_A = 105°C
- Integrated precision amplifier
  - Buffered output for easy interfacing to analog-to-digital converters
  - Dynamically selectable gain settings to maximize accuracy across high-voltage sensing range
- Measurement accuracy: ±0.25%
- Support for uni-directional and bi-directional voltage sensing up to ±1200V
- Dynamic switching between uni-directional and bi-directional voltage sensing operation
- Low supply current
  - 5mA ON state current
  - 5.5μA OFF state current
- SOIC (DWQ-11) package
  - Creepage and clearance ≥ 8mm from high-voltage sensing pin to all other pins

2 Applications

- Hybrid, electric, and power train systems
- Battery management systems (BMS)
- Solar energy

3 Description

The TPS4141-Q1 is a high-voltage, precision matched resistor divider with an integrated programmable-gain amplifier. The TPS4141-Q1 also integrates a high-voltage switch to allow for connecting or disconnecting the high-voltage sense pin and provides uni-directional current blocking when disconnected. The device is designed for automotive and industrial applications where accurate, high-voltage measurements are required.

The TPS4141-Q1 programmable-gain amplifier supports four divider ratios using DIV0 and DIV1 inputs. DIV0 and DIV1 can be set to fixed divider ratios and may also be changed dynamically while in operation. This allows for matching the amplifier output (AOUT) to the full-scale input voltage of the analog-to-digital signal chain, improving accuracy over the entire voltage sensing range of interest.

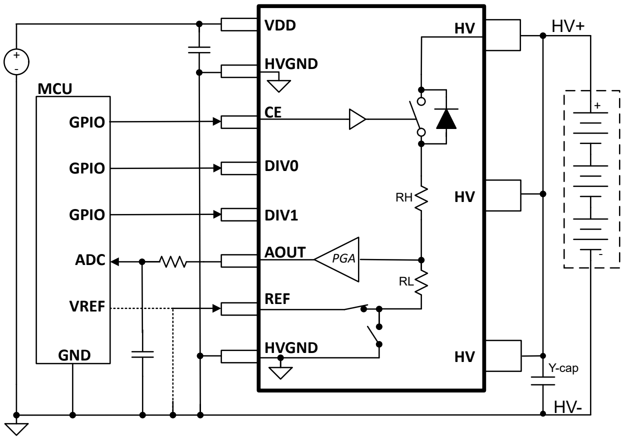
The TPS4141-Q1 supports uni-directional or bi-directional voltage measurement. Bi-directional voltage measurement is supported by supplying an external precision voltage reference from REF to HVGND. Switching between bi-directional and uni-directional voltage sensing during operation is possible using DIV0 and DIV1. Connecting REF to HVGND provides uni-directional voltage sensing only.

The TPS4141-Q1 integrates a high-voltage switch with a standoff voltage greater than 1200V from the high-voltage sense pin (HV) to ground (HVGND). The switch provides uni-directional current blocking from HV to HVGND when disconnected.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS4141-Q1[3]	DWQ (SOIC, 11)	10.30mm × 10.30mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product preview.



TPS4141-Q1 Simplified Application Schematic

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4 Pin Configuration and Functions

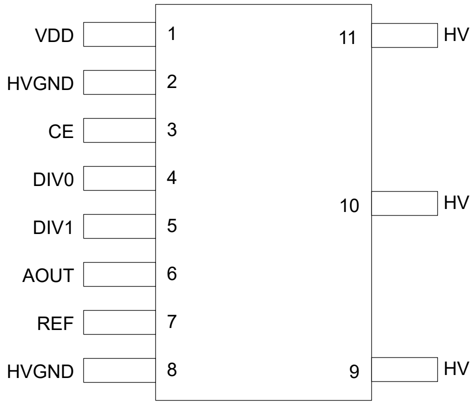


Figure 4-1. TPS4141-Q1 DWQ Package, 11-Pin SOIC-WB (Top View)

4.1 Pin Functions TPS4141-Q1

PIN NO.	PIN NAME	TYPE[1]	DESCRIPTION
1	VDD	P	Power supply
2	HVGND	GND	HV ground supply. Connect all HVGND pins to HV ground supply.
3	CE	I	Active high chip enable signal
4	DIV0	I	Trinary input for divider ratio selection
5	DIV1	I	Trinary input for divider ratio selection
6	AOUT	O	Amplifier output from HV resistor divider
7	REF	I	Reference for bottom of resistor divider, connect to external reference for bi-directional sensing or to HVGND.
8	HVGND	GND	HV ground supply. Connect all HVGND pins to HV ground return.
9	HV	I/O	High-voltage input. All HV pins must be connected in the application.
10			
11			

(1) P = power, I = input, O = output, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
V_{VDD}	Supply voltage(2)	–0.3	20.7	V
$V_{CE,\ DIV0,\ DIV1}$	Chip enable and tri-state inputs voltage(2)	–0.3	20.7	V
$V_{AOUT,\ REF}$	Resistor divider reference input and buffered resistor divider output(2)	–0.3	6	V
V_{HV}	High voltage input(2)	–1400	1400	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltage values are with respect to HVGND.

5.2 ESD Ratings

				VALUE	UNIT
HBM	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	All pins	±2000	V
CDM	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4	All pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{VDD}	Primary side supply voltage(1)	4.5		20	V
$V_{CE,\ DIV0,\ DIV1}$	Chip enable, divider selection input voltages(1)	0		20	V
V_{AOUT}	Buffered resistor divider output(1)	0		4.1	V
V_{REF}	Reference for bottom of resistor divider(1)	0		3.2	V
V_{HV}	Switch input voltage(1)	–1200		1200	V
R_{AOUT}	External series resistance on AOUT(2)	100		900	Ω
C_{AOUT}	External capacitance on AOUT(2)	1		200	nF
T_A	Ambient operating temperature	–40		125	°C
T_J	Junction operating temperature	–40		150	°C

(1) Voltage values are with respect to HVGND.
(2) External low pass RC filter from AOUT to HVGND.

5.4 Thermal Information

THERMAL METRIC (1)		TPS4141-Q1	UNIT
		DWQ (SOIC)	
		11 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC [1]		TPS4141-Q1 DWQ (SOIC) 11 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	21	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, total (VDD and HV supplies)	V_{VDD} = 5V, V_{CE} = 5V peak to peak, V_{HV} = 1200V f_{CE} = 1Hz square wave			110	mW
P_{D_VDD}	Maximum power dissipation (VDD supply)				50	mW
P_{D_HV}	Maximum power dissipation (HV supply)				60	mW

5.6 Electrical Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25℃, V_{VDD} = 5V, V_{CE} = 5V, C_{AOUT} = 1nF, R_{AOUT} = 100Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRECISION RESISTOR DIVIDER AND AMPLIFIER						
R_{TOTAL}	Resistance from HV to HVGND or HV to REF.		25.5	30	34.5	MΩ
DIV_{NOM}	Nominal divide ratio	DIV1 = L, DIV0 = L		160		V/V
		DIV1 = L, DIV0 = H		320		V/V
		DIV1 = H, DIV0 = L		640		V/V
		DIV1 = H, DIV0 = H		1000		V/V

5.6 Electrical Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25℃, V_{VDD} = 5V, V_{CE} = 5V, C_{AOUT} = 1nF, R_{AOUT} = 100Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$GAIN_{ERROR}$ (1)	DIV = 160V/V setting. Nominal gain = 1/DIV.	T_J = 25°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 640V Bi-directional measurement: –302V ≤ V_{HV} ≤ 322V, V_{REF} = 2.0V	–0.15		0.15	%
		–40°C ≤ T_J ≤ 150°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 640V Bi-directional measurement: –302V ≤ V_{HV} ≤ 322V, V_{REF} = 2.0V	–0.25		0.25	%
	DIV = 320V/V setting. Nominal gain = 1/DIV.	T_J = 25°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 1200V Bi-directional measurement: –606V ≤ V_{HV} ≤ 642V, V_{REF} = 2.0V	–0.15		0.15	%
		–40°C ≤ T_J ≤ 150°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 1200V Bi-directional measurement: –606V ≤ V_{HV} ≤ 642V, V_{REF} = 2.0V	–0.25		0.25	%
	DIV = 640V/V setting. Nominal gain = 1/DIV.	T_J = 25°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 1200V Bi-directional measurement: –1200V≤ V_{HV} ≤ 1200V, V_{REF} = 2.0V	–0.15		0.15	%
		–40°C ≤ T_J ≤ 150°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 1200V Bi-directional measurement: –1200V≤ V_{HV} ≤ 1200V, V_{REF} = 2.0V	–0.25		0.25	%
	DIV = 1000V/V setting. Nominal gain = 1/DIV.	T_J = 25°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 1200V Bi-directional measurement: –1200V≤ V_{HV} ≤ 1200V, V_{REF} = 2.0V	–0.15		0.15	%
		–40°C ≤ T_J ≤ 150°C Uni-directional measurement: 110V ≤ V_{HV} ≤ 1200V Bi-directional measurement: –1200V≤ V_{HV} ≤ 1200V, V_{REF} = 2.0V	–0.25		0.25	%
V_{OFFSET_HV}	Measurement offset voltage referred to HV input.	–40°C ≤ T_J ≤ 150°C	–240		240	mV
CMR_{AIN}	Amplifier common mode input range		0		3.2	V
CMR_{AOUT}	Amplifier common mode output range		0		4.1	V
BW_{HV_REF}	Measurement bandwidth - HV to AOUT, REF to AOUT	DIV = 160		7		kHz
		DIV = 320		14		kHz
		DIV = 640		28		kHz
		DIV =1000		47		kHz
$I_{SC,AOUT}$	Short circuit current - AOUT to HVGND/REF.	V_{VDD} = 5V, V_{CE} = 5V		±15		mA
SUPPLY (VDD)						
V_{UVLO_R}	VDD undervoltage threshold rising	VDD rising	4	4.2	4.4	V
V_{UVLO_F}	VDD undervoltage threshold falling	VDD falling	3.9	4.1	4.3	V

5.6 Electrical Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25℃, V_{VDD} = 5V, V_{CE} = 5V, C_{AOUT} = 1nF, R_{AOUT} = 100Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO_HYS}	VDD undervoltage threshold hysteresis			150		mV
I_{VDD_ON}	VDD current, device powered on	T_J = 25°C		5		mA
		–40°C ≤ T_J ≤ 150°C		5	7	mA
I_{VDD_OFF}	VDD current, device powered off	V_{VDD} = 5V, V_{CE} = 0V, T_J = 25°C		5.5	8	µA
		V_{VDD} = 5V, V_{CE} = 0V, –40°C ≤ T_J ≤ 150°C			48	µA
		V_{VDD} = 20V, V_{CE} = 0V, T_J = 25°C		10	20	µA
		V_{VDD} = 20V, V_{CE} = 0V, –40°C ≤ T_J ≤ 150°C			60	
SWITCH CHARACTERISTICS						
I_{OFF}	Off leakage	CE = L, V_{HV} = 1200V, T_J = 25°C		0.02	0.15	µA
		CE = L, V_{HV} = 1200V, T_J = 85°C			0.5	
		CE = L, V_{HV} = 1200V, T_J = 105°C			1.5	
		CE = L, V_{HV} = 1200V, T_J = 125°C			6	
		CE = L, V_{HV} = 1200V, –40°C ≤ T_J ≤ 150°C			50	
BV_{VDSS}	Switch breakdown voltage.	I_{HV} = 1µA, –40°C ≤ T_J ≤ 150°C CE = L	1270	1550		V
C_{OSS}	HV capacitance	V_{HV} = 0V, f = 1MHz		50		pF
LOGIC-LEVEL INPUT (CE, DIV0, DIV1)						
$V_{IL, CE}$	Chip enable input logic low voltage		0.0		0.8	V
$V_{IH, CE}$	Chip enable input logic high voltage		2.4		20.0	V
$V_{HYS, CE}$	Chip enable input logic hysteresis			250		mV
$V_{IL, DIVx}$	DIV0/DIV1 input logic for low state				0.8	V
$V_{IM, DIVx}$	DIV0/DIV1 input logic for mid state		1.3		1.8	V
$V_{IH, DIVx}$	DIV0/DIV1 input logic for high state		2.4			V
I_{IL_CE}	Input logic low current	V_{CE} = 0V	–0.1		0.1	µA
		V_{CE} = 0.8V	2	4	6.5	µA
I_{IH_CE}	Input logic high current	V_{CE} = 5V	10	22	50	µA
		V_{CE} = 20V	100	175	350	µA
I_{IL_DIVx}	Input logic low current	V_{DIVx} = 0V	–22	–15	–9	µA
		V_{DIVx} = 0.8V	–11	–7	–4	µA
I_{IM_DIVx}	Input logic mid current	V_{DIVx} = 1.3V	–3	–2	–1	µA
		V_{DIVx} = 1.8V	1.3	2.4	5	µA
I_{IH_DIVx}	Input logic high current	V_{DIVx} = 2.4V	4	8	23	µA
		V_{DIVx} = 5V	9	17	32	µA
		V_{DIVx} = 20V	9	17	32	µA
R_{PD_CE}	Pull down resistance on CE		100	200	350	kΩ
R_{PU_DIVx}	Pull up resistance on DIV0, DIV1		200	300	400	kΩ

5.6 Electrical Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25℃, V_{VDD} = 5V, V_{CE} = 5V, C_{AOUT} = 1nF, R_{AOUT} = 100Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD_DIVx}	Pull down resistance on DIV0, DIV1		80	120	280	kΩ

(1) Computed gain error (%) = $100 \times [DIV_{nom} (V_{AOUT,HV\_max} – V_{AOUT,HV\_min}) / (V_{HV\_max} – V_{HV\_min}) – 1]$

5.7 Switching Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25℃, V_{VDD} = 5V, V_{CE} = 5V, C_{AOUT} = 1nF, R_{AOUT} = 100Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Characteristics						
t_{ON}	CE rising to AOUT settles to 1% of steady state value.	V_{HV} = 300V, DIV = 160, CE = L → H		840		µs
t_{OFF}	CE falling to AOUT pulled down to HVGND.	V_{HV} = 300V, DIV = 160, CE = H → L Measure when AOUT reaches 100mV referenced to HVGND.		285		µs
$t_{DIV\_TOGGLE\_STEP}$	Transition time from present DIV setting to next DIV setting to AOUT settles to 0.25% of steady state value.	V_{HV} = 300V, V_{REF} = 0V or 2V. DIV = 160→320, DIV = 320→160 or DIV = 320→640, DIV = 640→320 or DIV = 640→1000, DIV = 1000→640.		30		µs
t_{DIV_TOGGLE}	Transition time from lowest DIV setting to highest DIV setting to AOUT settles to 0.25% of steady state value	V_{HV} = 300V, V_{REF} = 0V or 2V. DIV = 160→1000, DIV = 1000→160.		310		µs

6 Detailed Description

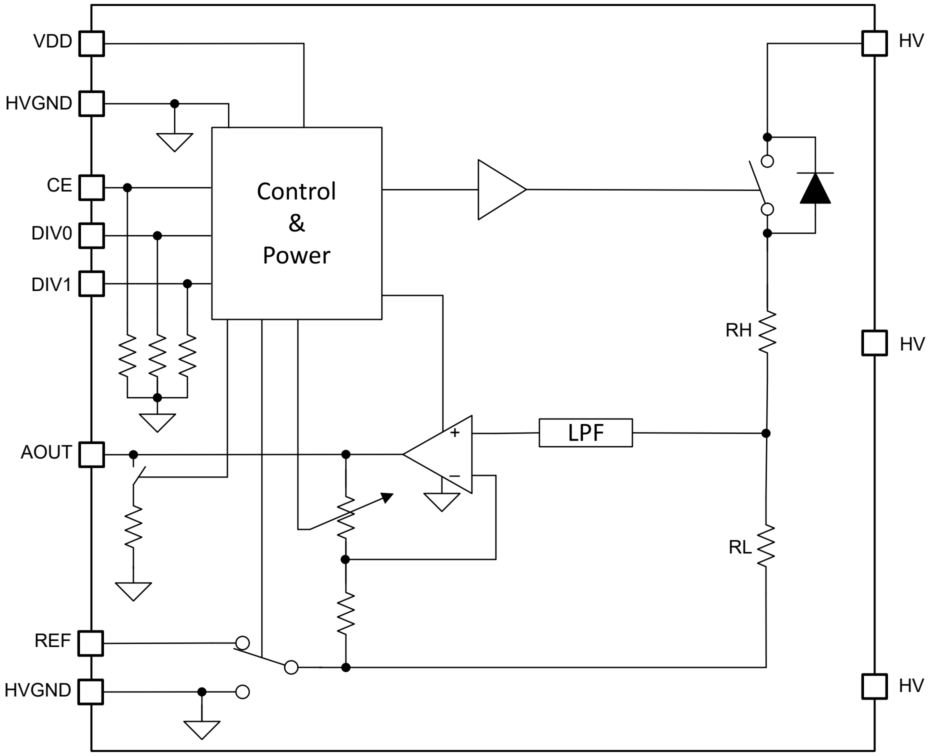
6.1 Overview

The TPS4141-Q1 is a high-voltage, precision matched resistor divider with an integrated programmable-gain amplifier. The TPS4141-Q1 also integrates a high-voltage switch to allow for connecting or disconnecting the high-voltage sense pin and provides uni-directional current blocking when disconnected. The device is designed for automotive and industrial applications where accurate, high-voltage measurements are required.

As seen in the *Functional Block Diagram* section, the TPS4141-Q1 integrates a high-voltage switch, two high-voltage resistors that form a precision matched divider, and a programmable gain amplifier (PGA). When the switch is enabled, a resistance (R_{TOTAL}) is presented between HV to HVGND or HV to REF.

The programmable gain amplifier has different gain settings. The gain settings, selectable via DIV0 and DIV1, in combination with the resistor divider, form an overall divide ratio (DIV) of the voltage present on the high-voltage pin (HV referenced to HVGND or REF). The resulting attenuated voltage is presented on AOUT relative to HVGND or REF. Four different divider ratios are possible. The divider ratios can be configured to be fixed via the DIV0 and DIV1 applied voltages or can be changed dynamically in the application.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Uni-directional Voltage Sensing

The TPS4141-Q1 can be configured for uni-directional voltage sensing as shown in Figure 6-1. With uni-directional voltage sensing, REF is normally connected to HVGND. When configured in this manner, the TPS4141-Q1 measures only positive voltages present on HV referenced to HVGND, for example, 0V to 1200V. The output voltage of AOUT will always be positive with respect to HVGND.

DIV0 and DIV1 select the divide ratio (DIV) of the TPS4141-Q1 and can be changed dynamically in the application. This allows for optimization of the AOUT output swing over the complete voltage range present on HV, thereby improving overall accuracy.

The range of voltages that can be measured accurately depends on the divider ratio selected by DIV0 and DIV1. Refer to the *High Voltage Input Range* section for supported ranges.

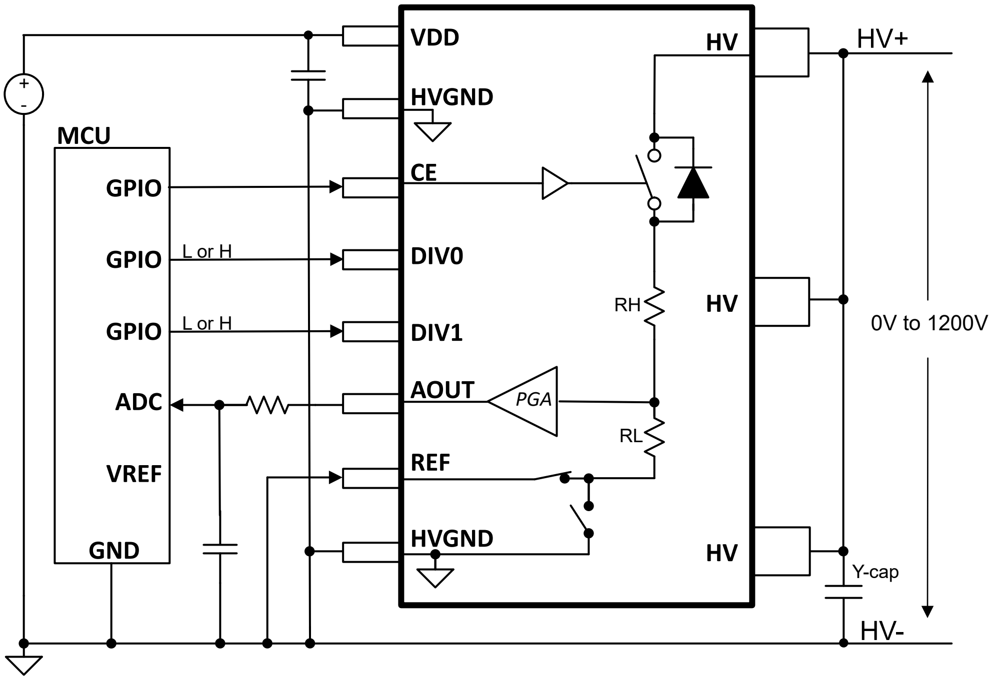


Figure 6-1. Uni-directional Voltage Sensing

6.3.2 Bi-directional Voltage Sensing

The TPS4141-Q1 can also be configured for bi-directional voltage sensing as shown in Figure 6-2. With bi-directional voltage sensing, REF is connected to an external precision voltage reference to offset the output voltage swing of the TPS4141-Q1 amplifier. With bi-directional voltage sensing, the TPS4141-Q1 can measure both positive and negative voltages present on HV referenced to HVGND, for example –1200V to 1200V. The voltage output of AOUT will swing above and below the applied voltage reference, V_{REF}.

DIV0 and DIV1 select the divide ratio (DIV) of the TPS4141-Q1 and can be changed dynamically in the application. This allows for optimization of the AOUT output swing over the complete voltage range present on HV, thereby improving overall accuracy.

The range of voltages that can be measured accurately depends on the divider ratio selected by DIV0 and DIV1, and reference voltage applied to REF. Refer to the *High Voltage Input Range* section for supported ranges. Normally, the external reference voltage is chosen to allow for symmetry of allowable ranges that can be supported for positive and negative input voltages, however this is not required.

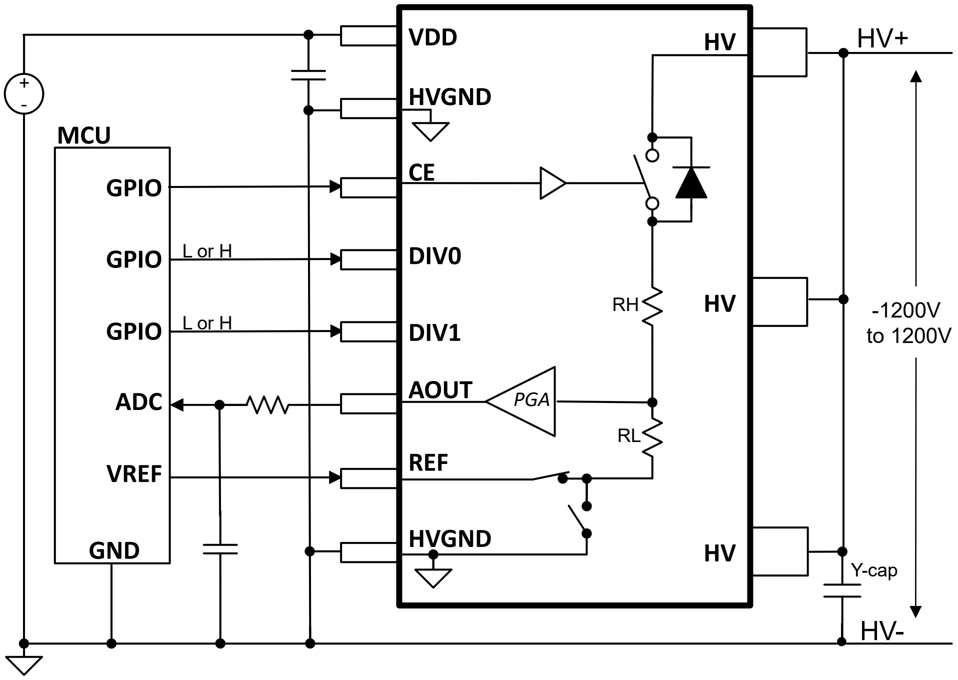


Figure 6-2. Bi-directional Voltage Sensing

6.3.3 Bi-directional and Uni-directional Voltage Sensing

The TPS4141-Q1 can also dynamically switch between uni-directional and bi-directional voltage sensing. REF is connected to an external precision voltage reference, identical to the bi-directional configuration.

DIV0 and DIV1 pins are trinary inputs in that they can detect a logic low or high, as well as a Hi-Z condition present on their respective pins. The states of the DIV0 and DIV1 pins not only select the divide ratio (DIV), but also configure the device for bi-directional or uni-directional voltage sensing. When in bi-directional operation, the external reference voltage present on the REF pin is used and the TPS4141-Q1 can measure both positive and negative voltages present on HV referenced to HVGND, for example, –1200V to 1200V. The voltage output of AOUT will swing above and below the voltage present on the REF pin. When in uni-directional operation, the external reference voltage is bypassed internal to the device and HVGND is used as the reference and the TPS4141-Q1 can measure only positive voltages present on HV referenced to HVGND, for example, 0V to 1200V. The voltage output of AOUT will always be positive referenced to HVGND. These cases are shown in Figure 6-3 and Figure 6-4.

The range of voltages that can be measured accurately depends on the divider ratio selected by DIV0 and DIV1, and reference voltage applied to REF. Refer to the *High Voltage Input Range* section for supported ranges. Normally, the external reference voltage is chosen to allow for symmetry of allowable ranges that can be supported for positive and negative input voltages, however this is not required.

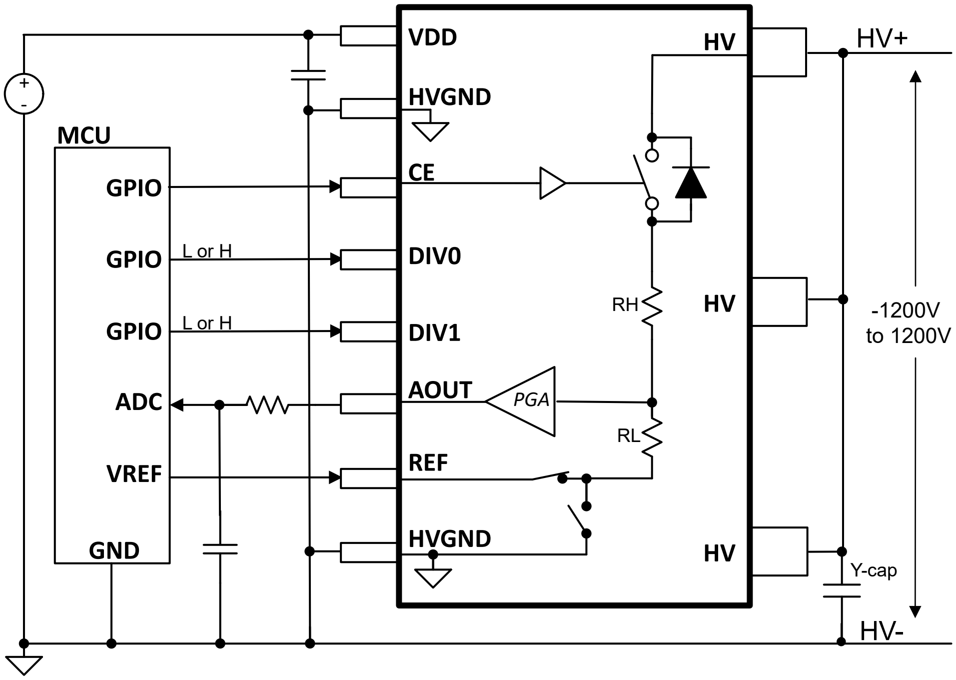


Figure 6-3. Bi-directional Voltage Sensing (DIV0 and DIV1 Set Logic Low or High)

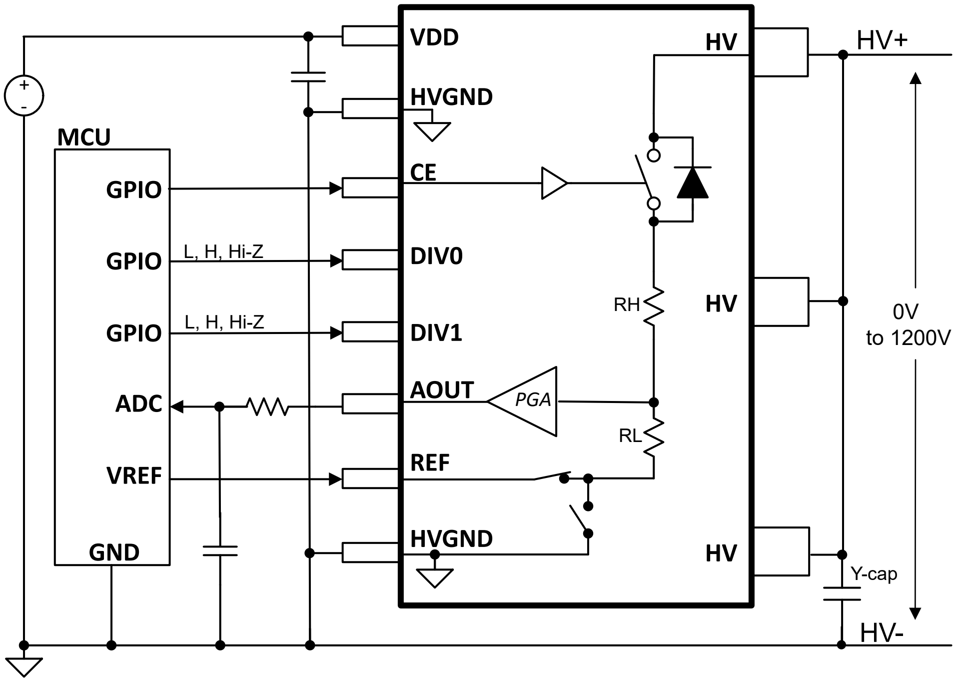


Figure 6-4. Bi-directional to Uni-directional Voltage Sensing (DIV0 and DIV1 Set Logic Low, High, or Hi-Z)

6.3.4 High Voltage Input Range

The input voltages on HV, V_{HV}, that can be sensed accurately by the TPS4141-Q1 depends on the DIV ratio selected and the REF voltage applied, V_{REF}. The common mode input and output voltage ranges of the integrated amplifier limit V_{HV} voltages that can be supported. Exceeding these ranges, cause the amplifier input or output to saturate.

The amplifier common mode output range, CMR_{AOUT}, limits the range of output voltages the amplifier can drive to AOUT. The voltage of AOUT is limited to $CMR_{AOUT(min)}$ to $CMR_{AOUT(max)}$ with respect to HVGND. Similarly, the amplifier common mode input range, CMR_{AIN}, limits the range of input voltages the amplifier can amplify. The input swing is limited to $CMR_{AIN(min)}$ to $CMR_{AIN(max)}$ with respect to HVGND.

The range of voltages that can be measured accurately depends on the divider ratio selected by DIV0 and DIV1 and the external reference voltage applied to REF. Figure 6-5 shows the typical characteristic of input ranges supported. For each DIV setting, a pair of curves is shown. The top curve corresponds to the upper bound of the V_{HV} voltage for the selected DIV setting and the bottom curve corresponds to the lower bound of the V_{HV} voltage.

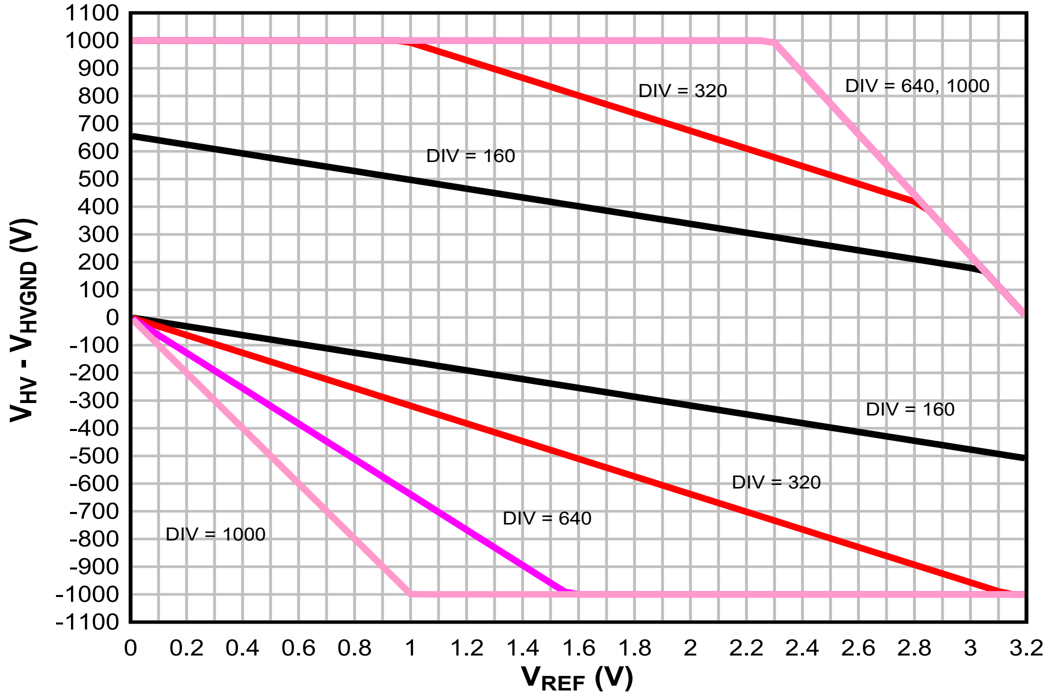


Figure 6-5. HV Input Ranges Supported

6.3.5 Calculating the Output Voltage (V_{AOUT})

There are several error sources that contribute to the overall measurement error of the system. These include, but are not limited, to the following:

- TPS4141-Q1 HV input offset error, V_{OFFSET_HV}.
- TPS4141-Q1 HV gain error, $GAIN_{ERROR}$.
- Reference absolute accuracy, REF_{ACC}.

Assuming no error sources, Equation 1 can be used to estimate the AOUT voltage (V_{AOUT}):

$$V_{AOUT} = \frac{V_{HV} - V_{REF}}{DIV_{NOM}} + V_{REF} \tag{1}$$

When including above error sources, Equation 2 can be used to estimate the AOUT voltage for V_{REF}, V_{HV}, and DIV_{NOM} values of interest:

$$V_{AOUT} = \left(1 \pm \frac{GAIN_{ERROR}}{100}\right) \times \left[\frac{(V_{HV} \pm V_{OFFSET\_HV}) - (V_{REF} \pm REF_{ACC})}{DIV_{NOM}}\right] + (V_{REF} \pm REF_{ACC}) \tag{2}$$

For uni-directional operation (V_{REF} = 0V), Equation 2 simplifies to Equation 3:

$$V_{AOUT} = \left(1 \pm \frac{GAIN_{ERROR}}{100}\right) \times \left[\frac{(V_{HV} \pm V_{OFFSET\_HV})}{DIV_{NOM}}\right] \qquad (3)$$

6.4 Device Functional Modes

Table 6-1. Device Functional Modes

VDD	CE(3)	V_{REF} (3)	DIV1(3)	DIV0(3)	DIV(3)	FUNCTION
Powered Up(1)	L	X	X	X	—	VDD current is in OFF state range. Resistor divider and AOUT buffer DISABLED.
	H	0 to 3.2V(4)	L	L	160	Bi-directional voltage sensing. VDD current is in ON state range. Resistor divider and AOUT buffer ENABLED.
			L	H	320	
			H	L	640	
			H	H	1000	
Powered Up(1)	H	X	L	Hi-Z	160	Uni-directional voltage sensing. VDD current is in ON state range. Resistor divider and AOUT buffer ENABLED.
			H	Hi-Z	320	
			Hi-Z	H	640	
			Hi-Z	L or Hi-Z	1000	
Powered Down(2)	X	X	X	X	—	VDD current is in OFF state range.

(1) VDD ≥ VDD undervoltage rising threshold.
(2) VDD ≤ VDD undervoltage falling threshold.
(3) X: do not care; L: logic low; H: logic high; Hi-Z: high-impedance.
(4) Refer to the *High Voltage Input Range* section for input ranges supported for a given V_{REF}.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS4141-Q1 is a high-voltage, precision matched resistor divider with an integrated programmable-gain amplifier. The TPS4141-Q1 also integrates a high-voltage switch to allow for connecting or disconnecting the high-voltage sense pin (HV) and provides uni-directional current blocking when disconnected. Intended applications include, but not limited to, are high-voltage monitoring in solar panels, electric vehicle (EV) chargers, EV battery management systems (BMS), and energy storage systems (ESS). The device is designed for automotive and industrial applications where accurate, high-voltage measurements are required.

The TPS4141-Q1 supports an input voltage range of 4.5V to 20V on the supply pin and a logic high of 2V to 20V on the CE, DIV0, and DIV1 pins. The TPS4141-Q1 supports up to 1200V uni-directional voltage sensing and up to ±1200V bi-directional voltage sensing when an external reference voltage is supplied on REF.

7.2 Typical Application

Figure 7-1 shows a simplified circuit diagram using TPS4141-Q1 in a system for high voltage measurement. TPS4141-Q1 interfaces with the BQ79731-Q1 UIR sensor that contains an integrated delta-sigma ADC. In this example, both the TPS4141-Q1 and BQ79731-Q1 reside in the high voltage domain with their respective grounds connected to the battery ground, BAT- (HVGND = AVSS = BAT-).

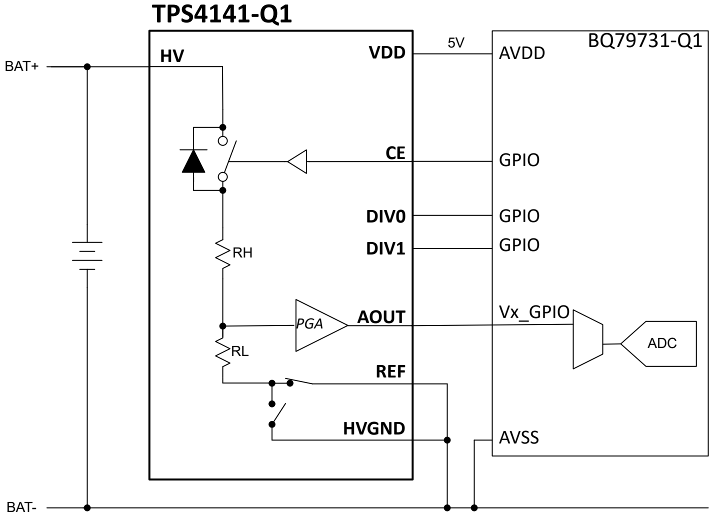


Figure 7-1. DC Bus Measurement With the TPS4141-Q1 and BQ79731-Q1

7.2.1 Design Requirements

Table 7-1 lists the Design Requirements for a typical high voltage measurement using a low voltage MCU to control the TPS4141-Q1. It assumes the MCU resides on the HVGND (ground of the high voltage domain).

Table 7-1. Design Requirements TPS4141-Q1 HV Measurement

PARAMETER	VALUE
V_{HV} voltage range	0V to 1000V
Supply (V_{VDD})	5V ±5%
ADC full scale input range	5V
ADC absolute measurement error	±1.5mV

7.2.2 Detailed Design Procedure

7.2.2.1 Divider Ratio Selection

In this example, the HV input range is positive with respect to BAT-, so the TPS4141-Q1 is configured for uni-directional operation as shown in Figure 7-2.

The divider ratio can be determined by referencing Figure 6-5. A divider ratio that maximizes the AOUT voltage range that is within the ADC full scale input range should be selected. With V_{REF} = 0V (REF = HVGND), the lowest divider ratio that can be used is DIV_{NOM} = 320V/V. Higher divider ratios are possible, but these reduce the AOUT voltage range with respect to the available ADC full scale input range.

DIV0 and DIV1 are used to select the nominal divider ratio. For applications that dynamically change the divider ratio in operation, these pins can be controlled by general purpose I/O of the MCU. For static divider ratio settings, DIV0 and DIV1 can be connected to the supply or ground thereby saving MCU general purpose I/O for other purposes. For this design, the divider ratio is assumed static, so DIV0 is connected to VDD and DIV1 is connected to HVGND.

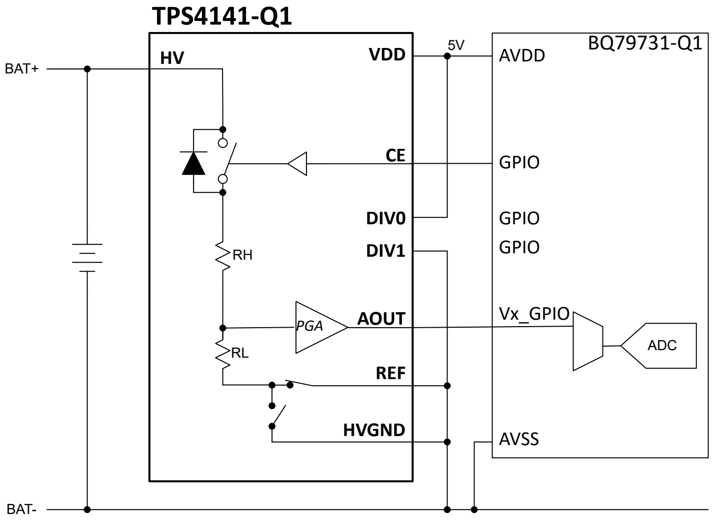


Figure 7-2. Uni-directional Measurement, DIV_{NOM} = 320V/V

If the application requires both positive and negative HV voltages to be measured with respect to BAT-, the TPS4141-Q1 can be configured for bi-directional operation as shown in Figure 7-3. An external 2.048V (V_{REF}) voltage reference is applied to REF which shifts the AOUT voltage to be centered around V_{REF}. DIV_{NOM} is increased to 640V/V to support a HV input range of –1000V to 1000V.

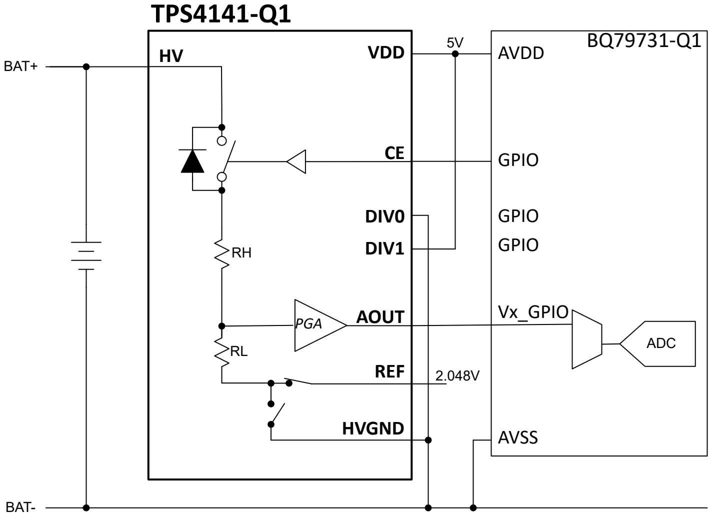


Figure 7-3. Bi-directional Measurement, DIV_{NOM} = 640V/V

7.2.2.2 Error Estimation

The following error sources are used to estimate the total measurement error:

- TPS4141-Q1 HV input offset error, V_{OFFSET_HV}, ±240mV.
- TPS4141-Q1 HV gain error, $GAIN_{ERROR}$, ±0.25%.
- ADC absolute accuracy, ADC_{ACC}. For BQ79731-Q1, ±1.5mV.

For uni-directional operation, Equation 3 is used to estimate the maximum and minimum AOUT voltage for a full scale range of V_{HV} = 1000V and DIV_{NOM} = 320V/V:

$$V_{AOUT} = (1 \pm 0.0025) \times \left[\frac{1000V \pm 0.24V)}{320}\right] \tag{4}$$

$$V_{AOUT\_MAX} = 3.13356V \quad V_{AOUT\_MIN} = 3.11644V \tag{5}$$

The AOUT voltage with no error source contribution (V_{AOUT_IDEAL}) can be found using Equation 1 with V_{REF} = 0V:

$$V_{AOUT\_IDEAL} = \frac{1000V}{320} = 3.125V \tag{6}$$

Using V_{AOUT_MAX}, V_{AOUT_MIN}, and V_{AOUT_IDEAL}, the total full scale range percentage error is ±0.274%. This may also be found by directly using Equation 7:

$$\%ERROR_{UNI} = \pm 100\% \times \left[\left(1 + \frac{GAIN_{ERROR}}{100}\right) \times \left(1 + \frac{V_{OFFSET_{HV}}}{V_{HV}}\right) - 1\right] \tag{7}$$

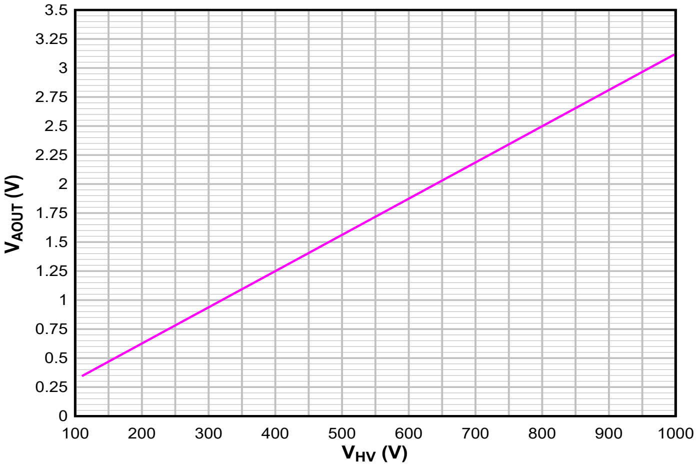
$$\%ERROR_{UNI} = \pm 100\% \times \left[\left(1 + \frac{0.25}{100}\right) \times \left(1 + \frac{0.24}{1000}\right) - 1\right] = \pm 0.274\% \tag{8}$$

The ADC measurement error at full scale range is:

$$\%ERROR_{ADC} = \pm 100\% \times \left(\frac{1.5mV}{3.125V}\right) = \pm 0.048\% \tag{9}$$

Adding these error contributions leads to a total error of ±0.322%.

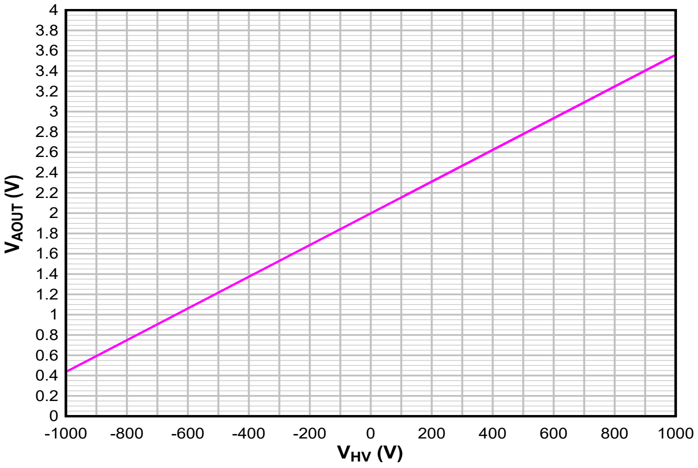
7.2.3 Application Curves



Uni-directional VDD = 5.0V T_A = 25°C

V_{REF} = 0V DIV_{NOM} = 320V/V

Figure 7-4. Transfer Function, Uni-directional Measurement



Bi-directional VDD = 5.0V T_A = 25°C

V_{REF} = 2.048V DIV_{NOM} = 640V/V

Figure 7-5. Transfer Function, Bi-directional Measurement

7.3 Power Supply Recommendations

To help ensure a reliable supply voltage, TI recommends that bypass capacitors be placed between VDD and HVGND. This capacitance consists of a 0.1µF bypass capacitor for high frequency decoupling in parallel with a 1µF capacitor for low frequency decoupling. Low-ESR and low-ESL capacitors must be connected close to the device as possible (<5mm).

7.4 Layout

7.4.1 Layout Guidelines

Component placement:

Decoupling capacitors intended for the filtering of high frequency signals must be placed as close as possible to the device pins. This action reduces the effect of trace inductance and achieves a cleaner signal.

EMI considerations:

To minimize EMI, capacitance placed between HV and HVGND will provide a low impedance path for any common mode noise generated by the device. In many applications, some form of capacitance may be present already and sufficient for this purpose.

IEC ESD considerations:

To improve robustness to meet IEC ESD contact discharge, capacitance can be placed from HV to HVGND. When doing so, this capacitance can serve a dual purpose to improve ESD and EMI performance. Typically, three to four series capacitors may be required to meet creepage and clearances, pending the system voltage.

High-voltage considerations:

To ensure high voltage spacing between HV and HVGND, avoid placing PCB or copper below the device. Proper placements and routing of signals to HV and all low voltage pins must be maintained to meet creepage and clearance standards.

Thermal considerations:

Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).

7.4.2 Layout Example

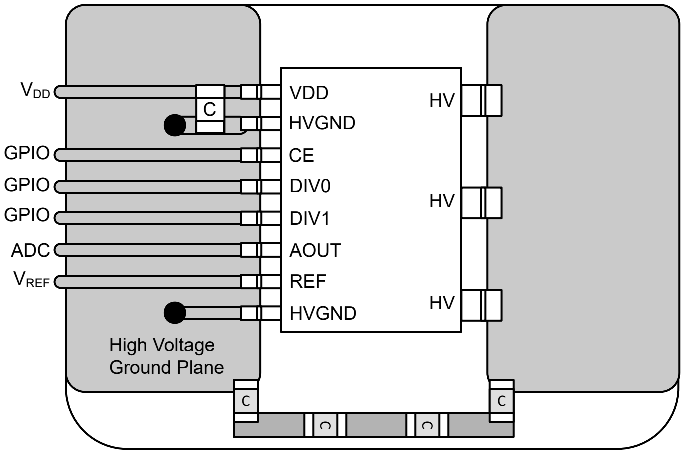


Figure 7-6. TPS4141-Q1 Example Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

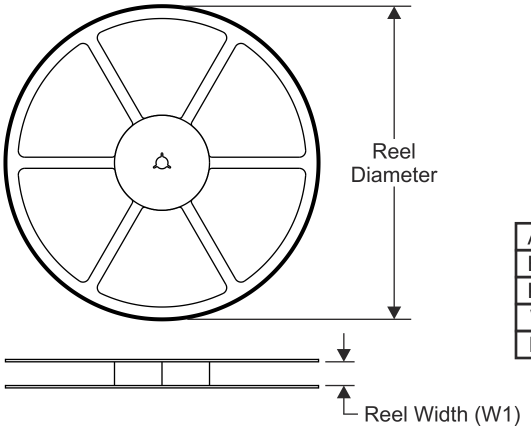
DATE	REVISION	NOTES
February 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

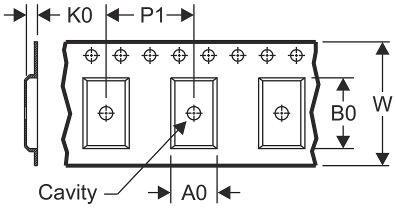
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

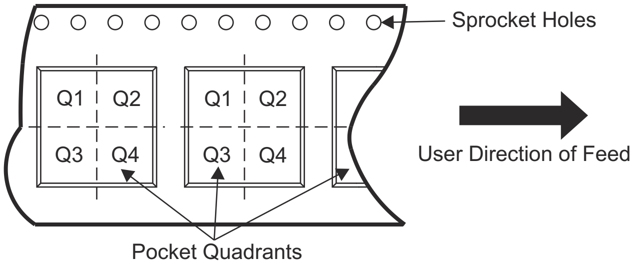


TAPE DIMENSIONS



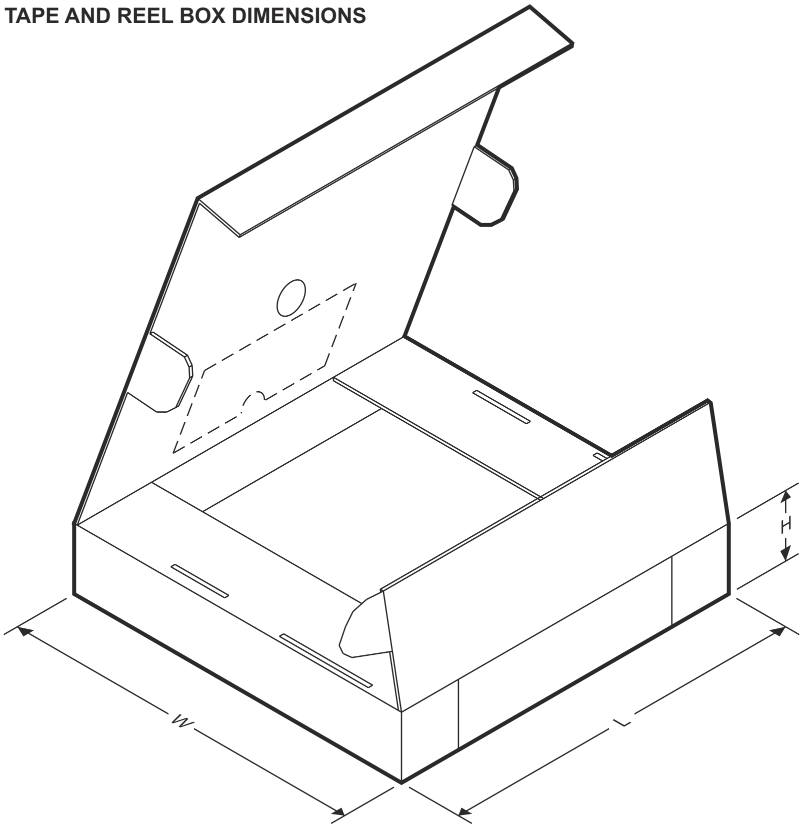
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTPS4141QDWQR	SOIC	DWQ	11	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



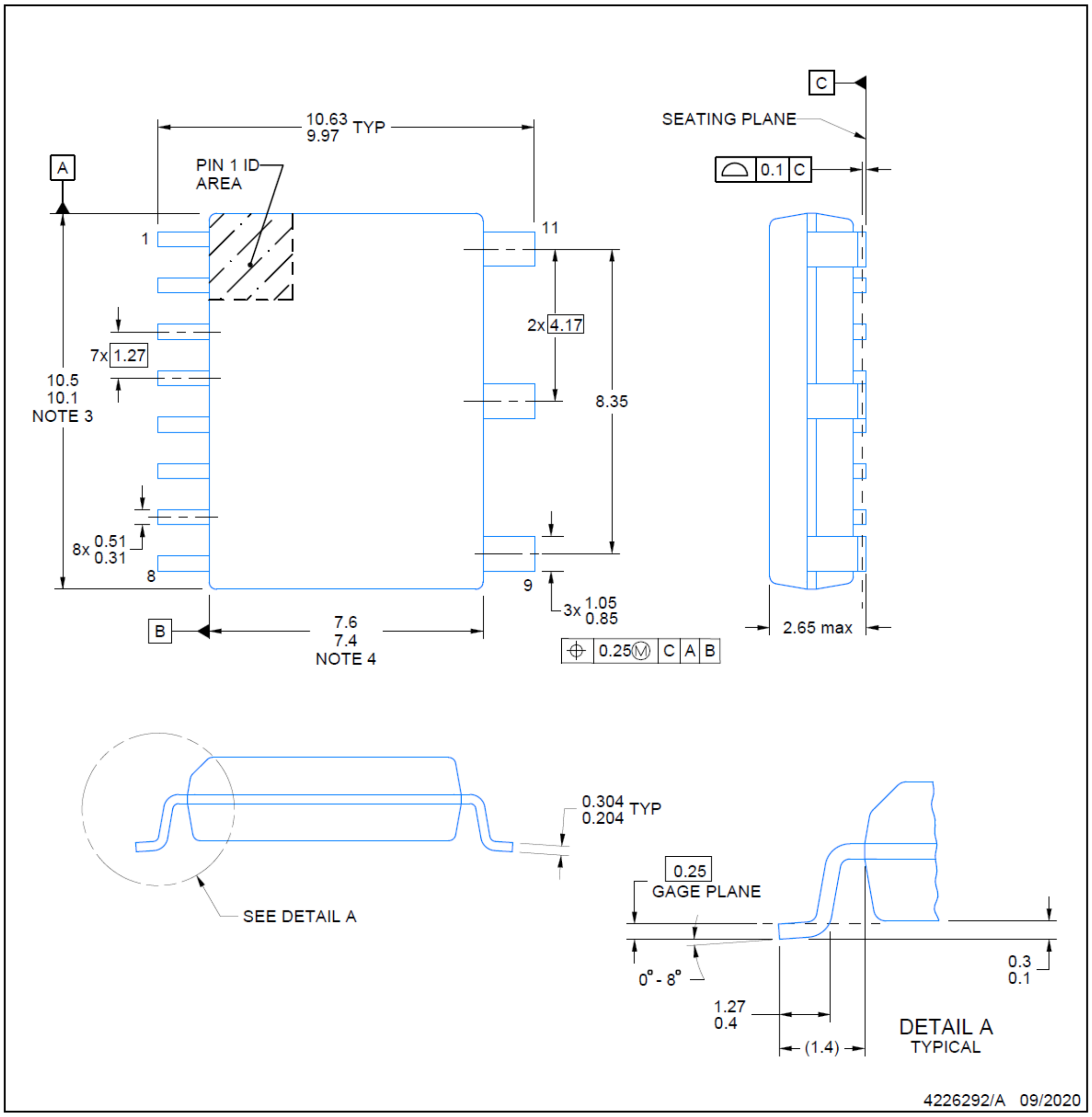
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTPS4141QDWQR	SOIC	DWQ	11	1000	350.0	350.0	43.0

PACKAGE OUTLINE

DWQ0011A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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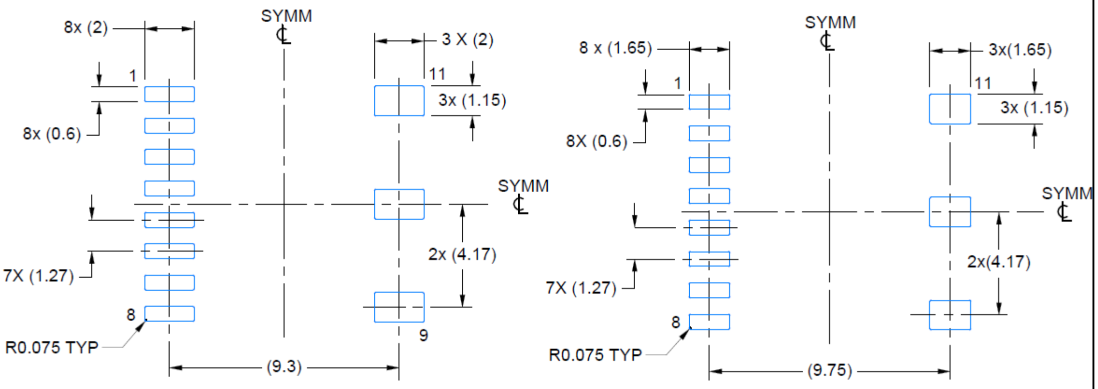
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DWQ0011A **SOIC - 2.65 mm max height**

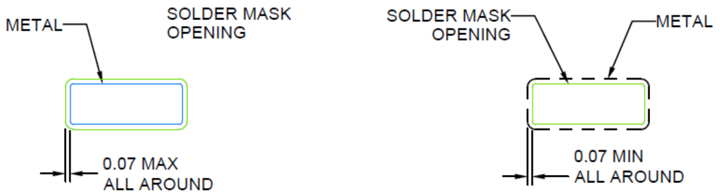
SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226292/A 09/2020

NOTES: (continued)

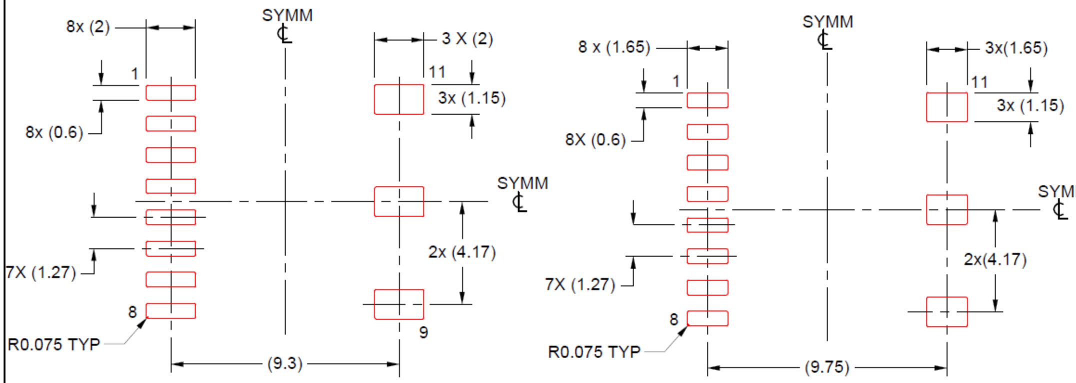
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWQ0011A

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4226292/A 09/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTPS4141QDWQRQ1	ACTIVE	SOIC	DWQ	11	1000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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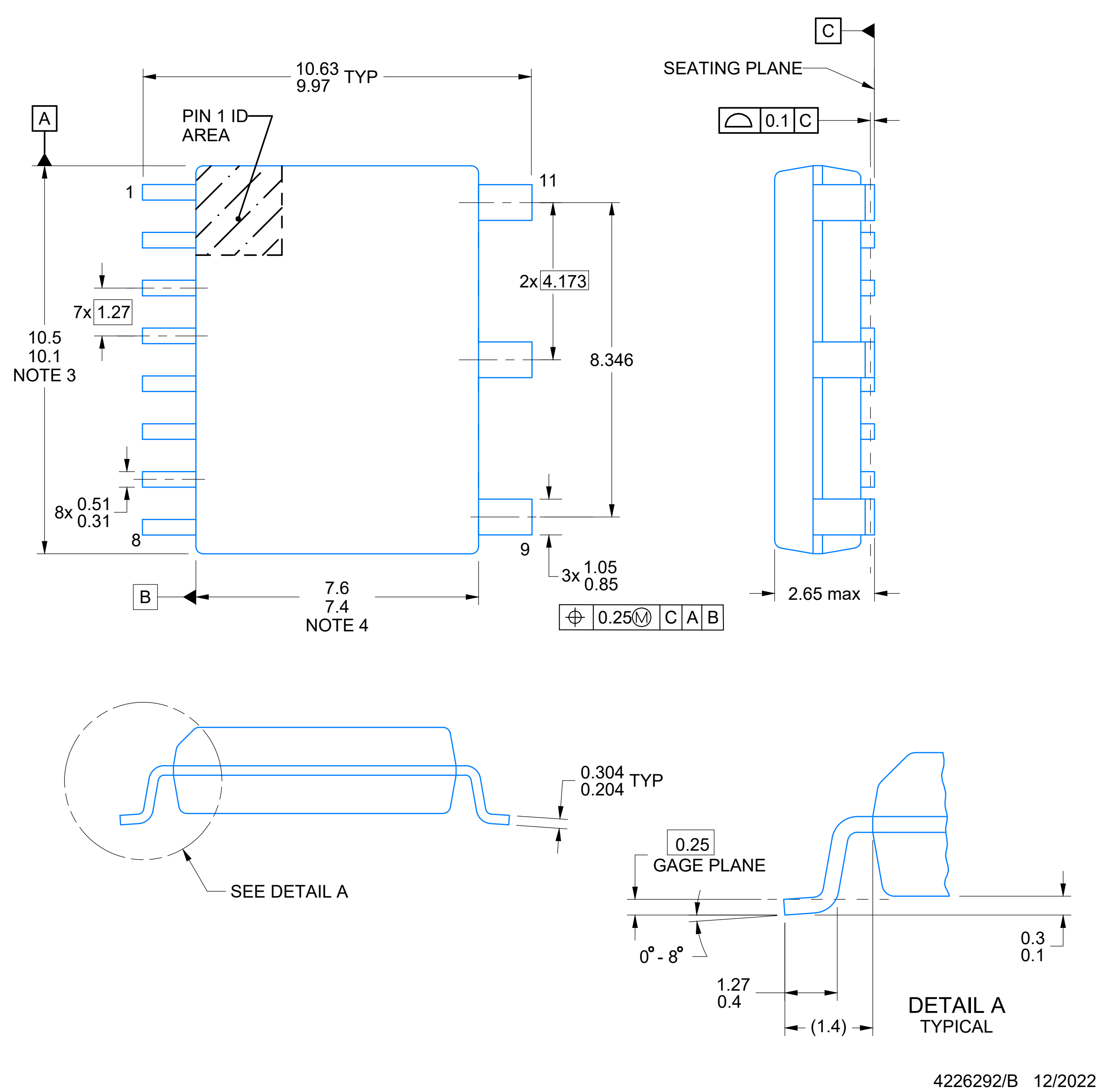

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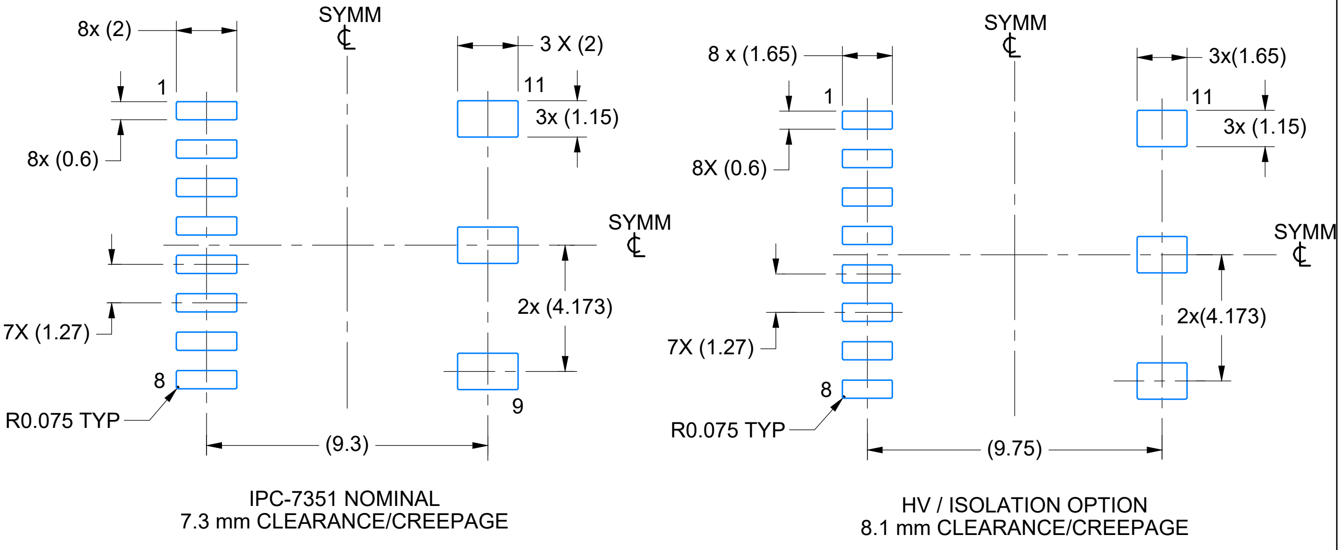
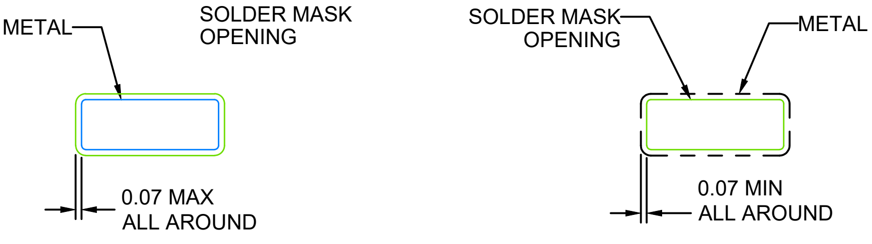


IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK
DEFINED

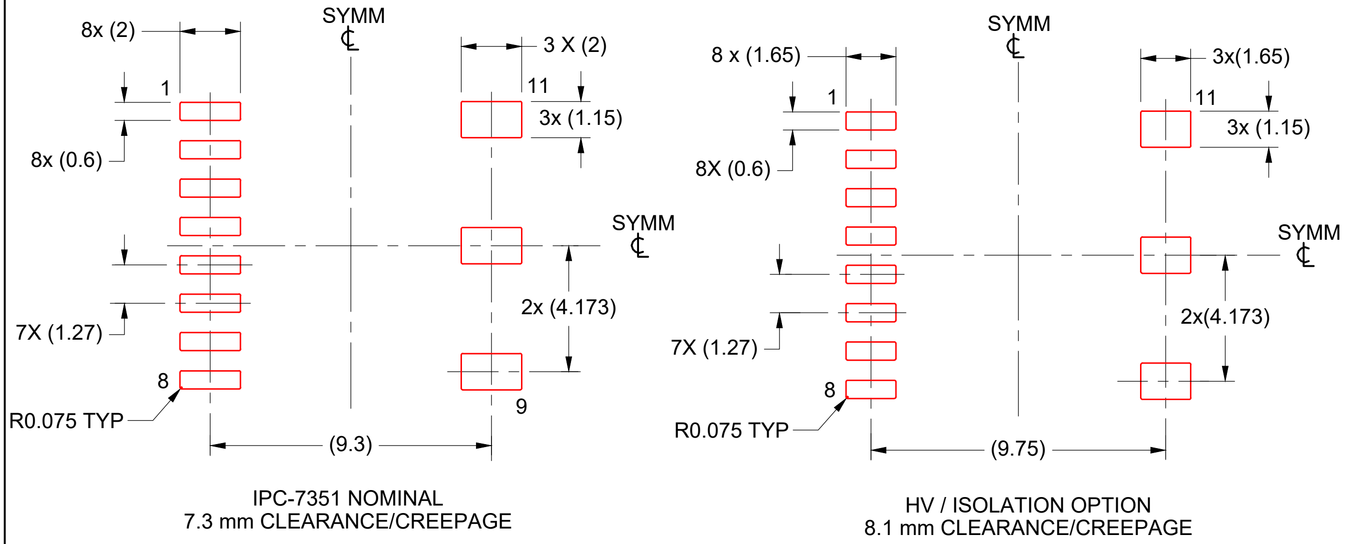
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226292/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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