

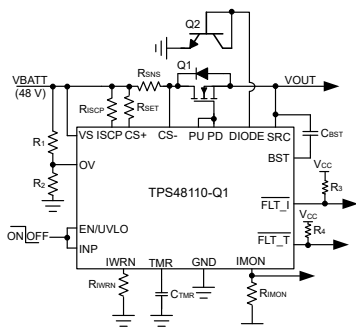
# TPS4811-Q1 100V 車載用スマート ハイサイド ドライバ、保護および診断機能付き

## 1 特長

- 下記結果で AEC-Q100 認定済み
  - デバイス温度グレード 1:
    - 動作時周囲温度範囲 -40°C~+125°C
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 3.5V~80V の入力範囲 (絶対最大定格 100V)
- 最小 -30V までの出力逆極性保護
- 100μA の電流能力を持つ内蔵 12V チャージポンプ
- 低シャットダウン電流 (EN/UVLO = Low): 1.6μA
- 強力なプルアップ (3.7A) / プルダウン (4A) ゲートドライバ
- 外付けバックツューバック N チャンネル MOSFET を駆動
- 容量性負荷を駆動するためのプリチャージスイッチドライバを内蔵したバリエーション (TPS48111-Q1)
- 調整可能なサーキットブレーカ タイマ (TMR) とフォルトフラグ出力 (FLT\_I) を備えた 2 レベルの調整可能な過電流保護 (IWRN, ISCP)
- 高速な短絡保護: 1.2μs (TPS48111-Q1)、4μs (TPS48110-Q1)
- 高精度アナログ電流モニタ出力 (IMON): ±2% (30mV V<sub>SNS</sub>)
- 調整可能な低電圧誤動作防止 (UVLO) および過電圧保護 (OV) < ±2%
- フォルトフラグ出力 (FLT\_T) を備えたリモート過熱検出 (DIODE) および保護

## 2 アプリケーション

- パワー・ディストリビューション・ボックス
- ボディ・コントロール・モジュール
- DC/DC コンバータ
- バッテリ・マネージメント・システム



ヒーター負荷用スマート ハイサイド ドライバ

## 3 概要

TPS4811x-Q1 ファミリーは、保護および診断機能を備えた 100V スマート ハイサイドドライバです。本デバイスは、動作電圧範囲が 3.5V~80V と広いため、12V、24V、48V のシステム設計に適しています。

本デバイスは、大電流システム設計において並列 FET を使って電力をスイッチングできる強力な 3.7A ピークソース (PU) と 4A ピークシンク (PD) ゲートドライバを備えています。ゲートドライバの制御入力として INP を使います。

本デバイスは、エネルギー管理システムの設計を可能にする高精度電流検出 (±2%) 出力 (IMON) を備えています。本デバイスは、スレッシュホールドと応答時間を精密に調整できる FLT\_I 出力を備えた 2 レベルの過電流保護機能を備えています。自動リトライおよびラッチオフ フォルト動作は設定可能です。本デバイスは、FLT\_T 出力を備えたりモート過熱保護機能を備えています。

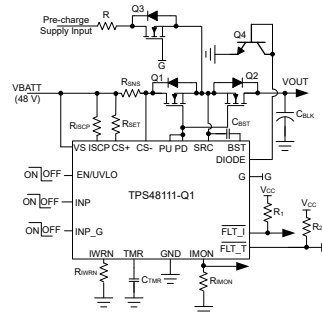
TPS48111-Q1 は、制御入力 (INP\_G) を備えたプリチャージドライバ (G) を内蔵しています。この機能は、大きな容量性負荷を駆動する必要がある設計を可能にします。シャットダウン モードでは、本コントローラは合計 1.6μA のシャットダウン電流を消費します (48V 電源入力の場合)。

TPS4811x-Q1 は、隣接する高電圧ピンと低電圧ピンの間のピンを取り除くことで 0.8mm の間隔を確保した 19 ピン VSSOP パッケージで供給されます。

### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS48110-Q1, TPS48111-Q1	DGX (VSSOP, 19)	5.10mm × 3.00mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



DC/DC コンバータ用サーキット ブレーカ



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>26</b>
<b>2 アプリケーション</b> .....	<b>1</b>	9.1 Application Information.....	26
<b>3 概要</b> .....	<b>1</b>	9.2 Typical Application: Driving HVAC PTC Heater Load on KL40 Line in Power Distribution Unit.....	26
<b>4 Device Comparison Table</b> .....	<b>3</b>	9.3 Typical Application: Driving B2B FETs With Pre- charging the Output Capacitance.....	33
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	9.4 Power Supply Recommendations.....	35
<b>6 Specifications</b> .....	<b>5</b>	9.5 Layout.....	36
6.1 Absolute Maximum Ratings.....	5	<b>10 Device and Documentation Support</b> .....	<b>38</b>
6.2 ESD Ratings.....	5	10.1 ドキュメントの更新通知を受け取る方法.....	38
6.3 Recommended Operating Conditions.....	5	10.2 サポート・リソース.....	38
6.4 Thermal Information.....	6	10.3 Trademarks.....	38
6.5 Electrical Characteristics.....	6	10.4 静電気放電に関する注意事項.....	38
6.6 Switching Characteristics.....	8	10.5 用語集.....	38
6.7 Typical Characteristics.....	9	<b>11 Revision History</b> .....	<b>38</b>
<b>7 Parameter Measurement Information</b> .....	<b>12</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>38</b>
<b>8 Detailed Description</b> .....	<b>14</b>		
8.1 Overview.....	14		
8.2 Functional Block Diagram.....	14		
8.3 Feature Description.....	15		

## 4 Device Comparison Table

	TPS48110-Q1	TPS48111-Q1
Overvoltage protection	Yes	No
Pre-charge driver	No	Yes
Short-circuit protection response time	4 $\mu$ s	1.2 $\mu$ s
Overtemperature fault response	Auto-retry with fixed 512-ms timer	Latch-off

## 5 Pin Configuration and Functions

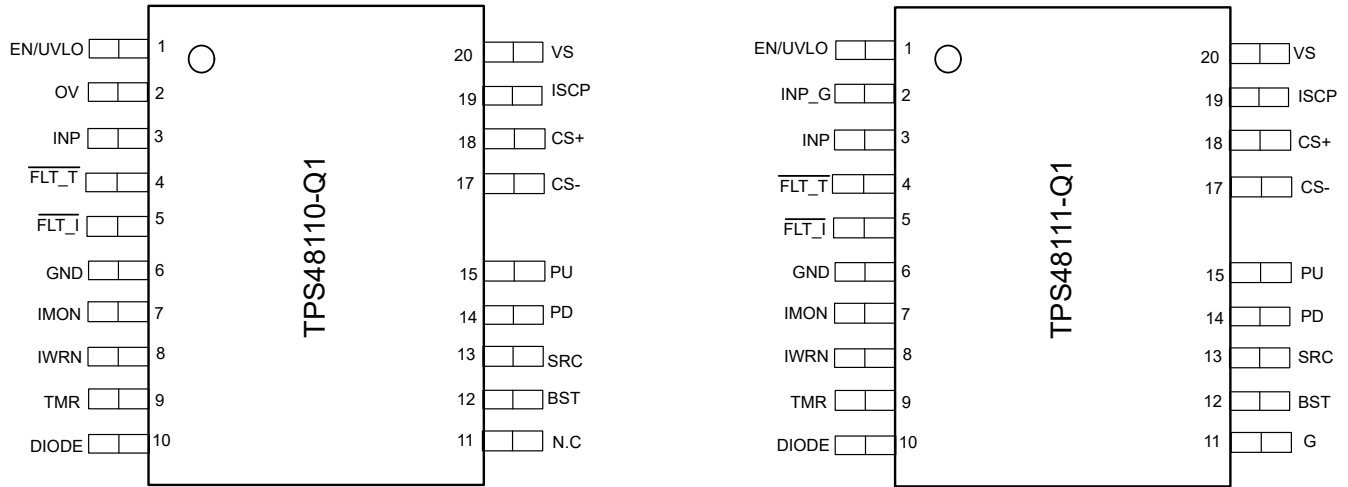


図 5-1. DGX Package, 19-Pin VSSOP (Top View)

表 5-1. Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	TPS48110-Q1	TPS48111-Q1		
	DGX-19 (VSSOP)			
EN/UVLO	1	1	I	EN/UVLO input. A voltage on this pin above 1 V enables normal operation. Forcing this pin below 0.3 V shuts down the TPS4811x-Q1, reducing quiescent current to approximately 1.6 $\mu$ A (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pull down of 60 nA pulls EN/UVLO low and keeps the device in OFF state.
OV	2	—	I	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply, OV to GND. When the voltage at OV exceeds the overvoltage cut-off threshold then the PD is pulled down to SRC turning OFF the external FET. When the voltage at OV goes below OV falling threshold then PU gets pulled up to BST, turning ON the external FET. OV must be connected to GND when not used. When OV is left floating an internal pull down of 60 nA pulls OV low and keeps PU pulled up to BST.
INP_G	—	2	I	Input Signal. CMOS compatible input reference to GND that sets the state of G pin. INP_G has an internal pull-down to GND to keep G pulled to SRC when INP_G is left floating. Connect INP_G to GND if the G drive functionality is unused.
INP	3	3	I	Input Signal. CMOS compatible input reference to GND that sets the state of PD and PU pins. INP has an internal pull-down to GND to keep PD pulled to SRC when INP is left floating.

表 5-1. Pin Functions (続き)

NAME	PIN		TYPE	DESCRIPTION
	TPS48110-Q1	TPS48111-Q1		
	DGX-19 (VSSOP)			
FLT_T	4	4	O	Open Drain Fault Output. This pin asserts low when overtemperature fault is detected.
FLT_I	5	5	O	Open Drain Fault Output. This pin asserts low after the voltage on the TMR pin has reached the fault threshold of 1.1 V. This pin indicates the pass transistor is about to turn off due to an overcurrent condition. The FLT_I pin does not go to a high-impedance state until the overcurrent condition and the auto-retry time expire.
GND	6	6	G	Connect GND to system ground.
IMON	7	7	O	Analog current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor $R_{SNS}$ . A resistor from this pin to GND converts current proportional to voltage. If unused, connect the pin to GND.
IWRN	8	8	I	Overcurrent detection setting. A resistor across IWRN to GND sets the over current comparator threshold. Connect IWRN to GND if overcurrent protection feature is not desired.
TMR	9	9	I	Fault Timer Input. A capacitor across TMR pin to GND sets the time for fault warning, fault turn-off (FLT_I) and retry periods. Leave it open for fastest setting. Connect TMR to GND to disable overcurrent protection.
DIODE	10	10	I	Diode connection for temperature sensing. Connect this pin to base and collector of an MMBT3904 NPN BJT. Connect DIODE to GND, if remote overtemperature protection feature is not desired.
G	—	11	O	GATE of external pre-charge FET. Connect to the GATE of the external FET. Leave the G pin floating if the G drive functionality is unused.
N.C	11	—	—	No connect.
BST	12	12	O	High Side Bootstrapped Supply. An external capacitor with a minimum value of $> Q_{g(tot)}$ of the external FET must be connected between this pin and SRC.
SRC	13	13	O	Source connection of the external FET.
PD	14	14	O	High Current Gate Driver Pull-Down. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
PU	15	15	O	High Current Gate Driver Pull-Up. This pin pulls up to BST. Connect this pin to PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on.
CS-	17	17	I	Current sense negative input.
CS+	18	18	I	Current sense positive input. Connect a 50 - 100- $\Omega$ resistor across CS+ to the external current sense resistor.
ISCP	19	19	I	Short-circuit detection threshold setting. Connect ISCP to CS- if short-circuit protection is not desired.
VS	20	20	Power	Supply pin of the controller.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input Pins	VS, CS+, CS–, ISCP to GND	–1	100	V
	VS, CS+, CS– to SRC	–60	100	
	SRC to GND	–30	100	
	PU, PD, G, BST to SRC	–0.3	16	
	TMR, IWRN, DIODE to GND	–0.3	5.5	
	OV, EN/UVLO, INP, INP_G, FLT_I, FLT_T to GND	–1	20	
	CS+ to CS–	–0.3	0.3	
	I <sub>(FLT_I)</sub> , I <sub>(FLT_T)</sub>		10	mA
I <sub>(CS+)</sub> to I <sub>(CS–)</sub> , 1msec	–100	100		
Output Pins	PU, PD, G, BST to GND	–30	112	V
	IMON to GND	–1	7.5	
Operating junction temperature, T <sub>j</sub> <sup>(2)</sup>		–40	150	°C
Storage temperature, T <sub>stg</sub>		–40	150	

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V	
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, DIODE, G, VS)		±750
			Other pins		±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Input Pins	VS, CS+, CS– to GND	0		80	V
	EN/UVLO, OV to GND	0		15	
Output Pins	FLT_I, FLT_T to GND	0		15	
	IMON to GND	0		5	
External Capacitor	VS to GND	22			nF
	BST to SRC	0.1			μF
T <sub>j</sub>	Operating Junction temperature <sup>(2)</sup>	–40		150	°C

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS4811x-Q1	
		DGX	UNIT
		19 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	43.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

$T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; typical values at  $T_J = 25^\circ\text{C}$ ,  $V_{(VS)} = V_{(CS+)} = V_{(CS-)} = 48\text{ V}$ ,  $V_{(BST-SRC)} = 12\text{ V}$ ,  $V_{(SRC)} = 0\text{ V}$ ,  $V_{SNS} =$  Voltage across  $R_{SNS}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE</b>						
$V_{(VS)}$	Operating input voltage		3.5		80	V
$V_{(VS\_PORR)}$	VS POR threshold, rising		2.75	3	3.2	V
$V_{(VS\_PORF)}$	VS POR threshold, falling		2.65	2.9	3.1	V
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)} = 2\text{ V}$		613	700	$\mu\text{A}$
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)} = 0\text{ V}$ , $V_{(SRC)} = 0\text{ V}$		1.6	5.36	$\mu\text{A}$
		$V_{(EN/UVLO)} = 0\text{ V}$ , $V_{(SRC)} = 0\text{ V}$ , $-40^\circ\text{C} < T_J < 85^\circ\text{C}$		1.6	2.65	$\mu\text{A}$
<b>ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT</b>						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.16	1.18	1.2	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.1	1.11	1.13	V
$V_{(ENF)}$	Enable threshold voltage for low IQ shutdown, falling		0.3	0.7	0.9	V
	Enable Hysteresis			43	60	mV
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)} = 12\text{ V}$		61	320	nA
<b>OVER VOLTAGE PROTECTION (OV) INPUT - TPS48110-Q1 Only</b>						
$V_{(OVR)}$	Overvoltage threshold input, rising	TPS48110-Q1 Only	1.16	1.18	1.2	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.1	1.11	1.13	V
$I_{(OV)}$	OV Input leakage current	$0\text{ V} < V_{(OV)} < 5\text{ V}$		60	300	nA
<b>CHARGE PUMP (BST-SRC)</b>						
$I_{(BST)}$	Charge Pump Supply current	$V_{(BST-SRC)} = 10\text{ V}$	80	100	126	$\mu\text{A}$
$V_{(BST-SRC)}$	Charge Pump Turn ON voltage		11	11.7	12.3	V
	Charge Pump Turn OFF voltage		11.6	12.3	13	V
$V_{(BST\_UVLOR)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising		7	7.6	8.1	V
$V_{(BST\_UVLOF)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, falling		6	6.5	6.9	V
$V_{(BST-SRC)}$	Charge Pump Voltage at $V_{(VS)} = 3.5\text{ V}$		8.6			V
<b>GATE DRIVER OUTPUTS (PU, PD, G)</b>						
$R_{(PD)}$	Pull-Down Resistance			0.69	1.34	$\Omega$
$I_{(PU)}$	Peak Source Current			3.75		A
$I_{(PD)}$	Peak Sink Current			4		A

## 6.5 Electrical Characteristics (続き)

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(VS)} = V_{(CS+)} = V_{(CS-)} = 48\text{ V}$ ,  $V_{(BST-SRC)} = 12\text{ V}$ ,  $V_{(SRC)} = 0\text{ V}$ ,  $V_{SNS} =$  Voltage across  $R_{SNS}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(G)}$	Gate charge (sourcing) current, on state	TPS48111-Q1 Only	72	100	140	$\mu\text{A}$
	Gate discharge (sinking) current, off state		92	131	190	$\text{mA}$
<b>CURRENT SENSE AND OVER CURRENT PROTECTION (CS+, CS-, IMON, ISCP, IWRN)</b>						
$V_{(OS\_SET)}$	Input referred offset ( $V_{SNS}$ to $V_{(IMON)}$ scaling)	$R_{SET} = 100\ \Omega$ , $R_{IMON} = 5\ \text{k}\Omega$ , $10\ \text{k}\Omega$ (corresponds to $V_{SNS} = 6\ \text{mV}$ to $30\ \text{mV}$ ) Gain of 45 and 90 respectively.	-200		200	$\mu\text{V}$
$V_{(GE\_SET)}$	Gain error ( $V_{SNS}$ to $V_{(IMON)}$ scaling)		-1.27		1.27	%
$V_{(IMON\_Acc)}$	IMON accuracy	$V_{SNS} = 30\ \text{mV}$ , $R_{SET} = 100\ \Omega$ , $R_{IMON} = 10\ \text{k}\Omega$	-2		2	%
		$V_{SNS} = 6\ \text{mV}$ , $R_{SET} = 100\ \Omega$ , $R_{IMON} = 5\ \text{k}\Omega$	-5		5	%
$V_{(SNS\_WRN)}$	Overcurrent protection (OCP) voltage threshold	$R_{SET} = 100\ \Omega$ , $R_{IWRN} = 39.7\ \text{k}\Omega$	29.2	30.6	31.5	$\text{mV}$
		$R_{SET} = 100\ \Omega$ , $R_{IWRN} = 120\ \text{k}\Omega$	8	10	12	$\text{mV}$
$I_{(ISCP)}$	SCP Input Bias current		13.7	15.6	17.6	$\mu\text{A}$
$V_{(SNS\_SCP)}$	Short-circuit protection (SCP) voltage threshold	$R_{ISCP} = 2.1\ \text{k}\Omega$	35	40	45	$\text{mV}$
		$R_{ISCP} = 750\ \Omega$		19		$\text{mV}$
<b>DELAY TIMER (TMR)</b>						
$I_{(TMR\_SRC\_CB)}$	TMR source current		73	82	91	$\mu\text{A}$
$I_{(TMR\_SRC\_FLT)}$	TMR source current		2.1	2.5	3.3	$\mu\text{A}$
$I_{(TMR\_SNK)}$	TMR sink current		2.1	2.5	3	$\mu\text{A}$
$V_{(TMR\_OC)}$	TMR voltage threshold for over current shutdown		1.112	1.2	1.3	$\text{V}$
$V_{(TMR\_FLT)}$	TMR voltage threshold for FLT_T assertion		1.03	1.1	1.2	$\text{V}$
$V_{(TMR\_LOW)}$	Voltage at TMR pin for AR counter falling threshold		0.15	0.2	0.22	$\text{V}$
<b>INPUT CONTROLS (INP, INP_G), FAULT FLAGS (FLT_I, FLT_T)</b>						
$R_{(FLT\_I)}$	FLT_I Pull-down resistance		54	70	90	$\Omega$
$R_{(FLT\_T)}$	FLT_T Pull-down resistance			70		$\Omega$
$I_{(FLT\_T)}$	FLT Input leakage current				400	$\text{nA}$
$V_{(INP\_H)}$				1.6	2	$\text{V}$
$V_{(INP\_L)}$			0.8	1.2		$\text{V}$
$V_{(INP\_Hys)}$				400		$\text{mV}$
$V_{(INP\_G\_H)}$				1.6	2	$\text{V}$
$V_{(INP\_G\_L)}$		TPS48111-Q1 Only	0.8	1.2		$\text{V}$
$V_{(INP\_G\_Hys)}$				400		$\text{mV}$
<b>TEMPERATURE SENSING AND PROTECTION (DIODE)</b>						
$I_{(DIODE)}$	External diode current source	High level		160		$\mu\text{A}$
		Low level		10		$\mu\text{A}$
	Diode current ratio		15.4	16	16.6	A/A
$T_{(DIODE\_TSD\_rising)}$	DIODE sense TSD rising threshold	With MMBT3904 BJT for sensing	140	150	160	$^{\circ}\text{C}$

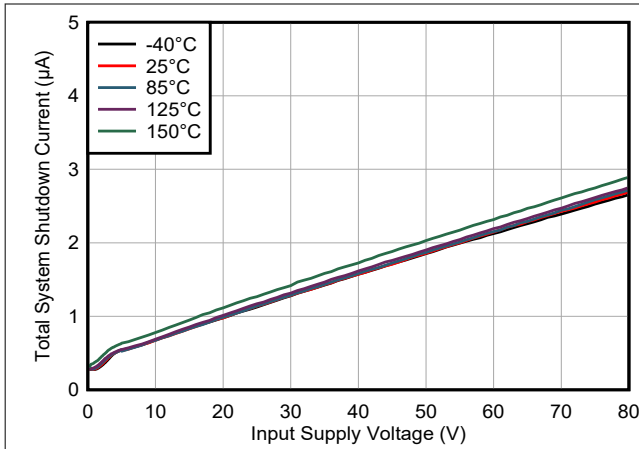
## 6.6 Switching Characteristics

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(VS)} = V_{(CS+)} = V_{(CS-)} = 48\text{ V}$ ,  $V_{(BST-SRC)} = 12\text{ V}$ ,  $V_{(SRC)} = 0\text{ V}$ ,  $V_{SNS} =$  Voltage across  $R_{SNS}$

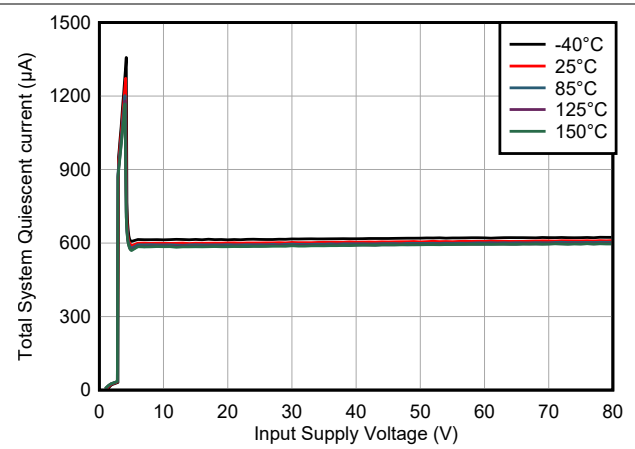
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PU(INP\_H)}$	INP Turn ON propagation Delay	INP $\uparrow$ to PU $\uparrow$ , $C_L = 47\text{ nF}$		1	2	$\mu\text{s}$
$t_{PD(INP\_L)}$	INP Turn OFF propagation Delay	INP $\downarrow$ to PD $\downarrow$ , $C_L = 47\text{ nF}$			1	$\mu\text{s}$
$t_{G(INP\_G\_H)}$	INP_G Turn ON propagation Delay	INP_G $\uparrow$ to G $\uparrow$ , $C_L = 1\text{ nF}$		21		$\mu\text{s}$
$t_{G(INP\_G\_L)}$	INP_G Turn OFF propagation Delay	INP_G $\downarrow$ to G $\downarrow$ , $C_L = 1\text{ nF}$		0.55	0.8	$\mu\text{s}$
$t_{PD(EN\_OFF)}$	EN Turn OFF Propagation Delay	EN $\downarrow$ to PD $\downarrow$ , $C_L = 47\text{ nF}$		3.2	5	$\mu\text{s}$
$t_{PD(UVLO\_OFF)}$	UVLO Turn OFF Propagation Delay	UVLO $\downarrow$ to PD $\downarrow$ , $C_L = 47\text{ nF}$		3.5	6	$\mu\text{s}$
$t_{PD(VS\_OFF)}$	PD Turn OFF delay during input supply (VS) interruption	VS $\downarrow$ $V_{(VS\_PORF)}$ to PD $\downarrow$ , $C_L = 47\text{ nF}$ , INP = EN/UVLO = 2 V		54		$\mu\text{s}$
$t_{PU(VS\_ON)}$	PU Turn ON delay during input supply (VS) recovery	VS $\uparrow$ $V_{(VS\_PORR)}$ to PU $\uparrow$ , $C_L = 47\text{ nF}$ , INP = EN/UVLO = 2 V, $V_{(BST-SRC)} > V_{(BST\_UVLOR)}$		328	465	$\mu\text{s}$
$t_{PD(OV\_OFF)}$	OV Turn Off propagation Delay	OV $\uparrow$ to PD $\downarrow$ , $C_L = 47\text{ nF}$		2.6	4	$\mu\text{s}$
$t_{sc}$	Short-circuit protection propagation Delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_SCP)}$ to PD $\downarrow$ , $C_L = 47\text{ nF}$ , TPS48111-Q1 Only		1.16	1.6	$\mu\text{s}$
	Short-circuit protection propagation Delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_SCP)}$ to PD $\downarrow$ , $C_L = 47\text{ nF}$ , TPS48110-Q1 Only		4	5	$\mu\text{s}$
$t_{oc}$	Over current protection delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_WRN)}$ to PD $\downarrow$ , $C_L = 47\text{ nF}$ , $C_{TMR} = 0\text{ nF}$		25	30	$\mu\text{s}$
	Over current protection delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_WRN)}$ to PD $\downarrow$ , $C_L = 47\text{ nF}$ , $C_{TMR} = 22\text{ nF}$		370		$\mu\text{s}$
$t_{(FLT\_I\_ASSERT)}$	FLT_I assertion delay	$C_{TMR} = 22\text{ nF}$		340		$\mu\text{s}$
$t_{(FLT\_I\_DEASSERT)}$	FLT_I de-assertion delay			260		$\mu\text{s}$
$t_{(FLT\_T)AR}$	TSD Auto-retry	TPS48110-Q1 Only		512		msec



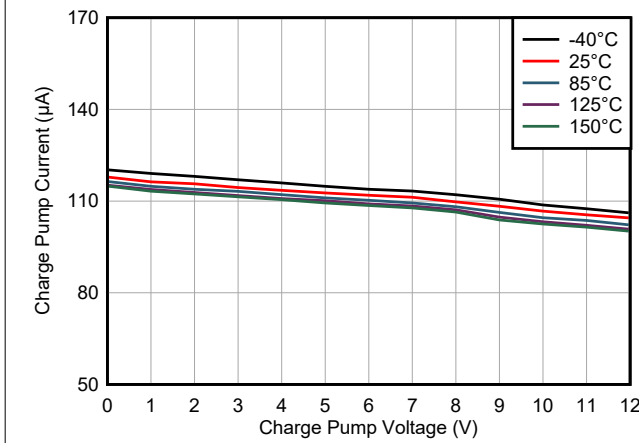
## 6.7 Typical Characteristics



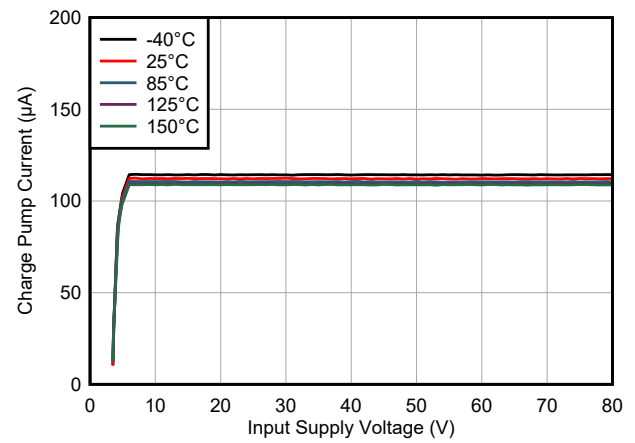
6-1. Shutdown Supply Current vs Supply Voltage



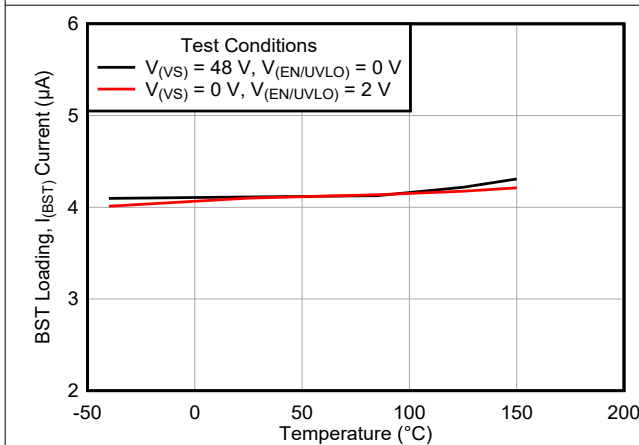
6-2. Operating Quiescent Current vs Supply Voltage



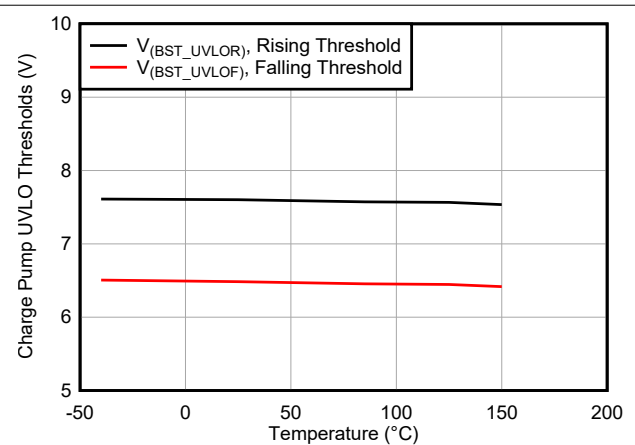
6-3. Charge Pump Current vs Charge Pump Voltage



6-4. Charge Pump Current vs Input Supply Voltage

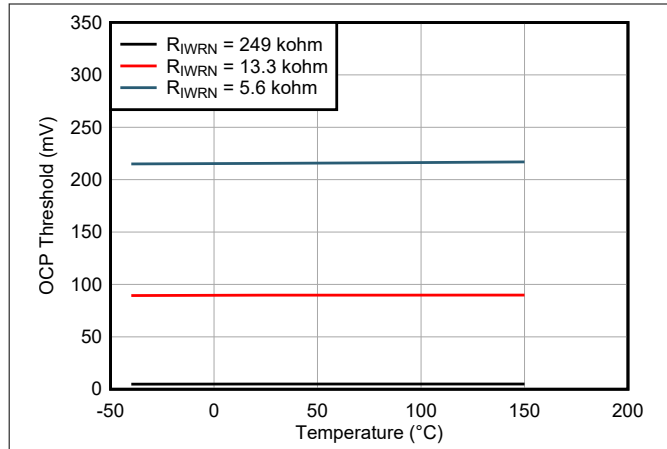


6-5. BST Loading Current ( $I_{BST}$ ) vs Temperature

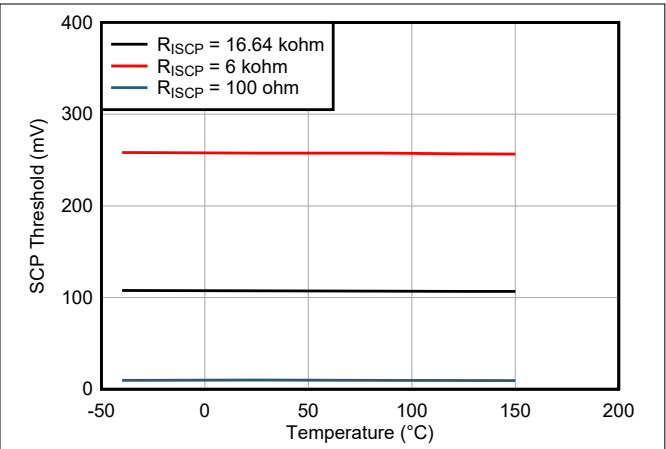


6-6. Charge Pump UVLO Thresholds vs Temperature

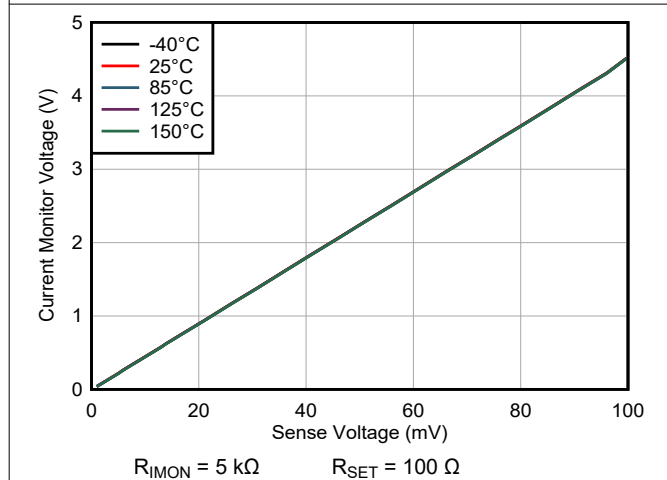
### 6.7 Typical Characteristics (continued)



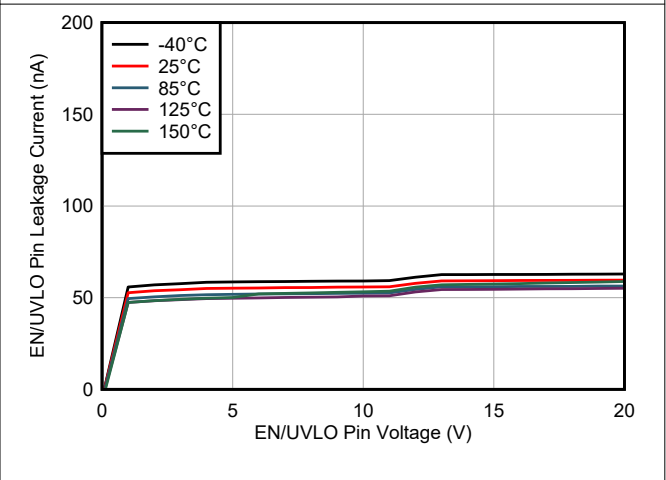
6-7. Overcurrent Threshold ( $V_{(SNS\_WRN)}$ ) vs Temperature



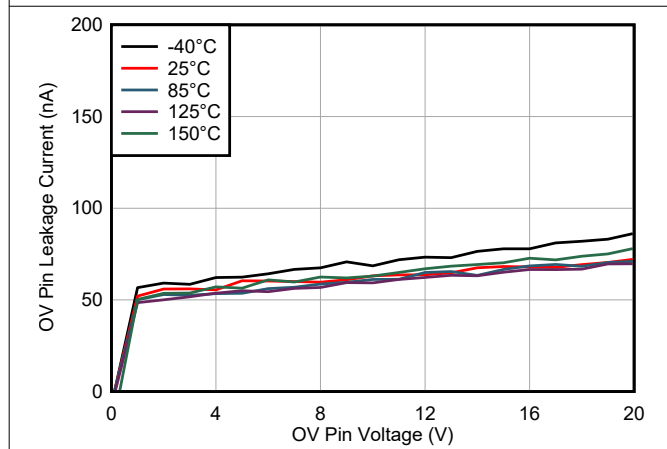
6-8. Short-Circuit Threshold ( $V_{(SNS\_SCP)}$ ) vs Temperature



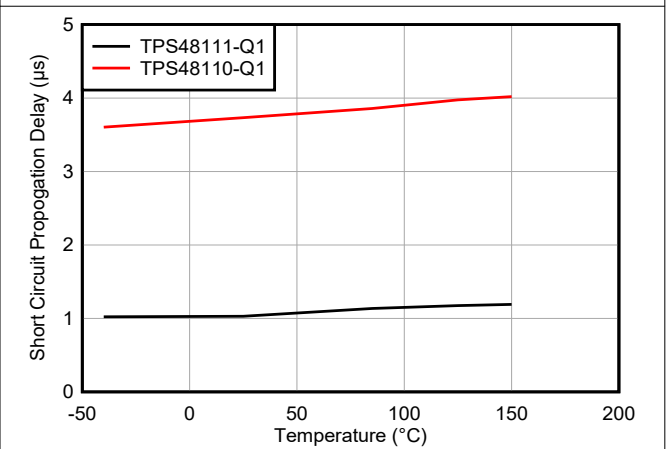
6-9. Current Monitor Output ( $V_{(IMON)}$ ) vs Sense Voltage ( $V_{(SNS)}$ )



6-10. EN/UVLO Pin Voltage vs Current

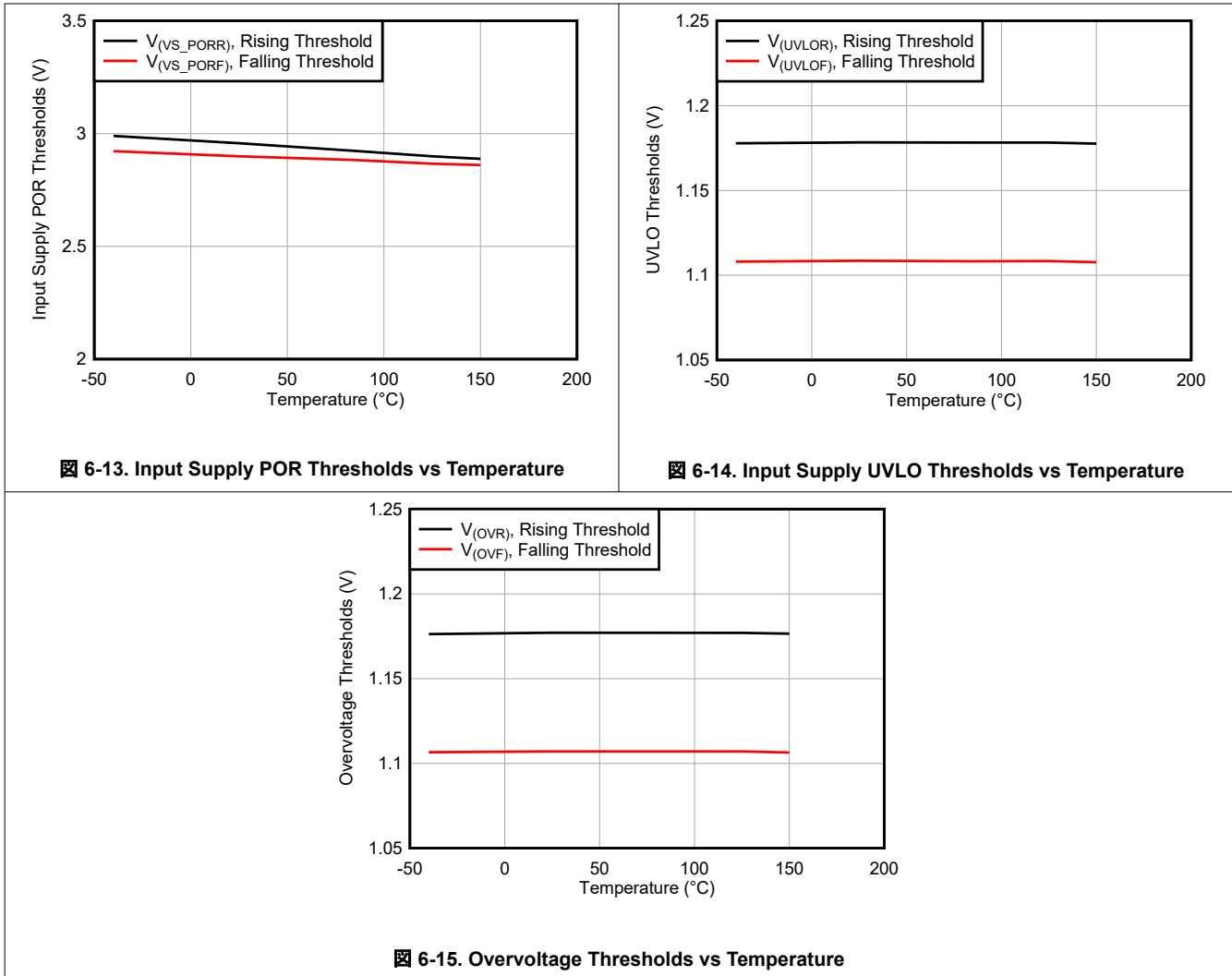


6-11. OV Pin Voltage vs Leakage Current

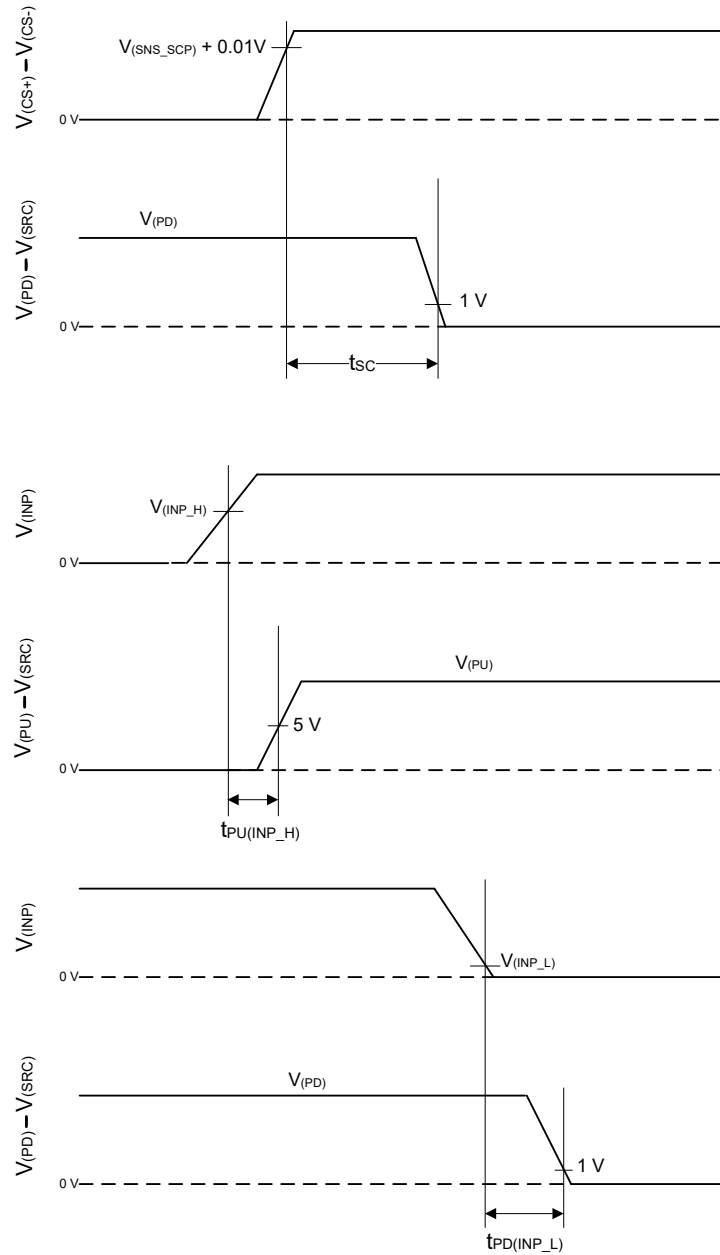


6-12. Short-Circuit Protection Response Time ( $t_{(SC)}$ ) vs Temperature

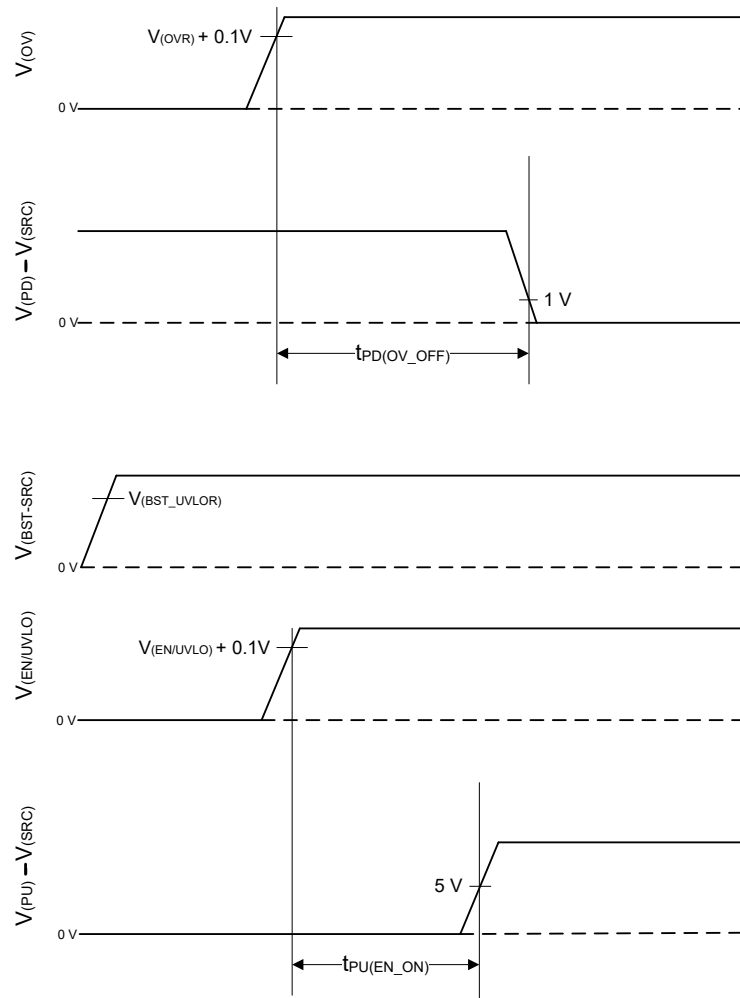
## 6.7 Typical Characteristics (continued)



## 7 Parameter Measurement Information



**7-1. Timing Waveforms**



**7-2. Timing Waveforms**

## 8 Detailed Description

### 8.1 Overview

The TPS4811x-Q1 family is a 100-V smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V – 80 V, the device is suitable for 12-V, 24-V, and 48-V system designs.

The device has a strong 3.7-A peak source (PU) and 4-A peak sink (PD) GATE driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input. MOSFET slew rate control (ON and OFF) is possible by placing external R-C components.

The device has accurate current sensing ( $\pm 2\%$  at 30-mV  $V_{SNS}$ ) output (IMON) enabling systems for energy management. The device has integrated two-level overcurrent protection with  $\overline{FLT\_I}$  output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured.

The device features remote overtemperature protection with  $\overline{FLT\_T}$  output enabling robust system protection.

TPS48110-Q1 has an accurate overvoltage protection ( $< \pm 2\%$ ), providing robust load protection.

The TPS48111-Q1 integrates a pre-charge driver (G) with control input (INP\_G). This feature enables system designs that need to drive large capacitive loads by pre-charging first and then turning ON the main power FETs.

TPS4811x-Q1 has an accurate undervoltage protection ( $< \pm 2\%$ ) using EN/UVLO pin. Pull EN/UVLO low ( $< 0.3$  V) to turn OFF the device and enter into shutdown state. In shutdown mode, the controller draws a total shutdown current of 1.6  $\mu$ A at 48-V supply input.

### 8.2 Functional Block Diagram

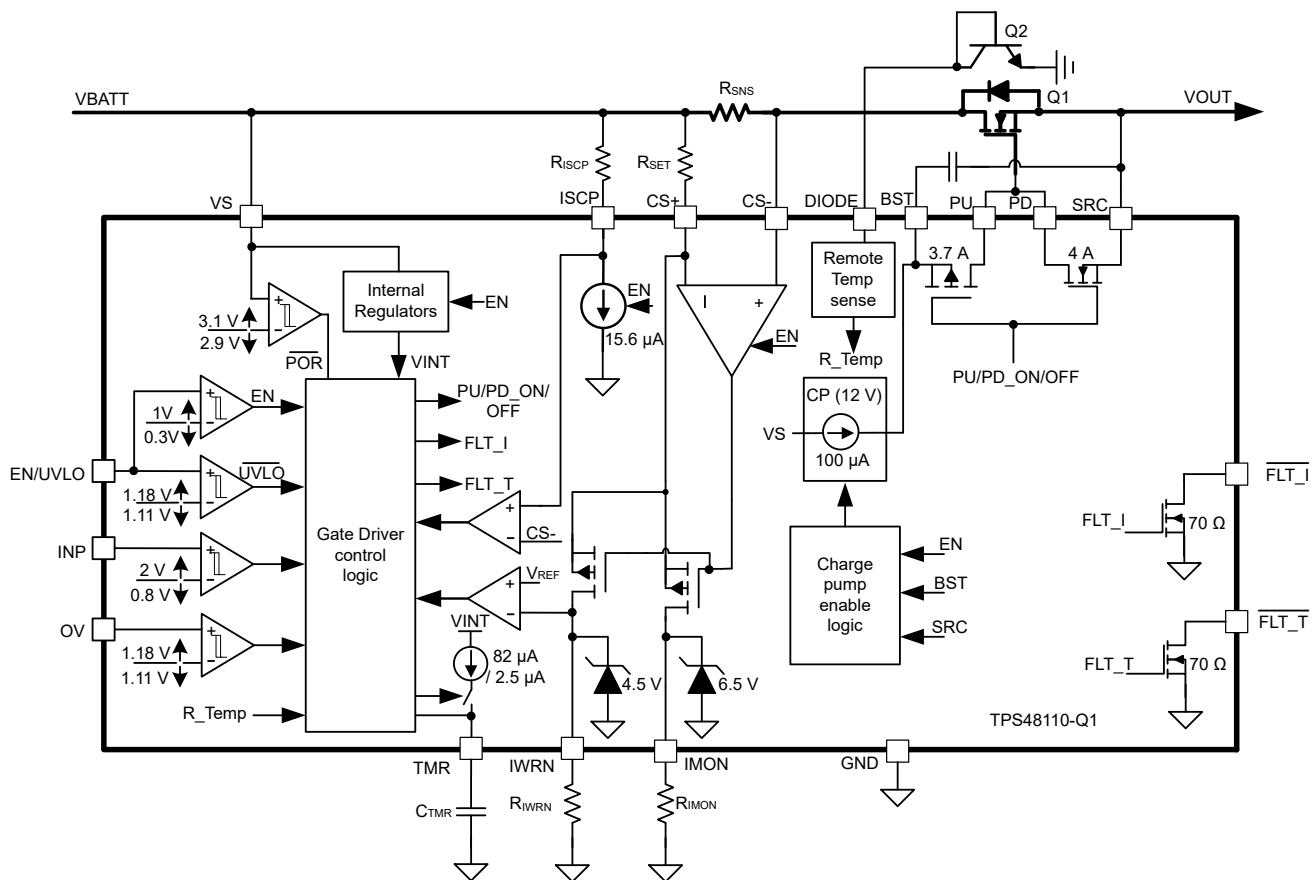


图 8-1. TPS48110-Q1 Functional Block Diagram

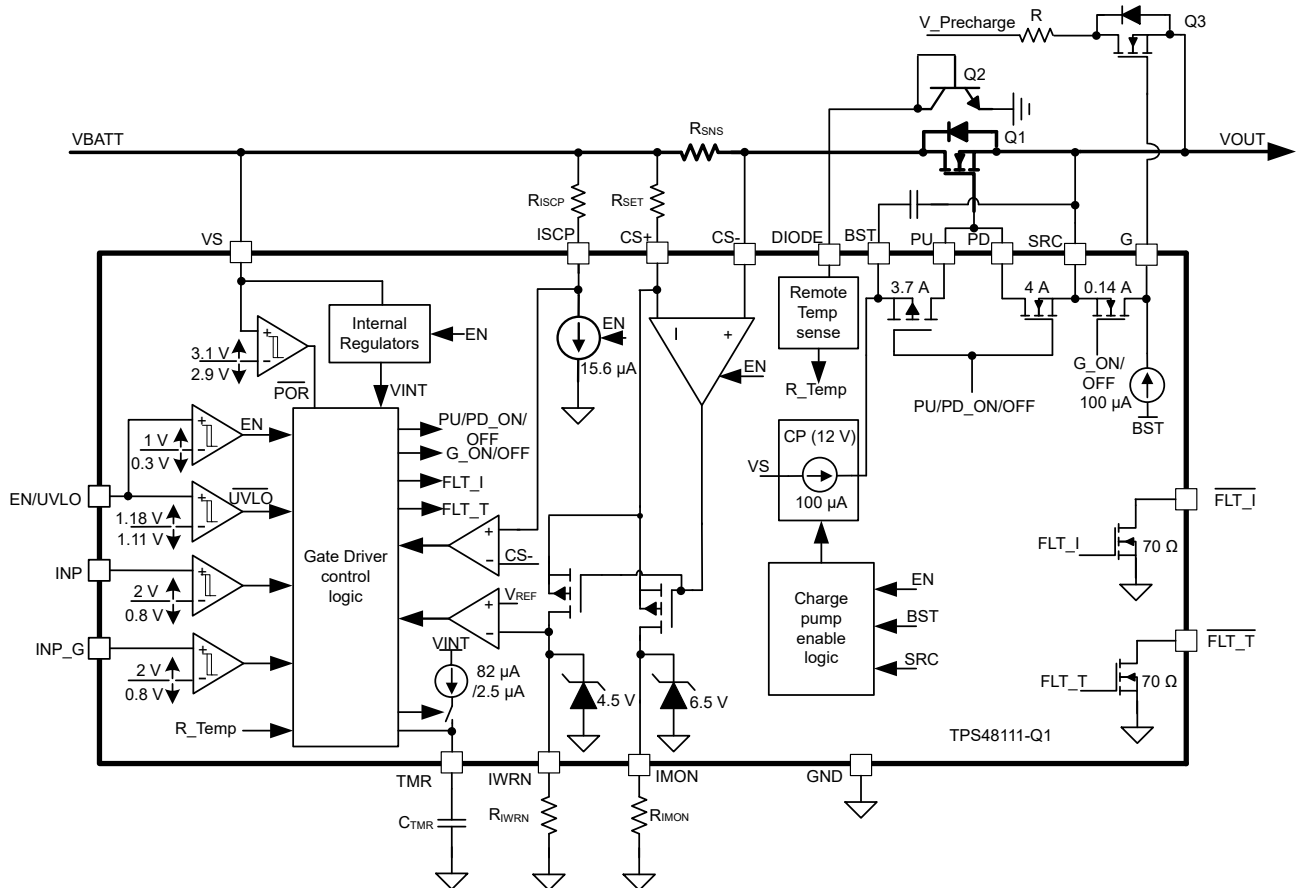


図 8-2. TPS48111-Q1 Functional Block Diagram

## 8.3 Feature Description

### 8.3.1 Charge Pump and Gate Driver output (VS, PU, PD, BST, SRC)

図 8-3 shows simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 3.7-A peak source and 4-A peak sink gate drivers. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 12-V, 100-μA charge pump is derived from VS terminal and charges the external boot-strap capacitor,  $C_{BST}$  that is placed across the GATE driver (BST and SRC).

In switching applications, if the charge pump supply demand is higher than 100 μA, then supply BST externally using a low leakage diode and  $V_{AUX}$  supply as shown in the 図 8-3.

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the  $C_{BST}$  capacitor. After the voltage across  $C_{BST}$  crosses  $V_{(BST\_UVLOR)}$ , the GATE driver section gets activated. The device has a 1-V (typical) UVLO hysteresis to ensure less performance during initial GATE turn ON. Choose  $C_{BST}$  based on the external FET's  $Q_G$  and allowed dip during FET turn ON. The charge pump remains enabled until the BST to SRC voltage reaches 12.3 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 11.7 V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 12.3 V and 11.7 V as shown in the 図 8-3.

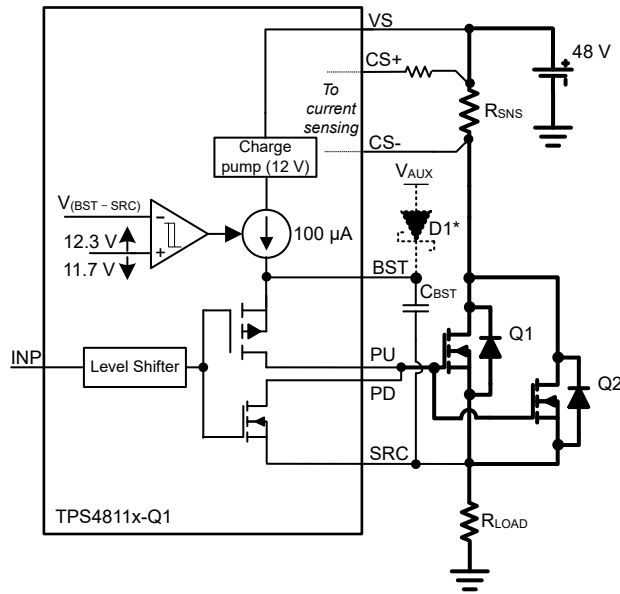


図 8-3. Gate Driver

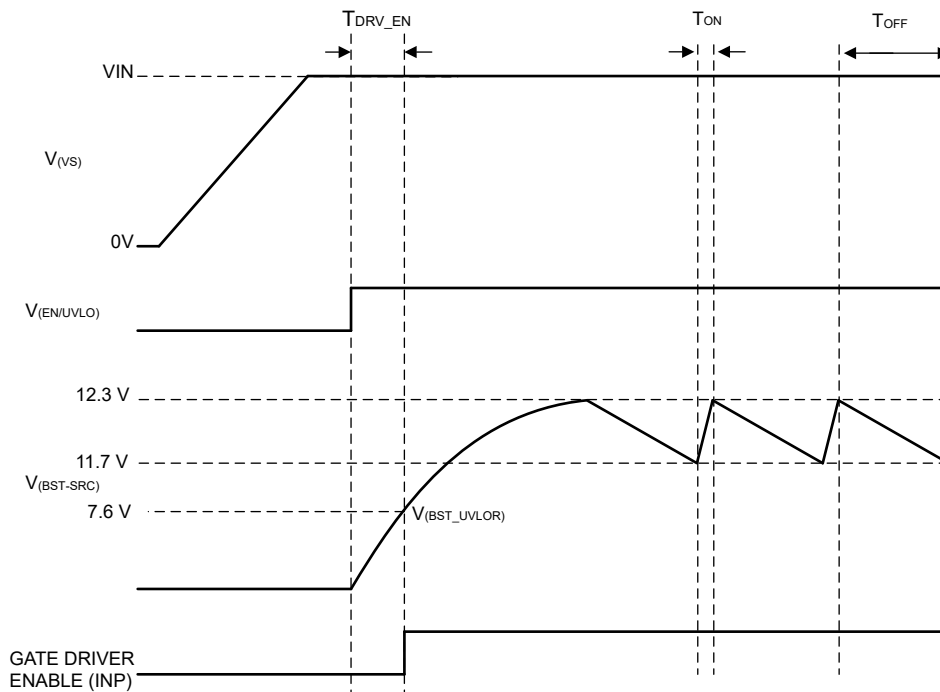


図 8-4. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay.

$$T_{\text{DRV\_EN}} = \frac{C_{\text{BST}} \times V_{(\text{BST\_UVLOR})}}{100 \mu\text{A}} \tag{1}$$

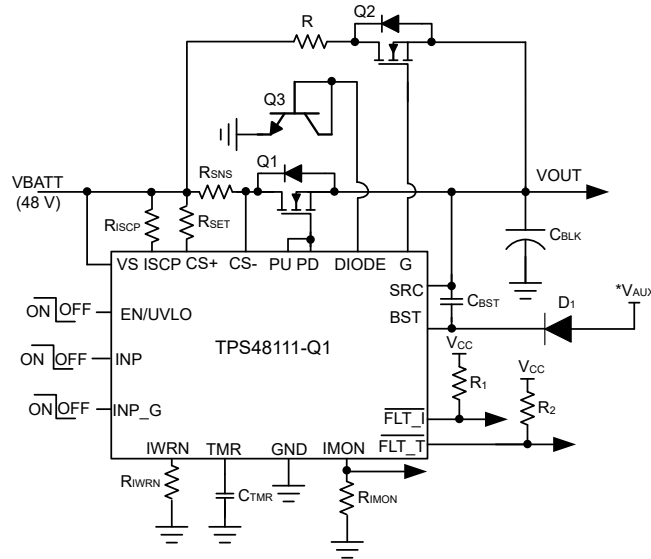
Where,

$C_{\text{BST}}$  is the charge pump capacitance connected across BST and SRC pins,



$V_{(BST\_UVLOR)} = 7.6 \text{ V}$  (typical).

If  $T_{DRV\_EN}$  needs to be reduced then pre-bias BST terminal externally using an external  $V_{AUX}$  supply through a low leakage diode D1 as shown in 8-3. With this connection,  $T_{DRV\_EN}$  reduces to 350  $\mu\text{s}$ . TPS4811x-Q1 application circuit with external supply to BST is shown in 8-5.



8-5. TPS4811-Q1 Application Circuit with external supply to BST

注

$V_{AUX}$  can be supplied by external supply ranging between 8.1 V and 15 V.

### 8.3.2 Capacitive Load Driving

Certain end equipments like automotive power distribution unit power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur potentially damaging the power FETs.

To limit the inrush current during capacitive load switching, the following system design techniques can be used with TPS4811x-Q1 devices.

#### 8.3.2.1 FET Gate Slew Rate Control

For limiting inrush current during turn ON of the FET with capacitive loads, use  $R_1$ ,  $R_2$ ,  $C_1$  as shown in 8-6. The  $R_1$  and  $C_1$  components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

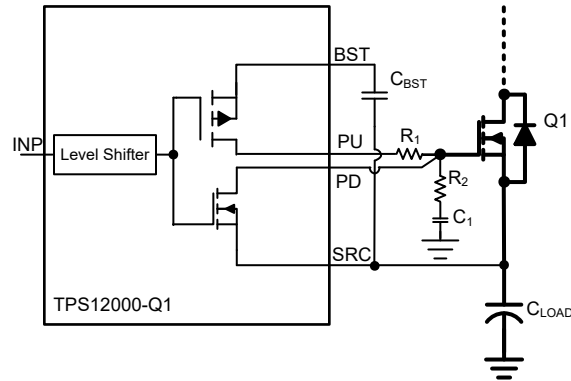


図 8-6. Inrush Current limiting

Use the 式 2 to calculate the inrush current during turn-ON of the FET.

$$I_{\text{INRUSH}} = C_{\text{LOAD}} \times \frac{V_{\text{BATT}}}{T_{\text{charge}}} \quad (2)$$

$$I_{\text{INRUSH}} = \frac{0.63 \times V_{(\text{BST-SRC})} \times C_{\text{LOAD}}}{R_1 \times C_1} \quad (3)$$

Where,

$C_{\text{LOAD}}$  is the load capacitance,  $V_{\text{BATT}}$  is the input voltage and  $T_{\text{charge}}$  is the charge time,  $V_{(\text{BST-SRC})}$  is the charge pump voltage (11 V),

Use a damping resistor  $R_2$  (~ 10  $\Omega$ ) in series with  $C_1$ . 式 3 can be used to compute required  $C_1$  value for a target inrush current. A 100 k $\Omega$  resistor for  $R_1$  can be a good starting point for calculations.

Connecting PD pin of TPS12000-Q1 directly to the gate of the external FET ensures fast turn OFF without any impact of  $R_1$  and  $C_1$  components.

$C_1$  results in an additional loading on  $C_{\text{BST}}$  to charge during turn ON. Use 式 4 to calculate the required  $C_{\text{BST}}$  value.

$$C_{\text{BST}} > Q_{\text{g}(\text{total})} + 10 \times C_1 \quad (4)$$

Where,  $Q_{\text{g}(\text{total})}$  is the total gate charge of the FET.

### 8.3.2.2 Using Precharge FET - (with TPS48111-Q1 Only)

In high-current applications where several FETs are connected in parallel, the gate slew rate control for the main FETs is not recommended due to unequal distribution of inrush currents among the FETs. This action makes FET selection complex and results in over sizing of the FETs.

The TPS48111-Q1 integrates precharge gate driver (G) with a dedicated control input (INP\_G). This feature can be used to drive a separate FET that can be used to precharge the capacitive load. 图 8-7 shows the precharge FET implementation for capacitive load charging using TPS48111-Q1. An external capacitor  $C_g$  reduces the gate turn-ON slew rate and controls the inrush current.

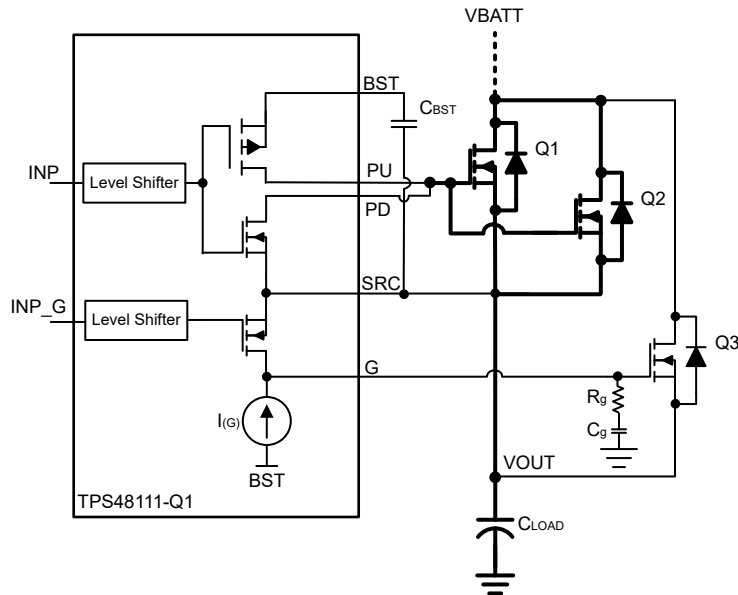


図 8-7. Capacitor Charging Using Gate Slew Rate Control of Precharge FET

During power up with EN/UVLO high and  $C_{BST}$  voltage above  $V_{(BST\_UVLOR)}$  threshold, INP and INP\_G controls are active. For the precharge functionality, drive INP low to keep the main FETs OFF and drive INP\_G high. G output gets pulled up to BST with  $I_G$ . Use 式 5 to calculate the required  $C_g$  value.

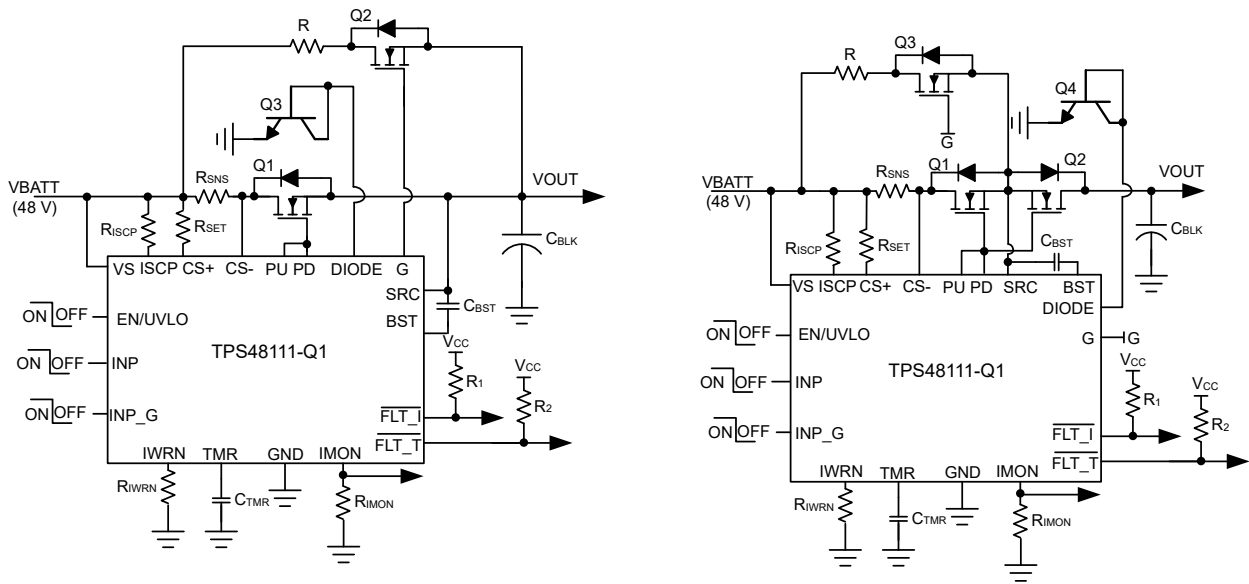
$$C_g = \frac{C_{LOAD} \times I_{(G)}}{I_{INRUSH}} \quad (5)$$

Where,

$I_{(G)}$  is 100  $\mu A$  (typical) and  $C_{LOAD}$  is total load capacitance.

Use 式 2 to calculate the  $I_{INRUSH}$ . A series resistor  $R_g$  must be used in conjunction with  $C_g$  to limit the discharge current from  $C_g$  during turn-off. The recommended value for  $R_g$  is between 220  $\Omega$  to 470  $\Omega$ . After the output capacitor is charged, turn OFF the precharge FET by driving INP\_G low. G gets pulled low to SRC with an internal 135-mA pulldown switch. The main FETs can be turned ON by driving INP high.

図 8-8 shows other system design approaches to charge large output capacitors in high current applications. The designs involve an additional power resistor in series in series with precharge FET. The back-to-back FET topology shown is typically used in bi-directional power control applications like battery management systems.



**8-8. TPS4811-Q1 application Circuits for Capacitive Load Driving Using Precharge FET and a Series Power Resistor**

**8.3.3 Short-Circuit Protection**

The TPS12000-Q1 feature adjustable short circuit protection. The threshold and the response time can be adjusted using ISCP resistor and TMR capacitor respectively. The device senses the voltage across the CS+ and CS– pins. These pins can be connected across an external current sense resistor or across the FET drain and source terminals for FET RDSON sensing. Set the circuit breaker detection threshold using an external resistor R<sub>ISCP</sub> across ISCP and GND. Use 式 6 to calculate the required R<sub>ISCP</sub> value.

$$R_{ISCP} (\Omega) = \frac{I_{SC} \times R_{SNS} - 10mV}{2 \mu} \tag{6}$$

Where, R<sub>SNS</sub> is the current sense resistor value or the FET RDSON value, I<sub>SC</sub> is the short circuit current level. The short circuit protection response is fastest < 6 μs with no C<sub>TMR</sub> cap connected across TMR and GND pins.

In the configurations of high side current sense with CS\_SEL connected to GND, during Q1 turn ON, first the FET’s VGS is sensed by monitoring the voltage across PD to SRC. Once VGS raises above G1\_GOOD threshold to ensure that the external FET gate is enhanced, then the SCP comparator output is monitored. If the sensed voltage across CS+ and CS– exceeds the ISCP set point, PD pulls low to SRC and FLT asserts low within 6μs (with TMR open). Subsequent events can be set either to be auto-retry or latch off as described in following sections

With CS\_SEL connected to >2V i.e low side current sense configurations, the device does not wait for the FETs to enhance (doesnot wait for G1\_GOOD threshold to reach) and directly looks at the SCP comparator output to pull PD to SRC in the case of a short circuit event.

**8.3.3.1 Overcurrent Protection With Auto-Retry**

The C<sub>TMR</sub> programs the over current protection delay (t<sub>OC</sub>) and auto-retry time (t<sub>RETRY</sub>). Once the voltage across CS+ and CS– exceeds the set point, the C<sub>TMR</sub> starts charging with 80-μA pull-up current. After the C<sub>TMR</sub> charges up to V<sub>(TMR\_FLT)</sub>, FLT asserts low providing warning on impending FET turn OFF. After C<sub>TMR</sub> charges to V<sub>(TMR\_OC)</sub>, PD pulls low to SRC turning OFF the FET. Post this event, the auto-retry behavior starts. The C<sub>TMR</sub>

capacitor starts discharging with 2.5- $\mu$ A pulldown current. After the voltage reaches  $V_{(TMR\_LOW)}$  level, the capacitor starts charging with 2.5- $\mu$ A pullup. After 32 charging-discharging cycles of  $C_{TMR}$  the FET turns ON back and FLT de-asserts

Use 式 7 to calculate the  $C_{TMR}$  capacitor to be connected across TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{OC}}{1.2} \quad (7)$$

Where,  $I_{TMR}$  is internal pull-up current of 80- $\mu$ A,  $t_{OC}$  is desired overcurrent response time.

The fastest  $t_{OC}$  is < 6  $\mu$ s with no  $C_{TMR}$  cap connected.

$$t_{RETRY} = 22.7 \times 10^6 \times C_{TMR}$$

If the overcurrent pulse duration is below  $t_{OC}$  then the FET remains ON and  $C_{TMR}$  gets discharged using internal pull down switch.

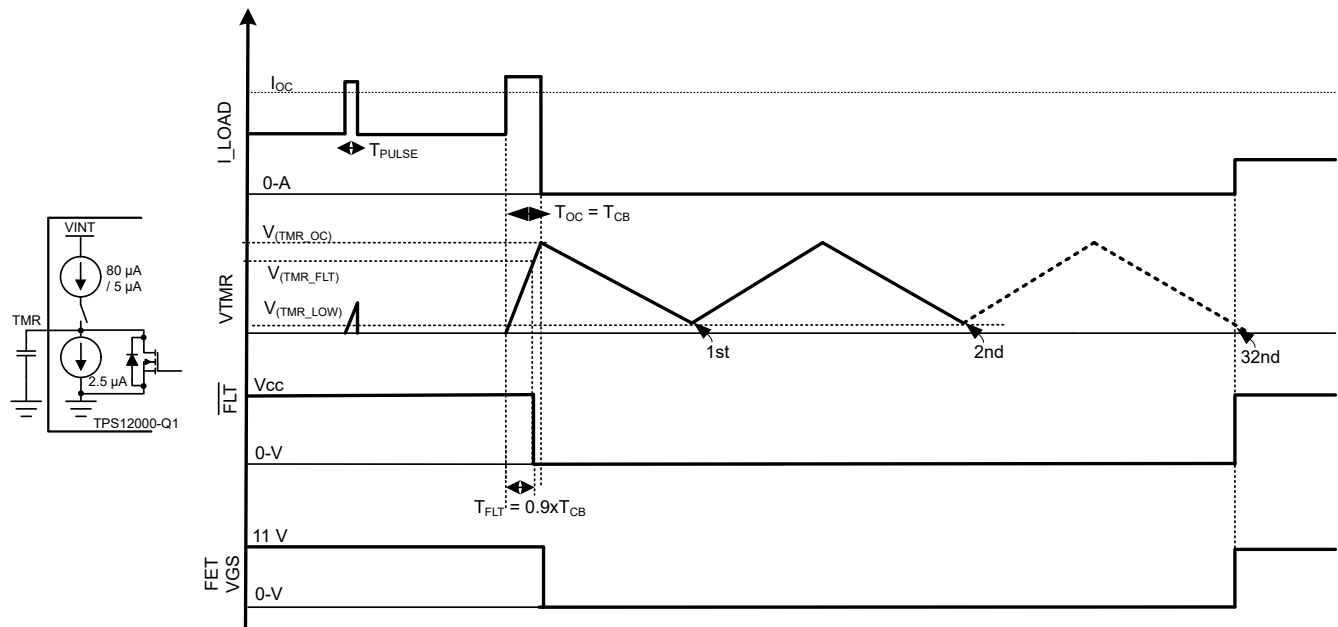


図 8-9. Overcurrent Protection With Auto-Retry

### 8.3.3.2 Overcurrent Protection With Latch-Off

Connect an approximately 100-k $\Omega$  resistor across  $C_{TMR}$  as shown in 図 8-10. With this resistor, during the charging cycle, the voltage across  $C_{TMR}$  gets clamped to a level below  $V_{(TMR\_OC)}$  resulting in a latch-off behavior.

Use 式 8 to calculate  $C_{TMR}$  capacitor to be connected between TMR and GND for  $R_{TMR} = 100$ -k $\Omega$ .

$$C_{TMR} = \frac{t_{OC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.2}{R_{TMR} \times I_{TMR}}}\right)} \quad (8)$$

Where,  $I_{TMR}$  is internal pull-up current of 80- $\mu$ A,  $t_{OC}$  is desired overcurrent response time.

Toggle INP or EN/UVLO (below  $V_{(ENF)}$ ) or power cycle VS below  $V_{(VS\_PORF)}$  to reset the latch. At low edge, the timer counter is reset and  $C_{TMR}$  is discharged. PU pulls up to BST when INP is pulled high.

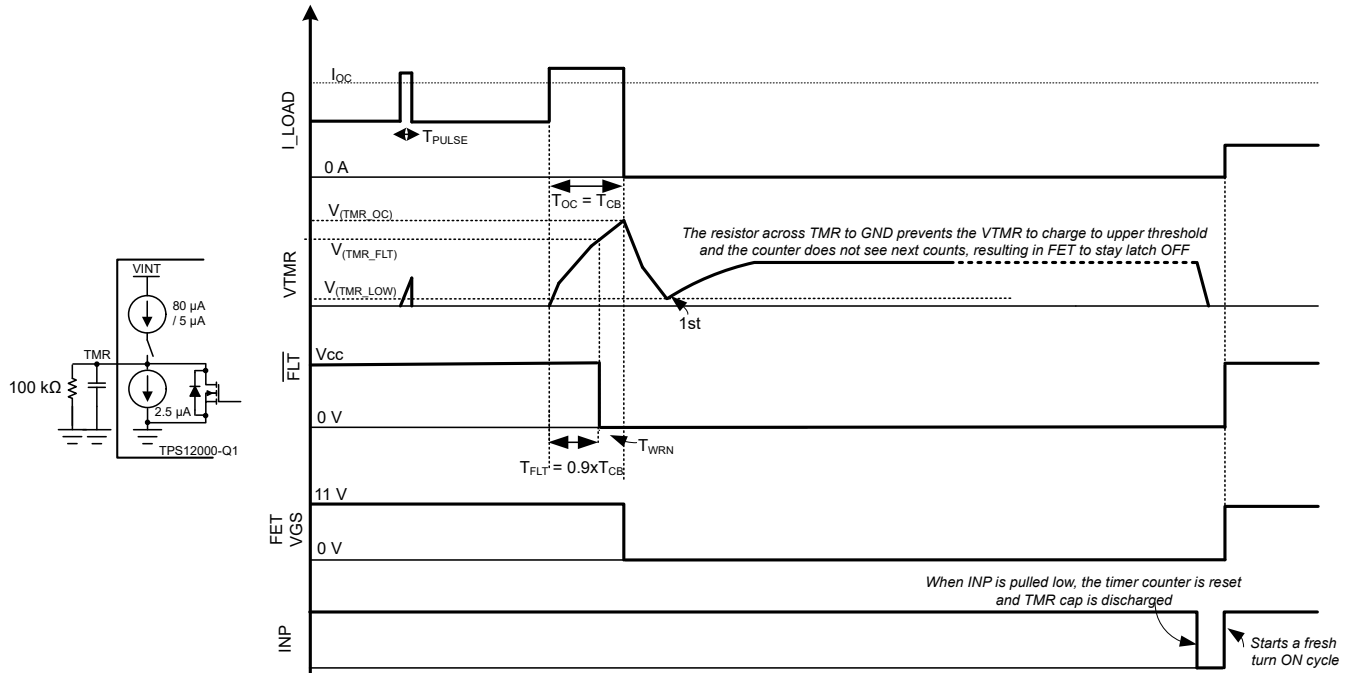


図 8-10. Overcurrent Protection With Latch-Off

### 8.3.4 Short-Circuit Protection

Connect a resistor,  $R_{ISCP}$  as shown in 図 8-11.

Use 式 9 to calculate the required  $R_{ISCP}$  value.

$$R_{ISCP} (\Omega) = \frac{I_{SC} \times R_{SNS}}{15.6 \mu} - 600 \tag{9}$$

Where,  $R_{SNS}$  is the current sense resistor, and  $I_{SC}$  is the desired short-circuit protection level. After the current exceeds the  $I_{SC}$  threshold then, PD pulls low to SRC within 1.2  $\mu$ s in TPS48111-Q1 and 4  $\mu$ s in TPS48110-Q1, protecting the FET.  $FLT_I$  asserts low at the same time. Subsequent to this event, the charge and discharge cycles of  $C_{TMR}$  starts similar to the behavior post FET OFF event in the over current protection scheme.

Latch-off can also achieved in the similar way as explained in the overcurrent protection scheme.

#### 注

Connect IWRN pin to GND if only short-circuit protection is required.  $R_{ISCP}$  resistor can be selected as per セクション 8.3.4.

### 8.3.5 Analog Current Monitor Output (IMON)

TPS4811x-Q1 features an accurate analog load current monitor output (IMON) with adjustable gain. The current source at IMON terminal is configured to be proportional to the current flowing through the  $R_{SNS}$  current sense resistor. This current can be converted to a voltage using a resistor  $R_{IMON}$  from IMON terminal to GND terminal. This voltage, computed using 式 10, can be used as a means of monitoring current flow through the system.

Use 式 10 to calculate the  $V_{(IMON)}$ .

$$V_{(IMON)} = (V_{SNS} + V_{(OS\_SET)}) \times \text{Gain} \tag{10}$$

Where  $V_{SNS} = I\_LOAD \times R_{SNS}$  and  $V_{(OS\_SET)}$  is the input referred offset ( $\pm 200 \mu$ V) of the current sense amplifier ( $V_{SNS}$  to  $V_{(IMON)}$  scaling). Use the following equation to calculate gain.

$$\text{Gain} = \frac{0.9 \times R_{\text{IMON}}}{R_{\text{SET}}} \quad (11)$$

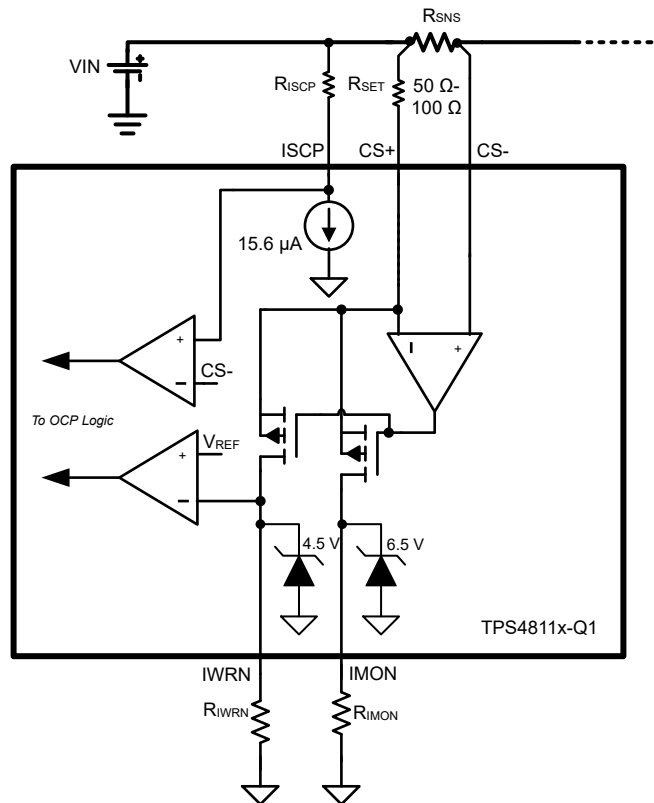
Where 0.9 is the current mirror factor between the current sense amplifier and the IMON pass FET.

The maximum voltage range for monitoring the current ( $V_{(\text{IMONmax})}$ ) is limited to minimum( $[V_{(\text{VS})} - 0.5\text{V}], 5.5\text{V}$ ) to ensure linear output. This puts limitation on maximum value of  $R_{\text{IMON}}$  resistor. The IMON pin has an internal clamp of 6.5 V (typical).

Accuracy of the current mirror factor is  $< \pm 1\%$ . Use the following equation to calculate the overall accuracy of  $V_{(\text{IMON})}$ .

$$\% V_{(\text{IMON})} = \frac{V_{(\text{OS\_SET})}}{V_{\text{SNS}}} \times 100 \quad (12)$$

☒ 8-11 shows external connections and simplified block diagram of current sensing and overcurrent protection implementation.

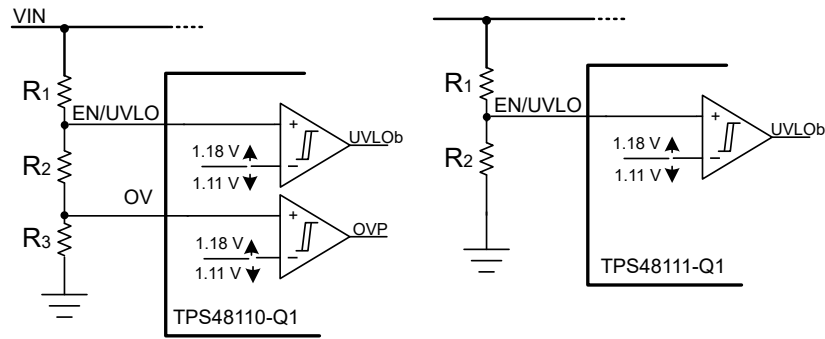


☒ 8-11. Current sensing and Overcurrent protection

### 8.3.6 Overvoltage (OV) and Undervoltage Protection (UVLO)

TPS4811x-Q1 has an accurate undervoltage protection ( $< \pm 2\%$ ) using EN/UVLO pin.

TPS48110-Q1 has an accurate overvoltage protection ( $< \pm 2\%$ ), providing robust load protection. Connect a resistor ladder as shown in ☒ 8-12 for undervoltage and overvoltage protection threshold programming.



**図 8-12. Programming Overvoltage and Undervoltage Protection Threshold**

**8.3.7 Device Functional Mode (Shutdown Mode)**

The TPS4811x-Q1 has two modes of operation. Active mode and low IQ shutdown mode. If the EN/UVLO pin voltage is greater than the rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers and all the protection and diagnostic features are enabled.

If the EN/UVLO voltage is pulled <math>V\_{(ENF)}</math>, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The external FETs turn OFF. The TPS4811x-Q1 consumes low IQ of 1.6  $\mu\text{A}$  (typical) in this mode.

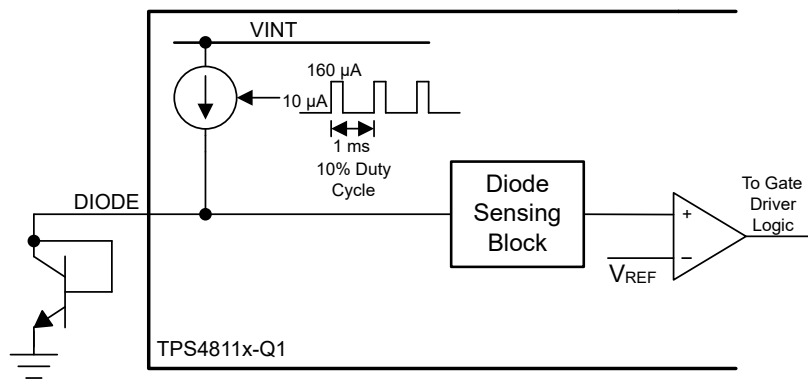
**8.3.8 Remote Temperature sensing and Protection (DIODE)**

The device features an integrated remote temperature sensing, protection and dedicated fault output. In TPS4811x-Q1, remote temperature measurement is done by using external transistor in diode configuration. Connect the DIODE pin of TPS4811x-Q1 to the collector and base of an MMBT3904 BJT. The temperature is calculated internally based on difference of measured diode voltages at two test currents.

In TPS48110-Q1, after the sensed temperature reaches 150°C, the device pulls PD low to SRC, turning off the external FET and asserts  $\overline{\text{FLT\_T}}$  low. After the temperature reduces to 130°C, an internally fixed auto-retry cycle of 512 ms commences.  $\overline{\text{FLT\_T}}$  de-asserts and the external FET turns ON after the retry duration of 512 ms is lapsed.

In TPS48111-Q1, after the sensed temperature crosses 150°C, PD and G get pulled low to SRC. After the TSD hysteresis, PU and G stays latched OFF. Latch gets reset by toggling EN/UVLO below  $V_{(ENF)}$  or by power cycling VS below  $V_{(VS\_PORF)}$ .

**図 8-13** shows simplified block diagram of TPS4811x-Q1 DIODE based remote temperature sensing.

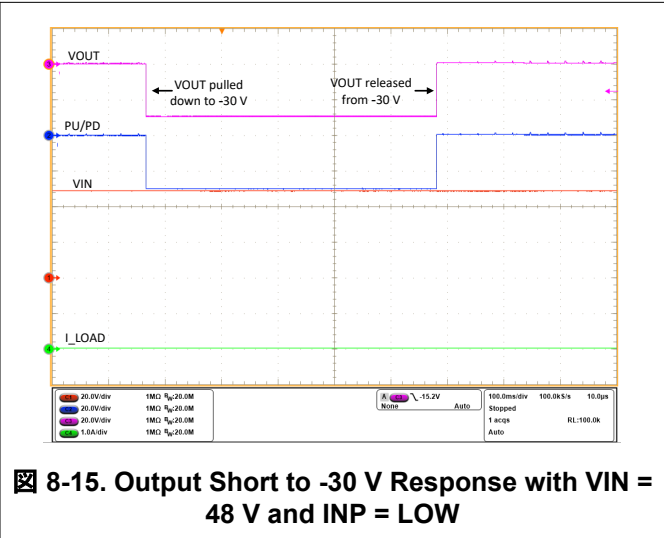
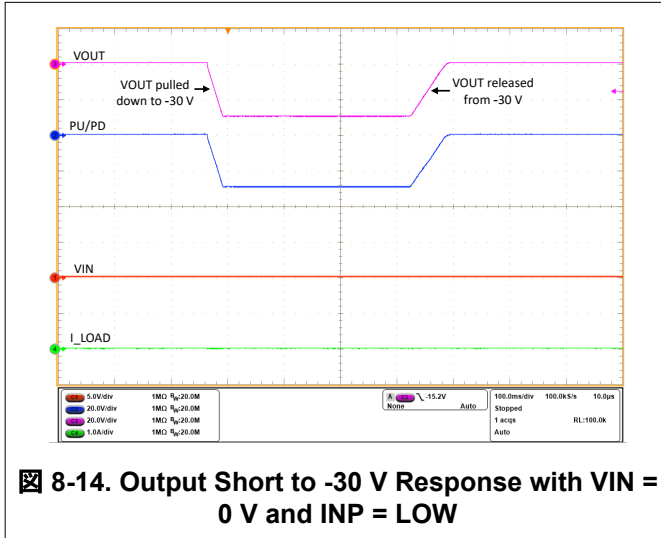


**図 8-13. DIODE based Remote Temperature Sensing Block Diagram**



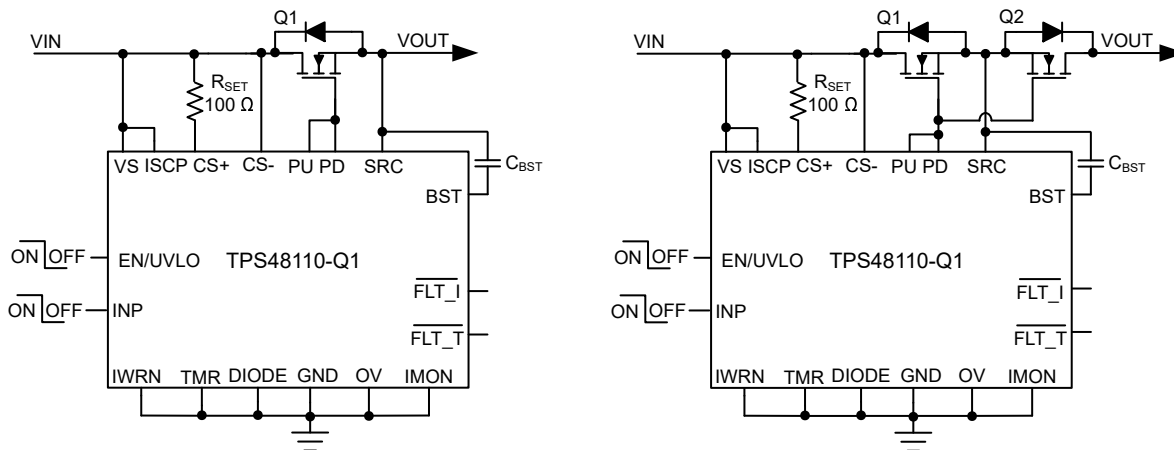
### 8.3.9 Output Reverse Polarity Protection

The TPS4811x-Q1 withstands output reverse voltages down to -30 V. With INP low, PD is pulled low to SRC and keeps the external FET OFF even with output (SRC) voltage at negative levels preventing high current flow and protecting the main FET. Refer to [Figure 8-14](#) and [Figure 8-15](#) for test waveforms.



### 8.3.10 TPS4811x-Q1 as a Simple Gate Driver

[Figure 8-16](#) shows application schematics of TPS4811x-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The protection features like two-level overcurrent protection, overvoltage protection, and overtemperature protection are disabled.



## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The TPS4811x-Q1 family is a 100-V smart high side driver with protection and diagnostics. The TPS4811x-Q1 device controls external N-channel MOSFETs and its drive architecture is suitable to drive back-to-back N-Channel MOSFETs. The strong gate 3.7-A peak source and 4-A peak sink capabilities enable switching parallel MOSFETs in high current applications such as circuit breaker in Powertrain (DC/DC converter), Battery Management System, Electric Power Steering, and driving PTC heater loads etc. The TPS4811x-Q1 device provides two-level adjustable overcurrent protection with adjustable circuit breaker timer, fast short-circuit protection, accurate analog current monitor output, and remote overtemperature protection.

The variant TPS48111-Q1 features a separate pre-charge driver (G) with independent control input (INP\_G). This feature enables system designs that need to pre-charge the large output capacitance before turning ON the main power path.

The following design procedure can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool [TPS4811-Q1 Design Calculator](#) is available in the web product folder.

### 9.2 Typical Application: Driving HVAC PTC Heater Load on KL40 Line in Power Distribution Unit

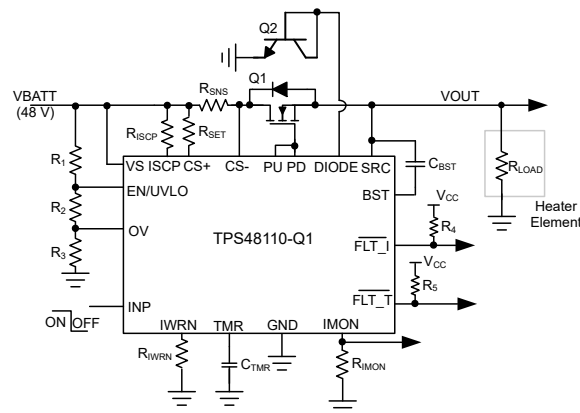


図 9-1. Typical Application Schematic: Driving HVAC PTC Heater

### 9.2.1 Design Requirements

表 9-1 shows the design parameters for this application example.

**表 9-1. Design Parameters**

PARAMETER	VALUE
Typical input voltage, $V_{IN}$	48 V
Undervoltage lockout set point, $V_{INUVLO}$	24 V
OV set point, $V_{INOVLP}$	58 V
Maximum load current, $I_{OUT}$	12 A
Overcurrent protection threshold, $I_{OC}$	15 A
Short-circuit protection threshold, $I_{SC}$	20 A
Fault timer period ( $t_{OC}$ )	1 ms
Fault response	Auto-retry
Load resistance, $R_{LOAD}$	$4 \pm 0.2 \Omega$
Load switching frequency, $F_{SW}$	100 Hz

### 9.2.2 Detailed Design Procedure

#### Selection of Current Sense Resistor, $R_{SNS}$

The recommended range of the overcurrent protection threshold voltage,  $V_{(SNS\_WRN)}$ , extends from 10 mV to 200 mV. Values near the low threshold of 10 mV can be affected by the system noise. Values near the upper threshold of 200 mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 25 mV is selected as the overcurrent protection threshold voltage. The current sense resistor,  $R_{SNS}$  can be calculated using 式 13.

$$R_{SNS} = \frac{V_{(SNS\_WRN)}}{I_{OC}} = \frac{25 \text{ mV}}{15 \text{ A}} = 1.66 \text{ m}\Omega \quad (13)$$

The next smaller available sense resistor 1.5 m $\Omega$ , 1% is chosen.

#### Selection of Scaling Resistor, $R_{SET}$

$R_{SET}$  is the resistor connected between VS and CS+ pins. This resistor scales the overcurrent protection threshold voltage and coordinates with  $R_{IWRN}$  and  $R_{IMON}$  to determine the overcurrent protection threshold and current monitoring output. The recommended range of  $R_{SET}$  is 50  $\Omega$ –100  $\Omega$ .

$R_{SET}$  is selected as 100  $\Omega$ , 1% for this design example.

#### Programming the Overcurrent Protection Threshold – $R_{IWRN}$ Selection

The  $R_{IWRN}$  sets the overcurrent protection (circuit breaker detection) threshold, whose value can be calculated using 式 14.

$$R_{IWRN} (\Omega) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{OC}} \quad (14)$$

To set 15 A as overcurrent protection threshold,  $R_{IWRN}$  value is calculated to be 52.88 k $\Omega$ .

Choose the closest available standard value: 54 k $\Omega$ , 1%

### Programming the Short-Circuit Protection Threshold – $R_{ISCP}$ Selection

The  $R_{ISCP}$  sets the short-circuit protection threshold, whose value can be calculated using 式 15.

$$R_{ISCP} (\Omega) = \frac{I_{SC} \times R_{SNS}}{15.6 \mu} - 600 \quad (15)$$

To set 20 A as short-circuit protection threshold,  $R_{ISCP}$  value is calculated to be 1.32 k $\Omega$ .

Choose the closest available standard value: 1.3 k $\Omega$ , 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between ISCP and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1 nF across ISCP and CS- pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

### Programming the Fault timer Period – $C_{TMR}$ Selection

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This blanking interval,  $t_{OC}$  (or circuit breaker interval,  $T_{CB}$ ) can be set by selecting appropriate capacitor  $C_{TMR}$  from TMR pin to ground. The value of  $C_{TMR}$  to set 1 ms for  $t_{OC}$  can be calculated using 式 16.

$$C_{TMR} = \frac{82 \mu \times t_{OC}}{1.2} = 68.33 \text{ nF} \quad (16)$$

Choose closest available standard value: 68 nF, 10%.

### Selection of MOSFET, $Q_1$

For selecting the MOSFET  $Q_1$ , important electrical parameters are the maximum continuous drain current  $I_D$ , the maximum drain-to-source voltage  $V_{DS(MAX)}$ , the maximum drain-to-source voltage  $V_{GS(MAX)}$ , and the drain-to-source ON resistance  $R_{DS(ON)}$ .

The maximum continuous drain current,  $I_D$ , rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage,  $V_{DS(MAX)}$ , must be high enough to withstand the highest voltage seen in the application. Considering 60 V as the maximum application voltage, MOSFETs with  $V_{DS}$  voltage rating of 80 V is suitable for this application.

The maximum  $V_{GS}$  TPS4811-Q1 can drive is 13 V, so a MOSFET with 15-V minimum  $V_{GS}$  rating must be selected.

To reduce the MOSFET conduction losses, lowest possible  $R_{DS(ON)}$  is preferred.

Based on the design requirements, IPB160N08S4-03ATMA1 is selected and its ratings are:

- 80-V  $V_{DS(MAX)}$  and  $\pm 20$ -V  $V_{GS(MAX)}$
- $R_{DS(ON)}$  is 2.6-m $\Omega$  typical at 10-V  $V_{GS}$
- MOSFET  $Q_{g(total)}$  is 86 nC

### Selection of Bootstrap Capacitor, $C_{BST}$

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 100  $\mu$ A. In case of switching applications, the BST must be powered externally from  $V_{AUX}$  supply (ranging between 8.1 V to 15 V) through a low-leakage silicon diode such as CMHD3595 or BAT46WH,115 to

avoid collapsing the BST-SRC supply. This need is determined by the value of the switching frequency and MOSFET gate charge.

The maximum possible frequency without external supply is given by 式 17.

$$F_{SW,max} = \frac{I_{(BST)}}{2 \times Q_{g(total)}} = 581 \text{ Hz} \quad (17)$$

As the present application is switched at 100 Hz, external supply is not required. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two parallel BUK7S0R5-40HJ MOSFETs.

$$C_{BST} = \frac{Q_{g(total)}}{1 \text{ V}} = 380 \text{ nF} \quad (18)$$

Choose closest available standard value: 470 nF, 10 %.

### Setting the Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage set point are adjusted using an external voltage divider network of  $R_1$ ,  $R_2$  and  $R_3$  connected between VS, EN/UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 式 19 and 式 20.

$$V_{(OVR)} = \frac{R_3}{(R_1 + R_2 + R_3)} \times V_{IN_{OVP}} \quad (19)$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{(R_1 + R_2 + R_3)} \times V_{IN_{UVLO}} \quad (20)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for  $R_1$ ,  $R_2$  and  $R_3$ . However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current,  $I(R_{123})$  must be chosen to be 20 times greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications,  $V_{(OVR)} = 1.18 \text{ V}$  and  $V_{(UVLOR)} = 1.18 \text{ V}$ . From the design requirements,  $V_{IN_{OVP}}$  is 58 V and  $V_{IN_{UVLO}}$  is 24 V. To solve the equation, first choose the value of  $R_1 = 470 \text{ k}\Omega$  and use 式 20 to solve for  $(R_2 + R_3) = 24.3 \text{ k}\Omega$ . Use 式 19 and value of  $(R_2 + R_3)$  to solve for  $R_3 = 10.1 \text{ k}\Omega$  and finally  $R_2 = 14.2 \text{ k}\Omega$ . Choose the closest standard 1 % resistor values:  $R_1 = 470 \text{ k}\Omega$ ,  $R_2 = 14.3 \text{ k}\Omega$ , and  $R_3 = 10.2 \text{ k}\Omega$ .

### Choosing the Current Monitoring Resistor, $R_{IMON}$

Voltage at IMON pin  $V_{(IMON)}$  is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The  $R_{IMON}$  must be selected based on the maximum load current and the input voltage range of the ADC used.  $R_{IMON}$  is set using 式 21.

$$V_{(IMON)} = \left( V_{SNS} + V_{(OS\_SET)} \right) \times \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (21)$$

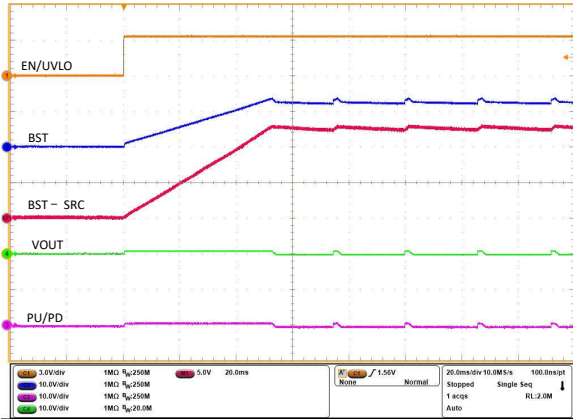
Where  $V_{SNS} = I_{OC} \times R_{SNS}$  and  $V_{(OS\_SET)}$  is the input referred offset ( $\pm 200 \mu\text{V}$ ) of the current sense amplifier.

For  $I_{OC} = 15 \text{ A}$  and considering the operating range of ADC to be 0 V to 3.3 V (for example,  $V_{(IMON)} = 3.3 \text{ V}$ ),  $R_{IMON}$  can be calculated as

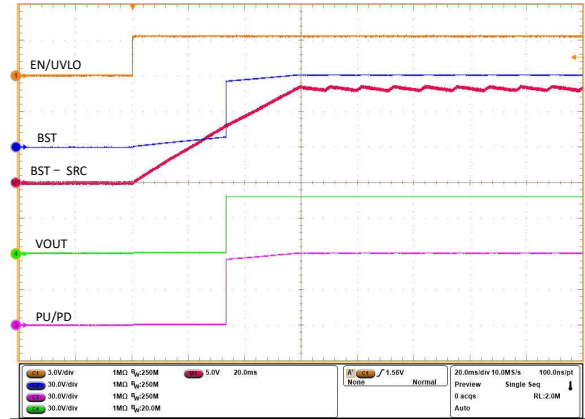
$$R_{\text{IMON}} = \frac{V_{(\text{IMON})} \times R_{\text{SET}}}{(V_{\text{SNS}} + V_{(\text{OS\_SET})}) \times 0.9} = 16.52 \text{ k}\Omega \quad (22)$$

Selecting  $R_{\text{IMON}}$  value less than shown in 式 22 ensures that ADC limits are not exceeded for maximum value of load current. Choose the closest available standard value: 16.5 k $\Omega$ , 1%.

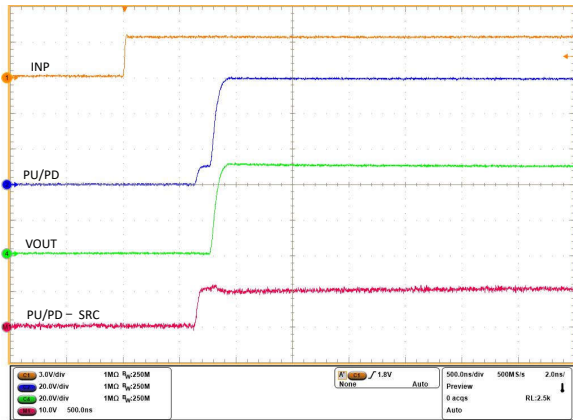
### 9.2.3 Application Curves



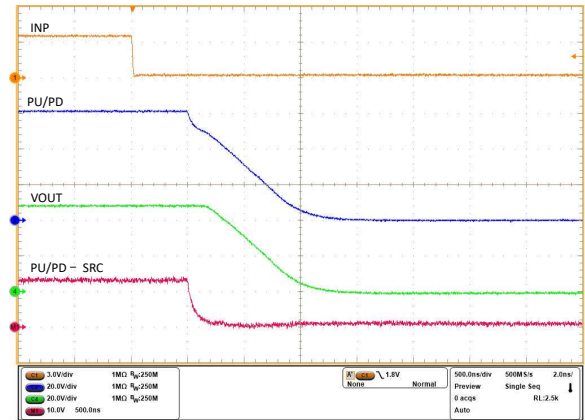
9-2. Start-Up Profile of Bootstrap Voltage for INP = GND and  $C_{BST} = 470 \text{ nF}$



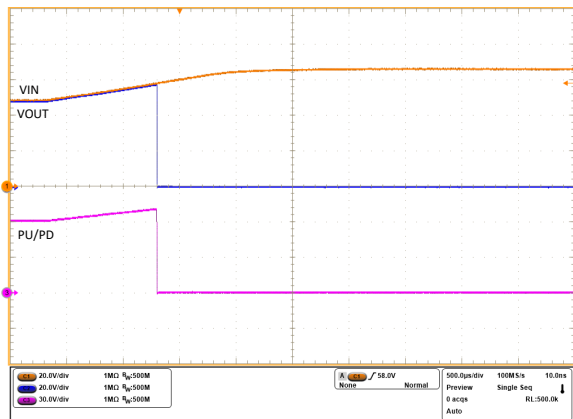
9-3. Start-Up Profile of Bootstrap Voltage for INP = HIGH and  $C_{BST} = 470 \text{ nF}$



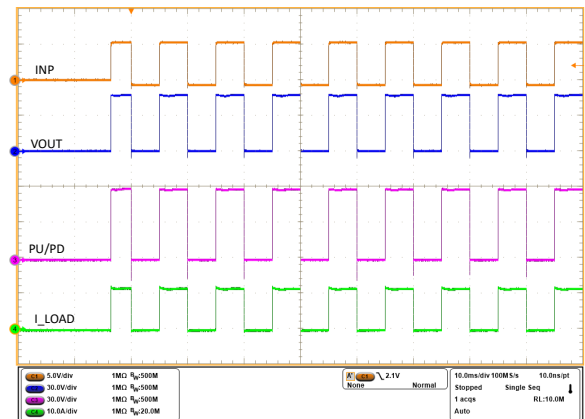
9-4. Turn-ON Response of TPS48110-Q1 for INP -> LOW to HIGH and  $C_{BST} = 470 \text{ nF}$



9-5. Turn-OFF Response of TPS48110-Q1 for INP -> HIGH to LOW and  $C_{BST} = 470 \text{ nF}$



9-6. Overvoltage Cut-off Response at 58-V Level of TPS48110-Q1



9-7. Load Switching at 100 Hz With TPS48110-Q1

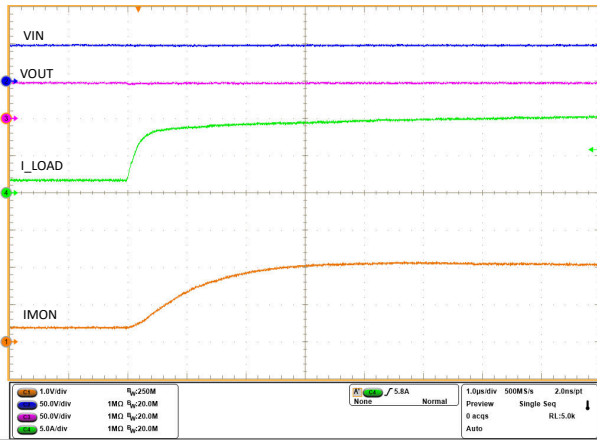


図 9-8. IMON Response During 10-A Load Step

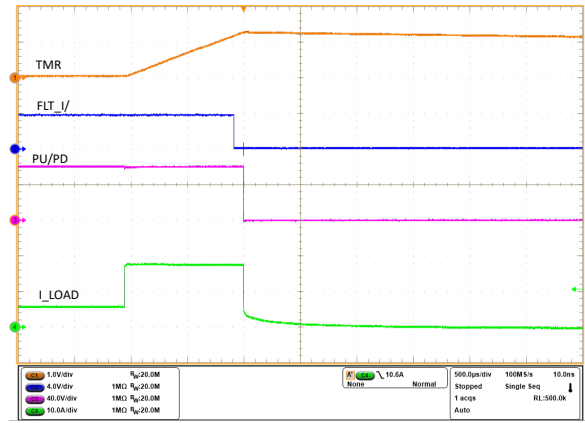


図 9-9. Overcurrent Response of TPS48110-Q1 for a Load Step from 5 A to 18 A With 15-A Overcurrent Protection Setting

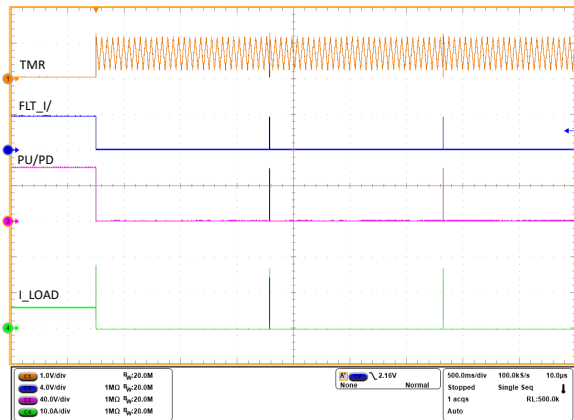


図 9-10. Auto-Retry Response of TPS48110-Q1 for an Overcurrent Fault

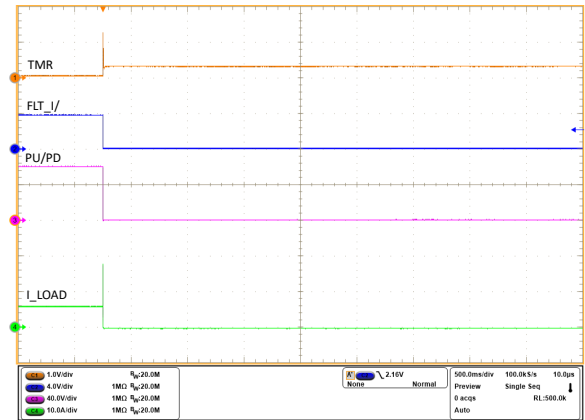


図 9-11. Latch-off Response of TPS48110-Q1 for an Overcurrent Fault

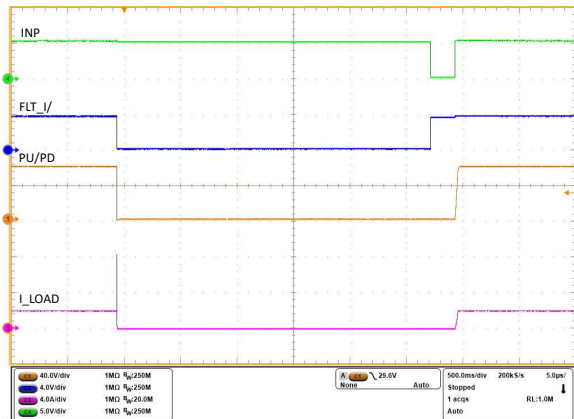


図 9-12. Response During Coming Out of Overload Fault With INP Reset

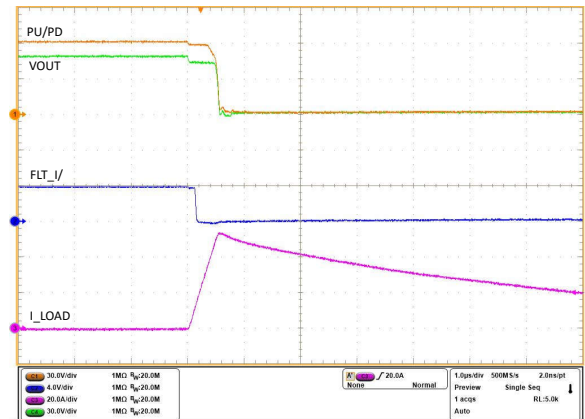


図 9-13. Output Hot-Short Response of the TPS48110-Q1 Device



### 9.3 Typical Application: Driving B2B FETs With Pre-charging the Output Capacitance

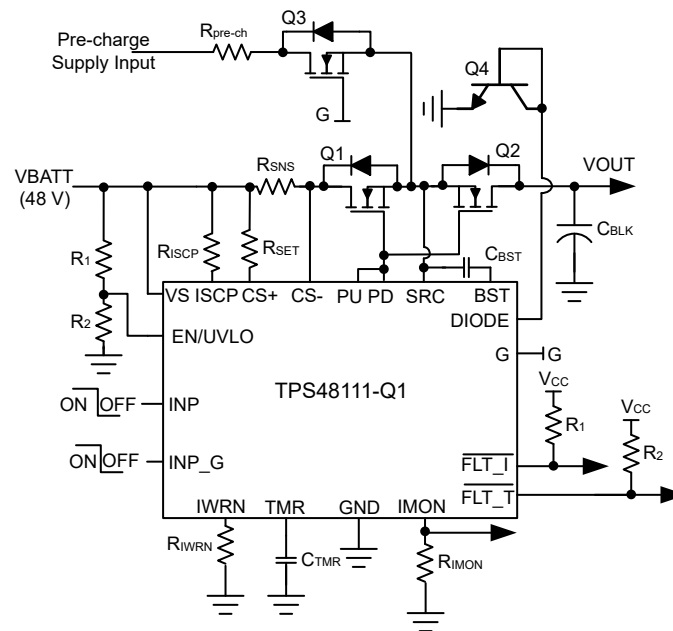


図 9-14. Typical Application Schematic: Driving DC-DC Converter Loads in Powertrain

#### 9.3.1 Design Requirements

表 9-2 shows the design parameters for this application example.

表 9-2. Design Parameters

PARAMETER	VALUE
Typical input voltage, $V_{IN}$	48 V
Undervoltage lockout set point, $V_{IN_{UVLO}}$	24 V
Maximum load current, $I_{OUT}$	40 A
Overcurrent protection threshold, $I_{OC}$	50 A
Short-circuit protection threshold, $I_{SC}$	60 A
Fault timer period ( $t_{OC}$ )	1 ms
Fault response	Latch-off
Load capacitance, $C_{OUT}$	400 $\mu$ F
Inrush current limit, $I_{inrush}$	500 mA

#### 9.3.2 External Component Selection

By following similar design procedure as outlined in [Detailed Design Procedure](#), the external component values are calculated as below:

- $R_{SNS} = 500 \mu\Omega$
- $R_{SET} = 100 \Omega$
- $R_{IWRN} = 47 \text{ k}\Omega$  to set 50 A as overcurrent protection threshold
- $R_{ISCP} = 1.4 \text{ k}\Omega$  to set 60 A as short-circuit protection threshold

- $C_{TMR} = 68 \text{ nF}$  to set 1 ms circuit breaker time
- $R_1$  and  $R_2$  are selected as 470 k $\Omega$  and 24.9 k $\Omega$  respectively to set  $V_{IN}$  undervoltage lockout threshold at 24 V
- $R_{IMON} = 15 \text{ k}\Omega$  to limit maximum  $V_{(IMON)}$  voltage to 3.3 V at full-load current of 50 A
- To reduce conduction losses, IAUS300N08S5N012 MOSFET is selected. Two FETs are used in parallel for control and another two FETs are used in parallel for reverse current blocking
  - 80-V  $V_{DS(MAX)}$  and  $\pm 20\text{-V } V_{GS(MAX)}$
  - $R_{DS(ON)}$  is 1-m $\Omega$  typical at 10-V  $V_{GS}$
  - $Q_g$  of each MOSFET is 231 nC
- $C_{BST} = (4 \times Q_g) / 1 \text{ V} = 1 \text{ }\mu\text{F}$

### Selection of Pre-Charge Resistor

The value of pre-charge resistor must be selected to limit the inrush current to  $I_{inrush}$  as per 式 23.

$$R_{pre-ch} = \frac{V_{IN}}{I_{inrush}} = 96 \text{ }\Omega \quad (23)$$

The power rating of the pre-charge resistor is decided by the average power dissipation given by 式 24.

$$P_{avg} = \frac{E_{pre-ch}}{T_{pre-ch}} = \frac{0.5 \times C_{OUT} \times V_{IN}^2}{5 \times R_{pre-ch} \times C_{OUT}} = 2.4 \text{ W} \quad (24)$$

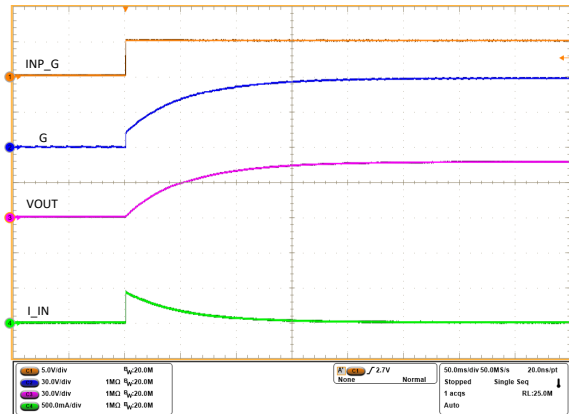
The peak power dissipation in the pre-charge resistor is given by 式 25.

$$P_{peak} = \frac{V_{IN}^2}{R_{pre-ch}} = 24 \text{ W} \quad (25)$$

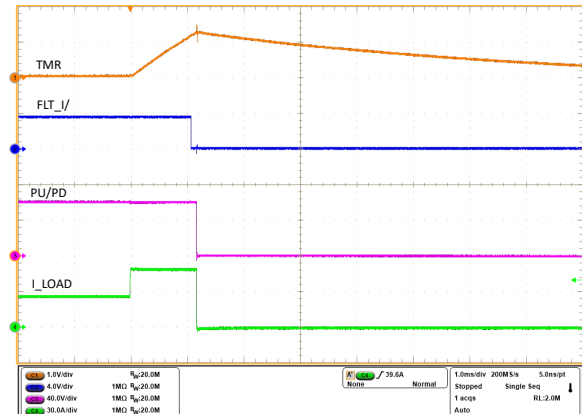
Two 220- $\Omega$ , 1.5-W, 5% CRCW2512220RJNEGHP resistors are used in parallel to support both average and peak power dissipation.

TI suggests the designer to share the entire power dissipation profile of pre-charge resistor with the resistor manufacturer and get their recommendation.

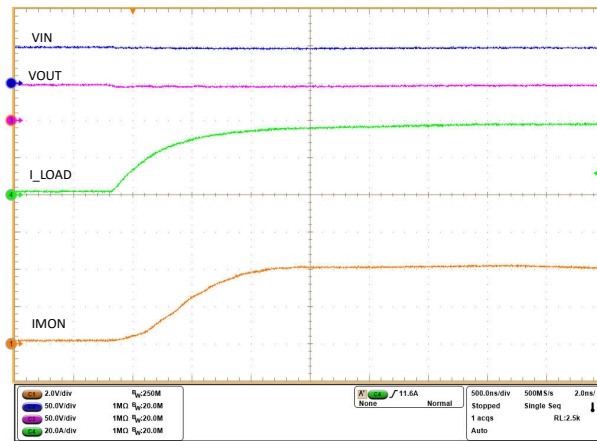
### 9.3.3 Application Curves



9-15. Pre-charge Profile of the Output Capacitance ( $V_{IN} = 48\text{ V}$ ,  $C_{OUT} = 440\ \mu\text{F}$ , No Load)



9-16. Overcurrent Response of TPS4811-Q1 for a Load Step from 24 A to 54 A With 50-A Overcurrent Protection Setting



9-17. IMON Response During 40-A Load Step

## 9.4 Power Supply Recommendations

When the external MOSFETs turn OFF during the conditions such as INP control, overvoltage cutoff, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS4811-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above  $V_{(VS\_PORR)}$  level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a  $R_{VS} - C_{VS}$  filter between the input supply line and VS pin to filter out the supply noise. TI recommends  $R_{VS}$  value around 100  $\Omega$ .

In case where large  $di/dt$  is involved, the system and layout parasitic inductances can generate large differential signal voltages between ISCP and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1 nF ( $C_{SCP}$ ) across ISCP and CS- pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

The following figure shows the circuit implementation with optional protection components.

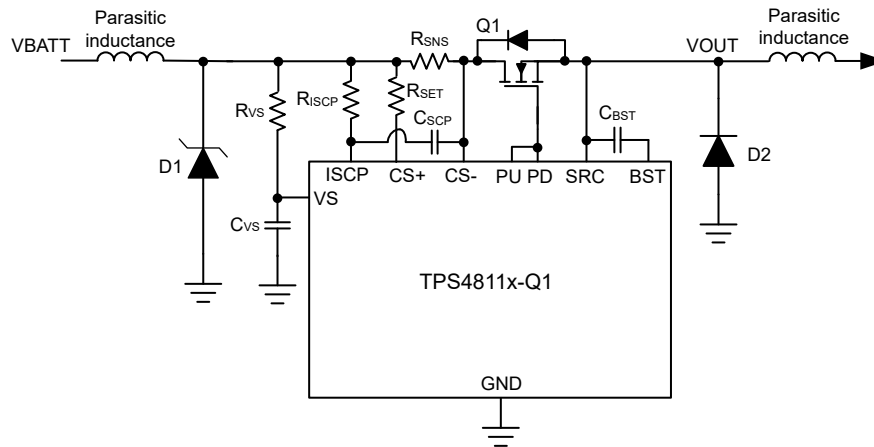


図 9-18. Circuit Implementation With Optional Protection Components for TPS4811-Q1

## 9.5 Layout

### 9.5.1 Layout Guidelines

- The sense resistor ( $R_{SNS}$ ) must be placed close to the TPS4811x-Q1 and then connect  $R_{SNS}$  using the Kelvin techniques. Refer to [Choosing the Right Sense Resistor Layout](#) for more information on the Kelvin techniques.
- For all the applications, TI recommends a 0.1  $\mu\text{F}$  or higher value ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- The high current path from the board's input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the GATE of the MOSFETs are close to PU/PD pins to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external boot-strap capacitor must be placed close to BST and SRC pins to form very short loop.
- The ground connections for the various components around the TPS4811x-Q1 must be connected directly to each other, and to the TPS4811x-Q1's GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- The DIODE pin sources current to measure the temperature. TI recommends BJT MMBT3904 to use as a remote temperature sense element. Take care in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. In addition, TI recommends to make a Kelvin connection from the emitter of the MMBT3904 to the GND of the part to ensure an accurate measurement. Additionally, a small 1000 pF bypass capacitor must be placed in parallel with the MMBT3904 to reduce the effects of noise.

### 9.5.2 Layout Example

- Top Layer
- Inner Layer GND plane
- Inner Layer PGND plane
- Via to GND plane
- Via to PGND plane

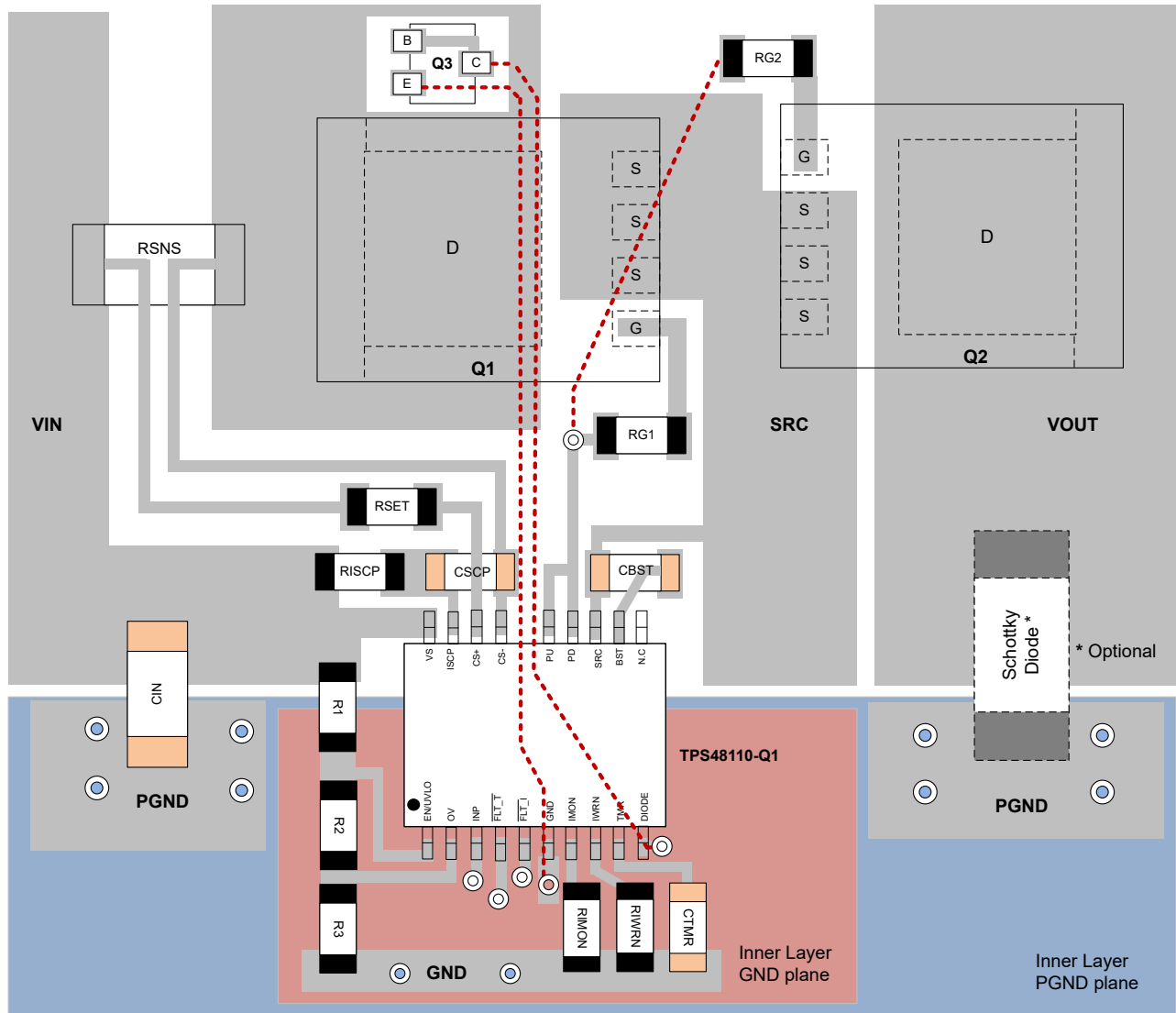


図 9-19. Typical PCB Layout Example With TPS4811-Q1 With B2B MOSFETs

## 10 Device and Documentation Support

### 10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 10.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (December 2022) to Revision D (April 2024)	Page
• Updated the DIODE sense TSD rising threshold, $T_{(DIODE\_TSD\_rising)}$ , specification in the <i>Electrical Characteristics</i> section.....	5

Changes from Revision B (September 2022) to Revision C (December 2022)	Page
• デバイス ステータスを「事前情報」から「量産データ」に変更.....	1

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS48110AQDGXRQ1	ACTIVE	VSSOP	DGX	19	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2UZS	<a href="#">Samples</a>
TPS48111LQDGXRQ1	ACTIVE	VSSOP	DGX	19	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2XXS	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS48110AQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
TPS48111LQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS48110AQDGXRQ1	VSSOP	DGX	19	5000	356.0	356.0	35.0
TPS48111LQDGXRQ1	VSSOP	DGX	19	5000	356.0	356.0	35.0

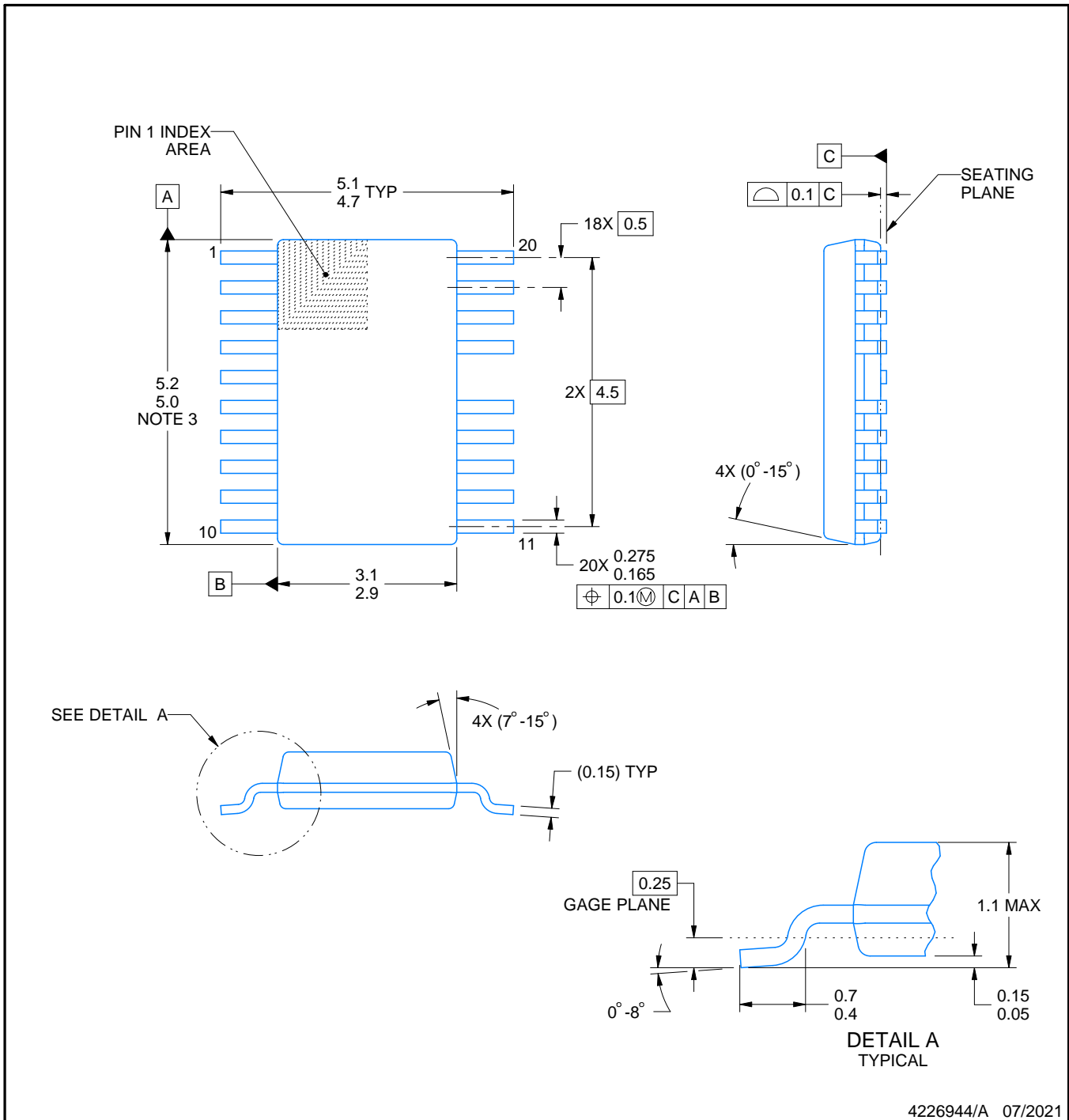
# DGX0019A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226944/A 07/2021

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

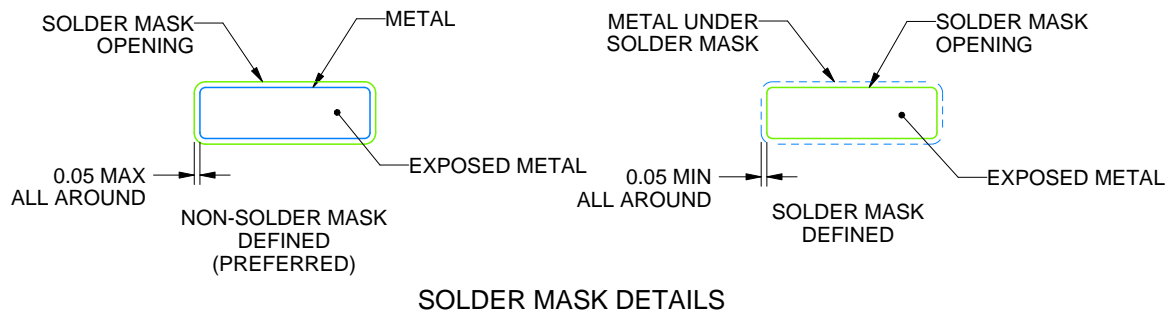
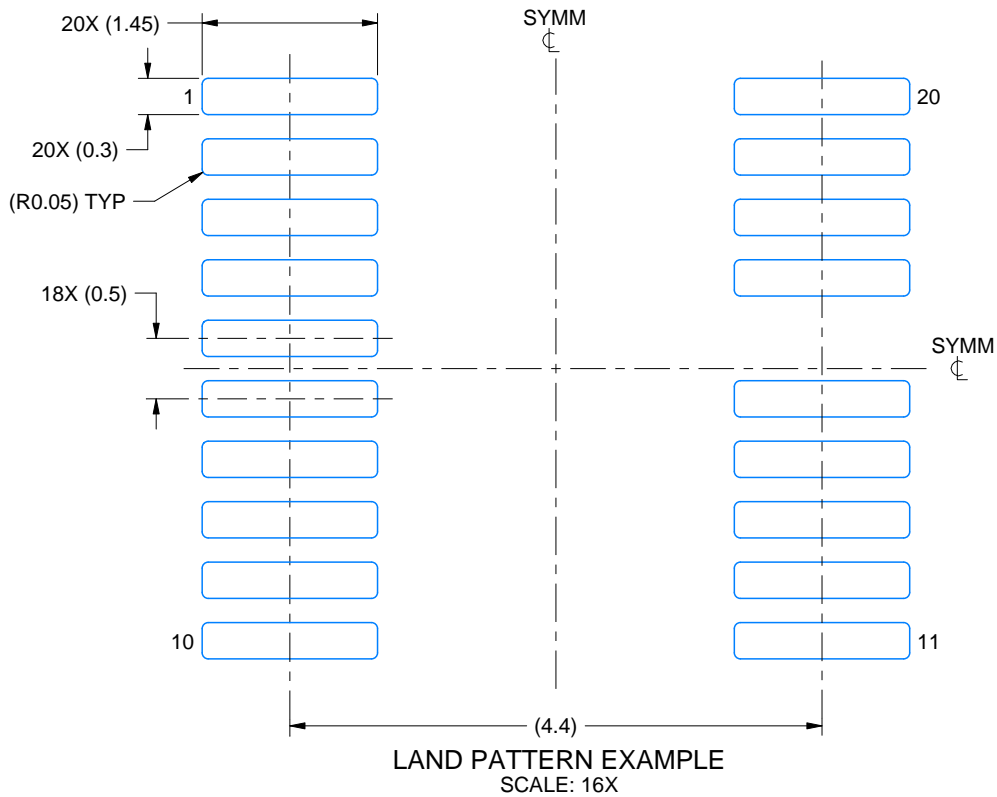
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226944/A 07/2021

NOTES: (continued)

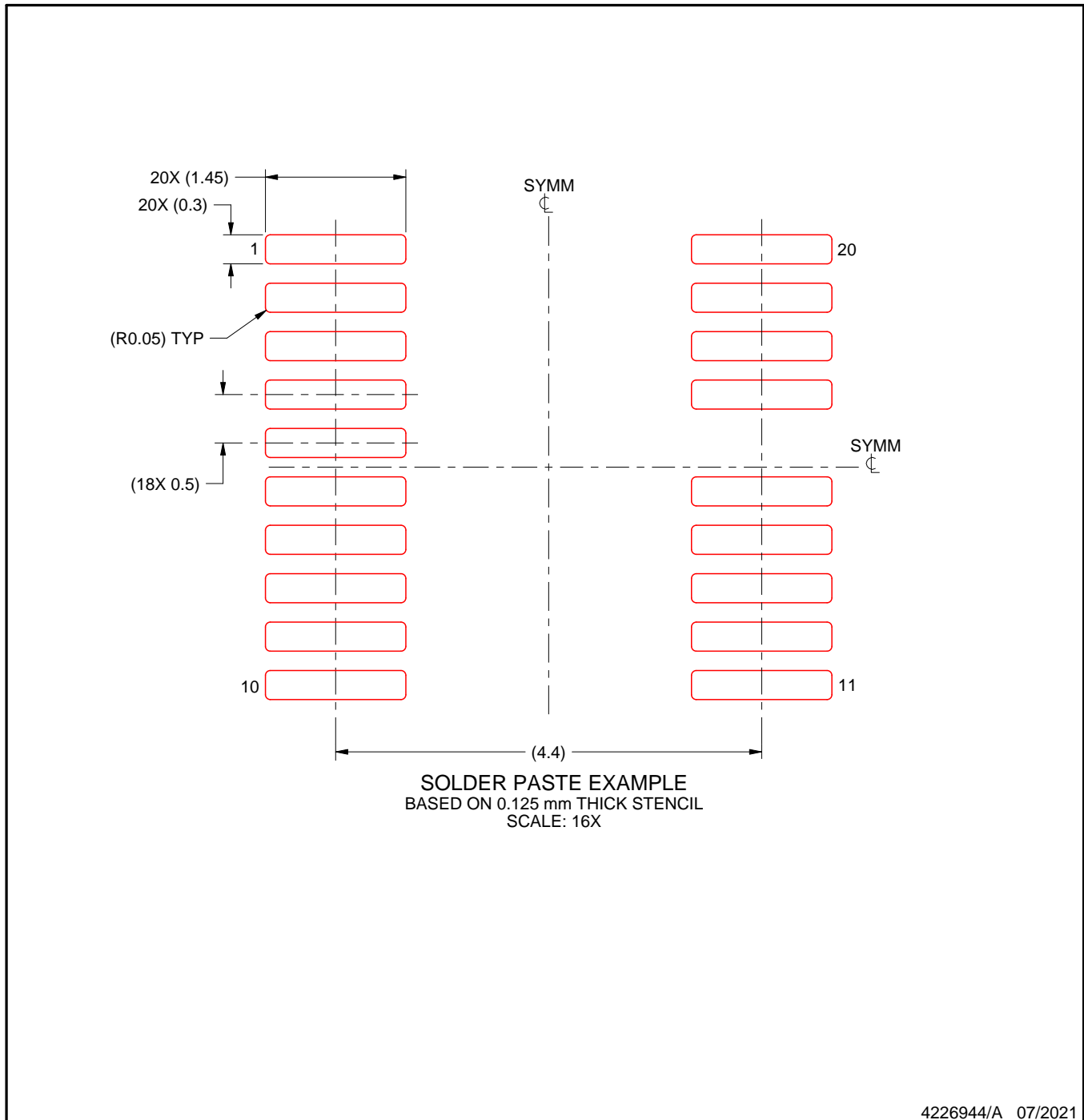
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated