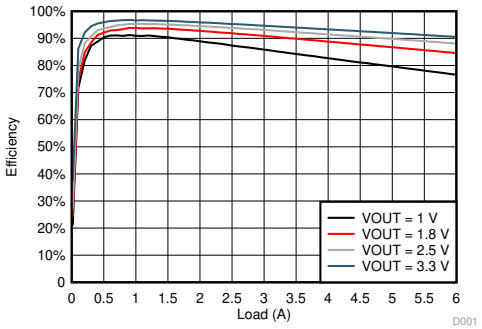
TPS50601A-SP 放射線耐性強化型、3V ～ 7V 入力、6A 同期整流降圧型コンバータ

1 特長

- 5962-10221:
  - 最大 TID 100 krad(Si) に放射線耐性を強化
  - ELDRSフリー 100krad (Si) ～ 10mrad(Si)/s
  - 単一イベント・ラッチアップ (SEL) 耐性:
    LET = 75MeV-cm^2/mg
  - SEB および SEGR 耐性:75MeV-cm^2/mg、SOA 曲線を利用可能
  - SET/SEFI 断面プロットを利用可能
- **ピーク効率：96.6% (V_O = 3.3V)**
- **58mΩ/50mΩのMOSFETを内蔵**
- **電源レール：3～7V (VIN)**
- **最大出力電流 6A**
- **柔軟なスイッチング周波数オプション**
  - 100kHz ～ 1MHz の可変内部発振器
  - 外部同期機能:100kHz ～ 1MHz
  - マスタ/スレーブ・アプリケーション用に SYNC ピンを 500kHz 出力として構成可能
- **温度、放射線、ライン/負荷レギュレーションの範囲全体で 0.804V±1.5% の基準電圧**
- **プリバイアスされた出力への単調スタートアップ**
- **外付けのコンデンサによりソフトスタートを設定可能**
- **入力イネーブルとパワー・グッド出力による電源シーケンス**
- **低電圧および過電圧用のパワー・グッド出力モニタ**
- **可変の入力低電圧誤動作防止 (UVLO)**
- **航空宇宙アプリケーション向けの、放熱特性に優れた 20 ピン超小型セラミック・フラットパック・パッケージ (HKH)**

VIN＝PVIN＝5Vでの効率



2 アプリケーション

- **人工衛星のポイント・オブ・ロード電源：FPGA、マイクロコントローラ、データ・コンバータ、ASIC 用**
- **人工衛星のペイロード**
- **放射線耐性強化アプリケーション**
- **軍事用温度範囲 (-55℃～125℃) に対応**
- **エンジニアリング評価用 (/EM) サンプルを利用可能**

3 概要

TPS50601A-SPは放射線耐性を強化した7V、6A同期整流降圧型コンバータで、高効率とハイサイド/ローサイドMOSFET内蔵により、小型設計に最適化されています。電流モード制御による部品数の削減と、高スイッチング周波数によるインダクタ・サイズの縮小が可能で、省スペースを実現します。このデバイスは、放熱特性に優れた、超小型の20ピン・セラミック・フラットパック・パッケージで供給されます。

出力電圧のスタートアップ・ランプはSS/TRピンにより制御されるため、スタンドアロンの電源でもトラッキング状況でも動作できます。イネーブルおよびオープン・ドレインのパワーグッド・ピンを適切に構成することにより、電源シーケンスも可能です。また、TPS50601A-SPはマスタ/スレーブ・モードに構成して、最大12Aの出力電流を供給できます。

製品情報(1)

型番	グレード	パッケージ
5962-1022102VSC	QMLV	CFP (20)(4)
5962R1022102VSC	RHA - 100krad (Si)	
TPS50601AHKH/EM	エンジニアリング評価(2)	
5962R1022102V9A	KGD RHA - 100krad (Si)	ダイ(3)

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

(2) これらのユニットは、技術的な評価のみを目的としています。標準とは異なるフローに従って処理されています。これらのユニットは、認定、量産、放射線テスト、航空での使用には適していません。これらの部品は、MILに規定されている温度範囲-55℃～125℃、または動作寿命全体にわたる性能を保証されていません。

(3) ワッフル・パックのベア・ダイ。

(4) 重量 = 1.22g で、約 ±10% に四捨五入されています。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (August 2018) から **Revision D** に変更 **Page**

- 「*製品情報*」表に「重量 = 1.22g」の注を追加 ... 1
- Changed the *Pin Configuration* image ... 4
- Changed SYNC out high level threshold MIN value From: 2 V To: V_{IN} - 0.3 in the *Electrical Characteristics* table ... 10
- Deleted test Condition "Percent of program frequency" from SYNC in frequency range in the *Electrical Characteristics* table ... 10
- Changed "180° out of phase to the internal 500-kHz switching frequency." To: "180° in phase to the internal 500-kHz switching frequency." in the Description of 表 3 ... 19
- Changed "180° out of phase respect to the internal oscillator.." To: "180° in phase respect to the internal oscillator.." in the *Parallel Operation* section ... 28
- Changed "(180° out of phase respect to the master device)." To: "(180° in phase respect to the master device).." in the *Parallel Operation* section ... 29

Revision B (June 2018) から **Revision C** に変更 **Page**

- Replaced all coordinates in Bond Pad Coordinates in Microns table with corrected values ... 6

Revision A (March 2018) から **Revision B** に変更 **Page**

- Added Bare Die Information table ... 5
- Added Bond Pad Coordinates in Microns table ... 6

2017年9月発行のものから更新 **Page**

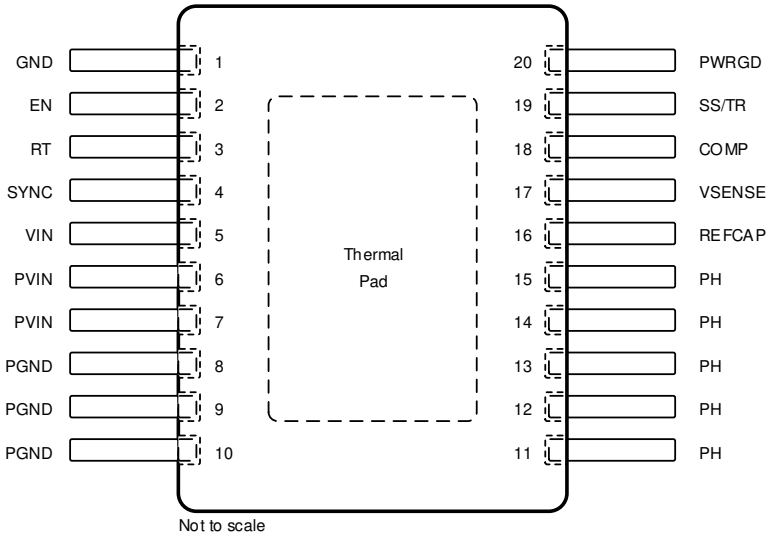
- 製品ステータスを「*事前情報*」から「*量産データ*」に 変更 ... 1

5 概要（続き）

ハイサイドFETにサイクル単位の電流制限を適用することで過負荷状況からデバイスを保護し、ローサイドのソース電流制限により電流暴走を防止します。また、ローサイドのシンク電流制限によりローサイドMOSFETをオフにすることで、過度な逆方向電流を防止します。ダイの温度がサーマル・シャットダウン温度を超えると、サーマル・シャットダウンによりデバイスがディセーブルになります。

6 Pin Configuration and Functions

HKH Package
20-Pin CFP
Bottom View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GND	—	Return for control circuitry.(1)
2	EN	I	EN pin is internally pulled up allowing for the pin to be floated to enable the device. Adjust the input undervoltage lockout (UVLO) with two resistors.
3	RT	I/O	In internal oscillation mode, a resistor is connected between the RT pin and GND to set the switching frequency. Leaving this pin floating sets the internal switching frequency to 500 kHz.
4	SYNC	I/O	Optional 100-kHz to 1-MHz external system clock input.
5	VIN	I	Input power for the control circuitry of the switching regulator.
6	PVIN	I	Input power for the output stage of the switching regulator.
7			
8	PGND	—	Return for low-side power MOSFET.
9			
10			
11	PH	O	Switch phase node.
12			
13			
14			
15			
16	REFCAP	O	Required 470-nF external capacitor for internal reference.
17	VSENSE	I	Inverting input of the gm error amplifier.
18	COMP	I/O	Error amplifier output and input to the output switch current comparator. Connect frequency compensation to this pin.
19	SS/TR	I/O	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
20	PWRGD	O	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during slow start.

(1) GND (pin 1, analog ground) must be connected to PGND external to the package. Thermal pad must be connected to a heat dissipating layer. Thermal pad is internally connected to the seal ring and GND.

Table 1. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	ALCU	1050 nm

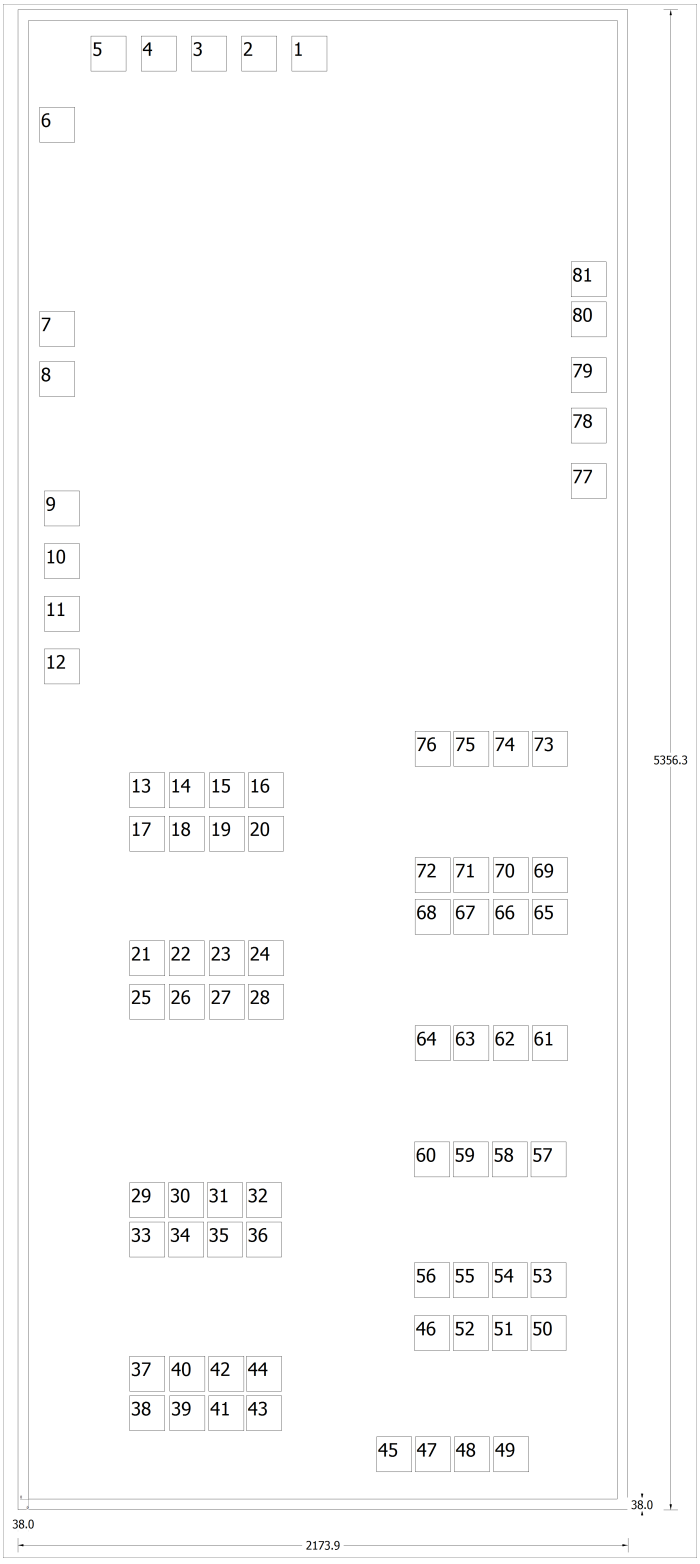


Table 2. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
AVSS	1	938.16	5098.41	1064.16	5224.41
AVSS	2	759.06	5098.41	885.06	5224.41
N/C	3	579.96	5098.41	705.96	5224.41
AVSS	4	400.86	5098.41	526.86	5224.41
AVSS	5	221.76	5098.41	347.76	5224.41
EN	6	38.7	4843.98	164.7	4969.98
RT	7	38.7	4115.43	164.7	4241.43
SYNC	8	38.7	3936.33	164.7	4062.33
VIN	9	55.89	3473.865	181.89	3599.865
VIN	10	55.89	3285.765	181.89	3411.765
VIN	11	55.89	3097.665	181.89	3223.665
VIN	12	55.89	2909.565	181.89	3035.565
PVIN	13	360.045	2468.025	486.045	2594.025
PVIN	14	500.805	2468.025	626.805	2594.025
PVIN	15	643.905	2468.025	769.905	2594.025
PVIN	16	782.505	2468.025	908.505	2594.025
PVIN	17	360.045	2312.595	486.045	2438.595
PVIN	18	500.805	2312.595	626.805	2438.595
PVIN	19	643.905	2312.595	769.905	2438.595
PVIN	20	782.505	2312.595	908.505	2438.595
PVIN	21	360.045	1868.265	486.045	1994.265
PVIN	22	500.805	1868.265	626.805	1994.265
PVIN	23	643.905	1868.265	769.905	1994.265
PVIN	24	782.505	1868.265	908.505	1994.265
PVIN	25	360.045	1712.835	486.045	1838.835
PVIN	26	500.805	1712.835	626.805	1838.835
PVIN	27	643.905	1712.835	769.905	1838.835
PVIN	28	782.505	1712.835	908.505	1838.835
PGND	29	360	1004.625	486	1130.625
PGND	30	498.6	1004.625	624.6	1130.625
PGND	31	637.2	1004.625	763.2	1130.625
PGND	32	775.8	1004.625	901.8	1130.625
PGND	33	360	863.955	486	989.955
PGND	34	498.6	863.955	624.6	989.955
PGND	35	637.2	863.955	763.2	989.955
PGND	36	775.8	863.955	901.8	989.955
PGND	37	360	384.525	486	510.525
PGND	38	360	243.855	486	369.855
PGND	39	503.1	243.855	629.1	369.855
PGND	40	503.1	384.525	629.1	510.525
PGND	41	641.7	243.855	767.7	369.855
PGND	42	641.7	384.525	767.7	510.525
PGND	43	775.8	243.855	901.8	369.855
PGND	44	775.8	384.525	901.8	510.525
PH	45	1239.66	97.425	1365.66	223.425
PH	46	1374.66	529.965	1500.66	655.965
PH	47	1378.26	97.425	1504.26	223.425

Table 2. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
PH	48	1516.86	97.425	1642.86	223.425
PH	49	1657.26	97.425	1783.26	223.425
PH	50	1790.46	529.965	1916.46	655.965
PH	51	1651.86	529.965	1777.86	655.965
PH	52	1513.26	529.965	1639.26	655.965
PH	53	1790.46	718.515	1916.46	844.515
PH	54	1651.86	718.515	1777.86	844.515
PH	55	1513.26	718.515	1639.26	844.515
PH	56	1374.66	718.515	1500.66	844.515
PH	57	1790.46	1150.065	1916.46	1276.065
PH	58	1651.86	1150.065	1777.86	1276.065
PH	59	1513.26	1150.065	1639.26	1276.065
PH	60	1374.66	1150.065	1500.66	1276.065
PH	61	1795.365	1565.1	1921.365	1691.1
PH	62	1655.865	1565.1	1781.865	1691.1
PH	63	1515.465	1565.1	1641.465	1691.1
PH	64	1376.865	1565.1	1502.865	1691.1
PH	65	1795.365	2016	1921.365	2142
PH	66	1655.865	2016	1781.865	2142
PH	67	1515.465	2016	1641.465	2142
PH	68	1376.865	2016	1502.865	2142
PH	69	1795.365	2164.86	1921.365	2290.86
PH	70	1655.865	2164.86	1781.865	2290.86
PH	71	1515.465	2164.86	1641.465	2290.86
PH	72	1376.865	2164.86	1502.865	2290.86
PH	73	1795.365	2615.76	1921.365	2741.76
PH	74	1655.865	2615.76	1781.865	2741.76
PH	75	1515.465	2615.76	1641.465	2741.76
PH	76	1376.865	2615.76	1502.865	2741.76
REFCAP_NU	77	1933.245	3572.46	2059.245	3698.46
VSENSE	78	1933.245	3770.415	2059.245	3896.415
COMP	79	1933.245	3949.515	2059.245	4075.515
SS	80	1933.2	4149.135	2059.2	4275.135
PWRGD	81	1933.2	4292.325	2059.2	4418.325

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7.5	V
	PVIN	–0.3	7.5	
	EN	–0.3	5.5	
	VSENSE	–0.3	3.3	
	COMP	–0.3	3.3	
	PWRGD	–0.3	5.5	
	SS/TR	–0.3	5.5	
	RT	–0.3	5.5	
	SYNC	–0.3	7.5	
Output voltage	REFCAP	–0.3	3.3	V
	PH	–1	7.5	
	PH 10-ns transient	–3	7.5	
Vdiff	(GND to exposed thermal pad)	–0.2	0.2	V
Source current	PH	Current limit	Current limit	A
	RT		±100	µA
Sink current	PH	Current limit	Current limit	A
	PVIN	Current limit	Current limit	A
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Operating junction temperature		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±750	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
T_J	Junction operating temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS50601A-SP HKH (CFP) 20 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.514	°C/W

(1) Taken per Mil Standard 883 method 1012.1.

7.5 Electrical Characteristics

T_J = –55°C to 125°C, V_{IN} = P_{VIN} = 3.0 V to 7.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (VIN AND PVIN Pins)					
PVIN operating input voltage		3		7	V
PVIN internal UVLO threshold	PV_{IN} rising		2.50		V
PVIN internal UVLO hysteresis			450		mV
VIN operating input voltage		3		7	V
VIN internal UVLO threshold	V_{IN} rising		2.75	3	V
VIN internal UVLO hysteresis			150		mV
VIN shutdown supply current	V_{EN} = 0 V		1.35	2.5	mA
VIN operating – non switching supply current	V_{SENSE} = V_{BG}		5	10	mA
Enable and UVLO (EN Pin)					
Enable threshold	Rising		1.14	1.18	V
	Falling	1.05	1.11		
Input current	V_{EN} = 1.1 V		6.1		µA
Hysteresis current	V_{EN} = 1.3 V		3		µA
Voltage Reference					
Voltage reference	0 A ≤ Iout ≤ 6 A, –55 to 125°C	0.792	0.804	0.816	V
REFCAP voltage	470 nF		1.211		V
Mosfet					
High-side switch resistance	PVIN = V_{IN} = 3 V, lead length = 4 mm		50		mΩ
High-side switch resistance(1)	PVIN = V_{IN} = 5 V, lead length = 4 mm		45		mΩ
High-side switch resistance(1)	PVIN = V_{IN} = 7 V, lead length = 4 mm		43		mΩ
Low-side switch resistance(1)	PVIN = V_{IN}= 3 V, lead length = 4 mm		35		mΩ
Low-side switch resistance(1)	PVIN = V_{IN} = 5 V, lead length = 4 mm		34		mΩ
Low-side switch resistance(1)	PVIN = V_{IN} = 7 V, lead length = 4 mm		33		mΩ
Error Amplifier					
Error amplifier transconductance (g_m)(2)	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V	1000	1400	2000	µS
Error amplifier dc gain(2)	V_{SENSE} = 0.804 V		10000		V/V
Error amplifier source/sink(2)	$V_{(COMP)}$ = 1 V, 100-mV input overdrive	–250	±115	250	µA
Error amplifier output resistance			7		MΩ
Start switching threshold(2)			0.25		V
COMP to Iswitch gm(2)			22		S
Current Limit					
High-side switch current limit threshold (3)	V_{IN} = 7 V		11		A
Low-side switch sourcing current limit(3)	V_{IN} = 7 V		10		A
Low-side switch sinking current limit	V_{IN} = 7 V		3		A
Thermal Shutdown					
Thermal shutdown			170		°C
Thermal shutdown hysteresis			30		°C
Internal Switching Frequency					
Internally set frequency	RT = Open	395	500	585	kHz
Externally set frequency	RT = 100 kΩ (1%)	395	500	585	kHz
	RT = 487 kΩ (1%)	85	100	120	
	RT = 47 kΩ (1%)	900	1000	1100	
External Synchronization					

(1) Measured at pins.
(2) Ensured by design only. Not tested in production.
(3) Parameter is not tested in production.

Electrical Characteristics (continued)

T_J = –55°C to 125°C, V_{IN} = P_{VIN} = 3.0 V to 7.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNC out low-to-high rise time (10%/90%)	C_{LOAD} = 25 pF		70	111	ns
SYNC out high-to-low fall time (90%/10%)	C_{LOAD} = 25 pF		6	15.5	ns
Falling edge delay time(4)			180		°
SYNC out high level threshold	I_{OH} = 50 µA	V_{IN} - 0.3			V
SYNC out low level threshold	I_{OL} = 50 µA			600	mV
SYNC in low level threshold	PVIN = V_{IN} = 3 V			900	mV
SYNC in high level threshold	PVIN = V_{IN} = 3 V	2.45			V
SYNC in low level threshold	PVIN = V_{IN} = 7 V			900	mV
SYNC in high level threshold	PVIN = V_{IN} = 7 V	4.25			V
SYNC in frequency range(5)		100		1000	kHz
PH (PH Pin)					
Minimum on time	Measured at 10% to 90% of VIN, 25°C, I_{PH} = 2 A		190	235	ns
Slow Start and Tracking (SS/TR Pin)					
SS charge current		1.5	2.5	3	µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		30	90	mV
Power Good (PWRGD Pin)					
VSENSE threshold	V_{SENSE} falling (fault)		91		% VREF
	V_{SENSE} rising (good)		94		
	V_{SENSE} rising (fault)		109		
	V_{SENSE} falling (good)		106		
Output high leakage	V_{SENSE} = V_{REF}, $V_{(PWRGD)}$ = 5 V		30	181	nA
Output low	$I_{(PWRGD)}$ = 2 mA			0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.6	1	V
Minimum SS/TR voltage for PWRGD				1.55	V

(4) Bench verified. Not tested in production.
(5) Parameter is production tested at nominal voltage with V_{IN} = P_{VIN} = 5 V.

7.6 Typical Characteristics

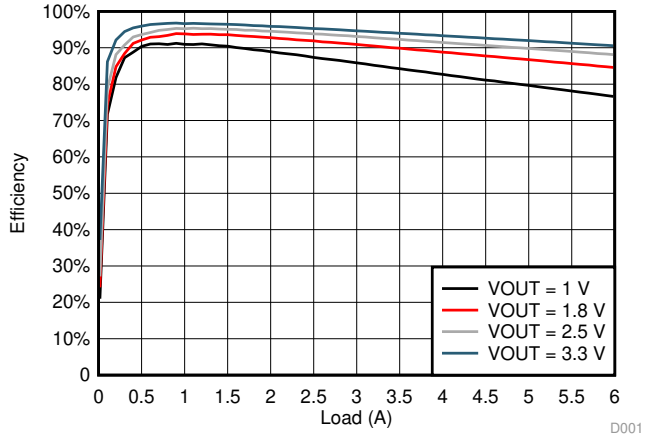


図 1. Efficiency at VIN = PVIN = 5 V

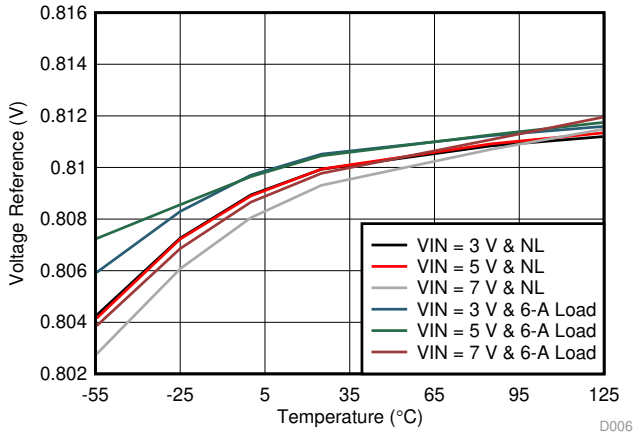


図 2. Voltage Reference vs Temperature

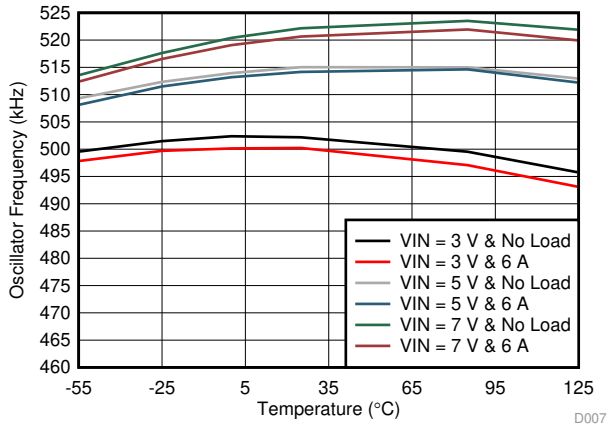


図 3. Internal Oscillator Frequency vs Temperature

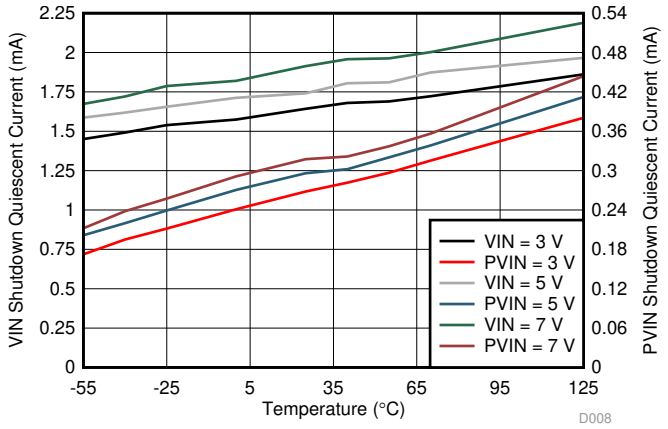


図 4. Shutdown Quiescent Current vs Temperature

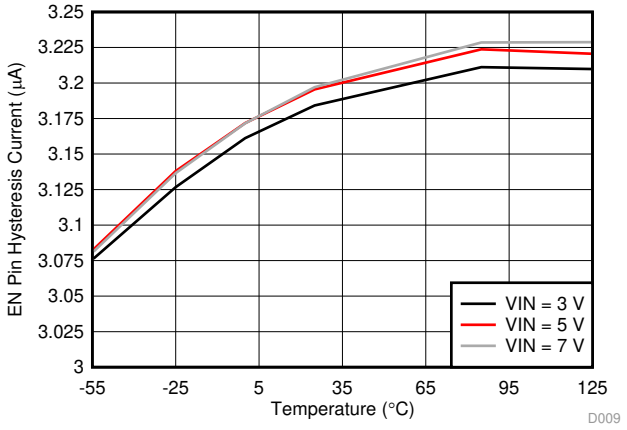


図 5. EN Pin Hysteresis Current vs Temperature

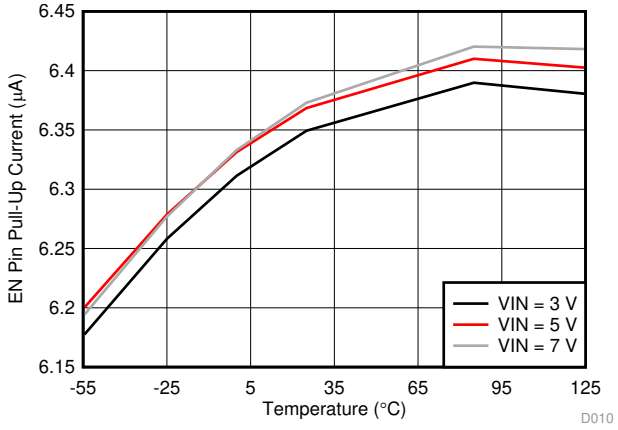


図 6. EN Pin Pull-Up Current vs Temperature

Typical Characteristics (continued)

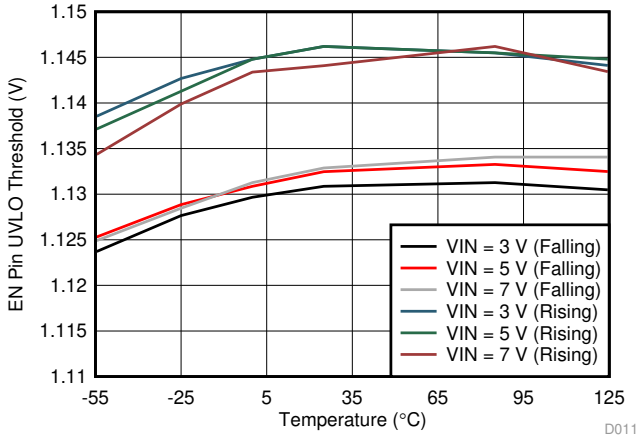


図 7. EN Pin UVLO Threshold vs Temperature

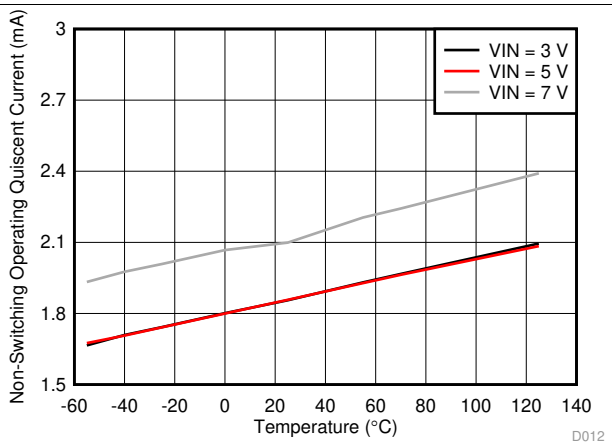


図 8. Non-Switching Operating Quiescent Current (VIN) vs Temperature

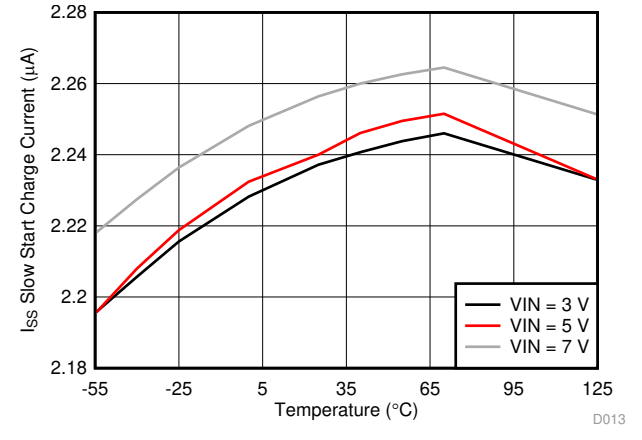


図 9. Slow Start Charge Current vs Temperature

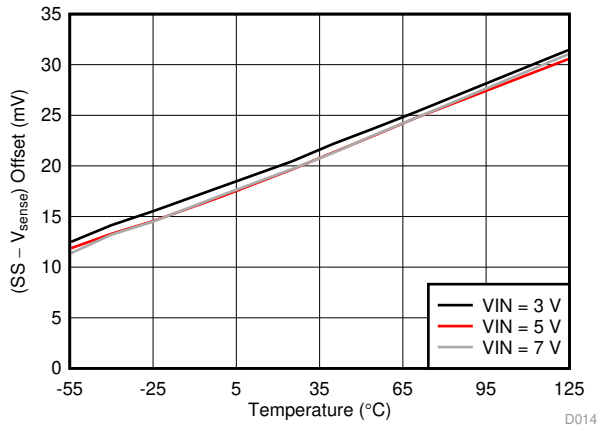


図 10. (SS-V_{SENSE}) Offset vs Temperature

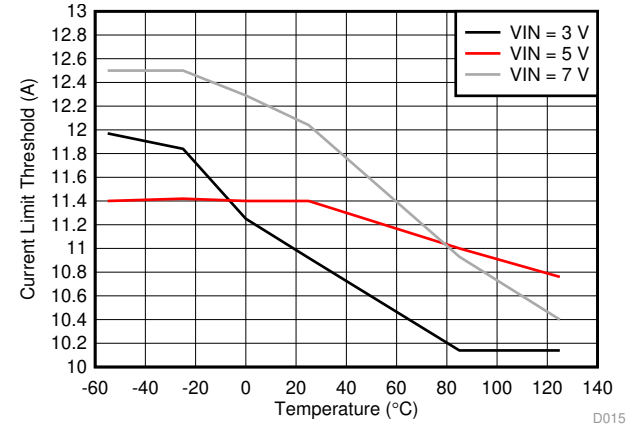


図 11. High-Side Current Limit Threshold vs Temperature

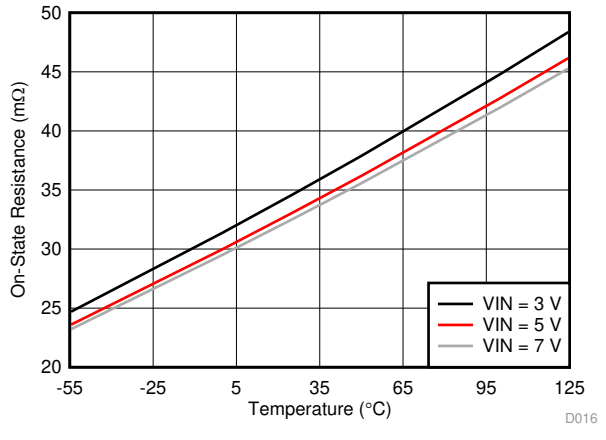


図 12. Low-Side $R_{DS(ON)}$ vs Temperature

Typical Characteristics (continued)

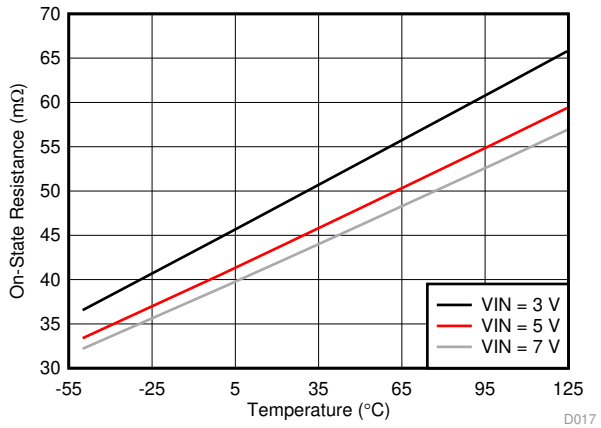


図 13. High-Side $R_{DS(ON)}$ vs Temperature

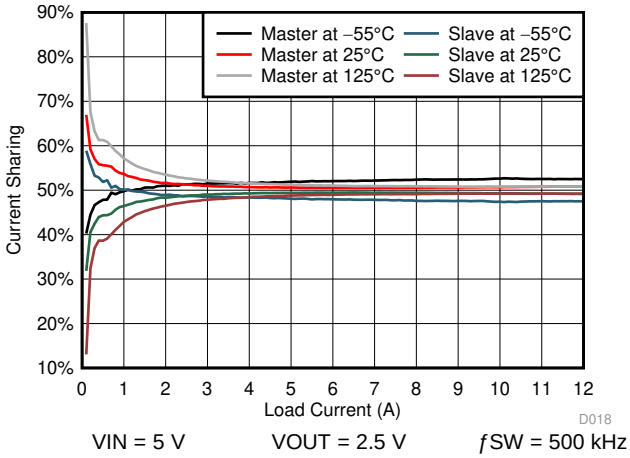


図 14. Current Sharing vs Load Current

8 Detailed Description

8.1 Overview

The device is a 7-V, 6-A synchronous step-down (buck) converter with two integrated MOSFETs, a PMOS for the high side and a NMOS for the low side. To improve performance during line and load transients, the device implements a constant frequency, peak current mode control, which also simplifies external frequency compensation. The wide switching frequency, 100 kHz to 1 MHz, allows for efficiency and size optimization when selecting the output filter components.

The device is designed for safe monotonic startup into prebiased loads. The default start up is when VIN is typically 3 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage UVLO with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. The total operating current for the device is approximately 5 mA when not switching and under no load. When the device is disabled, the supply current is typically less than 2.5 mA.

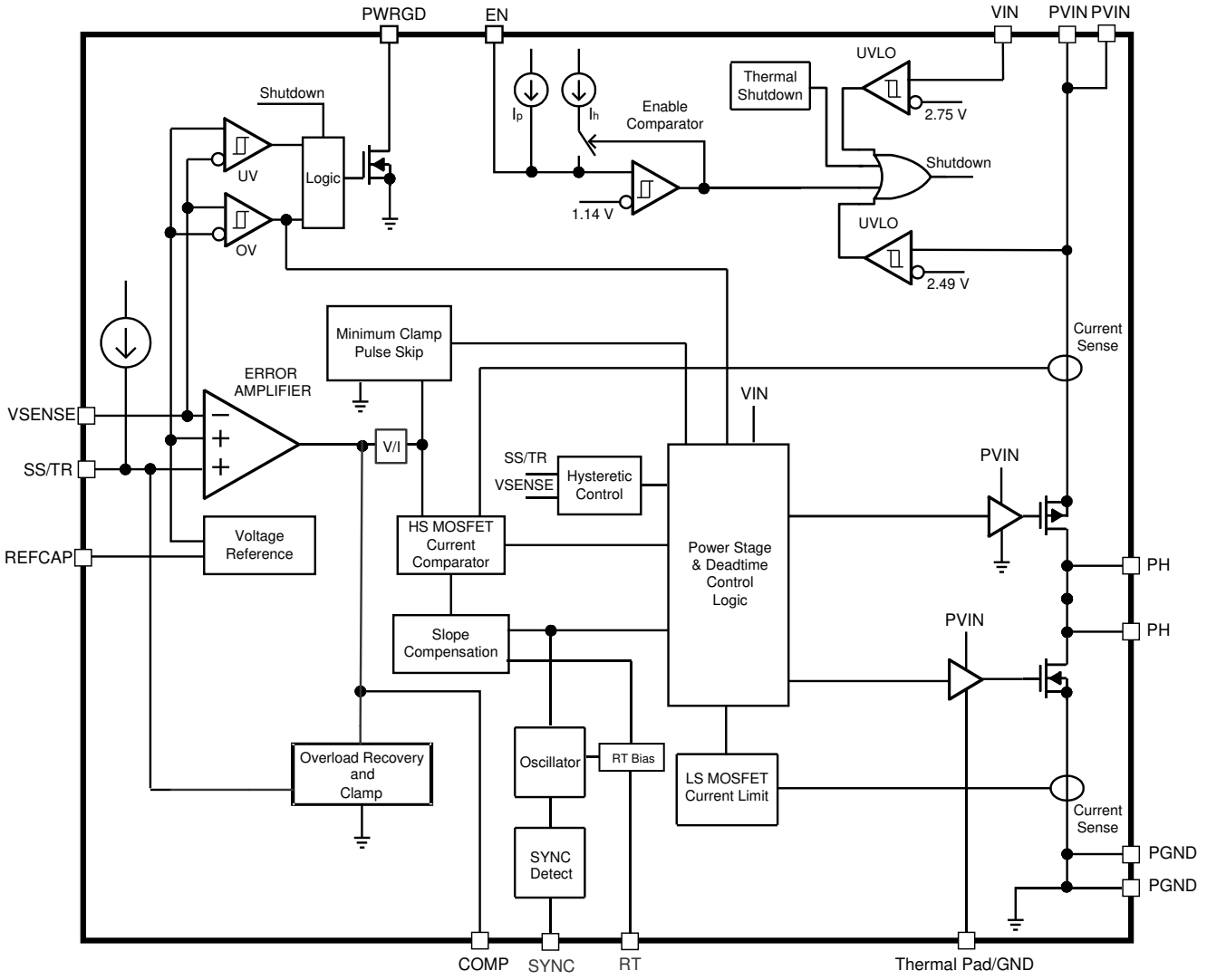
The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 6 A. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open-drain MOSFET which is pulled low when the VSENSE pin voltage is less than 91% or greater than 109% of the reference voltage VREF and asserts high when the VSENSE pin voltage is 94% to 106% of the VREF.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power-up. A small-value capacitor or resistor divider should be coupled to the pin for slow start or critical power-supply sequencing requirements.

The device is protected from output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the VREF. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections, which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow-start circuit automatically when the junction temperature drops 10°C typical below the thermal shutdown trip point.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system. Both pins have an input voltage range from 3 to 7 V. A voltage divider connected to the EN pin can adjust the input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power-up behavior.

8.3.2 Voltage Reference

The voltage reference system produces a precise voltage reference as indicated in *Electrical Characteristics*.

Feature Description (continued)

8.3.3 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. TI recommends to use 1% tolerance or better resistors. Start with a 10 kΩ for R_{TOP} and use 式 1 to calculate R_{BOTTOM}. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R_{BOTTOM} = \frac{V_{REF}}{VOUT - V_{REF}} \times R_{TOP} \quad (1)$$

where

- V_{REF} = 0.804 V

8.3.4 Safe Start-Up Into Prebiased Outputs

The device is designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased startup, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than 1.55 V.

8.3.5 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.804-V voltage reference. The transconductance of the error amplifier is 1475 μA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground. The error amplifier DC gain is typically 20,000 V/V.

8.3.6 Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents subharmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

8.3.7 Enable and Adjust UVLO

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low I_q state. The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150-mV typical.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN in split-rail applications, then the EN pin can be configured as shown in 図 15, 図 16, and 図 17. A ceramic capacitor in parallel with the bottom resistor R_2 is recommended to reduce noise on the EN pin as used in the TPS50601A-SP Evaluation Module, SLVUB65.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the EN pin crosses the enable threshold. Calculate the UVLO thresholds with 式 2 and 式 3.

Feature Description (continued)

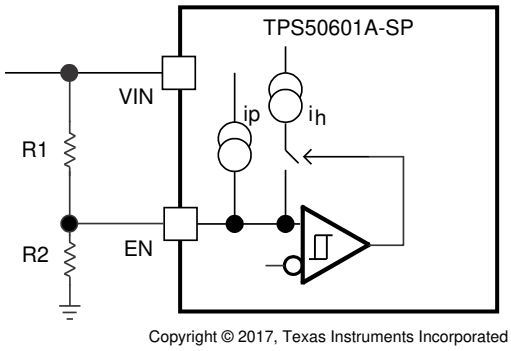


図 15. Adjustable VIN UVLO

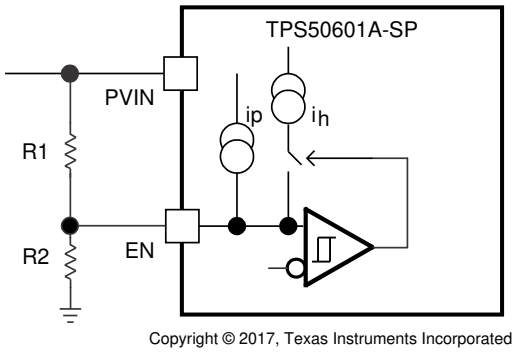


図 16. Adjustable PVIN UVLO

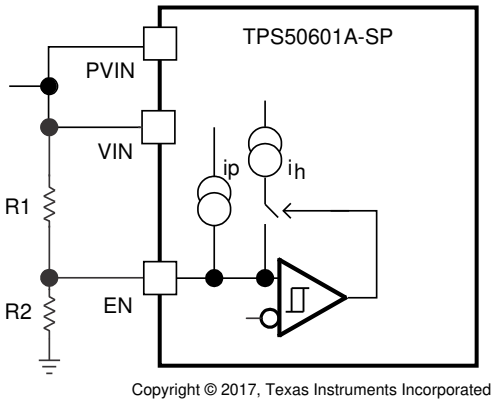


図 17. Adjustable VIN and PVIN UVLO

$$R_1 = \frac{V_{START} \times \frac{V_{ENFALLING}}{V_{ENRISING}} - V_{STOP}}{I_p \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

Feature Description (continued)

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_p + I_h)}$$

where

- I_h = 3 µA
- I_p = 6.1 µA
- $V_{ENRISING}$ = 1.14 V
- $V_{ENFALLING}$ = 1.11 V

(3)

8.3.8 Adjustable Switching Frequency and Synchronization (SYNC)

The switching frequency of the device supports three modes of operations. The modes of operation are set by the conditions on the RT and SYNC pins. At a high level, these modes can be described as master, internal oscillator, and external synchronization modes.

In master mode, the RT pin should be left floating; the internal oscillator is set to 500 kHz, and the SYNC pin is set as an output clock. The SYNC output is in phase with respect to the internal oscillator. SYNC out signal level is the same as V_{IN} level with 50% duty cycle. SYNC signal feeding the slave module, which is in phase with the master clock, gets internally inverted (180° out of phase with the master clock) internally in the slave module.

In internal oscillator mode, a resistor is connected between the RT pin and GND. The SYNC pin requires a 10-kΩ resistor to GND for this mode to be effective. The switching frequency of the device is adjustable from 100 kHz to 1 MHz by placing a maximum of 510 kΩ and a minimum of 47 kΩ respectively. To determine the RT resistance for a given switching frequency, use 式 4 or the curve in 図 18. To reduce the solution size, the designer should set switching frequency as high as possible, but consider the tradeoffs of supply efficiency and minimum controllable on-time.

$$RT(F_{SW}) = 67009 \times F_{SW}^{-1.0549}$$

where

- RT in kΩ
- f_{SW} in kHz

(4)

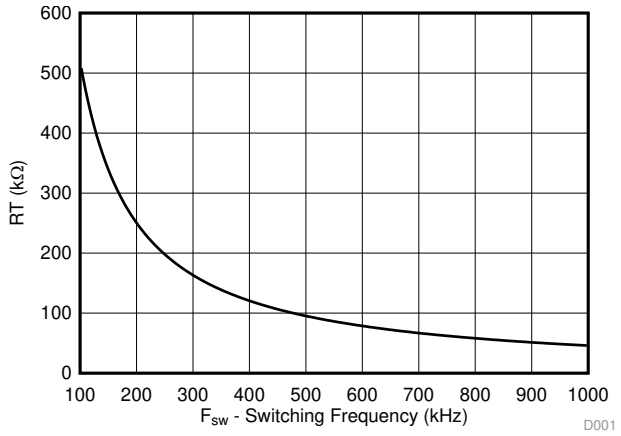


図 18. RT vs Switching Frequency

When operating the converter in internal oscillator mode (internal oscillator determines the switching frequency (500 kHz) default), the synchronous pin becomes the output and there is a phase inversion. When trying to parallel with another converter, the RT pin of the second (slave) converter must have its RT pin populated such that the converter frequency of the slave converter must be within ±5% of the master converter. This is required because the RT pin also sets the proper operation of slope compensation.

Feature Description (continued)

In external synchronization mode, a resistor is connected between the RT pin and GND. The SYNC pin requires a toggling signal for this mode to be effective. The switching frequency of the device goes 1:1 with that of SYNC pin. External system clock-user supplied sync clock signal determines the switching frequency. If no external clock signal is detected for 20 µs, then TPS50601A-SP transitions to its internal clock, which is typically 500 kHz. An external synchronization using an inverter to obtain phase inversion is necessary. RT values of the master and slave converter must be within ±5% of the external synchronization frequency. This is necessary for proper slope compensation. A resistance in the RT pin is required for proper operation of the slope compensation circuit. To determine the RT resistance for a given switching frequency, use 式 4 or the curve in 図 18.

These modes are described in 表 3.

表 3. Switching Frequency, SYNC and RT Pin Usage Table

RT PIN	SYNC PIN	SWITCHING FREQUENCY	DESCRIPTION AND NOTES
Float	Generates an output signal	500 kHz	SYNC pin behaves as an output. SYNC output signal is 180° in phase to the internal 500-kHz switching frequency.
47-kΩ to 510-kΩ resistor to AGND	10-kΩ resistor to GND	100 kHz to 1 MHz	Internally generated switching frequency is based upon the resistor value present at the RT pin.
	User-supplied sync clock or TPS50601A-SP master device sync output	Internally synchronized to external clock	Set value of RT that corresponds to the externally supplied sync frequency.

8.3.9 Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. 式 5 shows the calculations for the slow-start time (t_{SS}, 10% to 90%) and slow-start capacitor (C_{SS}). The voltage reference (VREF) is 0.804 V and the slow-start charge current (I_{SS}) is 2 µA.

$$t_{SS}\,(ms) = \frac{C_{SS}\,(nF) \times V_{REF}\,(V)}{I_{SS}\,(\mu A)} \tag{5}$$

When any of the following 3 scenarios occur; the input UVLO is triggered, the EN pin is pulled below 1.05 V, or a thermal shutdown event occurs; the device stops switching and enters low current operation. At the subsequent power-up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

8.3.10 Power Good (PWRGD)

The PWRGD pin is an open-drain output. When the VSENSE pin is between 94% and 106% of the internal voltage reference, the PWRGD pin pull-down is deasserted and the pin floats. TI recommends to use a pullup resistor between 10 kΩ to 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state when the VIN input voltage is greater than 1 V but has reduced current sinking capability. The PWRGD achieves full current sinking capability when the VIN input voltage is above 3 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS/TR pin is below 1.55 V.

8.3.11 Sequencing (SS/TR)

Many of the common power-supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins.

The sequential method is shown in 図 19 using two TPS50601A-SP devices. The power good of the first device is coupled to the EN pin of the second device, which enables the second power supply after the primary supply reaches regulation.

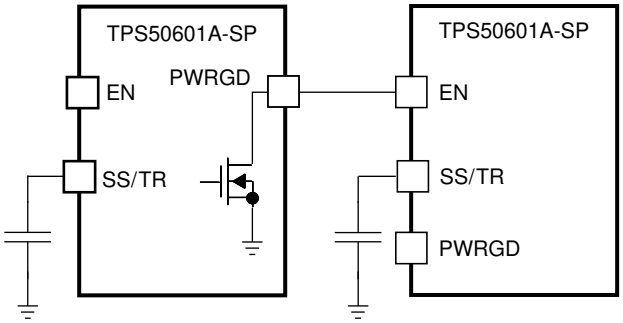


図 19. Sequential Start-Up Sequence

図 20 shows the method implementing ratiometric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup current source must be doubled in 式 5.

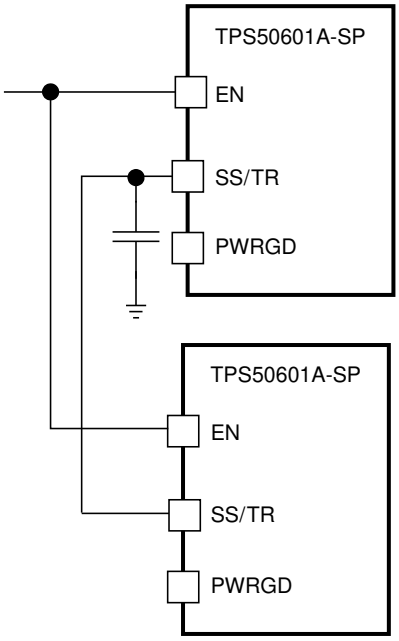


図 20. Ratiometric Start-Up Sequence

Ratiometric and simultaneous power-supply sequencing can be implemented by connecting the resistor network of R_1 and R_2 (shown in 図 21) to the output of the power supply that needs to be tracked or another voltage reference source. Using 式 6 and 式 7, the tracking resistors can be calculated to initiate the $VOUT_2$ slightly before, after, or at the same time as $VOUT_1$. 式 8 is the voltage difference between $VOUT_1$ and $VOUT_2$.

To design a ratiometric start-up in which the $VOUT_2$ voltage is slightly greater than the $VOUT_1$ voltage when $VOUT_2$ reaches regulation, use a negative number in 式 6 and 式 7 for ΔV. 式 8 results in a positive number for applications where the $VOUT_2$ is slightly lower than $VOUT_1$ when $VOUT_2$ regulation is achieved.

The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ($V_{SS\text{-}OFFSET}$, 30 mV) in the slow-start circuit and the offset created by the pullup current source (I_{SS} = 2 μA) and tracking resistors, the $V_{SS\text{-}OFFSET}$ and I_{SS} are included as variables in the equations.

To ensure proper operation of the device, the calculated R_1 value from 式 6 must be greater than the value calculated in 式 9.

$$R_1 = \frac{VOUT_2 + \Delta V}{V_{REF}} \times \frac{V_{SS-OFFSET}}{I_{SS}} \quad (6)$$

$$R_2 = \frac{V_{REF} \times R_1}{VOUT_2 + \Delta V - V_{REF}} \quad (7)$$

$$\Delta V = VOUT_1 - VOUT_2 \quad (8)$$

$$R_1 > 2800 \times VOUT_1 - 180 \times \Delta V \quad (9)$$

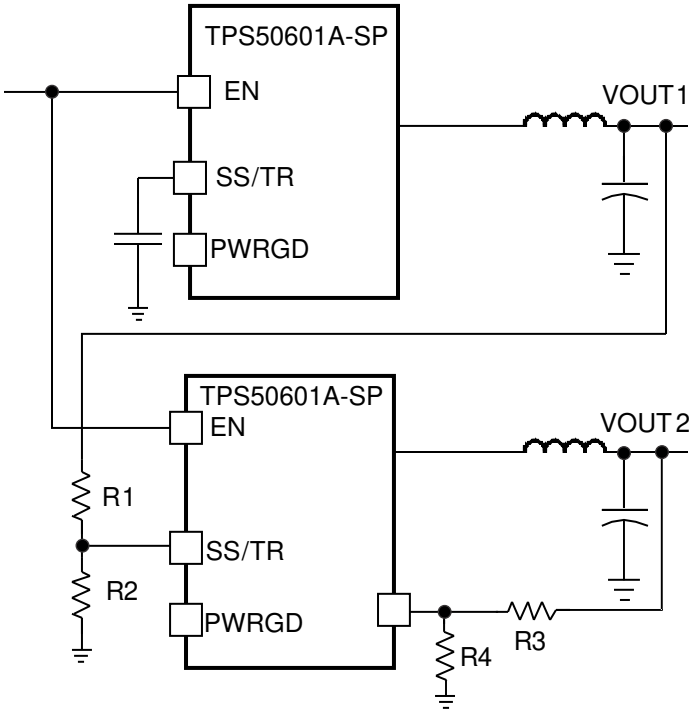


図 21. Ratiometric and Simultaneous Start-Up Sequence

8.3.12 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.13 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and low-side MOSFET.

8.3.13.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

8.3.13.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

When the low-side MOSFET turns off, the switch node increases and forward biases the high-side MOSFET parallel diode (the high-side MOSFET is still off at this stage).

8.3.14 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 165°C (typical).

8.3.15 Turn-On Behavior

Minimum on-time specification determines the maximum operating frequency of the design. As the unit starts up and goes through its soft-start process, the required duty-cycle is less than the minimum controllable on-time. This can cause the converter to skip pulses. Thus, instantaneous output pulses can be higher or lower than the desired voltage. This behavior is only evident when operating at high frequency with high bandwidth. When the minimum on-pulse is greater than the minimum controllable on-time, the turn-on behavior is normal.

8.3.16 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits shown in 図 22. In Type 2A, one additional high-frequency pole is added to attenuate high-frequency noise.

The following design guidelines are provided for advanced users who prefer to compensate using the general method. The step-by-step design procedure described in *Detailed Design Procedure* may also be used.

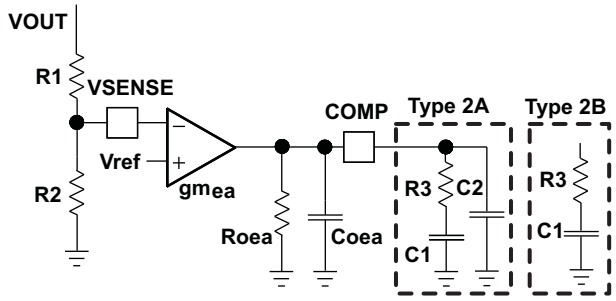


図 22. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency f_{co}. A good starting point is one-tenth of the switching frequency, f_{SW}.
2. R_3 can be determined by:

$$R_3 = \frac{2\pi \times f_{co} \times V_{OUT} \times C_{OUT}}{gm_{ea} \times Vref \times gm_{ps}} \quad (10)$$

where gm_{ea} is the gm of the error amplifier (1400 μS), gm_{ps} is the gm of the power stage (22 S) and VREF is the reference voltage (0.804 V).

3. Place a compensation zero at the dominant pole $f_p = \frac{1}{C_{OUT} \times R_L \times 2\pi}$ using C_1 and R_3.
   C_1 can be determined by
   $$C_1 = \frac{C_{OUT} \times R_L}{R_3} \quad (11)$$
4. C_2 is optional. It can be used to cancel the zero from the equivalent series resistance (ESR) of the output capacitor C_{OUT}.
   $$C_2 = \frac{C_{OUT} \times R_{ESR}}{R_3} \quad (12)$$

8.4 Device Functional Modes

8.4.1 Fixed-Frequency PWM Control

The device uses fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

8.4.2 Continuous Current Mode (CCM) Operation

As a synchronous buck converter, the device normally works in CCM under all load conditions.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS50601A-SP device is a highly-integrated synchronous step-down DC-DC converter. The device is used to convert a higher DC-DC input voltage to a lower DC output voltage with a maximum output current of 6 A.

The TPS50601A-SP user's guide is available on the TI website, SLVUB65. The guide highlights standard EVM test results, schematic, and BOM for reference.

9.2 Typical Application

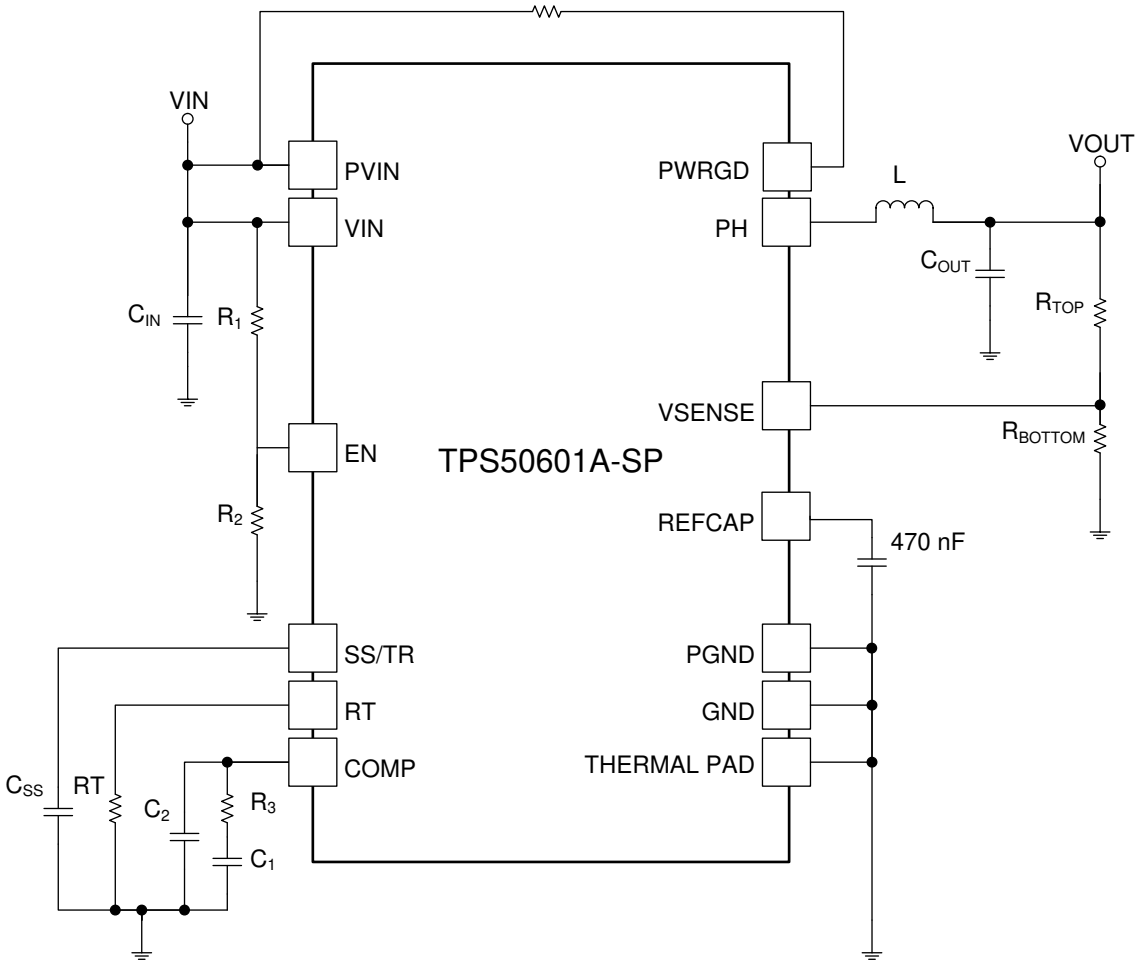


図 23. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

This example highlights a design using the TPS50601A-SP based on its evaluation module. For more details, please refer to the EVM user's guide, SLVUB65. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

表 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	2.5 V
Maximum output current	6 A
Transient response 1-A load step	ΔVOUT = 5%
Input voltage	5-V nominal, 4.5 V to 7 V
Output voltage ripple	20 mVp-p
Start input voltage (rising V_{IN})	4.5 V
Stop input voltage (falling V_{IN})	4.3 V
Switching frequency	100 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance. In this design, a switching frequency of 100 kHz is selected. Based on 図 18, the RT value is set to a standard value of 487 kΩ.

9.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, use 式 13. K_L is a coefficient that represents the amount of inductor ripple current relative to the maximum output current, I_O. The inductor ripple current is filtered by the output capacitor therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer depending on specific system needs. Typical values for K_L range from 0.1 to 0.5. For low output currents, the value of K_L could be increased to reduce the value of the output inductor.

$$L = \frac{V_{INMAX} - VOUT}{I_O \times K_L} \times \frac{VOUT}{V_{INMAX} \times f_{SW}} \quad (13)$$

For this design example, use K_L = 0.45 and the inductor value is calculated to be 4.7 µH for nominal VIN = 5 V.

9.2.2.3 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. 式 14 shows the minimum output capacitance, from the electrical point of view, necessary to accomplish this.

$$C_{OUT} > \frac{2 \times I_O}{f_{SW} \times \Delta VOUT} \quad (14)$$

Where ΔI_O is the change in output current, f_{SW} is the regulator switching frequency and ΔVOUT is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in VOUT for a load step of 1 A. For this example, ΔI_O = 1 A and ΔVOUT = 0.05 × 2.5 = 0.125 V. Using these numbers gives a minimum capacitance of 160 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. However, for space applications and large capacitance values, tantalum capacitors are typically used which have a certain ESR value to take into consideration.

式 15 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, $VOUT_{ripple}$ is the maximum allowable output voltage ripple, and I_{ripple} is the inductor ripple current. In this case, the maximum output voltage ripple is 20 mV. Under this requirement, 式 15 yields 168.75 µF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{I_{ripple}}{VOUT_{ripple}} \quad (15)$$

式 16 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. 式 16 indicates the ESR should be less than 7.41 mΩ.

$$R_{ESR} < \frac{VOUT_{ripple}}{I_{ripple}} \quad (16)$$

For this specific design, taking into consideration the stringent requirements for space applications, an output capacitor of 330 µF with ESR = 6 mΩ has been selected.

9.2.2.4 Slow Start Capacitor Selection

The slow start capacitor C_{SS}, determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS50601A-SP reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using 式 5. The example circuit has the soft start time set to an arbitrary value of about 4 ms which requires a 10-nF capacitor. In TPS50601A-SP, I_{SS} is 2-µA typical, and V_{REF} is 0.804 V.

9.2.2.5 Undervoltage Lockout (UVLO) Set Point

The UVLO can be adjusted using the external voltage divider network formed by R_1 and R_2. R_1 is connected between VIN and the EN pin of the TPS50601A-SP and R_2 is connected between EN and GND. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above selected voltage (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below (UVLO stop or disable) voltage. 式 2 and 式 3 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified in 表 4, the nearest standard resistor value for R_1 is 10 kΩ and for R_2 is 3.4 kΩ.

9.2.2.6 Output Voltage Feedback Resistor Selection

The resistor divider network R_{TOP} and R_{BOTTOM} is used to set the output voltage. For the example design, 10 kΩ was selected for R_{TOP}. Using 式 1, R_{BOTTOM} is calculated as 4.77 kΩ. The nearest standard 1% resistor is 4.7 kΩ.

9.2.2.7 Compensation Component Selection

There are several industry techniques used to compensate DC-DC regulators. For this design, type 2B compensation is used as shown in Small Signal Model for Frequency Compensation.

First, the modulator pole, f_{pmod}, and the R_{ESR} zero, f_{zmod} must be calculated using 式 17 and 式 18. Use 式 19 and 式 20 to estimate a starting point for the closed loop crossover frequency f_{co}, then the required compensation components may be derived. For this design example, f_{pmod} is 1.16 kHz and f_{zmod} is 80.38 kHz. 式 19 is the geometric mean of the modulator pole and the ESR zero and 式 20 is the geometric mean of the modulator pole and one half the switching frequency. Use a frequency near the lower of these two values as the intended crossover frequency f_{co}. In this case 式 19 yields 9.65 kHz and 式 20 yields 7.61 kHz. A frequency of 7.6 kHz is chosen as the intended crossover frequency.

$$f_{pmod} = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}} \tag{17}$$

$$f_{zmod} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{18}$$

$$f_{co} = \sqrt{f_{pmod} \times f_{zmod}} \tag{19}$$

$$f_{co} = \sqrt{f_{pmod} \times \frac{f_{SW}}{2}} \tag{20}$$

Now the compensation components can be calculated using 式 10 and 式 11. The standard values for R_3 and C_1 are 1.6 kΩ and 82 nF, respectively.

9.2.3 Parallel Operation

The TPS50601A-SP can be configured in master-slave mode to provide 12-A output current as shown in 図 24.

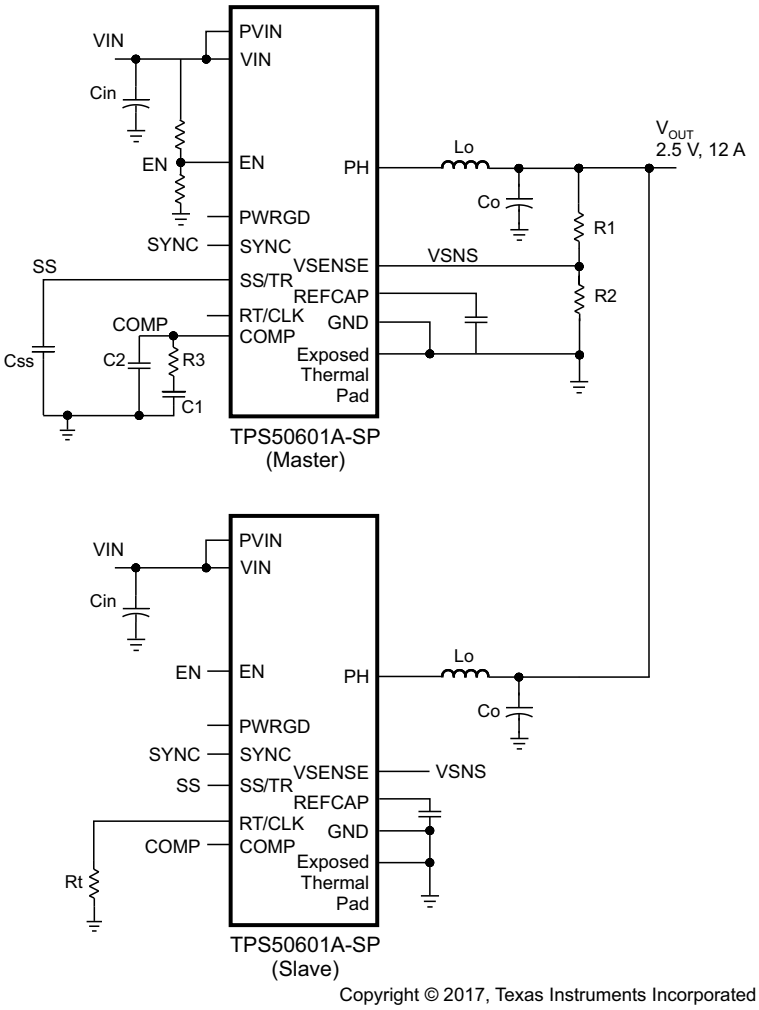


図 24. Parallel Configuration Showing Master and Slave

The design procedure to configure the master-slave operation using the internal oscillator is as follows:

- The RT pin of the master device must be left floating. This achieves 2 purposes, to set the frequency to 500 kHz (typical) using the internal oscillator and to configure the SYNC pin of the master device as an output pin with a 500-kHz clock, 180° in phase respect to the internal oscillator of the master device. For more details, see *Adjustable Switching Frequency and Synchronization (SYNC)* section.
- The RT pin on slave device should be connected to a resistor such that the frequency of the slave device is within 5% of the master's frequency, 500 kHz in this case. See 図 18 for reference.
- SYNC pin of the master device must be connected to the SYNC pin of the slave device.
- Only a single feedback network is needed connected to the VSENSE pin of the master device. Therefore, both VSENSE pins must be connected.
- Only a single compensation network is needed connected to the COMP pin of the master device. Therefore both COMP pins must be connected.
- Only a single soft start capacitor is needed connected to the SS pin of the master device. Therefore both SS pins must be connected.
- Only a single enable signal (or resistor divider) is needed connected to the EN pin of the master device. Therefore, both EN pins must be connected.
- Since the master device controls the compensation, soft start and enable networks, the factor of 2 must be

taken into account when calculating the components associated with these pins.

The master-slave mode can also be implemented using an external clock. In such case, a different frequency other than 500 kHz can be used. When using an external clock, only the RT and SYNC pins configuration varies as follows:

- RT pins of both master and slave device must be connected to a resistor matching the frequency of the external clock being used. See 図 18 for reference.
- The external clock is connected to the SYNC pin of the master device. A 10-kΩ resistor to GND should be connected to the SYNC pin as well.
- An inverted clock (180° in phase respect to the master device) must be connected to the SYNC pin of the slave device. A 10-kΩ resistor to GND should be connected to the SYNC pin as well.

9.2.4 Application Curve

The evaluation module for the TPS50601A-SP was used to capture a load step response of the device. The testing conditions were:

- VIN = PVIN = 5 V
- VOUT = 2.5 V
- Load step = 0 A to 5 A
- Switching frequency = 100 kHz

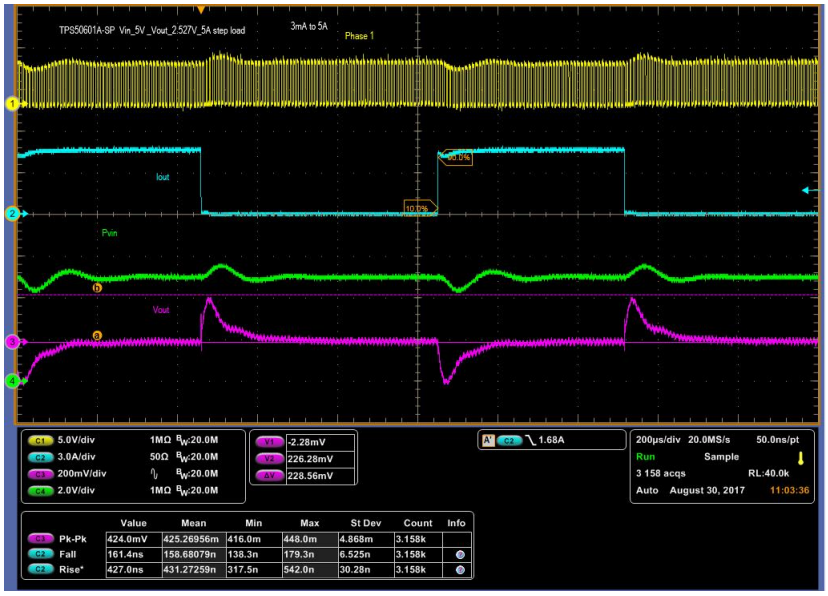


図 25. 5-A Step Response for 100-kHz Switching Operation

10 Power Supply Recommendations

The TPS50601A-SP is designed to operate from an input voltage supply range between 3 V and 7 V. This supply voltage must be well regulated and proper local bypass capacitors should be used for proper electrical performance from PVIN to GND and from VIN to GND. Due to stringent requirements for space applications, typically additional input bypass capacitors are used. The TPS50601A-SP Evaluation Module uses 6, 22-µF ceramic capacitors from PVIN to GND and a 4.7 µF and a 0.1 µF from VIN to GND.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. Standard good practices should be applied. Some basic guidelines follow:

- The top layer contains the main power traces for PVIN, VIN, VOUT, and PHASE. Also on the top layer are connections for the remaining pins of the TPS50601A-SP and a large top side area filled with ground.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor and the output filter capacitor.
- Thermal pad can be electrically floating or connected externally. If electrically connected externally then it must be connected to GND. Customer should evaluate their system performance when thermal pad is electrically isolated and thermally conductive.
- Preferred approach is that GND pin should be tied directly to the power pad under the IC and the PGND.
- The PVIN and VIN pins should be bypassed to ground with ceramic capacitors placed as close as possible to the pins.
- Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The RT, REFCAP and COMP pins are sensitive to noise so the respective components should be located as close as possible to the IC and routed with minimal lengths of trace.
- The feedback voltage signal VSENSE should be routed away from the switching node.

11.2 Layout Example

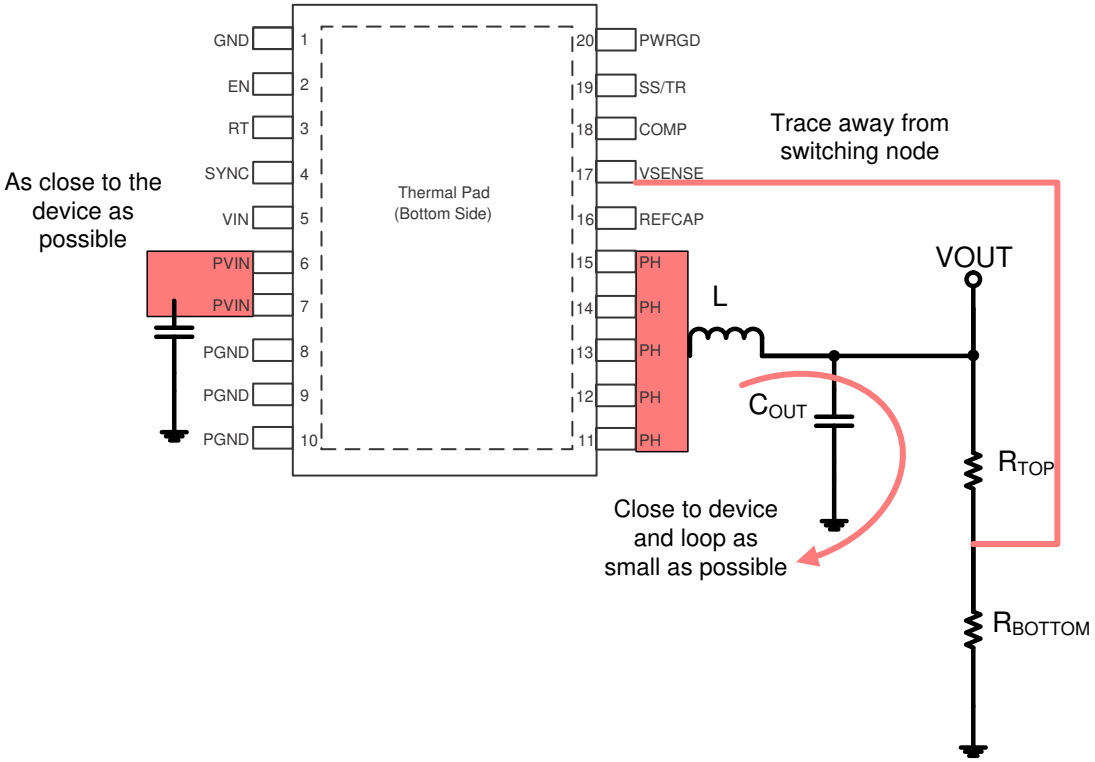


図 26. PCB Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

TPS50601ASPEVM 6Aレギュレータ評価基板

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-1022102VSC	Active	Production	CFP (HKH) | 20	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962-1022102VS C TPS50601AMHKHV
5962R1022102V9A	Active	Production	XCEPT (KGD) | 0	25 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R1022102VSC	Active	Production	CFP (HKH) | 20	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962R1022102VS C TPS50601AMHKHV
TPS50601AHKH/EM	Active	Production	CFP (HKH) | 20	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	25 to 25	TPS50601AHKH/EM EVAL ONLY
TPS50601AY/EM	Active	Production	XCEPT (KGD) | 0	5 | OTHER	Yes	Call TI	N/A for Pkg Type	25 to 25	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

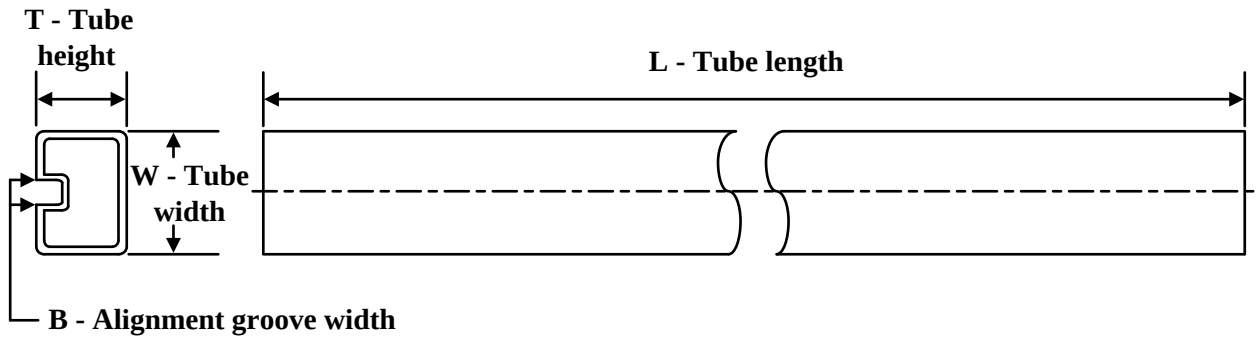
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

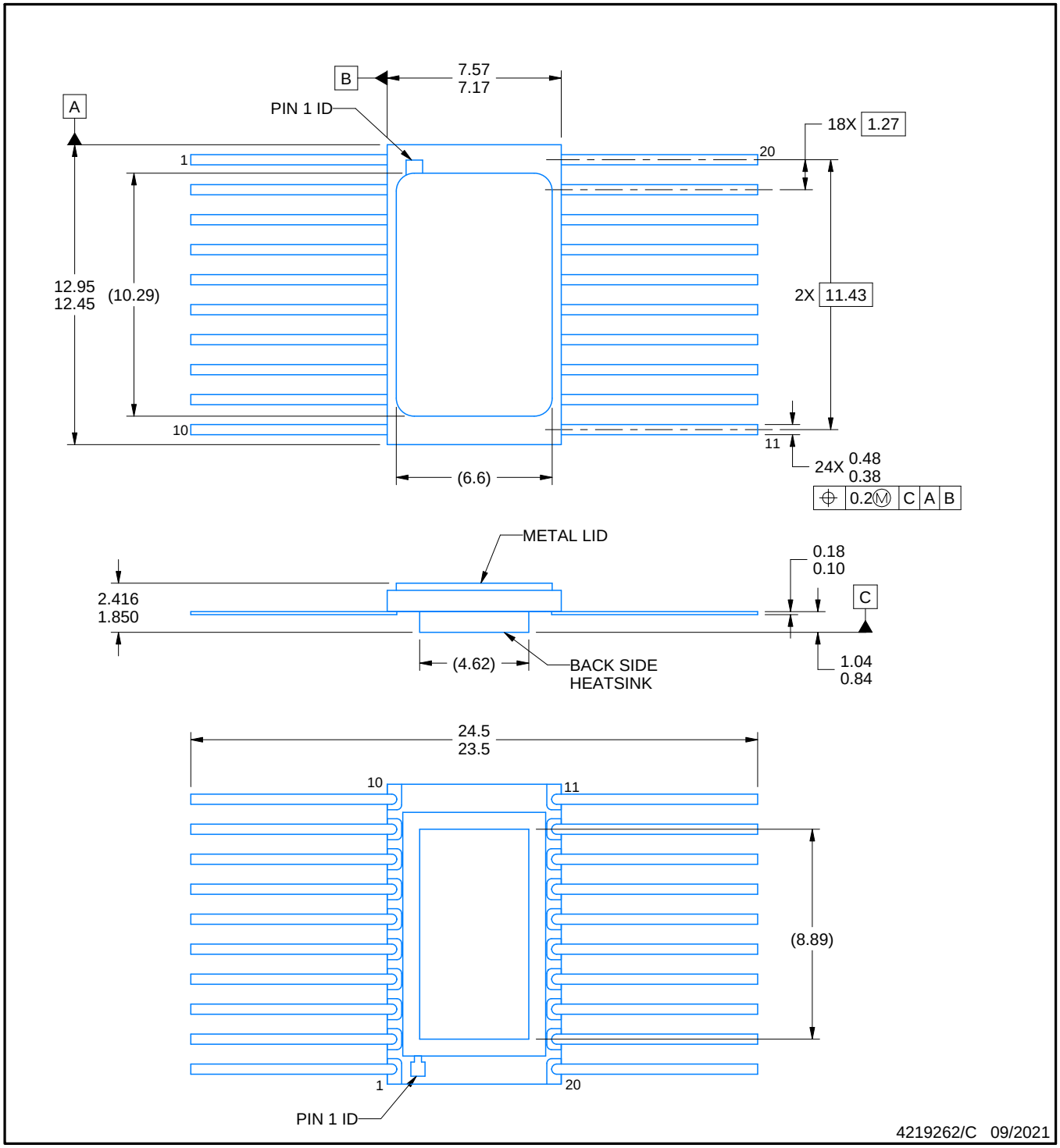
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1022102VSC	HKH	CFP	20	25	506.98	26.16	6220	NA
5962R1022102VSC	HKH	CFP	20	25	506.98	26.16	6220	NA
TPS50601AHKH/EM	HKH	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKH0020A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



NOTES:

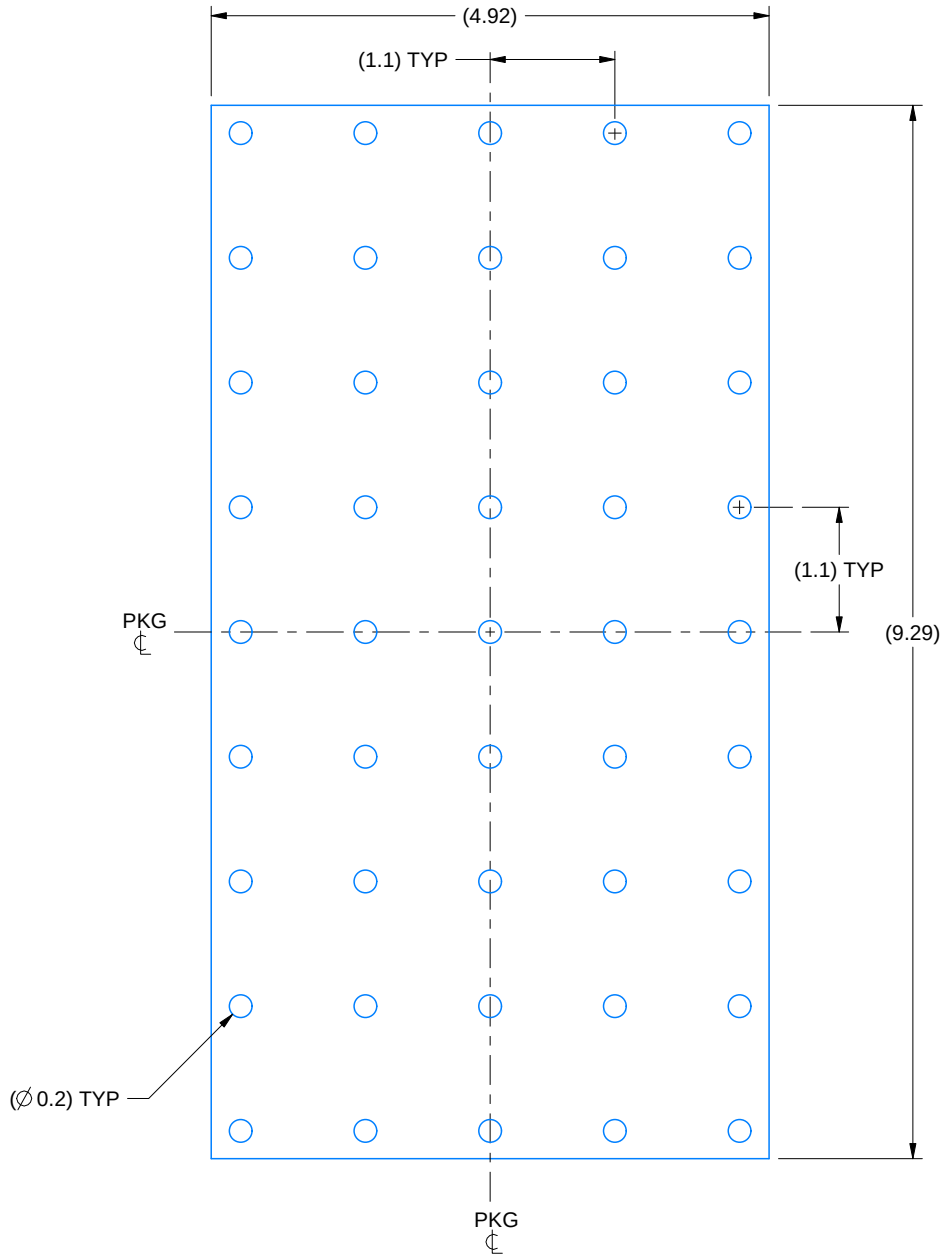
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.

EXAMPLE BOARD LAYOUT

HKH0020A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SCALE	SIZE		REV	PAGE
3X	A	4219262	C	3 OF 4

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月