

## TPS53311 3A スイッチャ内蔵降圧型レギュレータ

### 1 特長

- 最高95.5%の効率
- 3Aの連続出力電流
- すべてのMLCC出力コンデンサをサポート
- SmoothPWM™自動スキップ Eco-mode™によって軽負荷時の効率を向上
- 電圧モード制御
- マスタ/スレーブのインターリーブ動作をサポート
- 公称周波数の±20%まで同期
- 2.9V～6Vの電圧変換範囲
- ディセーブル時のソフトストップ出力放電
- 可変出力電圧範囲:  
0.6V～0.84V×V<sub>IN</sub>
- 過電流、過電圧、過熱保護
- 小型の3mm×3mm、16ピンVQFNパッケージ
- オープン・ドレインのパワー・グッド・インジケータ
- 内部ブートストラップ・スイッチ
- 低いR<sub>DS(on)</sub>、3.3V入力で24mΩ、5V入力で19mΩ
- プリバイアス・スタートアップ機能をサポート

### 2 アプリケーション

- 5V降圧レール
- 3.3V降圧レール

### 3 概要

TPS53311を使用すると、完全に統合された3V～5V V<sub>IN</sub>の統合同期FETコンバータ・ソリューションを実現でき、200mm<sup>2</sup>のPCB領域に合計16個の部品を搭載できます。低いR<sub>DS(on)</sub>とTI独自のSmoothPWM™スキップ・モード動作により、95.5%のピーク効率、100mAの軽負荷で90%超の効率を得られます。22μFセラミック出力コンデンサを2つ使用するだけで、電力密度の高い3Aソリューションを構築できます。

TPS53311は、1.1MHzのスイッチング周波数、SKIPモード動作のサポート、プリバイアスのスタートアップ、内部ソフトスタート、出力ソフト放電、内部VBSTスイッチ、パワー・グッド、EN/入力UVLO、過電流、過電圧、低電圧、過熱保護の機能があり、すべてのセラミック出力コンデンサをサポートしています。2.9V～3.5Vの電源電圧と、2.9V～6Vの変換電圧に対応し、出力電圧は0.6V～0.84V×V<sub>IN</sub>の範囲で調整可能です。

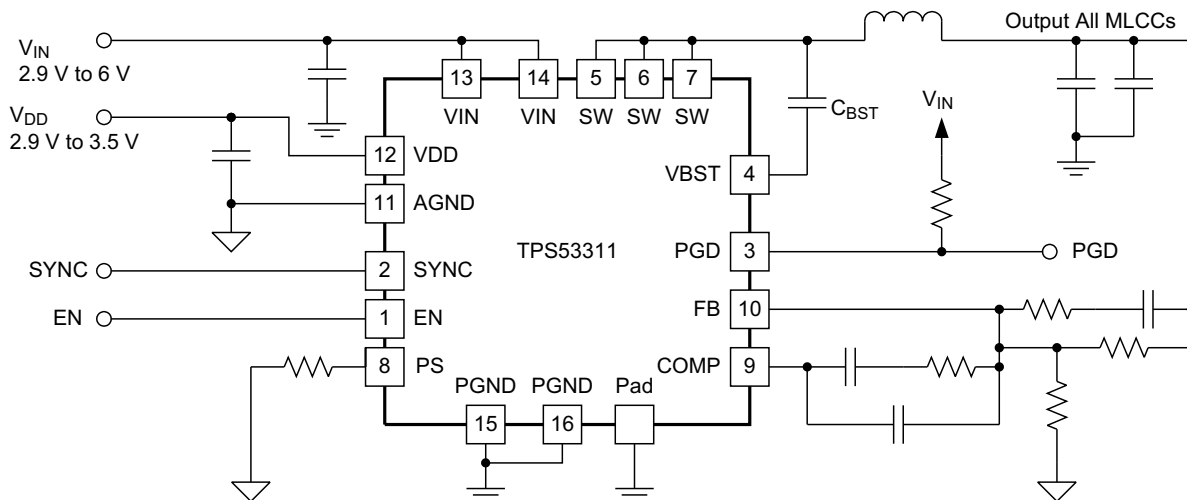
TPS53311は3mm×3mmの16ピンVQFNパッケージ (Green RoHs準拠、鉛フリー)で供給され、-40℃～85℃で動作します。

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
TPS53311	VQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

#### 代表的なアプリケーション回路



Copyright © 2016, Texas Instruments Incorporated



## 目次

1	特長	1	7.4	Device Functional Modes	11
2	アプリケーション	1	8	<b>Application and Implementation</b>	13
3	概要	1	8.1	Application Information	13
4	改訂履歴	2	8.2	Typical Application	13
5	<b>Pin Configuration and Functions</b>	3	9	<b>Power Supply Recommendations</b>	19
6	<b>Specifications</b>	4	10	<b>Layout</b>	19
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	19
6.2	ESD Ratings	4	10.2	Layout Example	19
6.3	Recommended Operating Conditions	4	11	デバイスおよびドキュメントのサポート	20
6.4	Thermal Information	5	11.1	ドキュメントのサポート	20
6.5	Electrical Characteristics	5	11.2	ドキュメントの更新通知を受け取る方法	20
6.6	Typical Characteristics	7	11.3	コミュニティ・リソース	20
7	<b>Detailed Description</b>	9	11.4	商標	20
7.1	Overview	9	11.5	静電気放電に関する注意事項	20
7.2	Functional Block Diagram	9	11.6	Glossary	20
7.3	Feature Description	9	12	メカニカル、パッケージ、および注文情報	20

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Revision A (March 2011) から Revision B に変更

Page

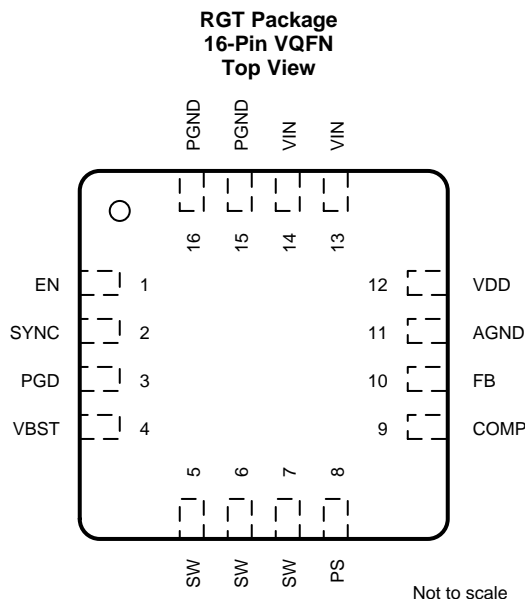
• 「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• データシートの末尾にあるPOAを参照し、「注文情報」表を削除	1
• Added <i>Thermal Information</i> table	5
• Deleted <i>Package Dissipation Ratings</i> table	5
• Changed value of component R2 in <i>Typical Application Circuit Diagram</i> From: 4.02 kΩ To: 2.67 kΩ	13
• Changed value of component V <sub>OUT</sub> on TPS53311 Master in <i>Master and Slave Configuration Schematic</i> From: 1.2 V To: 1.5 V	17
• Changed value of component R2 on TPS53311 Master in <i>Master and Slave Configuration Schematic</i> From: 4.02 kΩ To: 2.67 kΩ	17
• Changed value of component V <sub>OUT</sub> on TPS53311 Slave in <i>Master and Slave Configuration Schematic</i> From: 1.5 V To: 1.2 V	17
• Changed value of component R12 on TPS53311 Slave in <i>Master and Slave Configuration Schematic</i> From: 2.67 kΩ To: 4.02 kΩ	17

### 2010年6月発行のものから更新

Page

• 「特長」の箇条書き 追加	1
• 「概要」を明確化のため 変更	1
• Changed <i>Absolute Maximum Ratings</i> output voltage (SW pin DC) minimum from 0.3 V to –1 V (typographical error)	4
• Added information regarding DE mode in <i>Master/Slave Operation and Synchronization</i> section	11
• Changed value of component C2 in <i>Typical Application Circuit Diagram</i> to 2.2 nF (typographical error)	13
• Changed component labels and values in <i>Master/Slave Configuration Schematic</i> (typographical error)	17

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	EN	I	Enable. Internally pulled up to VDD with a 1.35-M $\Omega$ resistor.
2	SYNC	B	Synchronization signal for input interleaving. Master SYNC pin sends out 180° out-of-phase signal to slave SYNC. SYNC frequency must be within $\pm 20\%$ of slave nominal frequency.
3	PGD	O	Power good output flag. Open drain output. Pull up to an external rail through a resistor.
4	VBST	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
5	SW	B	Output inductor connection to integrated power devices.
6	SW	B	Output inductor connection to integrated power devices.
7	SW	B	Output inductor connection to integrated power devices.
8	PS	I	Mode configuration pin (with 10 $\mu$ A current): Connecting to ground: Forced CCM slave. Pulled high or floating (internal pulled high): Forced CCM master. Connect with 24.3 k $\Omega$ to GND: DE slave. Connect with 57.6 k $\Omega$ to GND: HEF mode. Connect with 105 k $\Omega$ to GND: reserved mode. Connect with 174 k $\Omega$ to GND: DE master.
9	COMP	O	Error amplifier compensation terminal. Type III compensation method is recommended for stability.
10	FB	I	Voltage feedback. Also used for OVP, UVP, and PGD determination.
11	AGND	G	Device analog ground terminal.
12	VDD	P	Input bias supply for analog functions.
13	VIN	P	Gate driver supply and power conversion voltage.
14	VIN	P	Gate driver supply and power conversion voltage.
15	PGND	P	IC power GND terminal.
16	PGND	P	IC power GND terminal.

(1) B = Bidirectional, G = Ground, I = Input, O = Output, P = Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
Input voltage	VIN, EN	-0.3	7	V	
	VBST	-0.3	17		
	VBST(with respect to SW)	-0.3	7		
	FB, PS, VDD	-0.3	3.7		
Output voltage	SW	DC	-1	7	V
		Pulse < 20 ns, E = 5 μJ	-3	10	
	PGD	-0.3	7		
	COMP, SYNC	-0.3	3.7		
	PGND	-0.3	0.3		
Operating temperature, T <sub>A</sub>		-40	85	°C	
Junction temperature, T <sub>J</sub>		-40	150	°C	
Storage temperature, T <sub>stg</sub>		-55	150	°C	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	2.9		6	V
	VDD	2.9	3.3	3.5	
	VBST	-0.1		13.5	
	VBST(with respect to SW)	-0.1		6	
	EN	-0.1		6	
	FB, PS	-0.1		3.5	
Output voltage	SW	-1		6.5	V
	PGD	-0.1		6	
	COMP, SYNC	-0.1		3.5	
	PGND	-0.1		0.1	
Junction temperature, T <sub>J</sub>		-40		125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS53311	UNIT
		RGT (VQFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	42.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	51.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	16	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	16	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended free-air temperature range, V<sub>IN</sub> = 3.3 V, V<sub>VDD</sub> = 3.3 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY: VOLTAGE, CURRENTS, AND UVLO</b>						
V <sub>IN</sub>	VIN supply voltage	Nominal input voltage	2.9		6	V
I <sub>VINSDN</sub>	VIN shutdown current	EN = LO			3	μA
V <sub>UVLO</sub>	VIN UVLO threshold	Ramp up, EN = HI		2.8		V
V <sub>UVLOHYS</sub>	VIN UVLO hysteresis	VIN UVLO Hysteresis		130		mV
V <sub>DD</sub>	Internal circuitry supply voltage	Nominal 3.3-V input voltage	2.9	3.3	3.5	V
I <sub>DDSDN</sub>	VDD shut down current	EN = LO			5	μA
I <sub>DD</sub>	Standby current	EN = HI, no switching		2.2	3.5	mA
V <sub>DDUVLO</sub>	3.3-V UVLO threshold	Ramp up, EN = HI		2.8		V
V <sub>DDUVLOHYS</sub>	3.3-V UVLO hysteresis			75		mV
<b>VOLTAGE FEEDBACK LOOP: VREF AND ERROR AMPLIFIER</b>						
V <sub>VREF</sub>	VREF	Internal precision reference voltage		0.6		V
TOL <sub>VREF</sub>	VREF Tolerance	0°C ≤ T <sub>A</sub> ≤ 85°C	-1%		1%	
		-40°C ≤ T <sub>A</sub> ≤ 85°C	-1.25%		1.25%	
UGBW <sup>(1)</sup>	Unity gain bandwidth		14			MHz
A <sub>OL</sub> <sup>(1)</sup>	Open loop gain		80			dB
I <sub>FBINT</sub>	FB input leakage current	Sourced from FB pin			30	nA
I <sub>EAMAX</sub> <sup>(1)</sup>	Output sinking and sourcing current	C <sub>COMP</sub> = 20 pF		5		mA
SR <sup>(1)</sup>	Slew rate			5		V/μs
<b>OCP: OVER CURRENT AND ZERO CROSSING</b>						
I <sub>OCP</sub>	Overcurrent limit on upper FET	When I <sub>OUT</sub> exceeds this threshold for 4 consecutive cycles. V <sub>IN</sub> = 3.3 V, V <sub>OUT</sub> = 1.5 V with 1-μH inductor, T <sub>A</sub> = 25°C	4.2	4.5	4.8	A
I <sub>OCPH</sub>	One time overcurrent latch off on the lower FET	Immediately shut down when sensed current reach this value. V <sub>IN</sub> = 3.3 V, V <sub>OUT</sub> = 1.5 V with 1-μH inductor, T <sub>A</sub> = 25°C	4.8	5.1	5.5	A
V <sub>ZXOFF</sub> <sup>(1)</sup>	Zero crossing comparator internal offset	PGND – SW, SKIP mode	-4.5	-3	-1.5	mV
<b>PROTECTION: OVP, UVP, PGD, AND INTERNAL THERMAL SHUTDOWN</b>						
V <sub>OVP</sub>	Overvoltage protection threshold voltage	Measured at FB wrt. VREF	114%	117%	120%	
V <sub>UVP</sub>	Undervoltage protection threshold voltage	Measured at FB wrt. VREF	80%	83%	86%	
V <sub>PGDL</sub>	PGD low threshold	Measured at FB wrt. VREF	80%	83%	86%	

(1) Ensured by design. Not production tested.

**Electrical Characteristics (continued)**

 over recommended free-air temperature range,  $V_{IN} = 3.3\text{ V}$ ,  $V_{VDD} = 3.3\text{ V}$ ,  $PGND = GND$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PGDU}$	PGD upper threshold	Measured at FB wrt. VREF	114%	117%	120%	
$V_{INMINPG}$	Minimum $V_{IN}$ voltage for valid PGD at start up.	Measured at $V_{IN}$ with 1-mA (or 2-mA) sink current on PGD pin at start up		1		V
THSD <sup>(1)</sup>	Thermal shutdown	Latch off controller, attempt soft-stop	130	140	150	°C
THSD <sub>HYS</sub> <sup>(1)</sup>	Thermal Shutdown hysteresis	Controller restarts after temperature has dropped		40		°C
<b>LOGIC PINS: I/O VOLTAGE AND CURRENT</b>						
$V_{PGPD}$	PGD pulldown voltage	Pulldown voltage with 4-mA sink current		0.2	0.4	V
$I_{PGLK}$	PGD leakage current	Hi-Z leakage current, apply 3.3-V in off state	-2	0	2	μA
$R_{ENPU}$	Enable pullup resistor			1.35		MΩ
$V_{ENH}$	EN logic high threshold		1.1	1.18	1.3	V
$V_{ENHYS}$	EN hysteresis			0.18	0.24	V
$PS_{THS}$	PS mode threshold voltage	Level 1 to level 2 <sup>(2)</sup>		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
$I_{PS}$	PS source	10-μA pullup current when enabled	8	10	12	μA
$f_{SYNCSL}$	Slave SYNC frequency range	Versus nominal switching frequency	-20%		20%	
$PW_{SYNC}$	SYNC low pulse width			110		ns
$I_{SYNC}$	SYNC pin sink current			10		μA
$V_{SYNCTHS}$ <sup>(1)</sup>	SYNC threshold	Falling edge		1		V
$V_{SYNCHYS}$ <sup>(1)</sup>	SYNC hysteresis			0.5		V
<b>BOOT STRAP: VOLTAGE AND LEAKAGE CURRENT</b>						
$I_{VBSTLK}$	VBST leakage current	$V_{IN} = 3.3\text{ V}$ , $V_{VBST} = 6.6\text{ V}$ , $T_A = 25^\circ\text{C}$			1	μA
<b>TIMERS: SS, FREQUENCY, RAMP, ON TIME AND I/O TIMING</b>						
$t_{SS\_1}$	Delay after EN asserting	EN = HI, master or HEF mode		0.2		ms
$t_{SS\_2}$	Delay after EN asserting	EN = HI, slave waiting time		0.5		ms
$t_{SS\_3}$	Soft-start ramp-up time	Rising from $V_{SS} = 0\text{ V}$ to $V_{SS} = 0.6\text{ V}$		0.4		ms
$t_{PGDENDLY}$	PGD startup delay time	Rising from $V_{SS} = 0\text{ V}$ to $V_{SS} = 0.6\text{ V}$ , from $V_{SS}$ reaching 0.6 V to $V_{PGD}$ going high		0.4		ms
$t_{OVPDLY}$	Overvoltage protection delay time	Time from FB out of 20% of VREF to OVP fault	1.0	1.7	2.5	μs
$t_{UVPDLY}$	Undervoltage protection delay time	Time from FB out of -20% of VREF to UVP fault		11		μs
$f_{SW}$	Switching frequency control	Forced CCM mode	0.99	1.1	1.21	MHz
	Ramp amplitude <sup>(1)</sup>	$2.9\text{ V} < V_{IN} < 6\text{ V}$		$V_{IN}/4$		V
$t_{MIN(off)}$	Minimum OFF time	FCCM mode or DE mode		100	140	ns
		HEF mode		175	250	
$D_{MAX}$	Maximum duty cycle	FCCM mode and DE mode, $f_{SW} = 1.1\text{ MHz}$ , $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	84%	89%		
		HEF mode, $f_{SW} = 1.1\text{ MHz}$ , $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	75%	81%		
$R_{SFTSTP}$	Soft-discharge transistor resistance	$V_{EN} = \text{Low}$ , $V_{IN} = 3.3\text{ V}$ , $V_{OUT} = 0.5\text{ V}$		60		Ω

(2) See PS pin description for levels.

## 6.6 Typical Characteristics

Inductor IN06142 (1  $\mu$ H, 5.4 m $\Omega$ ) is used.

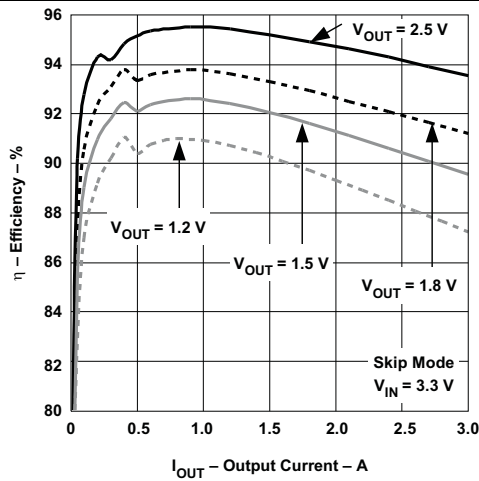


Figure 1. Efficiency vs Output Current, Skip Mode,  $V_{IN} = 3.3$  V

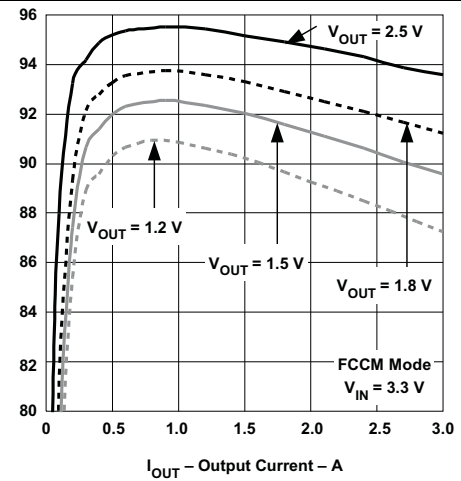


Figure 2. Efficiency vs Output Current, FCCM Mode,  $V_{IN} = 3.3$  V

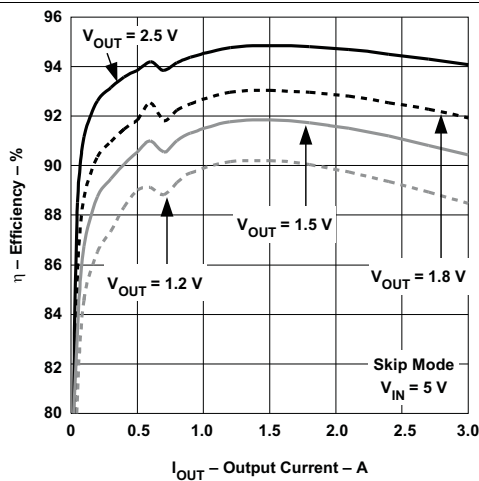


Figure 3. Efficiency vs Output Current, Skip Mode,  $V_{IN} = 5$  V

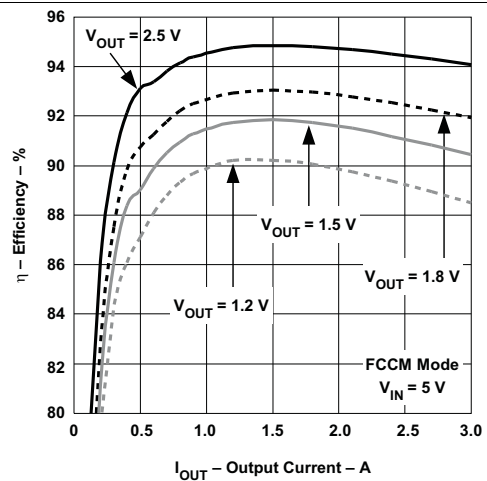


Figure 4. Efficiency vs Output Current, FCCM Mode,  $V_{IN} = 5$  V

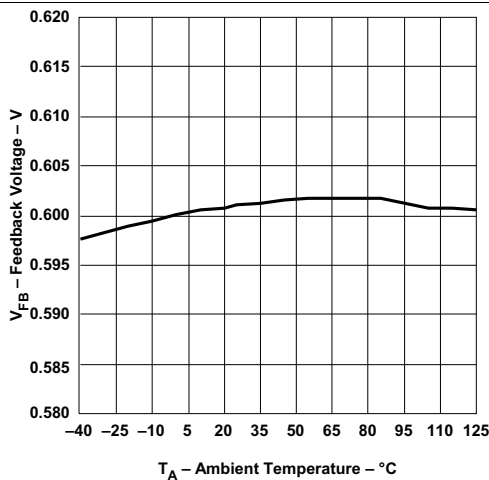


Figure 5. Feedback Voltage vs Ambient Temperature

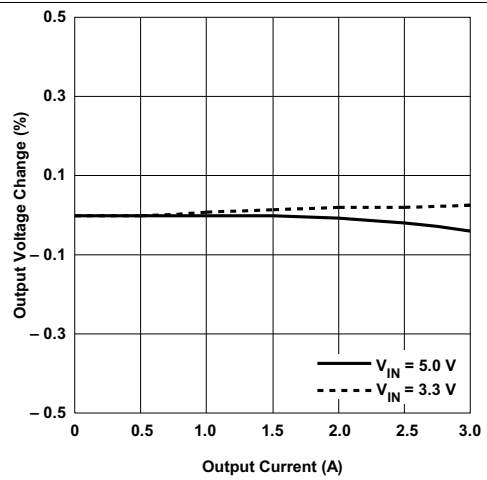


Figure 6. Output Voltage Change vs Output Current

Typical Characteristics (continued)

Inductor IN06142 (1  $\mu$ H, 5.4 m $\Omega$ ) is used.

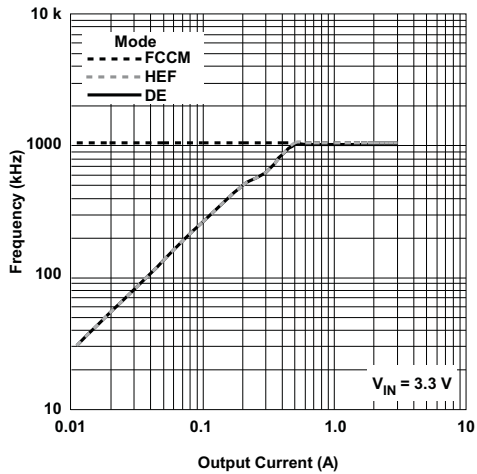


Figure 7. Frequency vs Output Current at  $V_{IN} = 3.3$  V

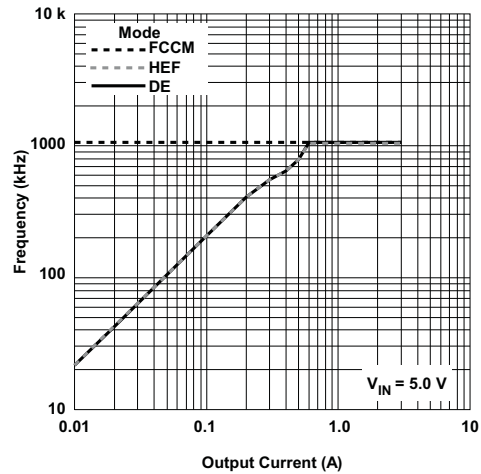


Figure 8. Frequency vs Output Current at  $V_{IN} = 5$  V

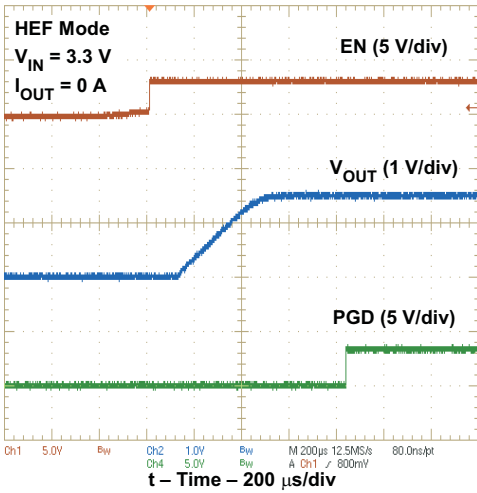


Figure 9. Normal Start-Up Waveform

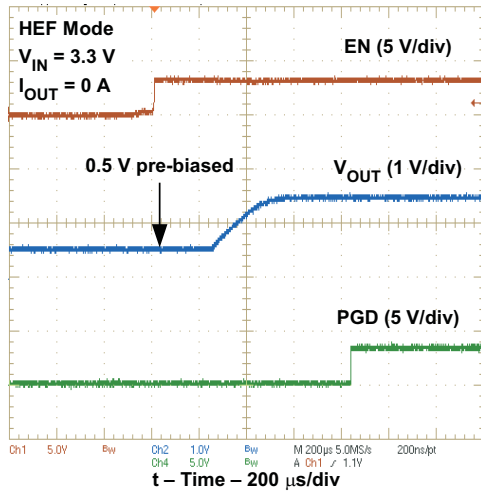


Figure 10. Prebias Start-Up Waveform

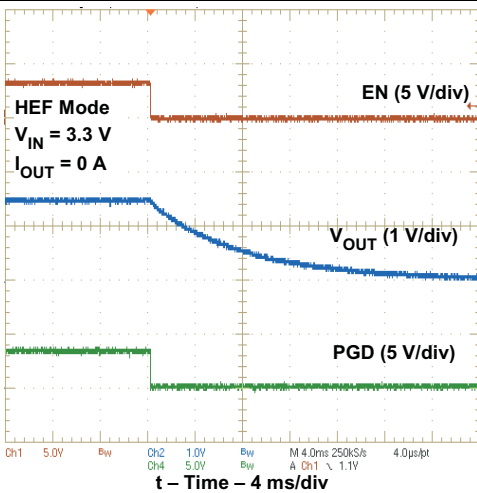


Figure 11. Soft-Stop Waveform

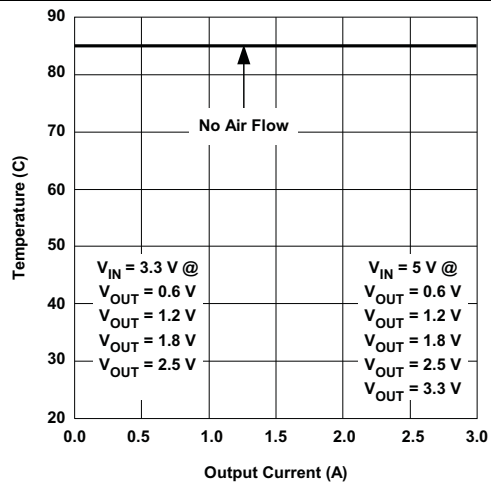


Figure 12. Safe Operating Area



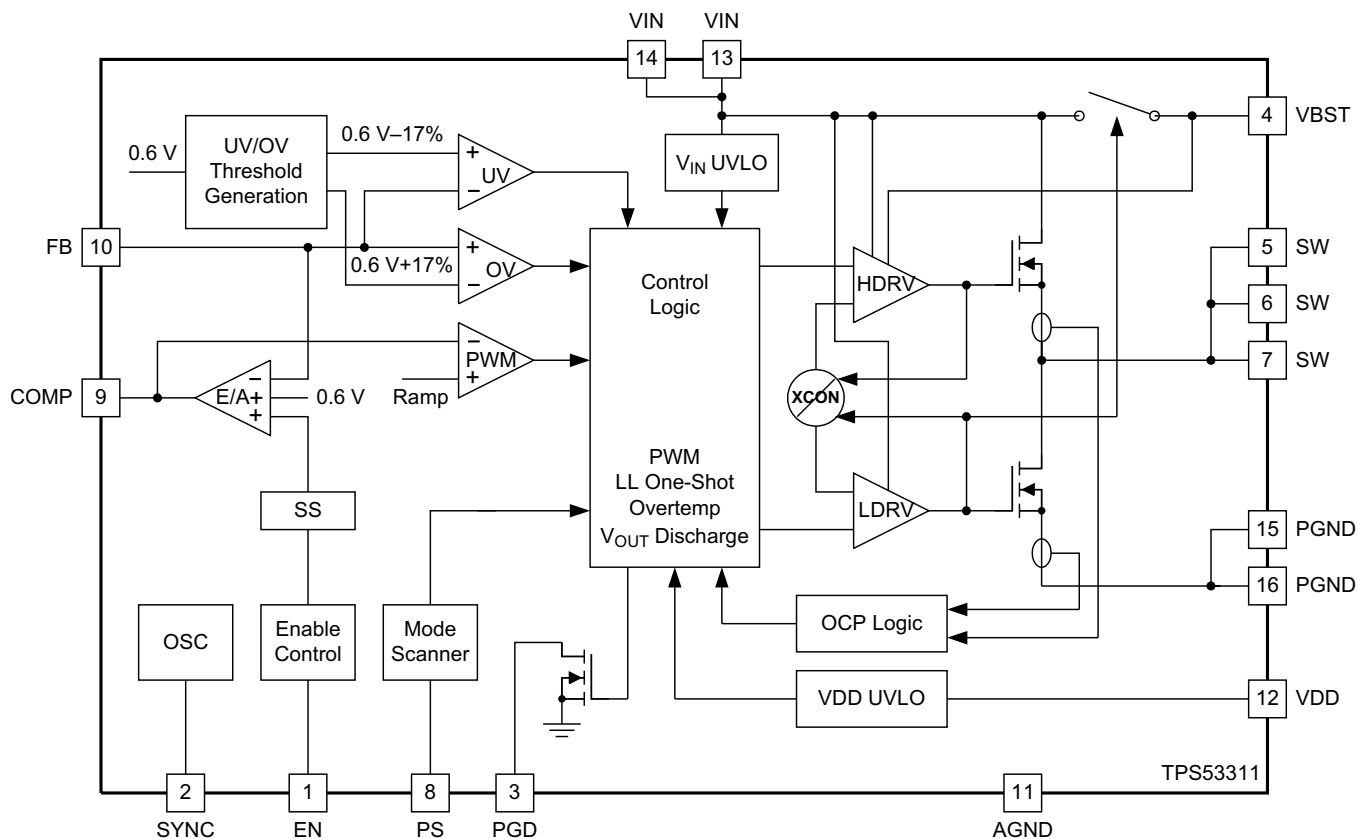
## 7 Detailed Description

### 7.1 Overview

The TPS53311 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 3 A of load current. The TPS53311 provides output voltage between 0.6 V and  $0.84 \times V_{IN}$  from 2.9-V to 6-V wide input voltage range.

This device employs five operation modes to fit various application requirements. The *master and slave* mode enables a two-phase interleaved operation to reduce input ripple. The *skip* mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

### 7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

### 7.3 Feature Description

#### 7.3.1 Soft Start

The soft-start function reduces the inrush current during the start-up sequence. A slow-rising reference voltage is generated by the soft-start circuitry and sent to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, the error amplifier switches to a fixed 600-mV reference. The typical soft-start time is 400  $\mu$ s.

## Feature Description (continued)

### 7.3.2 Power Good

The TPS53311 monitors the voltage on the FB pin. If the FB voltage is between 83% and 117% of the reference voltage, the power good signal remains high. If the FB voltage falls outside of these limits, the internal open-drain output pulls the power good pin (PGD) low.

During start-up, the input voltage must be higher than 1 V to have valid power good logic, and the power good signal is delayed for 400  $\mu$ s after the FB voltage falls to within the power good limits. There is also 10- $\mu$ s delay during the shutdown sequence.

### 7.3.3 Undervoltage Lockout (UVLO) Function

The TPS53311 provides undervoltage lockout (UVLO) protection for both power input ( $V_{IN}$ ) and bias input ( $V_{DD}$ ) voltage. If either of them is lower than the UVLO threshold voltage minus the hysteresis, the device shuts off. When the voltage rises above the threshold voltage, the device restarts. The typical UVLO rising threshold is 2.8 V for both  $V_{IN}$  and  $V_{VDD}$ . A hysteresis voltage of 130 mV for  $V_{IN}$  and 75 mV for  $V_{VDD}$  is also provided to prevent glitch.

### 7.3.4 Overcurrent Protection

The TPS53311 continuously monitors the current flowing through the high-side and the low-side MOSFETs. If the current through the high-side FET exceeds 4.5 A, the high-side FET turns off and the low-side FET turns on until the next PWM cycle. An overcurrent (OC) counter starts to increment each occurrence of an overcurrent event. The converter shuts down immediately when the OC counter reaches four. The OC counter resets if the detected current is less 4.5 A after an OC event.

Another set of overcurrent circuitry monitors the current flowing through low-side FET. If the current through the low-side FET exceeds 5.1 A, the overcurrent protection is enabled and immediately turns off both the high-side and the low-side FETs and shuts down the converter. The device is fully protected against overcurrent during both on-time and off-time. This protection is latched. See TPS53310 data sheet, [3-A Step-Down Regulator with Integrated Switcher](#) (SLUSA68), for information on hiccup overcurrent protection.

### 7.3.5 Overvoltage Protection

The TPS53311 monitors the voltage divided feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, the high-side MOSFET turns off and the low-side MOSFET turns on. The output voltage then drops until it reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device enters a high-impedance state.

### 7.3.6 Undervoltage Protection

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection timer starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10  $\mu$ s, the device turns off both the high-side and the low-side MOSFETs and goes into a high-impedance state. This protection is latched.

### 7.3.7 Overtemperature Protection

The TPS53311 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140°C typical), the device shuts off. When the device temperature falls to 40°C below the overtemperature threshold, it restarts and returns to normal operation.

### 7.3.8 Output Discharge

When the enable pin is low, the TPS53311 discharges the output capacitors through an internal MOSFET switch between SW and PGND while high-side and low-side MOSFETs remain off. The typical discharge switch-on resistance is 60  $\Omega$ . This function is disabled when  $V_{IN}$  is less than 1 V.

## Feature Description (continued)

### 7.3.9 Master and Slave Operation and Synchronization

Two TPS53311 can operate interleaved when configured as master and slave. The SYNC pins of the two devices are connected together for synchronization. In CCM, the master device sends the 180° out-of-phase pulse to the slave device through the SYNC pin, which determines the leading edge of the PWM pulse. If the slave device does not receive the SYNC pulse from the master device or if the SYNC connection is broken during operation, the slave device continues to operate using its own internal clock.

In DE mode, the master and slave switching node does not synchronize to each other if either one of them is operating in DCM. When both master and slave enters CCM, the switching nodes of master and slave synchronize to each other.

The SYNC pin of the slave device can also connect to external clock source within  $\pm 20\%$  of the 1.1-MHz switching frequency. The falling edge of the SYNC triggers the rising edge of the PWM signal.

## 7.4 Device Functional Modes

### 7.4.1 Operation Mode

The TPS53311 offers five operation modes determined by the PS pin connections listed in [Table 1](#).

**Table 1. Operation Mode Selection**

PS PIN CONNECTION	OPERATION MODE	AUTO-SKIP AT LIGHT LOAD	MASTER AND SLAVE SUPPORT
GND	FCCM Slave	—	Slave
24.3 k $\Omega$ to GND	DE Slave	Yes	Slave
57.6 k $\Omega$ to GND	HEF Mode	Yes	—
174 k $\Omega$ to GND	DE Master	Yes	Master
Floating or pulled to VDD	FCCM Master	—	Master

In *forced continuous conduction mode* (FCCM), the high-side FET is ON during the on-time and the low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In *diode emulation* mode (DE), the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET.

When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send a zero-crossing signal. The converter enters into *continuous conduction mode* (CCM) when no zero-crossing is detected for two consecutive PWM pulses. The switching synchronizes to the internal clock and the switching frequency is fixed.

In *high-efficiency* mode (HEF), the operation is the same as diode emulation mode at light load. However, the converter does not synchronize to the internal clock during CCM. Instead, the PWM modulator determines the switching frequency.

### 7.4.2 Light Load Operation

In skip modes (DE and HEF) when the load current is less than one-half of the inductor peak current, the inductor current becomes negative by the end of off-time. During light load operation, the low-side MOSFET is turned off when the inductor current reaches zero. The energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation and the switching frequency is reduced. The switching loss is reduced, thereby improving efficiency.

In both DE and HEF mode, the switching frequency is reduced in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. The difference between  $V_{V_{BST}}$  and  $V_{SW}$  must be maintained at a value higher than 2.4 V.

### 7.4.3 Forced Continuous Conduction Mode

When the PS pin is grounded or greater than 2.2 V, the TPS53311 is operating in *forced continuous conduction mode* in both light-load and heavy-load conditions. In this mode, the switching frequency remains constant over the entire load range, making it suitable for applications that need tight control of switching frequency at a cost of lower efficiency at light load.

## 8 Application and Implementation

### NOTE

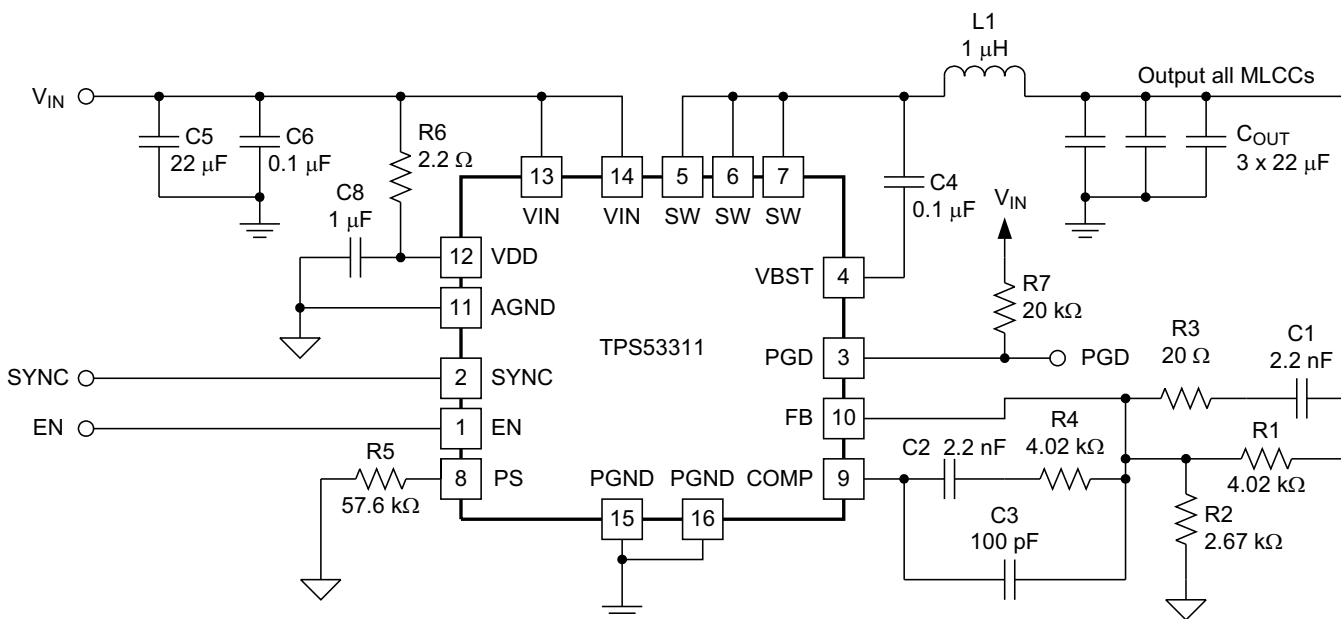
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS53311 device is a high-efficiency synchronous-buck converter. The device suits low-output voltage point-of-load applications with 3-A or lower output current in computing and similar digital consumer applications.

### 8.2 Typical Application

This design example describes a voltage-mode, 3-A synchronous buck converter with integrated MOSFETs. The TPS53311 device provides a fixed 1.5-V output at up to 3 A from a 3.3-V input bus.



Copyright © 2016, Texas Instruments Incorporated

Figure 13. Typical 3.3-V Input Application Circuit Diagram

#### 8.2.1 Design Requirements

Table 2 lists the parameters for this design example.

Table 2. TPS53311 Design Example Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>					
Input voltage, $V_{IN}$	$V_{IN}$	2.9	3.3	6	V
Maximum input current	$V_{IN} = 3.3\text{ V}, 1.5\text{ V or }3\text{ A}$			2.82	A
No load input current	$V_{IN} = 3.3\text{ V}, 1.5\text{ V or }0\text{ A}$			40	mA
<b>OUTPUT CHARACTERISTICS</b>					
Output voltage, $V_O$		1.485	1.5	1.515	V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		

**Typical Application (continued)**
**Table 2. TPS53311 Design Example Specifications (continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage ripple	$V_{IN} = 3.3\text{ V}, 1.5\text{ V}$ or 0 A to 3 A			20	mVpp
Output load current		0		3	A
Output over current			4.5		A
<b>SYSTEMS CHARACTERISTICS</b>					
Switching frequency	Fixed		1.1		MHz
1.5-V full load efficiency	$V_{IN} = 3.3\text{ V}, 1.5\text{ V}$ or 3 A		88.82%		
	$V_{IN} = 5\text{ V}, 1.5\text{ V}$ or 3 A		89.5%		
Operating temperature			25		°C

**8.2.2 Detailed Design Procedure**

Select the external components using the following steps.

**8.2.2.1 Determine the Value of R1 and R2**

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in [Figure 13](#). R1 is connected between the FB pin and the output, and R2 is connected between the FB pin and GND. The recommended value for R1 is from 1 kΩ to 5 kΩ. Determine R2 using equation in [Equation 1](#).

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \quad (1)$$

**8.2.2.2 Choose the Inductor**

The inductance value must be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by [Equation 2](#).

$$I_{L(\text{ripple})} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

**8.2.2.3 Choose the Output Capacitor(s)**

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components calculated with [Equation 3](#) through [Equation 6](#).

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (3)$$

$$V_{RIPPLE(C)} = \frac{I_{L(\text{ripple})}}{8 \times C_{OUT} \times f_{SW}} \quad (4)$$

$$V_{RIPPLE(ESR)} = I_{L(\text{ripple})} \times ESR \quad (5)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (6)$$

When ceramic output capacitors are used, the ESL component is usually negligible. In the case when multiple output capacitors are used, ESR and ESL must be the equivalent of ESR and ESL of all the output capacitor in parallel.

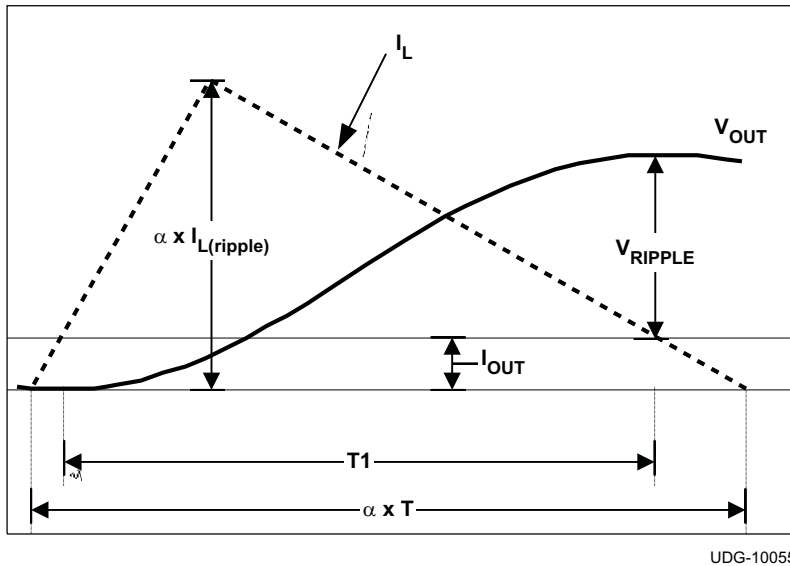
When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in [Equation 7](#).

$$V_{\text{RIPPLE(DCM)}} = \frac{(\alpha \times I_{L(\text{ripple})} - I_{\text{OUT}})^2}{2 \times C_{\text{OUT}} \times f_{\text{SW}} \times I_{L(\text{ripple})}}$$

where

- $\alpha$  is the DCM on-time coefficient and can be expressed in Equation 8 (typical value 1.25) (7)

$$\alpha = \frac{t_{\text{ON(DCM)}}}{t_{\text{ON(CCM)}}}$$



**Figure 14. DCM  $V_{\text{OUT}}$  Ripple Calculation**

### 8.2.2.4 Choose the Input Capacitor

The selection of input capacitor must be determined by the ripple current requirement. The ripple current generated by the converter needs to be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed in Equation 9.

$$I_{\text{IN(ripple)}} = I_{\text{OUT}} \times \sqrt{D \times (1-D)}$$

where

- $D$  is the duty cycle and can be expressed as shown in Equation 10 (9)

$$D = \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors must be placed close to the device. TI recommends the ceramic capacitor because it provides low ESR and low ESL. The input voltage ripple can be calculated as shown in Equation 11 when the total input capacitance is determined.

$$V_{\text{IN(ripple)}} = \frac{I_{\text{OUT}} \times D}{f_{\text{SW}} \times C_{\text{IN}}}$$

### 8.2.2.5 Compensation Design

The TPS53311 uses voltage mode control. To effectively compensate the power stage and ensure fast transient response, Type III compensation is typically used.

The control to output transfer function can be described in Equation 12.

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left( \frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (12)$$

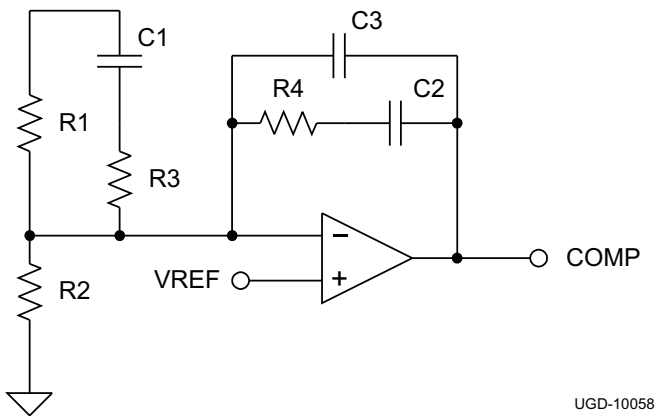
The output L-C filter introduces a double pole which can be calculated as shown in Equation 13.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (13)$$

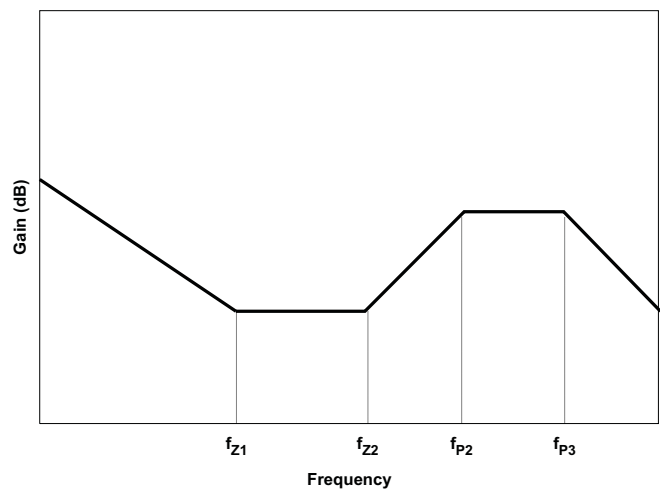
The ESR zero can be calculated as shown in Equation 14.

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (14)$$

Figure 15 and Figure 16 show the configuration of Type III compensation and typical pole and zero locations. Equation 16 through Equation 20 describe the compensator transfer function and poles and zeros of the Type III network.



**Figure 15. Type III Compensation Network Configuration Schematic**



**Figure 16. Type III Compensation Gain Plot and Zero/Pole Placement**

$$G_{EA} = \frac{(1 + s \times C_1 \times (R_1 + R_3))(1 + s \times R_4 \times C_2)}{(s \times R_1 \times (C_2 + C_3)) \times (1 + s \times C_1 \times R_3) \times \left( 1 + s \times R_4 \times \frac{C_2 \times C_3}{C_2 + C_3} \right)} \quad (15)$$

$$f_{z1} = \frac{1}{2 \times \pi \times R_4 \times C_2} \quad (16)$$

$$f_{z2} = \frac{1}{2 \times \pi \times (R_1 + R_3) \times C_1} \cong \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (17)$$

$$f_{p1} = 0 \quad (18)$$

$$f_{p2} = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad (19)$$

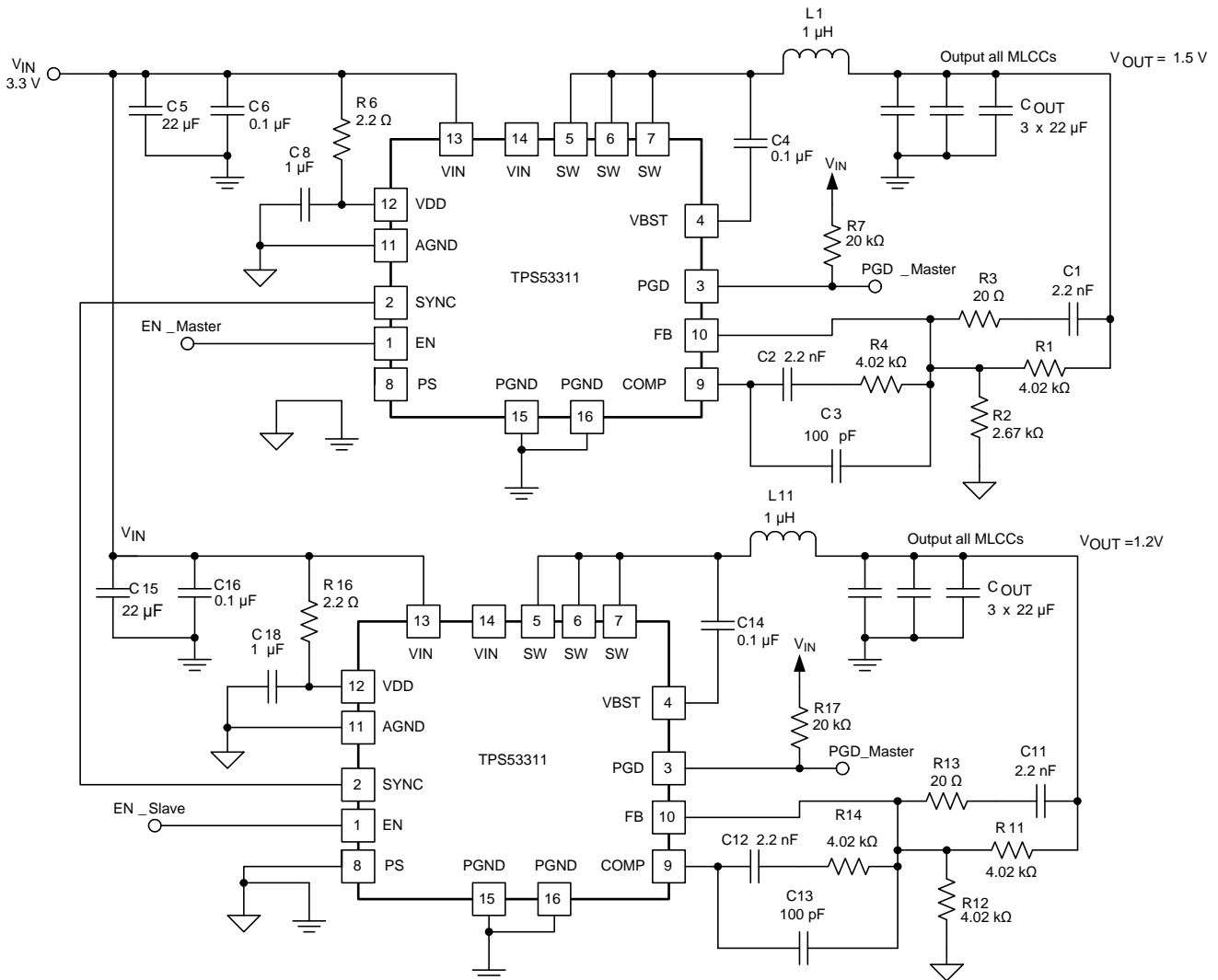
$$f_{p3} = \frac{1}{2 \times \pi \times R_4 \times \left( \frac{C_2 \times C_3}{C_2 + C_3} \right)} \cong \frac{1}{2 \times \pi \times R_4 \times C_3} \quad (20)$$



The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45 degrees is required for stable operation.

For DCM operation, a C3 between 56 pF and 150 pF is recommended for output capacitance between 20 μF to 200 μF.

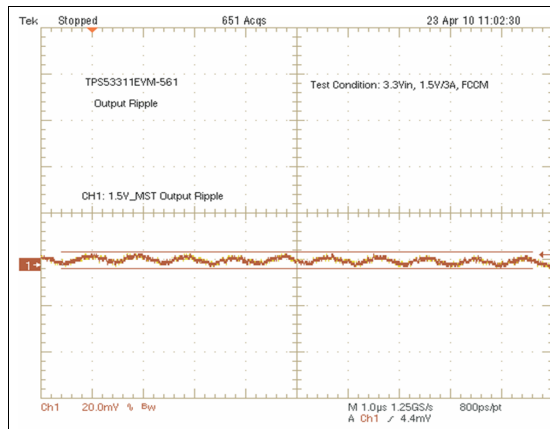
Figure 17 shows the master and slave configuration schematic for a design with a 3.3-V input.



Copyright © 2016, Texas Instruments Incorporated

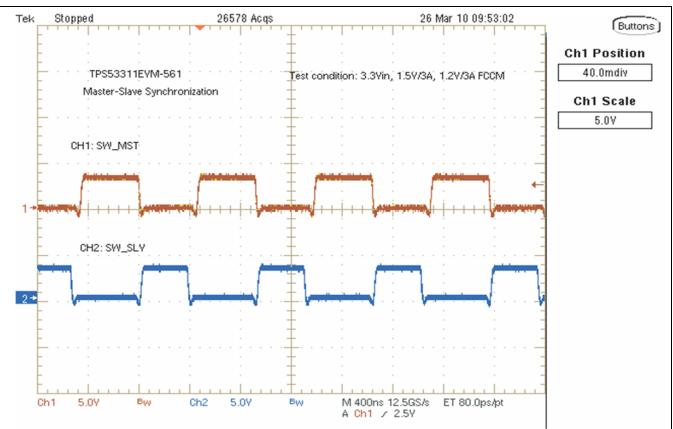
**Figure 17. Master and Slave Configuration Schematic**

**8.2.3 Application Curves**



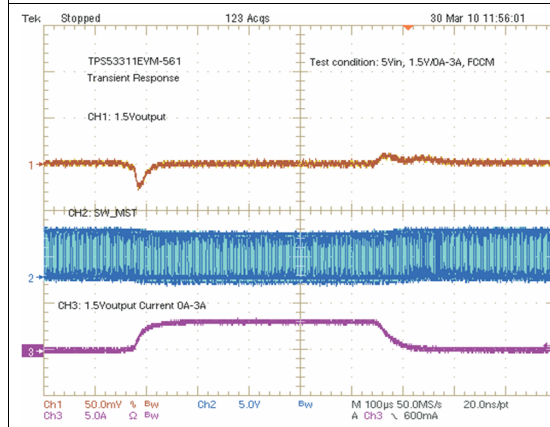
3.3 V<sub>IN</sub>, 1.5 V/3 A

**Figure 18. 1.5-V Output Ripple**



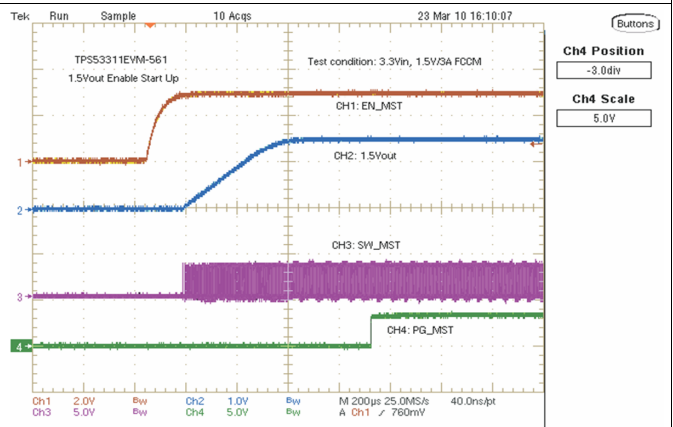
3.3 V<sub>IN</sub>, 1.5 V/3 A and 1.2 V/3 A

**Figure 19. Master-Slave 180° Synchronization**



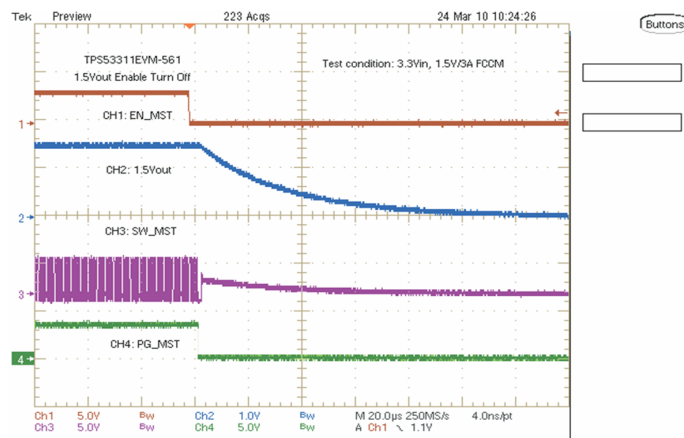
5 V<sub>IN</sub>, 1.5 V/0 A-3 A

**Figure 20. 1.5-V Output Transient**



3.3 V<sub>IN</sub>, 1.5 V/3 A

**Figure 21. 1.5-V Turnon Waveform**



3.3 V<sub>IN</sub>, 1.5 V/3 A

**Figure 22. 1.5-V Turnoff Waveform**

## 9 Power Supply Recommendations

The TPS53311 device is designed to operate from an input voltage supply range from 2.9 V to 6 V (2.9 V to 3.5 V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in [Layout](#).

## 10 Layout

### 10.1 Layout Guidelines

Good layout is essential for stable power supply operation. Follow these guidelines for a clean PCB layout:

- Separate the power ground and analog ground planes. Connect them together at one location.
- Use four vias to connect the thermal pad to power ground.
- Place  $V_{IN}$  and  $V_{DD}$  decoupling capacitors as close to the device as possible.
- Use wide traces for  $V_{IN}$ ,  $V_{OUT}$ , PGND and SW. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, SYNC, VBST).
- See [Using the TPS53311EVM-561, a 3-A Eco-mode™ Integrated Switcher With Master Slave](#) (SLUU428) for a layout example.

### 10.2 Layout Example

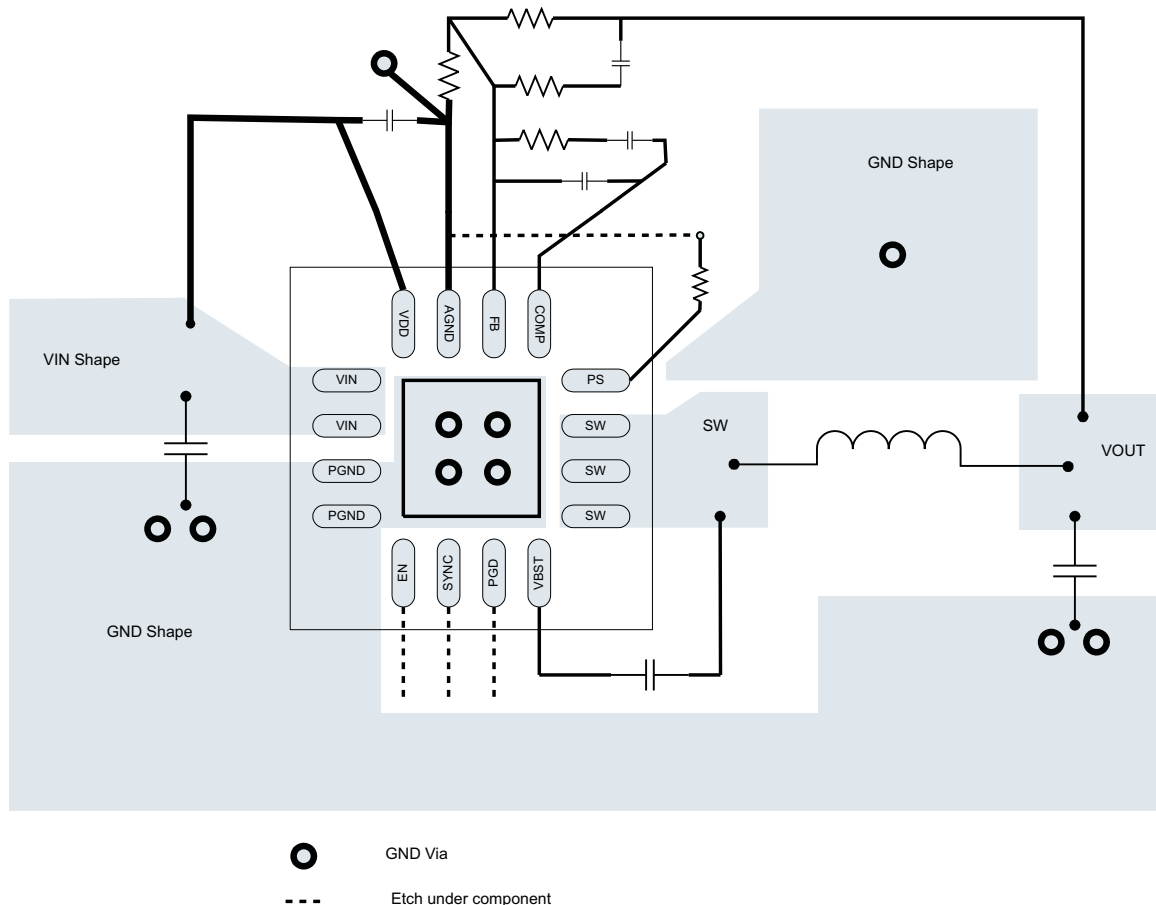


Figure 23. TPS533x Layout Example

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントのサポート

#### 11.1.1 関連資料

関連資料については、以下を参照してください。

- 『3A スイッチャ内蔵降圧型レギュレータ』(SLUSA68)
- 『TPS53311EVM-561、マスタ-スレーブ内蔵、3A Eco-mode™統合スイッチャの使用法』(SLUU428)

### 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 商標

SmoothPWM, Eco-mode, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53311RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311	<a href="#">Samples</a>
TPS53311RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53311RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53311RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53311RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS53311RGTT	VQFN	RGT	16	250	210.0	185.0	35.0



**RGT 16**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

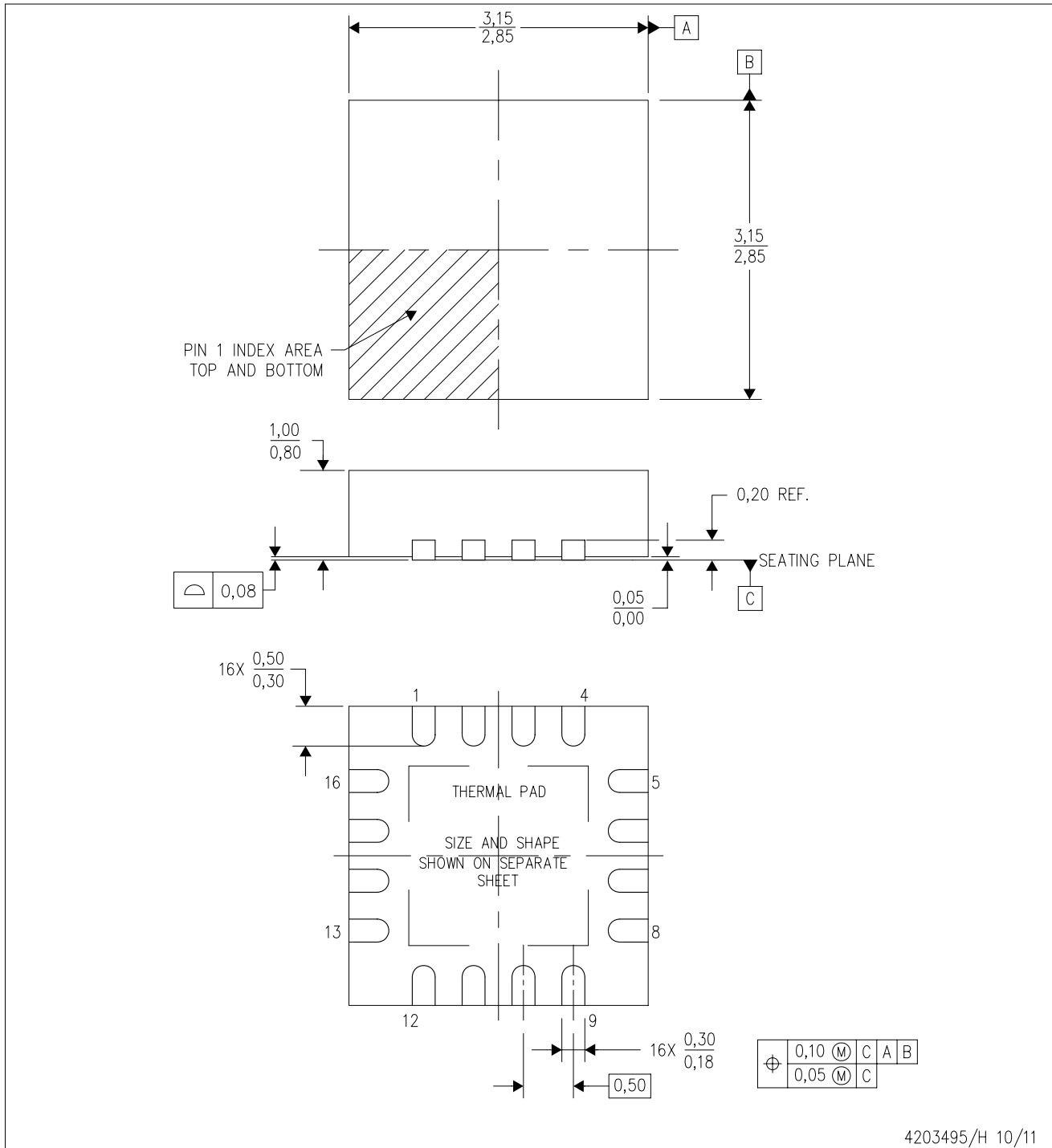


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

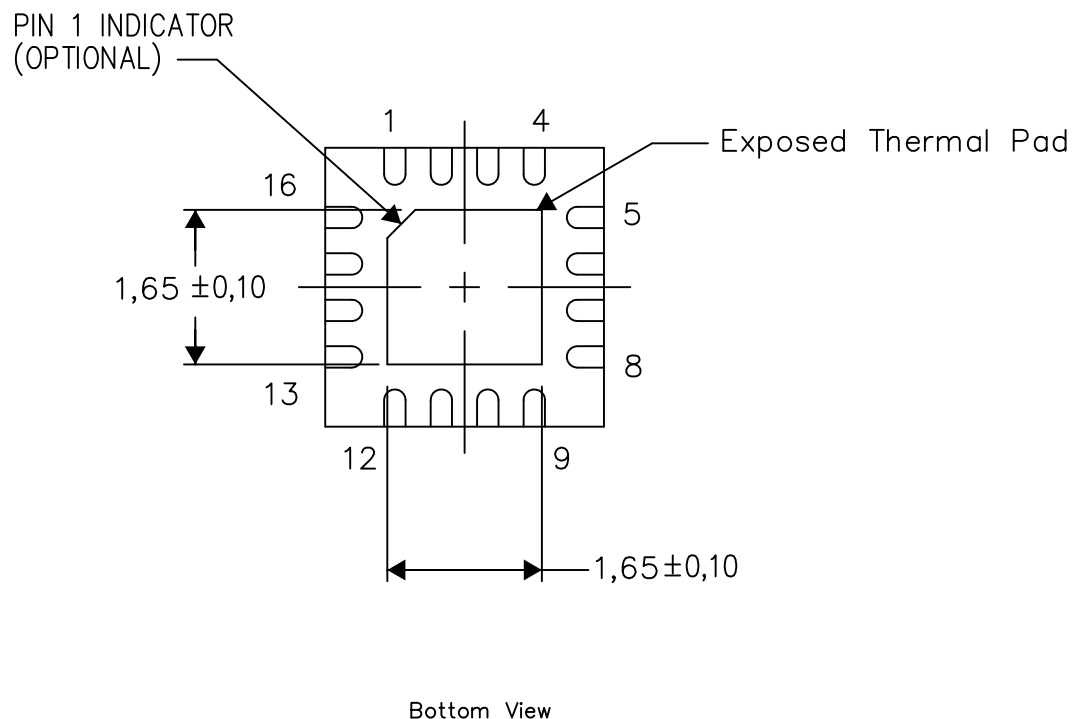
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206349-7/Z 08/15

NOTE: All linear dimensions are in millimeters



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/D 04/2022

NOTES:

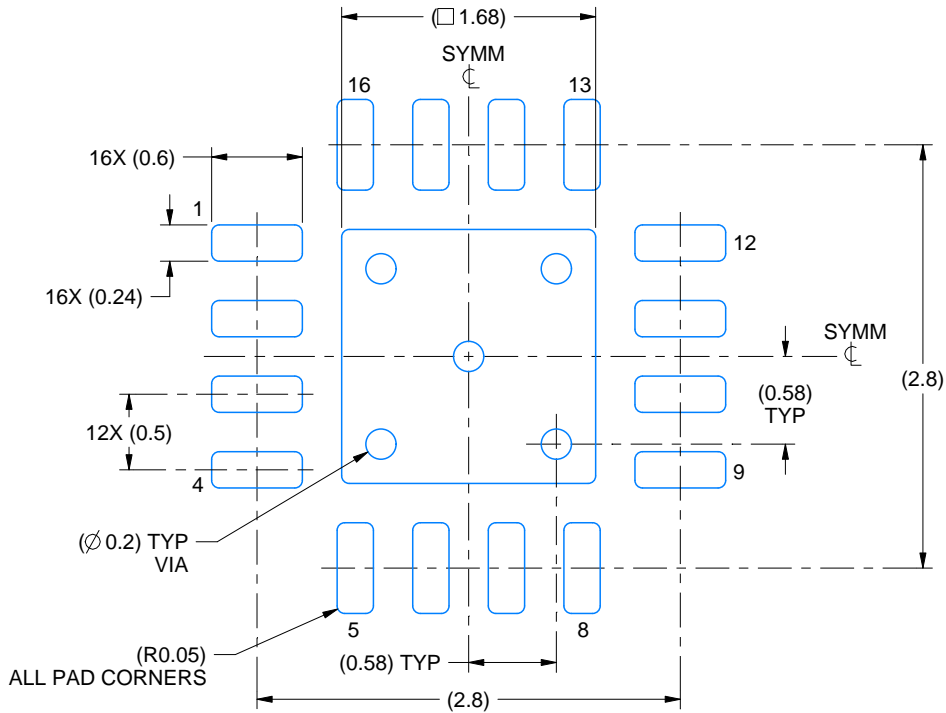
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

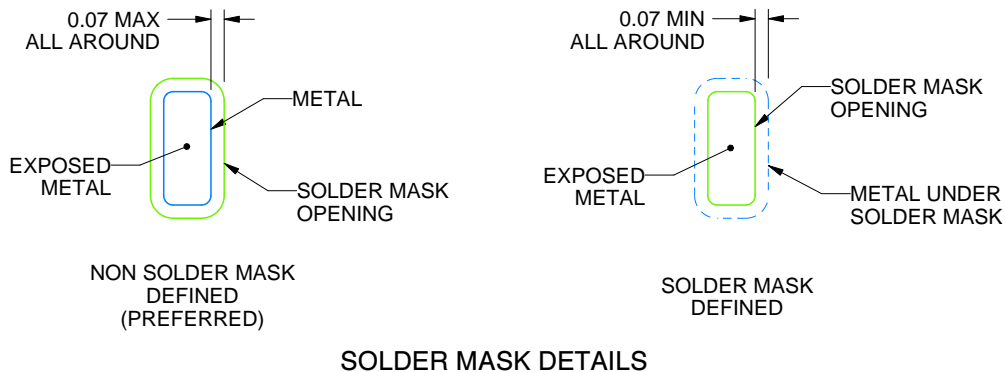
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated