

TPS54340 42V入力、3.5A、降圧型DC/DCコンバータ、Eco-mode™搭載

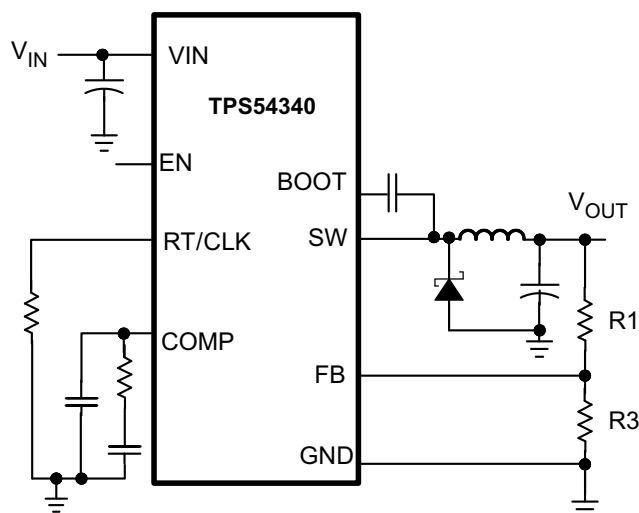
1 特長

- 入力範囲4.5V~42V (絶対最大定格45V)
- 連続電流3.5A、最小ピーク・インダクタ電流制限4.5A
- 電流モード制御のDC/DCコンバータ
- 92mΩのハイサイドMOSFET
- 軽負荷で高い効率を実現するパルス・スキップ Eco-mode™
- 内蔵のブート再充電FETにより軽負荷時のドロップアウトを低減
- 動作時の静止電流146μA
- シャットダウン時電流1μA
- 固定スイッチング周波数: 100kHz~2.5MHz
- 外部クロックに同期
- 調整可能なUVLO電圧およびヒステリシス
- 内部ソフト・スタート
- 高精度のサイクル単位電流制限
- 熱、過電圧、周波数フォールドバック保護
- 内部基準電圧: 0.8V、1%
- 8端子のHSOP PowerPAD™パッケージ
- 動作温度範囲T_J = -40°C~150°C
- WEBENCH Power Designerにより、TPS54340を使用するカスタム設計を作成

2 アプリケーション

12V、24Vの産業用、車載用、通信用電源システム

概略回路図



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3 概要

TPS54340は、ハイサイドMOSFETを内蔵した42V、3.5Aの降圧型レギュレータです。ISO 7637に準拠し、最大45Vの負荷ダンプ・パルスに耐えることができます。電流モード制御により、外部補償が単純化され、柔軟な部品選択が可能になります。低リップルのパルス・スキップ・モードを使用すると、無負荷時の消費電流を146μAまで低減できます。イネーブル・ピンをLowにすると、シャットダウン時消費電流が1μAまで減少します。

低電圧誤動作防止は内部で4.3Vに設定されていますが、イネーブル・ピンを使用してさらに高い電圧に設定することができます。起動時の出力電圧の上昇を内部で制御することにより、オーバーシュートを防ぎます。

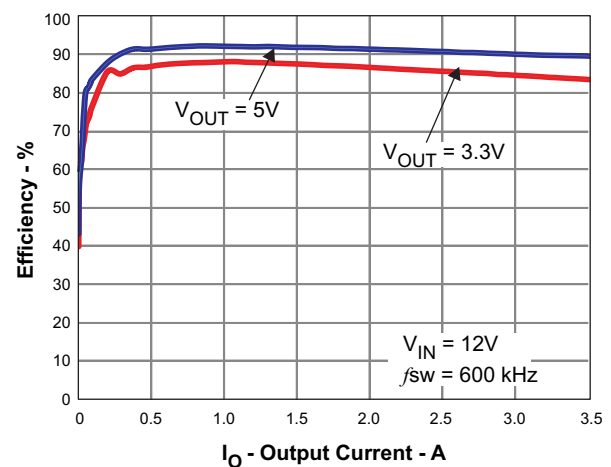
スイッチング周波数の範囲が広いいため、効率または外部部品のサイズを最適化できます。周波数フォールドバックと過熱シャットダウン機能によって、過負荷状態時に内部部品および外部部品を保護します。

TPS54340は、熱特性が強化された8端子のHSOP PowerPAD™パッケージで供給されます。

製品情報

発注型番	パッケージ	本体サイズ
TPS54340DDA	HSOP (8)	4.89mm×3.9mm

効率と負荷電流との関係



目次

1	特長	1	7.4	Device Functional Modes	22
2	アプリケーション	1	8	Application and Implementation	23
3	概要	1	8.1	Application Information	23
4	改訂履歴	2	8.2	Typical Applications	23
5	Pin Configuration and Functions	4	8.3	WEBENCH Power Designer	36
6	Specifications	5	9	Power Supply Recommendations	36
6.1	Absolute Maximum Ratings	5	10	Layout	37
6.2	ESD Ratings	5	10.1	Layout Guidelines	37
6.3	Recommended Operating Conditions	5	10.2	Layout Example	37
6.4	Thermal Information	5	11	デバイスおよびドキュメントのサポート	38
6.5	Electrical Characteristics	6	11.1	ドキュメントのサポート	38
6.6	Timing Requirements	7	11.2	商標	38
6.7	Typical Characteristics	7	11.3	コミュニティ・リソース	38
7	Detailed Description	11	11.4	静電気放電に関する注意事項	38
7.1	Overview	11	11.5	Glossary	38
7.2	Functional Block Diagram	12	12	メカニカル、パッケージ、および注文情報	39
7.3	Feature Description	12			

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (June 2016) から Revision D に変更

Page

•	Changed V_{IN} MIN Value From: 4.5 V To: $V_O + V_{DO}$, and added Note 1 in the <i>Recommended Operating Conditions</i>	5
•	Updated text and added Equation 1 in the <i>Low Dropout Operation and Bootstrap Voltage (BOOT)</i>	13
•	Deleted text: "The start and stop voltage for a typical 5 V..." and Figure: "5V Start/Stop Voltage" from the <i>Low Dropout Operation and Bootstrap Voltage (BOOT)</i> section	13
•	Added new section: <i>Minimum V_{IN}</i>	29
•	Deleted 2 graphs named "Low Dropout Operation" from the <i>Application Curves</i> section	32

Revision B (March 2014) から Revision C に変更

Page

•	「 特長 」セクション、およびデータシート全体でパッケージのHSOICをHSOPに変更	1
•	Moved Storage temperature to the <i>Absolute Maximum Ratings</i> ⁽¹⁾ table	5
•	Changed the <i>Handling Ratings</i> table to the <i>ESD Ratings</i> table	5
•	Changed Output current MAX value From: 5 A To: 3.5 A in the <i>Recommended Operating Conditions</i> table	5
•	Changed Error amplifier transconductance units from μ Mhos to μ S in the <i>Electrical Characteristics</i> table	6
•	Changed Equation 7 and Equation 8	15
•	Changed Equation 27	24

Revision A (February 2013) から Revision B に変更

Page

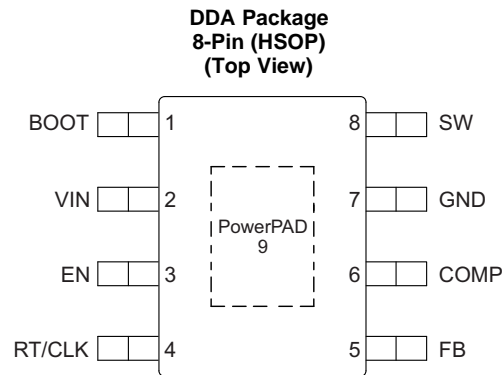
•	データシートを新しいTILレイアウトに変更	1
•	アプリケーションの一覧を「12V、24V、48Vの産業用」から「12V、24Vの産業用」に変更	1
•	製品情報の表を追加	1
•	Added the <i>Handling Ratings</i> table	5
•	Added the Recommended Operating Conditions table	5
•	Added the Thermal Information table inside the document	5
•	Changed the Operating: nonswitching supply current TEST CONDITIONS From: $FB = 0.83$ V To: $FB = 0.9$ V	6

• Changed RT/CLK high threshold MAX value From: 1.7 V To: 2 V	6
• Changed Figure 6 title From: HIGH FREQUENCY RANGE To: LOW FREQUENCY RANGE	7
• Changed Figure 7 title From: LOW FREQUENCY RANGE To: HIGH FREQUENCY RANGE	7
• Added the Power Supply Recommendations section	36

2012年10月発行のものから更新
Page

• Changed Figure 11 From: I_{EN} (μ V) To: I_{EN} (μ A)	8
• Changed Figure 12 From: I_{EN} (μ V) To: I_{EN} (μ A)	8

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high side MOSFET, the output is switched off until the capacitor is refreshed.
VIN	2	I	Input supply voltage with 4.5 V to 42 V operating range.
EN	3	I	Enable terminal, with internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the Enable and Adjusting Undervoltage Lockout section.
RT/CLK	4	I	Resistor Timing and External Clock. An internal amplifier holds this terminal at a fixed voltage when using an external resistor to ground to set the switching frequency. If the terminal is pulled above the PLL upper threshold, a mode change occurs and the terminal becomes a synchronization input. The internal amplifier is disabled and the terminal is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
FB	5	I	Inverting input of the transconductance (gm) error amplifier.
COMP	6	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this terminal.
GND	7	–	Ground
SW	8	I	The source of the internal high-side power MOSFET and switching node of the converter.
Thermal Pad	9	–	GND terminal must be electrically connected to the exposed pad on the printed circuit board for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V _{IN}	-0.3	45	V
	EN	-0.3	8.4	
	BOOT		53	
	FB	-0.3	3	
	COMP	-0.3	3	
	RT/CLK	-0.3	3.6	
Output voltage	BOOT-SW		8	V
	SW	-0.6	45	
	SW, 10-ns Transient	-2	45	
Operating junction temperature		-40	150	°C
Storage temperature, T _{STG}		-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _{ESD} ⁽¹⁾	Human Body Model (HBM) ESD Stress Voltage ⁽²⁾	±2000	V
	Charged Device Model (HBM) ESD Stress Voltage ⁽³⁾	±500	

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. terminals listed as 1000V may actually have higher performance.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. terminals listed as 250V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Supply input voltage ⁽¹⁾	V _O + V _{DO}	42	V
V _O	Output voltage	0.8	41.1	V
I _O	Output current	0	3.5	A
T _J	Junction Temperature	-40	150	°C

- (1) See [Equation 1](#)

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS54340	UNIT
		DDA (8 PINS)	
θ _{JA}	Junction-to-ambient thermal resistance (standard board)	42.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	5.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	23.4	°C/W
θ _{JCtop}	Junction-to-case(top) thermal resistance	45.8	°C/W
θ _{JCbot}	Junction-to-case(bottom) thermal resistance	3.6	°C/W
θ _{JB}	Junction-to-board thermal resistance	23.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.

6.5 Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$ to 150°C , $V_{IN} = 4.5\text{ V}$ to 42 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN TERMINAL)					
Operating input voltage		4.5		42	V
Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
Internal undervoltage lockout threshold hysteresis			325		mV
Shutdown supply current	$EN = 0\text{ V}$, 25°C , $4.5\text{ V} \leq V_{IN} \leq 42\text{ V}$		1.3	3.5	μA
Operating: nonswitching supply current	$FB = 0.9\text{ V}$, $T_A = 25^{\circ}\text{C}$		146	175	
ENABLE AND UVLO (EN TERMINAL)					
Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
Input current	Enable threshold +50 mV		-4.6		μA
	Enable threshold -50 mV	-0.58	-1.2	-1.8	
Hysteresis current		-2.2	-3.4	-4.5	μA
VOLTAGE REFERENCE					
Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET					
On-resistance	$V_{IN} = 12\text{ V}$, $BOOT-SW = 6\text{ V}$		92	190	m Ω
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (g_m)	$-2\ \mu\text{A} < I_{COMP} < 2\ \mu\text{A}$, $V_{COMP} = 1\text{ V}$		350		μS
Error amplifier transconductance (g_m) during soft-start	$-2\ \mu\text{A} < I_{COMP} < 2\ \mu\text{A}$, $V_{COMP} = 1\text{ V}$, $V_{FB} = 0.4\text{ V}$		77		μS
Error amplifier dc gain	$V_{FB} = 0.8\text{ V}$		10,000		V/V
Min unity gain bandwidth			2500		kHz
Error amplifier source/sink	$V_{(COMP)} = 1\text{ V}$, 100 mV overdrive		± 30		μA
COMP to SW current transconductance			12		A/V
CURRENT LIMIT					
Current limit threshold	All V_{IN} and temperatures, Open Loop ⁽¹⁾	4.5	5.5	6.8	A
	All temperatures, $V_{IN} = 12\text{ V}$, Open Loop ⁽¹⁾	4.5	5.5	6.25	
	$V_{IN} = 12\text{ V}$, $T_A = 25^{\circ}\text{C}$, Open Loop ⁽¹⁾	5.2	5.5	5.85	
THERMAL SHUTDOWN					
Thermal shutdown			176		$^{\circ}\text{C}$
Thermal shutdown hysteresis			12		$^{\circ}\text{C}$
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK TERMINAL)					
Switching frequency range using RT mode		100		2500	kHz
f_{SW} Switching frequency	$R_T = 200\text{ k}\Omega$	450	500	550	kHz
Switching frequency range using CLK mode		160		2300	kHz
RT/CLK high threshold			1.55	2	V
RT/CLK low threshold		0.5	1.2		V

(1) Open Loop current limit measured directly at the SW terminal and is independent of the inductor value and slope compensation.

6.6 Timing Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE AND UVLO (EN TERMINAL)					
Enable to COMP active	$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$		540		μs
INTERNAL SOFT-START TIME					
Soft-Start Time	$f_{SW} = 500\text{ kHz}$, 10% to 90%		2.1		ms
Soft-Start Time	$f_{SW} = 2.5\text{ MHz}$, 10% to 90%		0.42		ms
HIGH-SIDE MOSFET					
Minimum controllable on time	$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$		135		ns
CURRENT LIMIT					
Current limit threshold delay			60		ns
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK TERMINAL)					
Minimum CLK input pulse width			15		ns
RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with RT resistor in series		55		ns
PLL lock in time	Measured at 500 kHz		78		μs

6.7 Typical Characteristics

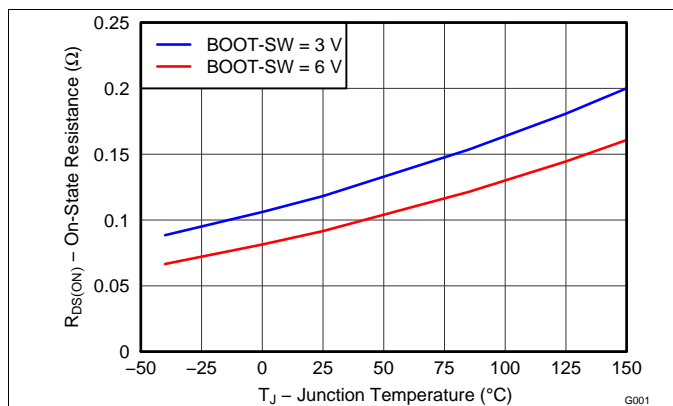


Figure 1. On Resistance vs Junction Temperature

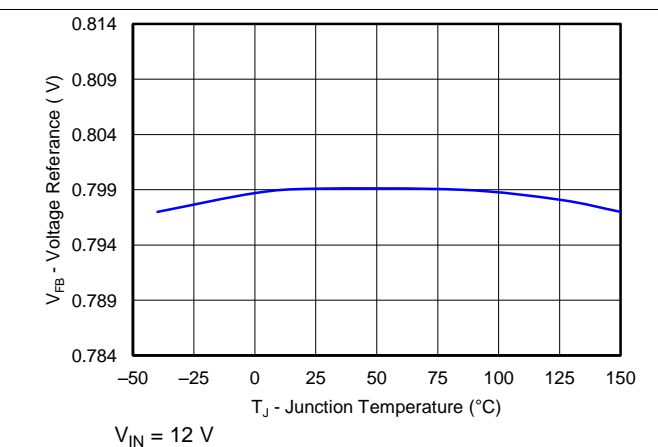


Figure 2. Voltage Reference vs Junction Temperature

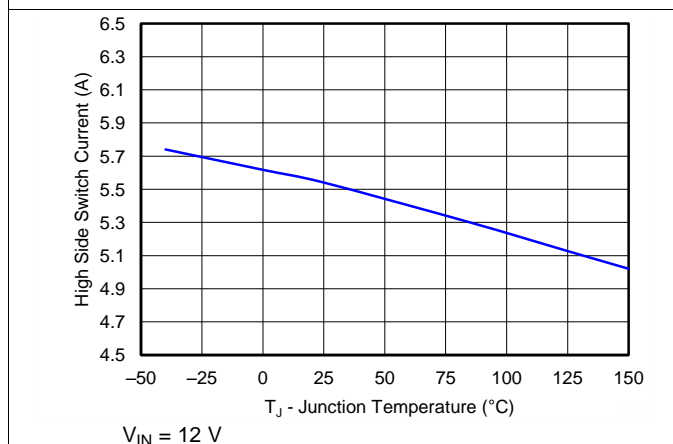


Figure 3. Switch Current Limit vs Junction Temperature

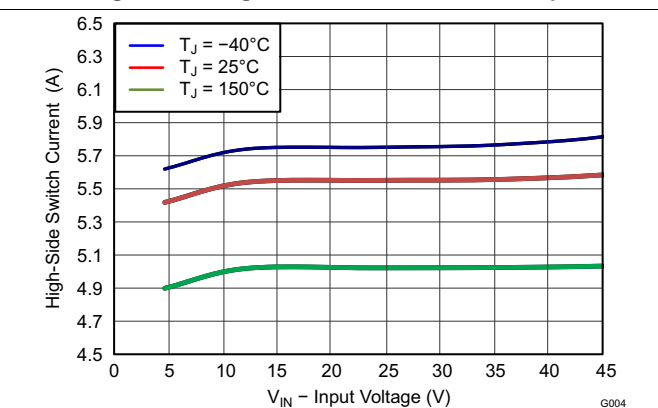


Figure 4. Switch Current Limit vs Input Voltage

Typical Characteristics (continued)

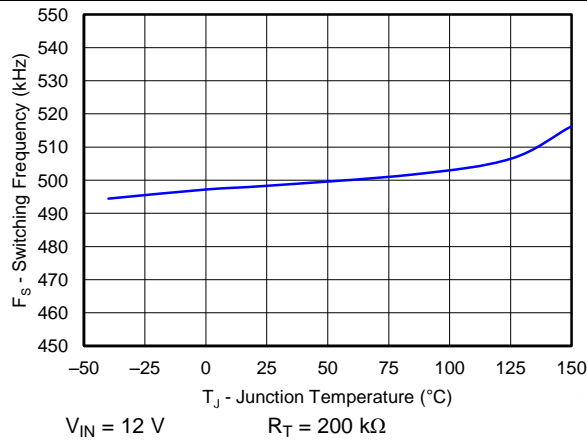


Figure 5. Switching Frequency vs Junction Temperature

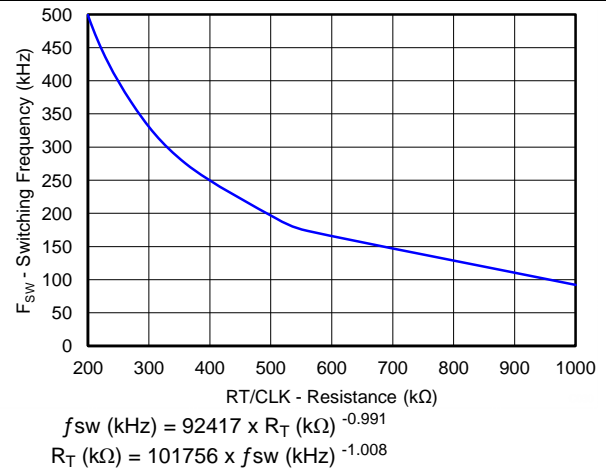


Figure 6. Switching Frequency vs RT/CLK Resistance Low Frequency Range

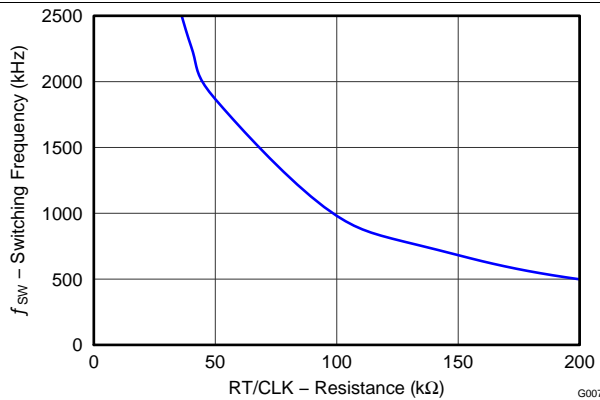


Figure 7. Switching Frequency vs RT/CLK Resistance High Frequency Range

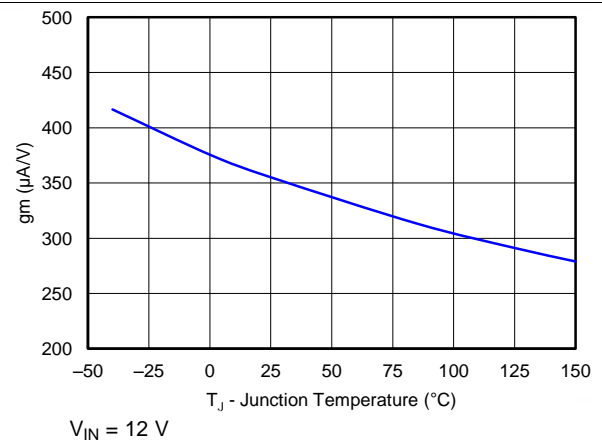


Figure 8. EA Transconductance vs Junction Temperature

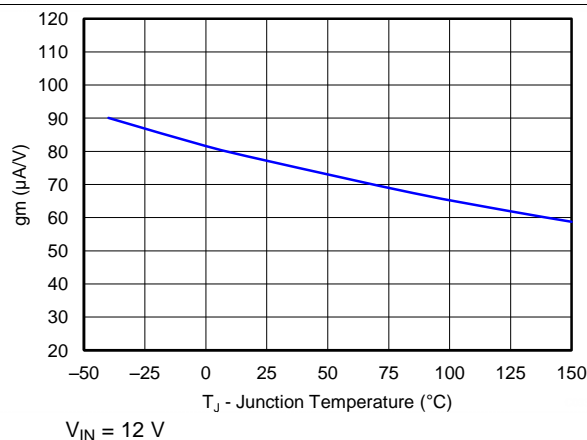


Figure 9. EA Transconductance During Soft-Start vs Junction Temperature

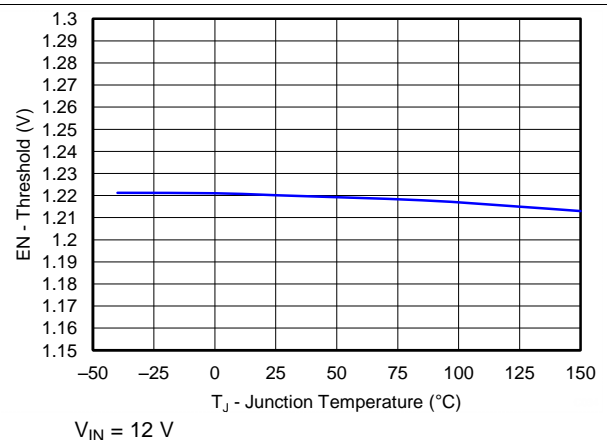


Figure 10. EN Terminal Voltage vs Junction Temperature

Typical Characteristics (continued)

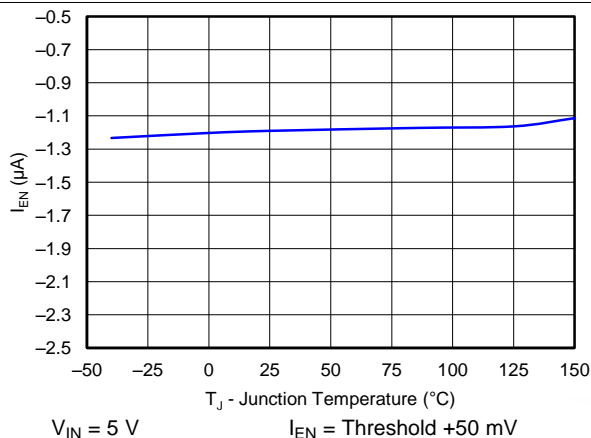


Figure 11. EN Terminal Current vs Junction Temperature

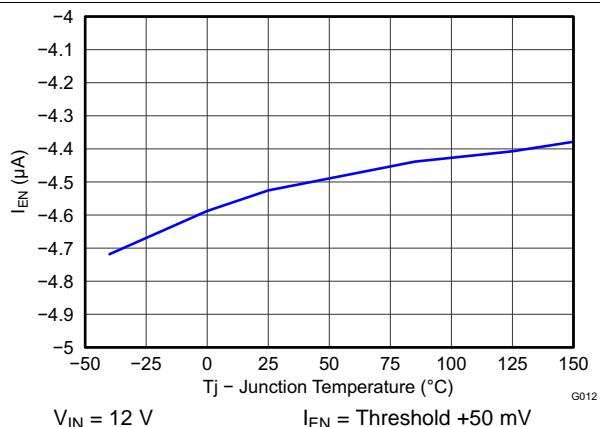


Figure 12. EN Terminal Current vs Junction Temperature

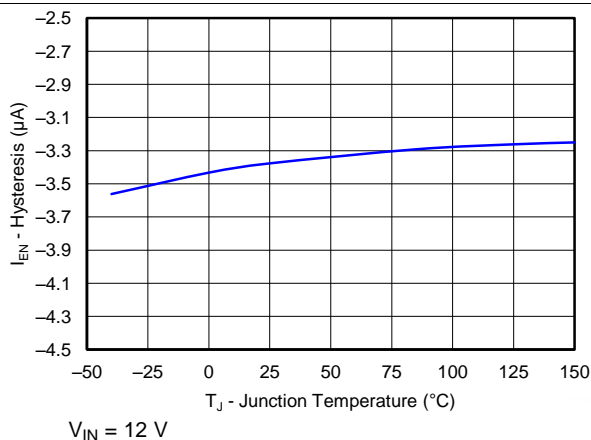


Figure 13. EN Terminal Current Hysteresis vs Junction Temperature

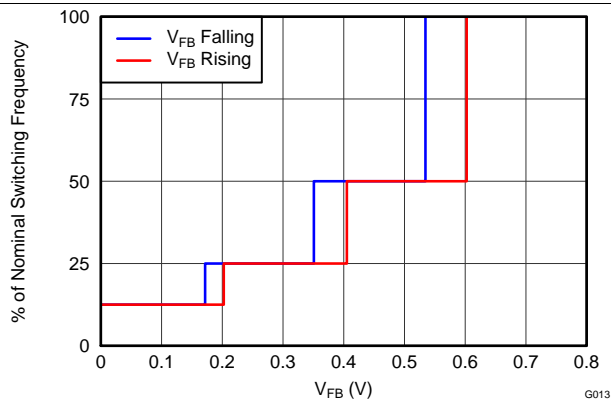


Figure 14. Switching Frequency vs FB

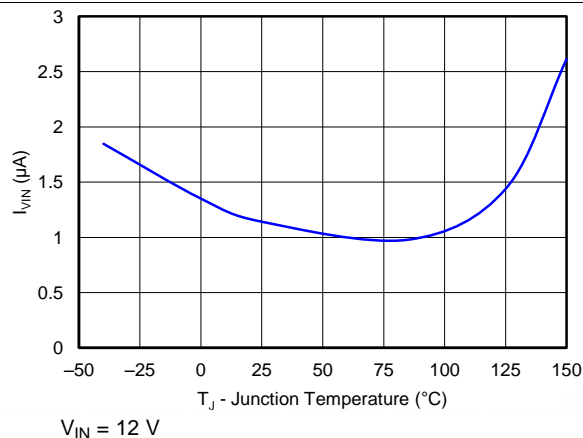


Figure 15. Shutdown Supply Current vs Junction Temperature

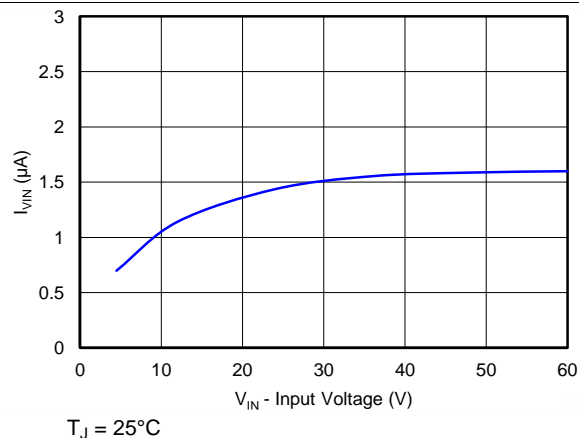


Figure 16. Shutdown Supply Current vs Input Voltage (V_{IN})

Typical Characteristics (continued)

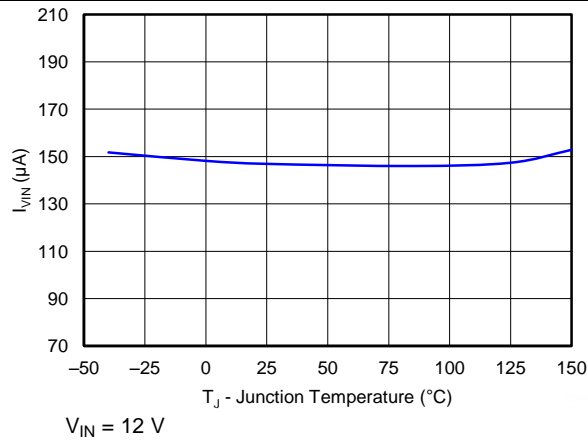


Figure 17. V_{IN} Supply Current vs Junction Temperature

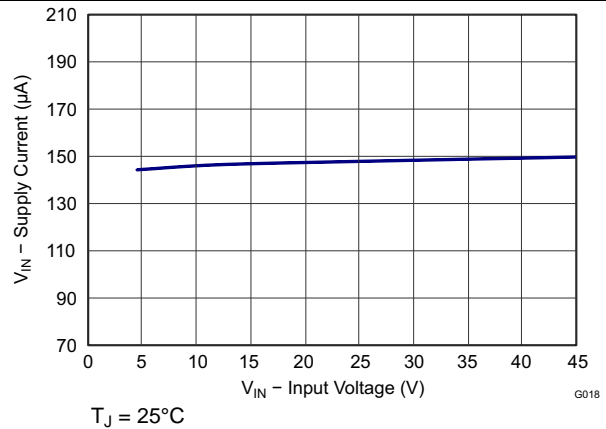


Figure 18. V_{IN} Supply Current vs Input Voltage

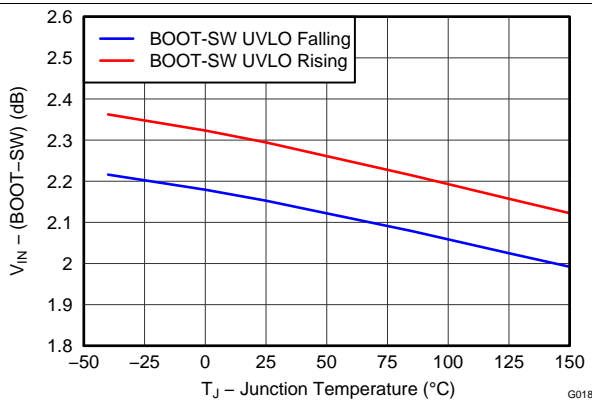


Figure 19. BOOT-SW UVLO vs Junction Temperature

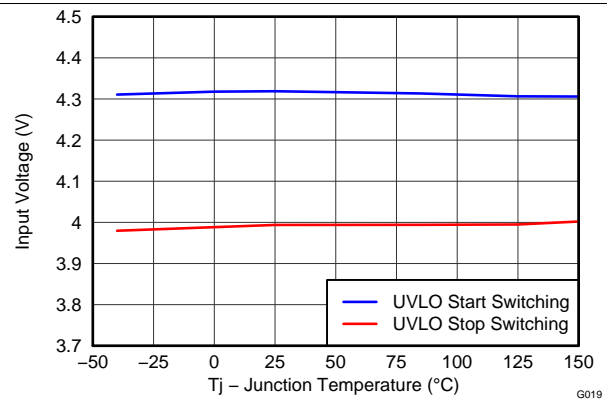


Figure 20. Input Voltage UVLO vs Junction Temperature

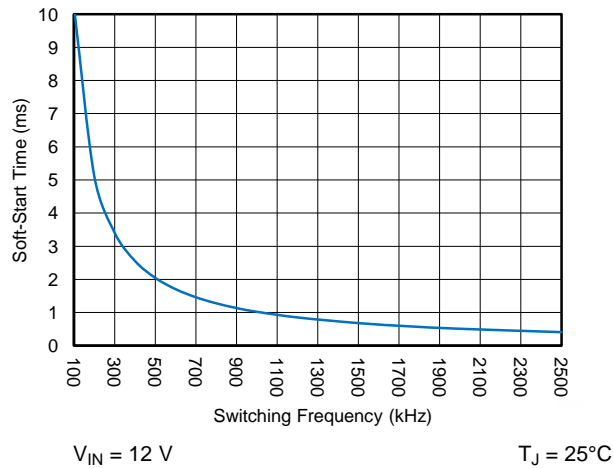


Figure 21. Soft-Start Time vs Switching Frequency

7 Detailed Description

7.1 Overview

The TPS54340 is a 42 V, 3.5 A, step-down (buck) regulator with an integrated high side n-channel MOSFET. The device implements constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2500 kHz allows either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK terminal. The device has an internal phase-locked loop (PLL) connected to the RT/CLK terminal that will synchronize the power switch turn on to a falling edge of an external clock signal.

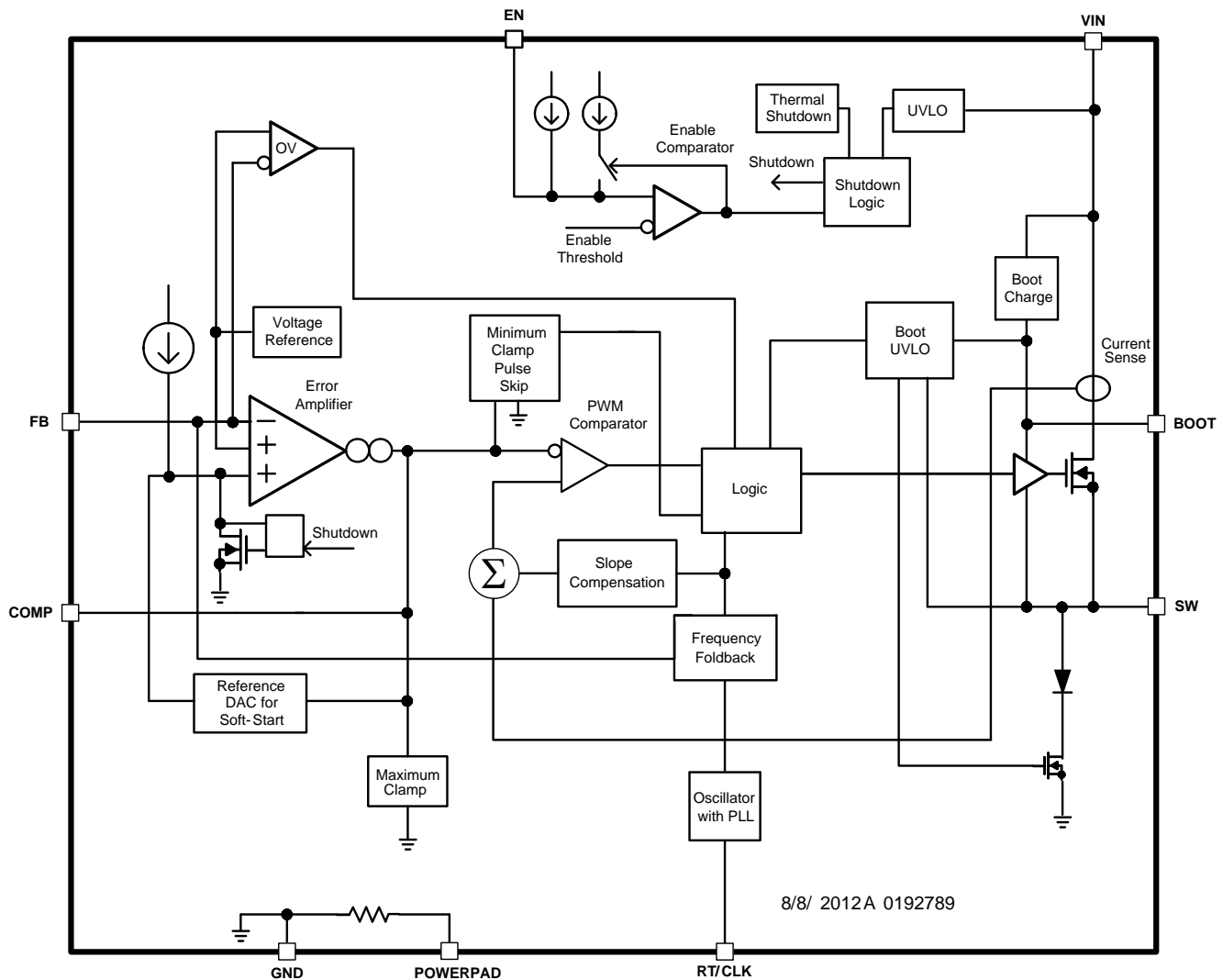
The TPS54340 has a default input start-up voltage of approximately 4.3 V. The EN terminal can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. An internal pull up current source enables operation when the EN terminal is floating. The operating current is 146 μ A under no load condition (not switching). When the device is disabled, the supply current is 1 μ A.

The integrated 92m Ω high side MOSFET supports high efficiency power supply designs capable of delivering 3.5 amperes of continuous current to a load. The gate drive bias voltage for the integrated high side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW terminals. The TPS54340 reduces the external component count by integrating the bootstrap recharge diode. The BOOT terminal capacitor voltage is monitored by a UVLO circuit which turns off the high side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54340 to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8 V feedback reference.

Output overvoltage transients are minimized by an Overvoltage Transient Protection (OVP) comparator. When the OVP comparator is activated, the high side MOSFET is turned off and remains off until the output voltage is less than 106% of the desired output voltage.

The TPS54340 includes an internal soft-start circuit that slows the output rise time during start-up to reduce in-rush current and output voltage overshoot. Output overload conditions reset the soft-start timer. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help maintain control of the inductor current.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54340 uses fixed frequency, peak current mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB terminal to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output at the COMP terminal controls the high side power switch current. When the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP terminal voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP terminal voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP terminal.

7.3.2 Slope Compensation Output Current

The TPS54340 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

Feature Description (continued)

7.3.3 Pulse Skip Eco-mode

The TPS54340 operates in a pulse skipping Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters Eco-mode. The pulse skipping current threshold is the peak switch current level corresponding to a nominal COMP voltage of 600 mV.

When in Eco-mode, the COMP terminal voltage is clamped at 600 mV and the high side MOSFET is inhibited. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP terminal voltage. The high side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-mode pulse skipping threshold at which time the device again enters Eco-mode. The internal PLL remains operational when in Eco-mode. When operating at light load currents in Eco-mode, the switching transitions occur synchronously with the external clock signal.

During Eco-mode operation, the TPS54340 senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters Eco-mode is dependent on the output inductor value. The circuit in [Figure 32](#) enters Eco-mode at about 31.4 mA output current. As the load current approaches zero, the device enters a pulse skip mode during which it draws only 146 μ A input quiescent current.

7.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54340 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW terminals provides the gate drive voltage for the high side MOSFET. The BOOT capacitor is refreshed when the high side MOSFET is off and the external low side diode conducts. The recommended value of the BOOT capacitor is 0.1 μ F. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high side MOSFET of the TPS54340 will operate at 100% duty cycle as long as the BOOT to SW terminal voltage is greater than 2.1V. When the voltage from BOOT to SW drops below 2.1V, the high side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low side MOSFET at high output voltages, it is disabled at 24 V output and re-enabled when the output reaches 21.5 V.

Since the gate drive current sourced from the BOOT capacitor is small, the high side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

[Equation 1](#) calculates the minimum input voltage required to regulate the output voltage and ensure normal operation of the device. This calculation must include tolerance of the component specifications and the variation of these specifications at their maximum operating temperature in the application

$$V_{IN}(\text{min}) = \frac{V_{OUT} + V_F + R_{dc} \times I_{OUT}}{0.99} + R_{DS(on)} \times I_{OUT} - V_F$$

where

- V_F = Schottky diode forward voltage
- R_{dc} = DC resistance of inductor and PCB
- $R_{DS(on)}$ = High-side MOSFET $R_{DS(on)}$

(1)

Feature Description (continued)

At heavy loads, the minimum input voltage must be increased to ensure a monotonic startup. Equation 2 can be used to calculate the minimum input voltage for this condition.

$$V_{OUT(max)} = D_{(max)} \times (V_{IN(min)} - I_{OUT(max)} \times R_{DS(on)} + V_F) - V_F + I_{OUT(max)} \times R_{dc}$$

where

- $D_{(max)} \geq 0.9$
- $IB2SW = 100 \mu A$
- $TSW = 1 / F_{sw}$
- $VB2SW = V_{BOOT} + V_F$
- $V_{BOOT} = (1.41 \times V_{IN} - 0.554 - V_F / TSW - 1.847 \times 10^3 \times IB2SW) / (1.41 + 1 / Tsw)$
- $R_{DS(on)} = 1 / (-0.3 \times VB2SW^2 + 3.577 \times VB2SW - 4.246)$ (2)

7.3.5 Error Amplifier

The TPS54340 voltage regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB terminal voltage to the lower of the internal soft-start voltage or the internal 0.8 V voltage reference. The transconductance (gm) of the error amplifier is 350 $\mu A/V$ during normal operation. During soft-start operation, the transconductance is reduced to 78 $\mu A/V$ and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor and capacitor) are connected between the error amplifier output COMP terminal and GND terminal.

7.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8 V $\pm 1\%$ voltage reference over the operating temperature and voltage range by scaling the output of a bandgap reference circuit. The output voltage is set by a resistor divider from the output node to the FB terminal. It is recommended to use 1% tolerance or better divider resistors. Select the low side resistor R_{LS} for the desired divider current and use Equation 3 to calculate R_{HS} . To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{V_{out} - 0.8V}{0.8V} \right) \quad (3)$$

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54340 is enabled when the VIN terminal voltage rises above 4.3 V and the EN terminal voltage exceeds the enable threshold of 1.2 V. The TPS54340 is disabled when the VIN terminal voltage falls below 4 V or when the EN terminal voltage is below 1.2 V. The EN terminal has an internal pull-up current source, I1, of 1.2 μA that enables operation of the TPS54340 when the EN terminal floats.

If an application requires a higher undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 22 to adjust the input voltage UVLO with two external resistors. When the EN terminal voltage exceeds 1.2 V, an additional 3.4 μA of hysteresis current, I_{hys}, is sourced out of the EN terminal. When the EN terminal is pulled below 1.2 V, the 3.4 μA I_{hys} current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use Equation 4 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use Equation 5 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (e.g., 4.5 V) and withstand high input voltages (e.g., 40 V), the EN terminal may experience a voltage greater than the absolute maximum voltage of 8.4 V during the high input voltage condition. It is recommended to use a zener diode to clamp the terminal voltage below the absolute maximum rating.

Feature Description (continued)

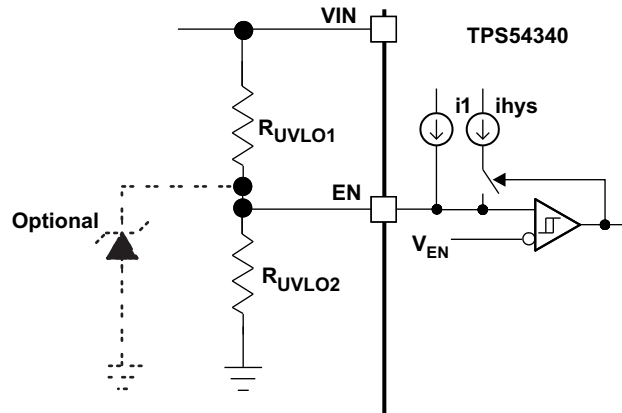


Figure 22. Adjustable Undervoltage Lockout (UVLO)

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (4)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \quad (5)$$

7.3.8 Internal Soft-Start

The TPS54340 has an internal digital soft-start that ramps the reference voltage from zero volts to its final value in 1024 switching cycles. The internal soft-start time (10% to 90%) is calculated using Equation 6.

$$t_{SS}(\text{ms}) = \frac{1024}{f_{SW}(\text{kHz})} \quad (6)$$

If the EN terminal is pulled below the stop threshold of 1.2 V, switching stops and the internal soft-start resets. The soft-start also resets in thermal shutdown.

7.3.9 Constant Switching Frequency and Timing Resistor (RT/CLK) Terminal)

The switching frequency of the TPS54340 is adjustable over a wide range from 100 kHz to 2500 kHz by placing a resistor between the RT/CLK terminal and GND terminal. The RT/CLK terminal voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 7 or Equation 8 or the curves in Figure 5 and Figure 6. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 135 ns which limits the maximum operating frequency in applications with high input to output step down ratios. The maximum switching frequency is also limited by the frequency foldback circuit. A more detailed discussion of the maximum switching frequency is provided in the next section.

$$R_T(\text{k}\Omega) = \frac{101756}{f_{SW}(\text{kHz})^{1.008}} \quad (7)$$

$$f_{SW}(\text{kHz}) = \frac{92417}{R_T(\text{k}\Omega)^{0.991}} \quad (8)$$

Feature Description (continued)

7.3.10 Accurate Current Limit Operation and Maximum Switching Frequency

The TPS54340 implements peak current mode control in which the COMP terminal voltage controls the peak current of the high side MOSFET. A signal proportional to the high side switch current and the COMP terminal voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP terminal high. The error amplifier output is clamped internally at a level which sets the peak switch current limit. The TPS54340 provides an accurate current limit threshold with a typical current limit delay of 60 ns. With smaller inductor values, the delay will result in a higher peak inductor current. The relationship between the inductor value and the peak inductor current is shown in [Figure 23](#).

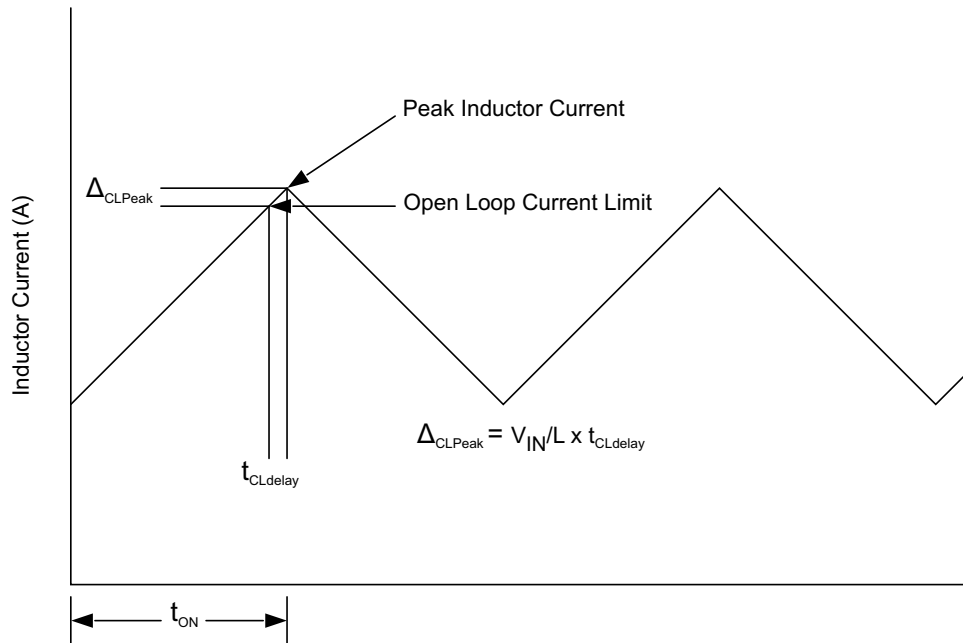


Figure 23. Current Limit Delay

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54340 implements a frequency foldback. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB terminal voltage falls from 0.8 V to 0 V. The TPS54340 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. [Equation 10](#) calculates the maximum switching frequency at which the inductor current will remain under control when V_{OUT} is forced to $V_{OUT(SC)}$. The selected operating frequency should not exceed the calculated value.

[Equation 9](#) calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required at maximum input voltage.

$$f_{SW(max\ skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right) \quad (9)$$

Feature Description (continued)

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right) \tag{10}$$

- I_o** Output current
- I_{CL}** Current limit
- R_{dc}** inductor resistance
- V_{IN}** maximum input voltage
- V_{OUT}** output voltage
- V_{OUTSC}** output voltage during short
- V_d** diode voltage drop
- R_{DS(on)}** switch on resistance
- t_{ON}** controllable on time
- f_{DIV}** frequency divide equals (1, 2, 4, or 8)

7.3.11 Synchronization to RT/CLK Terminal

The RT/CLK terminal can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature connect a square wave to the RT/CLK terminal through either circuit network shown in Figure 24. The square wave applied to the RT/CLK terminal must switch lower than 0.5 V and higher than 1.7 V and have a pulsewidth greater than 15 ns. The synchronization frequency range is 160 kHz to 2300 kHz. The rising edge of the SW will be synchronized to the falling edge of RT/CLK terminal signal. The external synchronization circuit should be designed such that the default frequency set resistor is connected from the RT/CLK terminal to ground when the synchronization signal is off. When using a low impedance signal source, the frequency set resistor is connected in parallel with an ac coupling capacitor to a termination resistor (e.g., 50 Ω) as shown in Figure 24. The two resistors in series provide the default frequency setting resistance when the signal source is turned off. The sum of the resistance should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10 pF ceramic capacitor to RT/CLK terminal.

The first time the RT/CLK is pulled above the PLL threshold the TPS54340 switches from the RT resistor free-running frequency mode to the PLL synchronized mode. The internal 0.5 V voltage source is removed and the RT/CLK terminal becomes high impedance as the PLL starts to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and locks onto the external clock frequency within 78 microseconds. During the transition from the PLL mode to the resistor programmed mode, the switching frequency will fall to 150 kHz and then increase or decrease to the resistor programmed frequency when the 0.5 V bias voltage is reapplied to the RT/CLK resistor.

The switching frequency is divided by 8, 4, 2, and 1 as the FB terminal voltage ramps from 0 to 0.8 volts. The device implements a digital frequency foldback to enable synchronizing to an external clock during normal start-up and fault conditions. Figure 25, Figure 26 and Figure 27 show the device synchronized to an external system clock in continuous conduction mode (CCM), discontinuous conduction (DCM), and pulse skip mode (Eco-Mode).

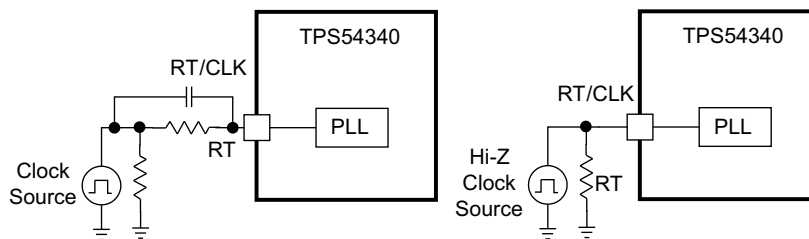
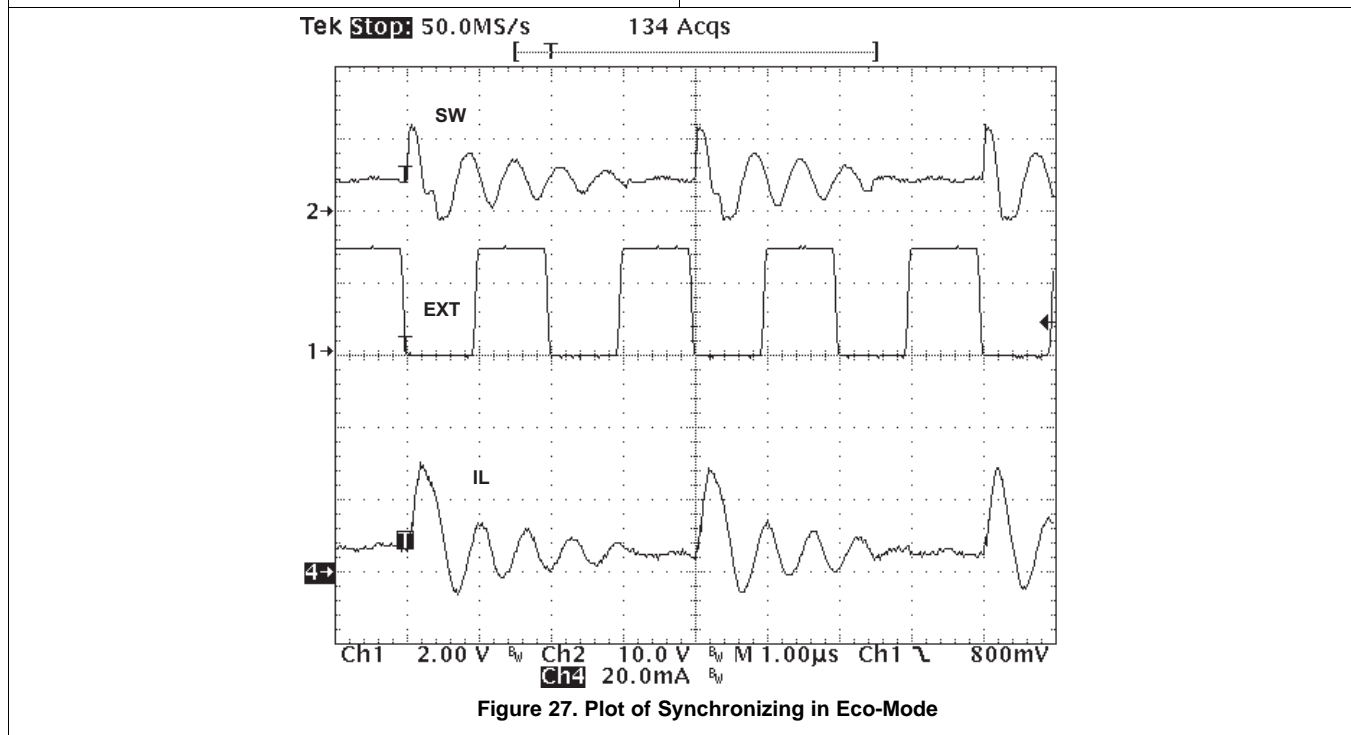
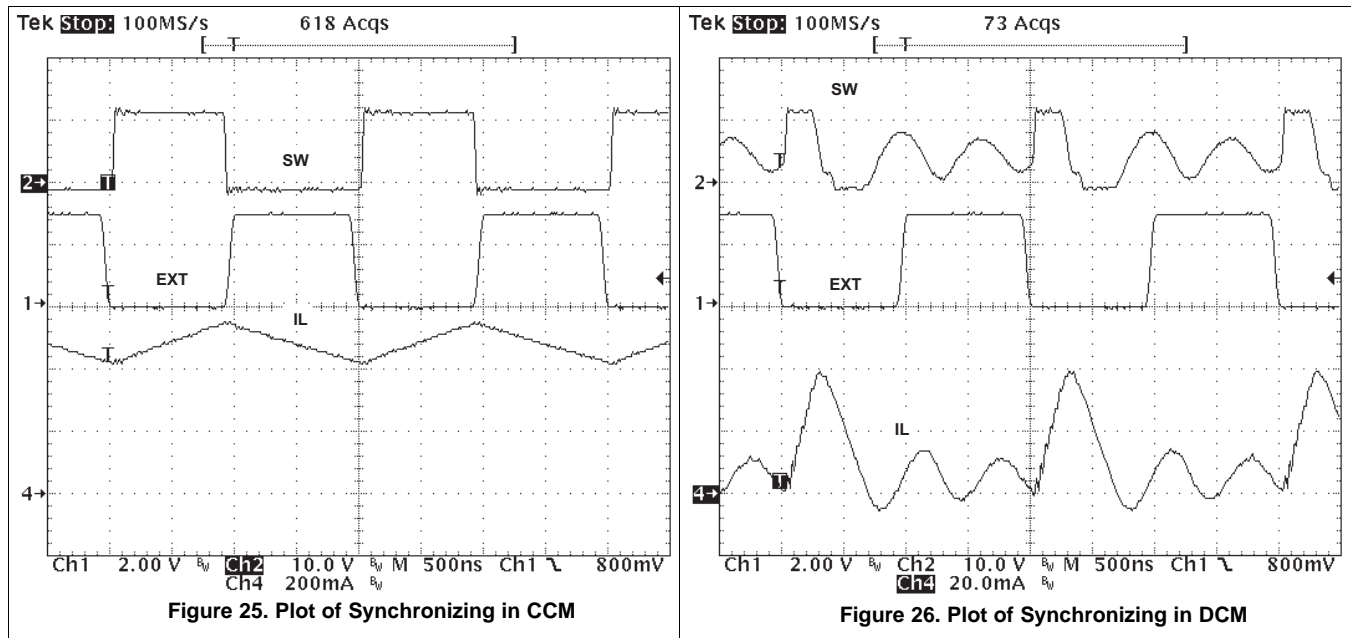


Figure 24. Synchronizing to a System Clock

Feature Description (continued)

7.3.12 Overvoltage Protection

The TPS54340 incorporates an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB terminal voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will increase to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power supply output voltage can increase faster than the response of the error amplifier output resulting in an output overshoot.

Feature Description (continued)

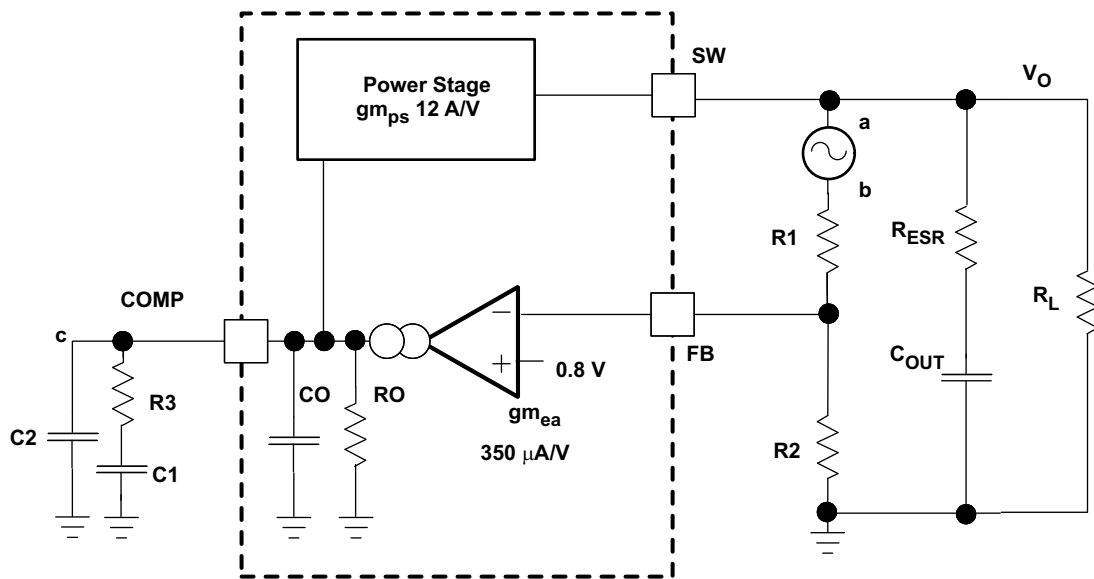
The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB terminal voltage to the rising OVP threshold which is nominally 109% of the internal voltage reference. If the FB terminal voltage is greater than the rising OVP threshold, the high side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high side MOSFET resumes normal operation.

7.3.13 Thermal Shutdown

The TPS54340 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

7.3.14 Small Signal Model for Loop Response

Figure 28 shows an equivalent model for the TPS54340 control loop which can be simulated to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a $g_{m_{EA}}$ of 3350 $\mu A/V$. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_o and capacitor C_o model the open loop gain and frequency response of the amplifier. The 1mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a provides the small signal response of the frequency compensation. Plotting a/b provides the small signal response of the overall loop. The dynamic loop response can be evaluated by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode (CCM) operation.



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Figure 28. Small Signal Model for Loop Response

7.3.15 Simple Small Signal Model for Peak Current Mode Control

Figure 29 describes a simple small signal model that can be used to design the frequency compensation. The TPS54340 power stage can be approximated by a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 11 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP terminal voltage (node c in Figure 28) is the power stage transconductance, $g_{m_{PS}}$. The $g_{m_{PS}}$ for the TPS54340 is 12 A/V. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 12.

Feature Description (continued)

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 13). The combined effect is highlighted by the dashed line in the right half of Figure 29. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin is increased by the ESR zero of the output capacitor (see Equation 14).

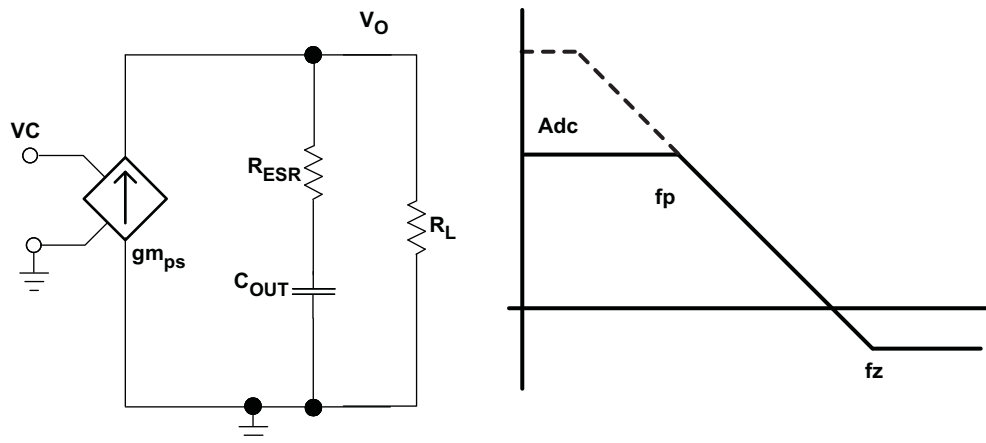


Figure 29. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{V_C} = A_{dc} \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (11)$$

$$A_{dc} = gm_{ps} \times R_L \quad (12)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (13)$$

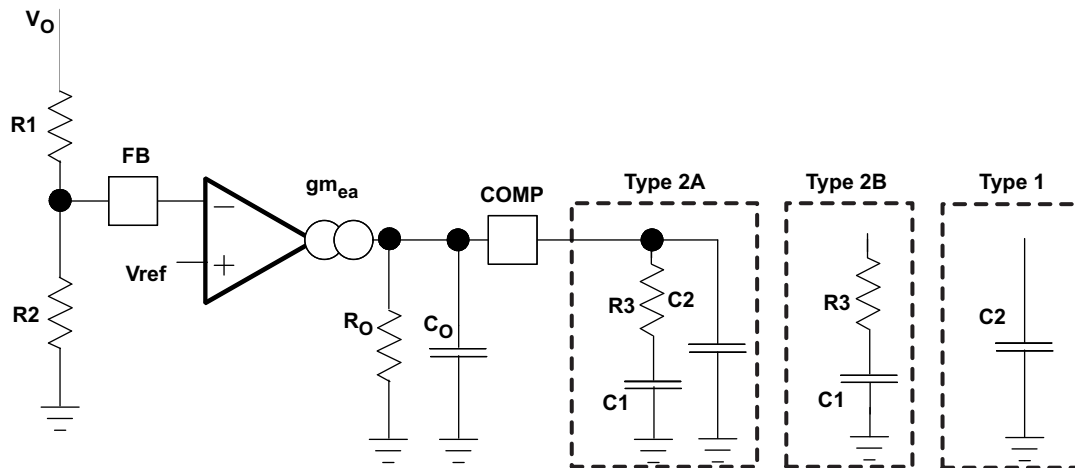
$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (14)$$

7.3.16 Small Signal Model for Frequency Compensation

The TPS54340 uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 30. Type 2 circuits are typically implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 15 and Equation 16 relate the frequency response of the amplifier to the small signal model in Figure 30. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 30. See the application section for a design example using a Type 2A network with a low ESR output capacitor.

Equation 15 through Equation 24 are provided as a reference. An alternative is to use WEBENCH software tools to create a design based on the power supply requirements.

Feature Description (continued)



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Figure 30. Types of Frequency Compensation

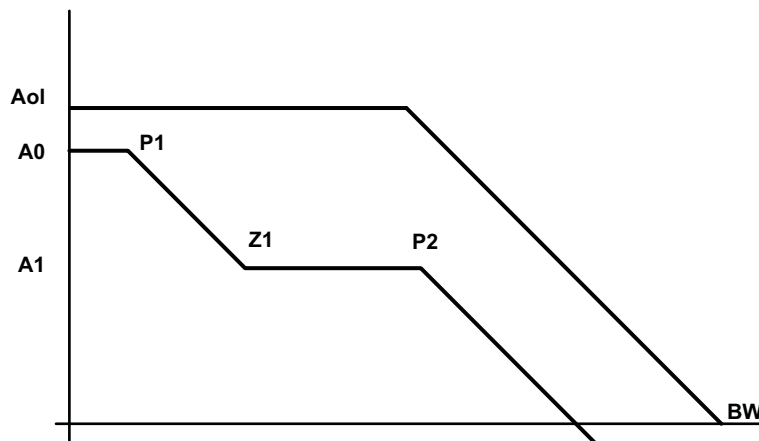


Figure 31. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$R_o = \frac{A_{ol}(V/V)}{g_{m_{ea}}} \quad (15)$$

$$C_o = \frac{g_{m_{ea}}}{2\pi \times BW \text{ (Hz)}} \quad (16)$$

$$EA = A_0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad (17)$$

$$A_0 = g_{m_{ea}} \times R_o \times \frac{R_2}{R_1 + R_2} \quad (18)$$

$$A_1 = g_{m_{ea}} \times R_o || R_3 \times \frac{R_2}{R_1 + R_2} \quad (19)$$

$$P_1 = \frac{1}{2\pi \times R_o \times C_1} \quad (20)$$

Feature Description (continued)

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (21)$$

$$P2 = \frac{1}{2\pi \times R3 \parallel R_O \times (C2 + C_O)} \text{ type 2a} \quad (22)$$

$$P2 = \frac{1}{2\pi \times R3 \parallel R_O \times C_O} \text{ type 2b} \quad (23)$$

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{ type 1} \quad (24)$$

7.4 Device Functional Modes

7.4.1 Operation with $V_{IN} < 4.5 \text{ V}$ (Minimum V_{IN})

The device is recommended to operate with input voltages above 4.5 V. The typical V_{IN} UVLO threshold is 4.3 V and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device will not switch. If EN is externally pulled up to V_{IN} or left floating, when V_{IN} passes the UVLO threshold the device will become active. Switching is enabled the soft start sequence is initiated. The TPS54340 will start at the soft start time determined by the internal soft start time.

7.4.2 Operation with EN Control

The enable threshold voltage is 1.2 V typical. With EN held below that voltage the device is disabled and switching is inhibited even if V_{IN} is above its UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage is increased above the threshold while V_{IN} is above its UVLO threshold, the device becomes active. Switching is enabled, and the soft start sequence is initiated. The TPS54340 will start at the soft start time determined by the internal soft start time.

8 Application and Implementation

NOTE

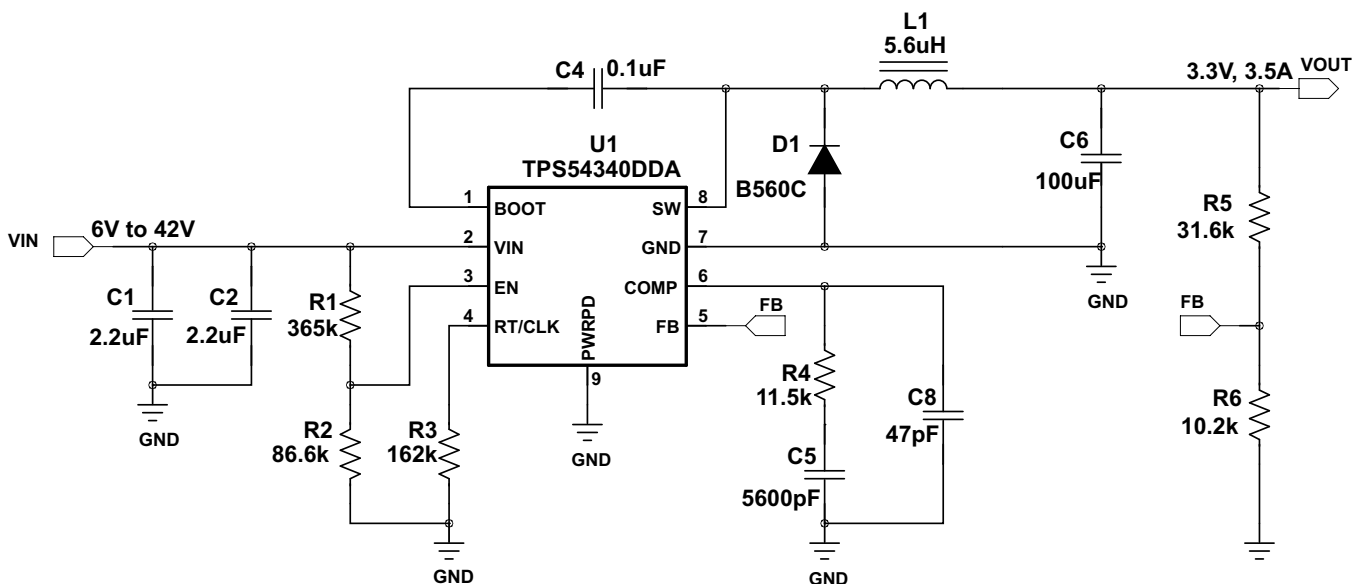
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54340 is a 42 V, 3.5 A, step down regulator with an integrated high side MOSFET. Idea applications are: 12 V, 24 V Industrial, Automotive and Communications Power Systems.

8.2 Typical Applications

8.2.1 Buck Converter



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Figure 32. 3.3 V Output TPS54340 Design Example

8.2.1.1 Design Requirements

This guide illustrates the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. For this example, we will start with the following known parameters:

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Output Voltage	3.3 V
Transient Response 0.875 A to 2.625 A load step	$\Delta V_{OUT} = 4\%$
Maximum Output Current	3.5 A
Input Voltage	12 V nom. 6 V to 42 V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	5.75 V
Stop Input Voltage (falling VIN)	4.5 V

8.2.1.2 Detailed Design Procedures

8.2.1.2.1 Custom Design with WEBENCH Tools

[Click here](#) to create a custom design using the TPS54340 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN} , V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
 - Run electrical simulations to see important waveforms and circuit performance,
 - Run thermal simulations to understand the thermal performance of your board,
 - Export your customized schematic and layout into popular CAD formats,
 - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.1.2.2 Selecting the Switching Frequency

The first step is to choose a switching frequency for the regulator. Typically, the designer uses the highest switching frequency possible since this produces the smallest solution size. High switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage and the frequency foldback protection.

[Equation 9](#) and [Equation 10](#) should be used to calculate the upper limit of the switching frequency for the regulator. Choose the lower value result from the two equations. Switching frequencies higher than these values results in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin} , is 135 ns for the TPS54340. For this example, the output voltage is 3.3 V and the maximum input voltage is 42 V, which allows for a maximum switch frequency up to 712 kHz to avoid pulse skipping from [Equation 9](#). To ensure overcurrent runaway is not a concern during short circuits use [Equation 10](#) to determine the maximum switching frequency for frequency foldback protection. With a maximum input voltage of 42 V, assuming a diode voltage of 0.7 V, inductor resistance of 21 mΩ, switch resistance of 92 mΩ, a current limit value of 4.7 A and short circuit output voltage of 0.1 V, the maximum switching frequency is 1260 kHz.

For this design, a lower switching frequency of 600 kHz is chosen to operate comfortably below the calculated maximums. To determine the timing resistance for a given switching frequency, use [Equation 7](#) or the curve in [Figure 6](#). The switching frequency is set by resistor R_3 shown in [Figure 32](#). For 600 kHz operation, the closest standard value resistor is 162 kΩ.

$$f_{SW(maxskip)} = \frac{1}{135ns} \times \left(\frac{3.5 A \times 21 m\Omega + 3.3 V + 0.7 V}{42 V - 3.5 A \times 92 m\Omega + 0.7 V} \right) = 712 \text{ kHz} \quad (25)$$

$$f_{SW(shift)} = \frac{8}{135 ns} \times \left(\frac{4.7 A \times 21 m\Omega + 0.1 V + 0.7 V}{42 V - 4.7 A \times 92 m\Omega + 0.7 V} \right) = 1260 \text{ kHz} \quad (26)$$

$$RT (k\Omega) = \frac{101756}{600 (kHz)^{1.008}} = 161 \text{ k}\Omega \quad (27)$$

8.2.1.2.3 Output Inductor Selection (L_o)

To calculate the minimum value of the output inductor, use [Equation 28](#).

K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as $K_{IND} = 0.3$ may be desirable. When using higher ESR output capacitors, $K_{IND} = 0.2$ yields better results. Since the inductor ripple current is part of the current mode PWM control system, the inductor ripple current should always be greater than 150 mA for stable PWM operation. In a wide input voltage regulator, it is best to choose relatively large inductor ripple current. This provides sufficient ripple current with the input voltage at the minimum.

For this design example, $K_{IND} = 0.3$ and the minimum inductor value is calculated to be 4.8 μH . The nearest standard value is 5.6 μH . It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from [Equation 30](#) and [Equation 31](#). For this design, the RMS inductor current is 3.5 A and the peak inductor current is 3.95 A. The chosen inductor is a WE 7443552560, which has a saturation current rating of 7.5 A and an RMS current rating of 6.7 A.

As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch current limit of the TPS54340 which is nominally 5.5 A.

$$L_{O(\min)} = \frac{V_{IN(\max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(\max)} \times f_{SW}} = \frac{42 \text{ V} - 3.3 \text{ V}}{3.5 \text{ A} \times 0.3} \times \frac{3.3 \text{ V}}{42 \text{ V} \times 600 \text{ kHz}} = 4.8 \mu\text{H} \quad (28)$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(\max)} - V_{OUT})}{V_{IN(\max)} \times L_O \times f_{SW}} = \frac{3.3 \text{ V} \times (42 \text{ V} - 3.3 \text{ V})}{42 \text{ V} \times 5.6 \mu\text{H} \times 600 \text{ kHz}} = 0.905 \text{ A} \quad (29)$$

$$I_{L(\text{rms})} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(\max)} - V_{OUT})}{V_{IN(\max)} \times L_O \times f_{SW}} \right)^2} = \sqrt{(3.5 \text{ A})^2 + \frac{1}{12} \times \left(\frac{3.3 \text{ V} \times (42 \text{ V} - 3.3 \text{ V})}{42 \text{ V} \times 5.6 \mu\text{H} \times 600 \text{ kHz}} \right)^2} = 3.5 \text{ A} \quad (30)$$

$$I_{L(\text{peak})} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 3.5 \text{ A} + \frac{0.905 \text{ A}}{2} = 3.95 \text{ A} \quad (31)$$

8.2.1.2.4 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for 2 clock cycles to maintain the output voltage within the specified range. [Equation 32](#) shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, f_{sw} is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0.875 A to 2.625 A. Therefore, ΔI_{OUT} is 2.625 A - 0.875 A = 1.75 A and $\Delta V_{OUT} = 0.04 \times 3.3 = 0.13 \text{ V}$. Using these numbers gives a minimum capacitance of 44.9 μF . This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be included in load step calculations.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator can not sink current so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. A typical load step response is shown in Figure [Figure 33](#). The excess energy absorbed in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. [Equation 33](#) calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where L_O is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the peak output voltage, and V_i is the initial voltage. For this example, the worst case load step will be from 2.625 A to 0.875 A. The output voltage increases during this load transition and the stated maximum in our specification is 4 % of the output voltage. This makes $V_f = 1.04 \times 3.3 = 3.432$. V_i is the initial capacitor voltage which is the nominal output voltage of 3.3 V. Using these numbers in [Equation 33](#) yields a minimum capacitance of 38.6 μF .

[Equation 34](#) calculates the minimum output capacitance needed to meet the output voltage ripple specification, where f_{sw} is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. [Equation 34](#) yields 11.4 μF .

[Equation 35](#) calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. [Equation 35](#) indicates the ESR should be less than 18 $\text{m}\Omega$.

The most stringent criteria for the output capacitor is 44.9 μF required to maintain the output voltage within regulation tolerance during a load transient.

Capacitance de-ratings for aging, temperature and dc bias increases this minimum value. For this example, 100 μF ceramic capacitors with 5 $\text{m}\Omega$ of ESR is used. The derated capacitance is 70 μF , well above the minimum required capacitance of 44.9 μF .

Capacitors are generally rated for a maximum ripple current that can be filtered without degrading capacitor reliability. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. [Equation 36](#) can be used to calculate the RMS ripple current that the output capacitor must support. For this example, [Equation 36](#) yields 261 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 1.75 \text{ A}}{600 \text{ kHz} \times 0.13 \text{ V}} = 44.9 \mu\text{F} \quad (32)$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2 \right)}{\left((V_f)^2 - (V_i)^2 \right)} = 5.6 \mu\text{H} \times \frac{\left(2.625 \text{ A}^2 - 0.875 \text{ A}^2 \right)}{\left(3.432 \text{ V}^2 - 3.3 \text{ V}^2 \right)} = 38.6 \mu\text{F} \quad (33)$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{ORIPPLE}}{I_{RIPPLE}} \right)} = \frac{1}{8 \times 600 \text{ kHz}} \times \frac{1}{\left(\frac{16.5 \text{ mV}}{0.905 \text{ A}} \right)} = 11.4 \mu\text{F} \quad (34)$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} = \frac{16.5 \text{ mV}}{0.905 \text{ A}} = 18 \text{ m}\Omega \quad (35)$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT} \right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} = \frac{3.3 \text{ V} \times (42 \text{ V} - 3.3 \text{ V})}{\sqrt{12} \times 42 \text{ V} \times 5.6 \mu\text{H} \times 600 \text{ kHz}} = 261 \text{ mA} \quad (36)$$

8.2.1.2.5 Catch Diode

The TPS54340 requires an external catch diode between the SW terminal and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 42 V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the TPS54340.

For the example design, the B560C-13-F Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the B560C-13-F is 0.70 volts at 5 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 37 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The B560C-13-F diode has a junction capacitance of 300 pF. Using Equation 37, the total loss in the diode is 2.42 Watts.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN(max)} - V_{OUT}) \times I_{OUT} \times V_{fd}}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times (V_{IN} + V_{fd})^2}{2} = \frac{(42 \text{ V} - 3.3 \text{ V}) \times 3.5 \text{ A} \times 0.7 \text{ V}}{42 \text{ V}} + \frac{300 \text{ pF} \times 600 \text{ kHz} \times (42 \text{ V} + 0.7 \text{ V})^2}{2} = 2.42 \text{ W} \quad (37)$$

8.2.1.2.6 Input Capacitor

The TPS54340 requires a high quality ceramic type X5R or X7R input decoupling capacitor with at least 3 μF of effective capacitance. Some applications will benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance due to dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54340. The input ripple current can be calculated using Equation 38.

The value of a ceramic capacitor varies significantly with temperature and the dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is more stable over temperature. X5R and X7R ceramic dielectrics are usually selected for switching regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with consideration for the dc bias. The effective value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 42 V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V. For this example, two 2.2 μF , 100 V capacitors in parallel are used. Table 2 shows several choices of high voltage capacitors.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 39. Using the design example values, $I_{OUT} = 3.5 \text{ A}$, $C_{IN} = 4.4 \mu\text{F}$, $f_{SW} = 600 \text{ kHz}$, yields an input voltage ripple of 331 mV and a rms input ripple current of 1.74 A.

$$I_{C(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} = 3.5 \text{ A} \times \sqrt{\frac{3.3 \text{ V}}{6 \text{ V}} \times \frac{(6 \text{ V} - 3.3 \text{ V})}{6 \text{ V}}} = 1.74 \text{ A} \quad (38)$$

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} = \frac{3.5 \text{ A} \times 0.25}{4.4 \mu\text{F} \times 600 \text{ kHz}} = 331 \text{ mV} \quad (39)$$

Table 2. Capacitor Types

VALUE (μF)	EIA Size	VOLTAGE	DIELECTRIC	COMMENTS	
1 to 2.2	1210	100 V	X7R	GRM32 series	
1 to 4.7		50 V			
1	1206	100 V		GRM31 series	
1 to 2.2		50 V			
1 to 1.8	2220	50 V		VJ X7R series	
1 to 1.2		100 V			
1 to 3.9	2225	50 V			
1 to 1.8		100 V			
1 to 2.2	1812	100 V			C series C4532
1.5 to 6.8		50 V			
1 to 2.2	1210	100 V		C series C3225	
1 to 3.3		50 V			
1 to 4.7	1210	50 V		X7R dielectric series	
1		100 V			
1 to 4.7	1812	50 V			
1 to 2.2		100 V			

8.2.1.2.7 Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor must be connected between the BOOT and SW terminals for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10 V or higher voltage rating.

8.2.1.2.8 Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) can be adjusted using an external voltage divider on the EN terminal of the TPS54340. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.75 V (UVLO start). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.5 V (UVLO stop).

Programmable UVLO threshold voltages are set using the resistor divider of R_{UVLO1} and R_{UVLO2} between V_{in} and ground connected to the EN terminal. Equation 4 and Equation 5 calculate the resistance values necessary. For the example application, a 365 kΩ between V_{in} and EN (R_{UVLO1}) and a 86.6 kΩ between EN and ground (R_{UVLO2}) are required to produce the 8 V and 6.25 V start and stop voltages.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} = \frac{5.75 \text{ V} - 4.5 \text{ V}}{3.4 \mu\text{A}} = 368 \text{ k}\Omega \quad (40)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} = \frac{1.2 \text{ V}}{\frac{5.75 \text{ V} - 1.2 \text{ V}}{365 \text{ k}\Omega} + 1.2 \mu\text{A}} = 87.8 \text{ k}\Omega \quad (41)$$

8.2.1.2.9 Output Voltage and Feedback Resistors Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, 10.2 kΩ was selected for R6. Using Equation 3, R5 is calculated as 31.9 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to the input current of the FB terminal, the current flowing through the feedback network should be greater than 1 μA to maintain the output voltage accuracy. This requirement is satisfied if the value of R6 is less than 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - 0.8 \text{ V}}{0.8 \text{ V}} = 10.2 \text{ k}\Omega \times \left(\frac{3.3 \text{ V} - 0.8 \text{ V}}{0.8 \text{ V}} \right) = 31.9 \text{ k}\Omega \quad (42)$$

8.2.1.2.10 Minimum V_{IN}

To ensure proper operation of the device and to keep the output voltage in regulation, the input voltage at the device must be above the value calculated with Equation 43. Using the typical values for the R_{HS} , R_{DC} and V_F in this application example, the minimum input voltage is 5.56 V. The BOOT-SW = 3 V curve in Figure 1 was used for $R_{DS(on)} = 0.12 \Omega$ because the device operates with low drop out. When operating with low dropout, the BOOT-SW voltage is regulated at a lower voltage because the BOOT-SW capacitor is not refreshed every switching cycle. In the final application, the values of $R_{DS(on)}$, R_{dc} and V_F used in this equation must include tolerance of the component specifications and the variation of these specifications at their maximum operating temperature in the application. In this application example the calculated minimum input voltage is near the input voltage UVLO for the TPS54340 so the device may turn off before going into drop out.

$$V_{IN(min)} = \frac{V_{OUT} + V_F + R_{dc} \times I_{OUT}}{0.99} + R_{DS(on)} \times I_{OUT} - V_F$$

$$V_{IN(min)} = \frac{3.3 \text{ V} + 0.5 \text{ V} + 0.0206 \Omega \times 3.5 \text{ A}}{0.99} + 0.12 \Omega \times 3.5 \text{ A} - 0.5 \text{ V} = 3.83 \text{ V} \quad (43)$$

8.2.1.2.11 Compensation

There are several methods to design compensation for DC-DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual crossover frequency will be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole.

To get started, the modulator pole, $f_{p(mod)}$, and the ESR zero, f_{z1} must be calculated using Equation 44 and Equation 45. For C_{OUT} , use a derated value of 70 μF . Use equations Equation 46 and Equation 47 to estimate a starting point for the crossover frequency, f_{co} . For the example design, $f_{p(mod)}$ is 2411 Hz and $f_{z(mod)}$ is 455 kHz. Equation 45 is the geometric mean of the modulator pole and the ESR zero and Equation 47 is the mean of modulator pole and the switching frequency. Equation 46 yields 33.1 kHz and Equation 47 gives 26.9 kHz. Use the lower value of Equation 46 or Equation 47 for an initial crossover frequency. For this example, the target f_{co} is 26.9 kHz.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f_{p(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{3.5 \text{ A}}{2 \times \pi \times 3.3 \text{ V} \times 70 \mu\text{F}} = 2411 \text{ Hz} \quad (44)$$

$$f_{z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2 \times \pi \times 5 \text{ m}\Omega \times 70 \mu\text{F}} = 455 \text{ kHz} \quad (45)$$

$$f_{co} = \sqrt{f_{p(mod)} \times f_{z(mod)}} = \sqrt{2411 \text{ Hz} \times 455 \text{ kHz}} = 33.1 \text{ kHz} \quad (46)$$

$$f_{co} = \sqrt{f_{p(mod)} \times \frac{f_{SW}}{2}} = \sqrt{2411 \text{ Hz} \times \frac{600 \text{ kHz}}{2}} = 26.9 \text{ kHz} \quad (47)$$

To determine the compensation resistor, R_4 , use Equation 48. Assume the power stage transconductance, g_{mps} , is 12 A/V. The output voltage, V_O , reference voltage, V_{REF} , and amplifier transconductance, g_{mea} , are 5 V, 0.8 V and 350 $\mu\text{A/V}$, respectively. R_4 is calculated to be 11.6 k Ω and a standard value of 11.5 k Ω is selected. Use Equation 49 to set the compensation zero to the modulator pole frequency. Equation 49 yields 5740 pF for compensating capacitor C_5 . 5600 pF is used for this design.

$$R_4 = \left(\frac{2 \times \pi \times f_{co} \times C_{OUT}}{g_{mps}} \right) \times \left(\frac{V_{OUT}}{V_{REF} \times g_{mea}} \right) = \left(\frac{2 \times \pi \times 26.9 \text{ kHz} \times 70 \mu\text{F}}{12 \text{ A/V}} \right) \times \left(\frac{3.3 \text{ V}}{0.8 \text{ V} \times 350 \mu\text{A/V}} \right) = 11.6 \text{ k}\Omega \quad (48)$$

$$C_5 = \frac{1}{2 \times \pi \times R_4 \times f_{p(mod)}} = \frac{1}{2 \times \pi \times 11.5 \text{ k}\Omega \times 2411 \text{ Hz}} = 5740 \text{ pF} \quad (49)$$

A compensation pole can be implemented if desired by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from Equation 50 and Equation 51 for C8 to set the compensation pole. The selected value of C8 is 47 pF for this design example.

$$C8 = \frac{C_{OUT} \times R_{ESR}}{R4} = \frac{70 \mu\text{F} \times 5 \text{ m}\Omega}{11.5 \text{ k}\Omega} = 30.4 \text{ pF} \quad (50)$$

$$C8 = \frac{1}{R4 \times f_{sw} \times \pi} = \frac{1}{11.5 \text{ k}\Omega \times 600 \text{ kHz} \times \pi} = 46.1 \text{ pF} \quad (51)$$

8.2.1.2.12 Discontinuous Conduction Mode and Eco-mode Boundary

With an input voltage of 12 V, the power supply enters discontinuous conduction mode when the output current is less than 342 mA. The power supply enters Eco-mode when the output current is lower than 31.4 mA. The input current draw is 237 μA with no load.

8.2.1.2.13 Power Dissipation

The following formulas show how to estimate the TPS54340 power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is operating in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}) and supply current (P_Q). Example calculations are shown with the 12 V typical input voltage of the design example.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}} \right) = 3.5 \text{ A}^2 \times 92 \text{ m}\Omega \times \frac{3.3 \text{ V}}{12 \text{ V}} = 0.31 \text{ W} \quad (52)$$

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times t_{rise} = 12 \text{ V} \times 600 \text{ kHz} \times 3.5 \text{ A} \times 4.9 \text{ ns} = 0.123 \text{ W} \quad (53)$$

$$P_{GD} = V_{IN} \times Q_G \times f_{SW} = 12 \text{ V} \times 3 \text{ nC} \times 600 \text{ kHz} = 0.022 \text{ W} \quad (54)$$

$$P_Q = V_{IN} \times I_Q = 12 \text{ V} \times 146 \mu\text{A} = 0.0018 \text{ W} \quad (55)$$

Where:

I_{OUT}	is the output current (A).
$R_{DS(on)}$	is the on-resistance of the high-side MOSFET (Ω).
V_{OUT}	is the output voltage (V).
V_{IN}	is the input voltage (V).
f_{sw}	is the switching frequency (Hz).
t_{rise}	is the SW terminal voltage rise time and can be estimated by $t_{rise} = V_{IN} \times 0.16 \text{ ns/V} + 3.0 \text{ ns}$.
Q_G	is the total gate charge of the internal MOSFET.
I_Q	is the operating nonswitching supply current.

Therefore,

$$P_{TOT} = P_{COND} + P_{SW} + P_{GD} + P_Q = 0.31 \text{ W} + 0.123 \text{ W} + 0.022 \text{ W} + 0.0018 \text{ W} = 0.457 \text{ W} \quad (56)$$

For given T_A ,

$$T_J = T_A + R_{TH} \times P_{TOT} \quad (57)$$

For given $T_{JMAX} = 150^\circ\text{C}$

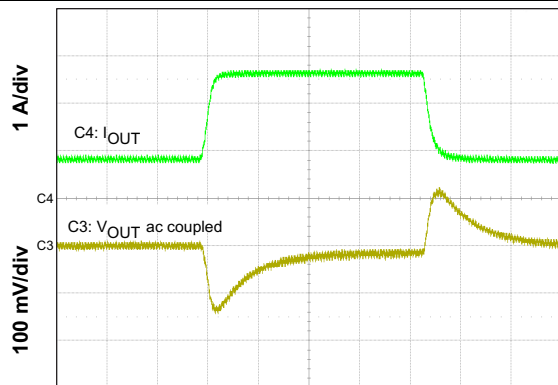
$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT} \quad (58)$$

Where:

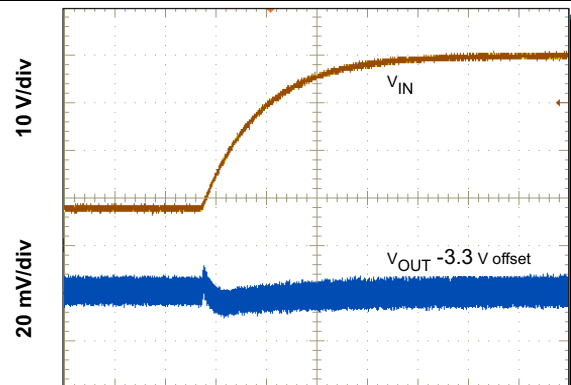
- P_{tot}** is the total device power dissipation (W),
- T_A** is the ambient temperature (°C).
- T_J** is the junction temperature (°C).
- R_{TH}** is the thermal resistance of the package (°C/W).
- T_{JMAX}** is maximum junction temperature (°C)
- T_{AMAX}** is maximum ambient temperature (°C).

There will be additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and PCB trace resistance impacting the overall efficiency of the regulator.

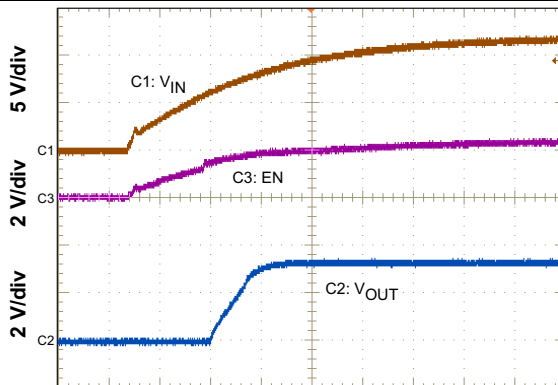
8.2.1.3 Application Curves



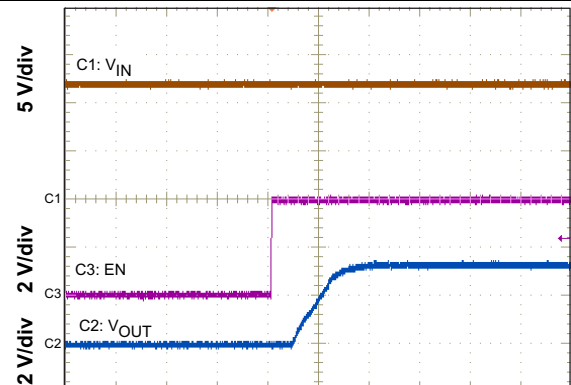
Time = 100 μ s/div
Figure 33. Load Transient



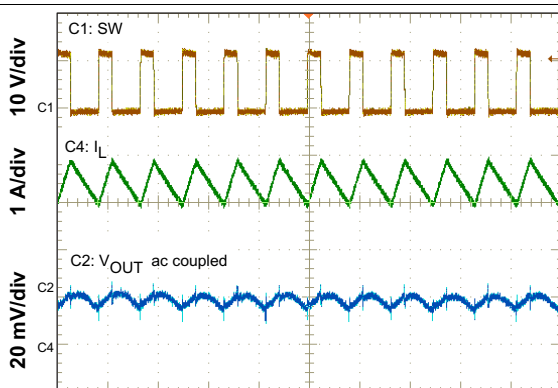
Time = 4 ms/div
Figure 34. Line Transient (8 V to 40 V)



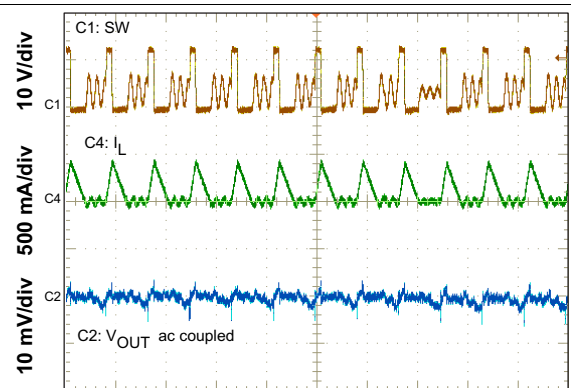
Time = 2 ms/div
Figure 35. Start-up With VIN



Time = 2 ms/div
Figure 36. Start-up With EN



Time = 2 μ s/div
 $I_{OUT} = 3.5$ A
Figure 37. Output Ripple CCM



Time = 2 μ s/div
 $I_{OUT} = 100$ mA
Figure 38. Output Ripple DCM

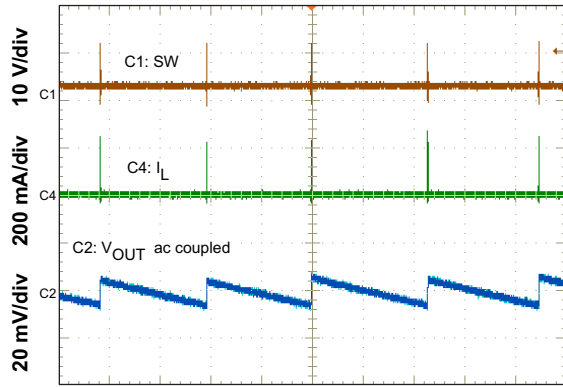


Figure 39. Output Ripple PSM

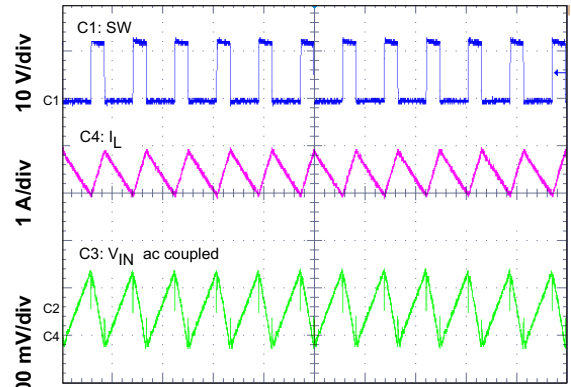


Figure 40. Input Ripple CCM

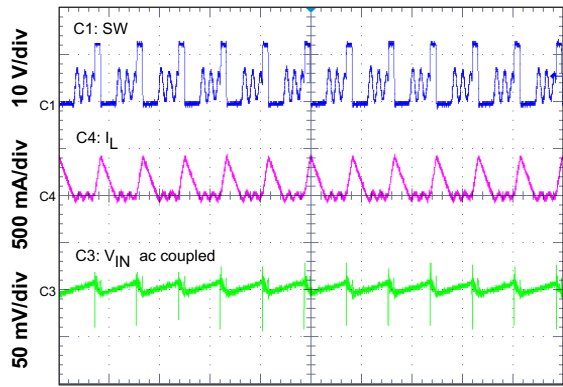


Figure 41. Input Ripple DCM

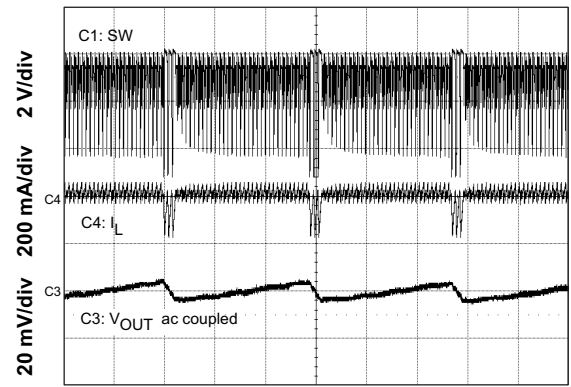


Figure 42. Low Dropout Operation

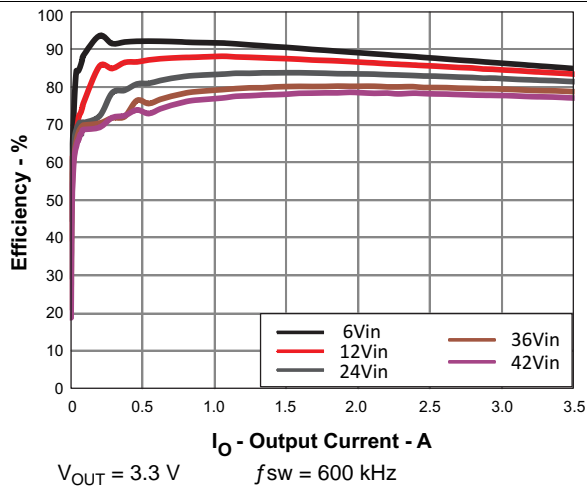


Figure 43. Efficiency vs Load Current

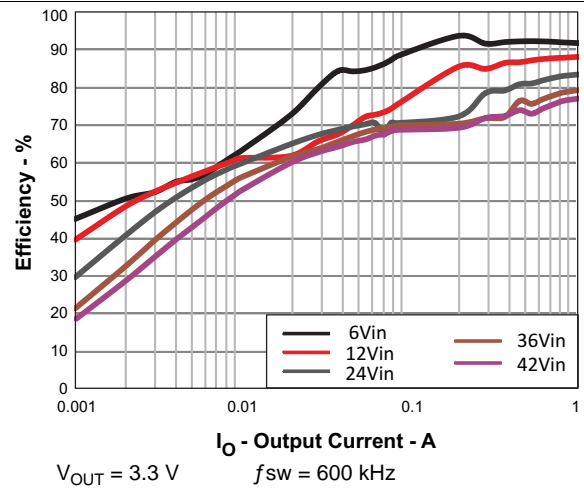


Figure 44. Light Load Efficiency

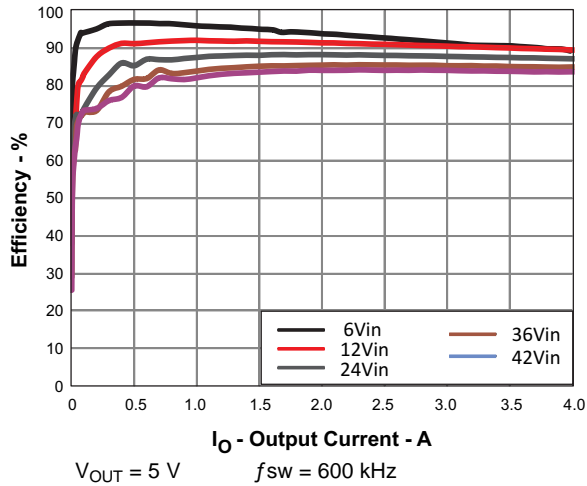


Figure 45. Efficiency vs Load Current

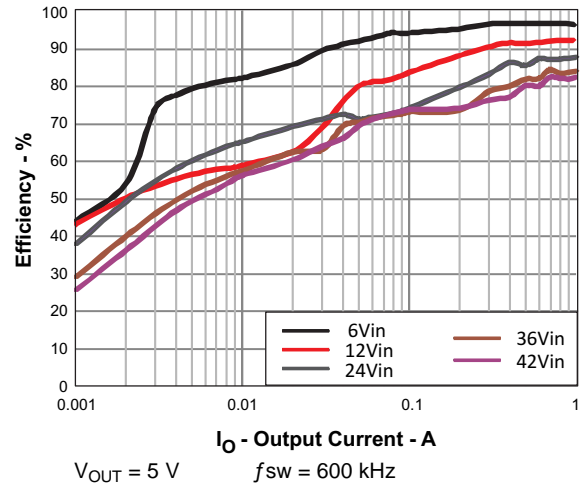


Figure 46. Light Load Efficiency

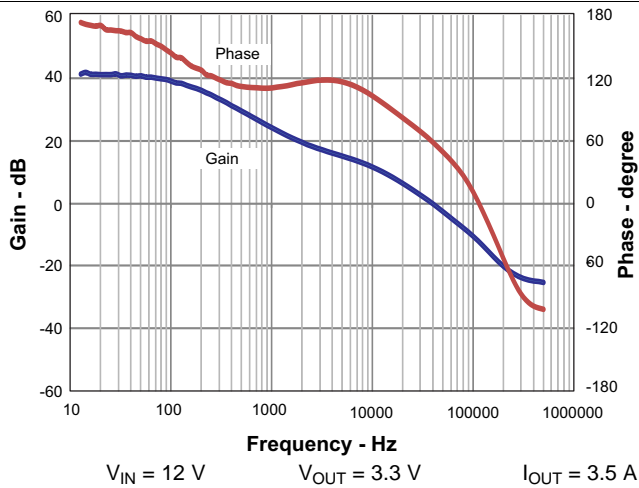


Figure 47. Overall Loop Frequency Response

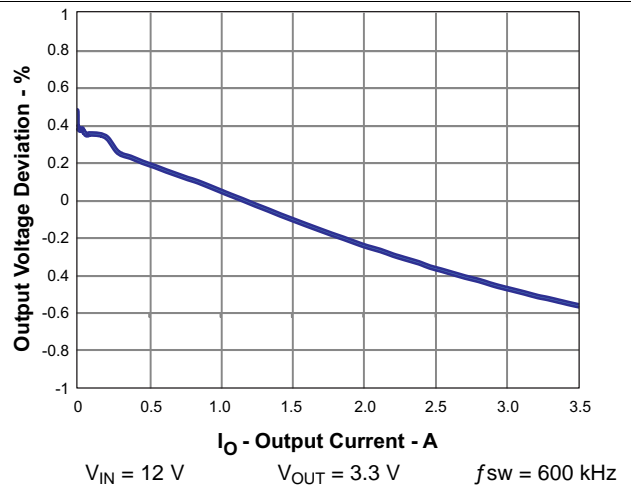


Figure 48. Regulation vs Load Current

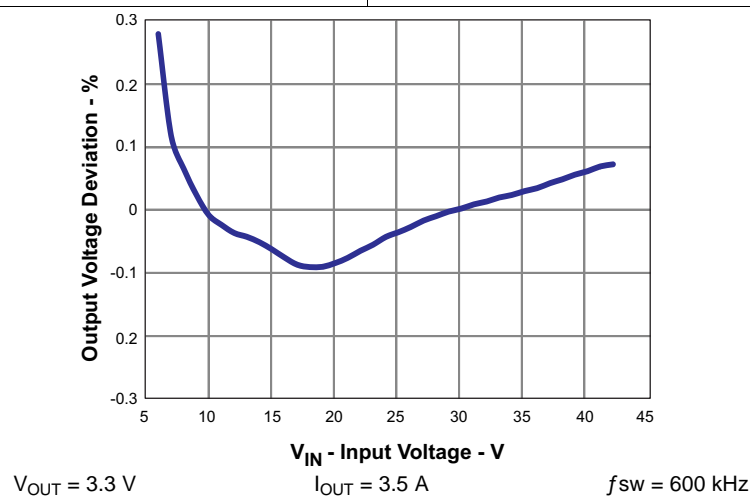
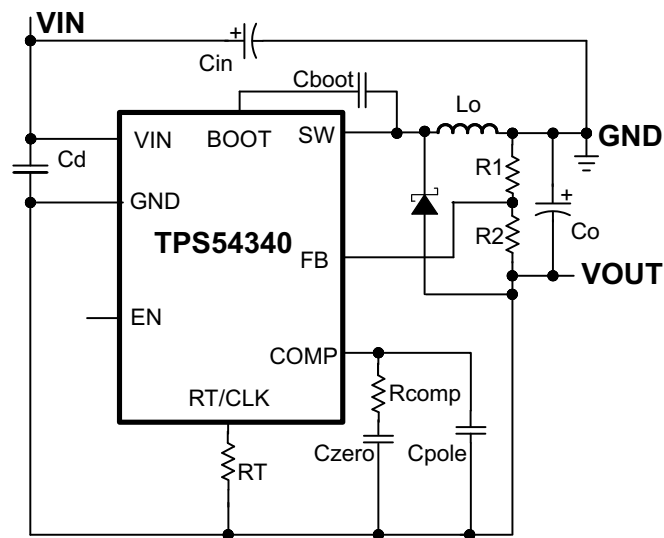


Figure 49. Regulation vs Input Voltage

8.2.2 Inverting Power

The TPS54340 can be used to convert a positive input voltage to a negative output voltage. Idea applications are amplifiers requiring a negative power supply. For a more detailed example see [SLVA317](#).

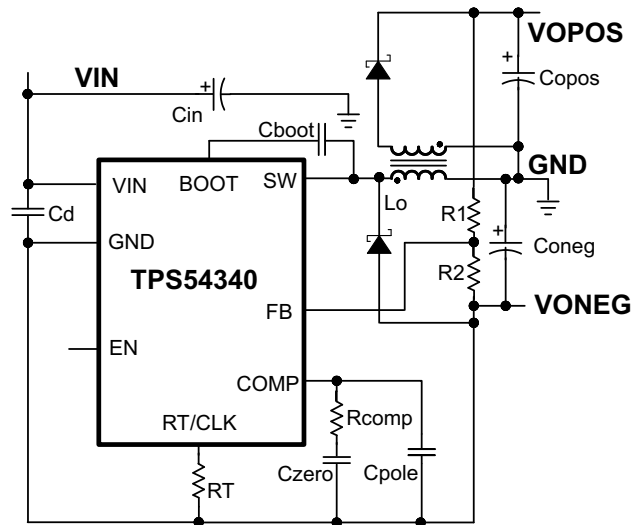


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Figure 50. TPS54340 Inverting Power Supply

8.2.3 Split Rail Power Supply

The TPS54340 can be used to convert a positive input voltage to a split rail positive and negative output voltage by using a coupled inductor. Idea applications are amplifiers requiring a split rail positive and negative voltage power supply. For a more detailed example see [SLVA369](#).



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Figure 51. TPS54340 Split Rail Power Supply

8.3 WEBENCH Power Designer

[TPS54340](#) with WEBENCH Power Designer

9 Power Supply Recommendations

The device are designed to operate from an input voltage supply range between 4.5 V and 42 V. If the input supply is located more than a few inches from the TPS54340 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μ F is a typical choice.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance

- To reduce parasitic effects, the VIN terminal should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN terminal, and the anode of the catch diode.
- The GND terminal should be tied directly to the power pad under the IC and the PowerPAD™.
- The PowerPAD™ should be connected to internal PCB ground planes using multiple vias directly under the IC.
- The SW terminal should be routed to the cathode of the catch diode and to the output inductor.
- Since the SW connection is the switching node, the catch diode and output inductor should be located close to the SW terminals, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- For operation at full rated load, the top side ground area must provide adequate heat dissipating area.
- The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
- The additional external components can be placed approximately as shown.
- It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

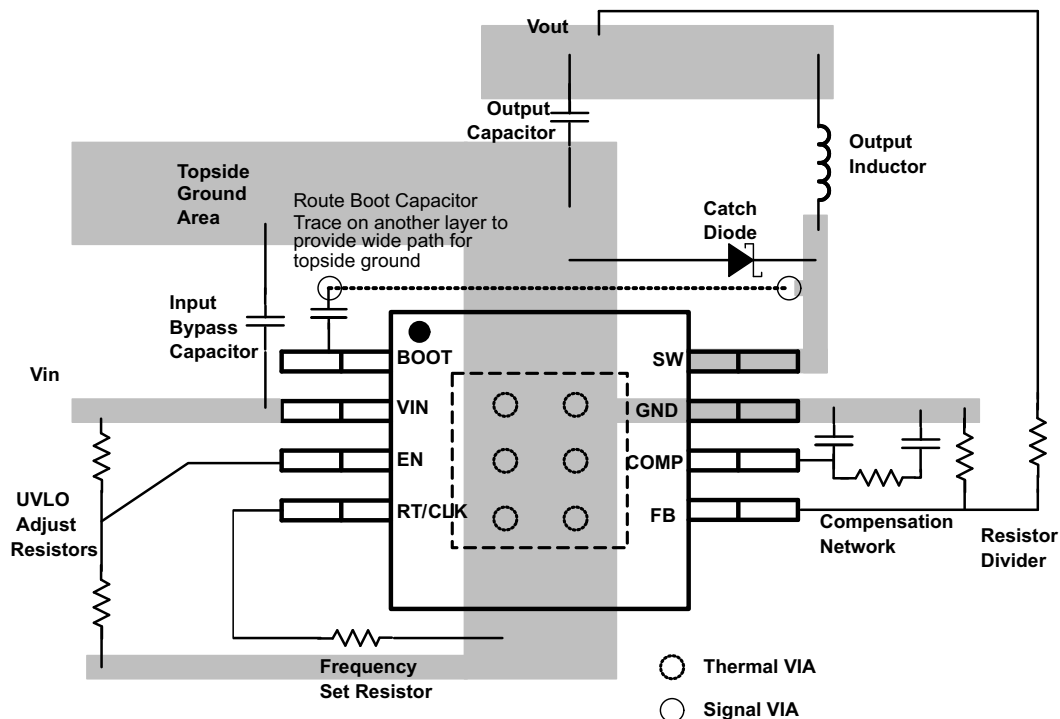


Figure 52. PCB Layout Example

10.2.1 Estimated Circuit Area

Boxing in the components in the design of Figure 32 the estimated printed circuit board area is 1.025 in² (661 mm²). This area does not include test points or connectors.

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 WEBENCHツールによるカスタム設計

[ここをクリック](#)すると、TPS54340デバイスを使用するカスタム設計を作成するために、WEBENCH®Power Designerを使用できます。

- 最初に、 V_{IN} 、 V_{OUT} 、 I_{OUT} の要件を入力します。
- 設計で効率、占有面積、コストなどの主要パラメータを最適化するため、オプティマイザのダイヤルを使用し、この設計と、テキサス・インスツルメンツによる他の可能なソリューションとを比較します。
- WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格や部品の在庫情報と併せて参照できます。
- ほとんどの場合、次の操作も実行できます。
 - 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
 - 熱的なシミュレーションを実行し、基板の熱特性を把握する。
 - カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
 - 設計のレポートをPDFで印刷し、同僚と設計を共有する。
- WEBENCHツールの詳細は、www.ti.com/webenchでご覧になれます。

11.1.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.1.3 関連資料

関連資料については、以下を参照してください。

- 『降圧型レギュレータから反転電源を作成する』、SLVA317
TPS54340: https://webench.ti.com/wb5/WBTablet/PartDesigner/quickview.jsp?base_pn=TPS54340

11.2 商標

Eco-mode, PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54340DDA	Active	Production	SO PowerPAD (DDA) 8	75 TUBE	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	54340
TPS54340DDA.B	Active	Production	SO PowerPAD (DDA) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54340
TPS54340DDAR	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	54340
TPS54340DDAR.B	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54340
TPS54340DDARG4	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54340
TPS54340DDARG4.B	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54340

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS54340 :

- Automotive : [TPS54340-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS54340DDA	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54340DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS54340DDA.B	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54340DDA.B	DDA	HSOIC	8	75	517	7.87	635	4.25



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

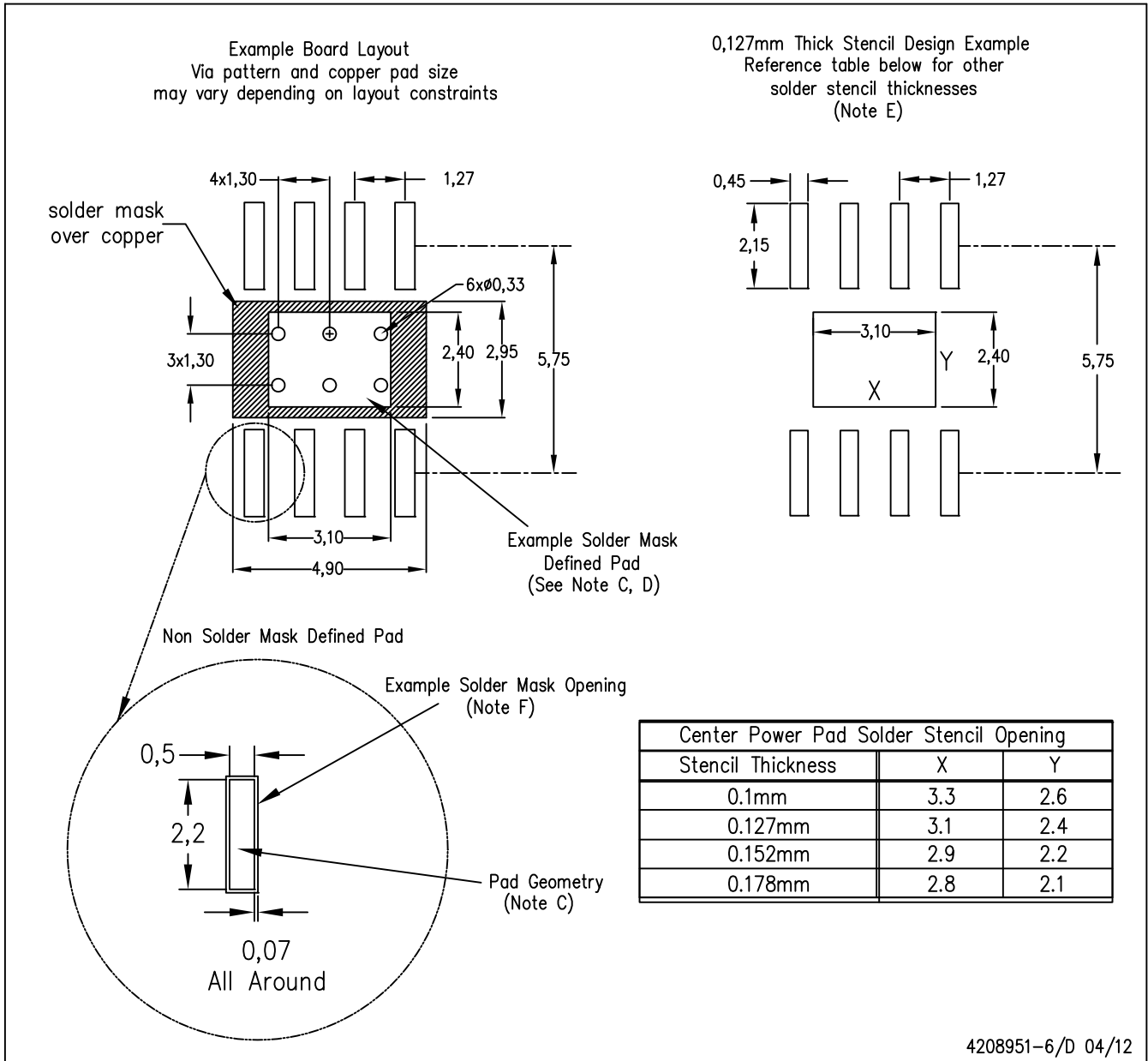


Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

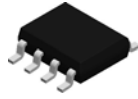
PowerPAD is a trademark of Texas Instruments



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

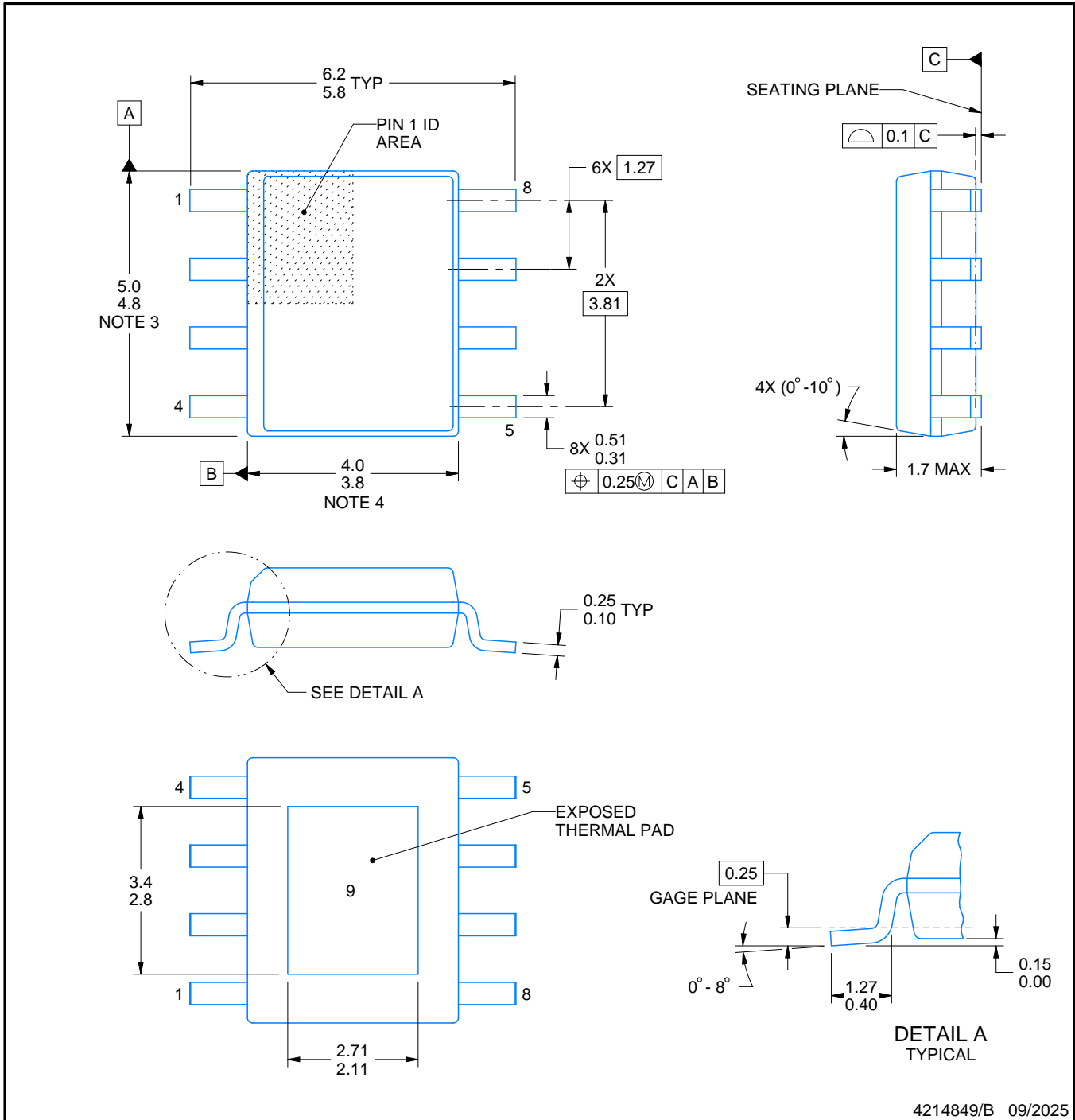
DDA0008B



PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/B 09/2025

NOTES:

PowerPAD is a trademark of Texas Instruments.

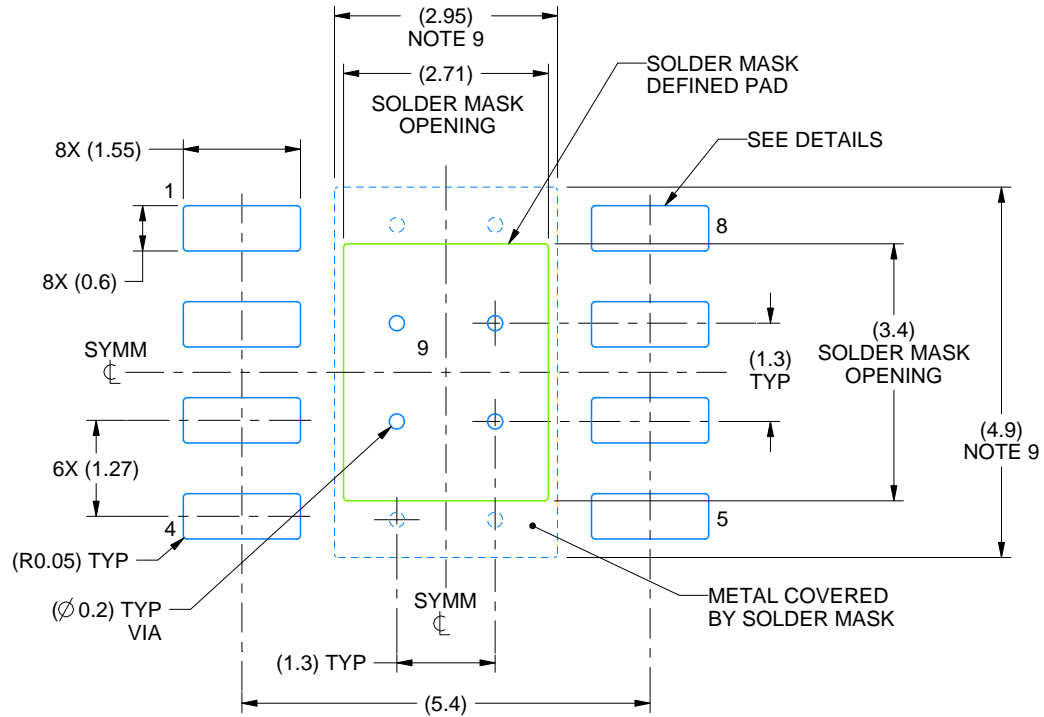
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

EXAMPLE BOARD LAYOUT

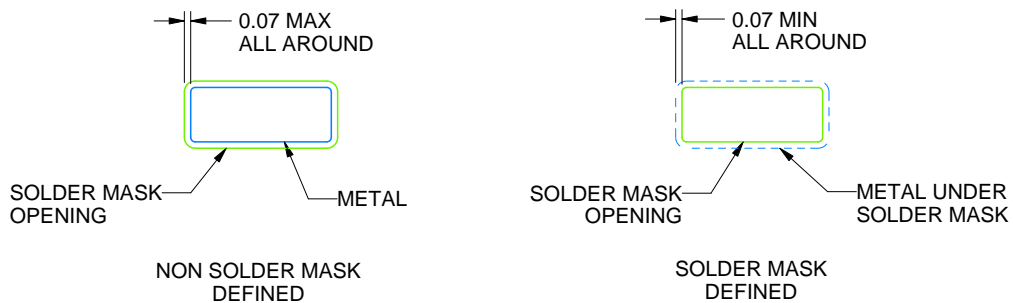
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

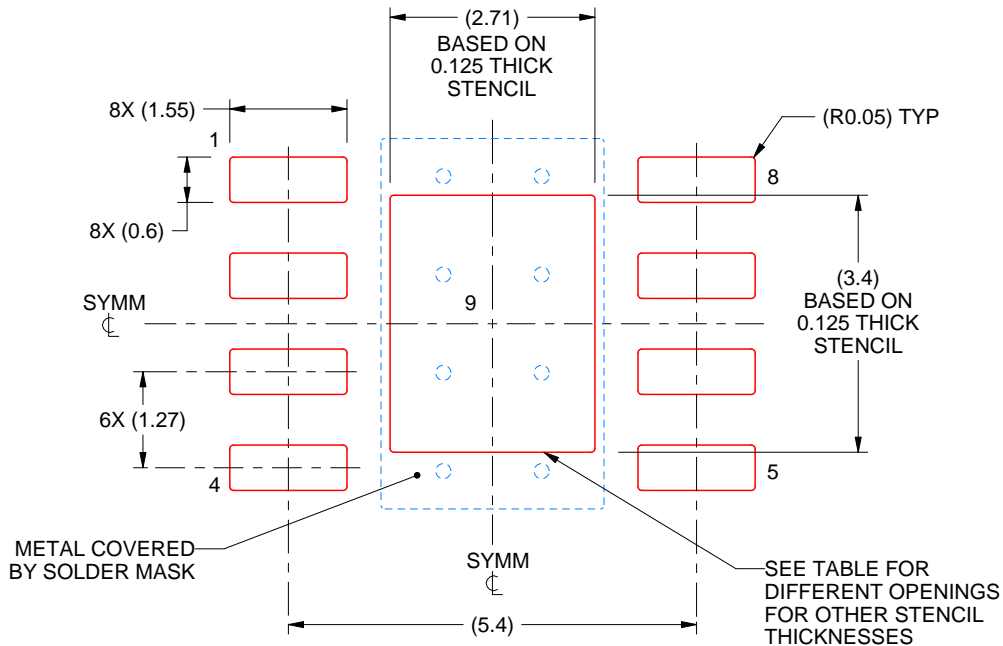
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
 EXPOSED PAD
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月