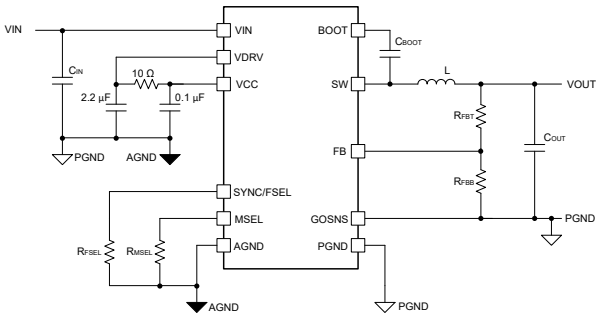
TPS543B22 4V～18V 入力、20A 同期整流 SWIFT™ 降圧コンバータ、内部補償型高度電流モード制御付き

1 特長

- 固定周波数、内部補償型の高度な電流モード (ACM) 制御
- 6.5mΩ および 2mΩ の MOSFET を内蔵
- 入力電圧範囲:4V～18V
- 出力電圧範囲:0.5V ～ 7V
- 真の差動リモート センス アンプ (RSA)
- 制御ループ性能を最適化する 3 つの 選択可能な PWM ランプ オプション
- 5 つの選択可能なスイッチング周波数:500kHz、750kHz、1MHz、1.5MHz、2.2MHz
- 外部クロックに同期可能
- 全温度範囲にわたって 0.5V、±0.5% の電圧リファレンス精度
- 選択可能なソフトスタート時間:1ms、2ms、4ms、8ms
- プリバイアス出力への単調スタートアップ
- 20A および 16A 動作をサポートする選択可能な電流制限
- 可変入力低電圧誤動作防止を利用可能
- パワー グッド出力監視
- 出力過電圧、出力低電圧、入力低電圧、過電流、過熱保護
- 動作時接合部温度:-40℃～150℃
- 2.5mm × 4.5mm の 17 ピン WQFN-HR パッケージ、0.5mm ピッチ
- 鉛フリー (RoHS 準拠)
- ピン互換: TPS543A26 および TPS543A22
- 放熱特性に優れたパッケージで提供する TPS543B25T (ドロップイン互換)
- SIMPLIS モデルが利用可能
- WEBENCH® Power Designer により、TPS543B22 を使用するカスタム設計を作成



TPS543B22 のアプリケーション概略図

2 アプリケーション

- 無線および有線の通信インフラストラクチャ機器
- 光およびファイバ・ネットワーク
- 試験 / 測定機器
- 医療 / ヘルスケア

3 概要

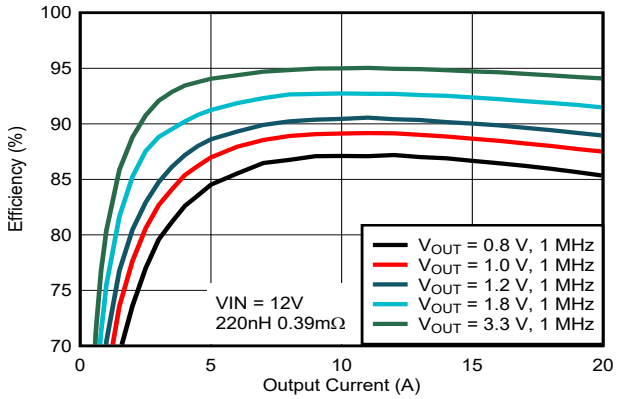
TPS543B22 は、高効率の 18V、20A の同期整流式降圧コンバータで、内部補償された固定周波数の高度電流モード (ACM) 制御アーキテクチャを採用しており、常に FCCM で動作し、0.5V～7V の出力電圧を生成します。本デバイスは、最大 2.2MHz のスイッチング周波数で動作しながら高い効率を実現できるため、小さいソリューション サイズが求められる設計に最適です。固定周波数コントローラは 500kHz～2.2MHz で動作でき、SYNC ピンを使用して外部クロックに同期できます。追加機能として、高精度の電圧リファレンス、2 線式のリモート検出、選択可能なソフト スタート時間、プリバイアス出力への単調なスタートアップ、選択可能な電流制限、EN ピンにより調整可能な UVLO、各種のフォルト保護があります。

TPS543B22 は小型の 2.5mm × 4.5mm HotRod™ WQFN-FCRLF パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS543B22	RYS (WQFN-FCRLF、17)	4.50mm × 2.50mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーションの効率

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4 Pin Configuration and Functions

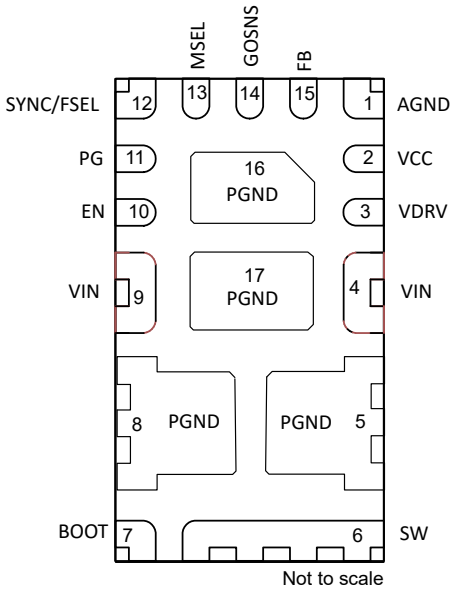


図 4-1. 17-Pin WQFN-FCRLF RYS Package (Bottom View)

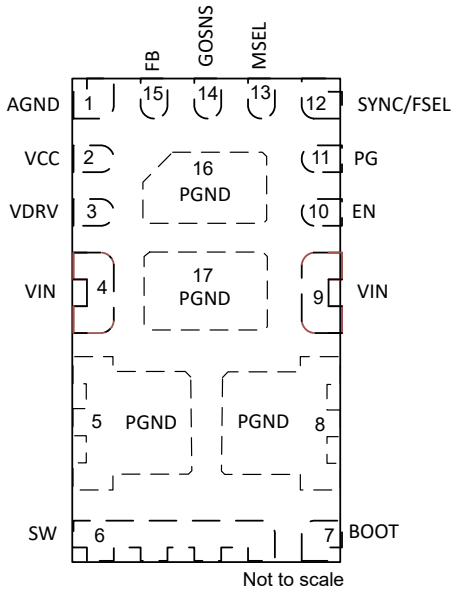


図 4-2. 17-Pin WQFN-FCRLF RYS Package (Top View)

表 4-1. Pin Functions

Pin		Type[1]	Description
Name	No.		
AGND	1	—	Ground return for internal analog circuits
VCC	2	I	Supply for analog control circuitry. Connect a 10-Ω resistor from VDRV to this pin and bypass with a 0.1-µF capacitor to AGND.
VDRV	3	O	Internal 5-V regulator output and internal connection to drivers. Bypass these pins with a 2.2-µF capacitor to PGND. See セクション 6.3.2.
VIN	4, 9	I	Input power to the power stage. Low impedance bypassing of these pins to PGND is critical. A 1-µF capacitor from each VIN to PGND close to the IC is required.
PGND	5, 8, 16, 17	—	Ground return for the power stage. This pin is internally connected to the source of the low-side MOSFET.
SW	6	O	Switch node of the converter. Connect this pin to the output inductor.
BOOT	7	I	Supply for the internal high-side MOSFET gate driver. Connect a capacitor from this pin to SW.
EN	10	I	Enable pin. Float or tie high to enable, or enable and disable with an external signal, or adjust the input undervoltage lockout with a resistor divider. See セクション 6.3.3.
PG	11	O	Open-drain power-good indicator. See セクション 6.3.10.
SYNC/FSEL	12	I	Frequency select and external clock synchronization. A resistor to ground sets the switching frequency of the device. An external clock can also be applied to this pin to synchronize the switching frequency. See セクション 6.3.5.3.
MSEL	13	I	A resistor to ground selects the current limit, soft-start rate, and PWM ramp amplitude. See セクション 6.3.9.
GOSNS	14	I	Ground sense return and input to the differential remote sense amplifier
FB	15	I	Feedback pin and input to the differential remote sense amplifier for output voltage regulation. Connect this pin to the midpoint of a resistor divider to set the output voltage. See セクション 6.3.6.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	20	V
Pin voltage	SW, DC	–0.3	20	V
Pin voltage	SW, transient 20ns	–5	22	V
Pin voltage	VIN to SW, DC	–0.3	20	V
Pin voltage	VIN to SW, transient 20ns	–6	25	V
Pin voltage	BOOT	–0.3	25	V
Pin voltage	BOOT to SW	–0.3	6	V
Pin voltage	EN, PG, MSEL, SYNC/FSEL, FB	–0.3	6	V
Pin voltage	VCC, VDRV	–0.3	6	V
Pin voltage	GOSNS	–0.3	0.3	V
Sink current	PG		5	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to PGND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Pin voltage	Input voltage range	4		18	V
V_{OUT}	Output voltage range		0.5		7	V
	Pin voltage	SW - PGND	–0.1		18	V
	Pin voltage	EN, FB, PG, MSEL, SYNC/FSEL	–0.1		5.5	V
	Pin voltage	GOSNS	–0.3		0.3	V
I_{OUT}	Output current range				20	A
I_{PG}	Power Good input current			2	5	mA
T_J	Operating junction temperature	Operating junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		RYS (QFN, JEDEC) 17 PINS	RYS (QFN, TI EVM) 17 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.9	18.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.6	Not applicable (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.5	Not applicable (2)	°C/W

5.4 Thermal Information (続き)

THERMAL METRIC(1)		RYS (QFN, JEDEC) 17 PINS	RYS (QFN, TI EVM) 17 PINS	UNIT
ψ_{JT}	Junction-to-top characterization parameter	0.8	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.5	6.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	Not applicable	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Not applicable to an EVM layout.

5.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VIN} = 4 V - 18 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$I_{Q(VIN)}$	VIN operating non-switching supply current	V_{EN} = 1.3 V, V_{FB} = 550 mV, V_{VIN} = 12 V, 1 MHz		1200	1600	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V, V_{VIN} = 12 V		20	32	µA
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	3.8	4.00	4.2	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			150		mV
INTERNAL LDO						
V_{VDRV}	Internal linear regulator output voltage	V_{VIN} = 12 V, I_{VDRV} = 25 mA		4.5		V
	Internal linear regulator dropout voltage	V_{VIN} – V_{VDRV}, V_{VIN} = 3.8 V, I_{VDRV} = 25 mA			390	mV
	Internal linear regulator short-circuit current limit	V_{VIN} = 12 V		150		mA
$VCC_{UVLO(R)}$	VCC UVLO rising threshold			3.4		V
$VCC_{UVLO(H)}$	VCC UVLO hysteresis			0.4		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching		1.2	1.25	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	1.05	1.1		V
$V_{EN(H)}$	EN voltage hysteresis			100		mV
	EN pin sourcing current	V_{EN} = 1.1 V		1.75		µA
	EN pin sourcing current	V_{EN} = 1.3 V		11.6		µA
	EN HIGH to start of switching delay (1)	EN from 0V to 3V rising		1		ms
REFERENCE VOLTAGE						
V_{FB}	Feedback Voltage	T_J = –40°C to 150°C	497.5	500	502.5	mV
$I_{FB(LKG)}$	Input leakage current into FB pin	V_{FB} = 500 mV, non-switching, V_{VIN} = 12 V, V_{EN} = 0 V		3		nA
REMOTE SENSE AMPLIFIER						
$I_{LEAK(GOSNS)}$	Current out of GOSNS pin		85	90	95	µA
$V_{IRNG(GOSNS)}$	GOSNS common mode voltage for regulation	AGND +/- V_{GOSNS}	–100		100	mV
SWITCHING FREQUENCY AND OSCILLATOR						
f_{SW}	Switching frequency	R_{FSEL} = 24.3 kΩ to AGND	450	500	550	kHz
f_{SW}	Switching frequency	R_{FSEL} = 17.4 kΩ to AGND	675	750	825	kHz
f_{SW}	Switching frequency	R_{FSEL} = 11.8 kΩ to AGND	900	1000	1100	kHz
f_{SW}	Switching frequency	R_{FSEL} = 8.06 kΩ to AGND	1350	1500	1650	kHz
f_{SW}	Switching frequency	R_{FSEL} = 4.99 kΩ to AGND	1980	2200	2420	kHz
SYNCHRONIZATION						
$V_{IH(sync)}$	High-level input voltage		1.8			V
$V_{IL(sync)}$	Low-level input voltage				0.8	V
$F_{SYNC(range)}$	Frequency synchronization range to not adversly affect loop stability. (1)		F_{CLK} – 20%		F_{CLK} + 20%	

5.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VIN} = 4 V - 18 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT-START						
t_{SS1}	Soft-start time 0 to 100% V_{OUT}	R_{MSEL} = 1.78 kΩ		1		ms
t_{SS2}	Soft-start time 0 to 100% V_{OUT}	R_{MSEL} = 2.21 kΩ		2		ms
t_{SS3}	Soft-start time 0 to 100% V_{OUT}	R_{MSEL} = 2.74 kΩ		4		ms
t_{SS4}	Soft-start time 0 to 100% V_{OUT}	R_{MSEL} = 3.32 kΩ		8		ms
POWER STAGE						
$R_{DS(on)HS}$	High-side MOSFET on-resistance	T_J = 25°C, V_{VIN} = 12 V, $V_{BOOT-SW}$ = 4.5 V		6.5		mΩ
$R_{DS(on)LS}$	Low-side MOSFET on-resistance	T_J = 25°C, V_{VDRV} = 4.5 V		2.0		mΩ
$V_{VIN(TH\_r)}$	VIN throttle rising threshold	T_J = 25°C. Weaken high-side gate drive upon VIN rising		16		V
$V_{VIN(TH\_f)}$	VIN throttle falling threshold	T_J = 25°C. Recover high-side gate drive upon VIN falling		15.5		V
$V_{BOOT-SW(UV\_R)}$	BOOT-SW UVLO rising threshold	$V_{BOOT-SW}$ rising		3.2		V
$V_{BOOT-SW(UV\_F)}$	BOOT-SW UVLO falling threshold	$V_{BOOT-SW}$ falling		2.8		V
$T_{ON(min)}$	Minimum ON pulse width			22	28	ns
$T_{OFF(min)}$	Minimum OFF pulse width (1)			115		ns
CURRENT SENSE AND OVERCURRENT PROTECTION						
$I_{HS(OC1)}$	High-side peak current limit	R_{MSEL} = 2.1 kΩ	26.1	29	31.9	A
$I_{HS(OC2)}$		R_{MSEL} = 22.1 kΩ	20.7	23	25.3	A
$I_{LS(OC1)}$	Low-side valley current limit	R_{MSEL} = 2.1 kΩ	21.15	23.5	25.85	A
$I_{LS(OC2)}$		R_{MSEL} = 22.1 kΩ	16.74	18.6	20.46	A
$I_{LS(NOC)}$	Low-side negative current limit	Current into SW pin	7			A
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTIONS						
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising		120%		V_{REF}
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	V_{FB} falling		80%		V_{REF}
POWER GOOD						
	Power good threshold	V_{FB} rising (Good)	88%	91%	94%	V_{REF}
	Power good threshold	V_{FB} rising (OV Fault)	112%	115%	118%	V_{REF}
	Power good threshold	V_{FB} falling (Good)	103.5%	106.5%	109.5%	V_{REF}
	Power good threshold	V_{FB} falling (UV Fault)	79%	82%	85%	V_{REF}
$I_{PG(LKG)}$	Leakage current into PG pin when open drain output is high	V_{PG} = 4.7 V			5	µA
$V_{PG(low)}$	PG low-level output voltage	I_{PG} = 2 mA, V_{IN} = 12 V			0.6	V
	Min VIN for valid PG output	EN = 0V, PG pulled up to 5V		1		V
	PG delay going from low to high			201		us
	PG delay going from high to low			11		µs
HICCUP						
	Hiccup time before re-start			7*t_{SS}		ms
OUTPUT DISCHARGE						
R_{Dischg}	Output discharge resistance	V_{VIN} = 12 V, V_{SW} = 0.5 V, power conversion disabled.		100		Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising		165	175	°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			12		°C

(1) Specified by design

5.6 Typical Characteristics

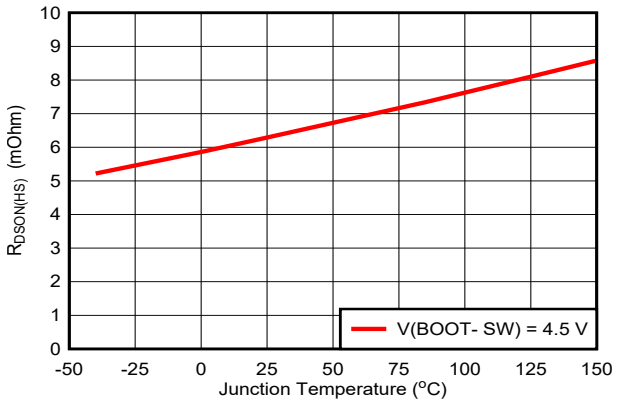


図 5-1. High-Side FET Rds_{ON}

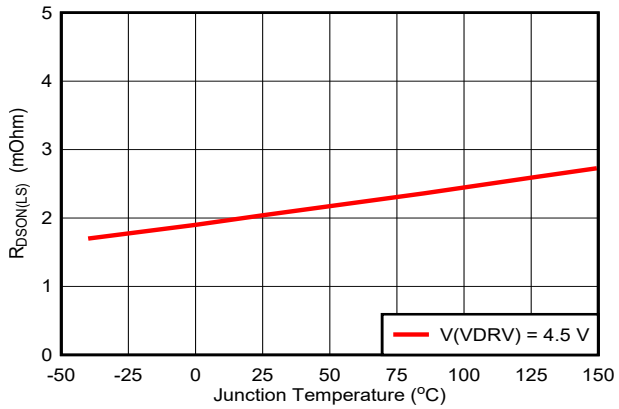


図 5-2. Low-Side FET Rds_{ON}

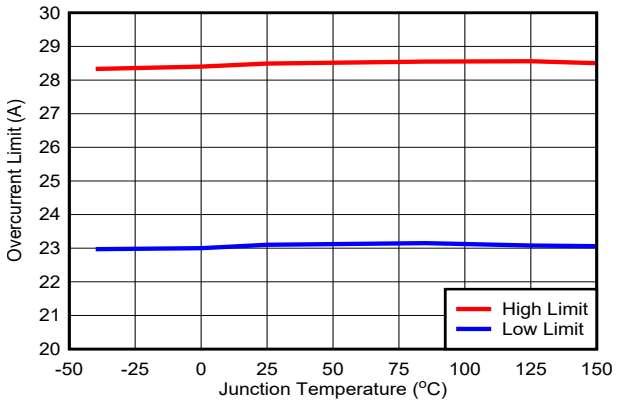


図 5-3. Overcurrent Limit

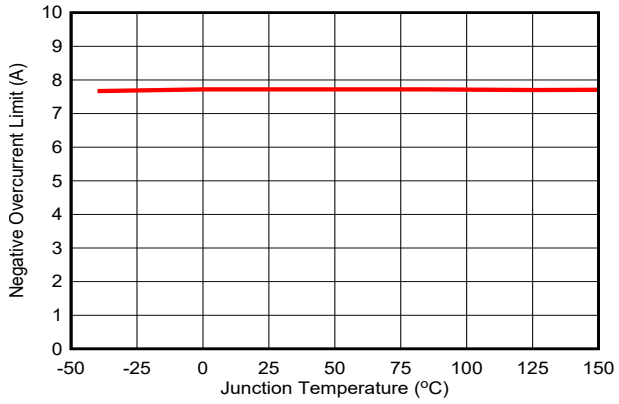


図 5-4. Negative Overcurrent Limit

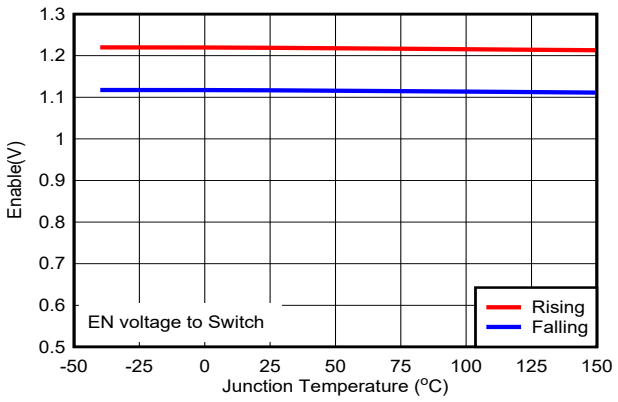


図 5-5. Enable Voltage

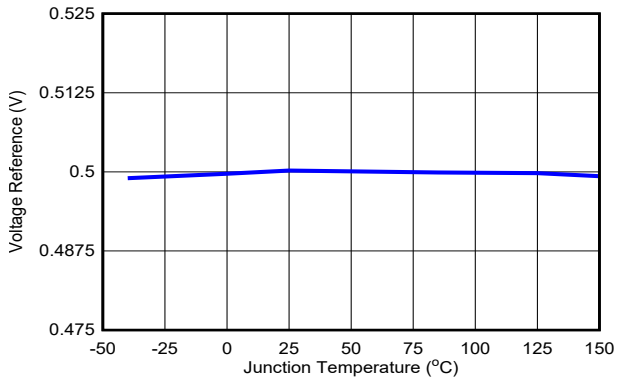


図 5-6. V_{REF}

5.6 Typical Characteristics (continued)

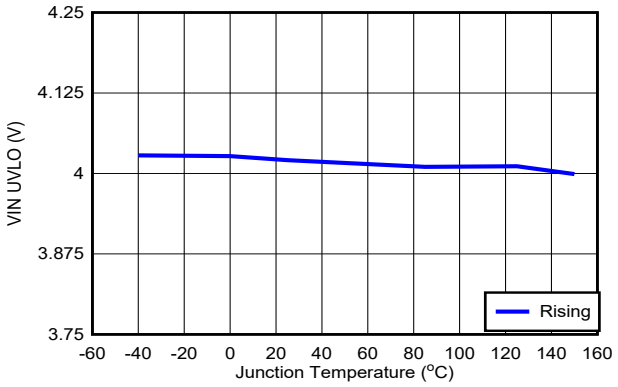


図 5-7. V_{IN} UVLO

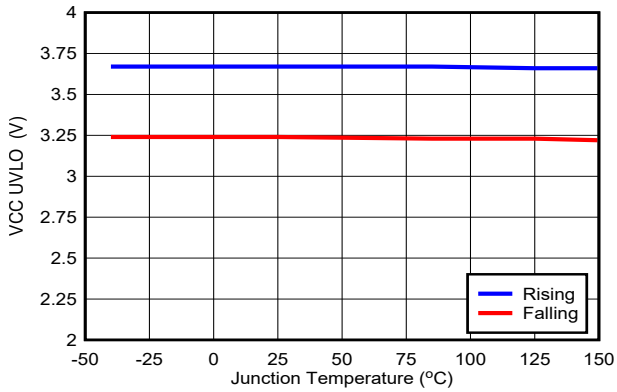


図 5-8. V_{CC} UVLO

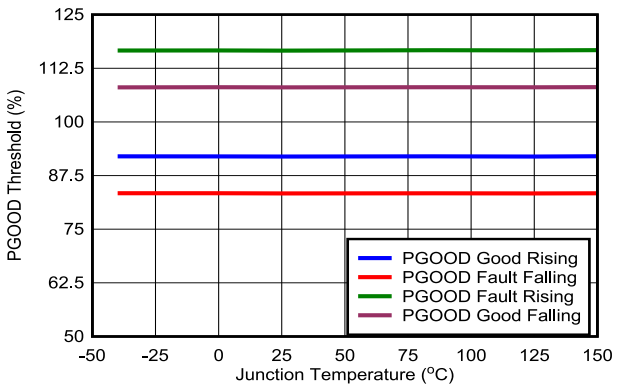


図 5-9. PG Threshold

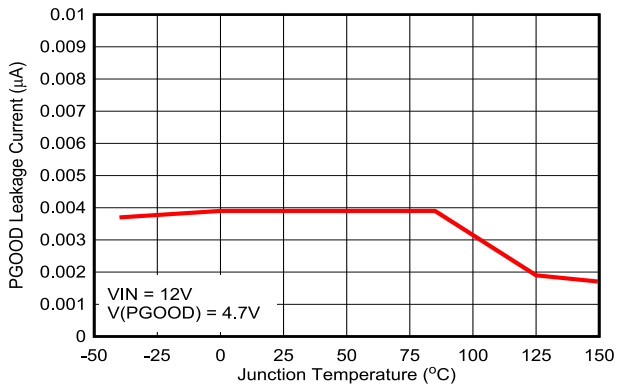


図 5-10. PG Leakage Current

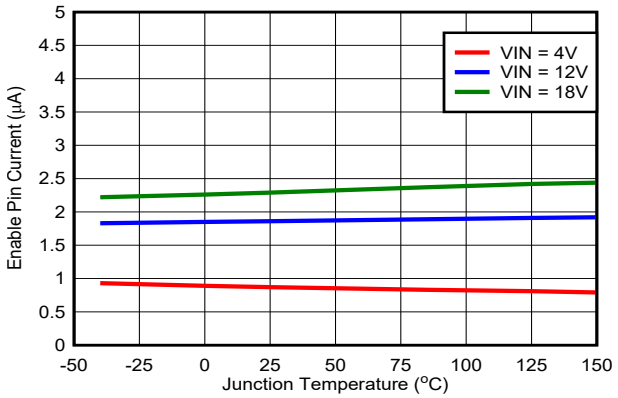


図 5-11. Enable Pin Current at Different VIN

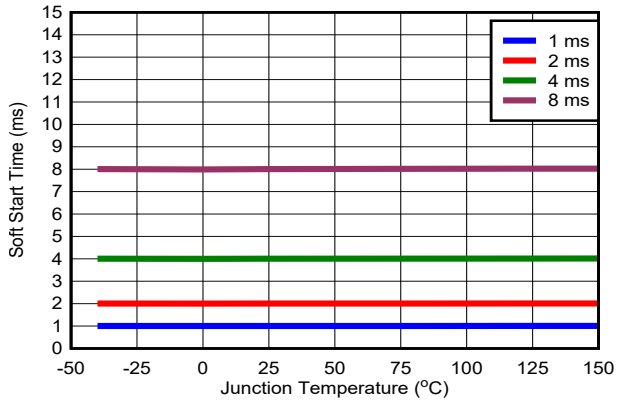


図 5-12. Soft Start

5.6 Typical Characteristics (continued)

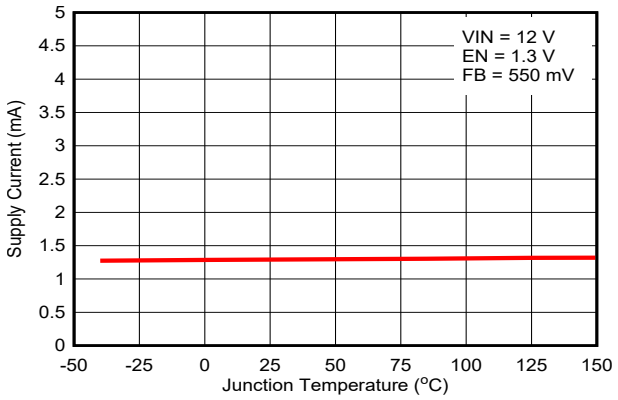


図 5-13. Non-Switching Supply Current

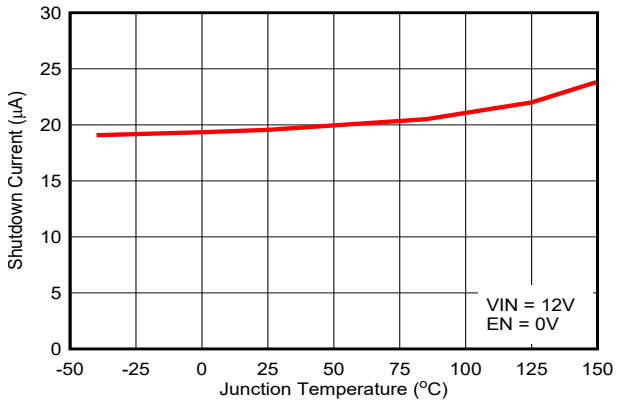


図 5-14. Shutdown Supply Current

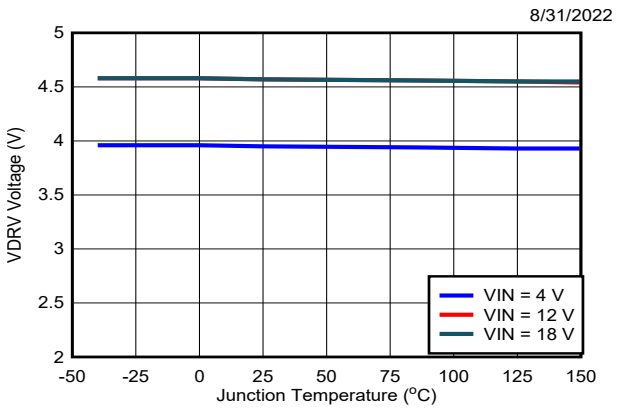


図 5-15. VDRV vs Temperature

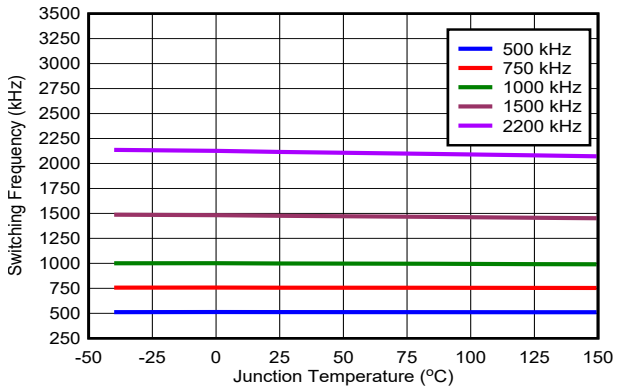


図 5-16. Switching Frequency vs Temperature

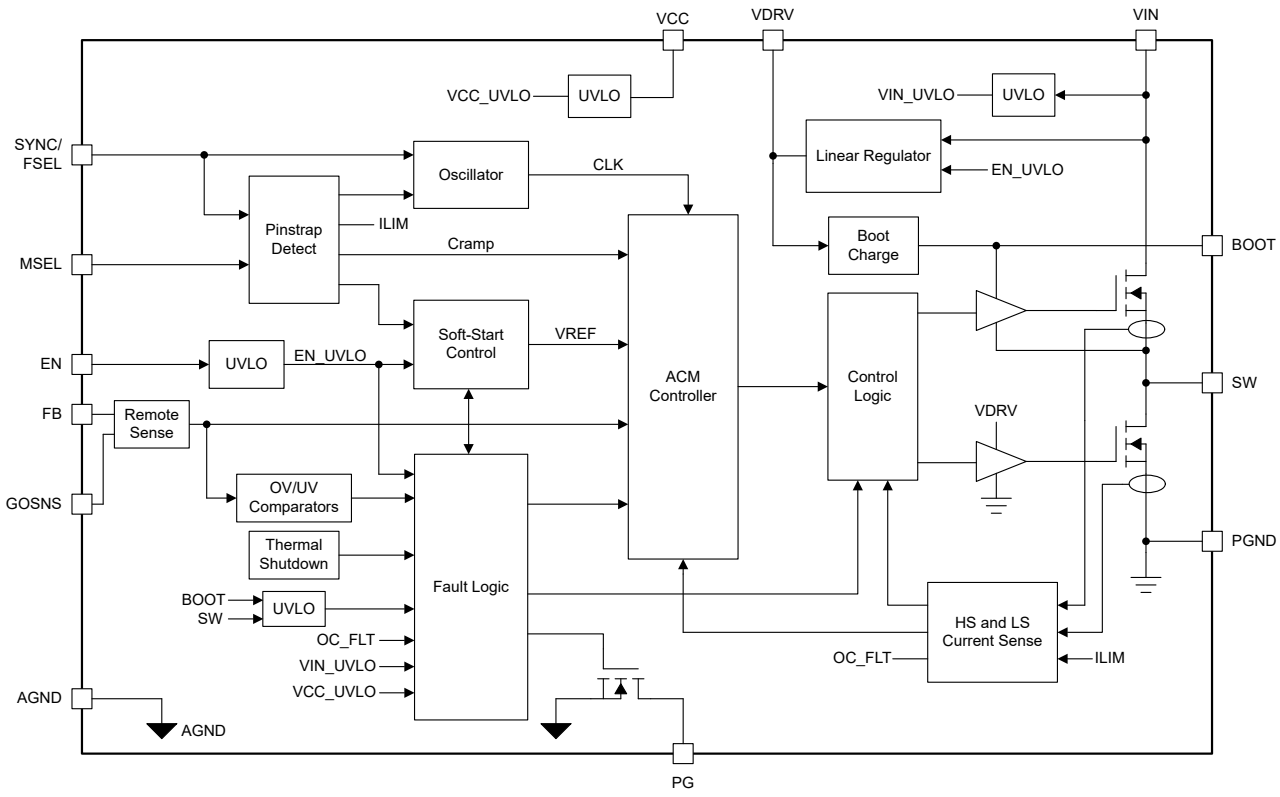
6 Detailed Description

6.1 Overview

The TPS543B22 is a 20-A, high-performance synchronous buck converter with two integrated N-channel MOSFETs. The TPS543B22 has a maximum operating junction temperature of 150°C, making the device designed for high-ambient temperature applications such as wireless infrastructure. The input voltage range is 4 V to 18 V and the output voltage range is 0.5 V to 7 V. The device features a fixed-frequency advanced current mode (ACM) control architecture with five switching frequency selection settings ranging from 500 kHz to 2.2 MHz, allowing for efficiency and size optimization when selecting output filter components. The switching frequency of the device can be synchronized to an external clock applied to the FSEL/SYNC pin.

Advanced current mode is an emulated peak current-mode control topology, supporting stable static and transient operation without the requirement for a complex external compensation design. ACM includes an internal ramp generation network that emulates inductor current information, enabling the use of low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). The internal ramp also creates a high signal-to-noise ratio for good noise immunity. The TPS543B22 has three ramp options to optimize the internal feedback loop for various inductor and output capacitor combinations with only a single resistor to AGND (see セクション 6.3.7.2 for details). The TPS543B22 is easy to use and allows low external component count with fast load transient response. Fixed-frequency modulation also provides ease-of-filter design to overcome EMI noise.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 VIN Pins and VIN UVLO

The VIN pin voltage supplies the internal control circuits of the device and provides the input voltage to the power stage. The input voltage for V_{IN} can range from 4 V to 18 V. The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold for start-up is 3.95 V typically with hysteresis of 150 mV.

A second means to enable the device is provided by interfacing to the EN pin. See セクション 6.3.3 for more details.

6.3.2 Internal Linear Regulator and Bypassing

The VDRV pin is connected internally to the output of the internal (4.5 V nominal) linear regulator (LDO) and to the MOSFET drivers. Bypass VDRV to PGND with a ceramic capacitor. TI recommends a value of 2.2 µF to 10 µF. The VCC pin is the source for the internal control circuitry. Connect a 10-Ω resistor from VDRV to VCC and bypass VCC to AGND with a ceramic capacitor (0.1 µF recommended).

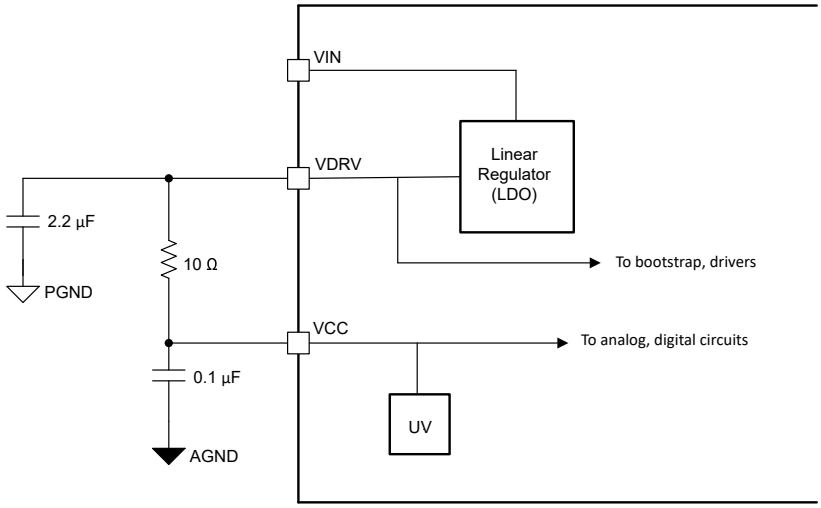


図 6-1. Device Bypassing

Not intended to drive VCC with any source other than VDRV.

Not intended to connect VDRV to any external source or load.

6.3.3 Enable and Adjustable UVLO

The EN pin provides means for on and off control of the device. After the EN pin voltage exceeds the threshold voltage, the device begins a start-up sequence. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low operating current state. The EN pin has an internal pullup current source, I_P, allowing the pin to be floated to enable the device by default. Make sure that leakage current of any circuitry connected to the EN pin does not exceed the minimum EN pullup current, otherwise the device can not be able to start. If an application requires digital control of the ENABLE function, an open-drain or open-collector output logic can be interfaced with the pin.

Alternatively, an external resistor divider can be added from VIN to the EN pin for adjustable UVLO as shown in 図 6-2. The EN pin pullup hysteresis current, *Ih*, is used to control the voltage hysteresis for the UVLO function by increasing the pin sourcing current after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using 式 1 and 式 2. When using the adjustable UVLO function, TI recommends 500 mV or greater hysteresis. For applications with very slow input voltage slew rate, a capacitor can be placed from the EN pin to ground to filter any noise on the input voltage.

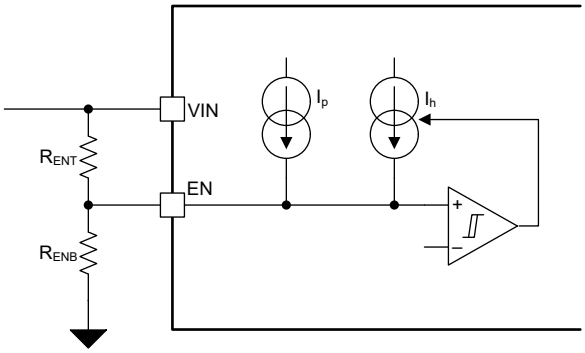


図 6-2. Adjustable UVLO Using EN

$$R_{ENT} = \frac{V_{START} \times \left(\frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_h} \quad (1)$$

$$R_{ENB} = \frac{R_{ENT} \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_{ENT} \times \left(I_p + I_h \right)} \quad (2)$$

6.3.3.1 Internal Sequence of Events During Start-Up

The enable feature of the TPS543B22 provides two-threshold-level functionality. When the EN pin voltage is less than the internal start-up threshold (approximately 0.8 V), the device is in a low-power shutdown mode. When the EN pin voltage rises to above this threshold, the internal linear regulator (LDO) is enabled and charges the external VDRV capacitor. When VCC is connected to VDRV, and the voltage on the VCC pin exceeds the UVLO threshold (approximately 3.6 V), the TPS543B22 reads the pin strap configuration as determined by the MSEL pin (see セクション 6.3.9) and SYNC/FSEL pin (see セクション 6.3.5.3) settings, and then enters a standby state.

The second EN pin threshold becomes active when both the VIN UVLO (approximately 4 V) and VCC UVLO thresholds are exceeded. Thus, when the EN pin reaches above the (nominally 1.2 V) upper threshold, the TPS543B22 initiates a power-on delay (typically 64 µs) to initialize the control loop circuitry. After the power-on delay, the power stage is enabled and soft start begins.

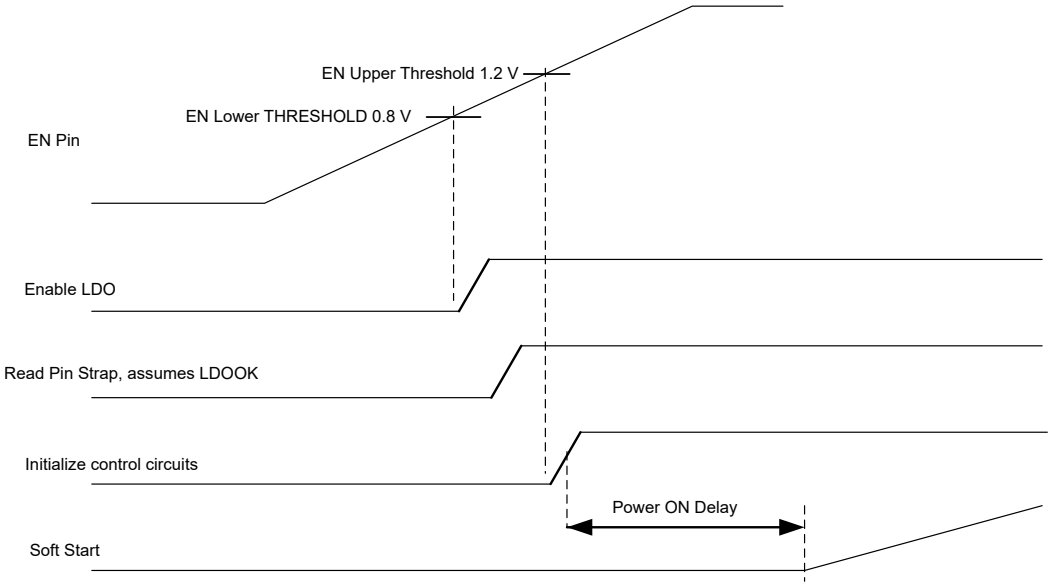


図 6-3. Internal Start-Up Sequence

If the enable signal rises very quickly, the delay time from EN rising to the beginning of soft start is a function of the time required to power and initialize the device (start-up of the linear regulator, VCC UVLO exceeded, reading pin strap level, initialize feedback circuitry, and so forth), and can take up to 1 ms (typical).

6.3.4 Switching Frequency Selection

The switching frequency of the device is selected by connecting a resistor (R_{FSEL}) from the SYNC/FSEL pin to AGND. The frequency options and the corresponding programming resistors are listed in 表 6-1. It is required to use a 1% tolerance resistor or better.

表 6-1. Switching Frequency Selection

R_{FSEL} Allowed Nominal Range (1%) (kΩ)	Recommended E96 Standard Value (1%) (kΩ)	Recommended E12 Standard Value (1%) (kΩ)	f_{SW} (kHz)
≥ 24.0	24.3	27.0	500
17.4 – 18.0	17.4	17.8	750
11.8 – 12.1	11.8	12.1	1000
8.06 – 8.25	8.06	8.25	1500
≤ 5.11	4.99	4.75	2200

6.3.5 Switching Frequency Synchronization to an External Clock

The TPS543B22 can be synchronized to an external clock by applying a square wave clock signal to the SYNC/FSEL pin with a duty cycle from 20% to 80%. The external clock can either be applied before the device starts up or during operation. If the external clock is applied before the device starts, a resistor from SYNC/FSEL to AGND is not needed. If the external clock is applied after the device starts, then the clock frequency must be within ±20% of the frequency set by the SYNC/FSEL resistor. When the external clock is applied after the device starts, the device begins synchronizing to this external clock after counting four consecutive switching cycles with the external clock pulse present. See セクション 6.3.5.2.

Although there is no internal circuit to detect the higher 20% range of the clock frequency, it falls outside the stability range of the LC design so it is imposed as a requirement on the customer to ensure the synchronization clock is within ±20% of the frequency set by the SYNC/FSEL resistor.

6.3.5.1 Internal PWM Oscillator Frequency

When the external clock is present, the device synchronizes the switching frequency to the clock. Any time the external clock is not present, the device defaults to the internal PWM oscillator frequency.

If the device starts up before an external clock signal is applied, then the internal PWM oscillator frequency is set by the R_{FSEL} resistor according to セクション 6.3.5.3. The device switches at this frequency until the external clock is applied or anytime the external clock is not present.

If the external clock is applied before the device starts up, then the R_{FSEL} resistor is not needed. The device then decodes the external clock frequency and selects an internal PWM oscillator frequency.

表 6-2. Internal Oscillator Frequency Decode

External Sync Clock Frequency (kHz)	Decoded Internal PWM Oscillator Frequency (kHz)
400 – 600	500
600 – 857	750
857 – 1200	1000
1200 – 1810	1500
1810 – 2640	2200

The thresholds for the external SYNC clock frequency ranges have approximately a ±5% tolerance. If the external clock frequency is within that tolerance range, it is possible for the internal PWM oscillator frequency to be decoded as either the frequency above or below that threshold. Because the internal frequency is what is used in case of the loss of the synchronization clock, TI recommends that the output LC filter and ramp selection are chosen for stability for either frequency. 表 6-3 shows the tolerance range of the decode thresholds. If the external clock is to be within any of these ranges, TI recommends to design the converter to ensure converter stability for both possible internal PWM oscillator frequencies.

表 6-3. Frequency Decode Thresholds

Minimum (kHz)	Typical (kHz)	Maximum (kHz)
570	600	630
814	857	900
1140	1200	1260
1736	1810	1884

6.3.5.2 Loss of Synchronization

If at any time during operation, there is a loss of synchronization, the device defaults to the internal PWM oscillator frequency until the synchronization clock returns. After the clock is no longer present, the device switches at 70% of the internal clock frequency for four consecutive cycles. After four consecutive cycles without clock pulses, the device operates at the normal internal PWM oscillator frequency.

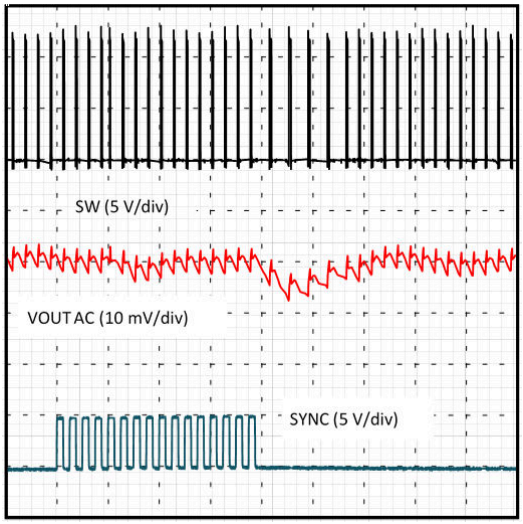


図 6-4. Clock Synchronization Transition

6.3.5.3 Interfacing the SYNC/FSEL Pin

If an application requires synchronizing to a SYNC clock but the clock is unavailable before the device is enabled, TI recommends a high impedance buffer to ensure proper detection of the R_{FSEL} value. 図 6-5 shows the recommended implementation. The leakage current into the buffer output must be less than 5 µA to ensure proper detection of the R_{FSEL} value. Power the buffer from the VDRV output of the device to ensure the VCC voltage is available and the buffer output is high impedance before the device tries to detect the R_{FSEL} value. When powering the buffer from the VDRV pin, the external load on the VDRV pin must be less than 2 mA.

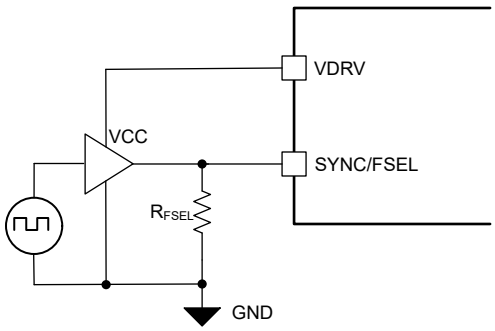


図 6-5. Interfacing the SYNC/FSEL Pin with a Buffer

6.3.6 Remote Sense Amplifier and Adjusting the Output Voltage

Remote sensing of the output voltage is provided through a dedicated high speed, low offset instrumentation type amplifier. Connect the output voltage setting resistive divider described below from the output voltage sensing point to the GOSNS pin. The center point is to be connected to the FB pin. Note the GOSNS pin is to be tied to the converter output voltage return at a location near to the load.

The output voltage is programmed with a resistor divider from the converter output (V_{OUT}) to the FB pin as shown in 図 6-6. Use 1% tolerance or better divider resistors.

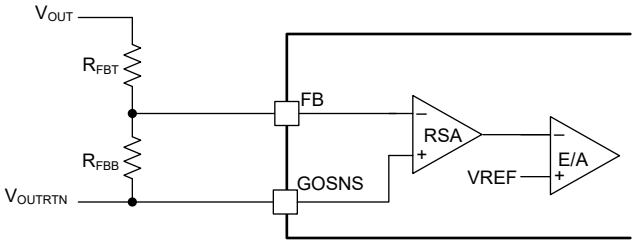


図 6-6. FB Resistor Divider

Starting with a fixed value for the bottom resistor, typically 10 kΩ, use 式 3 to calculate the top resistor in the divider.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{3}$$

6.3.7 Loop Compensation Guidelines

The TPS543B22 employs advanced current mode control (ACM) architecture to provide internal feedback loop compensation for most applications. By applying V_{IN}, duty cycle, and low-side FET current information to generate an internal ramp combined with contribution from internally sensed inductor valley current, ACM cancels one of the poles of the output LC filter and provides phase compensation to ensure loop stability. As with any internal compensation scheme, certain design guidelines must be followed. Guidelines for a converter design are provided in the following sections.

6.3.7.1 Output Filter Inductor Tradeoffs

The selection of the output inductor is one of the most important choices to make in designing a converter. The following is a short list of considerations to make when determining the value of the inductance used. Other considerations are found in the セクション 7.

Start with an inductor value that results in a ripple current (ΔI) between 30% and 50% of full load.

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \tag{4}$$

- A choice of inductor value has a direct correlation to load transient response. Too large an inductor value can result in poor load transient response.
- The ripple current has an impact on the DC load current at which the converter enters current limit. Ensure that the peak valley current at full load is less than the current limit threshold by an adequate margin. A recommended range is 60% to 80% of the current limit threshold.
- The ripple current has an impact on the RMS losses of the converter. The higher the ripple current, the higher the RMS losses.

6.3.7.2 Ramp Capacitor Selection

The TPS543B22 uses input voltage, duty cycle, and low-side FET current information to generate an internal ramp. The ramp amplitude is determined by an internal ramp generation capacitor, C_{RAMP}. Three different values for C_{RAMP} can be selected with a resistor to AGND on the MSEL pin (see セクション 6.3.9). The capacitor options are 1 pF, 2 pF, and 4 pF. A larger ramp capacitor results in a smaller ramp amplitude, which results in a higher control loop bandwidth. The following figures show how the loop changes with each ramp setting for the schematic in 図 7-1.

Many applications perform best with a C_{RAMP} value of 4 pF, however, the up to the user to measure the loop gain and phase to determine the optimum C_{RAMP} value for the specific application.

1. First, calculate the RAMP time constant using 式 5 and 表 6-4.

$$\tau_{CRAMP} = \frac{C_{RAMP} \times 10^6}{Lookup1 - Lookup2 \times \frac{V_{OUT}}{V_{IN}}} \quad (5)$$

表 6-4. RAMP Selection Lookup Values

f_{SW} (kHz)	Lookup1 Value	Lookup2 Value
500	0.372	0.297
750	0.548	0.445
1000	0.719	0.594
1500	1.04	0.891
2200	1.46	1.31

2. Next, calculate the RAMP capacitor voltage to ensure the capacitor chosen for C_{RAMP} does not result in a ramp amplitude of greater than 1.25 V, which ensures the ramp does not saturate to ground during a load transient.

$$V_{CRAMP} = \frac{V_{IN} \times (t_{ON} + 100\ ns)}{\tau_{CRAMP}} \quad (6)$$

- A larger C_{RAMP} capacitance results in highest loop gain.
- A smaller C_{RAMP} capacitance requires fewer output capacitors, and results in a higher crossover frequency.

図 6-7 and 図 6-8 show how the loop changes with each ramp setting for the schematic in セクション 7.

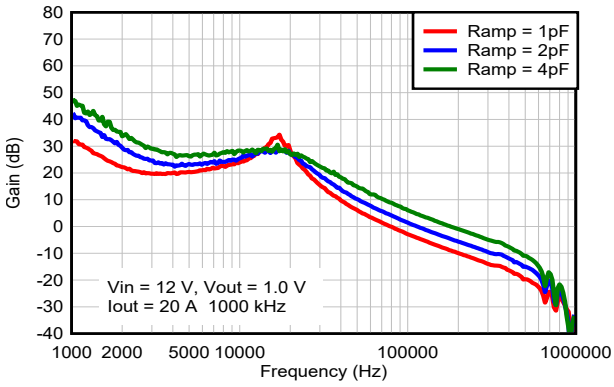


図 6-7. Loop Gain vs Ramp Settings

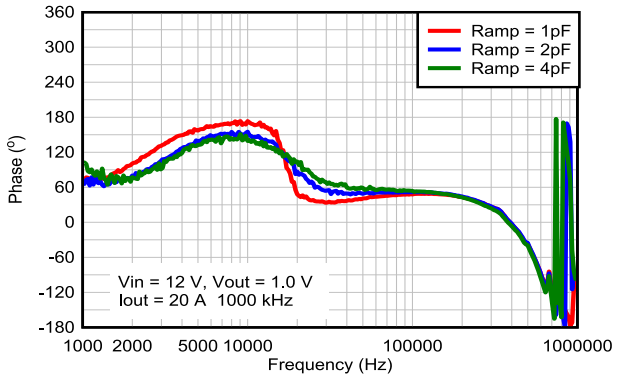


図 6-8. Loop Phase vs Ramp Settings

6.3.7.3 Output Capacitor Selection

- Ensure the ESR zero frequency of the capacitors used is at least 5× the expected crossover frequency. This way, the impact of the ESR on the loop gain is reduced to a manageable level.

$$f_{ESR\_ZERO} = \frac{1}{2\pi \times R_{ESR} \times C} \quad (7)$$

- The amount of output capacitance has a direct impact on the closed loop bandwidth of the converter. Too little capacitance and the bandwidth can be too high to maintain stability.
- The amount of output capacitance has a direct impact on output voltage overshoot during a load drop. Too little capacitance and the stored energy in the output inductor can cause the output voltage to overshoot during a sharp load decrease.
- The impedance of the output capacitance (impedance of the capacitors plus ESR) has an impact on the output ripple noise of the converter. Too high an impedance (due to not enough capacitance, too high ESR, or both) can result in output ripple above system requirements.

$$V_{RIPPLE} = \Delta I \times \left(R_{ESR} + \frac{1}{2\pi \times f_{SW} \times C} \right) \quad (8)$$

6.3.7.4 Design Method for Good Transient Response

The following method to design converter compensation optimizes the load transient response.

1. Calculate the require output impedance to meet transient response goals. This equation assumes the load step transient is faster than the BW of the converter.

$$Z_{OUT\_REQUIRED} = \frac{delta\_V_{OUT}}{delta\_I_{OUT}} \quad (9)$$

2. Select a value for output inductance.

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (10)$$

3. Calculate the required converter output impedance to meet the transient response goal.

$$Z_{OUT\_CONVERTER} = \frac{\left(0.00135 + \frac{L}{\tau_{CRAMP}} \right)}{34} \times \frac{V_{OUT}}{V_{REF}} \quad (11)$$

   Ensure $Z_{OUT\_CONVERTER}$ is less than the $Z_{OUT\_REQUIRED}$ found in step 1. Also recheck the voltage on C_{RAMP} is within acceptable limits. (see previous section) If it is too large, use a larger C_{RAMP} value.
4. Calculate the minimum output capacitance required to meet the impedance requirements.

$$C_{OUT\_MIN} = \frac{1}{2\pi \times Z_{OUT\_CONVERTER} \times f_{CO\_DESIRED}} \quad (12)$$

   where

   - $f_{CO\_DESIRED}$ is the desired converter closed loop crossover frequency, which is usually 1/8 to 1/4 of the converter switching frequency.
5. Calculate the number of output capacitors required. From the previous section, use the guidelines for ESR to select a capacitor type and value, then use the equation here to find the number of capacitors required. Notice that the *impedance* of the capacitors (ESR plus impedance of the capacitance itself at the chosen crossover frequency) is used.

$$Z_{CAPACITOR} = R_{ESR\_CAPACITOR} + \frac{1}{2\pi \times C_{CAPACITOR} \times F_{CO}} \quad (13)$$

$$N_{CAPACITORS} = \frac{Z_{CAPACITOR}}{Z_{OUT\_CONVERTER}} \quad (14)$$

6. Using one of the tools on TI.com, simulate with the values for the design.

6.3.8 Soft Start and Prebiased Output Start-Up

During start-up, the device softly increases the reference voltage from zero to the final value, thereby reducing converter inrush current. There are four options for the soft-start time, which is the time it takes for the reference to ramp to 0.5 V:

- 1 ms
- 2 ms
- 4 ms
- 8 ms

The soft-start time is selected with a resistor to AGND on the MSEL pin. See セクション 6.3.9.

If a prebiased output condition exists prior to start-up, the device prevents current from being discharged from the output. During monotonic prebiased start-up, the low-side MOSFET is not allowed to sink current until the SS

pin voltage is higher than the FB pin voltage and the high-side MOSFET begins to switch. The one exception is if the BOOT-SW voltage is below the UVLO threshold. While in BOOT-SW UVLO, the low-side MOSFET is allowed to turn on to charge the BOOT capacitor. The low-side MOSFET reverse current protection provides another layer of protection for the device after the high-side MOSFET begins to switch.

6.3.9 MSEL Pin

The ramp amplitude, soft-start time, and current limit settings are programmed with a single resistor, R_{MSEL}, from MSEL to AGND. 表 6-5 lists the resistor values for the available options. Use a 1% tolerance resistor or better. See セクション 6.3.11.1 for the corresponding current limit thresholds for the "High" and "Low" settings.

表 6-5. MSEL Pin Selection

R_{MODE} (kΩ)	Current Limits	C_{RAMP} (pF)	Soft-Start Time (ms)
1.78	High	1	1
2.21	High	1	2
2.74	High	1	4
3.32	High	1	8
4.02	High	2	1
4.87	High	2	2
5.9	High	2	4
7.32	High	2	8
9.09	High	4	1
11.3	High	4	2
14.3	High	4	4
18.2	High	4	8
22.1	Low	1	1
26.7	Low	1	2
33.2	Low	1	4
40.2	Low	1	8
49.9	Low	2	1
60.4	Low	2	2
76.8	Low	2	4
102	Low	2	8
137	Low	4	1
174	Low	4	2
243	Low	4	4
412	Low	4	8

6.3.10 Power Good (PG)

The TPS543B22 PG pin is an open-drain output requiring an external pullup resistor to output a high signal. After the FB pin is between 92% and 108% of the internal voltage reference, soft start is complete, and after a 256-µs deglitch time, the PG pin is de-asserted and the pin floats. TI recommends a pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. PG is in a defined state after the VIN input voltage is greater than 1 V but with reduced current sinking capability. When the FB is lower than 84% or greater than 116% of the nominal internal reference voltage, after a 8-µs deglitch time, the PG pin is pulled low. PG is immediately pulled low if VIN falls below the UVLO, the EN pin is pulled low or the device enters thermal shutdown.

6.3.11 Output Overload Protection

The TPS543B22 protects against output overload (that is, overcurrent) events by cycle-by-cycle current limiting both the high-side MOSFET and low-side MOSFET. In an extended overcurrent condition, the device enters hiccup mode. Different protections are active during positive inductor current and negative inductor current conditions.

6.3.11.1 Positive Inductor Current Protection

Current is sensed in the high-side MOSFET while it is conducting after a short blanking time to allow noise to settle. Whenever the high-side overcurrent threshold is exceeded, the high-side MOSFET is immediately turned off and the low-side MOSFET is turned on. The high-side MOSFET does not turn back on until the current falls below the low-side MOSFET overcurrent threshold, effectively limiting the peak current in the case of a short-circuit condition. If a high-side overcurrent is detected for 15 consecutive cycles, the device enters hiccup mode.

The current is also sensed in the low-side MOSFET while it is conducting after a short blanking time to allow noise to settle. If the low-side overcurrent threshold is exceeded when the next incoming PWM signal is received from the controller, the device skips processing that PWM pulse. The device does not turn the high-side MOSFET on again until the low-side overcurrent threshold is no longer exceeded. If the low-side overcurrent threshold remains exceeded for 15 consecutive cycles, the device enters hiccup. There are two separate counters for the high-side and low-side overcurrent events. If the off time is too short, the low-side overcurrent can not trip. The low-side overcurrent, however, begins tripping after the high-side peak overcurrent limit is crossed, as exceeding the peak current limit shortens the on time and lengthens the off time.

Both the high-side and low-side positive overcurrent thresholds are programmable using the MSEL pin. Two sets of thresholds are available ("High" and "Low"), which are summarized in 表 6-6. The values for these thresholds are obtained using open-loop measurements with a DC current to accurately specify the values. In real applications, the inductor current ramps and the ramp rate is a function of the voltage across the inductor (V_{IN} – V_{OUT}) as well as the inductance value. The ramp rate combined with delays in the current sense circuitry then results in slightly different values than specified. The current at which the high-side overcurrent limit takes effect can be slightly higher than specified, and the current at which the low-side overcurrent limit takes effect can be slightly lower than specified.

表 6-6. Overcurrent Thresholds

MSEL Current Limit Setting	High-Side Overcurrent Typical Value (A)	Low-Side Overcurrent Typical Value (A)
High	29	22
Low	23	17.6

6.3.11.2 Negative Inductor Current Protection

Negative current is sensed in the low-side MOSFET while it is conducting after a short blanking time to allow noise to settle. Whenever the low-side negative overcurrent threshold is exceeded, the low-side MOSFET is immediately turned off. The next high-side MOSFET turn-on is determined by the clock and PWM comparator. The negative overcurrent threshold minimum value is 7 A. Similar to the positive inductor current protections, the actual value of the inductor current when the current sense comparators trip is a function of the current ramp rate. As a result, the current at which the negative inductor current limit takes effect can be slightly more negative than specified.

6.3.12 Output Overvoltage and Undervoltage Protection

The TPS543B22 incorporates both output overvoltage and undervoltage protection. If an overvoltage is detected, the device tries to discharge the output voltage to a safe level before attempting to restart. When the overvoltage threshold is exceeded, the low-side MOSFET is turned on until the low-side negative overcurrent threshold is reached. At this point, the high-side MOSFET is turned on until the inductor current reaches zero. Then, the low-side MOSFET is turned back on until the low-side negative overcurrent threshold is reached. The

process repeats until the output voltage falls back into the PG window. After this happens, the device restarts and goes through a soft start cycle. The device does not wait the hiccup time before restarting.

When an undervoltage condition is detected, the device enters hiccup where it waits seven soft-start cycles before restarting. Undervoltage protection is enabled after soft start is complete.

6.3.13 Overtemperature Protection

When the die temperature exceeds 165°C, the device turns off. After the die temperature cools below the hysteresis level, typically by 12°C, the device restarts. While waiting for the temperature to fall below the hysteresis level, the device does not switch or attempt to hiccup to restart. After the temperature falls below the hysteresis level, the device restarts without going through hiccup.

6.3.14 Output Voltage Discharge

When the TPS543B22 is enabled, but the high-side FET and low-side FET are disabled due to a fault condition, the output voltage discharge mode is enabled, turning on the discharge FET from SW to PGND to discharge the output voltage. The discharge FET is turned off when the converter is ready to resume switching, either after the fault clears or after the wait time before hiccup is over.

The output voltage discharge mode is activated by any of the following fault events:

- High-side or low-side positive overcurrent
- Thermal shutdown
- Output voltage undervoltage
- VIN UVLO

6.4 Device Functional Modes

6.4.1 Forced Continuous-Conduction Mode

The TPS543B22 operates in forced continuous-conduction mode (FCCM) throughout normal operation.

6.4.2 Discontinuous Conduction Mode During Soft Start

At the beginning of soft start, the converter operates in discontinuous conduction mode (DCM) for the first 16 PWM cycles. During this time, a zero-cross detect comparator is used to turn off the low-side MOSFET when the current reaches zero amps, preventing the discharge of any prebiased conditions on the output. After the 16 cycles of DCM, the converter enters FCCM mode for the remainder of start-up and into regulation.

7 Application and Implementation

注

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7.1 Application Information

The TPS543B22 is a synchronous buck converter designed for 4-V to 18-V input and 20-A load. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors.

7.2 Typical Applications

7.2.1 1.0-V Output, 1-MHz Application

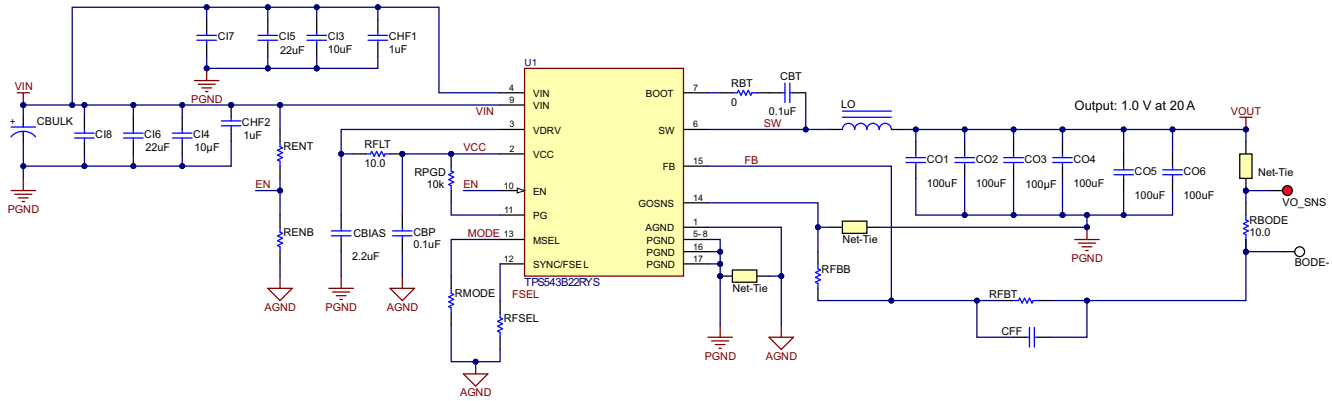

図 7-1. 12-V Input, 1.0-V Output, 1-MHz Schematic

7.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 7-1.

表 7-1. Design Parameters

Parameter	Example Value
Input voltage range (V_{IN})	4.5 to 18 V, 12-V nominal
Output voltage (V_{OUT})	1.0 V
Output current rating (I_{OUT})	20 A
Switching frequency (f_{SW})	1000 kHz
Steady state output ripple voltage	10 mV
Output current load step	10 A
Transient response	± 50 mV (± 5%)

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS543B22 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability. In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.1.2.2 Switching Frequency

The first step is to decide on a switching frequency. The TPS543B22 can operate at five different frequencies from 500 kHz to 2.2 MHz. f_{SW} is set by the resistor value from the FSEL pin to ground. Typically, the highest switching frequency possible is desired because it produces the smallest design size. A high switching frequency allows for smaller inductors and output capacitors compared to a power supply that switches at a lower frequency. The main tradeoff made with selecting a higher switching frequency is extra switching power loss, which hurts the efficiency of the regulator.

The maximum switching frequency for a given application can be limited by the minimum on time of the regulator and the maximum f_{SW} can be estimated with 式 15. Using the maximum minimum on time of 40 ns and 18.0-V maximum input voltage for this application, the maximum switching frequency is 1389 kHz. The selected switching frequency must also consider the tolerance of the switching frequency. A switching frequency of 1000 kHz was selected for a good balance of design size and efficiency. To set the frequency to 1000 kHz the selected FSEL resistor is 11.8 kΩ per 表 6-1.

$$f_{SW}(max) = \frac{1}{t_{on\,min}} \times \frac{V_{OUT}}{V_{IN}(max)} \tag{15}$$

図 7-2 shows the maximum recommended input voltage versus output voltage for each FSEL frequency. This graph uses the maximum minimum on time of 40 ns and includes 10% tolerance on the switching frequency.

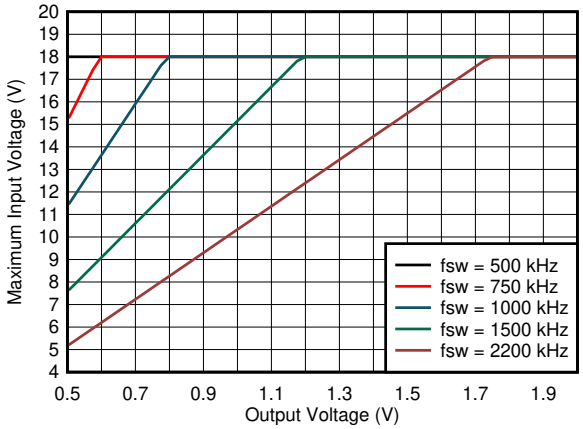

図 7-2. Maximum Input Voltage vs Output Voltage

7.2.1.2.3 Output Inductor Selection

To calculate the value of the output inductor, use 式 16. K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Choosing small inductor ripple currents can degrade the transient response performance. The inductor ripple, K_{IND}, is normally from 0.1 to 0.4 for the majority of applications giving a peak to peak ripple current range of 2 A to 8 A. The target I_{RIPPLE} must be 1 A or larger.

For this design example, K_{IND} = 0.2 is used and the inductor value is calculated to be 0.236 µH. An inductor with an inductance of 0.220 µH is selected. It is important that the RMS (root mean square) current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from 式 18 and 式 19. For this design, the RMS inductor current is 20.46 A, and the peak inductor current is 22.1 A. The chosen inductor is a SLR1050A-221. The inductor has a saturation current rating of 35 A, an RMS current rating of 56.7 A, and a typical DC series resistance of 0.39 mΩ.

The peak current through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated in 式 19. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify the current ratings of the inductor based on the switch current limit rather than the steady-state peak inductor current.

$$L1 = \frac{(V_{IN} - V_{OUT})}{Io \times K_{IND}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \tag{16}$$

$$I_{ripple} = \frac{(V_{INMAX} - V_{OUT})}{L1} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \tag{17}$$

$$IL_{rms} = \sqrt{{I_O}^2 + \frac{1}{12} \times \left(\frac{(V_{INMAX} - V_{OUT})}{L1} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}\right)^2} \tag{18}$$

$$IL_{peak} = I_{OUT} + \frac{I_{ripple}}{2} \tag{19}$$

7.2.1.2.4 Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output voltage ripple and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these criteria.

The desired response to a large change in the load current is the first criteria and is typically the most stringent. A regulator does not respond immediately to a large, fast increase or decrease in load current. The output capacitor supplies or absorbs charge until the regulator responds to the load step. The control loop must sense the change in the output voltage then adjust the peak switch current in response to the change in load. The minimum output capacitance is selected based on an estimate of the loop bandwidth. Typically, the loop bandwidth is near f_{SW} / 10. 式 20 estimates the minimum output capacitance necessary.

For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 10 A . Therefore, ΔI_{OUT} is 10 A and ΔV_{OUT} is 50 mV. Using this target gives a minimum capacitance of 318 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the effect of the ESR can be small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be considered for load step response.

$$C_{OUT} > \frac{\Delta I_{OUT}}{\Delta V_{OUT}} \times \frac{1}{2\pi \times \frac{f_{SW}}{10}} \tag{20}$$

where

- ΔI_{OUT} is the change in output current.
- ΔV_{OUT} is the allowable change in the output voltage.

In addition to the loop bandwidth, it is possible for the inductor current slew rate to limit how quickly the regulator responds to the load step. For low duty cycle applications, the time it takes for the inductor current to ramp down after a load step down can be the limiting factor. 式 21 estimates the minimum output capacitance necessary to limit the change in the output voltage after a load step down. Using the 0.22-µH inductance selected gives a minimum capacitance of 91 µF.

$$C_{OUT} > \frac{L_{OUT} \times \Delta I_{OUT}^{2}}{2 \times \Delta V_{OUT} \times V_{OUT}} \tag{21}$$

式 22 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the target maximum steady state output voltage ripple is 10 mV. Under this requirement, 式 22 yields 52 µF.

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \tag{22}$$

where

- ΔI_{OUT} is the change in output current.
- ΔV_{OUT} is the allowable change in the output voltage.
- f_{SW} is the regulators switching frequency.
- $V_{ORIPPLE}$ is the maximum allowable steady state output voltage ripple.
- I_{RIPPLE} is the inductor ripple current.

Lastly, if an application does not have a strict load transient response or output ripple requirement, a minimum amount of capacitance is still required to ensure the control loop is stable with the lowest gain ramp setting on the MODE pin. 式 23 estimates the minimum capacitance needed for loop stability. 式 23 sets the minimum amount of capacitance by keeping the LC frequency relative to the switching frequency at a minimum value. See 図 7-3 for the limit versus output voltage with the lowest gain ramp setting of 1 pF. With a 1-V output, the minimum ratio is 35 and with this ratio, 式 23 gives a minimum capacitance of 141 µF.

$$C_{OUT} > \left(\frac{Ratio}{2\pi \times f_{SW}} \right)^{2} \times \frac{1}{L_{OUT}} \tag{23}$$

式 24 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification and this shows the ESR must be less than 6 mΩ. In this case, ceramic capacitors are used and the combined ESR of the ceramic capacitors in parallel is much less than is needed to meet the ripple. Capacitors also have limits to the amount of ripple current they can handle without producing excess heat and failing. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheet specifies the RMS value of the maximum ripple current. 式 25 can be used to calculate the RMS ripple current the output capacitor must support. For this application, 式 25 yields 1.2 A and ceramic capacitors typically have a ripple current rating much higher than this.

$$Resr < \frac{Voripple}{Iripple} \tag{24}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \quad (25)$$

Select X5R and X7R ceramic dielectrics or equivalent for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias and AC voltage derating taken into account. The derated capacitance value of a ceramic capacitor due to DC voltage bias and AC RMS voltage is usually found on the capacitor manufacturer's website. For this application example, six 100-µF, 10-V, X5R, 1210 ceramic capacitors each with 3 mΩ of ESR are used. With the six parallel capacitors, the estimated effective output capacitance after derating using the capacitor manufacturer's website is 570 µF. There is about -5% DC bias derating at 1 V. This design was able to use less than the calculated minimum because the loop crossover frequency was above the f_{SW} / 10 estimate as shown in 図 7-8.

7.2.1.2.5 Input Capacitor

Input decoupling ceramic capacitors type X5R, X7R, or similar from VIN to PGND that are placed as close as possible to the IC are required. A total of at least 66 µF of capacitance is required and some applications can require a bulk capacitance. TI recommends at least 1 µF of bypass capacitance as close as possible to each VIN pin to minimize the input voltage ripple. A 1-µF capacitor must be placed as close as possible to both VIN pins 4 and 9 on the same side of the board of the device to provide high frequency bypass to reduce the high frequency overshoot and undershoot on VIN and SW pins. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum RMS input current. The RMS input current can be calculated using 式 26.

For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. Two 22-µF, 1210, X7R, 25-V, two 10-µF, 0805, X7S, 25-V, and two 1-µF, 0402 or 0603, X7R 25-V capacitors in parallel has been selected to be placed on both sides of the IC near both VIN pins to PGND pins. Based on the capacitor manufacturer's website, the total ceramic input capacitance derates to 25 µF at the nominal input voltage of 12 V. Additional 100-µF ceramic capacitance and 220-µF aluminum electrolytic are also used to bypass long leads when connected a lab bench top power supply.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 26. The maximum input ripple occurs when operating nearest to 50% duty cycle. Using the nominal design example values of $I_{OUT(MAX)}$ = 20 A , C_{IN} = 25 µF, and f_{SW} = 1000 kHz, the input voltage ripple with the 12-V nominal input is 61 mV and the RMS input ripple current with the 4.5-V minimum input is 8.3 A.

$$I_{CINRMS} = I_{OUT} \times \sqrt{\frac{(V_{INMIN} - V_{OUT})}{V_{INMIN}} \times \frac{V_{OUT}}{V_{INMIN}}} \quad (26)$$

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}}{C_{IN} \times fsw} \quad (27)$$

7.2.1.2.6 Adjustable Undervoltage Lockout

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply is set to turn on and start switching after the input voltage increases above 4.5 V (UVLO start or enable). After the regulator starts switching, it continues to do so until the input voltage falls below 3.95 V (UVLO stop or disable). In this example, these start and stop voltages set by the EN resistor divider were selected to have more hysteresis than the internally fixed VIN UVLO.

式 1 and 式 2 can be used to calculate the values for the upper and lower resistor values. For these equations to work, V_{START} must be 1.1 × V_{STOP} due to the voltage hysteresis of the EN pin. For the voltages specified, the standard resistor value used for R_{ENT} is 16.9 kΩ and for R_{ENB} is 6.04 kΩ.

7.2.1.2.7 Output Voltage Resistors Selection

The output voltage is set with a resistor divider created by R_{FBT} and R_{FBB} from the output node to the FB pin. Use 1% tolerance or better resistors. For this example design, 4.99 kΩ was selected for R_{FBB}. Using 式 28, R_{FBT} is calculated as 4.99 kΩ. This is a standard 1% resistor.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{28}$$

If the PCB layout does not use the recommended AGND to PGND connection in セクション 7.4.1, noise on the feedback pin can degrade the output voltage regulation at maximum load. Using a smaller R_{FBB} of 1.00 kΩ minimizes the impact of this noise.

7.2.1.2.8 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. The capacitor must be rated for at least 10-V to minimize DC bias derating.

A resistor can be added in series with the BOOT capacitor to slow down the turn on of the high-side MOSFET and reduce overshoot rising edge overshoot on the SW pin. This comes with the tradeoff of more power loss and lower efficiency. As a best practice, include a 0-Ω placeholder in prototype designs in case parasitic inductance in the PCB layout results in more voltage overshoot at the SW pin than is normal. This helps keep the voltage within the ratings of the device and reduces the high frequency noise on the SW node.

7.2.1.2.9 VDRV and VCC Capacitor Selection

A 2.2-µF ceramic capacitor must be connected between the VDRV pin and PGND for proper operation. The capacitor must be rated for at least 10 V to minimize DC bias derating. The VDRV pin is the output of an internal linear regulator and the supply to the gate drivers. The VCC pin is the supply for the analog control circuits and must have a 0.1-µF and 10-V rated or better ceramic capacitor connected from VCC to AGND. A 10-Ω 0402 resistor must be connected between the VDRV to VCC pins.

7.2.1.2.10 PGOOD Pullup Resistor

A 10-kΩ resistor is used to pull up the power-good signal when FB conditions are met. The pullup voltage source must be less than the 6-V absolute maximum of the PGOOD pin.

7.2.1.2.11 Current Limit Selection

The MODE pin is used to select between two current limit settings. Select the current limit setting whose minimum is greater than at least 1.1 times the maximum steady state peak current. This is to provide margin for component tolerance and load transients. For this design, the minimum current limit must be greater than 7.45 A so the high current limit setting is selected.

7.2.1.2.12 Soft-Start Time Selection

The MODE pin is used to select between four different soft-start times, which is useful if a load has specific timing requirements for the output voltage of the regulator. A longer soft-start time is also useful if the output capacitance is very large and requires large amounts of current to quickly charge the output capacitors to the output voltage level. The large currents necessary to charge the capacitor can reach the current limit or cause the input voltage rail to sag due excessive current draw from the input power supply. Limiting the output voltage slew rate solves both of these problems. The example design has the soft-start time set to 1.0 ms. With this soft-start time, the current required to charge the output capacitors to the nominal output voltage is only 0.14 A.

7.2.1.2.13 Ramp Selection and Control Loop Stability

The MODE pin is used to select between three different ramp settings. The most optimal ramp setting depends on V_{OUT}, f_{SW}, L_{OUT}, and C_{OUT}. To get started, calculate LC double pole frequency using 式 29. Then calculate the ratio between f_{SW} and f_{LC}. Based on this ratio and the output voltage, select the recommended ramp setting using 図 7-3. With a 1-V output, TI recommends the 1-pF ramp for ratios between approximately 35 and 58, TI recommends the 2-pF ramp for ratios between approximately 58 and 86, and TI recommends the 4-pF ramp for ratios greater than approximately 86. In general, use the largest ramp capacitor the design can support. Increasing the ramp capacitor improves transient response but can reduce stability margin or increase on-time jitter.

For this design, f_{LC} is 17.5 kHz and the ratio is 57 which is on the border of the 1-pF and 2-pF ramp settings. Through bench evaluation, it was found the design had sufficient stability margin with the 2-pF ramp so this setting was selected for the best transient response. The recommended ramp settings given by 図 7-3 include margin to account for potential component tolerances and variations across operating conditions so it is possible to use a higher ramp setting as shown in this example.

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{29}$$

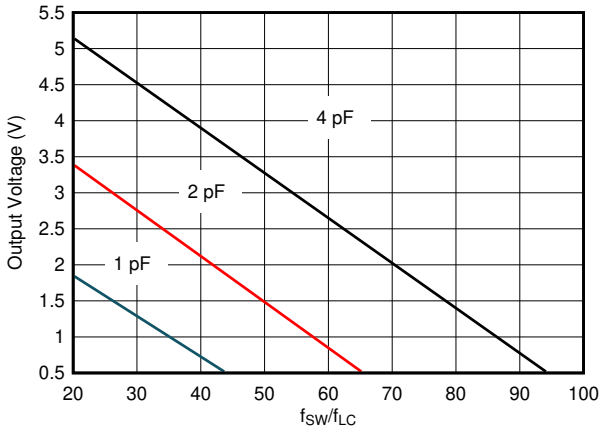

図 7-3. Recommended Ramp Settings

Use a feedforward capacitor (C_{FF}) in parallel with the upper feedback resistor (R_{FBT}) to add a zero into the control loop to provide phase boost. Include a placeholder for this capacitor as the zero it provides can be required to meet phase margin requirements. This capacitor also adds a pole at a higher frequency than the zero. The pole and zero frequency are not independent so as a result, after the zero location is chosen, the pole is fixed as well. The zero is placed at 1 / 4 the f_{SW} by calculating the value of C_{FF} with 式 30. The calculated value is 128 pF — round this down to the closest standard value of 120 pF.

Using bench measurements of the AC response, the feedforward capacitor for this example design was increased to 180 pF to improve the transient response.

$$C_{FF} = \frac{1}{\pi \times R_{FBT} \times \frac{f_{SW}}{2}} \tag{30}$$

Using a larger feedforward capacitors to further improve the transient response but take care to ensure there is a minimum of –9-dB gain margin in all operating conditions is possible. The feedforward capacitor injects noise on the output into the FB pin. This added noise can result in increased on-time jitter at the switching node. Too little gain margin can cause a repeated wide and narrow pulse behavior. Adding a 100-Ω resistor in series with the feedforward capacitor can help reduce the impact of noise on the FB pin in case of non-ideal PCB layout. The value of this resistor must be kept small as larger values bring the feedforward pole and zero closer together degrading the phase boost the feedforward capacitor provides.

When using higher ESR output capacitors, such as polymer or tantalum, the ESR zero (f_{ESR}) must be accounted for. The ESR zero can be calculated using 式 31. If the ESR zero frequency is less than the estimated bandwidth of 1/10th the f_{SW}, it can affect the gain margin and phase margin. A series R-C from the FB pin to ground can be used to add a pole into the control loop if necessary. All ceramic capacitors are used in this design so the effect of the ESR zero is ignored.

$$f_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} \tag{31}$$

7.2.1.2.14 MODE Pin

The MODE resistor is set to 4.87 kΩ to select the high current limit setting, 2.0-ms soft-start, and the 2-pF ramp. See 表 6-5 for the full list of the MODE pin settings.

7.2.1.3 Application Curves

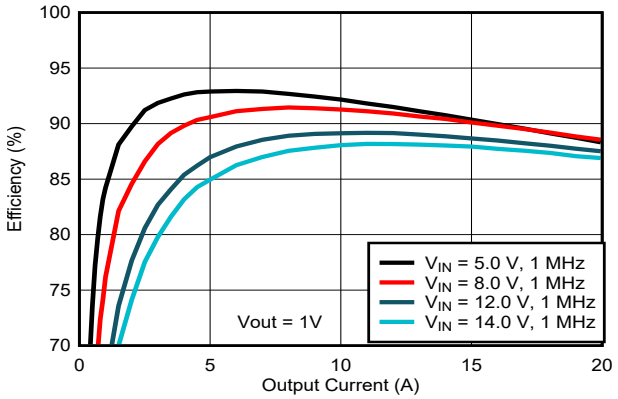

図 7-4. Efficiency Curves

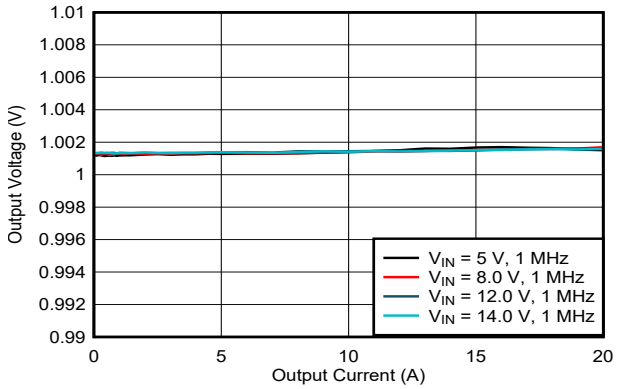

図 7-5. Load Regulation

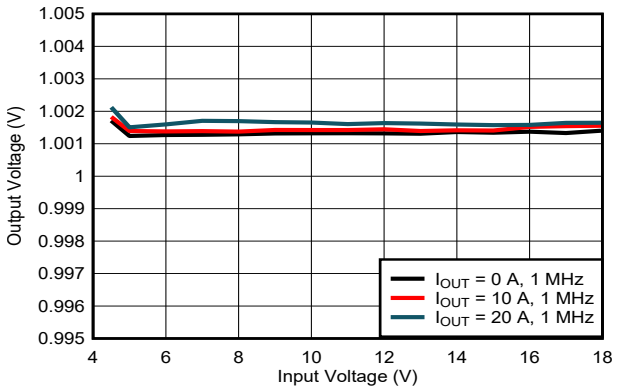

図 7-6. Line Regulation

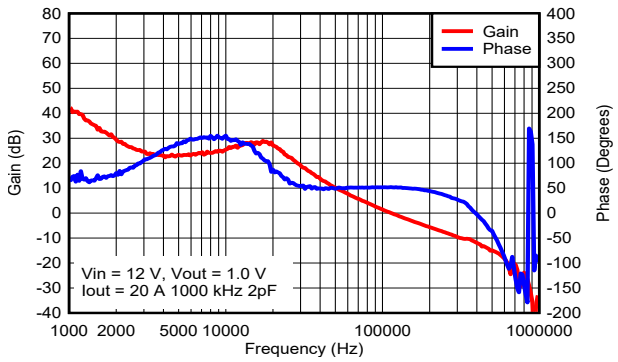

図 7-7. Bode Plot

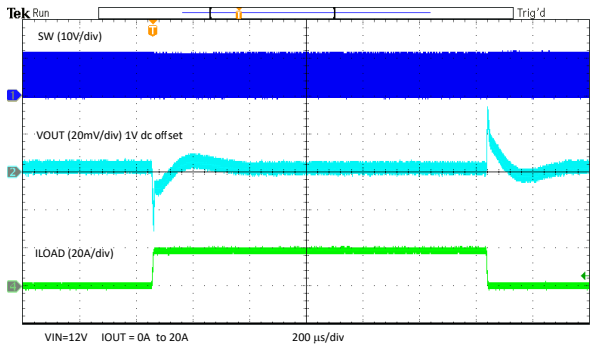

図 7-8. Load Transient

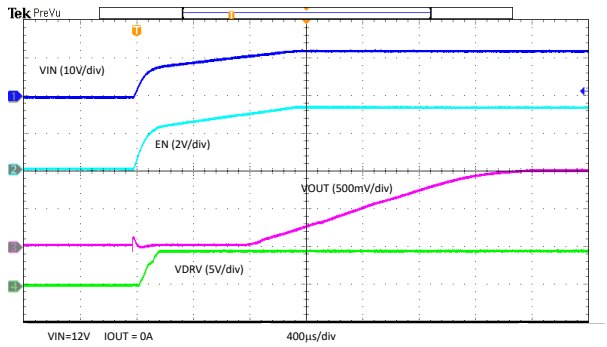

図 7-9. EN Start-up – Measuring BP5

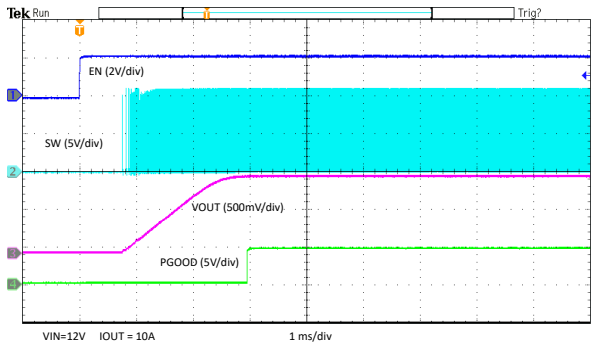

図 7-10. EN Start-up – Measuring SW

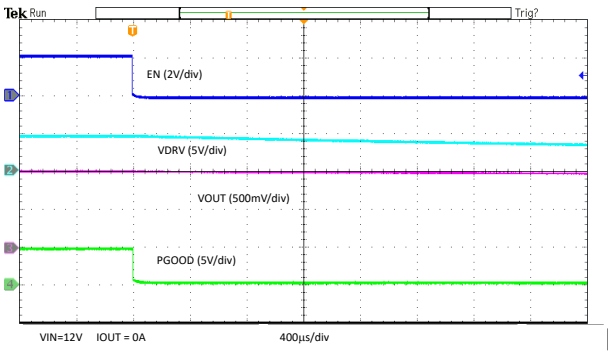

図 7-11. EN Shutdown

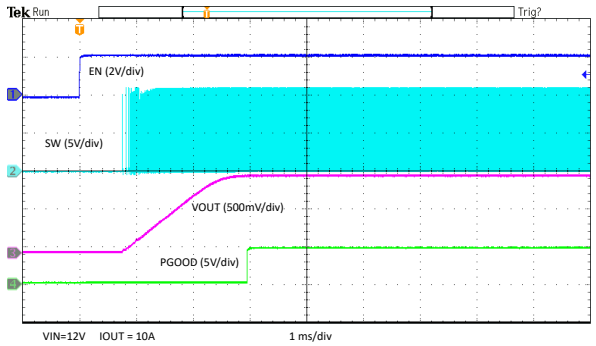

図 7-12. EN Start-up – with Load

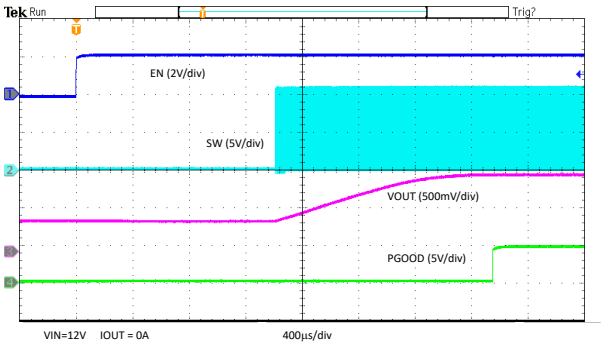

図 7-13. EN Start-up – 0.5-V Prebias

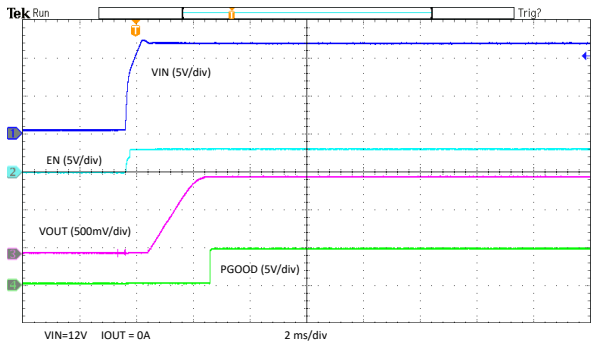

図 7-14. V_{IN} Start-up

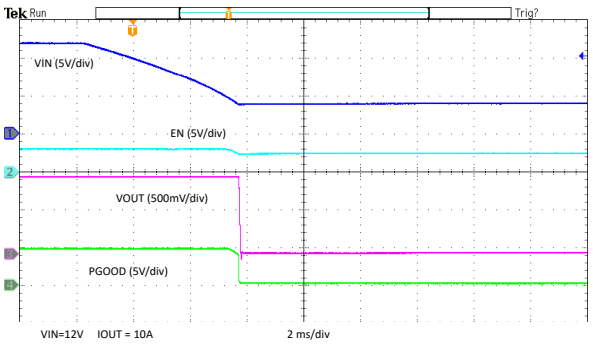

図 7-15. V_{IN} Shutdown

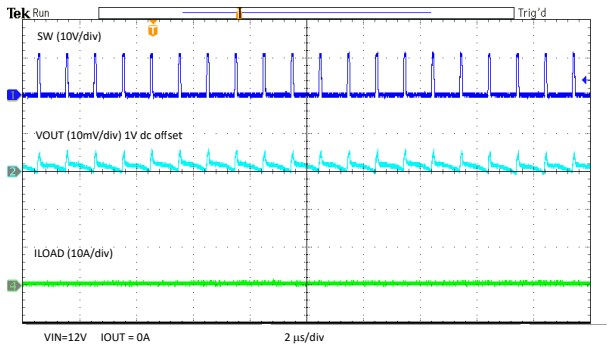

図 7-16. Output Ripple – No Load

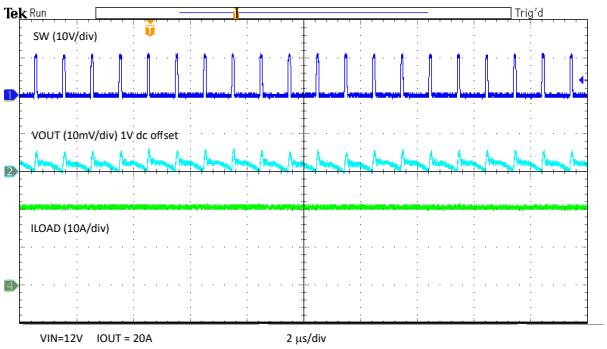

図 7-17. Output Ripple – Full Load

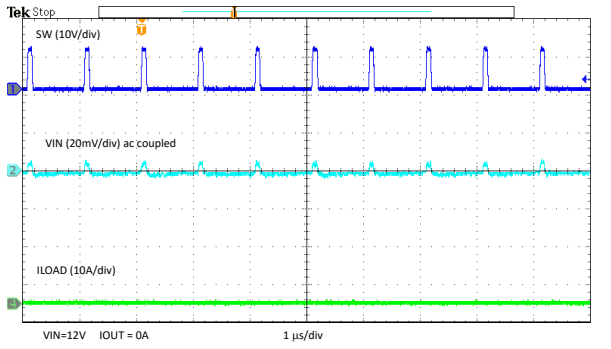

図 7-18. Input Ripple – No Load

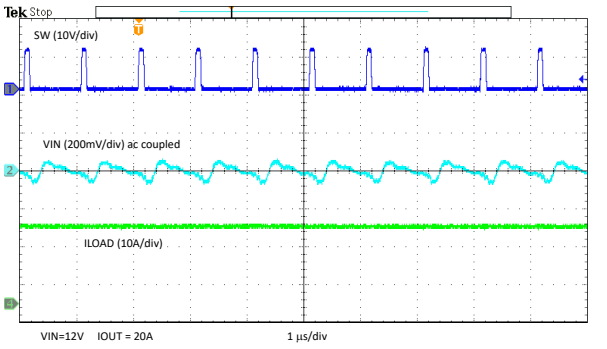

図 7-19. Input Ripple – Full Load

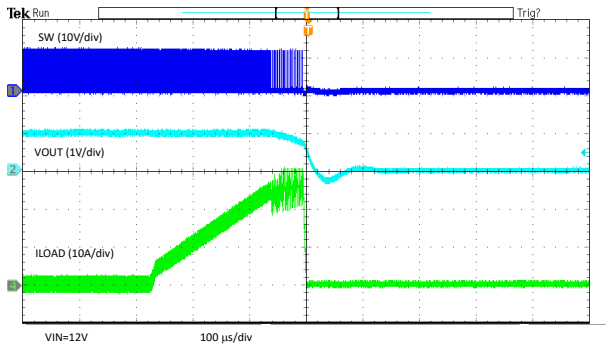

図 7-20. Overcurrent Protection – Overload

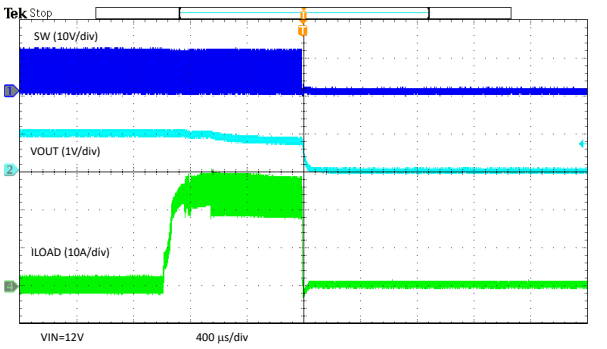

図 7-21. Overcurrent Protection – Short

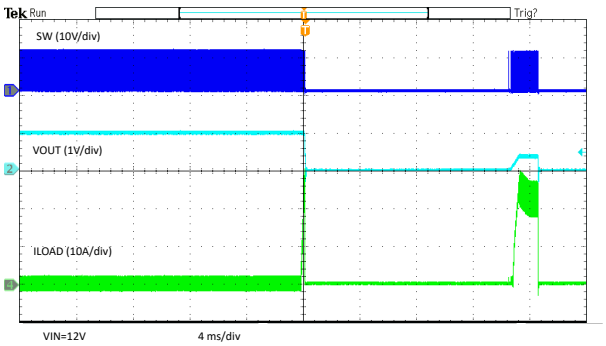

図 7-22. Overcurrent Protection – Hiccup and Recover

7.3 Power Supply Recommendations

The TPS543B22 is designed to operate from an input voltage supply range between 4 V and 18 V. This supply voltage must be well regulated. Proper bypassing of the input supply is critical for proper electrical performance, as is the PCB layout and the grounding scheme. A minimum of 10-µF (after derating) ceramic capacitance, type X5R or better, must be placed near the device. TI recommends splitting the ceramic input capacitance equally between the VIN and PGND pins on each side of the device resulting in at least 5 µF of ceramic capacitance on each side of the device.

7.4 Layout

7.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. See 図 7-23 for a PCB layout example. Key guidelines to follow for the layout are:

- Make VIN, PGND, and SW traces as wide as possible to reduce trace impedance and improve heat dissipation. Use vias and traces on others layers to reduce VIN and PGND trace impedance.
- Use multiple vias near the PGND pins and use the layer directly below the device to connect them together, which helps to minimize noise and can help heat dissipation.
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer.
- Place a 1-µF/25-V/X6R or better dielectric ceramic capacitors from each VIN to PGND pins and place them as close as possible to the device on the same side of the PCB. Place the remaining ceramic input capacitance next to these high frequency bypass capacitors. The remaining input capacitance can be placed on the other side of the board but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Place the inductor as close as possible to the device to minimize the length of the SW node routing.
- Place the BOOT-SW capacitor as close as possible to the BOOT and SW pins. Use a 0.1-µF/16-V/X6R or better dielectric ceramic capacitor for the BOOT capacitor.
- Place the 2.2-µF/10-V/X6R or better dielectric ceramic capacitor as close as possible to the VDRV and PGND pins.
- Connect 10-Ω resistor from VDRV to VCC and a 0.1-µF/10-V/X6R or better dielectric ceramic capacitor from VCC to AGND.
- Place the bottom resistor in the FB divider as close as possible to the FB and GOSNS pins of the IC. Also keep the upper feedback resistor and the feedforward capacitor near the IC. Connect the FB divider to the output voltage at the desired point of regulation.
- Use vias on the AGND islands on top layer to connect to AGND layer island on an internal layer. Connect the internal AGND island to PGND at one point.
- Return the FSEL and MODE resistors to a quiet AGND island.

7.4.2 Layout Example

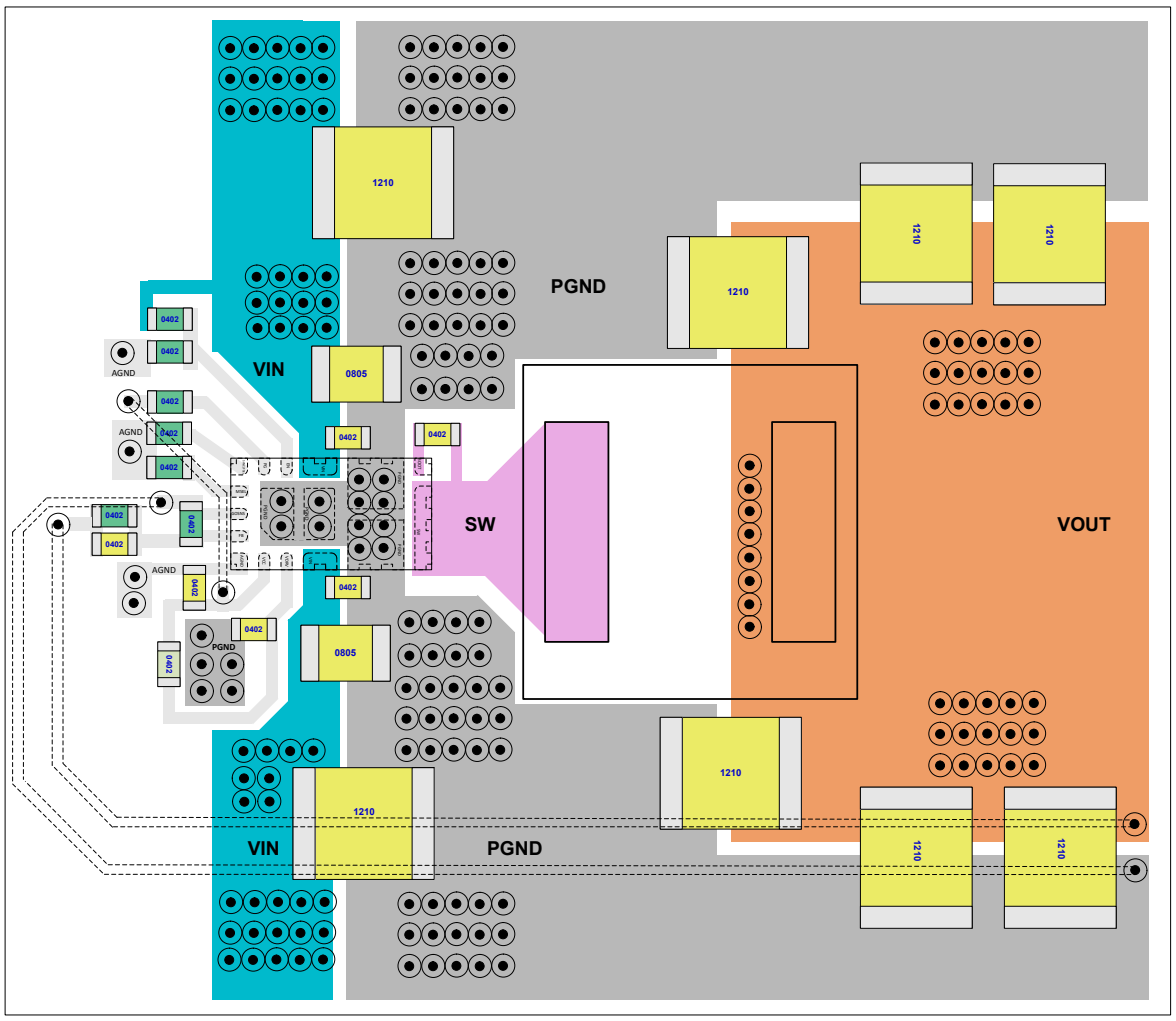

図 7-23. Example PCB Layout

7.4.3 Thermal Performance

Test conditions: f_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1 V, I_{OUT} = 20 A, Inductor = 220 nH (0.325 mΩ typical), ambient temperature = 25°C

図 7-24. Thermal Image at 25°C Ambient

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS543B22 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability. In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2022) to Revision B (February 2024)	Page
• 新しいデバイスのハイパーリンクを追加	1
• WEBENCH のコンテンツを追加	1
• Added WEBENCH content	23
• Added WEBENCH content	37

Changes from Revision * (August 2022) to Revision A (December 2022)	Page
• ステータスを「事前情報」から「量産データ」に変更	1
• 最初の公開リリース	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS543B22RYSR	Active	Production	WQFN-FCRLF (RYS) | 17	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T543B22
TPS543B22RYSR.A	Active	Production	WQFN-FCRLF (RYS) | 17	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T543B22

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

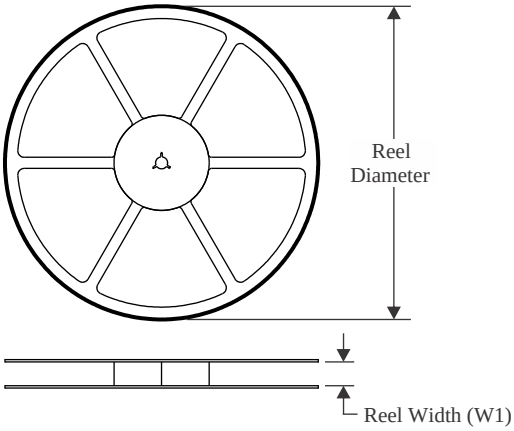
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

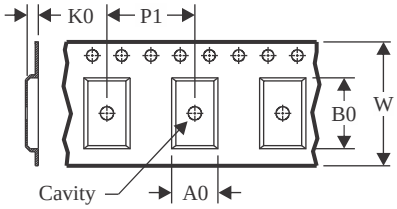
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

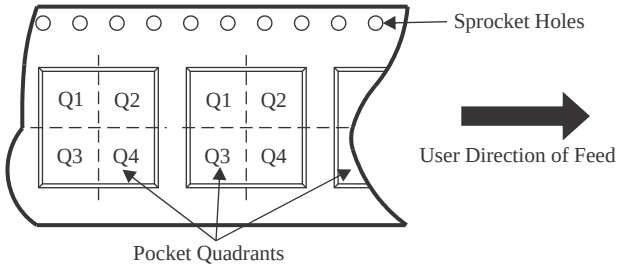


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

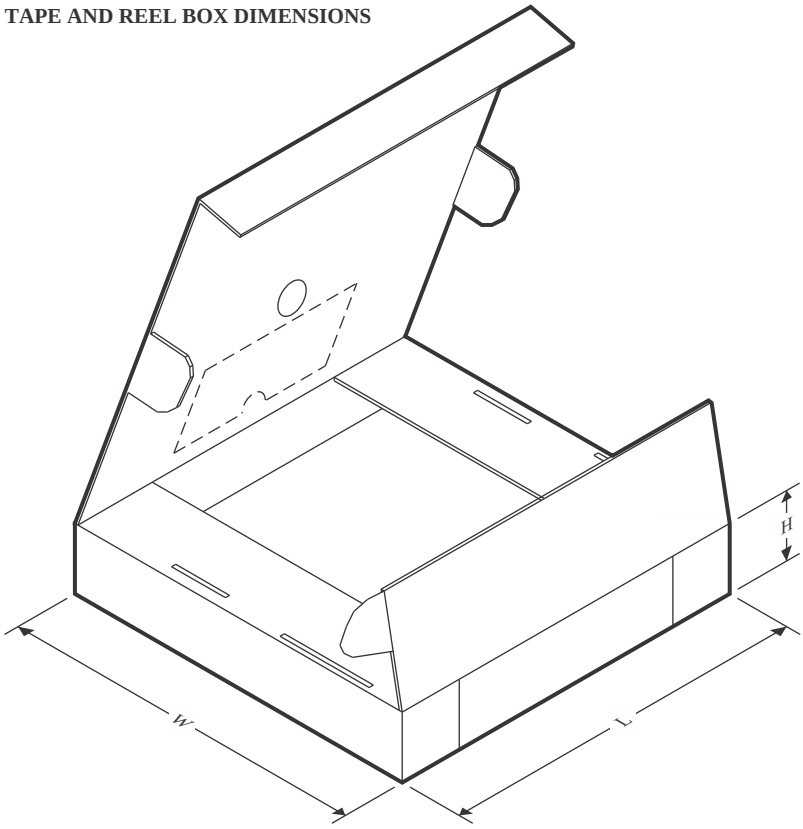
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS543B22RYSR	WQFN-FCRLF	RYS	17	5000	330.0	12.4	2.7	4.75	0.9	8.0	12.0	Q1
TPS543B22RYSR	WQFN-FCRLF	RYS	17	5000	330.0	12.4	2.7	4.75	0.9	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

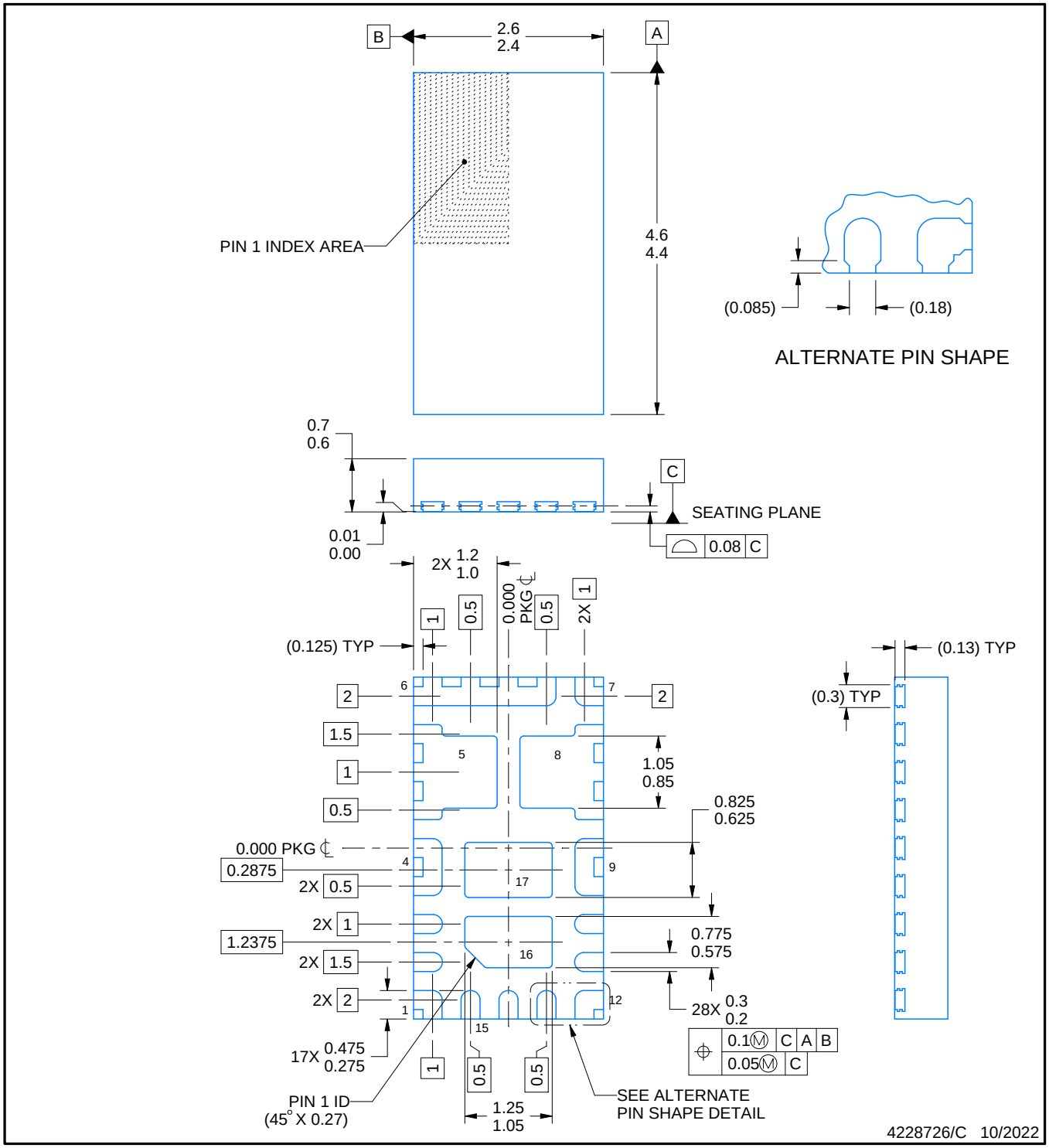
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS543B22RYSR	WQFN-FCRLF	RYS	17	5000	338.0	355.0	50.0
TPS543B22RYSR	WQFN-FCRLF	RYS	17	5000	454.0	454.0	35.0

PACKAGE OUTLINE

RYS0017A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

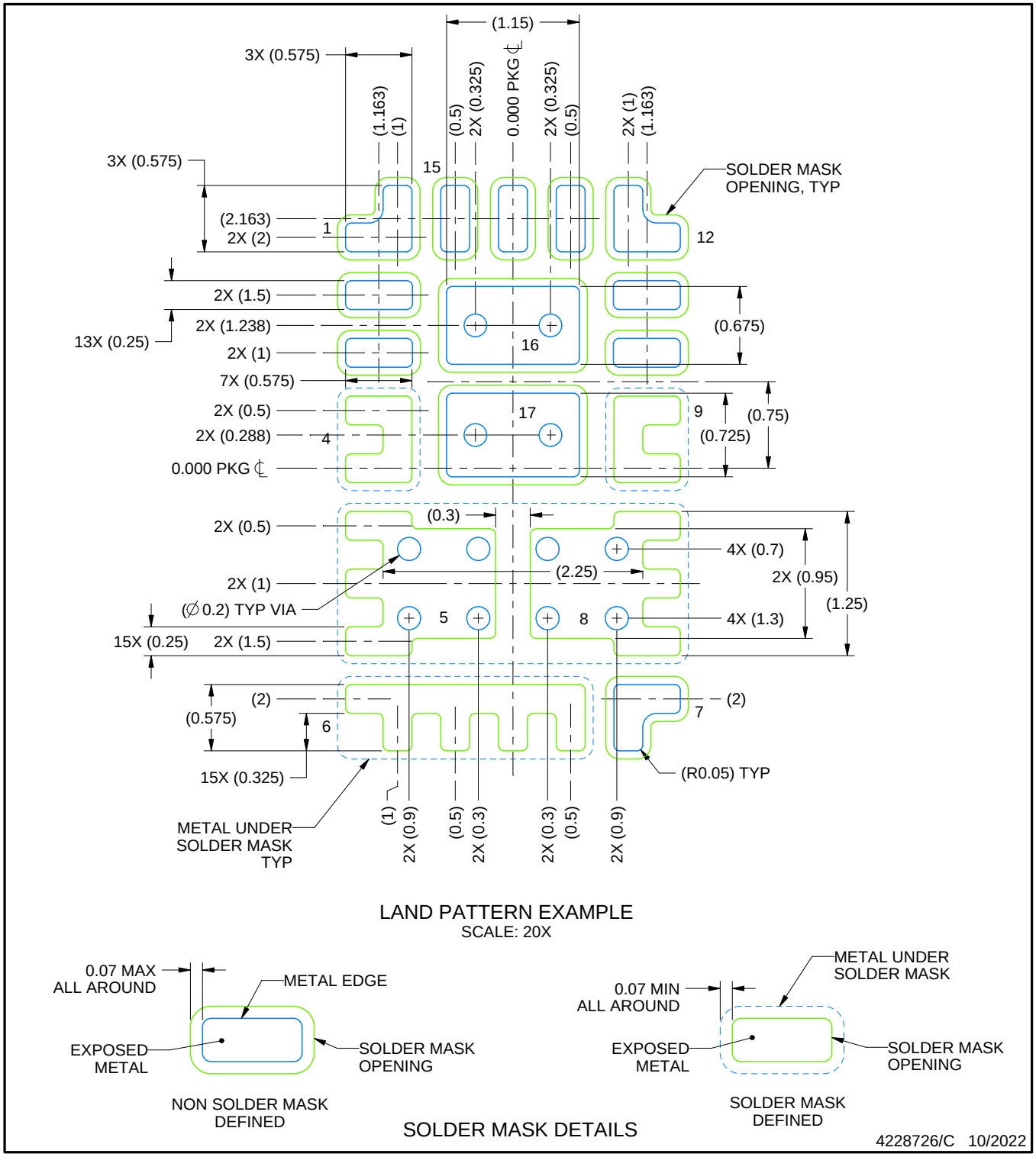
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RYS0017A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE

SCALE: 20X

SOLDER MASK DETAILS

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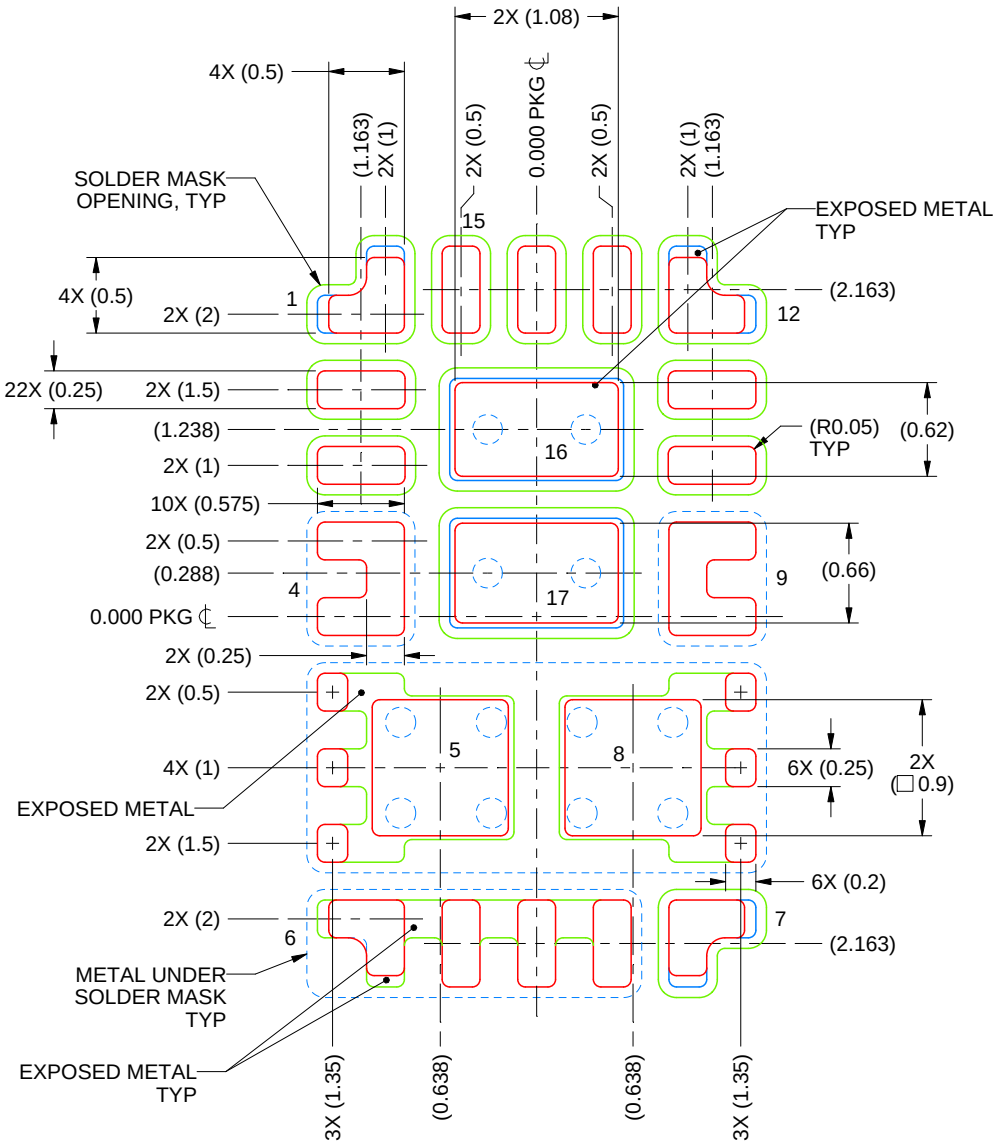
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA
PADS 1, 7 & 12: 83%
PAD 5 & 8: 87%
PAD 6: 73%
PAD 16: 85%
PAD 17: 86%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月