TEXAS INSTRUMENTS

# TPS55340-EP 統合型、5A、40V、広い入力範囲、昇圧 / SEPIC / フライバック DC-DC レギュレータ

1 特長

- 5A、40V のローサイド MOSFET スイッチを内蔵
- 2.9V〜32V の入力電圧範囲
- 精度 ±0.7% の基準電圧
- 動作時の静止電流:0.5mA
- シャットダウン時の消費電流:2.7µA
- 固定周波数の電流モード PWM 制御
- 周波数を 100kHz〜1.2MHz の範囲で変更可能
- 外部クロックへの同期機能
- 調整可能なソフトスタート時間
- パルス・スキッピングによる軽負荷時の効率向上
- サイクル単位の電流制限、サーマル・シャットダウン、UVLO 保護
- 防衛、航空宇宙、および医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ/テスト施設
  - 単一の製造施設
  - 軍用温度範囲 (-55℃〜125℃) で利用可能
  - 長い製品ライフ・サイクル
  - 製品変更通知期間の延長
  - 製品のトレーサビリティ

2 アプリケーション

- 3.3V、5V、12V、24V の電力変換
- 昇圧、SEPIC、フライバックのトポロジ
- Thunderbolt ポート、タブレットおよび携帯型 PC 用のパワー・ドッキング
- 産業用電源システム
- ADSL モデム
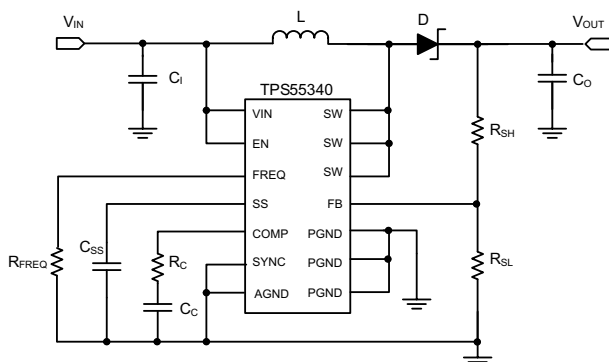
3 概要

TPS55340-EP は、5A、40V のパワー・スイッチを内蔵したモノリシック非同期スイッチング・レギュレータです。このデバイスは、昇圧、SEPIC、絶縁フライバックなど、複数の標準的なスイッチング・レギュレータのトポロジに構成できます。このデバイスは広い入力電圧範囲に対応しているため、マルチセル・バッテリやレギュレートされた 3.3V、5V、12V、24V 電源レールからの入力電圧を使用するアプリケーションをサポートできます。
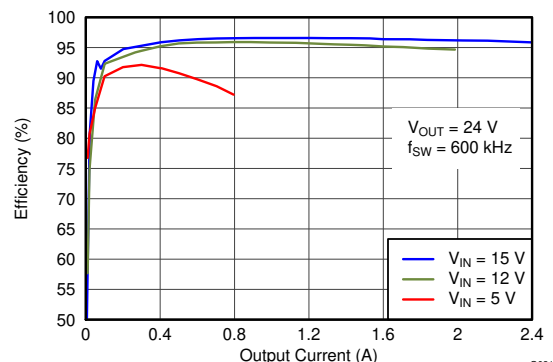
TPS55340-EP は電流モード PWM (パルス幅変調) 制御を使用して出力電圧をレギュレートします。また、発振器を内蔵しています。PWM のスイッチング周波数は、外付け抵抗、または外部クロック信号への同期により設定されます。ユーザーは、スイッチング周波数を 100kHz〜1.2MHz の範囲でプログラムできます。

このデバイスは、プログラム可能なソフトスタート機能によりスタートアップ時の突入電流を制限します。また、その他の保護機能 (例:サイクル単位の過電流制限、サーマル・シャットダウン) も内蔵しています。

製品情報

発注型番	パッケージ[1]	本体サイズ (公称)
TPS55340MRTETEP	WQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーション (昇圧)

効率と出力電流との関係

English Data Sheet: SLVSCG7

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4 Revision History

5 概要 (続き)

5A、40V の TPS55340-EP 昇圧コンバータは、3A、40V の TPS61175 とピン互換であり、最大入力電圧が 18V から 32V に拡張されています。
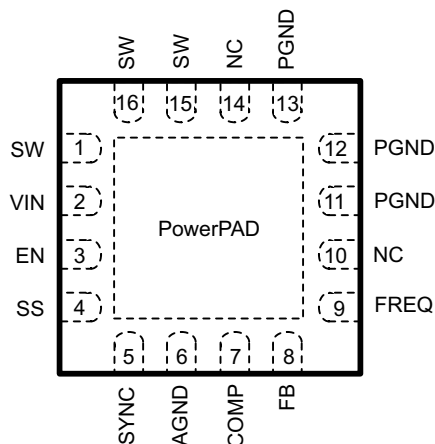
6 Pin Configuration and Functions

図 6-1. 16-Pin WQFN RTE Package (Top View)

表 6-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	6	Signal ground of the IC
COMP	7	Output of the transconductance error amplifier. An external RC network connected to this pin compensates the regulator feedback loop.
EN	3	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1 ms, the IC turns off.
FB	8	Error amplifier input and feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
FREQ	9	Switching frequency program pin. An external resistor connected between the FREQ pin and AGND sets the switching frequency.
NC	10	Reserved pin that must be connected to ground
	14	
PGND	11	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
	12	
	13	
PowerPAD	17	The PowerPAD™ should be soldered to the AGND. If possible, use thermal vias to connect to internal ground plane for improved power dissipation.
SS	4	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start timing.
SW	1	SW is the drain of the internal power MOSFET. Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
	15	
	16	
SYNC	5	Switching frequency synchronization pin. An external clock signal can be used to set the switching frequency between 200 kHz and 1 MHz. If not used, this pin should be tied to AGND.
VIN	2	The input supply pin to the IC. Connect VIN to a supply voltage between 2.9 and 32 V. It is acceptable for the voltage on the pin to be different from the boost power stage input.

Product Folder Links: *TPS55340-EP*

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltages on pin VIN[2]	−0.3	34	V
Voltage on pin EN[2]	−0.3	34	V
Voltage on pins FB, FREQ, and COMP[2]	−0.3	3	V
Voltage on pin SS[2]	−0.3	5	V
Voltage on pin SYNC[2]	−0.3	7	V
Voltage on pin SW[2]	−0.3	40	V
Operating junction temperature	−55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	−500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.9		32	V
V_{OUT}	Output voltage	V_{IN}		38	V
V_{EN}	EN voltage	0		32	V
V_{SYN}	External switching frequency logic input	0		5	V
T_A	Operating free-air temperature	−55		125	°C
T_J	Operating junction temperature	−55		150	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS55340-EP	UNIT
		WQFN (16 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	14.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

Vin = 5 V, T_J = –55°C to 150°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage		2.9		32	V
I_Q	Operating quiescent current into Vin	Device nonswitching, V_{FB} = 2 V		0.5		mA
I_{SD}	Shutdown current	EN = GND		2.7	10	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.5	2.7	V
V_{hys}	Undervoltage lockout hysteresis		120	140	160	mV
ENABLE AND REFERENCE CONTROL						
V_{EN}	EN threshold voltage	EN rising input	0.9	1.08	1.30	V
V_{ENh}	EN threshold hysteresis		0.1	0.16	0.22	V
R_{EN}	EN pulldown resistor		400	950	1600	kΩ
T_{off}	Shutdown delay, SS discharge	EN high to low		1.0		ms
V_{SYNh}	SYN logic high voltage		1.2			
V_{SYNl}	SYN logic low voltage				0.4	V
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
I_{FB}	Voltage feedback input bias current			1.6	30	nA
I_{sink}	Comp pin sink current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1 V		42		µA
I_{source}	Comp pin source current	V_{FB} = V_{REF} – 200 mV, V_{COMP} = 1 V		42		µA
V_{CCLP}	Comp pin clamp voltage	High Clamp, V_{FB} = 1 V Low Clamp, V_{FB} = 1.5 V		3.1 0.75		V
V_{CTH}	Comp pin threshold	Duty cycle = 0%		1.04		V
G_{ea}	Error amplifier transconductance		240	360	440	µmho
R_{ea}	Error amplifier output resistance			10		MΩ
f_{ea}	Error amplifier crossover frequency			500		kHz
FREQUENCY						
f_{SW}	Frequency	R_{FREQ} = 480 kΩ	75	94	130	kHz
		R_{FREQ} = 80 kΩ	460	577	740	
		R_{FREQ} = 40 kΩ	920	1140	1480	
D_{max}	Maximum duty cycle	V_{FB} = 1 V, R_{FREQ} = 80 kΩ	89%	96%		
V_{FREQ}	FREQ pin voltage			1.25		V
T_{min_on}	Minimum on pulse width	R_{FREQ} = 80 kΩ		77		ns
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 5 V V_{IN} = 3 V		60 70	110 120	mΩ
I_{LN_NFET}	N-channel leakage current	V_{DS} = 25 V			2.1	µA
OCP and SS						
I_{LIM}	N-channel MOSFET current limit	D = D_{max}	5.25	6.6	8.25	A
I_{SS}	Soft-start bias current	Vss = 0 V		6		µA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			165		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

Product Folder Links: TPS55340-EP

7.6 Typical Characteristics

Vin = 5 V, T_J = 25°C (unless otherwise noted)
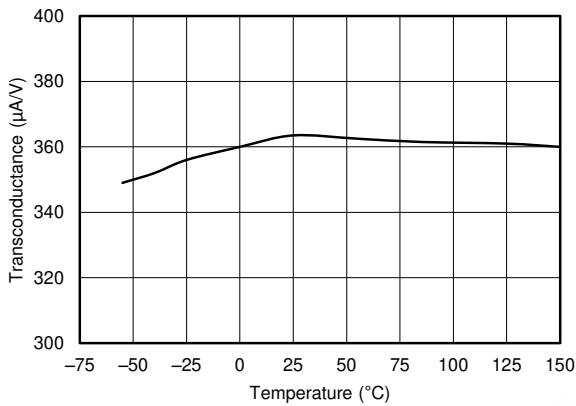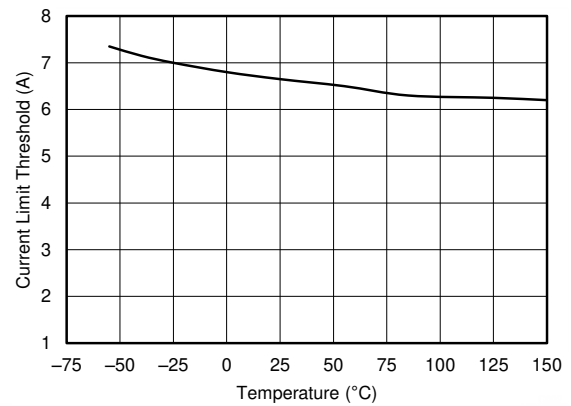

図 7-1. Error Amplifier Transconductance vs Temperature
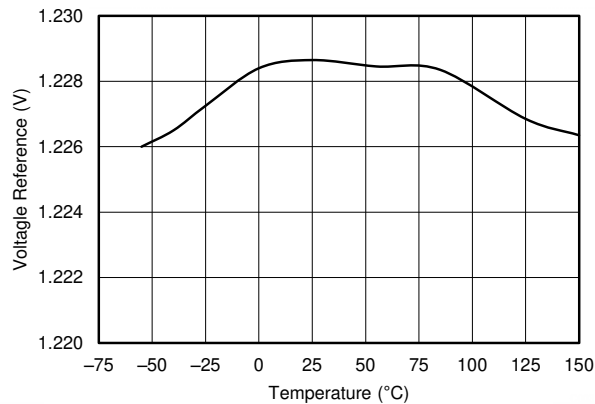

図 7-2. Switch Current Limit vs Temperature
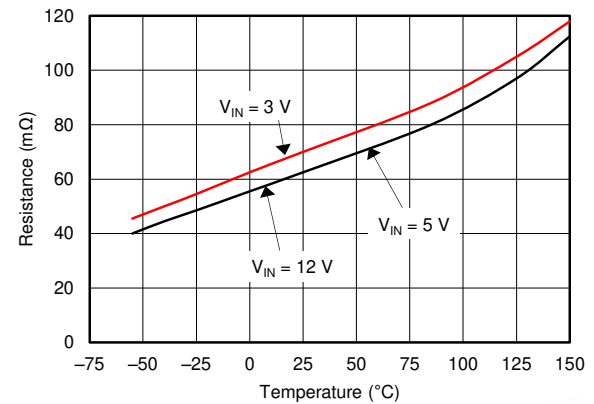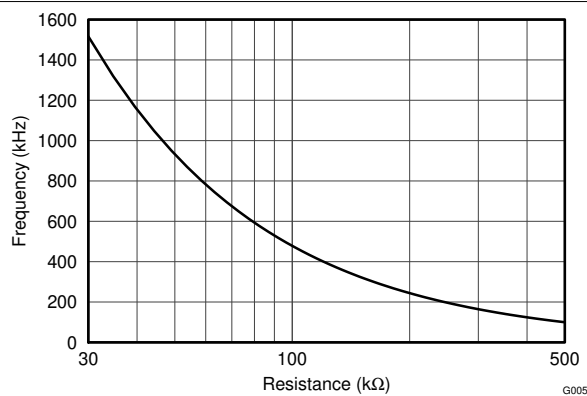

図 7-3. Feedback Voltage Reference vs Temperature

図 7-4. $R_{DS(ON)}$ vs Temperature

図 7-5. Frequency vs FREQ Resistance
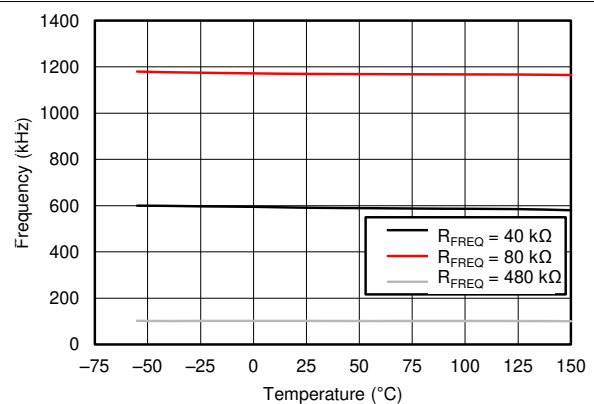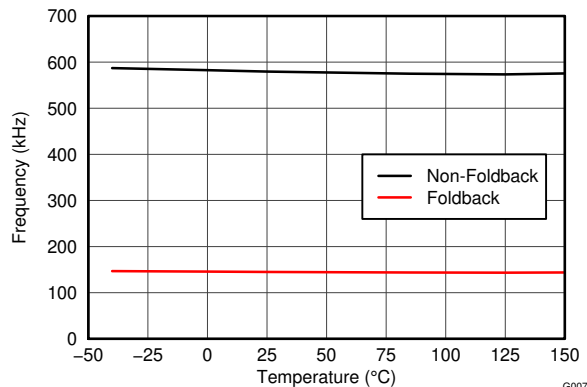

図 7-6. Frequency vs Temperature

Product Folder Links: *TPS55340-EP*
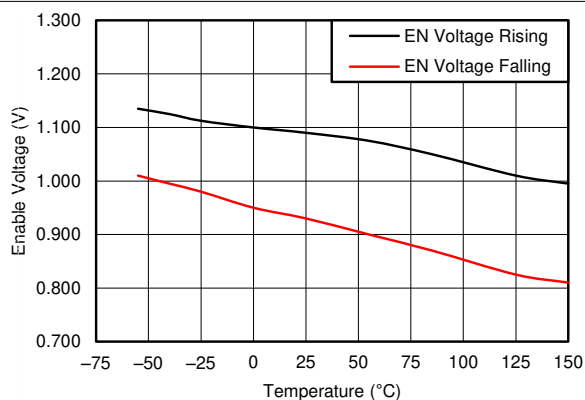
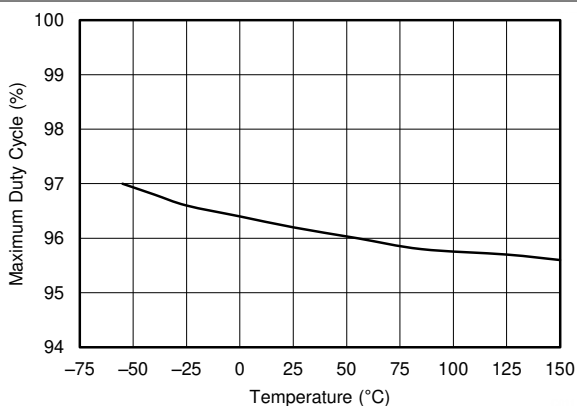図 7-7. Non-Foldback Frequency vs Foldback Frequency
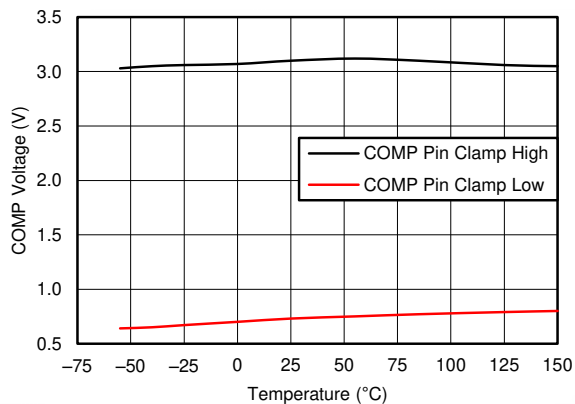
図 7-8. COMP Clamp Voltage vs Temperature
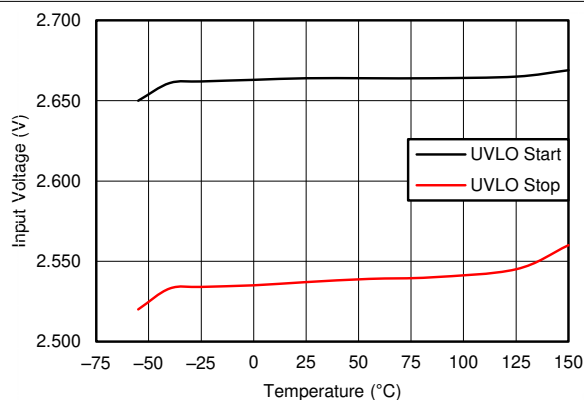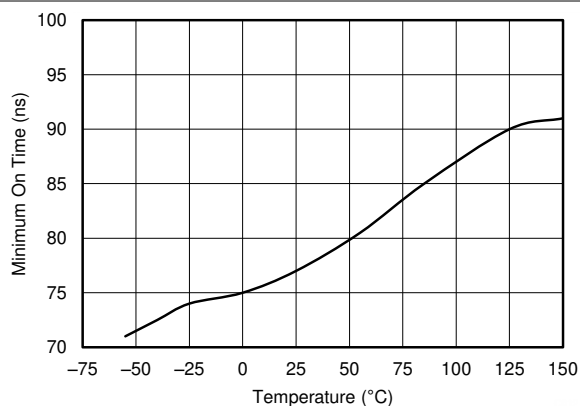

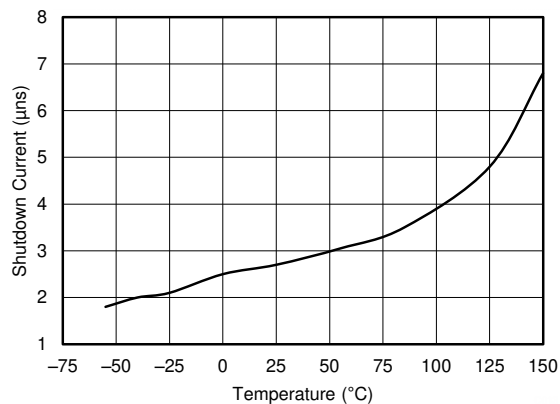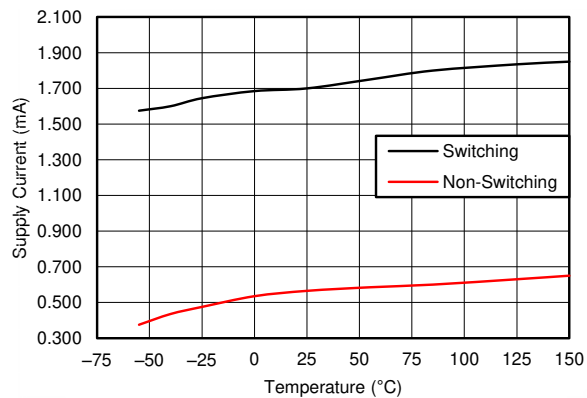図 7-9. Input Voltage UVLO vs Temperature

図 7-10. Enable Voltage vs Temperature

図 7-11. Maximum Duty Cycle vs Temperature

図 7-12. Minimum On Time vs Temperature

図 7-13. Shutdown Current vs Temperature

図 7-14. Supply Current vs Temperature

Product Folder Links: *TPS55340-EP*

8 Detailed Description

8.1 Overview

The TPS55340-EP integrates a 5-A, 40-V low-side N-channel MOSFET for boost converter output up to 38 V. The TPS55340-EP regulates the output with current mode PWM control. The PWM control circuitry turns on the switch at the beginning of each oscillator clock cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the output capacitor provides the load current. When the inductor current reaches a threshold level set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased to allow the inductor current to flow to the output. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The duty cycle of the converter is determined by the PWM control comparator which compares the error amplifier output and the current signal. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal.

A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. Slope compensation is necessary to avoid subharmonic oscillation that is intrinsic to peak current mode control at duty cycles higher than 50%. If the inductor value is too small, the internal slope compensation may not be adequate to maintain stability.

The PWM control feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC compensation network connected to the COMP pin is chosen for feedback loop stability and optimum transient response.

8.2 Functional Block Diagram

Product Folder Links: *TPS55340-EP*
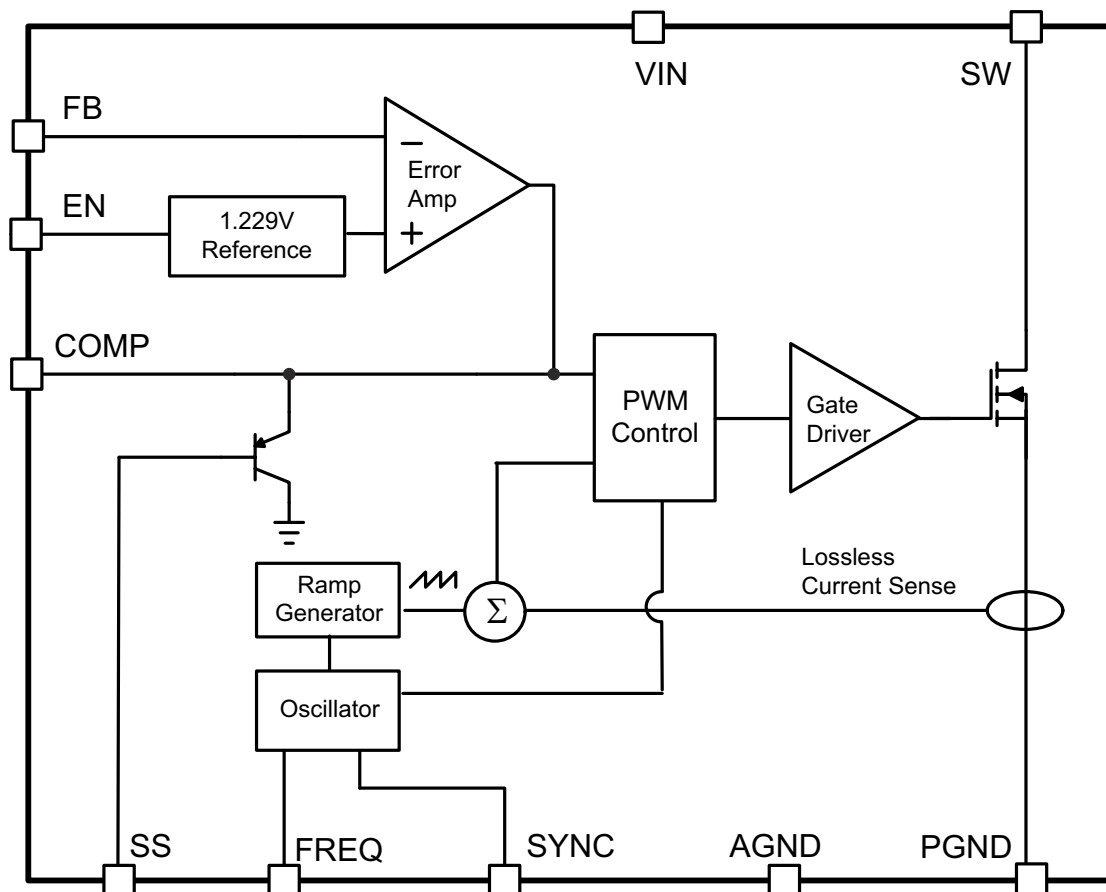
8.3 Feature Description

8.3.1 Switching Frequency

The switching frequency is set by a resistor (R_{FREQ}) connected to the FREQ pin of the TPS55340-EP. The relationship between the timing resistance R_{FREQ} and frequency is shown in 図 7-5. Do not leave this pin open. A resistor must always be connected from the FREQ pin to ground for proper operation. Calculate the resistor value required for a desired frequency using 式 1.

$$R_{FREQ}(k\Omega) = 57500 \times f_{sw}(kHz)^{-1.03} \tag{1}$$

For the given resistor value, calculate the corresponding frequency with 式 2.

$$f_{sw}(kHz) = 41600 \times R_{FREQ}(k\Omega)^{-0.97} \tag{2}$$

The TPS55340-EP switching frequency can be synchronized to an external clock signal that is applied to the SYNC pin. The required logic levels of the external clock are shown in the specification table. The recommended duty cycle of the clock is in the range of 10% to 90%. A resistor must be connected from the FREQ pin to ground when the converter is synchronized to the external clock and the external clock frequency must be within ±20% of the corresponding frequency set by the resistor. For example, if the frequency programmed by the FREQ pin resistor is 600 kHz, the external clock signal should be in the range of 480 to 720 kHz.

8.3.2 Voltage Reference and Setting Output Voltage

An internal voltage reference provides a precise 1.229-V voltage reference at the error amplifier non-inverting input. To set the output voltage, select the FB pin resistor R_{SH} and R_{SL} according to 式 3.

$$V_{OUT} = 1.229\,V \times \left(\frac{R_{SH}}{R_{SL}} + 1 \right) \tag{3}$$

8.3.3 Soft Start

The TPS55340-EP has a built-in soft-start circuit which significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (6 µA typical) charges a capacitor (C_{SS}) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the peak current and duty cycle of PWM controller. Limiting the peak switch current during start-up with a slow ramp on the SS pin reduces in-rush current and output voltage overshoot. After the capacitor reaches 1.8 V, the soft-start cycle is completed and the soft-start voltage no longer clamps the error amplifier output. When the EN is pulled low for at least 1 ms, the IC enters the shutdown mode and the SS capacitor is discharged through a 5-kΩ resistor to prepare for the next soft-start sequence.

8.3.4 Slope Compensation

The TPS55340-EP has internal slope compensation to prevent subharmonic oscillations. The sensed current slope of boost converter can be expressed as 式 4.

$$S_n = \frac{V_{IN}}{L} \times R_{SENSE} \tag{4}$$

Calculate the slope compensation dv/dt using 式 5.

$$S_e = \frac{0.32\,V/R_{FREQ}}{16 \times (1-D) \times 6\,pF} + \frac{0.5\,\mu A}{6\,pF} \tag{5}$$

In a converter with current mode control, in addition to the output voltage feedback loop, take into account the inner current loop including the inductor current sampling effect and slope compensation on the small signal response, which can be modeled as seen in 式 6.

$$He(s) = \cfrac{1}{1 + \cfrac{s \times \left[\left(1 + \cfrac{S_e}{S_n} \right) \times (1 - D) - 0.5 \right]}{f_{sw}} + \cfrac{s^2}{\left(\pi \times f_{sw} \right)^2}}$$

(6)

where

- R_{SENSE} (15 mΩ) is the equivalent current sense resistor
- R_{FREQ} is timing resistor used to set frequency
- D is the duty cycle

Note that if S_n << S_e, the converter operates in voltage mode control rather than current mode control, and 式 6 is no longer valid.

8.3.5 Overcurrent Protection and Frequency Foldback

The TPS55340-EP provides cycle-by-cycle overcurrent protection that turns off the power switch when the inductor current reaches the overcurrent limit threshold. The PWM circuitry resets itself at the beginning of the next switch cycle. During an overcurrent event, the output voltage begins to droop as a function of the load on the output. When the FB voltage through the feedback resistors drops lower than 0.9 V, the switching frequency is automatically reduced to 1/4 of the normal value. 図 7-7 shows the non-foldback frequency with an 80-kΩ timing resistor and the corresponding foldback frequency. The switching frequency does not return to normal until the overcurrent condition is removed and the FB voltage increases above 0.9 V. The frequency foldback feature is disabled during soft start.

8.3.6 Enable and Thermal Shutdown

The TPS55340-EP enters shutdown when the EN voltage is less than 0.68 V (min) for more than 1 ms. In shutdown, the input supply current for the device is less than 10 µA (max). The EN pin has an internal 950-kΩ pulldown resistor to disable the device if the pin is floating.

An internal thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical). The device restarts when the junction temperature drops by 15°C.

8.3.7 Undervoltage Lockout (UVLO)

An UVLO circuit prevents misoperation of the device at input voltages below 2.5 V (typical). When the input voltage is below the UVLO threshold, the device remains off and the internal power MOSFET is turned off. The UVLO threshold is set below minimum operating voltage of 2.9 V to ensure that a transient VIN dip will not cause the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are not ensured.

8.3.8 Minimum On-Time and Pulse Skipping

The TPS55340-EP PWM control system has a minimum PWM pulse width of 77 ns (typical). This minimum on-time determines the minimum duty cycle of the PWM, for any set switching frequency. When the voltage regulation loop of the TPS55340-EP requires a minimum on-time pulse width less than 77 ns, the IC enters pulse-skipping mode. In this mode, the device holds the power switch off for several switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the PWM operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in 図 9-7.

8.3.9 Layout Considerations

As for all switching power supplies, especially those with high frequency and high switch current, printed circuit board (PCB) layout is an important design step. If the layout is not carefully designed, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent radiation of high-frequency resonance problems, proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a

ground plane under the switching regulator to minimize interplane coupling. The high current path including the internal MOSFET switch, Schottky diode, and output capacitor, contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the AGND pin to reduce the IC supply ripple.

8.3.10 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55340-EP. The TPS55340-EP features a thermally enhanced WQFN package. This package includes a PowerPAD that improves the thermal capabilities of the package. The thermal resistance of the WQFN package in any application greatly depends on the PCB layout and the PowerPAD connection. The PowerPAD must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPAD to achieve good thermal performance.

8.4 Device Functional Modes

8.4.1 Operation With V_{IN} < 2.9 V (Minimum V_{IN})

The device operates with input voltages above 2.9 V. The maximum UVLO voltage is 2.7 V, and the device will operate at input voltages above 2.7 V. The typical UVLO voltage is 2.5 V, and the device may operate at the input voltages above point. The device may also operate at lower input voltages; the minimum UVLO is not specified. At input voltages below the actual UVLO voltage, the device will not operate.

8.4.2 Synchronization

The synchronization pin (pin 5) can be configured as external clock signal used to set the switching frequency between 200 kHz to 1 MHz. When not used, this pin should be tied to AGND as shown in the *セクション 8.2*.

When using as an external clock signal to set switching frequency, a resistor must be connected from the FREQ pin to ground and the external clock frequency must be within ±20% of the corresponding frequency set by the resistor. A typical example of this operation is shown in *図 9-1*. The required levels for the external clock are shown in *表 9-1*. The recommended duty cycle of the clock is in the range of 10% to 90%.

8.4.3 Oscillator

TPS55340-EP regulates output voltage with current mode PWM, and has an internal oscillator. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal. A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. The functional block diagram highlights the typical oscillator operation.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

TPS55340-EP is a monolithic non-synchronous switching regulator with an integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and flyback. The device has a wide input voltage range to support application with input voltage from multi-cell batteries or regulated 3.3-, 5-, 12-, and 24-V power rails. The switching frequency of PWM is set by either an external resistor or by synchronizing to an external clock signal. The user can program the switching frequency from 100 kHz to 1.2 MHz.

The following sections highlights the different approaches for configuring TPS55340-EP as boost, SEPIC, and flyback converter.

9.2 Typical Applications

9.2.1 Boost Converter Application

The following section provides a step-by-step design approach for configuring the TPS55340-EP as a voltage regulating boost converter, as shown in 図 9-1. When configured as SEPIC or flyback converter, a different design approach is required. A design example of SEPIC converter is provided in the next section.

図 9-1. Boost Converter Application Schematic

Product Folder Links: *TPS55340-EP*
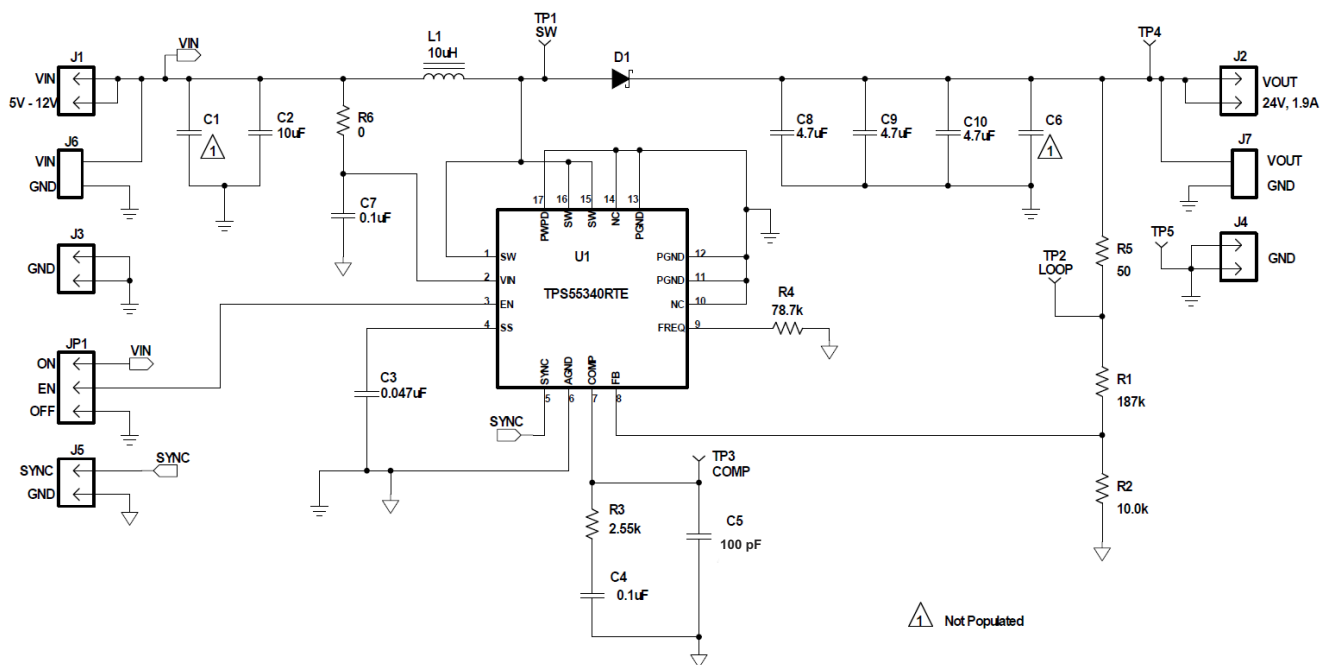
9.2.1.1 Design Requirements

A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, start with the following known parameters:

表 9-1. Key Parameters of Boost Converter Example

PARAMETER	VALUE
Output voltage	24 V
Input voltage	5 to 12 V
Maximum output current	800 mA
Transient response 50% load step (ΔV_{OUT} = 3%)	960 mV
Output voltage ripple (0.5% of V_{OUT})	120 mV

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Selecting the Switching Frequency (R4)

The first step is to decide on a switching frequency for the regulator. There are tradeoffs to consider for a higher or lower switching frequency. A higher switching frequency allows for a lower-valued inductor and smaller output capacitors leading to the smallest solution size. A lower switching frequency results in a larger solution size, but better efficiency. The user typically sets the frequency for the minimum tolerable efficiency to avoid excessively large external components.

A switching frequency of 600 kHz is a good trade-off between efficiency and solution size. The appropriate resistor value is found from the resistance versus frequency graph of 図 7-5, or calculated using 式 1. R4 is calculated to be 78.4 kΩ and the nearest standard value resistor of 78.7 kΩ is selected. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

9.2.1.2.2 Determining the Duty Cycle

The input to output voltage conversion ratio of the TPS55340-EP is limited by the worst-case maximum duty cycle of 89% and the minimum duty cycle, which is determined by the minimum on-time of 77 ns and the switching frequency. The minimum duty cycle can be estimated with 式 7. With a 600-kHz switching frequency the minimum duty cycle is 4%.

$$D_{PS} = T_{ON} \text{ min} \times f_{sw} \tag{7}$$

The duty cycle at which the converter operates depends on the mode in which the converter is running. If the converter is running in discontinuous conduction mode (DCM), where the inductor current ramps to 0 at the end of each cycle, the duty cycle varies with changes of the load much more than it does when running in continuous conduction mode (CCM). In CCM, where the inductor maintains a minimum DC current, the duty cycle is related primarily to the input and output voltages as calculated in 式 8. Assume a 0.5-V drop V_D across the Schottky rectifier. At the minimum input of 5 V, the duty cycle is 80%. At the maximum input of 12 V, the duty cycle is 51%.

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \tag{8}$$

At light loads, the converter operates in DCM. In this case, the duty cycle is a function of the load, input and output voltages, inductance, and switching frequency as calculated in 式 9. This can be calculated only after an inductance is chosen in the following section. While operating in DCM with very-light load conditions, the duty cycle demand forces the TPS55340-EP to operate with the minimum on-time. The converter then begins pulse skipping, which can increase the output ripple.

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \tag{9}$$

All converters using a diode as the freewheeling or catch component have a load current level at which they transit from DCM to CCM. This is the point where the inductor current just falls to 0 during the off-time of the power switch. At higher load currents, the inductor current does not fall to 0, and diode and switch current assume a trapezoidal wave shape as opposed to a triangular wave shape. The load current boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as follows.

$$I_{OUT(crit)} = \frac{(V_{OUT} + V_D - V_{IN}) \times V_{IN}^2}{2 \times (V_{OUT} + V_D)^2 \times f_{SW} \times L}$$

(10)

For loads higher than the result of 式 10, the duty cycle is given by 式 8. For loads less than the results of 式 10, the duty cycle is given 式 9. For 式 7 through 式 10, the variable definitions are as follows.

- V_{OUT} is the output voltage of the converter in V
- V_D is the forward conduction voltage drop across the rectifier or catch diode in V
- V_{IN} is the input voltage to the converter in V
- I_{OUT} is the output current of the converter in A
- L is the inductor value in H
- f_{SW} is the switching frequency in Hz

Note

Unless otherwise stated, the design equations that follow assume that the converter is running in CCM, which typically results in a higher efficiency for the power levels of this converter.

9.2.1.2.3 Selecting the Inductor (L1)

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance, and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The minimum value of the inductor should be able to meet inductor current ripple (ΔI_L) requirement at worst case. In a boost converter, maximum inductor current ripple occurs at 50% duty cycle. For the applications where duty cycle is always smaller or larger than 50%, 式 12 should be used with the duty cycle closest to 50% and corresponding input voltage to calculate the minimum inductance. For applications that need to operate with 50% duty cycle when input voltage is somewhere between the minimum and the maximum input voltage, use 式 13. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum input current ($I_{IN}DC = I_L avg$). The maximum input current can be estimated with 式 11, with an estimated efficiency based on similar applications (η_{EST}). The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value (K_{IND}) is at the discretion of the designer. However, the following guidelines may be used.

For CCM operation, TI recommends to use K_{IND} values in the range of 0.2 to 0.4. Choosing K_{IND} closer to 0.2 results in a larger inductance value, maximizes the converter's potential output current, and minimizes EMI. Choosing K_{IND} closer to 0.4 results in a smaller inductance value, a physically smaller inductor, and improved transient response, but potentially worse EMI and lower efficiency. Using an inductor with a smaller inductance value may result in the converter operating in DCM. This reduces the boost converter's maximum output current and causes larger input voltage and output voltage ripple and reduced efficiency. For this design, choose K_{IND} = 0.3 and a conservative efficiency estimate of 85% with the minimum input voltage and maximum output current. 式 12 is used with the maximum input voltage because this corresponds to duty cycle closest to 50%. The maximum input current is estimated at 4.52 A and the minimum inductance is 7.53 µH. A standard value of 10 µH is chosen.

$$I_{IN}DC = \frac{V_{OUT} \times I_{OUT}}{\eta_{EST} \times V_{IN}\,min} \tag{11}$$

$$L_O\,min \geq \frac{V_{IN}}{I_{IN}DC \times K_{IND}} \times \frac{D}{f_{SW}} \quad , D \neq 50\%,\; V_{IN}\; with\; D\; closest\; to\; 50\% \tag{12}$$

$$L_O\,min \geq \frac{(V_{OUT} + V_D)}{I_{IN}DC \times K_{IND}} \times \frac{1}{4 \times f_{SW}} \quad , D=50\% \tag{13}$$

After choosing the inductance, the required current ratings can be calculated. The inductor will be closest to its ratings with the minimum input voltage. The ripple with the chosen inductance is calculated with 式 14. The RMS and peak inductor current can be found with 式 15 and 式 16. For this design, the current ripple is 663 mA, the RMS inductor current is 4.52 A, and the peak inductor current is 4.85 A. TI generally recommends that the peak inductor current rating of the selected inductor be 20% higher to account for transients during power up, faults, or transient load conditions. The most conservative approach is to specify an inductor with a saturation current greater than the maximum peak current limit of the TPS55340-EP. This approach helps to avoid saturation of the inductor. The chosen inductor is a Würth Elektronik 74437368100. It has a saturation current rating of 12.5 A, RMS current rating of 5.2 A, and typical DCR of 27 mΩ.

$$\Delta I_L = \frac{V_{IN}\,min}{L_O} \times \frac{D\,max}{f_{SW}} \tag{14}$$

$$I_L rms = \sqrt{(I_{IN}DC)^2 + \left(\frac{\Delta I_L}{12}\right)^2} \tag{15}$$

$$I_L peak = I_{IN}DC + \frac{\Delta I_L}{2} \tag{16}$$

The TPS55340-EP has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too small, the slope compensation may not be adequate, and the loop can be unstable.

9.2.1.2.4 Computing the Maximum Output Current

The overcurrent limit for the integrated power MOSFET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage, and efficiency can all change maximum current output ($I_{OUT}max$). The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. Decreasing the K_{IND} or designing for a higher efficiency will increase the maximum output current. This can be evaluated with the chosen inductance or the chosen K_{IND}. This should be evaluated with the minimum input voltage and minimum peak current limit (I_{LIM}) of 5.25 A.

$$I_{OUT}\,max = \frac{V_{IN}\,min \times \left(I_{LIM} - \frac{\Delta I_L}{2}\right) \times \eta_{EST}}{V_{OUT}} = \frac{V_{IN}\,min \times I_{LIM} \times \left(1 - \frac{K_{IND}}{2}\right) \times \eta_{EST}}{V_{OUT}} \tag{17}$$

In this design with 5 V input boosted to 24 V output and a 10-µH inductor with an assumed the Schottky forward voltage of 0.5 V and estimated efficiency of 85%, the maximum output current is 871 mA. With the 12-V input and increased estimated efficiency of 90%, the maximum output current increases to 2.13 A. This circuit was evaluated to its maximum output currents with both the minimum and maximum input voltage.

Product Folder Links: *TPS55340-EP*

9.2.1.2.5 Selecting the Output Capacitor (C8 to C10)

TI recommends at least 4.7 µF of ceramic type X5R or X7R capacitance at the output. The output capacitance is mainly selected to meet the requirements for the output ripple (V_{RIPPLE}) and voltage change during a load transient. Then the loop is compensated for the output capacitor selected. The output capacitance should be chosen based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with 0 ESR, the minimum capacitance needed for a given ripple can be calculated by 式 18. If high-ESR capacitors are used, it will contribute additional ripple. The maximum ESR for a specified ripple is calculated with 式 19. ESR ripple can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used. The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by the 式 20. 式 21 can be used to calculate the RMS current that the output capacitor needs to support.

$$C_{OUT} \geq \frac{Dmax \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \tag{18}$$

$$ESR \leq \frac{\left(V_{RIPPLE} - \dfrac{Dmax \times I_{OUT}}{f_{SW} \times C_{OUT}}\right)}{\Delta I_L} \tag{19}$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2 \times \pi \times f_{BW} \times \Delta V_{TRAN}} \tag{20}$$

$$I_{CO}rms = I_{OUT}\sqrt{\frac{Dmax}{(1-Dmax)}} \tag{21}$$

Using 式 18 for this design, the minimum output capacitance for the specified 120-mV output ripple is 8.8 µF. For a maximum transient voltage change (ΔV_{TRAN}) of 960 mV with a 400-mA load transient (ΔI_{TRAN}) and a 6-kHz control loop bandwidth (f_{BW}) with 式 20, the minimum output capacitance is 11.1 µF. The most stringent criteria is the 11.1 µF for the required load transient. 式 21 gives a 1.58-A RMS current in the output capacitor. The capacitor should also be properly rated for the desired output voltage.

Take care when evaluating ceramic capacitors that derate under DC bias, aging, and AC signal conditions. For example, larger form factor capacitors (in 1206 size) have self-resonant frequencies in the range of converter switching frequency. Self-resonance causes the effective capacitance to be significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of the capacitance when operated at the rated voltage. Therefore, allow margin in selected capacitor voltage rating to ensure adequate capacitance at the required output voltage. For this example, three 4.7-µF, 50-V 1210 X7R ceramic capacitors are used in parallel leading to a negligible ESR. Choosing 50-V capacitors instead of 35 V reduces the effects of DC bias and allows this example circuit to be rated for the maximum output voltage range of the TPS55340-EP.

9.2.1.2.6 Selecting the Input Capacitors (C2, C7)

TI recommends at least 4.7 µF of ceramic input capacitance. Additional input capacitance may be required to meet ripple and transient requirements. TI recommends a high-quality ceramic, type X5R or X7R to minimize capacitance variations over temperature. The capacitor must also have an RMS current rating greater than the maximum RMS input current of the TPS55340-EP calculated with 式 22. The input capacitor must also be rated greater than the maximum input voltage. The input voltage ripple can be calculated with 式 23.

$$I_{CI}rms = \frac{\Delta I_L}{\sqrt{12}} \tag{22}$$

$$V_I ripple = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}} + \Delta I_L \times R_{CIN} \tag{23}$$

In the design example, the input RMS current is calculated to be 191 mA. The chosen input capacitor is a 10-µF, 35-V 1210 X7R with 3-mΩ ESR. Although one with a lower voltage rating can be used, a 35-V rated capacitor was chosen to limit the affects of DC bias and to allow the circuit to be rated for the entire input range of the TPS55340-EP. The input ripple is calculated to be 30 mV. An additional 0.1-µF, 50-V 0603 X5R is located close to the VIN and GND pins for extra decoupling.

9.2.1.2.7 Setting Output Voltage (R1, R2)

To set the output voltage in either DCM or CCM, select the values of R1 and R2 according to 式 24 and 式 25.

$$V_{OUT} = 1.229\,V \times \left(\frac{R1}{R2} + 1 \right)$$

(24)

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.229\,V} - 1 \right)$$

(25)

Considering the leakage current through the resistor divider and noise decoupling into FB pin, an optimum value for R2 is around 10 kΩ. The output voltage tolerance depends on the V_{FB} accuracy and the tolerance of R1 and R2. In this example with a 24-V output using 式 25, R1 is calculated to 185.3 kΩ. The nearest standard value of 187 kΩ is used.

9.2.1.2.8 Setting the Soft-Start Time (C7)

Choose the appropriate capacitor to set soft-start time and avoid overshoot. Increasing the soft-start time reduces the overshoot during start-up. A 0.047-µF ceramic capacitor is used in this example.

9.2.1.2.9 Selecting the Schottky Diode (D1)

The high switching frequency of the TPS55340-EP demands high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the regulated output voltage. The diode must also be rated for the power dissipated, which can be calculated with 式 26.

$$P_D = V_D \times I_{OUT}$$

(26)

In this conservative design example, the diode is chosen to be rated for the maximum output current of 2.13 A. During normal operation with 800-mA output current and assuming a Schottky diode drop of 0.5 V, the diode must be capable of dissipating 400 mW. For this design, the recommended minimum ratings are a 40-V, 3-A diode. However, to improve the flexibility of this design, a Diodes Inc B540-13-F in an SMC package is used with voltage and current ratings of 40 V and 5 A.

9.2.1.2.10 Compensating the Control Loop (R3, C4, C5)

The TPS55340-EP requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor, R3, and ceramic capacitor, C4, are connected to the COMP pin to provide a pole and a zero, shown in 図 9-1. This pole and zero, along with the inherent pole and zero of a boost converter, determine the closed-loop frequency response. This is important for converter stability and transient response. Loop compensation should be designed for the minimum operating voltage.

The following equations summarize the loop equations for the TPS55340-EP configured as a CCM boost converter. They include the power stage output pole (f_{OUT}) and the right-half-plane zero (f_{RHPZ}) of a boost converter calculated with 式 27 and 式 28 respectively. When calculating f_{OUT}, it is important to include the derating of ceramic output capacitors. In the example with an estimated 10.2-µF capacitance, these frequencies are calculated to 980 and 22.1 kHz respectively. The DC gain (A) of the power stage is calculated with 式 27 and is 39.9 dB in this design. The compensation pole (f_P) and zero (f_Z) generated by R3, C4, and internal transconductance amplifier are calculated with 式 30 and 式 31, respectively.

Most CCM boost converters have a stable control loop if f_Z is set slightly above f_P through proper sizing of R3 and C4. A good starting point is C4 = 0.1 µF and R3 = 2 kΩ. Increasing R3 or reducing C4 increases the closed-loop bandwidth, and therefore improves the transient response. Adjusting R3 and C4 in opposite directions increases the phase and gain margin of the loop, which improves loop stability. TI generally recommends to limit the bandwidth of the loop to the lower of either 1/5 of the switching frequency f_{SW} or 1/3 the RHPZ frequency, f_{RHPZ}, shown in 式 28. The spreadsheet tool located in the TPS55340-EP product folder can also be used to aid in compensation design.

$$f_{OUT} \approx \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \tag{27}$$

$$f_{RHPZ} \approx \frac{R_{OUT}}{2\pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \tag{28}$$

$$A = \frac{1.229}{V_{OUT}} \times G_{ea} \times 10M\Omega \times \frac{V_{IN}}{V_{OUT} \times R_{SENSE}} \times R_{OUT} \times \frac{1}{2} \tag{29}$$

$$f_P = \frac{1}{2\pi \times 10M\Omega \times C4} \tag{30}$$

$$f_Z = \frac{1}{2\pi \times R3 \times C4} \tag{31}$$

$$f_{co1} = \frac{f_{SW}}{5} \tag{32}$$

$$f_{co2} = \frac{f_{RHPZ}}{3} \tag{33}$$

where
- C_{OUT} is the equivalent output capacitor (C_{OUT} = C8 + C9 + C10)
- R_{OUT} is the equivalent load resistance (V_{OUT} / I_{OUT})
- Gea is the error amplifier transconductance located in the セクション 7.5
- R_{SENSE} (15 mΩ, typical) is the sense resistor in the current control loop
- f_{co1} and f_{co2} are possible bandwidth.

An additional capacitor from the COMP pin to GND (C5) can be used to place a high-frequency pole in the control loop. This is not always necessary with ceramic output capacitors. If a non-ceramic output capacitor is used, there is an additional zero (f_{ZESR}) in the control loop which can be calculated with 式 35. The value of C5 and the pole created by C5 can be calculated with 式 36 and 式 34, respectively. Finally, if more phase margin is needed, an additional zero (f_{ZFF}) can be added by placing a capacitor (C_{FF}) in parallel with the top feedback resistor R1. TI recommends to place the zero at the target crossover frequency or higher. The feed forward capacitor also adds a pole at a higher frequency. Calculate the recommended value of C_{FF} with 式 37.

$$f_{P2} = \frac{1}{2\pi \times R3 \times C5} \tag{34}$$

$$f_{ZESR} \approx \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{35}$$

$$C5 = \frac{R_{ESR} \times C_{OUT}}{R3} \tag{36}$$

$$C_{FF} = \frac{1}{2\pi \times R1 \times f_{ZFF} \times \sqrt{\dfrac{V_{REF}}{V_{OUT}}}}$$

(37)

where

- R_{ESR} is the ESR of the output capacitor

If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the minimum 5-V input and maximum 800-mA load. This measurement is shown in 図 9-2. In this design, only one pole and one zero are used, so the maximum phase increase from the compensation will be 180°. For a 60° phase margin, the power stage phase must be –120° at its lowest point. Based on the target 6-kHz bandwidth, the measured power stage gain, $K_{PS}(f_{BW})$, is 24.84 dB and the phase is –110.3°.
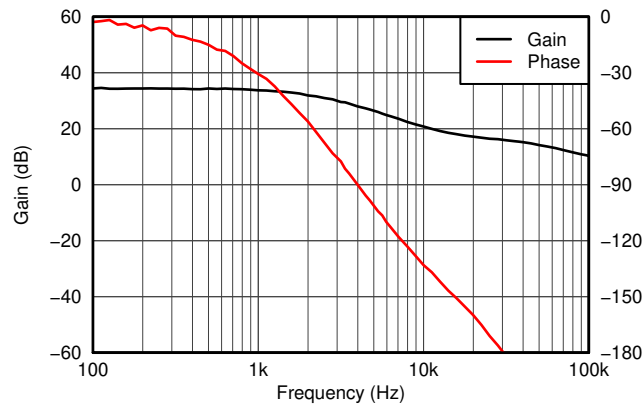
図 9-2. Power Stage Gain and Phase of the Boost Converter

R3 is then chosen to set the compensation gain to be the reciprocal of the power stage gain at the target bandwidth using 式 38. C4 is then chosen to place a zero at 1/10 the target bandwidth with 式 39. In this case, R3 is calculated to be 2.56 kΩ, the nearest standard value 2.55 kΩ is used. C4 is calculated at 0.104 µF and the nearest standard value 0.100 µF is used. Although not necessary because this design uses all ceramic capacitors, a 100-pF capacitor is selected for C5 to add a high-frequency pole at a frequency 100× the target bandwidth.

$$R3 = \frac{1}{\left(Gea \times \dfrac{R1}{(R1+R2)} \times 10^{\frac{K_{PS}(f_{BW})}{20}} \right)}$$

(38)

$$C4 = \frac{1}{2\pi \times R3 \times \dfrac{f_{BW}}{10}}$$
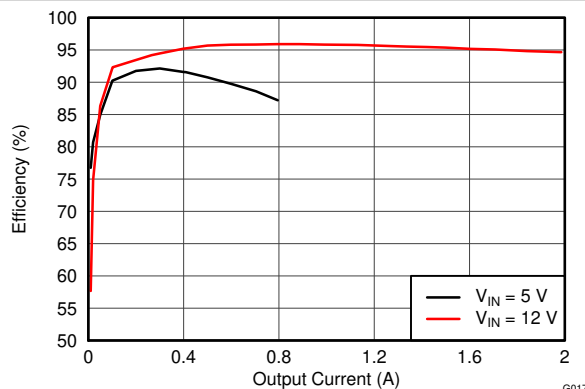
(39)

9.2.1.3 Application Curves

図 9-3. Efficiency vs Output Current

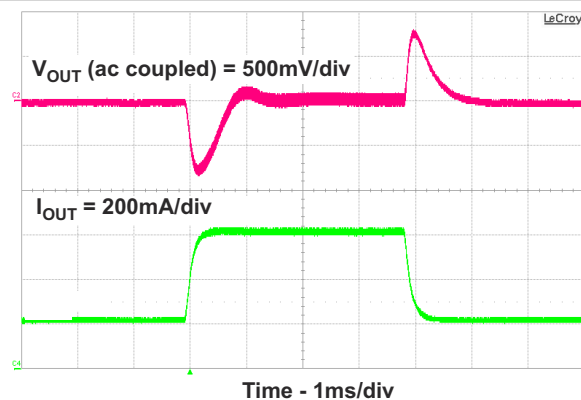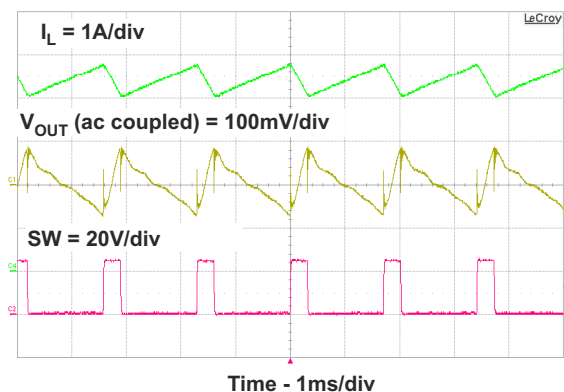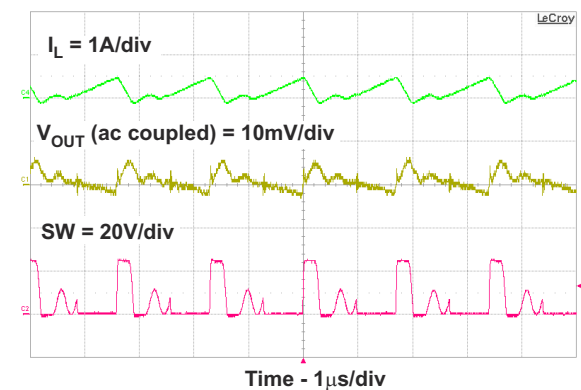図 9-4. Load Transient Response

図 9-5. CCM PWM Operation

図 9-6. DCM PWM Operation

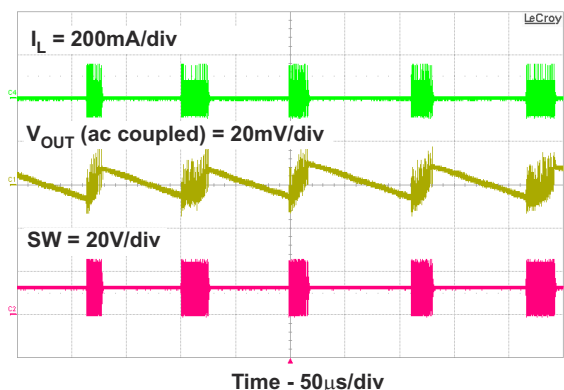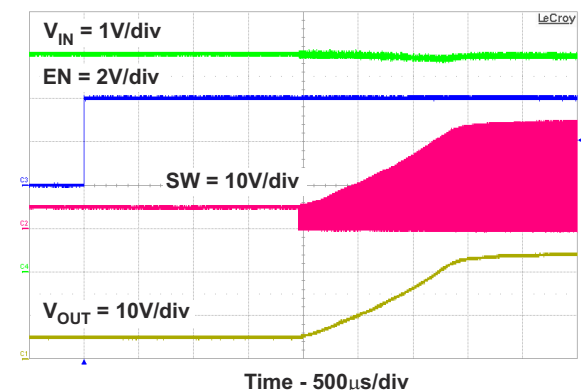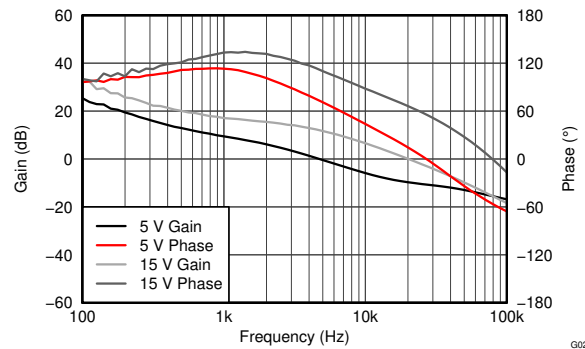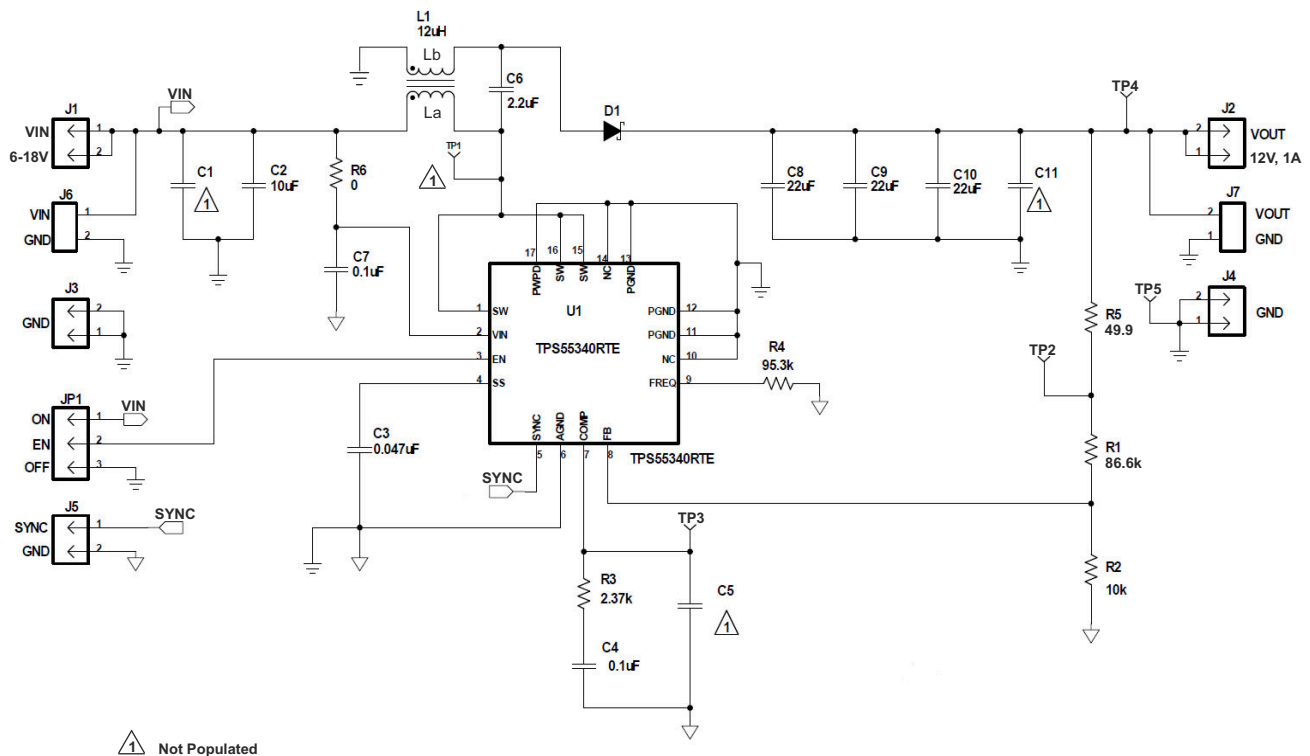図 9-7. Pulse Skipping

図 9-8. Start Up

I_{OUT} = 800 mA

図 9-9. Closed Loop Gain and Phase of the Boost Converter

9.2.2 SEPIC Converter Application

図 9-10. SEPIC Converter Application Schematic

9.2.2.1 Design Requirements

The following parameters are used for a SEPIC converter design. These calculations are performed only for CCM operation, and assume the use of a coupled inductor.

表 9-2. Key Parameters of SEPIC Converter Example

PARAMETER	VALUE
Output voltage	12 V
Input voltage	6 to 18 V, 12 V nominal
Maximum output current	1 A
Transient response 50% load step (ΔV_{OUT} = 4%)	480 mV

Product Folder Links: *TPS55340-EP*

表 9-2. Key Parameters of SEPIC Converter Example (continued)

PARAMETER	VALUE
Output voltage ripple (0.5% of V_{OUT})	60 mV

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Selecting the Switching Frequency (R4)

A 500-kHz switching frequency (f_{SW}) is selected for this design. Using 式 1, R4 is calculated and the nearest standard value 95.3 kΩ is used.

9.2.2.2.2 Duty Cycle

The duty cycle of a SEPIC converter is calculated with 式 40. With the 6-V minimum input the duty cycle is 68% and with the 18 V maximum input voltage the duty cycle is 41%.

$$D = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + V_{IN}}$$

(40)

9.2.2.2.3 Selecting the Inductor (L1)

With an estimated 85% efficiency, the input current is calculated with 式 9 to be 2.35 A. With K_{IND} of 0.3 and the maximum 18-V input, the minimum inductance is calculated to be 10.5 µH using 式 41. The nearest standard value of 12 µH is used. As mentioned previously, this equation assumes a coupled inductor is used.

$$L \geq \frac{V_{IN}\,max \times D\,min}{2 \times f_{SW} \times I_{IN}DC \times K_{IND}}$$

(41)

The inductor ripple current is recalculated to be 615 mA with 式 42. The peak current is calculated to 3.69 A. The typical current limit is used as the saturation rating for the inductor used. The RMS current for La is approximately the average input current 2.35 A. The RMS current for Lb is approximately the output current of 1 A. For this design, a CoilCraft MSD1260-123 is used with 6.86-A saturation, 74-mΩ DCR, and 3.12-A RMS current rating for one winding.

$$\Delta I_L = \frac{V_{IN}\,max \times D\,min}{2 \times f_{SW} \times L}$$

(42)

$$I_L peak = I_{La}peak + I_{Lb}peak = \left(I_{IN}DC + \frac{\Delta I_L}{2}\right) + \left(I_{OUT} + \frac{\Delta I_L}{2}\right)$$

(43)

9.2.2.2.4 Calculating the Maximum Output Current

The maximum output current with the minimum input voltage 6 V, chosen inductance 12 µH, 5.25-A minimum current limit, and estimated 85% efficiency is calculated to be 1.47 A using 式 44.

$$I_{OUT}\,max = \frac{(I_{LIM} - \Delta I_L)}{\left(\dfrac{V_{OUT}}{V_{IN}\,min \times \eta_{EST}} + 1\right)} = \frac{(I_{LIM} - I_{IN}DC \times K_{IND})}{\left(\dfrac{V_{OUT}}{V_{IN}\,min \times \eta_{EST}} + 1\right)}$$

(44)

9.2.2.2.5 Selecting the Output Capacitor (C8 to C10)

To meet the 60-mV ripple specification, the minimum output capacitance is calculated to be 22.5 µF with 式 45. This design uses ceramic output capacitors and the effects of ESR are ignored. To meet the transient response of 500 mA with less than 480-mV voltage change and a 7-kHz control loop bandwidth, the minimum output capacitance is calculated to be 23.7 µF using 式 46. The RMS current is calculated with 式 22 to be 1.44 A. The output capacitors used in this design is 3 × 22-µF, 25-V X7R 1210 ceramic capacitors. With voltage derating, the effective total output capacitance is estimated to be 30.4 µF.

$$C_{OUT} \geq \frac{Dmax \times I_{OUT}}{f_{SW} \times V_{RIPPLE}}$$

(45)

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}}$$

(46)

9.2.2.2.6 Selecting the Series Capacitor (C6)

The series capacitor is chosen to limit the ripple current to 5% of the maximum input voltage. Using 式 47, the minimum capacitance is 1.5 µF. Using 式 48, the RMS current is calculated to be 1.63 A. A 2.2-µF ceramic capacitor in a 1206 package is selected.

$$C_P \geq \frac{I_{OUT} \times Dmax}{0.05 \times V_{IN}max \times f_{SW}}$$

(47)

$$I_{CP}rms = I_{IN}DC \times \sqrt{\frac{(1-Dmax)}{Dmax}}$$

(48)

9.2.2.2.7 Selecting the Input Capacitor (C2, C7)

Based on the minimum 4.7-µF ceramic recommended for the TPS55340-EP, a 10-µF X7R input capacitor is used with an additional 0.1 µF placed close to the VIN and GND pins. With an estimated 6-µF capacitance after voltage derating, the input ripple voltage is calculated to be 39.9 mV using 式 49. The RMS current of the input capacitance is calculated to be 0.177 A with 式 50.

$$V_I ripple = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}}$$

(49)

$$I_{CI}rms = \frac{\Delta I_L}{\sqrt{12}}$$

(50)

9.2.2.2.8 Selecting the Schottky Diode (D1)

The selected diode must have a minimum breakdown voltage (V_{BR}) calculated with 式 51, which is 30.5 V in this design. TI recommends that the average current rating be greater than the maximum output current. With the maximum 18-V input, average current is calculated to be 2.6 A using 式 17. The package must also be capable of handling the power dissipation. With an estimated 0.5-V forward voltage, power dissipation is calculated with 式 26 to be 500 mW. Diodes Inc B340B is chosen with a 40-V, 3-A rating in a SMB package.

$$V_{BR} = V_O + V_{IN}max + V_F$$

(51)

9.2.2.2.9 Setting the Output Voltage (R1, R2)

With R2 fixed at 10 kΩ using 式 25, the nearest standard value of 86.6 kΩ is chosen for R1.

9.2.2.2.10 Setting the Soft-Start Time (C3)

The recommended 0.047-µF soft-start capacitor is used.

9.2.2.2.11 MOSFET Rating Considerations

In a SEPIC converter, the MOSFET must be rated to handle the sum of the input and output voltages. In this design with the maximum input voltage of 18 V and output voltage of 12 V, the FET will see approximately 30 V. TI recommends a 10% tolerance to account for any ringing. The 40-V rating of the TPS55340-EP power MOSFET comfortably satisfies this requirement.

9.2.2.2.12 Compensating the Control Loop (R3, C4)

This design was compensated by measuring the frequency response of the power stage at the lowest input voltage of 6 V and choosing the components for the desired bandwidth. The lowest right half plane zero (f_{RHPZ})

is calculated to be 36.7 kHz with 式 52. Using the recommendation to limit the bandwidth to 1/3 of f_{RHPZ}, the maximum recommended is 12.2 kHz.

$$f_{RHPZ} = \frac{\dfrac{V_{OUT}}{I_{OUT}}}{2 \times \pi \times L \times \left(\dfrac{D}{(1-D)}\right)^2}$$

(52)

This design also uses only one pole and one zero. To achieve approximately 60° of phase margin, the power stage phase must be no lower than approximately –120° at the desired bandwidth. To ensure a stable design, R3 was initially set to 1 kΩ and C4 was 1 µF. 図 9-11 shows the measurement of the power stage At 7 kHz, the power stage has a gain of 19.52 dB and phase of –118.1°.
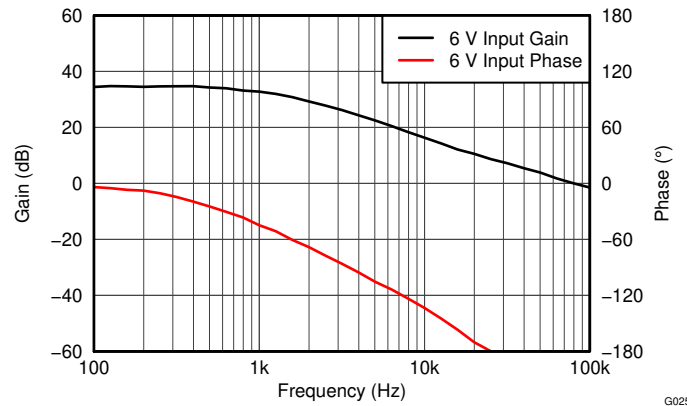
図 9-11. SEPIC Power Stage Gain and Phase

As there are no changes in the transconductance amplifier, the equations used to calculate the external compensation components in a boost design can be used in the SEPIC design. Using the maximum Gea from the electrical specification of 440 µmho, 式 38 calculates the nearest standard value of R3 to be 2.37 kΩ. Using 式 39, C4 is calculated to the nearest standard value of 0.1 µF.
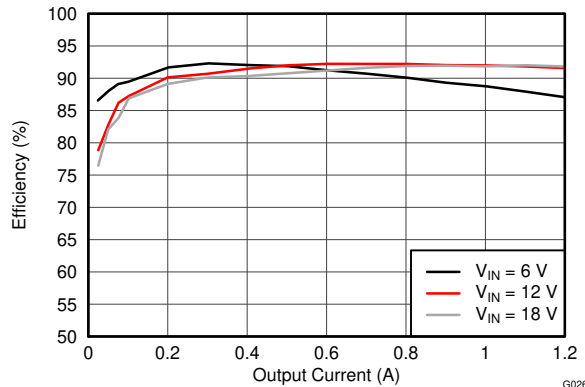
9.2.2.3 SEPIC Converter Application Curves
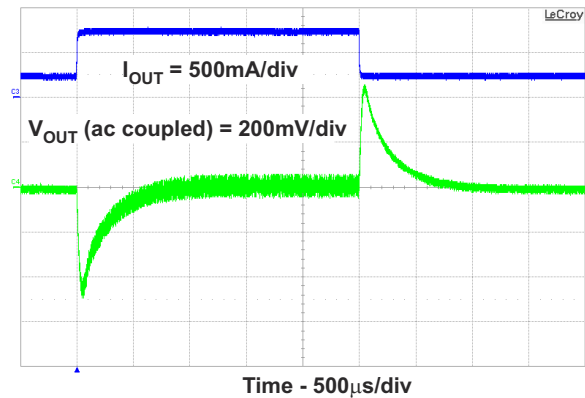

図 9-12. Efficiency vs Output Current
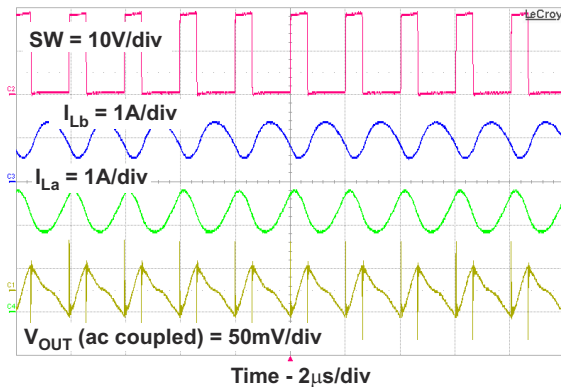

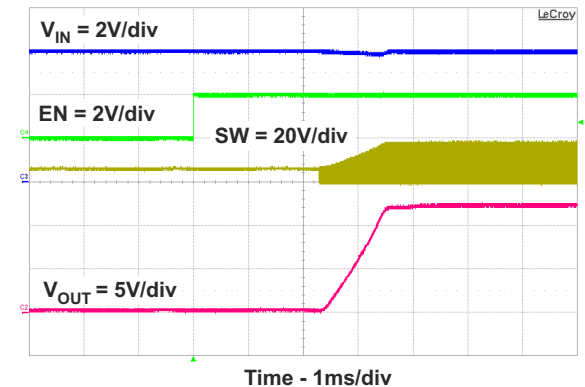**図 9-13. Load Transient Response**

図 9-14. CCM PWM Operation

図 9-15. Output Voltage Soft-Start
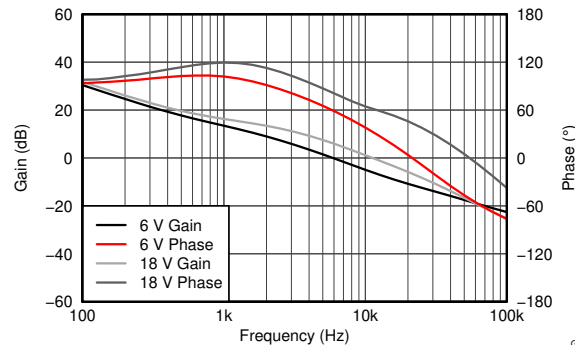

図 9-16. Closed Loop Gain and Phase of the SEPIC Converter

Product Folder Links: *TPS55340-EP*

10 Power Supply Recommendations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55340-EP. The TPS55340-EP features a thermally-enhanced WQFN package. This package includes a PowerPAD that improves the thermal capabilities of the package. The thermal resistance of the WQFN package in any application greatly depends on the PCB layout and the PowerPAD connection. The PowerPAD must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPAD to achieve good thermal performance.
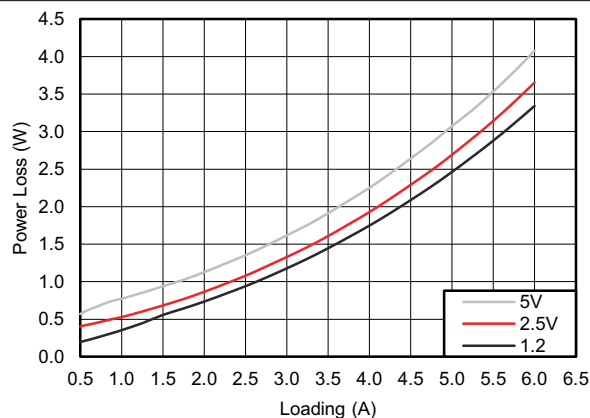
V_{IN} = 24 V
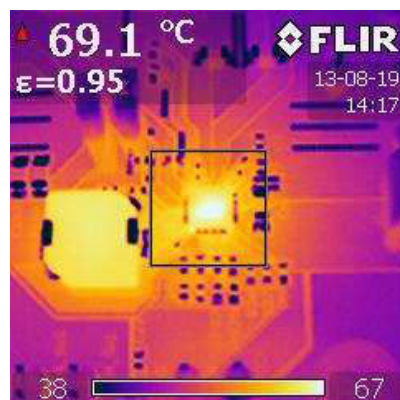
図 10-1. Power Dissipation of TPS55340-EP

V_{IN} = 12 V
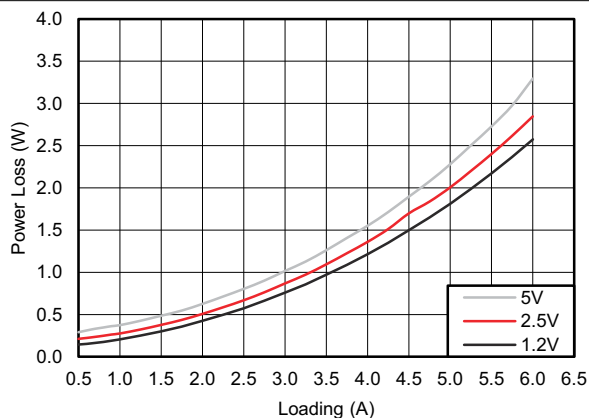
図 10-2. Power Dissipation of TPS55340-EP
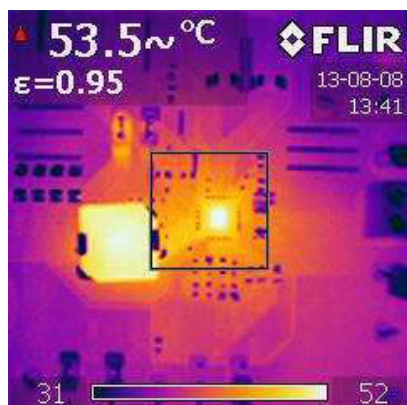
T_A = Room temperature V_{IN} = 24 V
V_{OUT} to V_{SW_in} = 5 V/0 A $I_{SW\_OUT1/2}$ = 1.2 A
EVM board: 4-layer PCB, 1.6-mm thickness, 2-oz. copper thickness, 65-mm × 65-mm size, 25 vias at thermal pad

図 10-3. Thermal Signature of TPS55340EVM

T_A = Room temperature V_{IN} = 24 V
V_{OUT} = 5 V/4 A $I_{SW\_OUT1/2}$ = 0 A
EVM board: 4-layer PCB, 1.6-mm thickness, 2-oz. copper thickness, 65-mm × 65-mm size, 25 vias at thermal pad

図 10-4. Thermal Signature of TPS55340EVM

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those with high frequency and high switch current, PCB layout is an important design step. If the layout is not carefully designed, the regulator could suffer from instability and noise problems.

図 11-1 and 図 11-2 show the board layout. The top-side layer is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. The top layer contains the main power traces for VIN, VOUT, and SW. The top layer also has connections for the remaining pins of the TPS55340-EP and a large area filled with ground. The internal layers and bottom are primarily ground with additional fill areas for VIN and VOUT. The top-side ground traces connect to the bottom and internal ground planes with multiple vias placed around the board. Nine vias directly under the TPS55340-EP device provide a thermal path from the top-side ground plane to the bottom-side ground plane. Place the output decoupling capacitors (C8 through C10 and C6) as close to the IC as possible. The copper area of the SW node is kept small to minimize noise. The vias near the diode, D1, on the VOUT plane aid with thermal dissipation. Additionally, keep the voltage setpoint resistor divider components close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper VOUT trace at the J7 output connector. For the TPS55340-EP, an additional input bulk capacitor may be necessary, depending on the board connection to the input supply. Critical analog circuits such as the voltage setpoint divider, frequency-set resistor, slow-start capacitor, and compensation components terminate to ground using a separate ground trace on the top and bottom connected power ground; pour only at one point directly under the IC.

11.2 Layout Examples
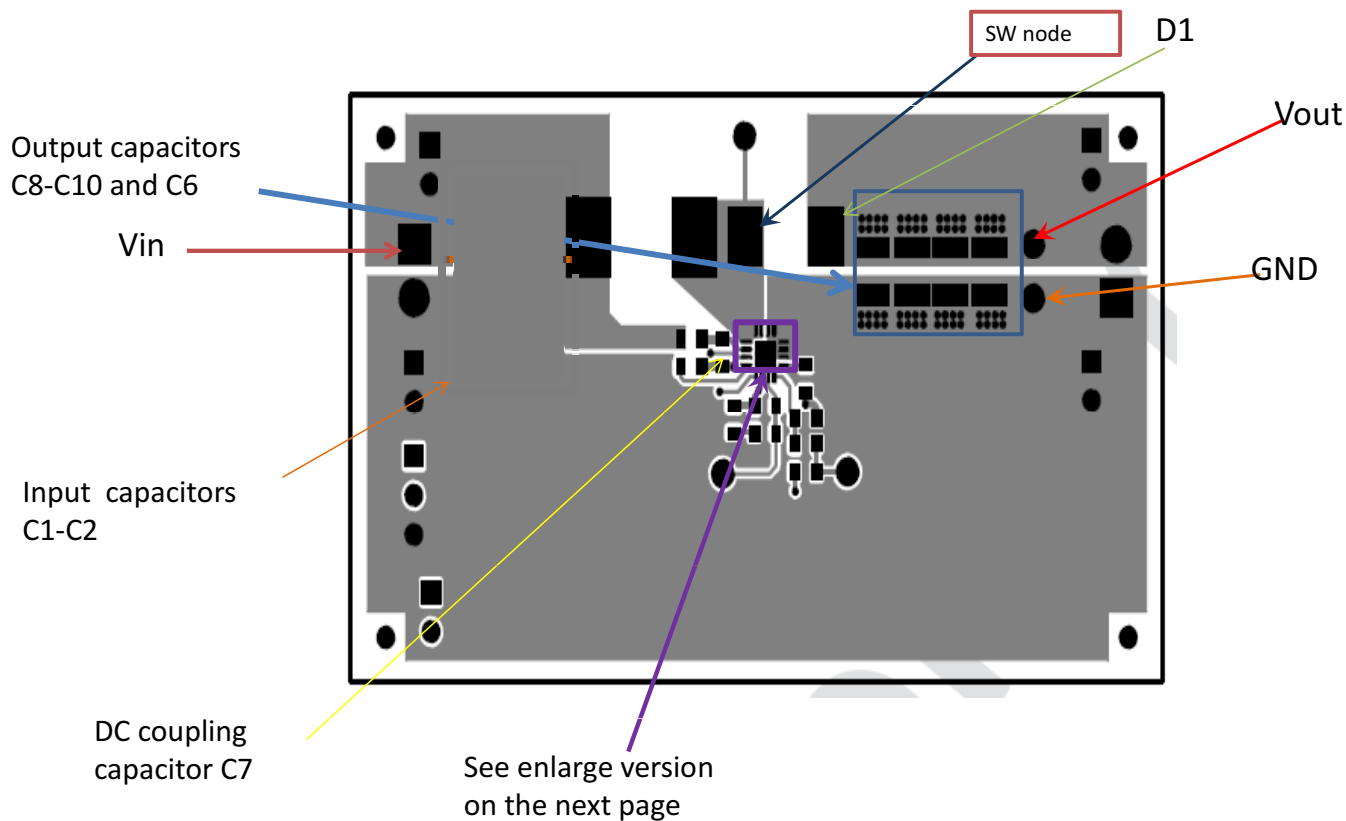
図 11-1. TPS55340 Top-Side Layout
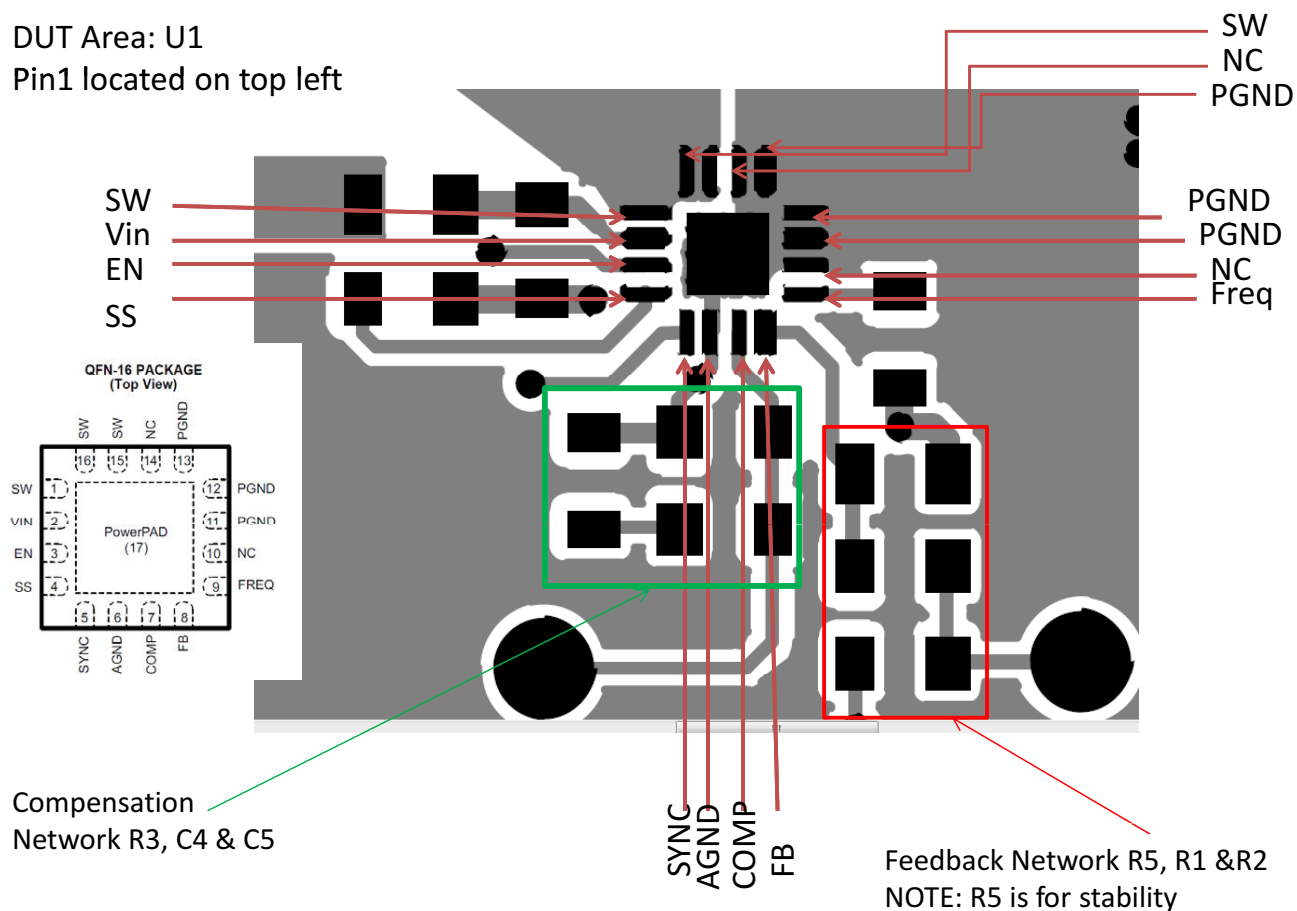
図 11-2. TPS55340 Top-Side Layout DUT1 Enlarged Version

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS55340MRTETEP	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	5340M
V62/14611-01XE	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	5340M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS55340-EP :

● Catalog : TPS55340

● Automotive : TPS55340-Q1

NOTE: Qualified Version Definitions:

 ● Catalog - TI's standard catalog product

 ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55340MRTETEP	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55340MRTETEP	WQFN	RTE	16	250	210.0	185.0	35.0

RTE 16

3 x 3, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225944/A

A

3.1
2.9

B

PIN 1 INDEX AREA

3.1
2.9

SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

0.8 MAX

C

SEATING PLANE

0.05
0.00

⌒ 0.08

□ 1.68± 0.07

5   8

12X 0.5

4

4X

1.5

EXPOSED THERMAL PAD

9

17

SYMM ℄

1

12

PIN 1 ID (OPTIONAL)

16   SYMM   13
      ℄

16X 0.30
    0.18

⊕ 0.1 Ⓜ C A B
0.05 Ⓜ

16X 0.5
    0.3

(DIM A) TYP
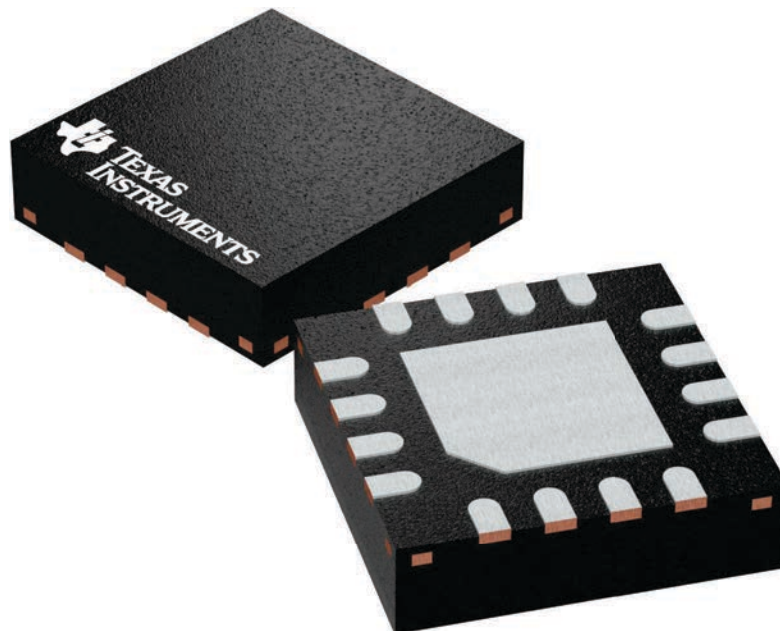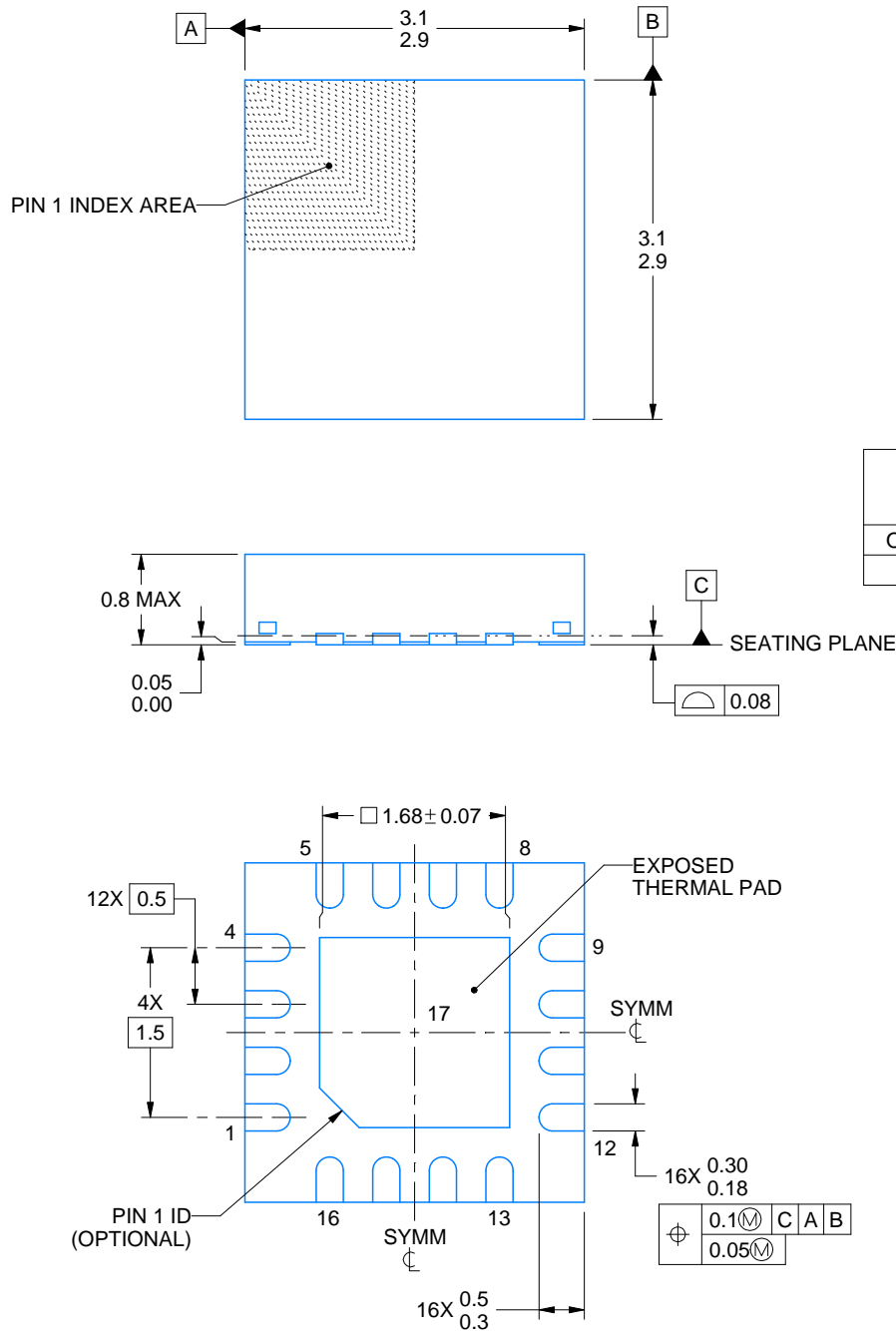
4219117/B   04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

(□ 1.68)

SYMM

16X (0.6)

16X (0.24)

12X (0.5)

(⌀ 0.2) TYP
VIA

(R0.05)
ALL PAD CORNERS

(2.8)

(0.58)
TYP

(0.58) TYP

(2.8)

SYMM
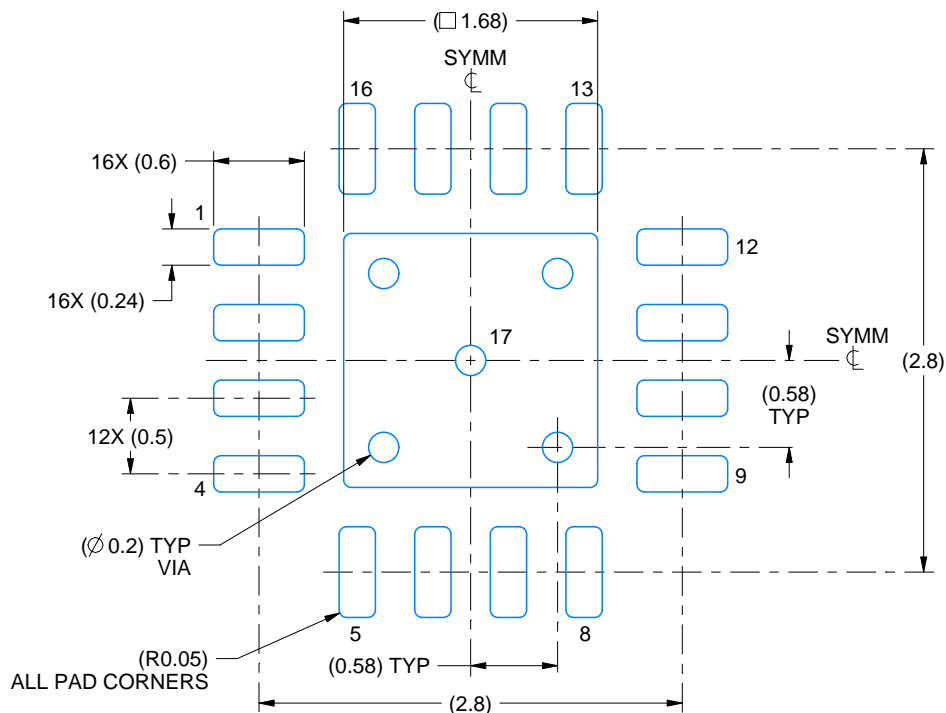
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

METAL

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED
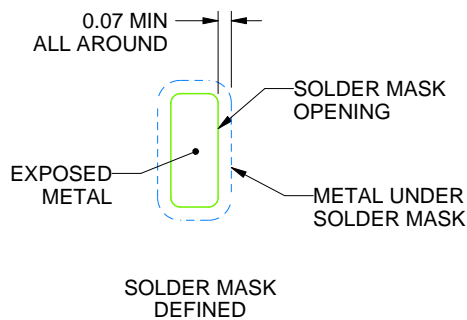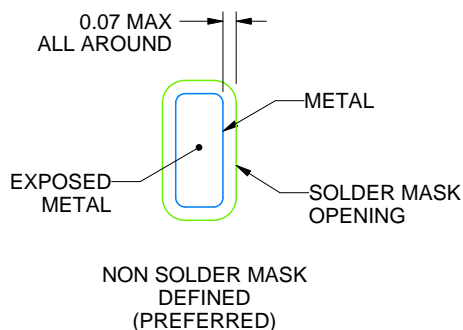
SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
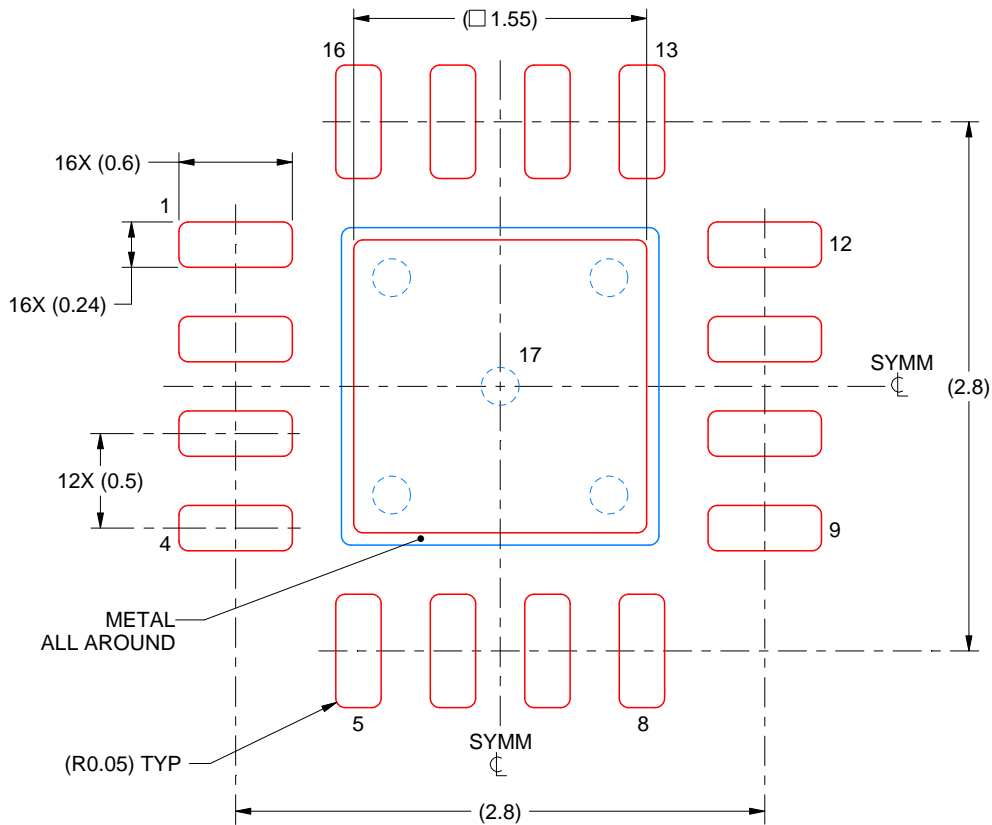
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B   04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.