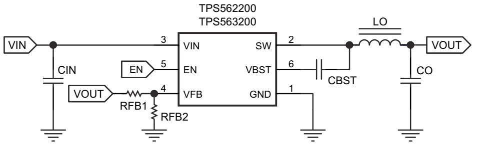
TPS56x200、4.5V～17V 入力、2A、3A 同期整流降圧型レギュレータ 6 ピン SOT-23 パッケージ

1 特長

- 122mΩ および 72mΩ FET を内蔵した TPS562200 - 2A コンバータ
- 68mΩ および 39mΩ FET を内蔵した TPS563200 - 3A コンバータ」
- D-CAP2™ 制御トポロジによる高速過渡応答
- 入力電圧範囲：4.5V～17V
- 出力電圧範囲：0.76V～7V
- スイッチング周波数：650kHz
- 高度な Eco-mode パルス・スキップ
- 低いシャットダウン電流：10μA 未満
- 帰還電圧精度：1% (25℃)
- プリバイアス出力電圧からのスタートアップ
- サイクル単位の過電流制限
- ヒカップ・モード低電圧保護
- 非ラッチ型の OVP、UVLO、および TSD 保護
- 固定ソフト・スタート：1ms
- TPS563252 を使用すると、小型パッケージで効率が向上し、周波数が高くなります
- WEBENCH® ツールによるカスタム設計を作成します

2 アプリケーション

- デジタル・テレビ用電源
- 高精細 Blu-ray Disc™ プレーヤ
- ネットワーク・ホーム・ターミナル
- デジタル・セットトップ・ボックス (STB)



簡略回路図

3 概要

TPS562200 および TPS563200 は、シンプルで使いやすい 2A および 3A 同期整流降圧 (バック) コンバータで、6 ピン SOT-23 パッケージで供給されます。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が小さくなるよう最適化されています。

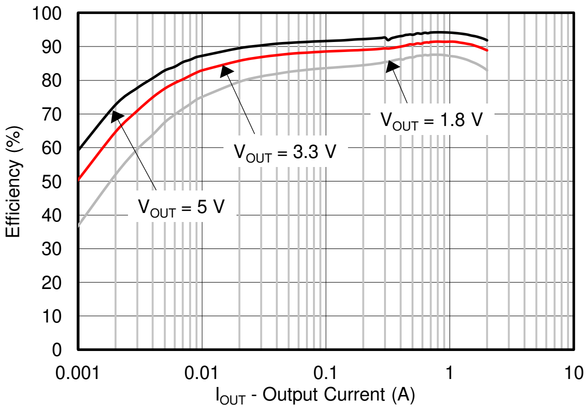
これらのスイッチ・モード電源 (SMPS) デバイスは、D-CAP2 制御トポロジを採用し、高速の過渡応答を実現します。また、特殊ポリマーなど ESR (等価直列抵抗) の低い出力コンデンサと、超低 ESR のセラミック・コンデンサの両方を、外部補償部品なしでサポートします。

TPS562200 および TPS563200 は、高度な Eco-mode を搭載し、軽負荷動作中も高効率を維持します。1.6mm × 2.9mm の 6 ピン SOT (DDC) パッケージで供給され、周囲温度 –40℃～85℃で仕様が規定されています。

製品情報 (1)

部品番号	出力電流 (最大値)	パッケージ
TPS562200	2A	DRL (SOT-236、6)
TPS563200	3A	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



TPS562200 の効率

English Data Sheet: SLVSCB0

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (June 2016) to Revision E (May 2023) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.................... 1
- TPS563252 の情報を追加.................... 1
- 商標の情報を更新.................... 1
- ドキュメント全体にわたって画像の色を除去.................... 1

Changes from Revision C (August 2015) to Revision D (June 2016) **Page**

- Updated the Pinout image in *Pin Configuration And Functions* 4
- Changed $R_{\theta JB}$ for TPS562200 From: 3.4 To: 13.4 in *Thermal Information* 6
- セクション 7.3.1, changed text From: "proportional to the converter input voltage, V_{IN}, and inversely proportional to the output voltage, V_O" To: "inversely proportional to the converter input voltage, V_{IN}, and proportional to the output voltage, V_O".................... 13

Changes from Revision B (July 2014) to Revision C (August 2015) **Page**

- 「特長」を以下のように変更:「内蔵 122mΩ および 72mΩ FET ('562200)」から「122mΩ および 72mΩ FET を内蔵した TPS562200 - 2A コンバータ」.................... 1
- 「特長」を以下のように変更:「内蔵 68mΩ および 39mΩ FET ('563200)」から「68mΩ および 39mΩ FET を内蔵した TPS563200 - 3A コンバータ」.................... 1
- セクション 1 を追加:650kHz のスイッチング周波数.................... 1
- 「特長」を以下のように変更:「サイクル単位のヒカップ過電流制限」から「サイクル単位の過電流制限」.................... 1
- 「特長」を追加:ヒカップ・モード低電圧保護.................... 1
- 「概要」セクションの第 1 段落のテキストを以下のように変更:「SOT-23 パッケージで..」から「6 ピン SOT-23 パッケージで」.................... 1
- Moved Storage temperature range, T_{stg} From: *Handling Ratings* To: *Absolute Maximum Ratings* 5
- Changed the *Handling Ratings* table to the *ESD Ratings* table.................... 5
- Changed the TPS562200 *Thermal Information* values.................... 6
- Changed V_{OVP} Description in the *Electrical Characteristics* From: OVP Detect (L > H) To: OVP Detect, and the TYP value From: 125% To: 125% x Vfbth.................... 7
- Changed V_{UVP} Description in the *Electrical Characteristics* From: Hiccup detect (H < L) To: Hiccup detect , and the TYP value From: 65% To: 65% x Vfbth.................... 7

- Changed the Output Current (A) scale of 図 6-7 8
- Changed V_{OUT} = 5 V To V_{OUT} = 3.3 V in 図 6-15 10
- Changed the X axis From: Junction Temperature To: Ambient Temperature in 図 6-16 10
- Added a NOTE to the Application and Implementation section........ 15
- Changed column heading C8 + C9 (μF) To: C5 + C6 (μF) in 表 8-2 17
- Changed column heading C8 + C9 (μF) To: C5 + C6 + C7 (μF) in 表 8-2 22

Changes from Revision A (January 2014) to Revision B (July 2014)	Page

- 「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- データシートのタイトルを「4.5V～17V 入力、2A、同期整流降圧コンバータ」から「4.5V～17V 入力、2A/3A、同期整流降圧コンバータ」に変更........ 1
- デバイス番号を以下のように変更：TPS563209 から TPS563200........ 1
- 「特長」を以下のように変更：「帰還電圧精度：2% (25℃)」から「帰還電圧精度：1% (25℃)」........ 1
- Added the Timing Requirements table 7
- Added 表 8-1 15
- Changed 表 8-2 17
- Deleted sentence following 表 8-2 "For higher output voltages, additional phase boost can be achieved by adding a feed forward capacitor (C7) in parallel with R2."........ 17
- Added Application Information for the TPS563200 device 22
- Added 表 8-3 22

Changes from Revision * (January 2014) to Revision A (January 2014)	Page

- 製品ステータスを「製品プレビュー」から「量産」に変更........ 1

5 Pin Configuration and Functions

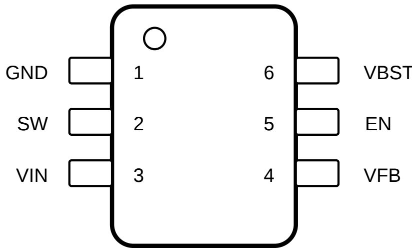


図 5-1. DDC Package 6 Pin (SOT) Top View

表 5-1. Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins.

6 Specifications

6.1 Absolute Maximum Ratings(1)

T_J = -40°C to 150°C(unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10-ns transient)	–0.3	27.5	V
	VBST (vs SW)	–0.3	6.5	V
	VFB	–0.3	6.5	V
	SW	–2	19	V
	SW (10-ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_J = -40°C to 150°C(unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	17	V
V_I	Input voltage range	VBST	–0.1	23	V
		VBST (10-ns transient)	–0.1	26	
		VBST(vs SW)	–0.1	6	
		EN	–0.1	17	
		VFB	–0.1	5.5	
		SW	–1.8	17	
		SW (10-ns transient)	–3.5	20	
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC [1]		TPS562200 DDC (SOT) (6 PINS)	TPS563200 DDC (SOT) (6 PINS)	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.0	87.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	44.5	42.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	13.4	13.6	
Ψ_{JT}	Junction-to-top characterization parameter	2.2	1.9	
Ψ_{JB}	Junction-to-board characterization parameter	13.2	13.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = -40°C to 150°C, VIN = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VIN)}$	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V	TPS562200		230	330	µA
			TPS563200		190	290	
$I_{(VINSDN)}$	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V			3	10	µA
LOGIC THRESHOLD							
$V_{EN(H)}$	EN high-level input voltage	EN		1.6			V
$V_{EN(L)}$	EN low-level input voltage	EN				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
$V_{FB(TH)}$	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10 mA, Eco-mode operation			772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation		758	765	772	mV
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V	TPS562200		122		mΩ
			TPS563200		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C	TPS562200		72		mΩ
			TPS563200		39		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L_{OUT} = 2.2 µF	TPS562200	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V, L_{OUT} = 1.5 µF	TPS563200	3.5	4.2	5.3	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature			155		°C
		Hysteresis			35		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{OVP}	Output OVP threshold	OVP Detect			125% x Vfbth		
V_{UVP}	Output Hiccup threshold	Hiccup detect			65% x Vfbth		
$t_{HiccupOn}$	Hiccup On Time	Relative to soft-start time			1		ms
$t_{HiccupOff}$	Hiccup Off Time	Relative to soft-start time			7		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage		3.45	3.75	4.05	V
		Hysteresis VIN voltage		0.13	0.32	0.55	

(1) Not production tested

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.5 V		260	310	ns
SOFT START						
t_{ss}	Soft-start time	Internal soft-start time, T_A = 25°C	0.7	1	1.3	ms

6.7 Typical Characteristics TPS562200

V_{IN} = 12 V (unless otherwise noted).

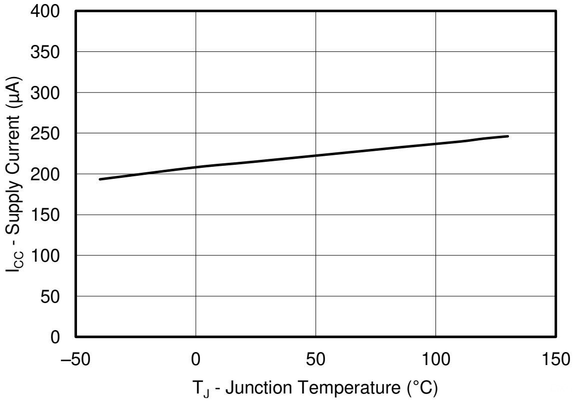
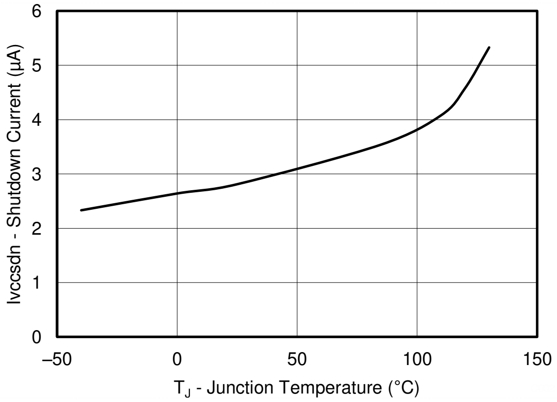
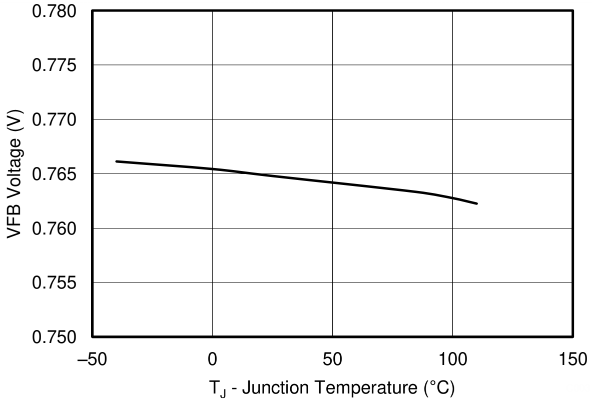


図 6-1. Supply Current vs Junction Temperature



EN = 0 V

図 6-2. VIN Shutdown Current vs Junction Temperature



I_O = 1 A

図 6-3. Vfb Voltage vs Junction Temperature

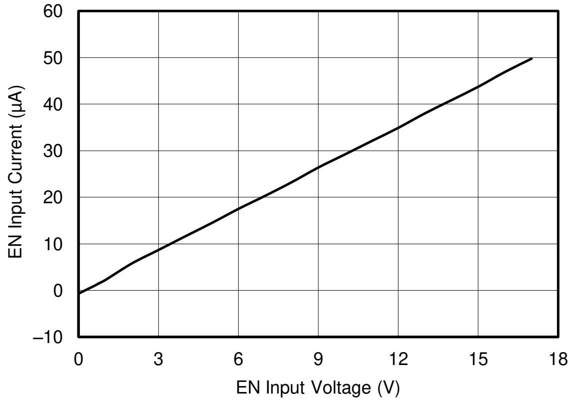


図 6-4. En Current vs En Voltage

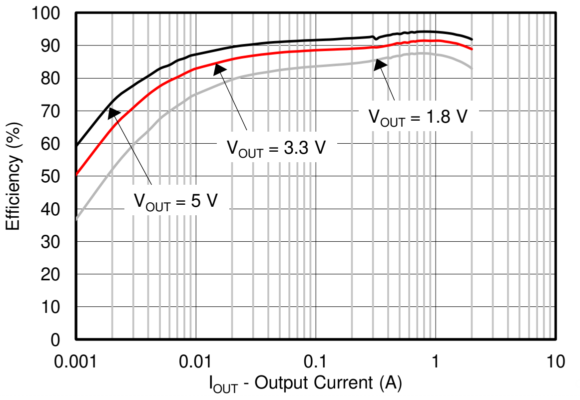
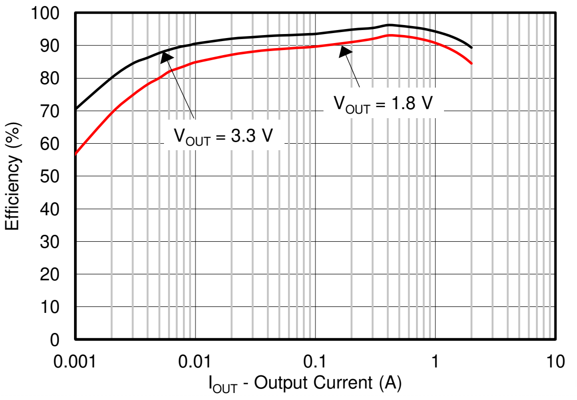


図 6-5. Efficiency vs Output Current



V_{IN} = 5 V

図 6-6. Efficiency vs Output Current

6.7 Typical Characteristics TPS562200 (continued)

V_{IN} = 12 V (unless otherwise noted).

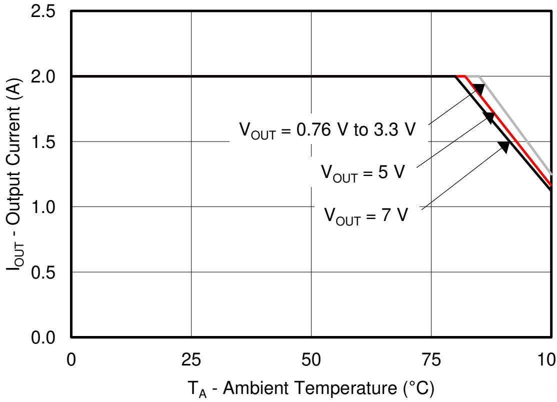
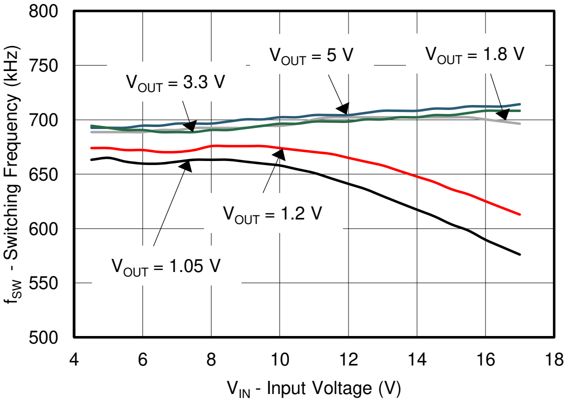


図 6-7. Output Current vs Ambient Temperature



I_{OUT} = 500 mA

図 6-8. Switching Frequency vs Input Voltage

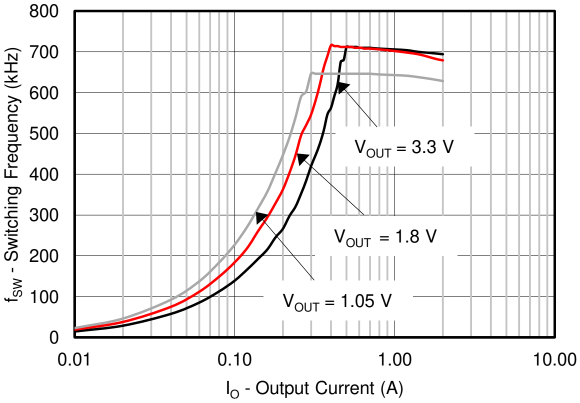


図 6-9. Switching Frequency vs Output Current

6.8 Typical Characteristics TPS563200

V_{IN} = 12 V (unless otherwise noted).

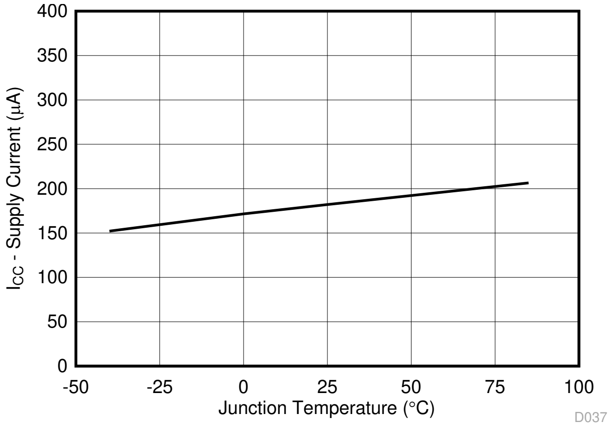
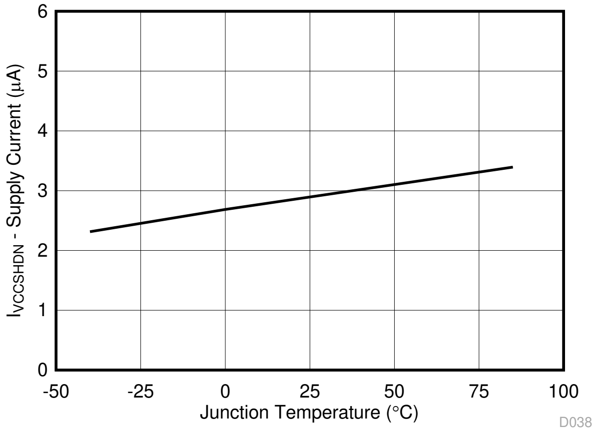
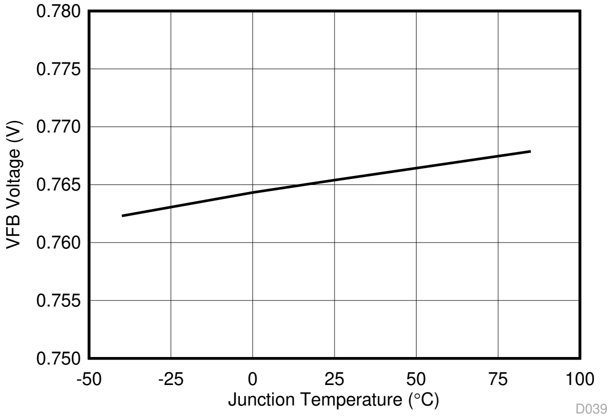


図 6-10. Supply Current vs Junction Temperature



EN = 0 V

図 6-11. VIN Shutdown Current vs Junction Temperature



I_O = 1 A

図 6-12. Vfb Voltage vs Junction Temperature

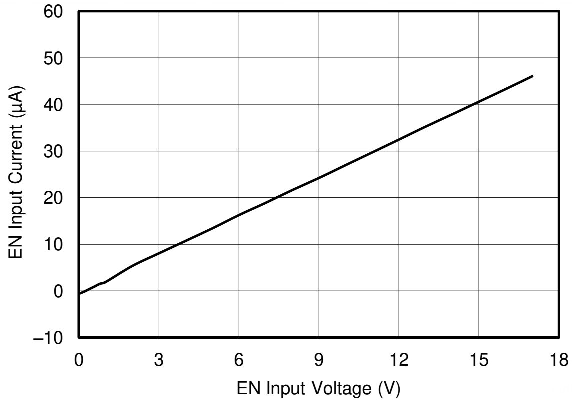


図 6-13. En Current vs En Voltage

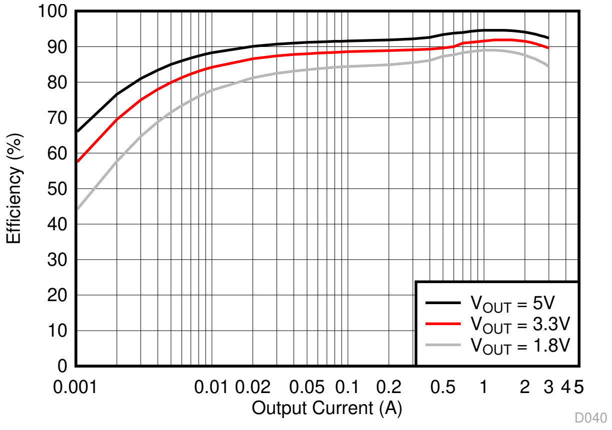
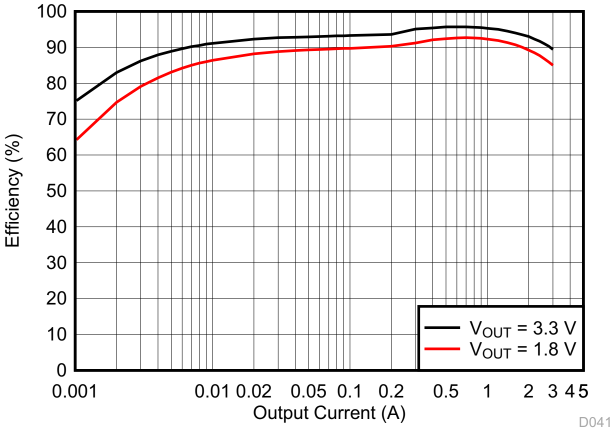


図 6-14. Efficiency vs Output Current



V_{IN} = 5 V

図 6-15. Efficiency vs Output Current

6.8 Typical Characteristics TPS563200 (continued)

V_{IN} = 12 V (unless otherwise noted).

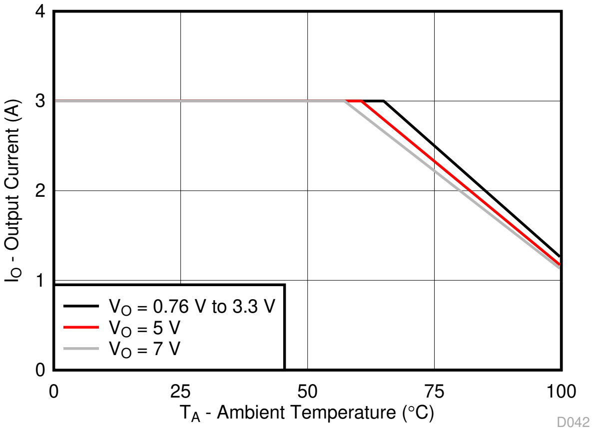
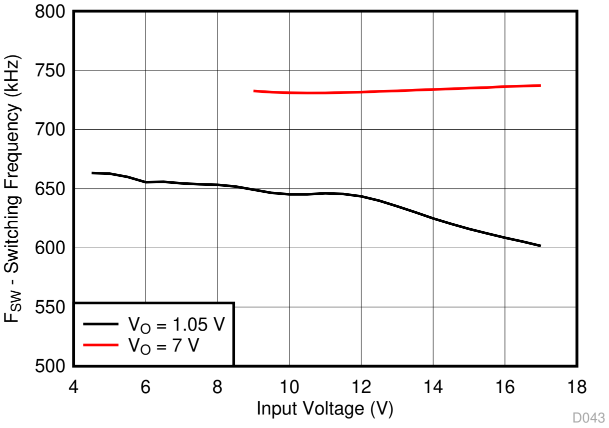


図 6-16. Output Current vs Ambient Temperature



I_{OUT} = 1 A

図 6-17. Switching Frequency vs Input Voltage

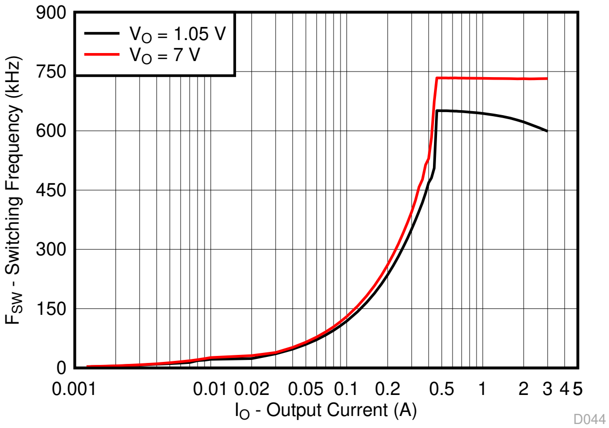


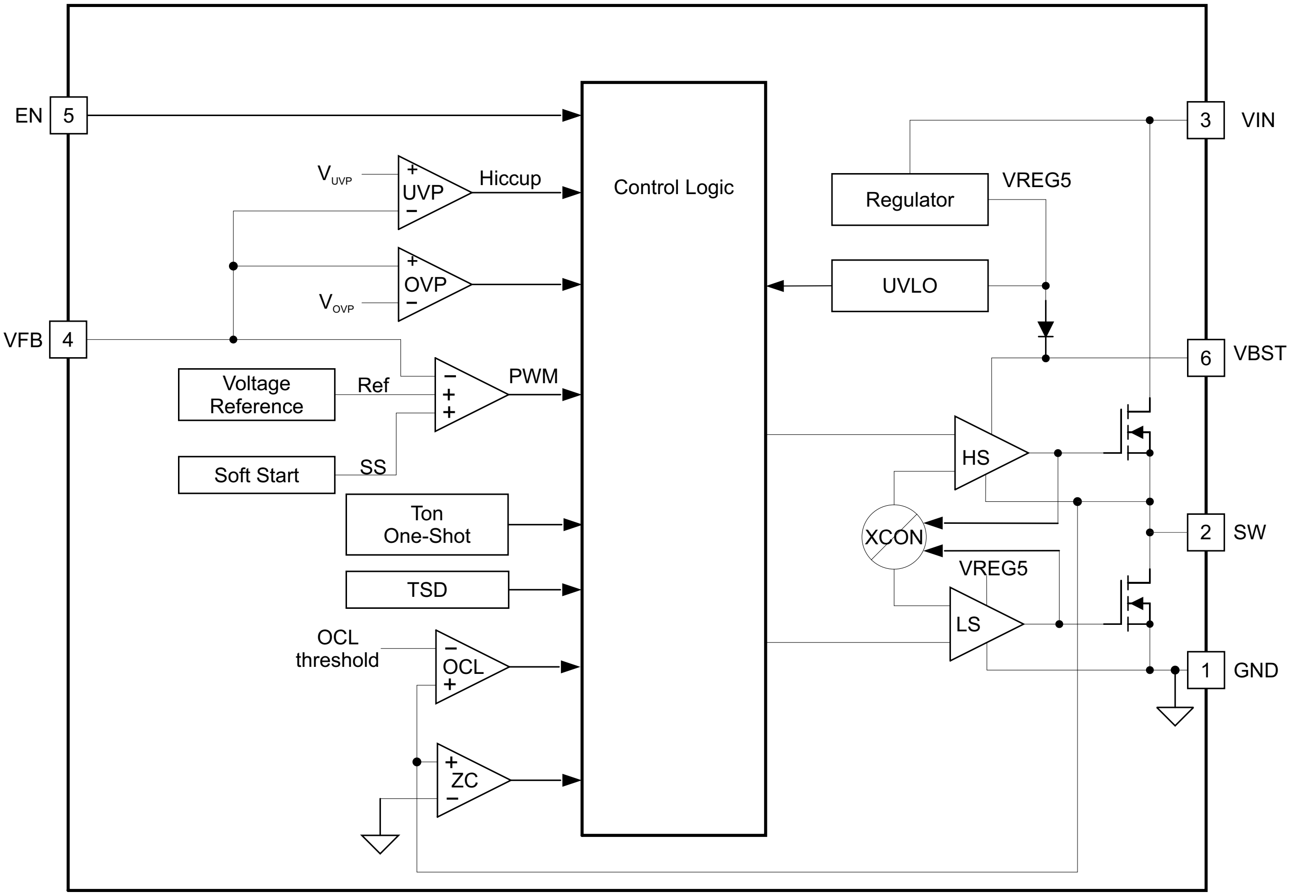
図 6-18. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS562200 and TPS563200 are 2-A and 3-A synchronous step-down converters. The proprietary D-CAP2 control scheme supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 control scheme can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 The Adaptive On-Time Control And PWM Operation

The main control loop of the TPS562200 and TPS563200 are adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 control scheme. The D-CAP2 control scheme combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set inversely proportional to the converter input voltage, V_{IN}, and proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 control scheme.

7.3.2 Advanced Eco-mode Control

The TPS562200 and TPS563200 are designed with Advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{1}$$

7.3.3 Soft Start And Pre-Biased Soft Start

The TPS562200 and TPS563200 have an internal 1 ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Current Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter. This can cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. Then, the device shuts down after the UVP delay time (typically 14 µs) and re-start after the hiccup time (typically 12 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

7.3.5 Over Voltage Protection

TPS562200 and TPS563200 detect overvoltage condition by monitoring the feedback voltage (VFB). When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET driver and the low-side MOSFET driver turn off. This function is non-latch operation.

7.3.6 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.7 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS562200 and TPS563200 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS562200 and TPS563200 operate at a quasi-fixed frequency of 650 kHz.

7.4.2 Eco-mode Operation

When the TPS562200 and TPS563200 are in the normal CCM operating mode and the switch current falls to 0 A, the TPS562200 and TPS563200 begin operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-mode threshold voltage. As the output current decreases the perceived time between switching pulses increases.

7.4.3 Standby Operation

When the TPS562200 and TPS563200 are operating in either normal CCM or Eco-mode, they can be placed in standby by asserting the EN pin low.

8 Application and Implementation

注

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8.1 Application Information

The TPS562200 and TPS563200 are typically used as step down converters, which convert a voltage from 4.5 V – 17 V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits

8.2 Typical Applications

8.2.1 Tps562200 4.5-V To 17-V Input, 1.05-V Output Converter

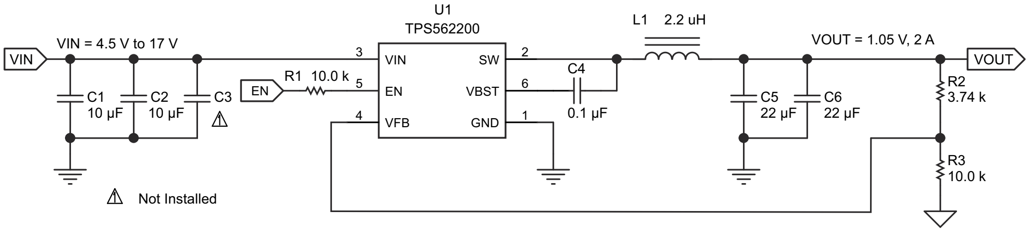

図 8-1. Tps562200 1.05v/2a Reference Design

8.2.1.1 Design Requirements

To begin the design process, the user must know a few application parameters:

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	2 A
Output voltage ripple	20 mVpp

8.2.1.2 Detailed Design Procedures

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the WEBENCH Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.

8.2.1.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate V_{OUT}.

To improve efficiency at light loads consider using larger value resistors, too high of resistance is more susceptible to noise and voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R2}{R3}\right) \tag{2}$$

8.2.1.2.3 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 control scheme introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.

表 8-2. TPS562200 Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1(uH)			C5 + C6 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 - 68
1.05	3.74	10.0	1.5	2.2	4.7	20 - 68
1.2	5.76	10.0	1.5	2.2	4.7	20 - 68
1.5	9.53	10.0	1.5	2.2	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	2.2	3.3	4.7	20 - 68
3.3	33.2	10.0	2.2	3.3	4.7	20 - 68
5	54.9	10.0	3.3	4.7	4.7	20 - 68
6.5	75	10.0	3.3	4.7	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 式 5 and the RMS current of 式 6.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$Il_{PEAK} = I_O + \frac{Il_{P-P}}{2} \tag{5}$$

$$I_{LO(RMS)} = \sqrt{I_O^{2} + \frac{1}{12} Il_{P-P}^{2}} \tag{6}$$

For this design example, the calculated peak current is 2.34 A and the calculated RMS current is 2.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5 A and an RMS current rating of 4.3 A

The capacitor value and ESR determines the amount of output voltage ripple. The device is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design, two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

8.2.1.2.4 Input Capacitor Selection

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor(C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.1.2.5 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.1.3 Application Curves

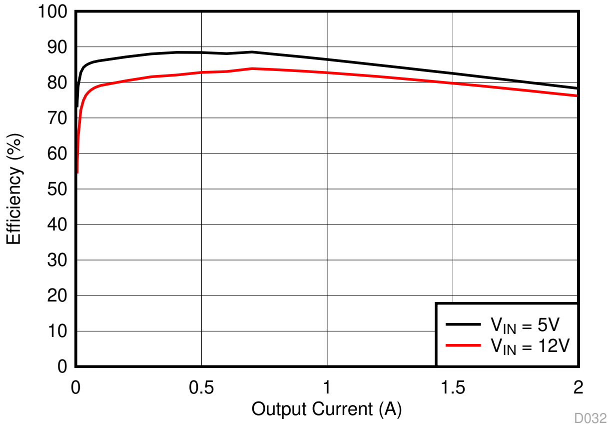

図 8-2. Tps562200 Efficiency

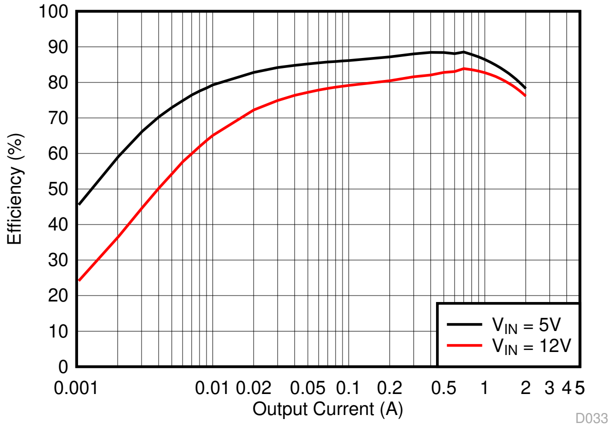

図 8-3. Tps562200 Light Load Efficiency

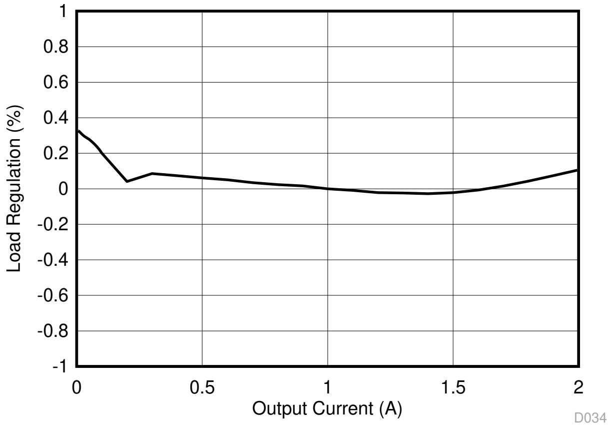

図 8-4. Tps562200 Load Regulation, V_I = 5 V

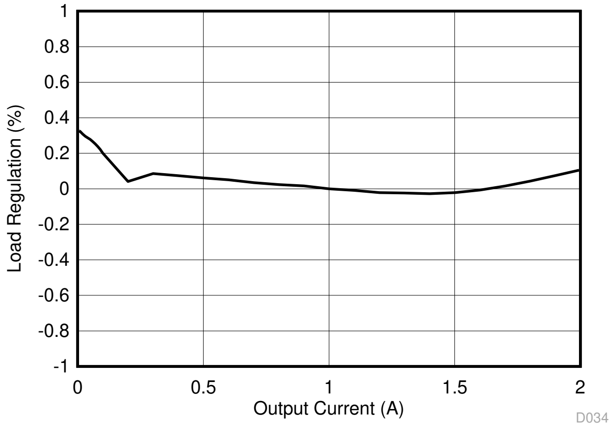

図 8-5. Tps562200 Load Regulation, V_I = 12 V

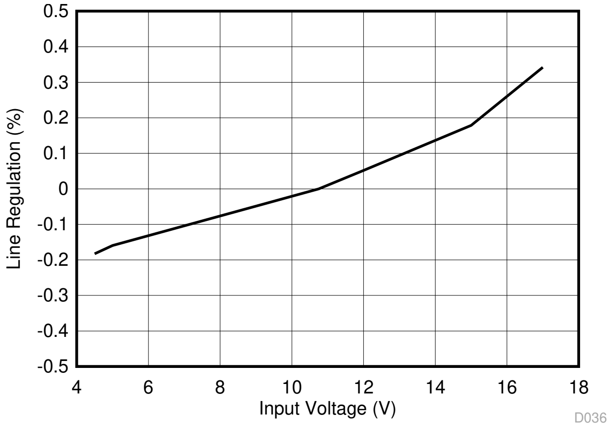

図 8-6. Tps562200 Line Regulation

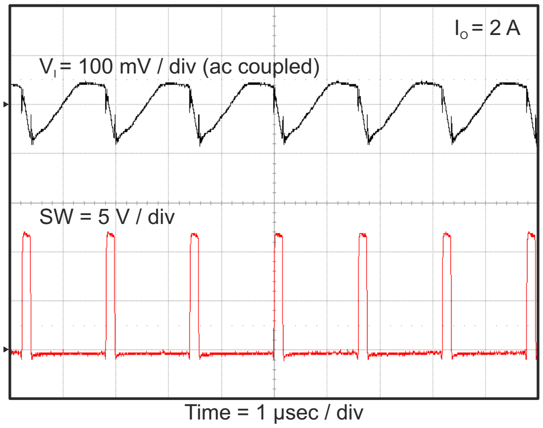

図 8-7. Tps562200 Input Voltage Ripple

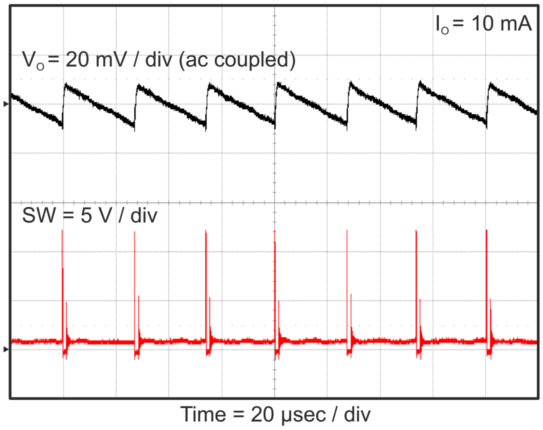

図 8-8. Tps562200 Output Voltage Ripple

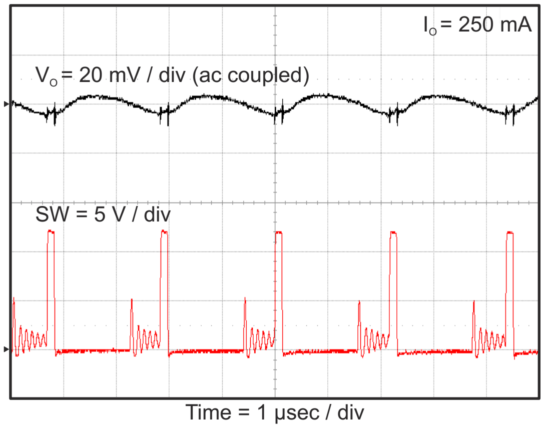

図 8-9. Tps562200 Output Voltage Ripple

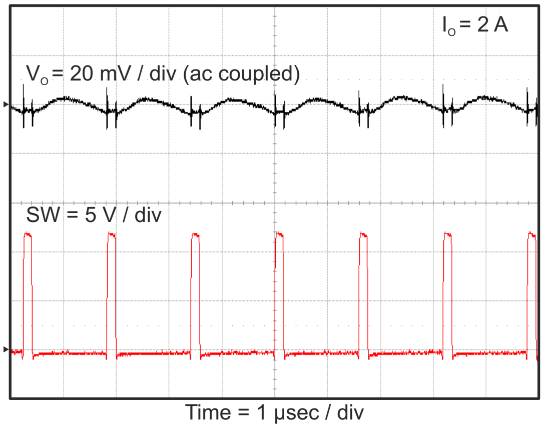

図 8-10. Tps562200 Output Voltage Ripple

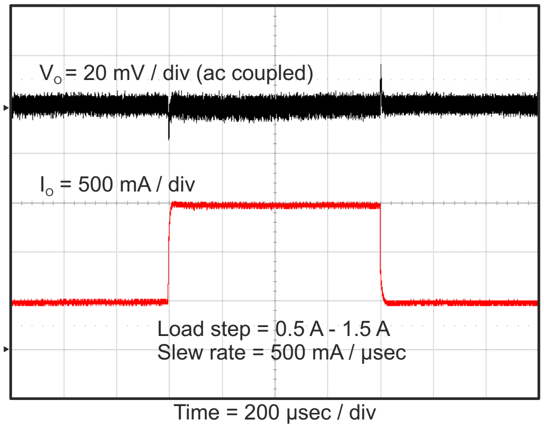

図 8-11. Tps562200 Transient Response

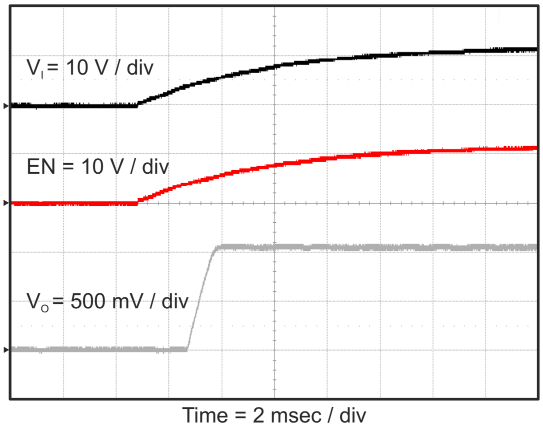

図 8-12. Tps562200 Start Up Relative to V_I

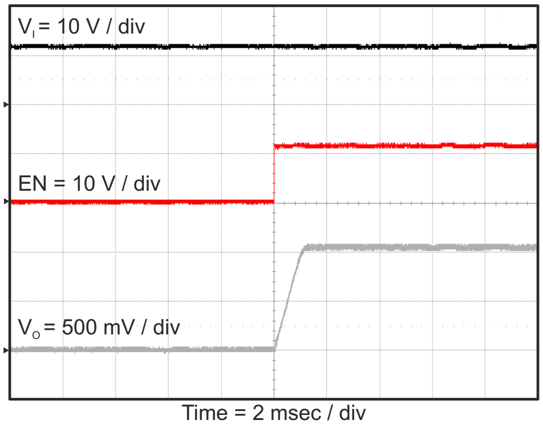

図 8-13. Tps562200 Start Up Relative to En

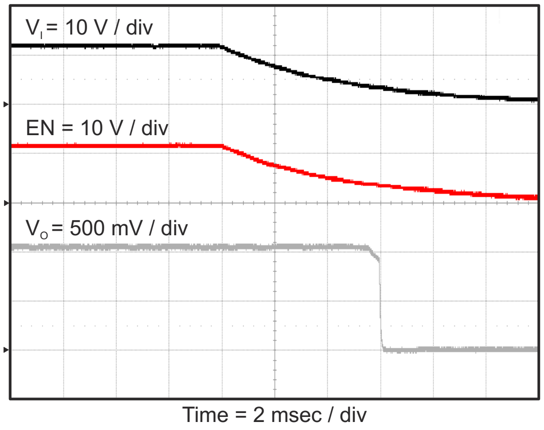

図 8-14. Tps562200 Shut Down Relative to V_I

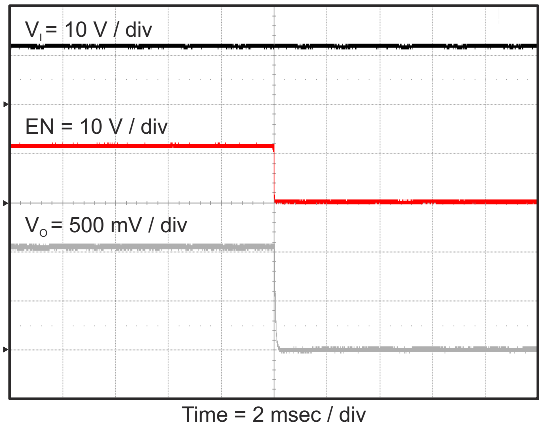

図 8-15. Tps562200 Shut Down Relative to En

8.2.2 Tps563200 4.5-V To 17-V Input, 1.05-V Output Converter

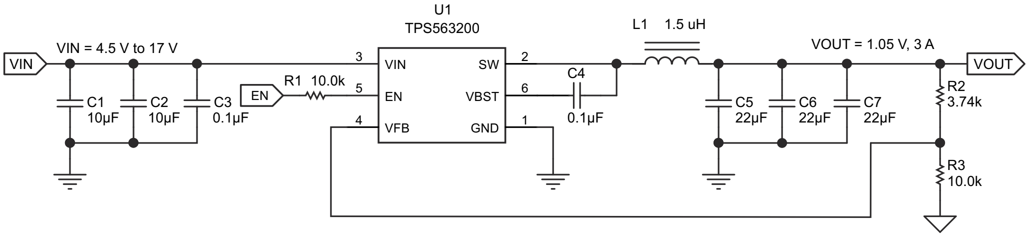

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図 8-16. Tps563200 1.05v/3a Reference Design

8.2.2.1 Design Requirements

To begin the design process, the user must know a few application parameters:

表 8-3. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	3 A
Output voltage ripple	20 mVpp

8.2.2.2 Detailed Design Procedures

The detailed design procedure for TPS563200 is the same as for TPS562200 except for inductor selection.

8.2.2.2.1 Output Filter Selection

表 8-4. Tps563200 Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1 (µH) MIN	L1 (µH) TYP	L1 (µH) MAX	C5 + C6 + C7 (µF)
1	3.09	10.0	1.0	1.5	4.7	20 - 68
1.05	3.74	10.0	1.0	1.5	4.7	20 - 68
1.2	5.76	10.0	1.0	1.5	4.7	20 - 68
1.5	9.53	10.0	1.0	1.5	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	1.5	2.2	4.7	20 - 68
3.3	33.2	10.0	1.5	2.2	4.7	20 - 68
5	54.9	10.0	2.2	3.3	4.7	20 - 68
6.5	75	10.0	2.2	3.3	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 8, 式 9 and 式 10. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 式 9 and the RMS current of 式 10.

$$\mathrm{Il}_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (8)$$

$$I_{lPEAK} = I_O + \frac{I_{lP-P}}{2} \tag{9}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{lP-P}^2} \tag{10}$$

For this design example, the calculated peak current is 3.505 A and the calculated RMS current is 3.014 A. The inductor used is a TDK CLF7045T-1R5N with a peak current rating of 7.3 A and an RMS current rating of 4.9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563209 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use Equation 6 to determine the required RMS current rating for the output capacitor. For this design three TDK C3216X5R0J226M 22μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.292 A and each output capacitor is rated for 4 A.

8.2.2.3 Application Curves

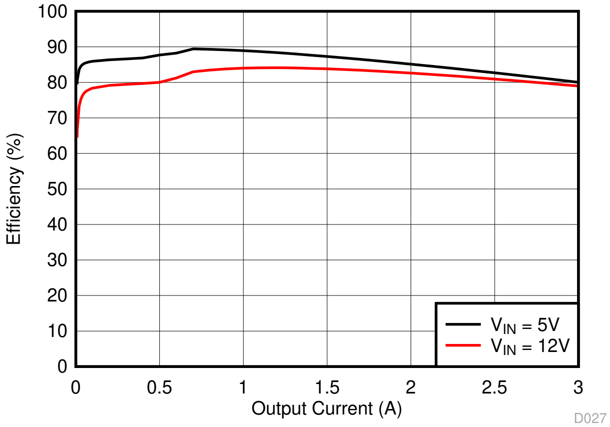

図 8-17. Tps563200 Efficiency

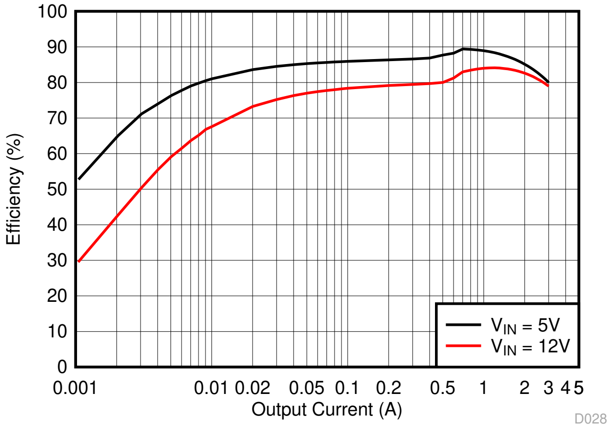

図 8-18. Tps563200 Light Load Efficiency

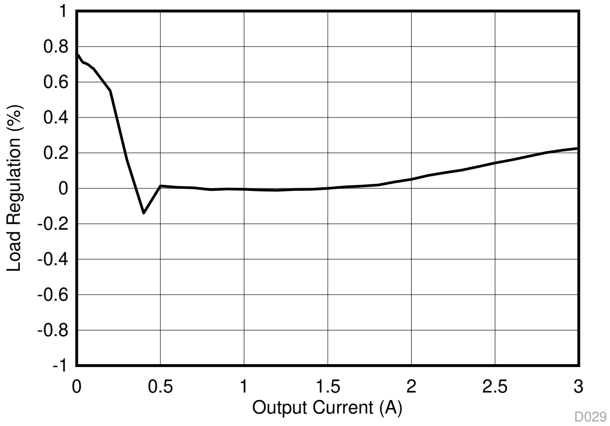

図 8-19. Tps563200 Load Regulation, V_I = 5 V

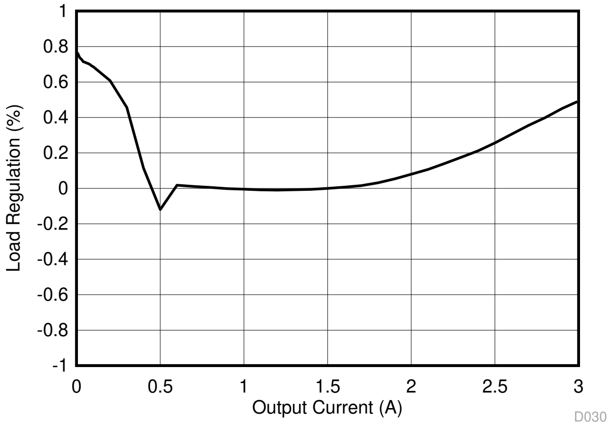

図 8-20. Tps563200 Load Regulation, V_I = 12 V

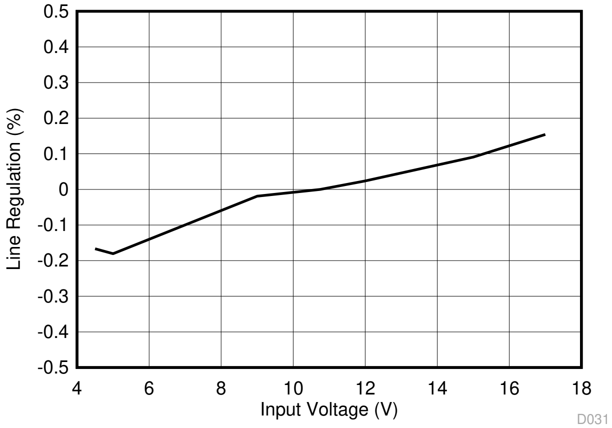

図 8-21. Tps563200 Line Regulation

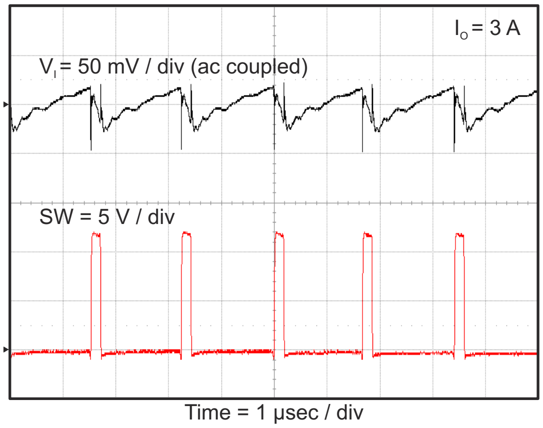

図 8-22. Tps563200 Input Voltage Ripple

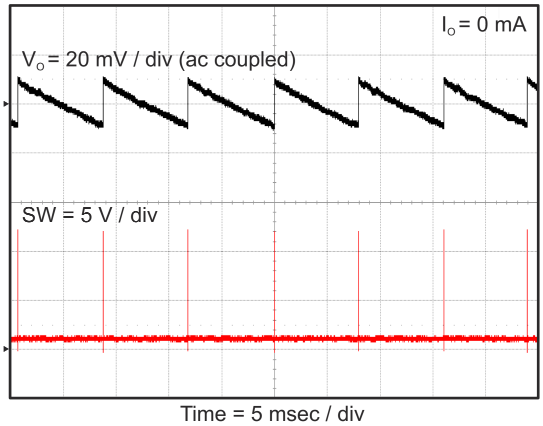

図 8-23. Tps563200 Output Voltage Ripple

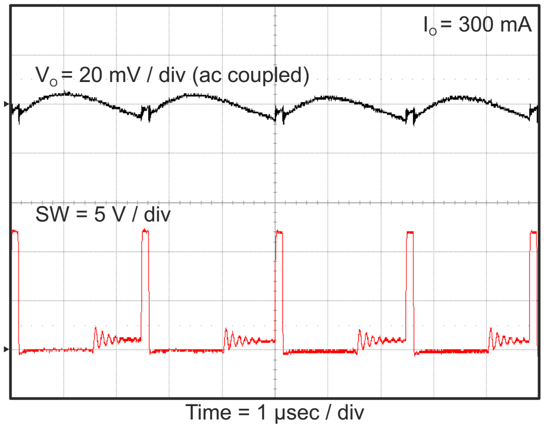

図 8-24. Tps563200 Output Voltage Ripple

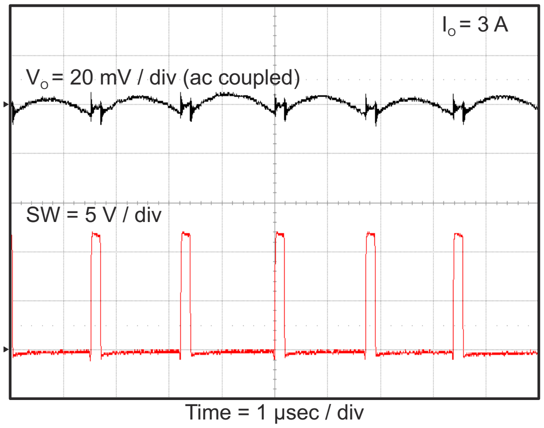

図 8-25. Tps563200 Output Voltage Ripple

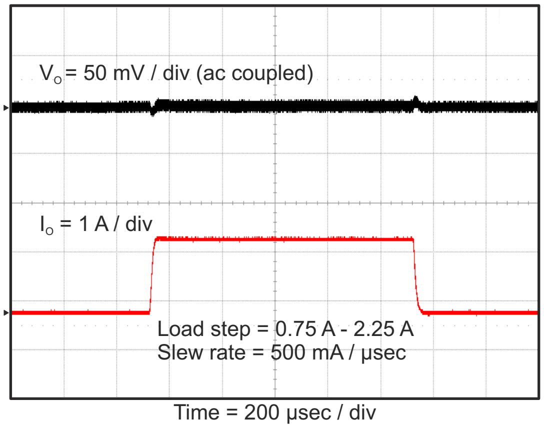

図 8-26. Tps563200 Transient Response

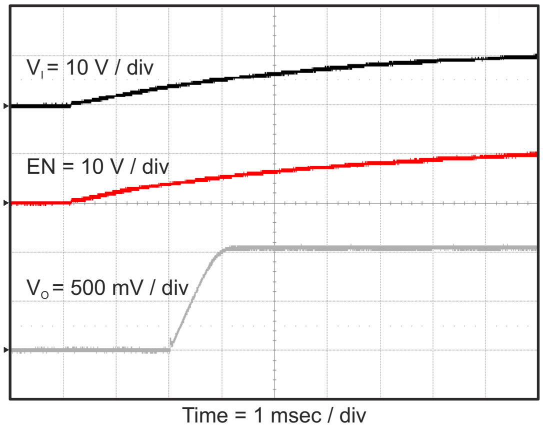

図 8-27. Tps563200 Start-up Relative to V_I

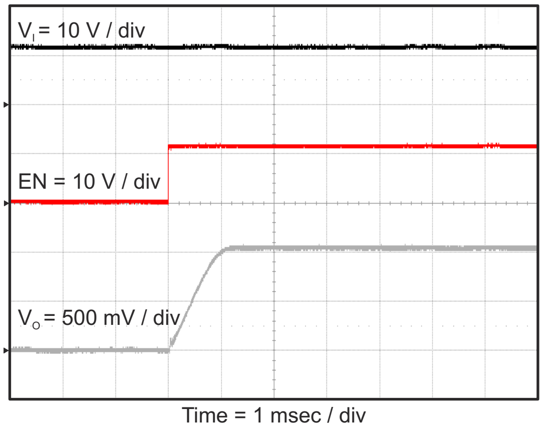

図 8-28. Tps563200 Start-up Relative to En

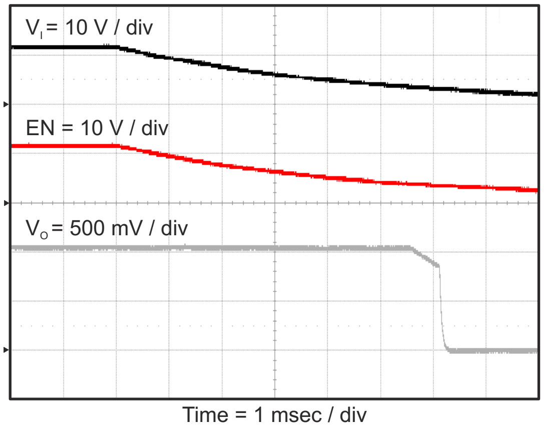

図 8-29. Tps563200 Shut Down Relative to V_I

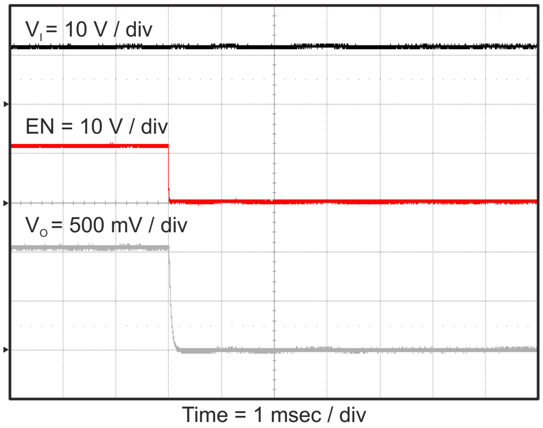

図 8-30. Tps563200 Shutdown Relative to En

8.3 Power Supply Recommendations

The TPS562200 and TPS563200 are designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is V_O / 0.65.

8.4 Layout

8.4.1 Layout Guidelines

1. VIN and GND traces must be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor must be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path must be connected to the upper feedback resistor
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop must be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node must be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin must be as wide as possible to minimize its trace impedance.

8.4.2 Layout Example

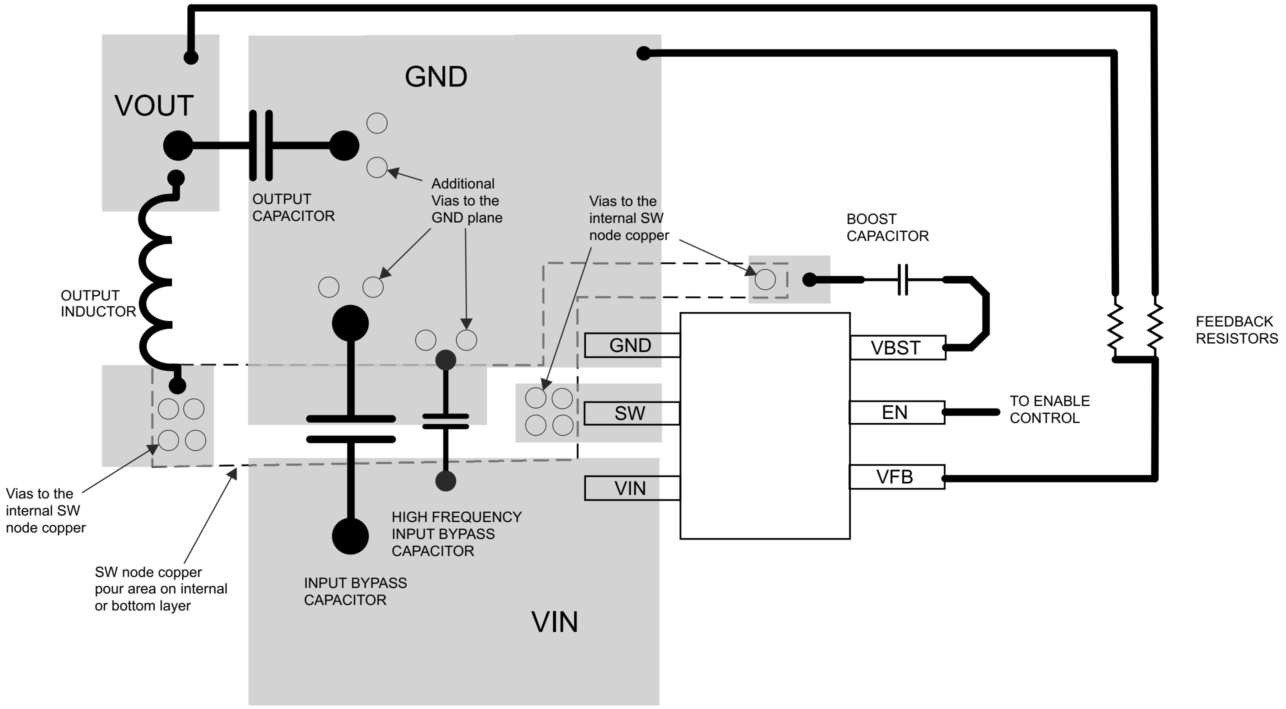

図 8-31. Typical Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the WEBENCH Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS562200DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	200	Samples
TPS562200DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	200	Samples
TPS563200DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	320	Samples
TPS563200DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	320	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

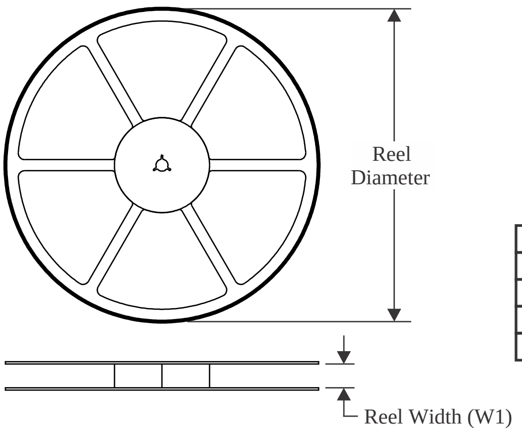
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

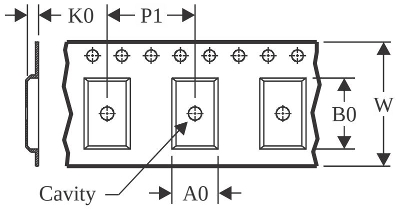
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

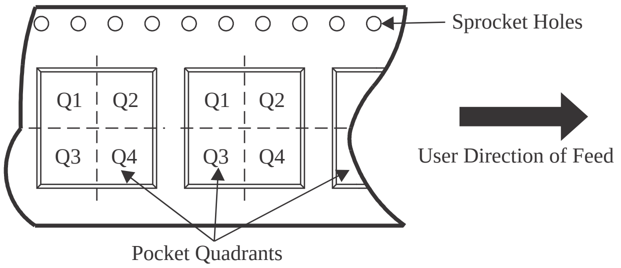


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

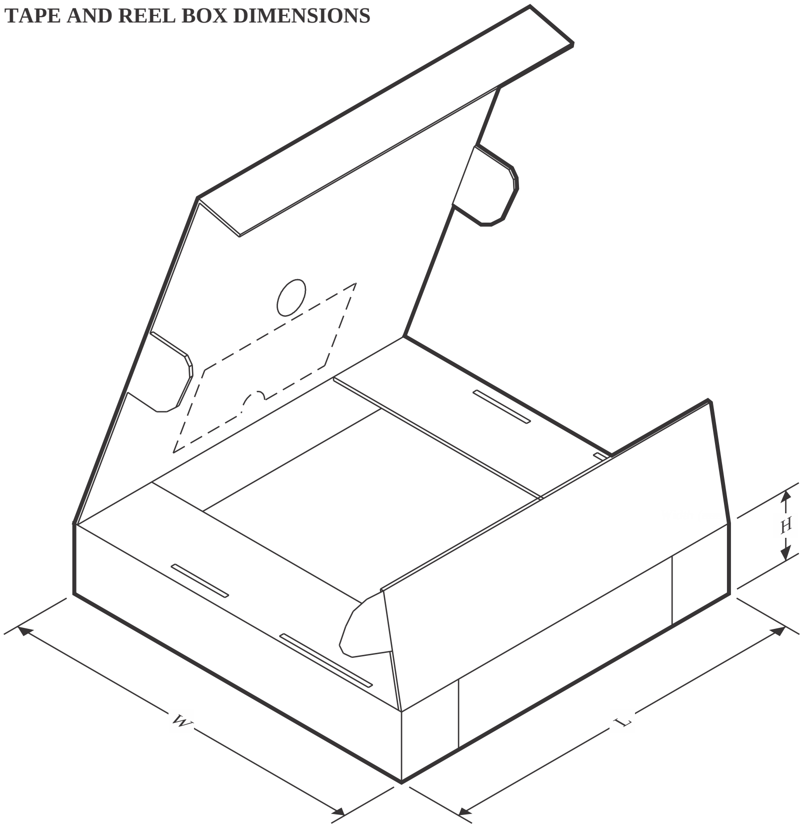
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

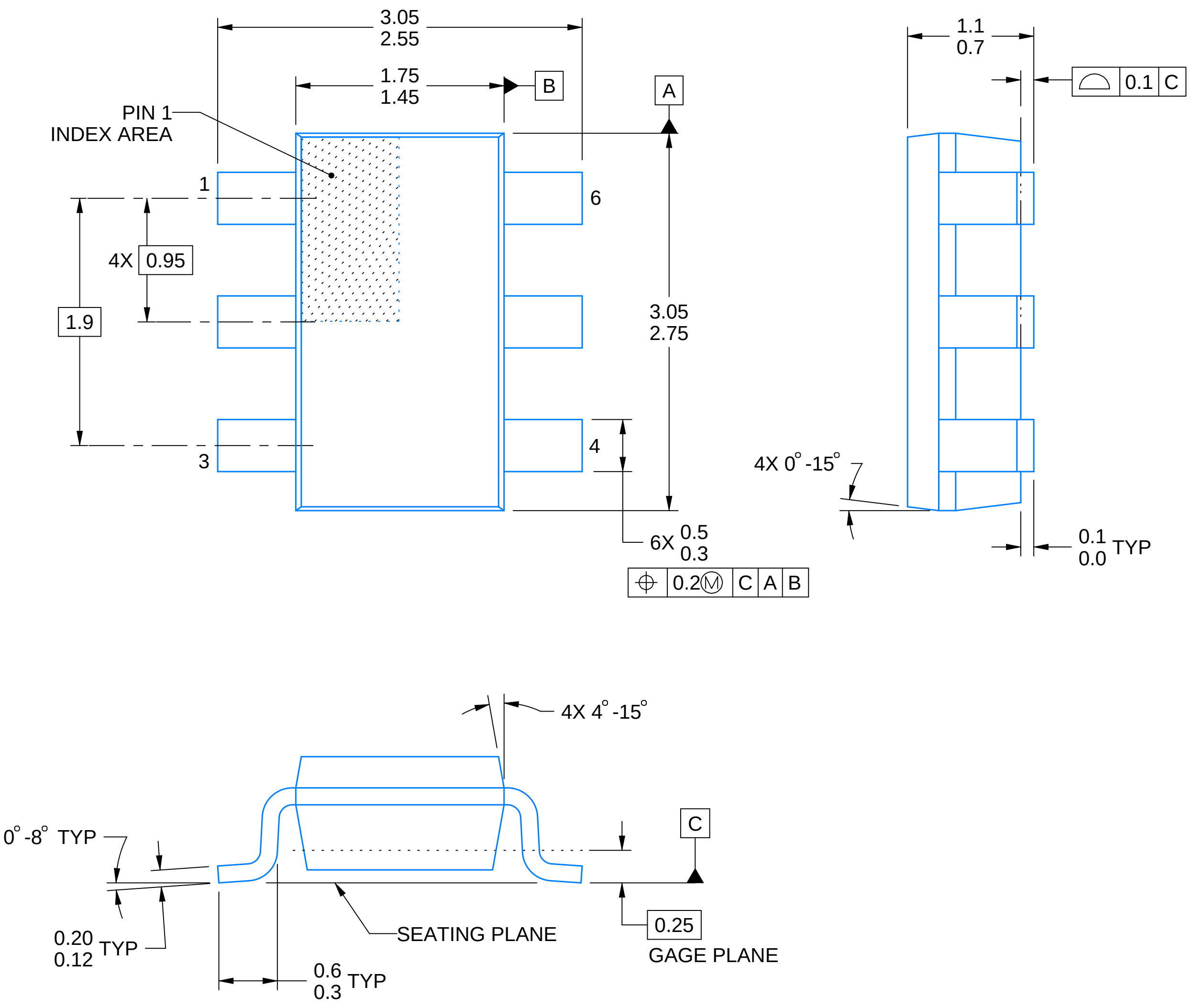
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS562200DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS562200DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563200DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563200DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS562200DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS562200DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
TPS563200DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563200DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0



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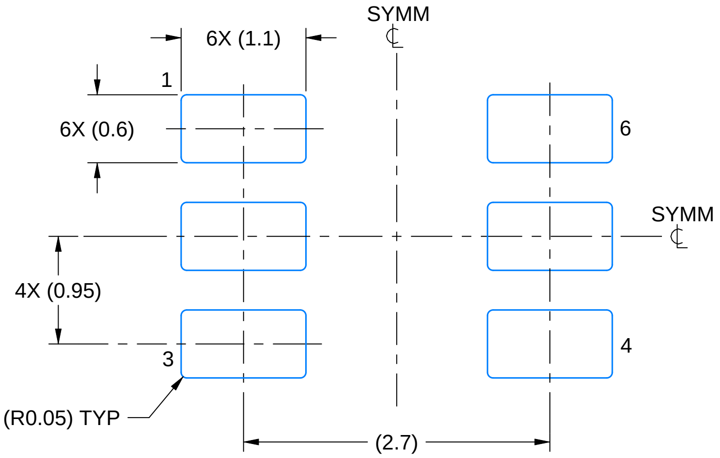
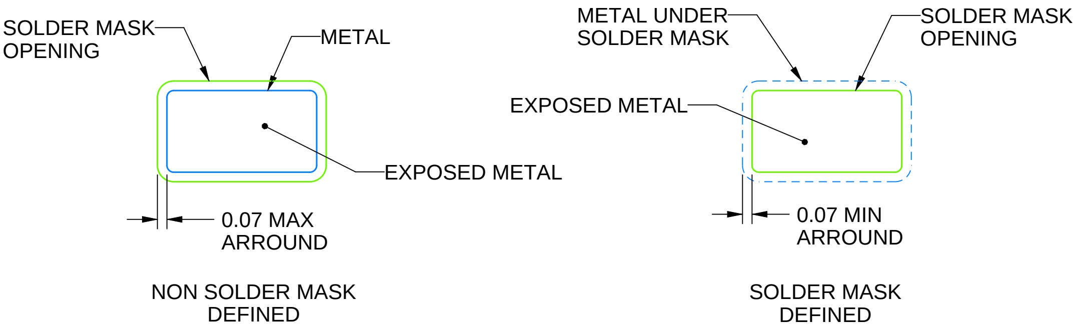
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



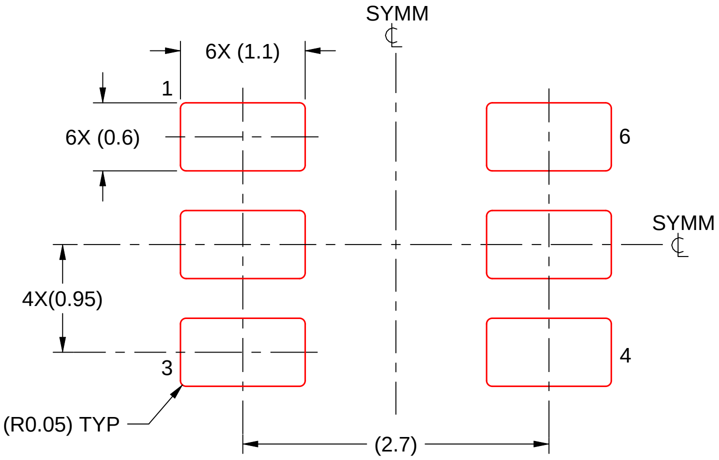
LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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