TPS563249 17V、3A、固定 1.4MHz 同期整流降圧電圧レギュレータ

1 特長

- 70mΩおよび 30mΩのFET内蔵の3Aコンバータ
- D-CAP3™モード制御による高速過渡応答
- 入力電圧範囲: 4.5V～17V
- 出力電圧範囲: 0.6V～7V
- 強制連続導通モード
- 固定1.4MHzのスイッチング周波数
- 低いシャットダウン電流: 10μA未満
- 帰還電圧精度: 1% (25℃)
- プリバイアス出力電圧からのスタートアップ
- サイクル単位の過電流制限
- ヒカップ・モードによる過電流保護
- 非ラッチUVPおよびTSD保護
- 固定ソフトスタート: 1.7ms

2 アプリケーション

- ブロードバンド・モデム
- アクセス・ポイント・ネットワーク
- ワイヤレス・ルータ
- 監視機器
- TV、セットトップ・ボックス

3 概要

TPS563249は、単純で使いやすい3A同期整流降圧型コンバータで、SOT-23パッケージに搭載されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が低くなるよう最適化されています。

このスイッチング・レギュレータは、D-CAP3 モード制御によって高速の過渡応答を実現します。また、特殊ポリマーなど ESR (等価直列抵抗) の低い出力コンデンサと、超低 ESR のセラミック・コンデンサの両方を、外部補償部品なしでサポートします。

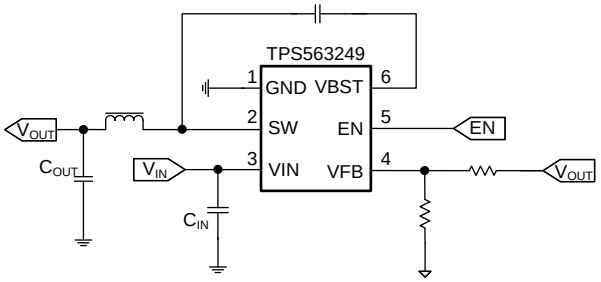
TPS563249は強制連続導通モード(FCCM)で動作し、軽負荷での動作時にも1.4MHzの固定スイッチング周波数を維持し、システムの干渉を排除します。TPS563249は6ピンの1.6mm×2.9mm SOT (DDC)パッケージで供給され、接合部温度-40℃～125℃で動作が規定されています。

製品情報(1)

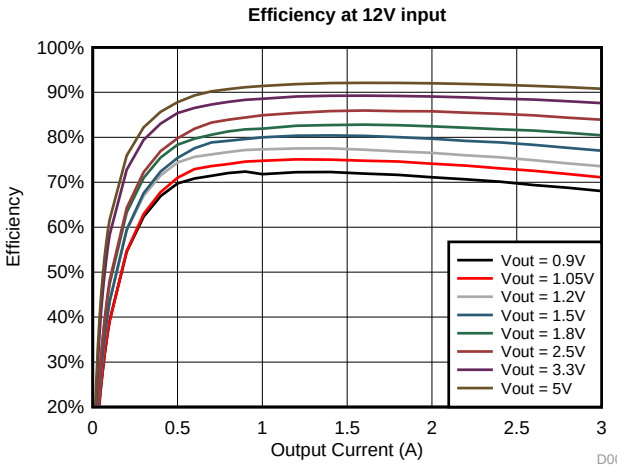
型番	パッケージ	本体サイズ(公称)
TPS563249	SOT-23-THIN (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



TPS563249の効率



目次

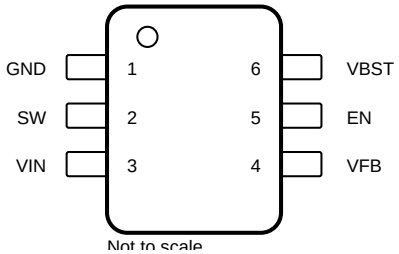
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2018年12月	*	初版

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	19	V
	VBST	–0.3	24.5	V
	VBST (10 ns transient)	–0.3	26.5	V
	VBST (vs SW)	–0.3	5.5	V
	VFB	–0.3	5.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
	EN	-0.3	V_{IN} + 0.3	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range	4.5		17	V
EN	EN Input voltage range	–0.1		V_{IN}	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS563249 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{VIN(SDN)}$	Shutdown supply current	V_{IN} current, EN = 0 V, T_J = 25°C		2.5	10	µA
LOGIC THRESHOLD						
V_{ENH}	Enable threshold	Rising		1.27	1.34	V
V_{ENL}	Enable threshold	Falling	1.08	1.15		V
R_{EN}	EN pin resistance to GND	V_{EN} = 1 V	800	1000	1200	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FB}	FB voltage	T_J = 25°C	594	600	606	mV
			588	600	612	mV
I_{FB}	FB input current	V_{FB} = 0.7 V		0	±50	nA
MOSFET						
$R_{DS(on)h}$	High-side switch resistance	T_J = 25°C		70		mΩ
$R_{DS(on)l}$	Low-side switch resistance	T_J = 25°C		30		mΩ
CURRENT LIMIT						
$I_{ocl\_h\_source}$	High side FET source Current limit		5.5	6.3	7.1	A
$I_{ocl\_l\_source}$	Low side FET source Current limit		3.1	3.9	4.7	A
$I_{ocl\_l\_sink}$	Low side FET sink Current limit		1.1	1.7		A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		160		°C
		Hysteresis		25		
ON-TIME TIMER CONTROL						
$t_{ON(MIN)}$	Minimum on time(1)	V_{IN} = 12 V, load = 3 A		50		ns
$t_{OFF(MIN)}$	Minimum off time			250		ns
SOFT START						
t_{ss}	Soft-start time	Internal soft-start time		1.7		ms
FREQUENCY						
F_{sw}	Switching frequency		1250	1400	1550	kHz
OUTPUT UNDERVOLTAGE PROTECTION						
V_{UVP}	Output UVP threshold	Hiccup detect (H > L)		65%		
t_{UVPDLY}	UVP propagation delay			0.36		ms
t_{HIC}	UVP protection Hiccup Time before restart			25		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage		4.2	4.4	V
		Shutdown VIN voltage	3.6	3.8		
		Hysteresis VIN voltage		0.4		

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

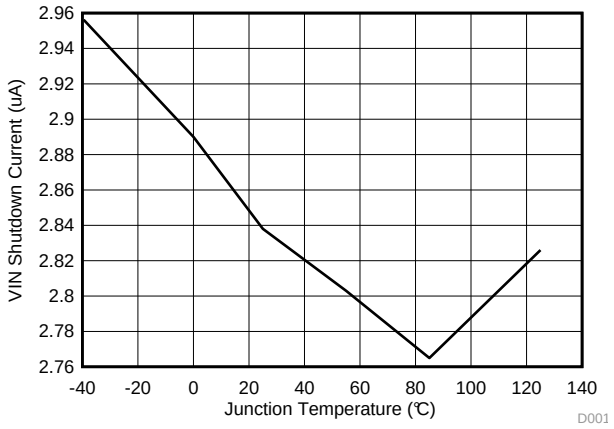


図 1. Shutdown Current vs Junction Temperature

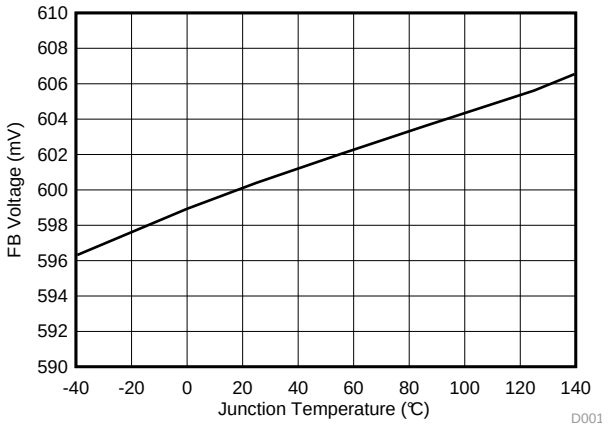


図 2. VFB Voltage vs Junction Temperature

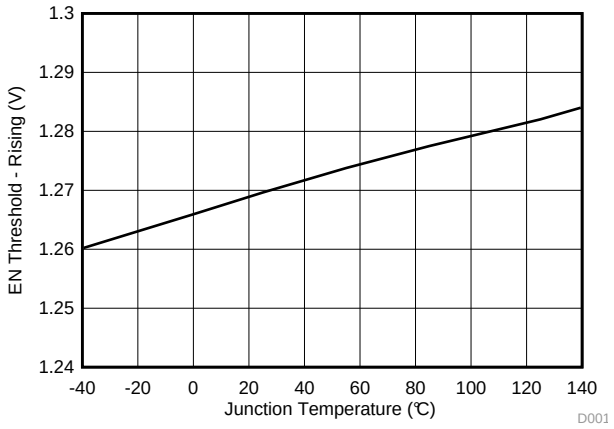


図 3. EN Rising threshold vs Junction Temperature

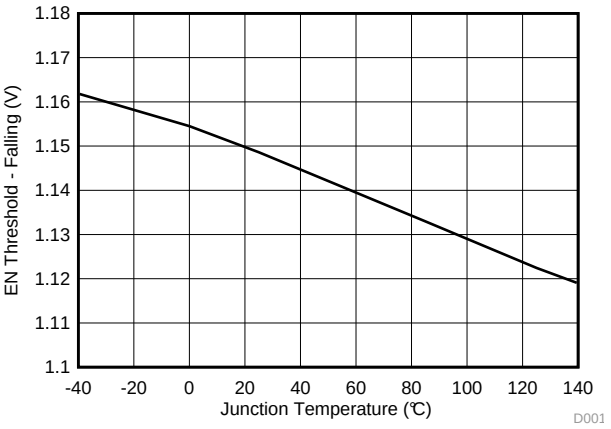


図 4. EN Falling threshold vs Junction Temperature

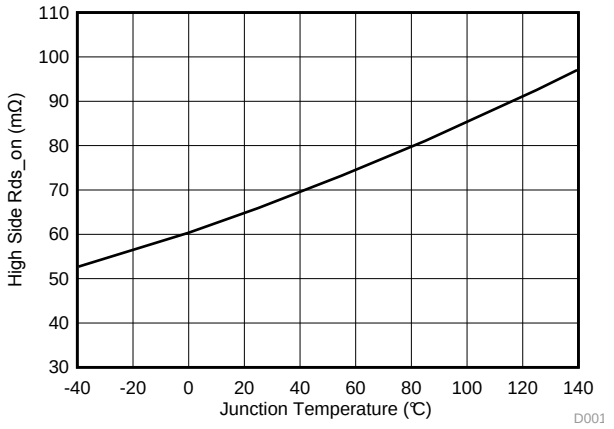


図 5. High-Side $R_{ds(On)}$ vs Junction Temperature

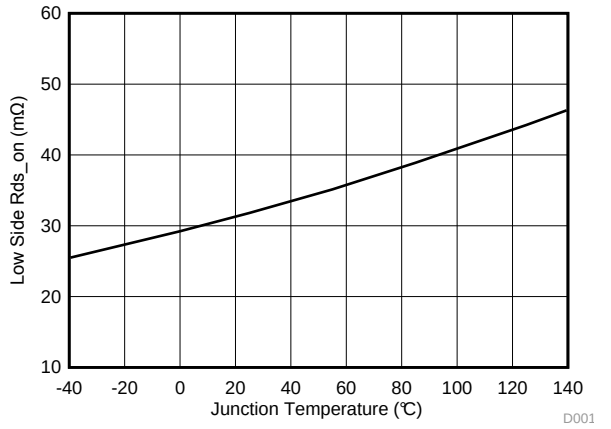


図 6. Low-Side $R_{ds(On)}$ vs Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

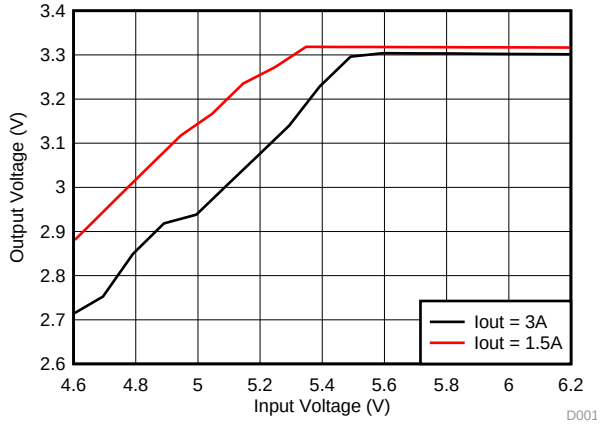


図 7. Dropout for 3.3 V Output Voltage

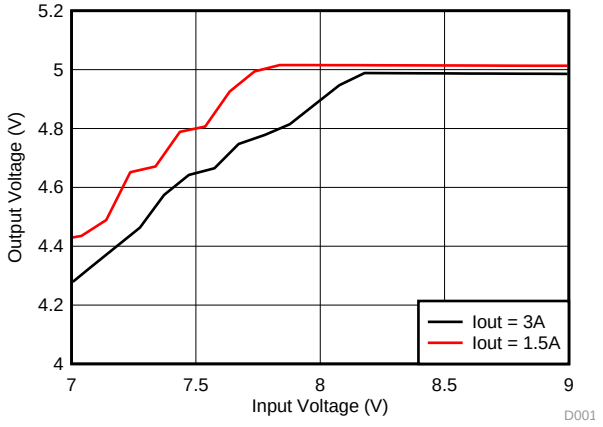
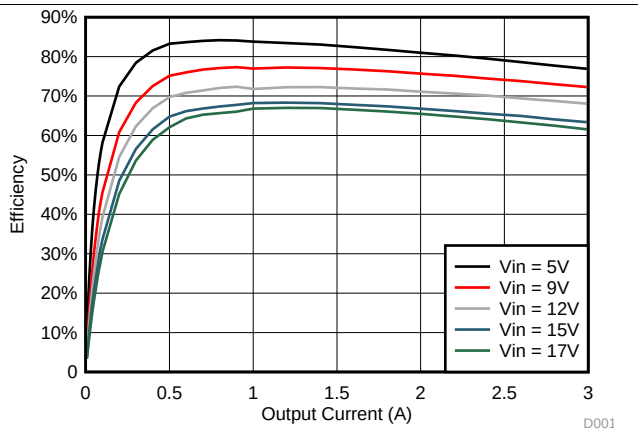
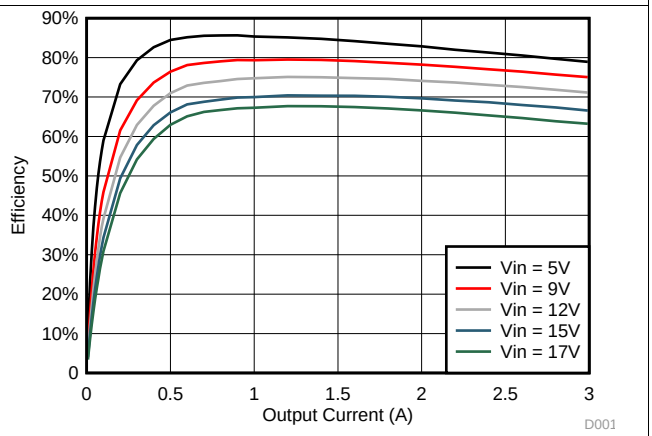


図 8. Dropout for 5 V Output Voltage



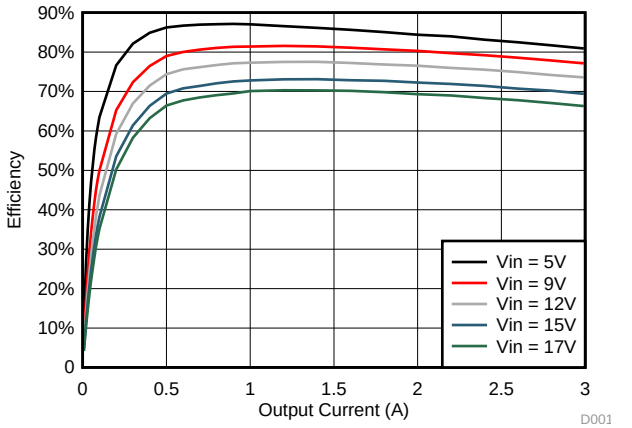
0.9 V Efficiency L = 0.56 µH (Wurth:744383560056)

図 9. Efficiency vs Output Current, V_{OUT} = 0.9 V



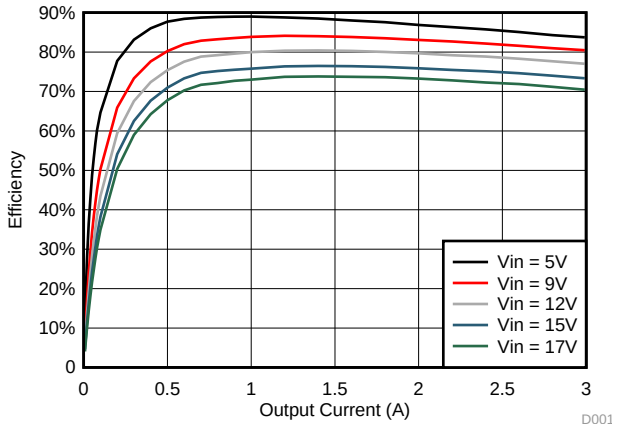
1.05 V Efficiency L = 0.56 µH (Wurth:744383560056)

図 10. Efficiency vs Output Current, V_{OUT} = 1.05 V



1.2 V Efficiency L = 0.68 µH (Wurth:744383560068)

図 11. Efficiency vs Output Current, V_{OUT} = 1.2 V

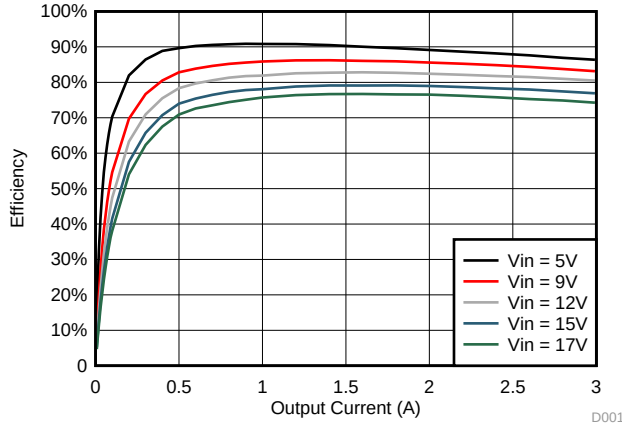


1.5 V Efficiency L = 0.68 µH (Wurth:744383560068)

図 12. Efficiency vs Output Current, V_{OUT} = 1.5 V

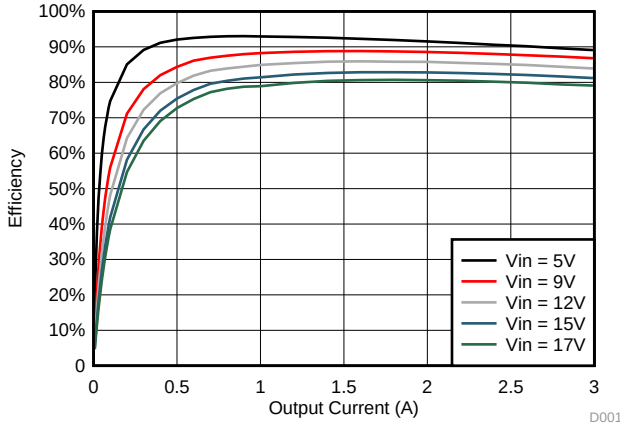
Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)



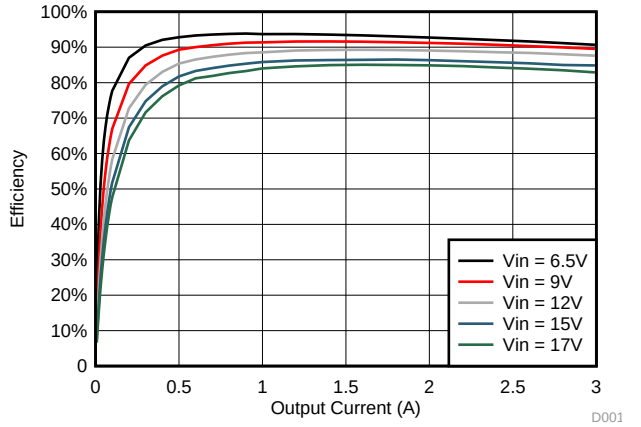
1.8 V Efficiency L = 1 µH (Wurth:744311100)

図 13. Efficiency vs Output Current, V_{OUT} = 1.8 V



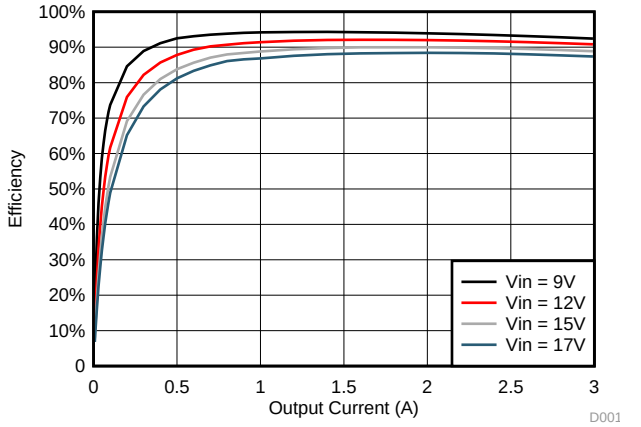
2.5 V Efficiency L = 1 µH (Wurth:744311100)

図 14. Efficiency vs Output Current, V_{OUT}= 2.5 V



3.3 V Efficiency L = 1.5 µH (Wurth:744311150)

図 15. Efficiency vs Output Current, V_{OUT}= 3.3 V



5 V Efficiency L = 1.5 µH (Wurth:744311150)

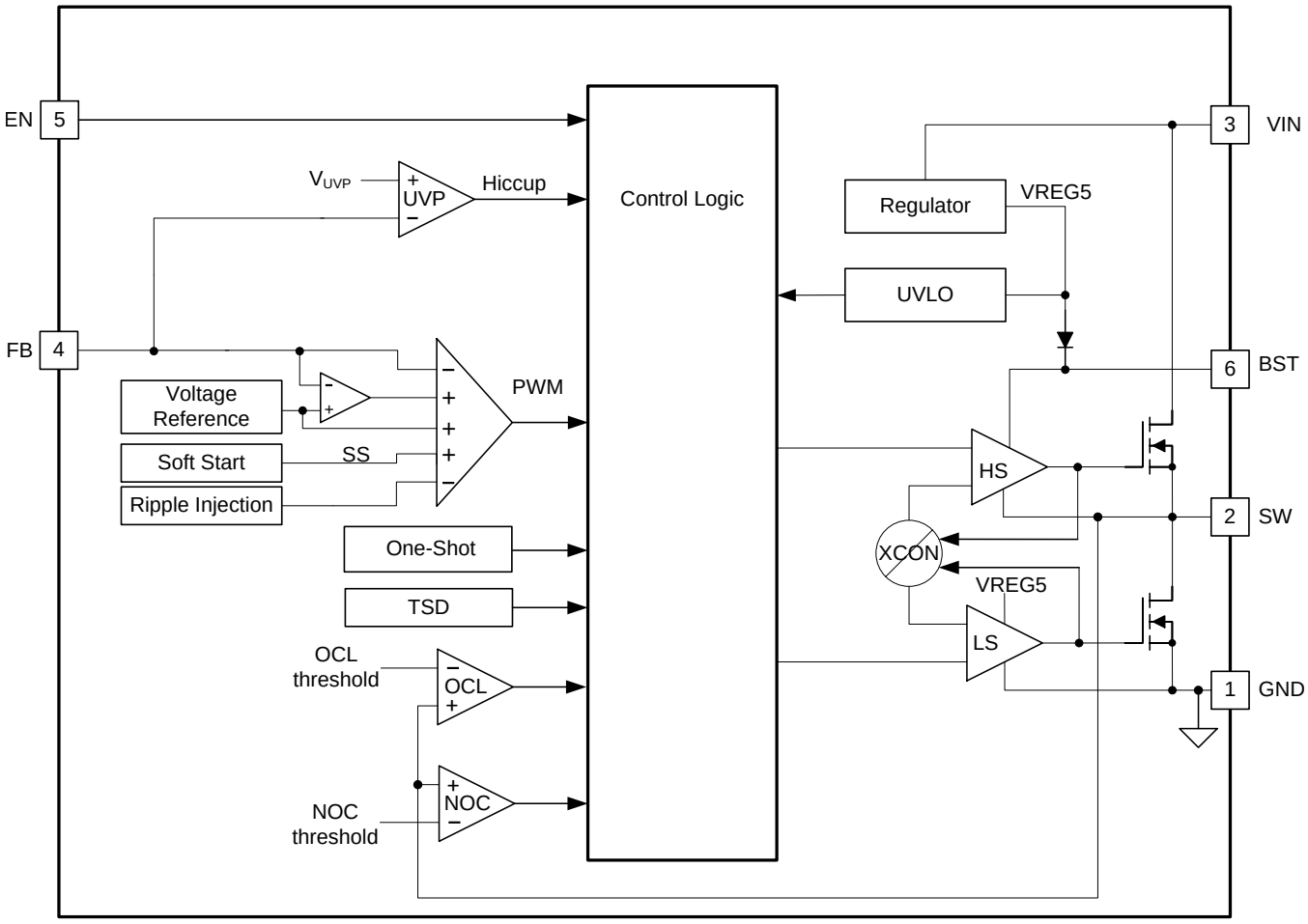
図 16. Efficiency vs Output Current, V_{OUT} = 5 V

7 Detailed Description

7.1 Overview

The TPS563249 is a 3-A synchronous step-down converter. The proprietary D-CAP3 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP3 mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS563249 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 mode control. The D-CAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, VIN, and inversely proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3 mode control.

Feature Description (continued)

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS563249 has an internal 1.7-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.3 Current Protection

There are three kinds of current protection in TPS563249: High-side FET source current limit, low-side FET source current limit, and low-side FET sink current limit.

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the low-side FET switch, the inductor current flow through low-side FET and decreases linearly. The average value of the inductor current is the load current I_{OUT}. If the monitored current is above the low-side FET source current limit level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current cross the low-side FET source current limit level. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 0.36 ms) and re-start after the hiccup time (typically 25 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

During the on time of the high-side FET switch, the inductor current flow through high-side FET and increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. The switch current is compared with high-side FET source current limit after a short blanking time. If the cross-limit event detected before the one shot timer expires, the high-side FET is turn off immediately, and is not allowed on in the following 1 µS period.

TPS563249 works in Forced Continuous Conduction Mode (FCCM). To support light load operation, the current flowing through low-side FET is allowed to be negative, which means the current flow from drain to source of low-side FET. This negative current is compared with low-side FET sink current limit to prevent device from being over-current damaged. Once the sink current cross limit, the low-side FET is turn off immediately. Both high-side FET and low-side FET will keep off until the VFB voltage falls below reference voltage.

7.3.4 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.5 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the thermal shutdown threshold value (typically 160°C), the device will shut off. This is a non-latch protection. The device will resume normal working once the temperature return below the recovery threshold value (typically 135°C).

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS563249 can operate in the continuous conduction mode (CCM) at a fixed frequency of 1.4 MHz. If EN pin is driven by a control signal, the required power on sequence is that applying input voltage at VIN pin firstly, then pull EN pin high. Be sure that the EN pin voltage isn't higher than VIN pin voltage. If EN pin is not used, it can be tied to VIN pin directly.

7.4.2 Standby Operation

TPS563249 can be placed in standby by asserting the EN pin low.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical step-down DC-DC converter. It is typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the TPS563249. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in 図 17 was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

図 17 shows the TPS563249 6.5-V to 17-V input, 3.3-V output converter schematic.

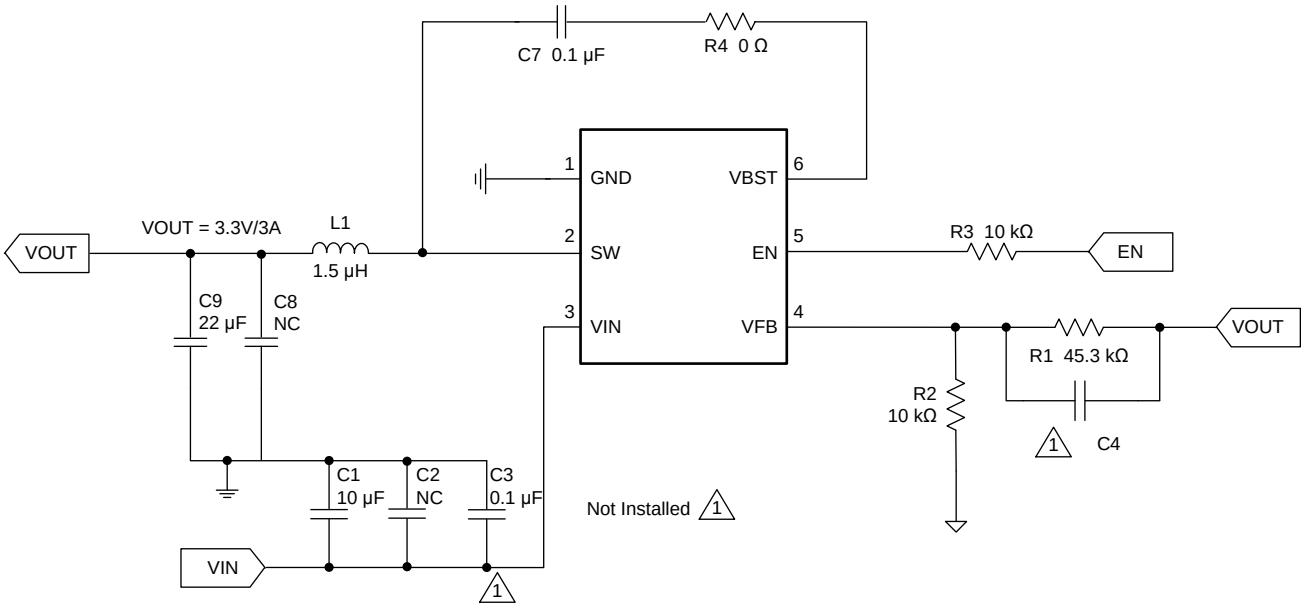


図 17. 3.3-V/3-A Reference Design

Typical Application (continued)

8.2.1 Design Requirements

表 1 shows the design parameters for this application.

表 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	6.5 to 17 V
Output voltage	3.3 V
Transient response, 1.5-A load step	ΔV_{OUT} = ±5%
Input ripple voltage	400 mV
Output ripple voltage	100 mV
Output current rating	3 A
Operating frequency	1.4 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 1 to calculate V_{OUT}.

Too high of resistance is more susceptible to noise, and voltage errors from the VFB input current is more noticeable.

$$V_{OUT} = 0.6 \times (1 + \frac{R1}{R2}) \quad (1)$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (2)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP3 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 2 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 2.

表 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	6.65	10.0	0.33	0.56	1	10 to 44
1.05	7.5	10.0	0.33	0.56	1	10 to 44
1.2	10	10.0	0.47	0.68	1.5	10 to 44
1.5	15	10.0	0.47	0.82	1.5	10 to 44
1.8	20	10.0	0.56	1	2.2	10 to 44
2.5	31.6	10.0	0.68	1	2.2	10 to 44
3.3	45.3	10.0	0.82	1.5	3.3	10 to 44
5	73.2	10.0	1	1.5	3.3	10 to 44
6.5	97.6	10.0	1	1.5	3.3	10 to 44

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 3, 式 4, and 式 5. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (3)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (4)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (5)$$

For this design example, the calculated peak current is 3.63 A and the calculated RMS current is 3.02 A. The inductor used is a WE 744311150 with a rated current of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563249 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 10 µF to 44 µF. Use 式 6 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (6)$$

For this design one Murata GRM31CR61A226KE19 22-µF output capacitor is used. The typical ESR is 2 mΩ. The calculated RMS current is 0.365 A and output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS563249 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.2.5 Dropout

With a constant 1.4-MHz switching frequency, there is a minimum input voltage limit for a given output voltage to be regulated. This is due to the minimum off time limit. If the input voltage less than the minimum input voltage limit, the output voltage drops accordingly, which is called dropout condition. 図 7 and 図 8 show the typical dropout curve for 3.3 V and 5 V output voltage with 3 A and 1.5 A load respectively. 式 7 can be used to estimate this minimum input voltage limit.

$$V_{IN(MIN)} = \frac{\frac{V_{OUT}}{F_{SW}} + (R_{dsl} + R_L) \times I_O \times (t_{off\,(min)} - t_{d1} - t_{d2}) + (V_d + R_L \times I_O) \times (t_{d1} + t_{d2})}{\frac{1}{F_{SW}} - t_{off\,(min)}} + (R_{dsh} + R_L) \times I_O \quad (7)$$

where

- V_{OUT} = target output voltage
- F_{SW} = maximum switching frequency including tolerance
- $t_{off(min)}$ = minimum off time including tolerance
- R_{dsl} = low side FET on resistance
- R_{dsh} = high side FET on resistance
- R_L = inductor DC resistance
- I_O = maximum load current
- t_{d1} = dead time between high side FET off and low side FET on, 15nS typical
- t_{d2} = dead time between low side FET off and high side FET on, 10nS typical
- V_d = forward voltage of low side FET body diode

8.2.3 Application Curves

T_A = 25°C, V_{IN} = 12 V (unless otherwise noted)

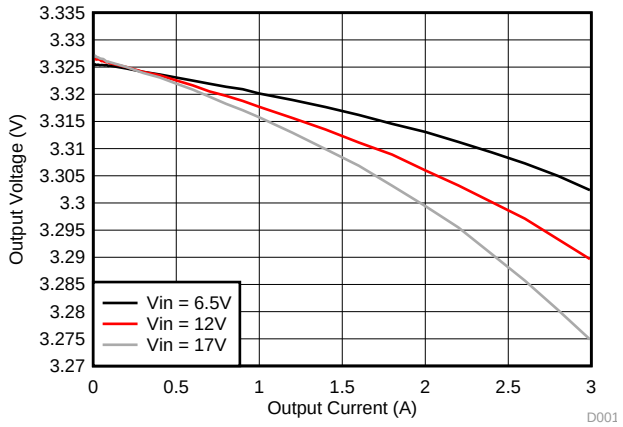


図 18. Load Regulation

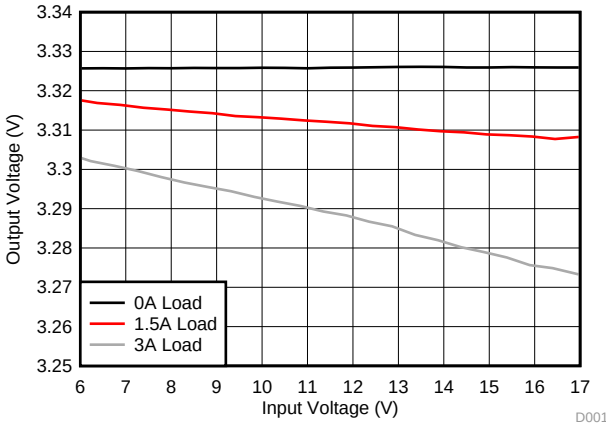


図 19. Line Regulation

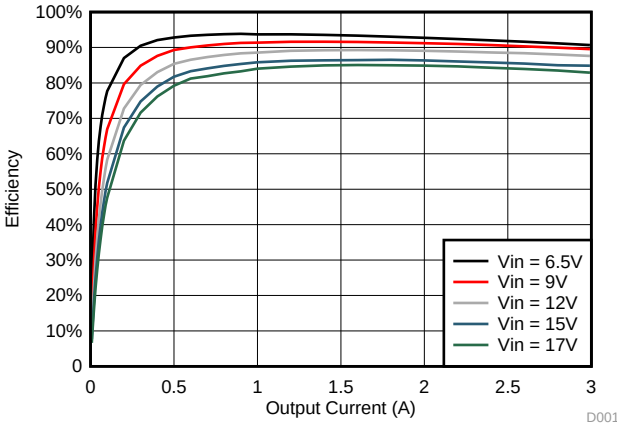
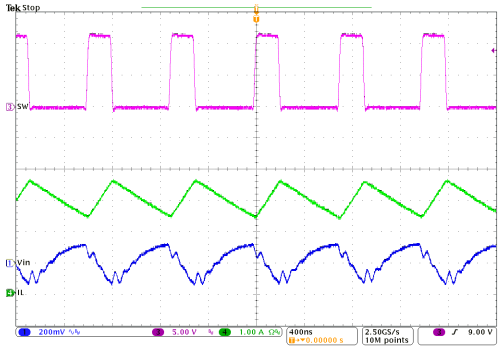
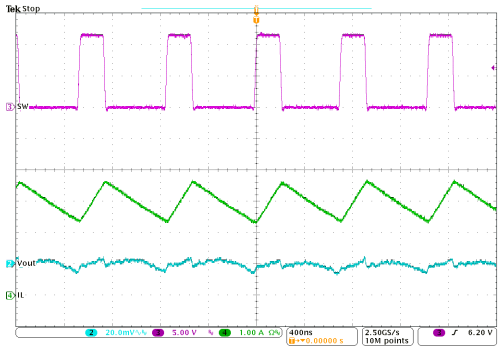


図 20. Efficiency



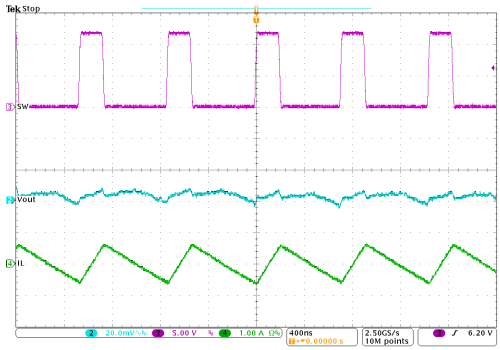
I_{out} = 3 A

図 21. Input Voltage Ripple



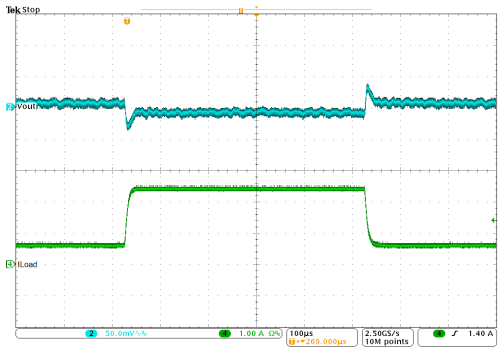
I_{out} = 3 A

図 22. Output Voltage Ripple



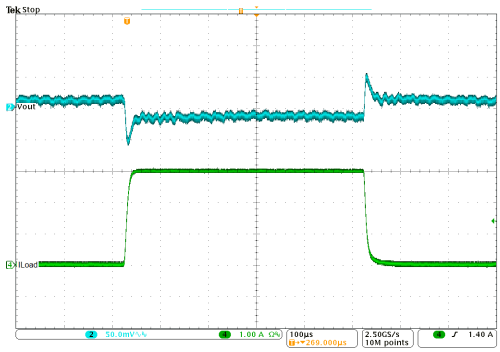
I_{OUT} = 0 A

図 23. Output Voltage Ripple



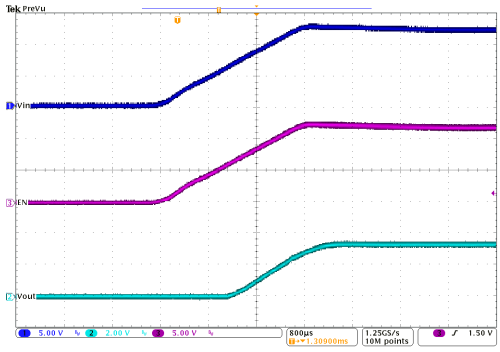
Slew rate is 1.6 A/µS

図 24. Transient Response, 0.6 to 2.4 A



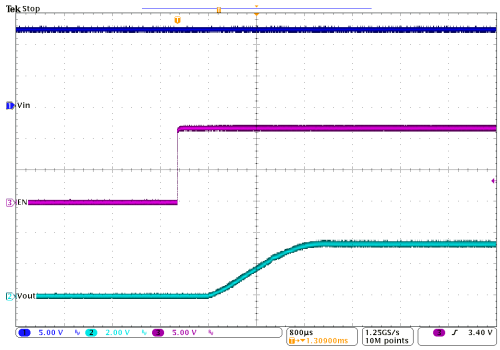
Slew rate is 1.6 A/µS

図 25. Transient Response, 0 to 3 A



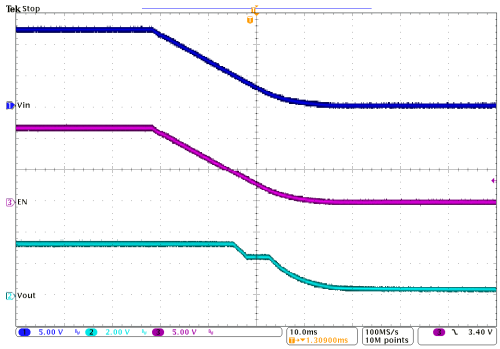
I_{OUT} = 0 A

図 26. Start Up Relative to V_{IN}



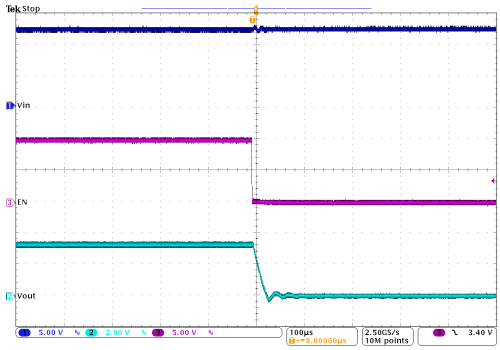
I_{OUT} = 3 A

図 27. Start-Up Relative to EN



I_{OUT} = 0 A

図 28. Shutdown Relative to V_{IN}



I_{OUT} = 3 A

図 29. Shutdown Relative to EN

9 Power Supply Recommendations

TPS563249 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not suggest routing SW copper under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

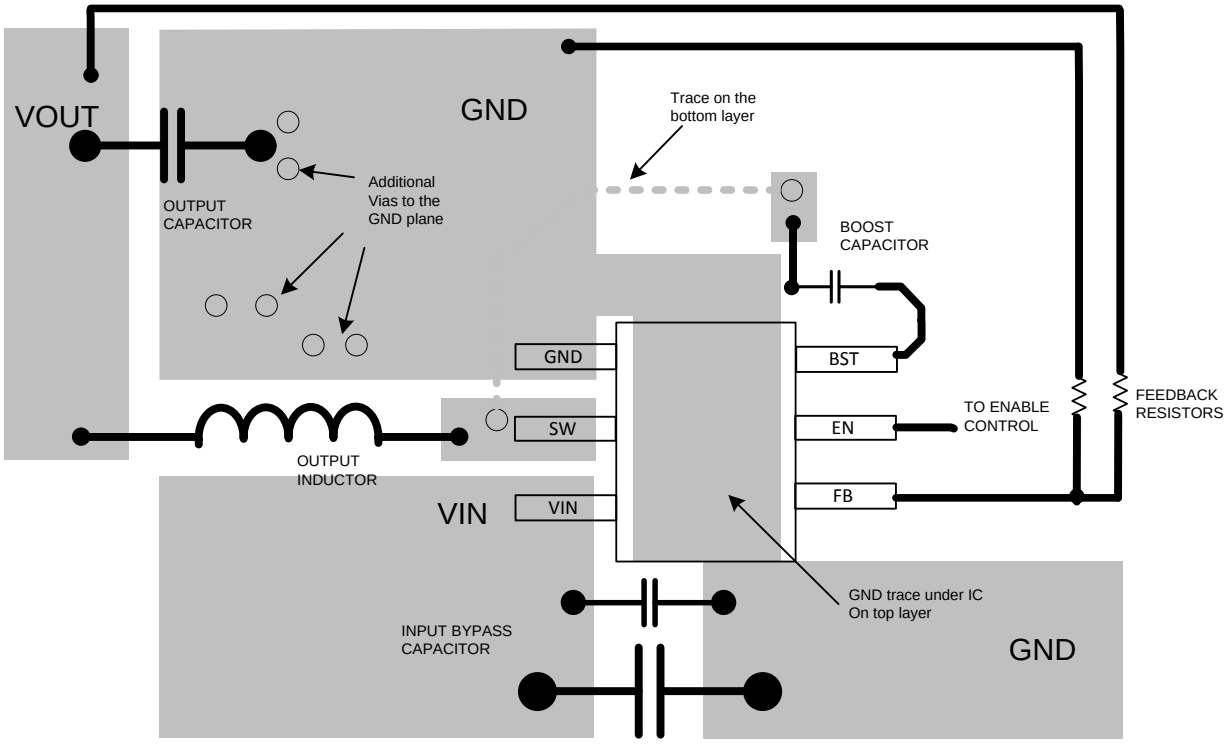


図 30. Example Layout

11 デバイスおよびドキュメントのサポート

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS563249DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	249	Samples
TPS563249DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	249	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

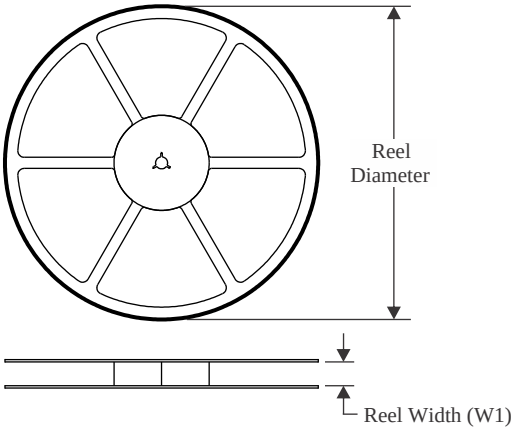
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

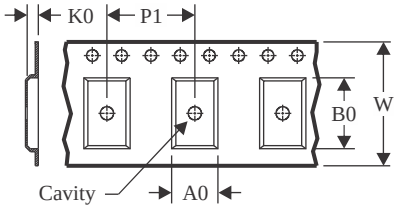
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

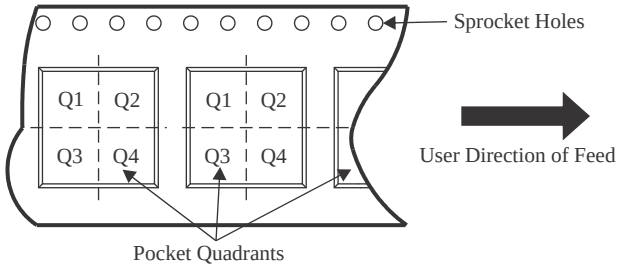


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

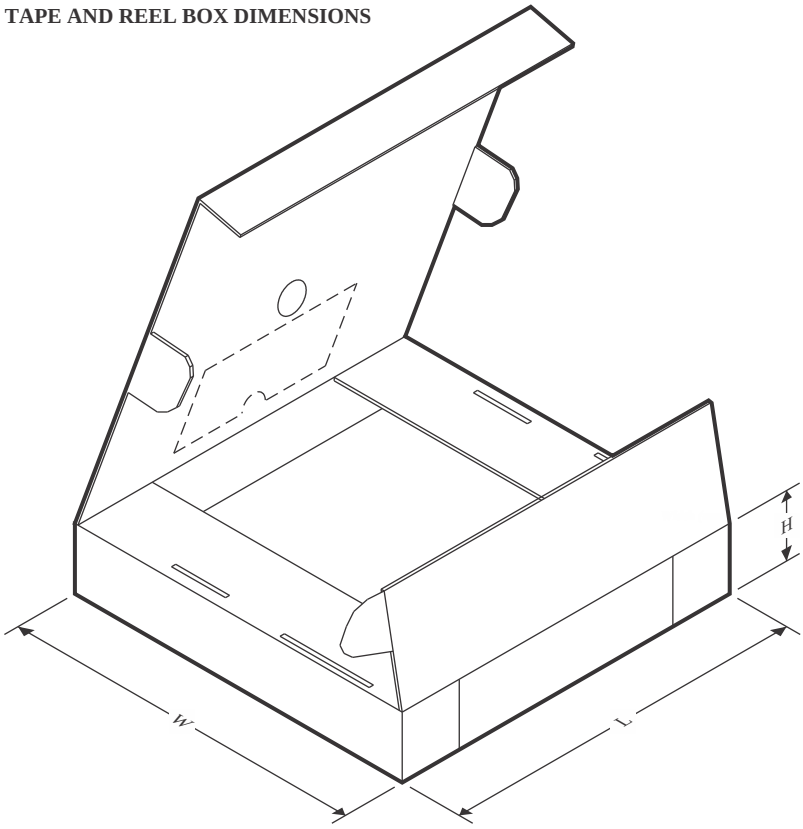
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS563249DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563249DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563249DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

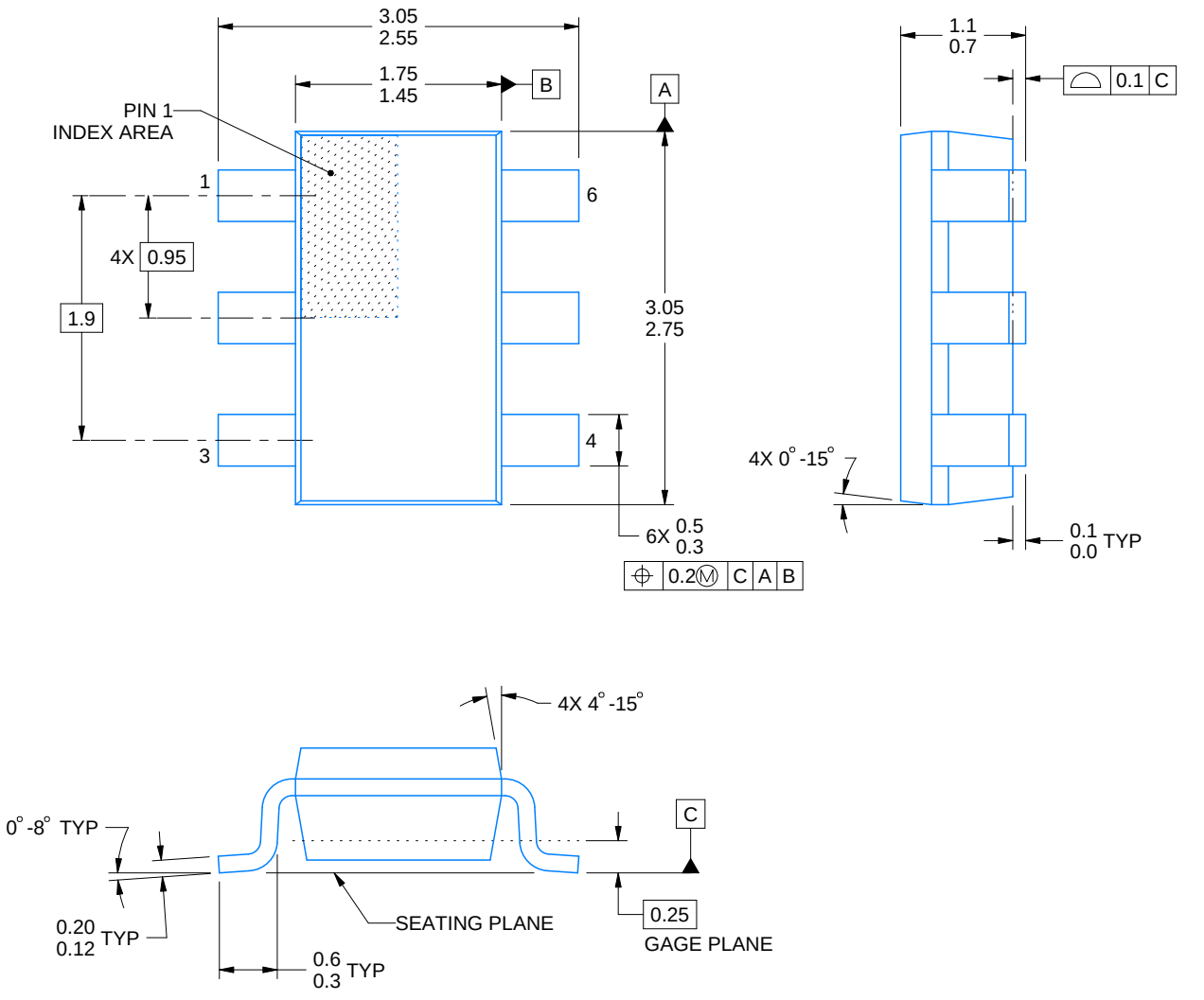
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS563249DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563249DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
TPS563249DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

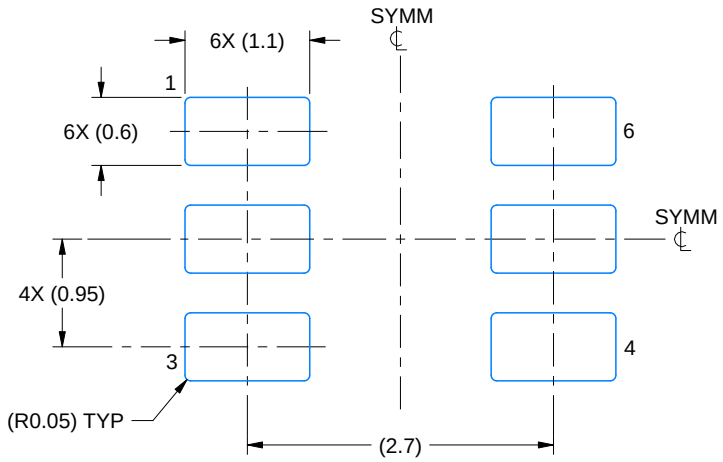
SMALL OUTLINE TRANSISTOR



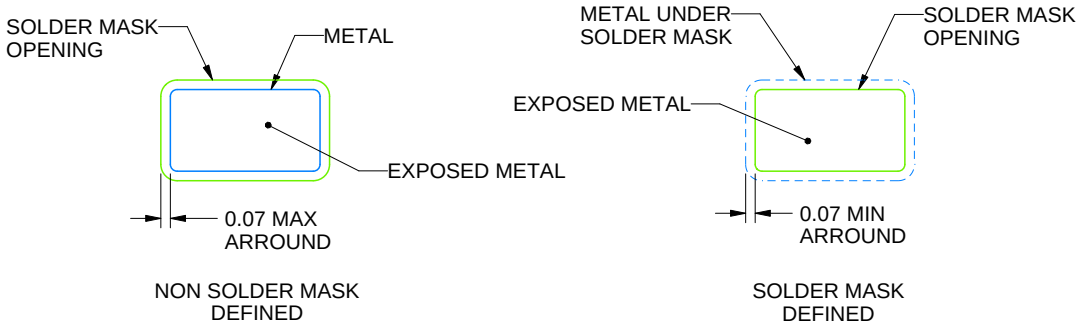
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

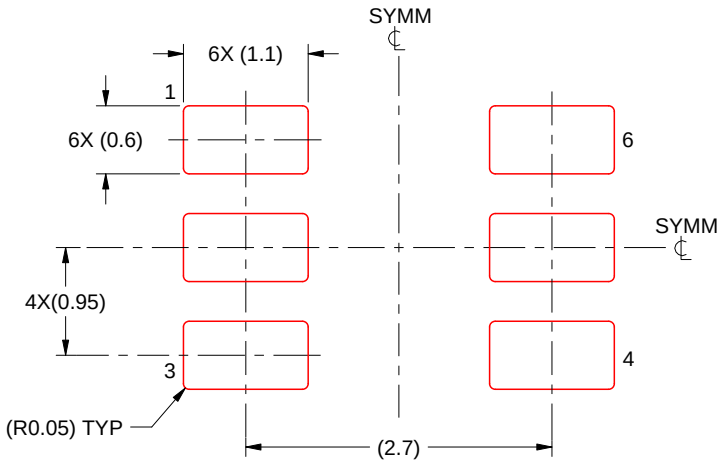


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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