

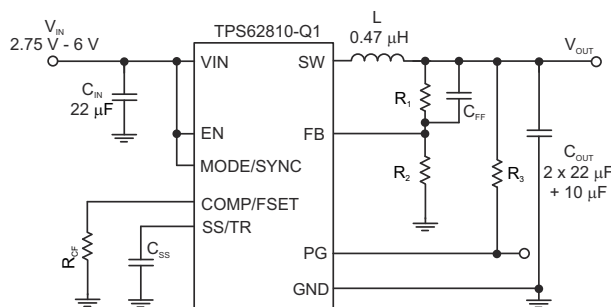
## TPS6281x-Q1 2.75V~6V 可変周波数降圧コンバータ

### 1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - デバイス温度グレード 1:
    - 40°C~+125°C, T<sub>A</sub>
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 入力電圧範囲: 2.75V~6V
- 1A, 2A, 3A, 4A のファミリー
- 静止電流: 15μA (代表値)
- 出力電圧: 0.6V~5.5V
- 出力電圧精度 ±1% (PWM 動作)
- 調整可能なソフト・スタート
- 強制 PWM または PWM/PFM 動作
- 1.8MHz~4MHz の調整可能なスイッチング周波数
- 高精度の ENABLE 入力
  - ユーザー定義の低電圧誤動作防止機能
  - 正確なシーケンシング
- 100% デューティ・サイクル・モード
- アクティブ出力放電
- 拡散スペクトラム・クロック処理 - オプション
- ウィンドウ・コンパレータを使用したパワー・グッド出力
- ウェットプル・フランク付きパッケージ

### 2 アプリケーション

- インフォテインメント用ヘッド・ユニット
- ハイブリッドおよび再構成可能クラス
- テレマティクス制御ユニット
- サラウンド・ビュー ECU、ADAS センサ・フュージョン
- 外部アンプ



簡略回路図

### 3 概要

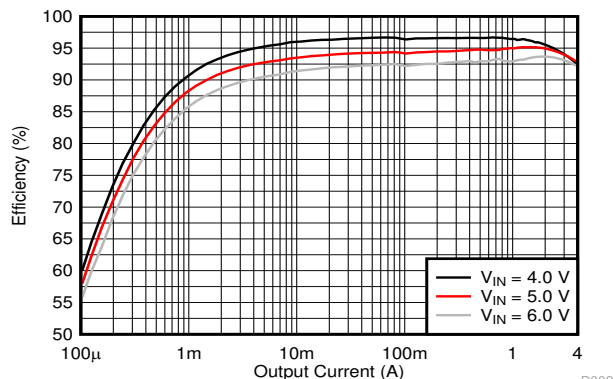
TPS6281x-Q1 はピン互換の 1A、2A、3A、4A の同期整流式降圧 DC/DC コンバータのファミリーです。すべてのデバイスは、高い効率と使いやすさを特長としています。TPS6281x-Q1 ファミリーは、ピーク電流モード制御方式に基づいています。TPS6281x-Q1 は、インフォテインメント、先進運転支援システムなどの車載アプリケーション用に設計されています。低抵抗のスイッチにより、高い周囲温度でも最大 4A の連続出力電流を供給できます。スイッチング周波数は 1.8MHz~4MHz の範囲で外部から変更でき、同じ周波数範囲の外部クロックと同期することもできます。PWM/PFM モードでは、TPS6281x-Q1 は負荷が軽いときに自動的にパワーセーブ・モードへ移行するため、負荷範囲全体にわたって高い効率が維持されます。TPS6281x-Q1 は PWM モードで 1% の出力電圧精度を実現するため、出力電圧精度の高い電源の設計に役立ちます。SS/TR ピンを使用して、スタートアップ時間を設定したり、出力電圧が外部ソースに追従するよう設定したりできます。この特長によって、各種の電源レールの外部シーケンシングが可能で、スタートアップ時の突入電流が制限されます。

TPS6281x-Q1 は 3mm × 2mm の VQFN パッケージで供給されます (ウェットプル・フランク付き)

#### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
TPS62810-Q1	RWY (VQFN, 9)	3.00mm × 2.00mm
TPS62811-Q1		
TPS62812-Q1		
TPS62813-Q1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流との関係、V<sub>OUT</sub> = 3.3V、PWM/PFM、f<sub>s</sub> = 2.25MHz



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision I (December 2021) to Revision J (March 2023)</b>	<b>Page</b>
• Added planned device spins to <i>Device Comparison Table</i> .....	3
<b>Changes from Revision H (April 2021) to Revision I (December 2021)</b>	<b>Page</b>
• Added planned device spins to <i>Device Comparison Table</i> .....	3
• Added feedback voltage for fixed voltage version TPS628122A, TPS6281006.....	6
<b>Changes from Revision G (March 2021) to Revision H (April 2021)</b>	<b>Page</b>
• Added device version to <i>Device Comparison Table</i> .....	3

## 5 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	Vout DISCHARGE	FOLDBACK CURRENT LIMIT	SPREAD SPECTRUM CLOCKING (SSC)	OUTPUT VOLTAGE
TPS62811QWRWYRQ1	1 A	ON	OFF	OFF	adjustable
TPS6281120QWRWYRQ1	1 A	ON	OFF	ON	adjustable
TPS6281126QWRWYRQ1	1 A	ON	OFF	ON	fixed 1.0 V
TPS6281109QWRWYRQ1	1 A	ON	OFF	OFF	fixed 1.15 V
TPS628110AQWRWYRQ1	1 A	ON	OFF	OFF	fixed 1.2 V
TPS628112AQWRWYRQ1	1 A	ON	OFF	ON	fixed 1.2 V
TPS628112MQWRWYRQ1	1 A	ON	OFF	ON	fixed 1.8 V
TPS628113HQWRWYRQ1	1 A	ON	OFF	ON	fixed 3.3 V
TPS62812QWRWYRQ1	2 A	ON	OFF	OFF	adjustable
TPS6281220QWRWYRQ1	2 A	ON	OFF	ON	adjustable
TPS6281240QWRWYRQ1	2 A	OFF	OFF	ON	adjustable
TPS6281206QWRWYRQ1	2 A	ON	OFF	OFF	fixed 1.0 V
TPS6281208QWRWYRQ1	2 A	ON	OFF	OFF	fixed 1.1 V
TPS6281228QWRWYRQ1	2 A	ON	OFF	ON	fixed 1.1 V
TPS628122AQWRWYRQ1	2A	ON	OFF	ON	fixed 1.2 V
TPS628122GQWRWYRQ1	2 A	ON	OFF	ON	fixed 1.5 V
TPS628120MQWRWYRQ1	2 A	ON	OFF	OFF	fixed 1.8 V
TPS62813QWRWYRQ1	3 A	ON	OFF	OFF	adjustable
TPS6281320QWRWYRQ1	3 A	ON	OFF	ON	adjustable
TPS6281326QWRWYRQ1	3 A	ON	OFF	ON	fixed 1.0 V
TPS628132DQWRWYRQ1	3 A	ON	OFF	ON	fixed 1.35 V
TPS628132MQWRWYRQ1	3 A	ON	OFF	ON	fixed 1.8 V
TPS628130AQWRWYRQ1	3 A	ON	OFF	OFF	fixed 1.2 V
TPS6281302QWRWYRQ1	3 A	ON	OFF	OFF	fixed 0.8 V
TPS62810QWRWYRQ1	4 A	ON	OFF	OFF	adjustable
TPS6281020QWRWYRQ1	4 A	ON	OFF	ON	adjustable
TPS6281006QWRWYRQ1	4A	ON	OFF	OFF	fixed 1.0 V
TPS6281008QWRWYRQ1	4 A	ON	OFF	OFF	fixed 1.1 V
TPS628100MQWRWYRQ1	4 A	ON	OFF	OFF	fixed 1.8 V

## 6 Pin Configuration and Functions

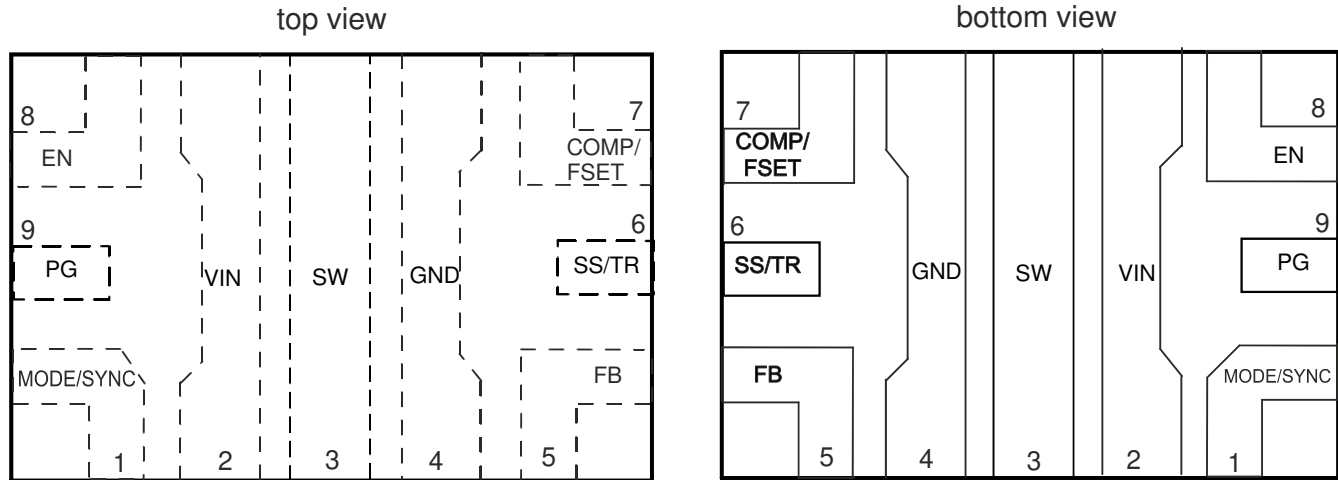


图 6-1. RWY Package 9 Pin (VQFN)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	5	I	Voltage feedback input, connect the resistive output voltage divider to this pin. For the fixed voltage versions, connect the FB pin directly to the output voltage.
GND	4		Ground pin
MODE/SYNC	1	I	The device runs in PFM/PWM mode when this pin is pulled low. If the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See the <a href="#">セクション 7</a> for the detailed specification of the digital signal applied to this pin for external synchronization.
COMP/FSET	7	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. If the pin is tied to GND or VIN, the switching frequency is set to 2.25 MHz. Do not leave this pin unconnected.
PG	9	O	Open drain power good output. Low impedance when not "power good", high impedance when "power good". This pin can be left open or be tied to GND when not used.
SS/TR	6	I	Soft-Start / Tracking pin. A capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing - see the <a href="#">Soft Start / Tracking (SS/TR)</a> section.
SW	3		This pin is the switch pin of the converter and is connected to the internal Power MOSFETs.
VIN	2		Power supply input. Connect the input capacitor as close as possible between pin VIN and GND.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage range <sup>(1)</sup>	VIN	-0.3	6.5	V
	SW	-0.3	V <sub>IN</sub> +0.3	V
	SW (transient for less than 10 ns) <sup>(2)</sup>	-3	10	V
	FB	-0.3	4	V
	PG, SS/TR, COMP/FSET	-0.3	V <sub>IN</sub> +0.3	V
Pin voltage range <sup>(1)</sup>	EN, MODE/SYNC	-0.3	6.5	V
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) While switching

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Supply voltage range	2.75		6	V
V <sub>OUT</sub>	Output voltage range	0.6		5.5	V
L	Effective inductance for a switching frequency of 1.8 MHz to 3.5 MHz	0.32	0.47	0.9	μH
L	Effective inductance for a switching frequency of 3.5 MHz to 4 MHz	0.25	0.33	0.9	μH
C <sub>OUT</sub>	Effective output capacitance for 1A and 2A version <sup>(1)</sup>	15	22	470	μF
C <sub>OUT</sub>	Effective output capacitance for 3A and 4A version <sup>(1)</sup>	27	47	470	μF
C <sub>IN</sub>	Effective input capacitance <sup>(1)</sup>	5	10		μF
R <sub>CF</sub>		4.5		100	kΩ
T <sub>J</sub>	Operating junction temperature	-40		+150	°C

- (1) The values given for the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer's DC bias curves for the effective capacitance vs DC voltage applied. Further restrictions may apply. Please see the feature description for COMP/FSET about the output capacitance vs compensation setting and output voltage.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS6281x-Q1	UNIT
		RWY	
		9 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	71.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	37.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	16.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	16.1	°C/W

## 7.4 Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>		TPS6281x-Q1	UNIT
		RWY	
		9 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

over operating junction temperature ( $T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ) and  $V_{IN} = 2.75\text{ V}$  to  $6\text{ V}$ . Typical values at  $V_{IN} = 5\text{ V}$  and  $T_J = 25\text{ °C}$ . (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_Q$	Operating Quiescent Current	EN = high, $I_{OUT} = 0\text{ mA}$ , Device not switching, $T_J = 125\text{ °C}$			21	$\mu\text{A}$
$I_Q$	Operating Quiescent Current	EN = high, $I_{OUT} = 0\text{ mA}$ , Device not switching		15	30	$\mu\text{A}$
$I_{SD}$	Shutdown Current	EN = 0 V, at $T_J = 125\text{ °C}$			18	$\mu\text{A}$
$I_{SD}$	Shutdown Current	EN = 0 V, Nominal value at $T_J = 25\text{ °C}$ , Max value at $T_J = 150\text{ °C}$		1.5	26	$\mu\text{A}$
$V_{UVLO}$	Undervoltage Lockout Threshold	Rising Input Voltage	2.5	2.6	2.75	V
		Falling Input Voltage	2.25	2.5	2.6	V
$T_{SD}$	Thermal Shutdown Temperature	Rising Junction Temperature		170		°C
	Thermal Shutdown Hysteresis			15		
<b>CONTROL (EN, SS/TR, PG, MODE/SYNC)</b>						
$V_{IH}$	High Level Input Voltage for MODE/SYNC Pin		1.1			V
$V_{IL}$	Low Level Input Voltage for MODE/SYNC Pin				0.3	V
$f_{SYNC}$	Frequency Range on MODE/SYNC Pin for Synchronization	requires a resistor from COMP/FSET to GND, see application section	1.8		4	MHz
	Duty Cycle of Synchronization Signal at MODE/SYNC Pin		20%	50%	80%	
	Time to Lock to External Frequency			50		$\mu\text{s}$
$V_{IH}$	Input Threshold Voltage for EN pin; Rising Edge		1.06	1.1	1.15	V
$V_{IL}$	Input Threshold Voltage for EN pin; Falling Edge		0.96	1.0	1.05	V
$I_{LKG}$	Input Leakage Current for EN, MODE/SYNC	$V_{IH} = V_{IN}$ or $V_{IL} = \text{GND}$			150	nA
	Resistance from COMP/FSET to GND for Logic Low	internal frequency setting with $f = 2.25\text{ MHz}$	0		2.5	k $\Omega$
	voltage on COMP/FSET for logic high	internal frequency setting with $f = 2.25\text{ MHz}$		$V_{IN}$		V
$V_{TH\_PG}$	UVP Power Good Threshold Voltage; dc Level	Rising ( $\%V_{FB}$ )	92%	95%	98%	
	UVP Power Good Threshold Voltage; dc Level	Falling ( $\%V_{FB}$ )	87%	90%	93%	
	OVP Power Good Threshold; dc Level	Rising ( $\%V_{FB}$ )	107%	110%	113%	
	OVP Power Good Threshold; dc Level	Falling ( $\%V_{FB}$ )	104%	107%	111%	
	Power Good De-glitch Time	for a high level to low level transition on power good		40		$\mu\text{s}$
$V_{OL\_PG}$	Power Good Output Low Voltage	$I_{PG} = 2\text{ mA}$		0.07	0.3	V
$I_{LKG\_PG}$	Input Leakage Current (PG)	$V_{PG} = 5\text{ V}$			100	nA

## 7.5 Electrical Characteristics (continued)

over operating junction temperature ( $T_J = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ ) and  $V_{IN} = 2.75\text{ V}$  to  $6\text{ V}$ . Typical values at  $V_{IN} = 5\text{ V}$  and  $T_J = 25\text{ }^\circ\text{C}$ . (unless otherwise noted)

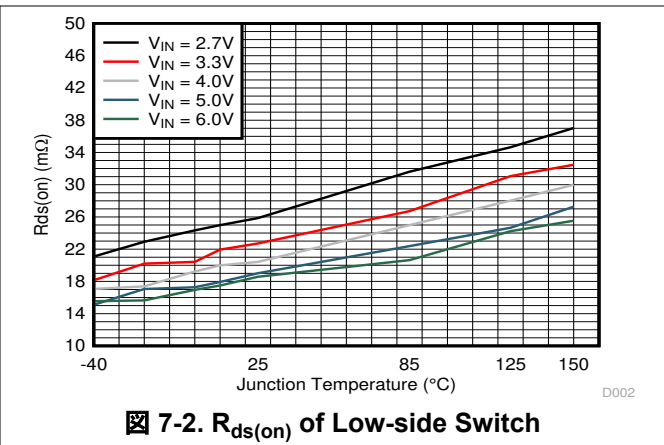
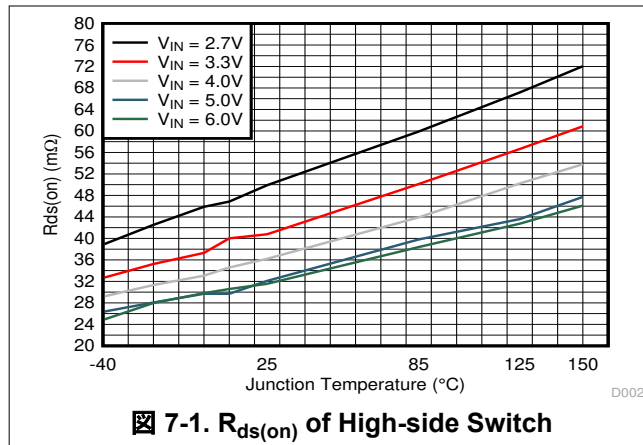
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SS/TR}$	SS/TR Pin Source Current		2.1	2.5	2.8	$\mu\text{A}$
	Tracking Gain	$V_{FB} / V_{SS/TR}$ for nominal $V_{FB} = 0.6\text{ V}$		1		
	Tracking Offset	feedback voltage with $V_{SS/TR} = 0\text{ V}$ for nominal $V_{FB} = 0.6\text{ V}$		17		mV
<b>POWER SWITCH</b>						
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	$V_{IN} \geq 5\text{ V}$		37	60	m $\Omega$
$R_{DS(ON)}$	Low-Side MOSFET ON-Resistance	$V_{IN} \geq 5\text{ V}$		15	35	m $\Omega$
	High-Side MOSFET leakage current	$V_{IN} = 6\text{ V}$ ; $V(\text{SW}) = 0\text{ V}$			30	$\mu\text{A}$
	Low-Side MOSFET leakage current	$V(\text{SW}) = 6\text{ V}$			55	$\mu\text{A}$
	SW leakage	$V(\text{SW}) = 0.6\text{ V}$ ; current into SW pin	-0.025		30	$\mu\text{A}$
$I_{LIMH}$	High-Side MOSFET Current Limit	dc value, for TPS62810; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	4.8	5.6	6.55	A
$I_{LIMH}$	High-Side MOSFET Current Limit	dc value, for TPS62813; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	3.9	4.5	5.25	A
$I_{LIMH}$	High-Side MOSFET Current Limit	dc value, for TPS62812; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	2.8	3.4	4.2	A
$I_{LIMH}$	High-Side MOSFET Current Limit	dc value, for TPS62811; $V_{IN} = 3\text{ V}$ to $6\text{ V}$	2.0	2.6	3.25	A
$I_{LIMNEG}$	Negative Valley Current Limit	dc value		-1.8		A
$f_s$	PWM Switching Frequency Range		1.8	2.25	4	MHz
$f_s$	PWM Switching Frequency	with COMP/FSET tied to $V_{IN}$ or GND	2.025	2.25	2.475	MHz
	PWM Switching Frequency Tolerance	using a resistor from COMP/FSET to GND, $f_s = 1.8\text{ MHz}$ to $4\text{ MHz}$	-19%		18%	
$t_{on,min}$	Minimum on-time of HS FET	$T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$ , $V_{IN} = 3.3\text{ V}$		50	75	ns
$t_{on,min}$	Minimum on-time of LS FET	$V_{IN} = 3.3\text{ V}$		30		ns
<b>OUTPUT</b>						
$V_{FB}$	Feedback Voltage	adjustable output voltage versions		0.6		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS6281302		0.8		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS6281206, TPS6281126, TPS6281326, TPS6281006		1.0		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS6281208, TPS6281008, TPS6281228		1.1		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS6281109		1.15		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS628110A, TPS628112A, TPS628122A, TPS628130A		1.2		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS628132D		1.35		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS628122G		1.5		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS628112M, TPS628120M, TPS628132D, TPS628100M, TPS628132M		1.8		V
$V_{FB}$	Feedback Voltage	fixed output voltage TPS628113H		3.3		V

## 7.5 Electrical Characteristics (continued)

over operating junction temperature ( $T_J = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ ) and  $V_{IN} = 2.75\text{ V}$  to  $6\text{ V}$ . Typical values at  $V_{IN} = 5\text{ V}$  and  $T_J = 25\text{ }^\circ\text{C}$ . (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{LKG\_FB}$	FB Input Leakage Current for Adjustable Voltage Versions	$V_{FB} = 0.6\text{ V}$		1	70	nA
$I_{LKG\_FB}$	FB Input Current for Fixed Voltage Versions	$V_{FB}$ voltage at target output voltage		1		$\mu\text{A}$
$V_{FB}$	Feedback Voltage Accuracy for Adjustable Voltage Versions	$V_{IN} \geq V_{OUT} + 1\text{ V}$		PWM mode	-1%	1%
$V_{FB}$	Feedback Voltage Accuracy for Fixed Voltage Versions	$V_{IN} \geq V_{OUT} + 1\text{ V}$		PWM mode, $T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	-1%	1%
$V_{FB}$	Feedback Voltage Accuracy for Fixed Voltage Versions	$V_{IN} \geq V_{OUT} + 1\text{ V}$		PWM mode	-1%	1.3%
$V_{FB}$	Feedback Voltage Accuracy	$V_{IN} \geq V_{OUT} + 1\text{ V};$ $V_{OUT} \geq 1.5\text{ V}$		PFM mode; $C_{o,eff} \geq 22\text{ }\mu\text{F},$ $L = 0.47\text{ }\mu\text{H}$	-1%	2%
$V_{FB}$	Feedback Voltage Accuracy	$1\text{ V} \leq V_{OUT} < 1.5\text{ V}$		PFM mode; $C_{o,eff} \geq 47\text{ }\mu\text{F},$ $L = 0.47\text{ }\mu\text{H}$	-1%	2.5%
$V_{FB}$	Feedback Voltage Accuracy with Voltage Tracking	$V_{IN} \geq V_{OUT} + 1\text{ V};$ $V_{SS/TR} = 0.3\text{ V}$		PWM mode	-1%	7%
	Load Regulation	PWM mode operation		0.05		%/A
	Line Regulation	PWM mode operation, $I_{OUT} = 1\text{ A}, V_{IN} \geq V_{OUT} + 1\text{ V}$		0.02		%/V
	Output Discharge Resistance				50	$\Omega$
$t_{delay}$	Start-up Delay Time	$I_{OUT} = 0\text{ mA}$ , Time from EN=high to start switching; $V_{IN}$ applied already	135	250	470	$\mu\text{s}$
$t_{ramp}$	Ramp time; SS/TR Pin Open	$I_{OUT} = 0\text{ mA}$ , Time from first switching pulse until 95% of nominal output voltage; device not in current limit	100	150	200	$\mu\text{s}$

## 7.6 Typical Characteristics





## 8 Parameter Measurement Information

### 8.1 Schematic

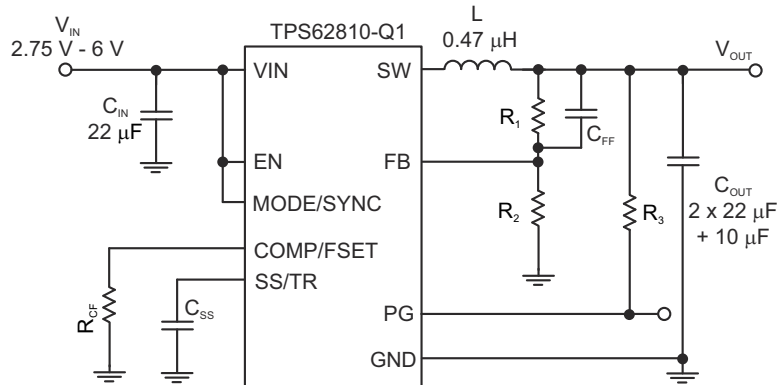


图 8-1. Measurement Setup for TPS62810-Q1 and TPS62813-Q1

表 8-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER <sup>(1)</sup>
IC	TPS62810-Q1 or TPS62813-Q1	Texas Instruments
L	0.47-μH inductor; XEL4030-471MEB	Coilcraft
C <sub>IN</sub>	22 μF / 10 V; GCM31CR71A226KE02L	Murata
C <sub>OUT</sub>	2 × 22 μF / 10 V; GCM31CR71A226KE02L + 1 × 10 μF 6.3 V; GCM188D70J106ME36	Murata
C <sub>SS</sub>	4.7 nF (equal to 1-ms start-up ramp)	Any
R <sub>CF</sub>	8.06 kΩ	Any
C <sub>FF</sub>	10 pF	Any
R <sub>1</sub>	Depending on V <sub>OUT</sub>	Any
R <sub>2</sub>	Depending on V <sub>OUT</sub>	Any
R <sub>3</sub>	100 kΩ	Any

(1) See the [Third-party Products Disclaimer](#).

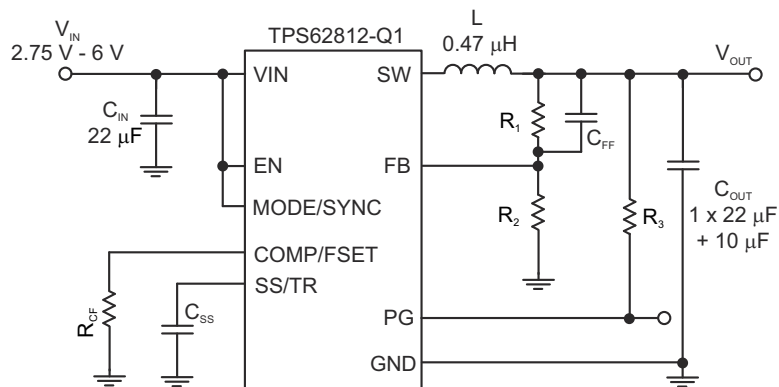


图 8-2. Measurement Setup for TPS62812-Q1 and TPS62811-Q1

**表 8-2. List of Components**

REFERENCE	DESCRIPTION	MANUFACTURER <sup>(1)</sup>
IC	TPS62812-Q1 or TPS62811-Q1	Texas Instruments
L	0.56- $\mu$ H inductor; XEL4020-561MEB	Coilcraft
C <sub>IN</sub>	22 $\mu$ F / 10 V; GCM31CR71A226KE02L	Murata
C <sub>OUT</sub>	1 $\times$ 22 $\mu$ F / 10 V; GCM31CR71A226KE02L + 1 $\times$ 10 $\mu$ F 6.3 V; GCM188D70J106ME36	Murata
C <sub>SS</sub>	4.7 nF (equal to 1-ms start-up ramp)	Any
R <sub>CF</sub>	8.06 k $\Omega$	Any
C <sub>FF</sub>	10 pF	Any
R <sub>1</sub>	Depending on V <sub>OUT</sub>	Any
R <sub>2</sub>	Depending on V <sub>OUT</sub>	Any
R <sub>3</sub>	100 k $\Omega$	Any

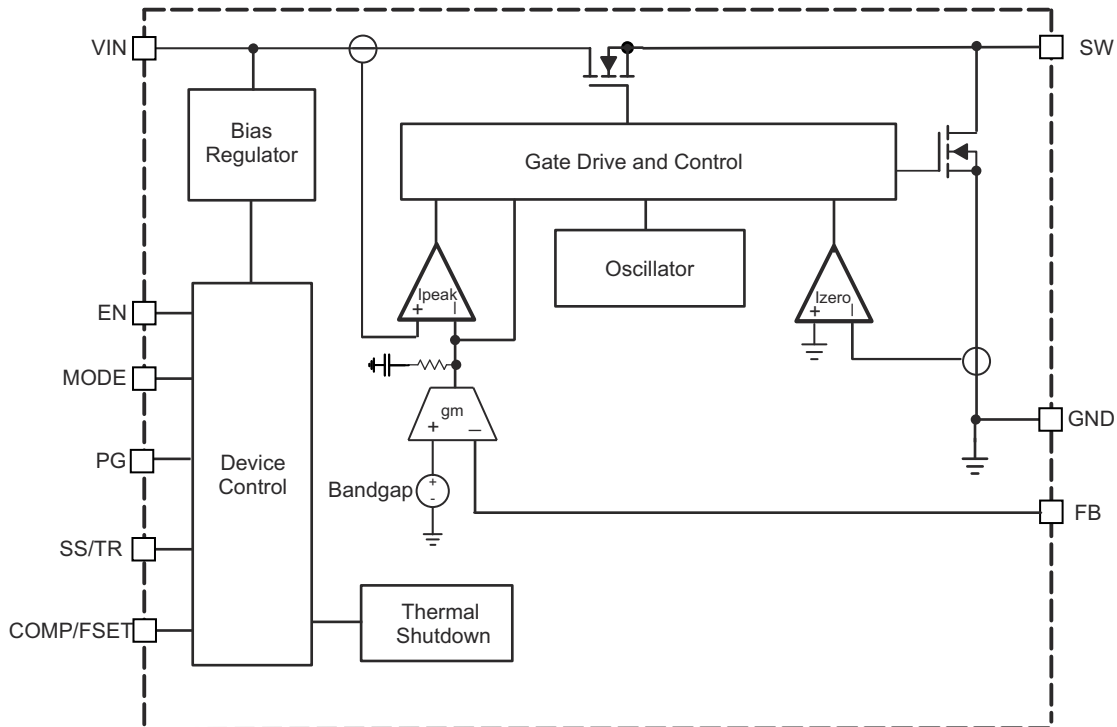
## 9 Detailed Description

### 9.1 Overview

The TPS6281x-Q1 synchronous switch mode DC/DC converters are based on a peak current mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with TPS6281x-Q1, one of three internal compensation settings can be selected. See [セクション 9.3.2](#). The compensation setting is selected either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low ESR ceramic output capacitors. The device can be operated without a feedforward capacitor on the output voltage divider, however, using a typically 10-pF feedforward capacitor improves transient response.

The devices support forced fixed frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as either 2.25 MHz internally fixed when COMP/FSET is tied to GND or VIN, or in a range of 1.8 MHz to 4 MHz defined by a resistor from COMP/FSET to GND. Alternatively, the devices can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. External synchronization is only possible if a resistor from COMP/FSET to GND is used. If COMP/FSET is directly tied to GND or VIN, the TPS6281x-Q1 cannot be synchronized externally. An internal PLL allows to change from internal clock to external clock during operation. The synchronization to the external clock is done on a falling edge of the clock applied at MODE to the rising edge on the SW pin. This allows a roughly 180° phase shift when the SW pin is used to generate the synchronization signal for a second converter. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current.

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Precise Enable

The voltage applied at the Enable pin of the TPS6281x-Q1 is compared to a fixed threshold of 1.1 V for a rising voltage. This allows to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS6281x-Q1 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 1  $\mu$ A. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

### 9.3.2 COMP/FSET

This pin allows to set two different parameters independently:

- Internal compensation settings for the control loop
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows you to adapt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency / compensation. Do not leave the pin floating.

The switching frequency has to be selected based on the input voltage and the output voltage to meet the specifications for the minimum on-time and minimum off-time.

For example:  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 1\text{ V}$  --> duty cycle (DC) =  $1\text{ V} / 5\text{ V} = 0.2$

- with  $t_{on} = DC \times T$  -->  $t_{on,min} = 1 / f_{s,max} \times DC$
- -->  $f_{s,max} = 1 / t_{on,min} \times DC = 1 / 0.075\ \mu\text{s} \cdot 0.2 = 2.67\text{ MHz}$

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in [表 9-1](#) and [表 9-2](#), up to the maximum of 470  $\mu$ F in all of the three compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1:

$$R_{CF}(k\Omega) = \frac{18\text{MHz} \cdot k\Omega}{f_s(\text{MHz})} \quad (1)$$

For compensation (comp) setting 2:

$$R_{CF}(k\Omega) = \frac{60MHz \cdot k\Omega}{f_s(MHz)} \quad (2)$$

For compensation (comp) setting 3:

$$R_{CF}(k\Omega) = \frac{180MHz \cdot k\Omega}{f_s(MHz)} \quad (3)$$

**表 9-1. Switching Frequency and Compensation for TPS62810-Q1 (4 A) and TPS62813-Q1 (3 A)**

COMPENSATION	R <sub>CF</sub>	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR V <sub>OUT</sub> < 1 V	MINIMUM OUTPUT CAPACITANCE FOR 1 V ≤ V <sub>OUT</sub> < 3.3 V	MINIMUM OUTPUT CAPACITANCE FOR V <sub>OUT</sub> ≥ 3.3 V
for smallest output capacitance (comp setting 1)	10 kΩ ... 4.5 kΩ	1.8 MHz (10 kΩ) ... 4 MHz (4.5 kΩ) according to 式 1	53 μF	32 μF	27 μF
for medium output capacitance (comp setting 2)	33 kΩ ... 15 kΩ	1.8 MHz (33 kΩ) ... 4 MHz (15 kΩ) according to 式 2	100 μF	60 μF	50 μF
for large output capacitance (comp setting 3)	100 kΩ ... 45 kΩ	1.8 MHz (100 kΩ) ... 4 MHz (45 kΩ) according to 式 3	200 μF	120 μF	100 μF
for smallest output capacitance (comp setting 1)	tied to GND	internally fixed 2.25 MHz	53 μF	32 μF	27 μF
for large output capacitance (comp setting 3)	tied to V <sub>IN</sub>	internally fixed 2.25 MHz	200 μF	120 μF	100 μF

**表 9-2. Switching Frequency and Compensation for TPS62812-Q1 (2 A) and TPS62811-Q1 (1 A)**

COMPENSATION	R <sub>CF</sub>	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR V <sub>OUT</sub> < 1 V	MINIMUM OUTPUT CAPACITANCE FOR 1 V ≤ V <sub>OUT</sub> < 3.3 V	MINIMUM OUTPUT CAPACITANCE FOR V <sub>OUT</sub> ≥ 3.3 V
for smallest output capacitance (comp setting 1)	10 kΩ ... 4.5 kΩ	1.8 MHz (10 kΩ) ... 4 MHz (4.5 kΩ) according to 式 1	30 μF	18 μF	15 μF
for medium output capacitance (comp setting 2)	33 kΩ ... 15 kΩ	1.8 MHz (33 kΩ) ... 4 MHz (15 kΩ) according to 式 2	60 μF	36 μF	30 μF
for large output capacitance (comp setting 3)	100 kΩ ... 45 kΩ	1.8MHz (100 kΩ) ...4 MHz (45 kΩ) according to 式 3	130 μF	80 μF	68 μF
for smallest output capacitance (comp setting 1)	tied to GND	internally fixed 2.25 MHz	30 μF	18 μF	15 μF
for large output capacitance (comp setting 3)	tied to V <sub>IN</sub>	internally fixed 2.25 MHz	130 μF	80 μF	68 μF

Refer to [セクション 10.1.3.2](#) for further details on the output capacitance required depending on the output voltage.

A too high resistor value for R<sub>CF</sub> is decoded as "tied to V<sub>IN</sub>", a value below the lowest range is decoded as "tied to GND". The minimum output capacitance in [表 9-1](#) and [表 9-2](#) is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required. All values are effective capacitance, including all tolerances, aging, dc bias effect, and so forth.

### 9.3.3 MODE / SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin allows to force PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. Similar to COMP/FSET, the specifications for the minimum on-time and minimum off-time have to be taken into account when setting the external frequency. For use with external synchronization on the MODE/SYNC pin, the internal switching frequency must be set by  $R_{CF}$  to a similar value than the externally applied clock. This ensures a fast settling to the external clock and, if the external clock fails, the switching frequency stays in the same range and the compensation settings are still valid. When there is no resistor from COMP/FSET to GND but the pin is pulled high or low, external synchronization is not possible.

### 9.3.4 Spread Spectrum Clocking (SSC)

For device versions with SSC enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized by applying a clock signal to the MODE/SYNC pin, the TPS6281x-Q1 follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

### 9.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

### 9.3.6 Power Good Output (PG)

Power good is an open-drain output driven by a window comparator. PG is held low when the device is disabled, in undervoltage lockout, and in thermal shutdown. When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

表 9-3. PG Status

EN	DEVICE STATUS	PG STATE
X	$V_{IN} < 2\text{ V}$	undefined
low	$V_{IN} \geq 2\text{ V}$	low
high	$2\text{ V} \leq V_{IN} \leq \text{UVLO}$ OR in thermal shutdown OR $V_{OUT}$ not in regulation	low
high	$V_{OUT}$ in regulation	high impedance

### 9.3.7 Thermal Shutdown

The junction temperature ( $T_J$ ) of the device is monitored by an internal temperature sensor. If  $T_J$  exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When  $T_J$  decreases by the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During a PFM pause, the thermal shutdown is not active. After a PFM pause, the device needs up to 9  $\mu\text{s}$  to detect a too high junction temperature. If the PFM burst is shorter than this delay, the device does not detect a too high junction temperature.

## 9.4 Device Functional Modes

### 9.4.1 Pulse Width Modulation (PWM) Operation

TPS6281x-Q1 has two operating modes: Forced PWM mode (discussed in this section) and PWM/PFM (discussed in [セクション 9.4.2](#)).

With the MODE/SYNC pin set to high, the TPS6281x-Q1 operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP pin to GND or by an external clock signal applied to the MODE/SYNC pin. With an external clock is applied to MODE/SYNC, the TPS6281x-Q1 follows the frequency applied to the pin. To maintain regulation, the frequency must be in a range the TPS6281x-Q1 can operate at, taking the minimum on-time into account.

#### 9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 1.2 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

#### 9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as  $D = V_{OUT} / V_{IN}$ . The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 30 ns is reached, the TPS6281x-Q1 skips switching cycles while it approaches 100% mode. In 100% mode, it keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low-side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

#### 9.4.4 Current Limit and Short Circuit Protection

The TPS6281x-Q1 is protected against overload and short circuit events. If the inductor current exceeds the current limit  $I_{LIMH}$ , the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low-side switch has decreased below the low-side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where

- $I_{LIMH}$  is the static current limit as specified in the electrical characteristics
- $L$  is the effective inductance at the peak current
- $V_L$  is the voltage across the inductor ( $V_{IN} - V_{OUT}$ )
- $t_{PD}$  is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50nS \quad (5)$$

#### 9.4.5 Foldback Current Limit and Short Circuit Protection

This is valid for devices where foldback current limit is enabled.

When the device detects current limit for more than 1024 subsequent switching cycles, it reduces the current limit from its nominal value to typically 1.8 A. Foldback current limit is left when the current limit indication goes away. For the case that device operation continues in current limit, it can, after 3072 switching cycles, try again full current limit for again 1024 switching cycles.

#### 9.4.6 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after TPS6281x-Q1 has been enabled at least once because the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V. Output discharge is not activated during a current limit or foldback current limit event.

### 9.4.7 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200  $\mu$ s then the internal reference and hence  $V_{OUT}$  rises with a slope controlled by an external capacitor connected to the SS/TR pin.

Leaving the SS/TR pin un-connected provides the fastest startup ramp with 150  $\mu$ s typically. A capacitor connected from SS/TR to GND is charged with 2.5  $\mu$ A by an internal current source during soft start until it reaches the reference voltage of 0.6 V. The capacitance required to set a certain ramp-time ( $t_{ramp}$ ) therefore is:

$$C_{SS} [nF] = \frac{2.5 \mu A \cdot t_{ramp} [ms]}{0.6V} \quad (6)$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND to ensure a proper low level. Returning from those states causes a new start-up sequence.

A voltage applied at SS/TR can be used to track a master voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. The SS/TR pin must not be connected to the SS/TR pin of other devices. An external voltage applied on SS/TR is internally clamped to the feedback voltage (0.6 V). TI recommends to set the target for the external voltage on SS/TR slightly above the feedback voltage. Given the tolerances of the resistor divider  $R_5$  and  $R_6$  on SS/TR, this ensures the device "switches" to the internal reference voltage when the power-up sequencing is finished. See [10-58](#).



## 10 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 10.1 Application Information

#### 10.1.1 Programming the Output Voltage

The output voltage of the TPS6281x-Q1 is adjustable. The output voltage can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from 式 7. TI recommends to choose resistor values which allow a current of at least 2 μA, meaning the value of R<sub>2</sub> must not exceed 400 kΩ. TI recommends lower resistor values for highest accuracy and most robust design.

$$R_1 = R_2 \cdot \left( \frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (7)$$

#### 10.1.2 External Component Selection

##### 10.1.2.1 Inductor Selection

The TPS6281x-Q1 is designed for a nominal 0.47-μH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 0.47 μH cause a larger inductor current ripple which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly. See [Recommended Operating Conditions](#) for details.

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PFM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). 式 8 calculates the maximum inductor current.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (8)$$

$$\Delta I_{L(max)} = \frac{V_{OUT} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}{L \min} \cdot \frac{1}{f_{SW}} \quad (9)$$

where

- $I_{L(max)}$  is the maximum inductor current
- $\Delta I_{L(max)}$  is the peak-to-peak inductor ripple current
- $L_{min}$  is the minimum inductance at the operating point

**表 10-1. Typical Inductors**

TYPE	INDUCTANCE [μH]	CURRENT [A] <sup>(1)</sup>	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [LxBxH] mm	MANUFACTURER <sup>(2)</sup>
XFL4015-471ME	0.47 μH, ±20%	3.5	TPS62813-Q1, TPS62812-Q1	2.25 MHz	4 × 4 × 1.6	Coilcraft
XEL4020-561ME	0.56 μH, ±20%	9.9	TPS62810-Q1, TPS62813-Q1, TPS62812-Q1	2.25 MHz	4 × 4 × 2.1	Coilcraft

**表 10-1. Typical Inductors (continued)**

TYPE	INDUCTANCE [μH]	CURRENT [A] (1)	FOR DEVICE	NOMINAL SWITCHING FREQUENCY	DIMENSIONS [LxBxH] mm	MANUFACTURER(2)
XEL4030-471ME	0.47 μH, ±20%	12.3	TPS62810-Q1, TPS62813-Q1, TPS62812-Q1	2.25 MHz	4 × 4 × 3.1	Coilcraft
XEL3515-561ME	0.56 μH, ±20%	4.5	TPS62813-Q1, TPS62812-Q1	2.25 MHz	3.5 × 3.2 × 1.5	Coilcraft
XFL3012-331MEB	0.33 μH, ±20%	2.6	TPS62811-Q1 TPS62812-Q1	≥ 3.5 MHz	3 × 3 × 1.3	Coilcraft
XPL2010-681ML	0.68 μH, ±20%	1.5	TPS62811-Q1	2.25 MHz	2 × 1.9 × 1	Coilcraft
DFE252012PD-R47M	0.47 μH, ±20%	see data sheet	TPS62812-Q1, TPS62813-Q1	2.25 MHz	2.5 × 2 × 1.2	Murata

(1) Lower of  $I_{RMS}$  at 20°C rise or  $I_{SAT}$  at 20% drop.

(2) See the [Third-party Products Disclaimer](#).

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends a margin of about 20% to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

### 10.1.3 Capacitor Selection

#### 10.1.3.1 Input Capacitor

For most applications, 22 μF nominal is sufficient and recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a low-ESR multilayer ceramic capacitor (MLCC) for best filtering and must be placed between VIN and GND as close as possible to those pins.

#### 10.1.3.2 Output Capacitor

The architecture of the TPS6281x-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use dielectric X7R, X7T, or an equivalent. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in three steps based on the minimum capacitance used on the output. The maximum capacitance is 470 μF in any of the compensation settings.

The minimum capacitance required on the output depends on the compensation setting as well as on the current rating of the device. TPS62810-Q1 and TPS62813-Q1 require a minimum output capacitance of 27 μF while the lower current versions TPS62812-Q1 and TPS62811-Q1 requires 15 μF at minimum. The required output capacitance also changes with the output voltage.

For output voltages below 1 V, the minimum increases linearly from 32 μF at 1 V to 53 μF at 0.6 V for the TPS62810-Q1, the TPS62813-Q1 with the compensation setting for smallest output capacitance. Other compensation ranges for TPS62811-Q1 and TPS62812-Q1, or both are equivalent. See [表 9-1](#) and [表 9-2](#) for details.

## 10.2 Typical Application

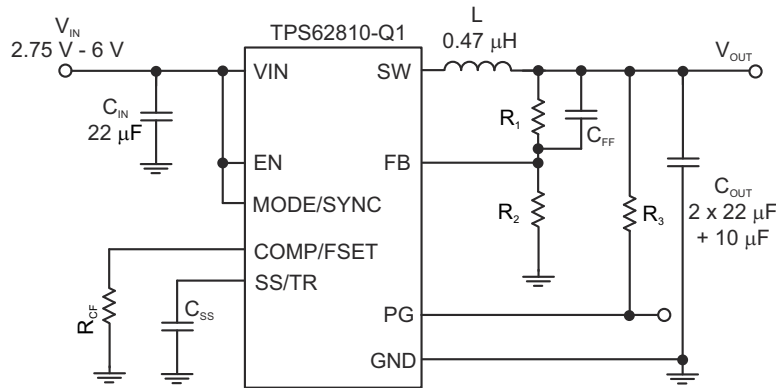


图 10-1. Typical Application

### 10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

### 10.2.2 Detailed Design Procedure

$$R_1 = R_2 \cdot \left( \frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (10)$$

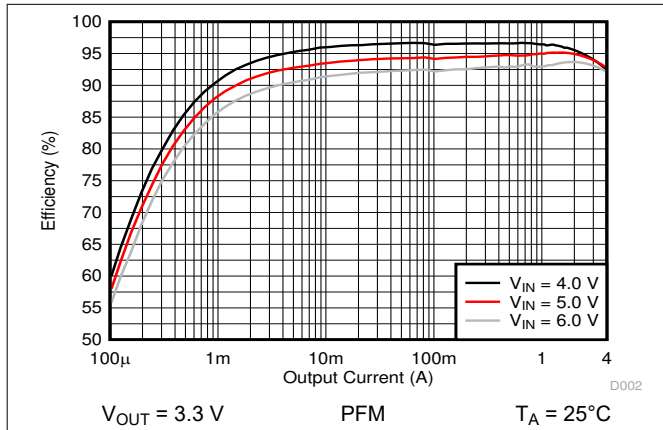
With  $V_{FB} = 0.6 \text{ V}$ :

表 10-2. Setting the Output Voltage

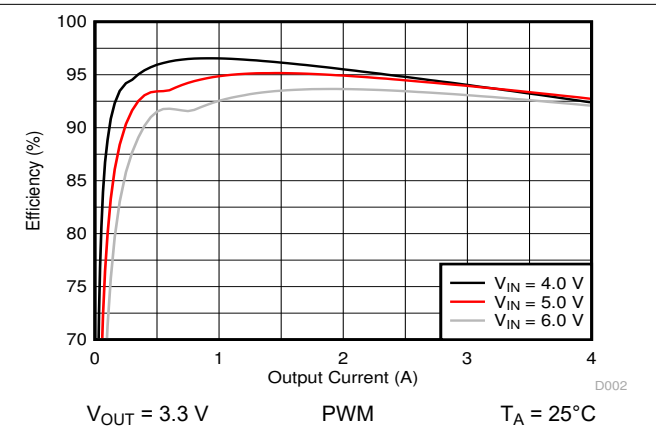
NOMINAL OUTPUT VOLTAGE $V_{OUT}$	$R_1$	$R_2$	$C_{FF}$	EXACT OUTPUT VOLTAGE
0.8 V	16.9 k $\Omega$	51 k $\Omega$	10 pF	0.7988 V
1.0 V	20 k $\Omega$	30 k $\Omega$	10 pF	1.0 V
1.1 V	39.2 k $\Omega$	47 k $\Omega$	10 pF	1.101 V
1.2 V	68 k $\Omega$	68 k $\Omega$	10 pF	1.2 V
1.5 V	76.8 k $\Omega$	51 k $\Omega$	10 pF	1.5 V
1.8 V	80.6 k $\Omega$	40.2 k $\Omega$	10 pF	1.803 V
2.5 V	47.5 k $\Omega$	15 k $\Omega$	10 pF	2.5 V
3.3 V	88.7 k $\Omega$	19.6 k $\Omega$	10 pF	3.315 V

### 10.2.3 Application Curves

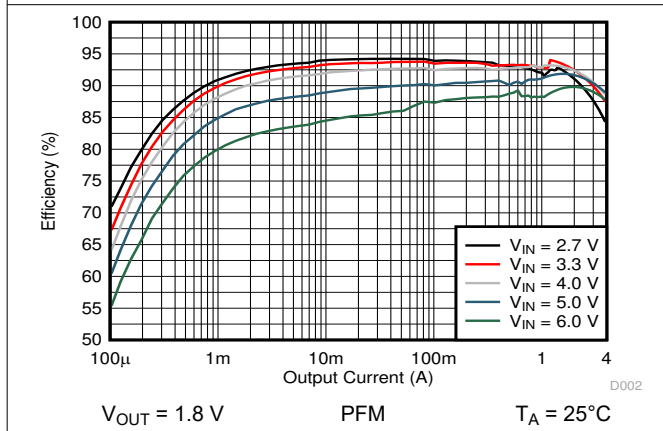
All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to 表 8-1.



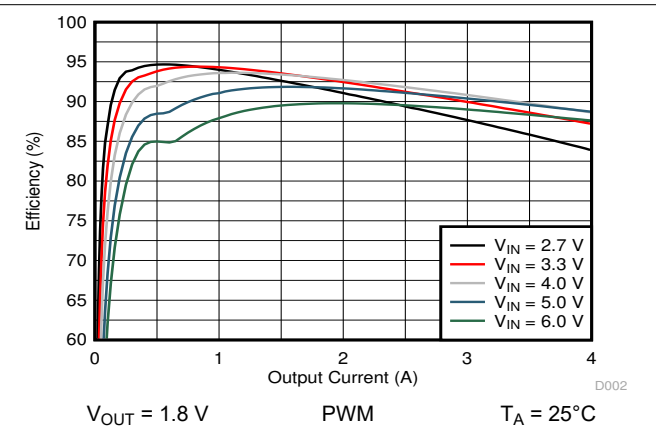
**10-2. Efficiency versus Output Current**



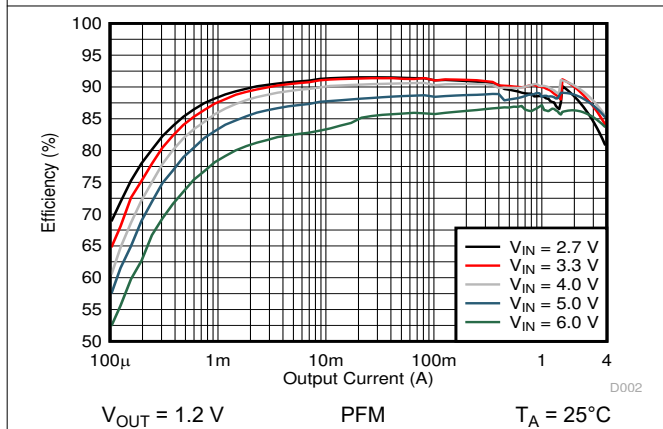
**10-3. Efficiency versus Output Current**



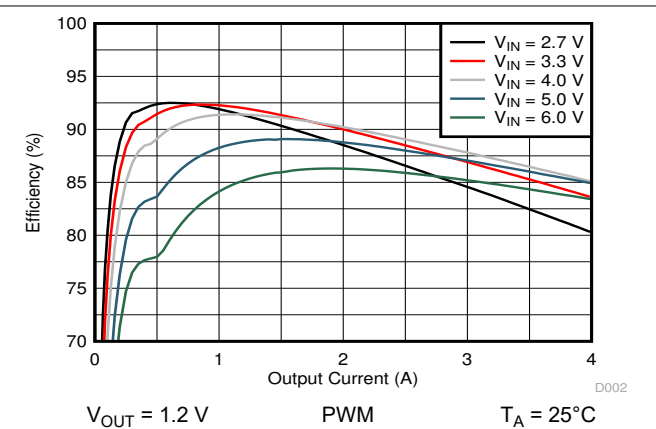
**10-4. Efficiency versus Output Current**



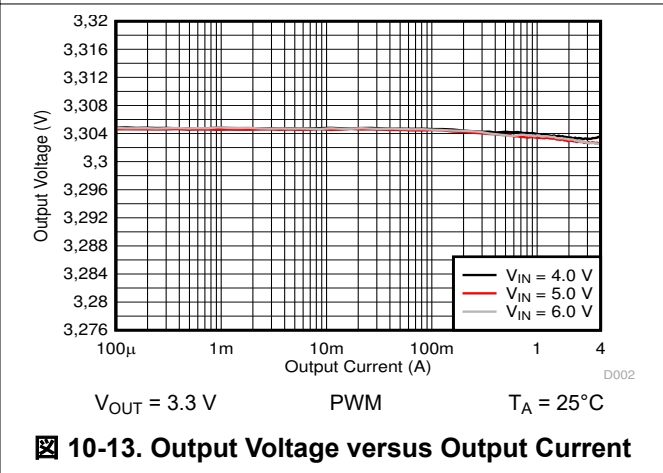
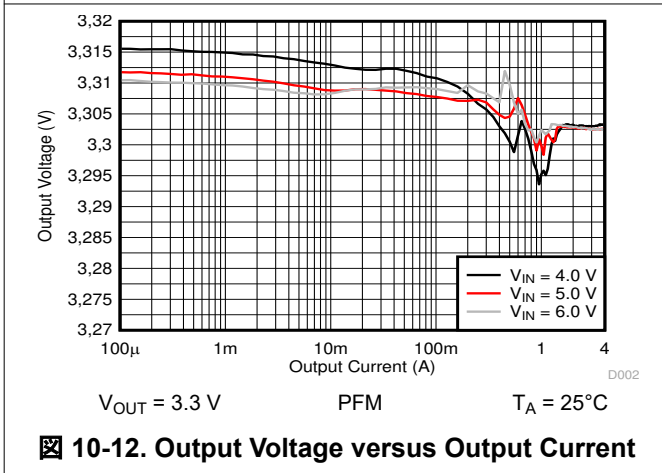
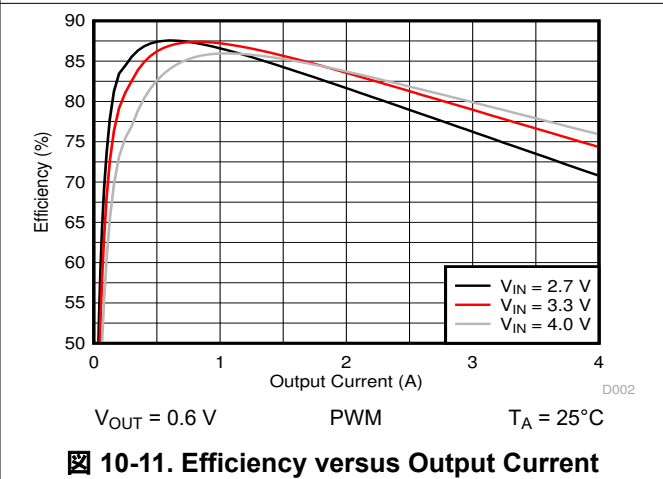
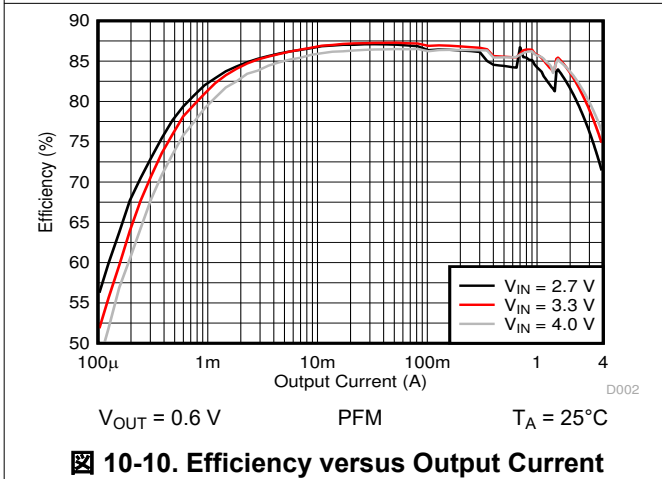
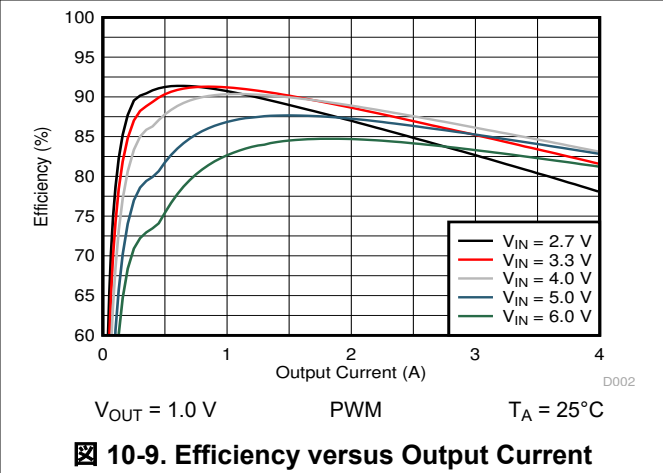
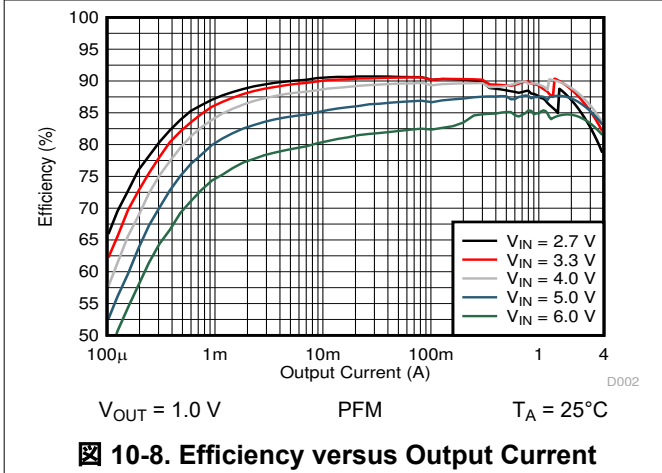
**10-5. Efficiency versus Output Current**

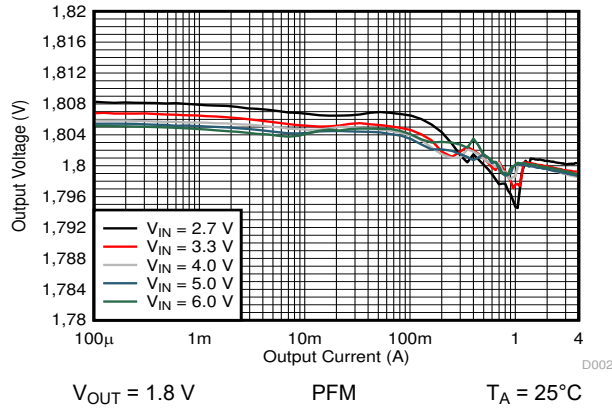


**10-6. Efficiency versus Output Current**

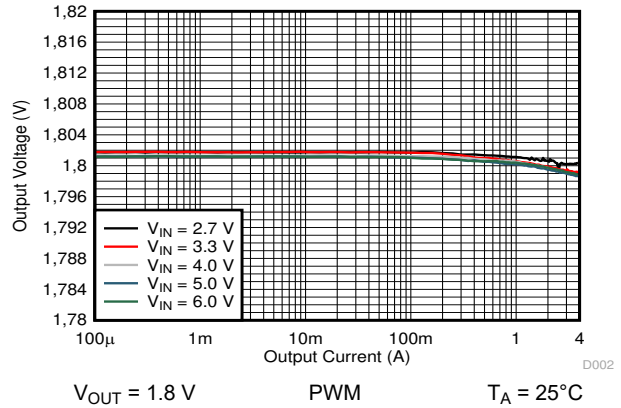


**10-7. Efficiency versus Output Current**

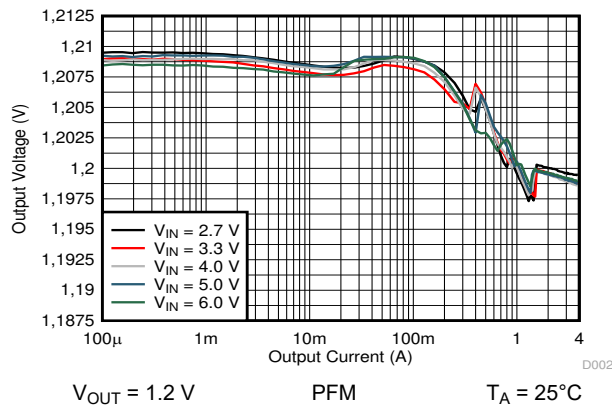




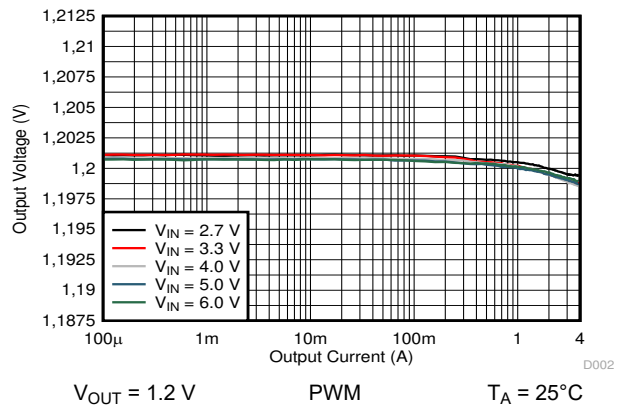
**10-14. Output Voltage versus Output Current**



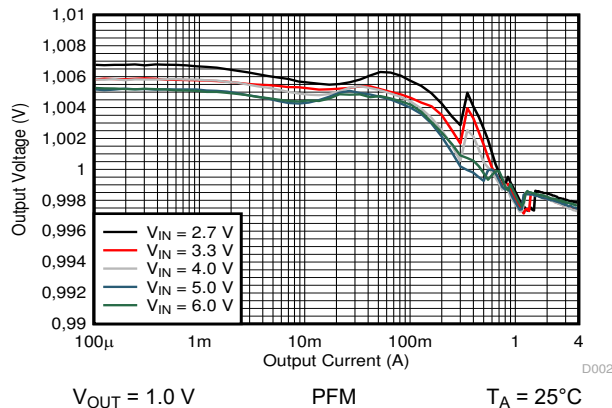
**10-15. Output Voltage versus Output Current**



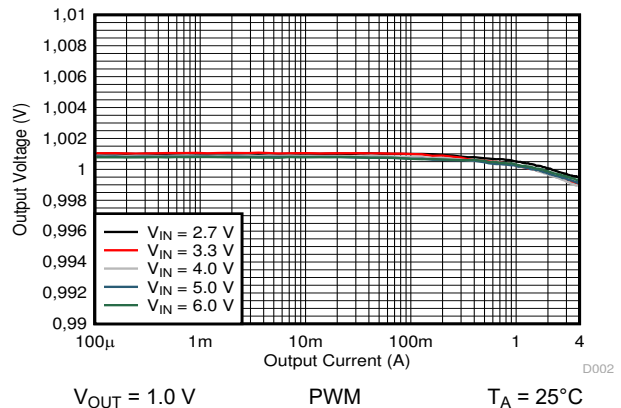
**10-16. Output Voltage versus Output Current**



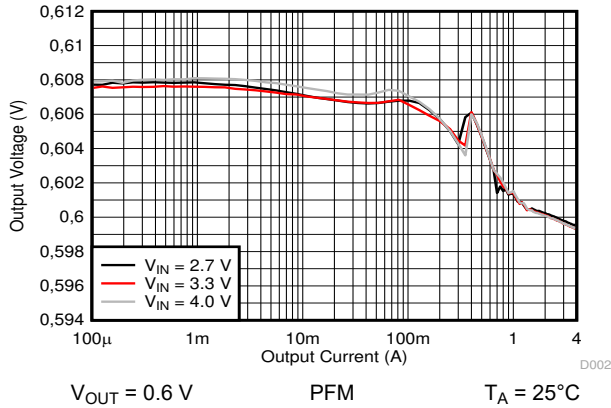
**10-17. Output Voltage versus Output Current**



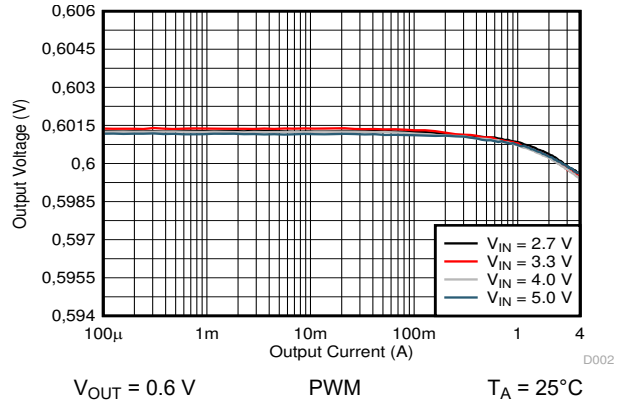
**10-18. Output Voltage versus Output Current**



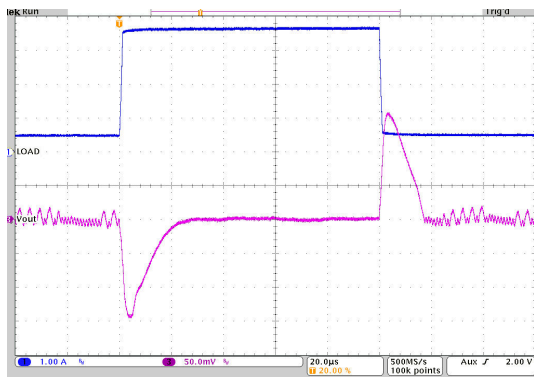
**10-19. Output Voltage versus Output Current**



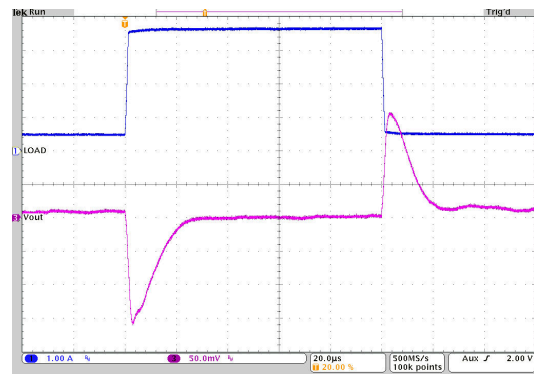
**10-20. Output Voltage versus Output Current**



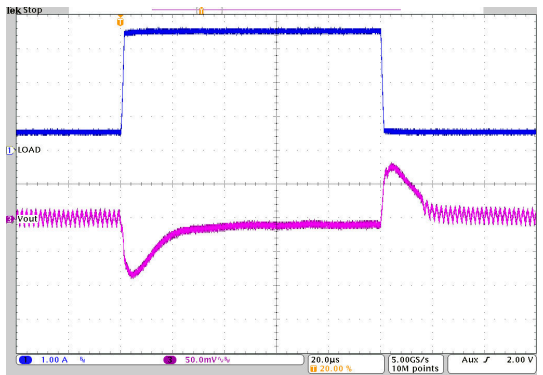
**10-21. Output Voltage versus Output Current**



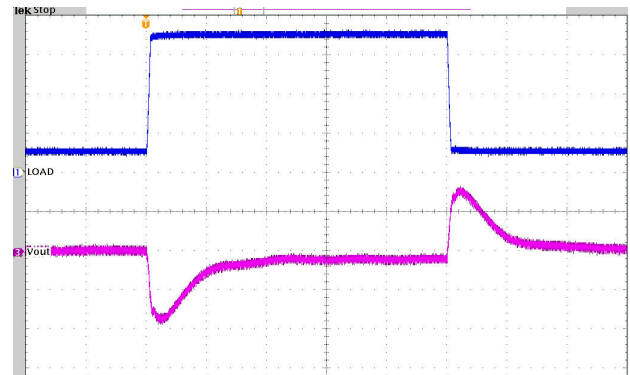
**10-22. Load Transient Response**



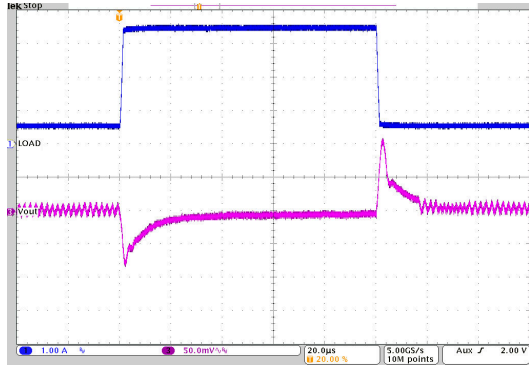
**10-23. Load Transient Response**



**10-24. Load Transient Response**

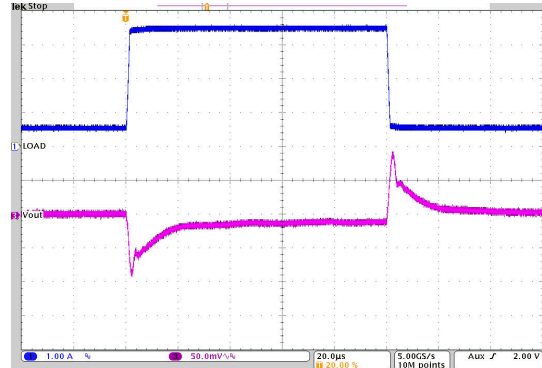


**10-25. Load Transient Response**



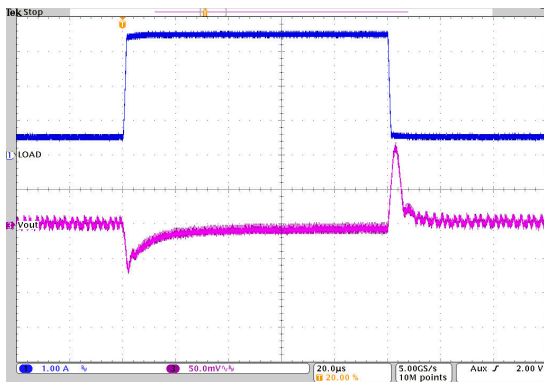
$V_{OUT} = 1.2\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.4\text{ A to } 3.6\text{ A to } 0.4\text{ A}$

 **10-26. Load Transient Response**



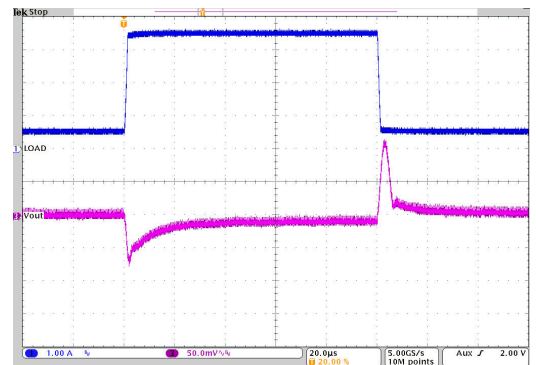
$V_{OUT} = 1.2\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.4\text{ A to } 3.6\text{ A to } 0.4\text{ A}$

 **10-27. Load Transient Response**



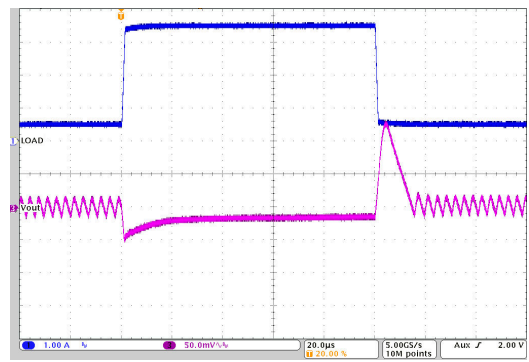
$V_{OUT} = 1.0\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.4\text{ A to } 3.6\text{ A to } 0.4\text{ A}$

 **10-28. Load Transient Response**



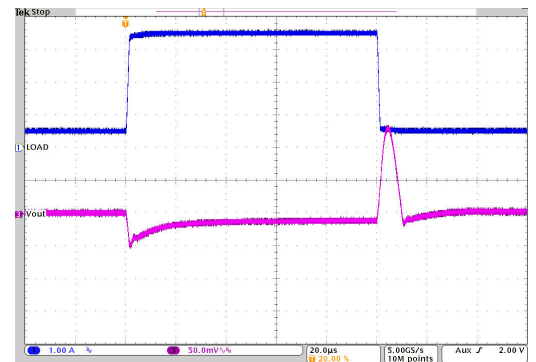
$V_{OUT} = 1.0\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 5.0\text{ V}$        $I_{OUT} = 0.4\text{ A to } 3.6\text{ A to } 0.4\text{ A}$

 **10-29. Load Transient Response**



$V_{OUT} = 0.6\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 3.3\text{ V}$        $I_{OUT} = 0.4\text{ A to } 3.6\text{ A to } 0.4\text{ A}$

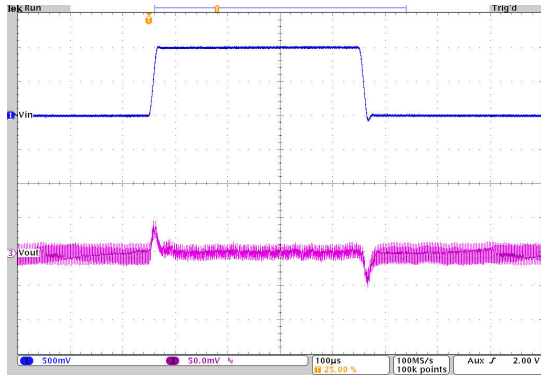
 **10-30. Load Transient Response**



$V_{OUT} = 0.6\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $V_{IN} = 3.3\text{ V}$        $I_{OUT} = 0.4\text{ A to } 3.6\text{ A to } 0.4\text{ A}$

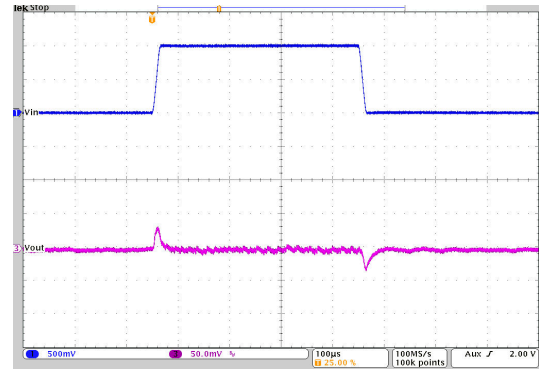
 **10-31. Load Transient Response**





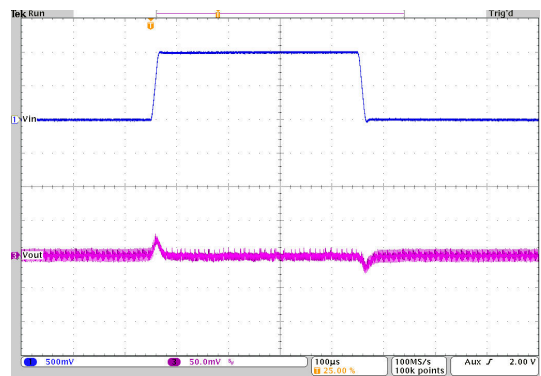
$V_{OUT} = 3.3\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-32. Line Transient Response**



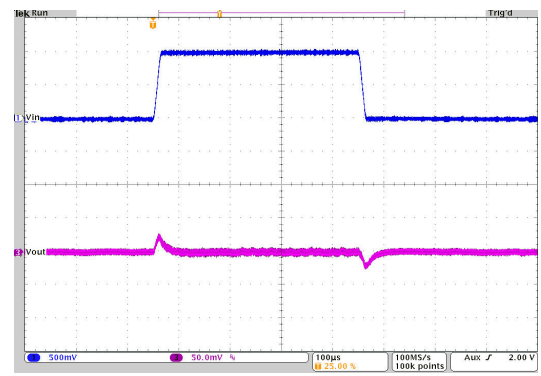
$V_{OUT} = 3.3\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-33. Line Transient Response**



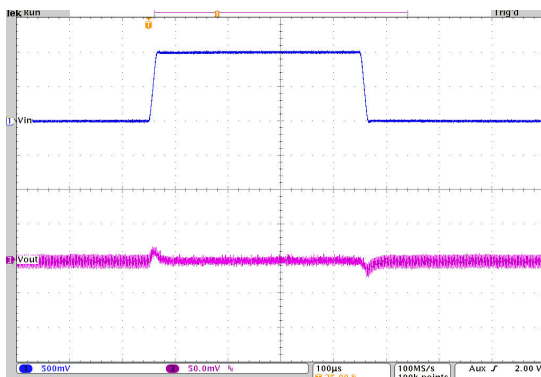
$V_{OUT} = 1.8\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-34. Line Transient Response**



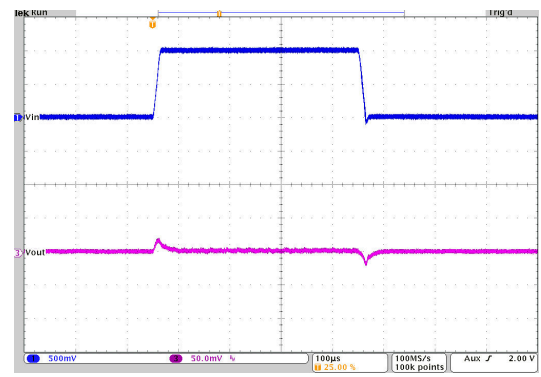
$V_{OUT} = 1.8\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-35. Line Transient Response**



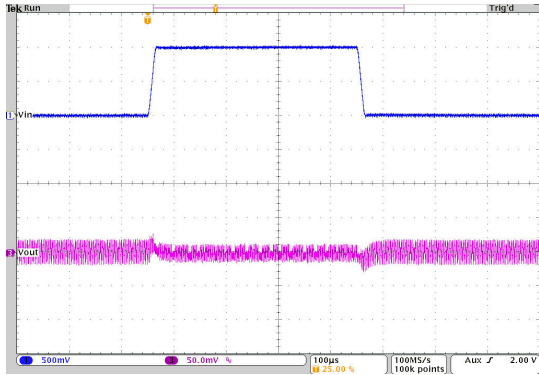
$V_{OUT} = 1.2\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-36. Line Transient Response**



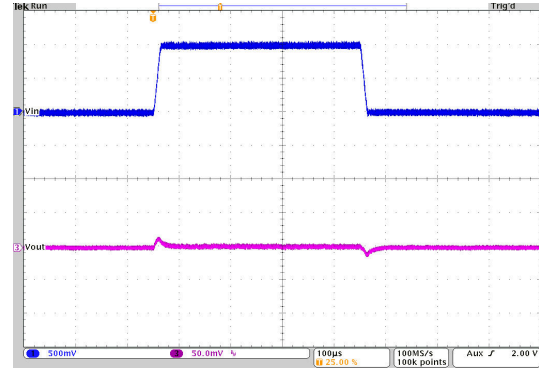
$V_{OUT} = 1.2\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-37. Line Transient Response**



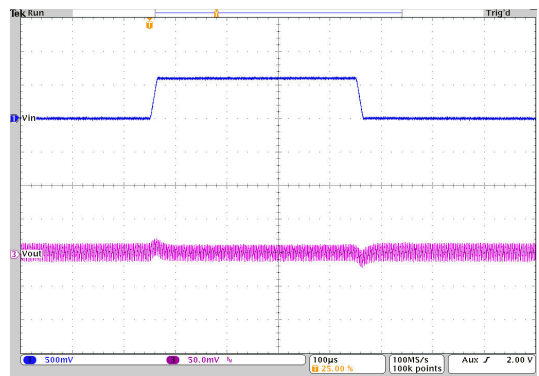
$V_{OUT} = 1.0\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-38. Line Transient Response**



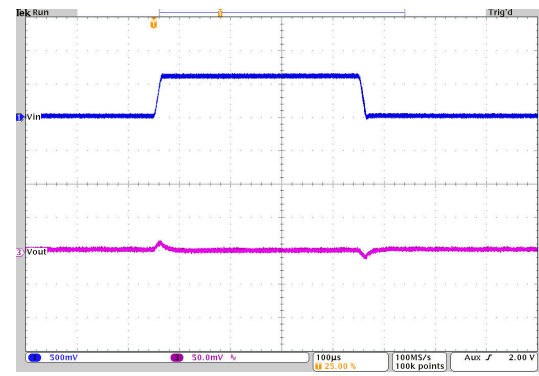
$V_{OUT} = 1.0\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 4.5\text{ V to } 5.5\text{ V to } 4.5\text{ V}$

**10-39. Line Transient Response**



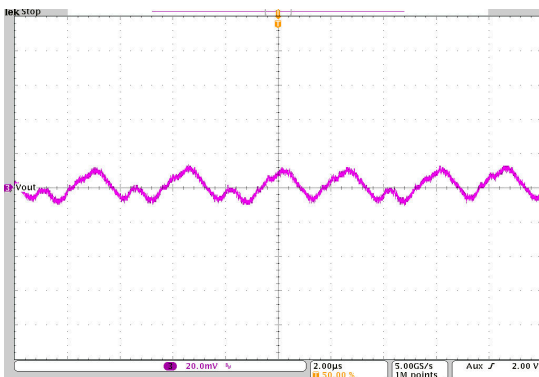
$V_{OUT} = 0.6\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 3.0\text{ V to } 3.6\text{ V to } 3.0\text{ V}$

**10-40. Line Transient Response**



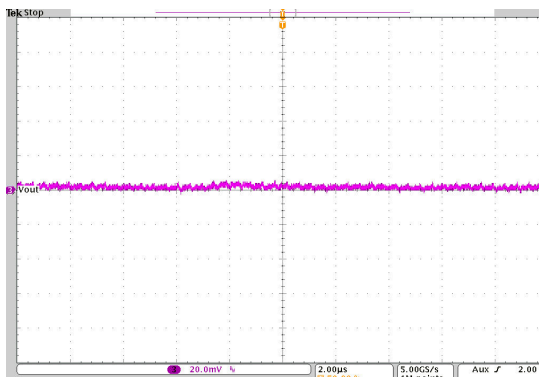
$V_{OUT} = 0.6\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 3.0\text{ V to } 3.6\text{ V to } 3.0\text{ V}$

**10-41. Line Transient Response**



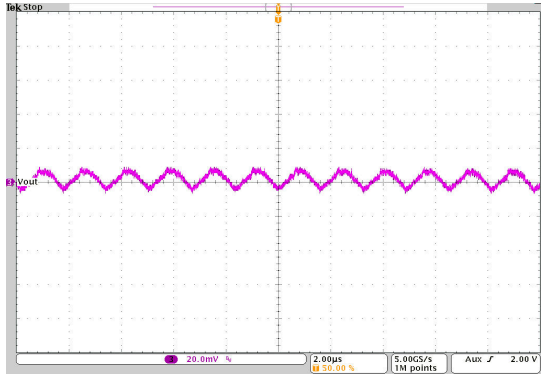
$V_{OUT} = 3.3\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 5.0\text{ V}$        $BW = 20\text{ MHz}$

**10-42. Output Voltage Ripple**



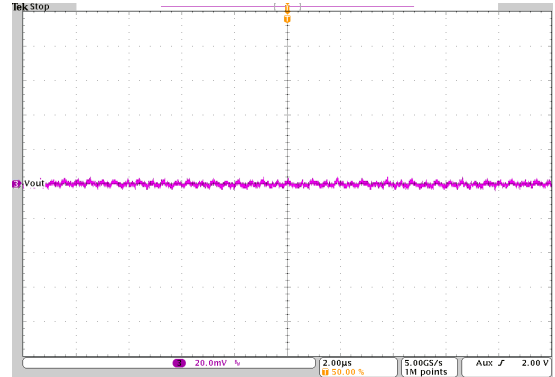
$V_{OUT} = 3.3\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5.0\text{ V}$        $BW = 20\text{ MHz}$

**10-43. Output Voltage Ripple**



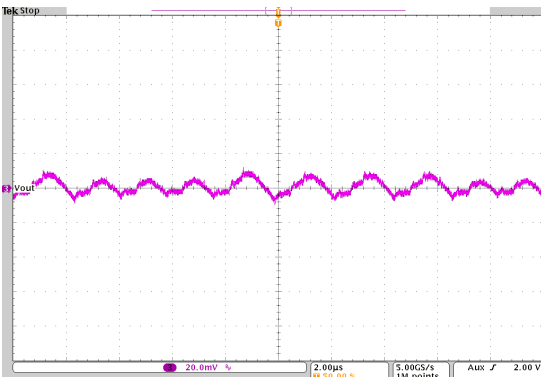
$V_{OUT} = 1.8\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 5.0\text{ V}$       BW = 20 MHz

**10-44. Output Voltage Ripple**



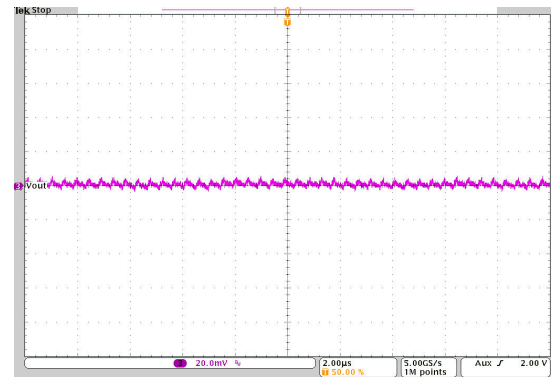
$V_{OUT} = 1.8\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5.0\text{ V}$       BW = 20 MHz

**10-45. Output Voltage Ripple**



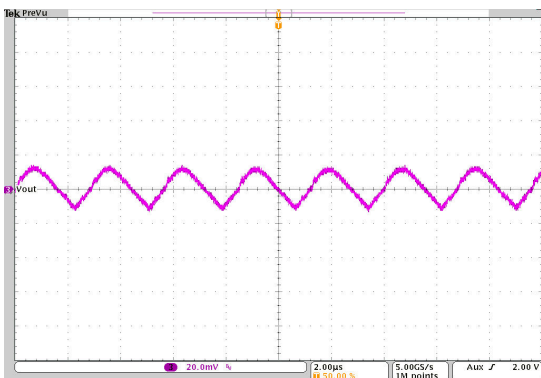
$V_{OUT} = 1.2\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 5.0\text{ V}$       BW = 20 MHz

**10-46. Output Voltage Ripple**



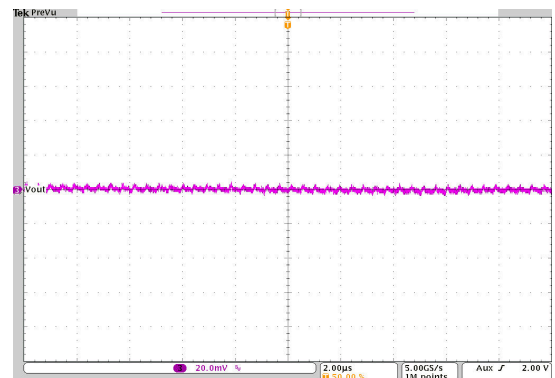
$V_{OUT} = 1.2\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5.0\text{ V}$       BW = 20 MHz

**10-47. Output Voltage Ripple**



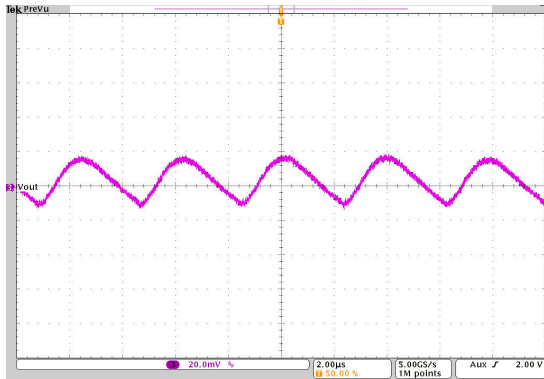
$V_{OUT} = 1.0\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 5.0\text{ V}$       BW = 20 MHz

**10-48. Output Voltage Ripple**



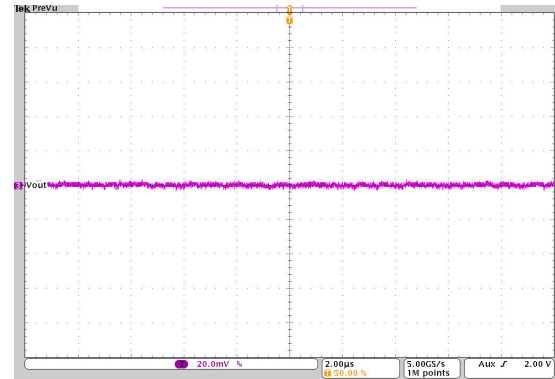
$V_{OUT} = 1.0\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5.0\text{ V}$       BW = 20 MHz

**10-49. Output Voltage Ripple**



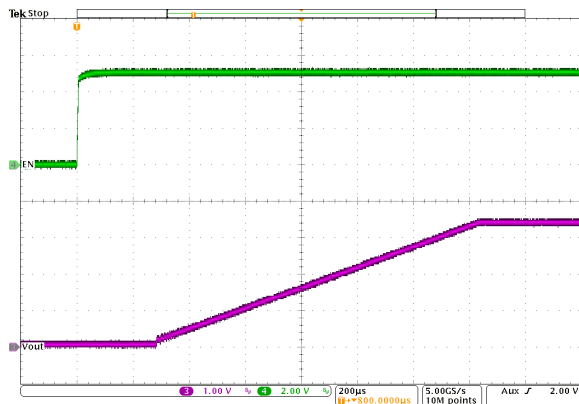
$V_{OUT} = 0.6\text{ V}$       PFM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 0.5\text{ A}$        $V_{IN} = 3.3\text{ V}$       BW = 20 MHz

**10-50. Output Voltage Ripple**



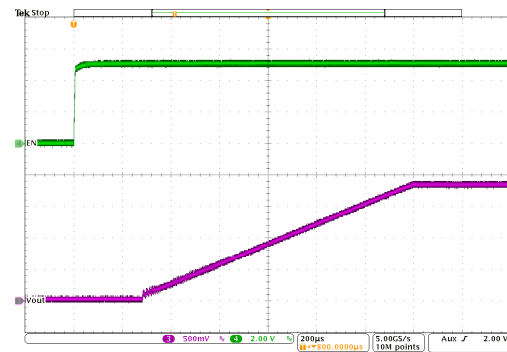
$V_{OUT} = 0.6\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 3.3\text{ V}$       BW = 20 MHz

**10-51. Output Voltage Ripple**



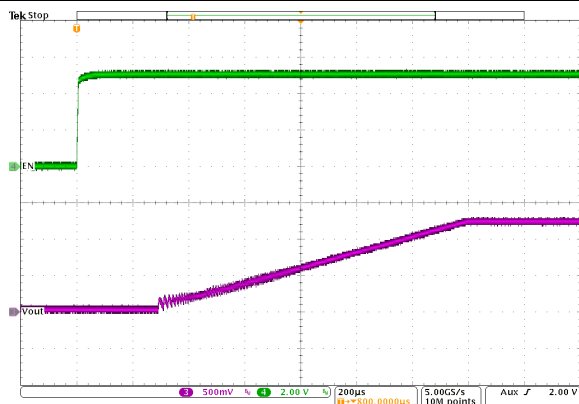
$V_{OUT} = 3.3\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5\text{ V}$        $C_{SS} = 4.7\text{ nF}$

**10-52. Start-Up Timing**



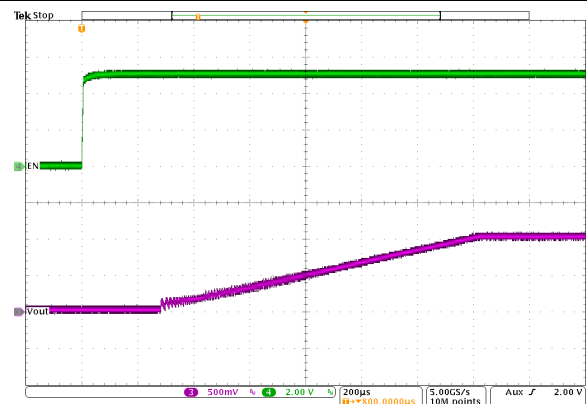
$V_{OUT} = 1.8\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5\text{ V}$        $C_{SS} = 4.7\text{ nF}$

**10-53. Start-Up Timing**



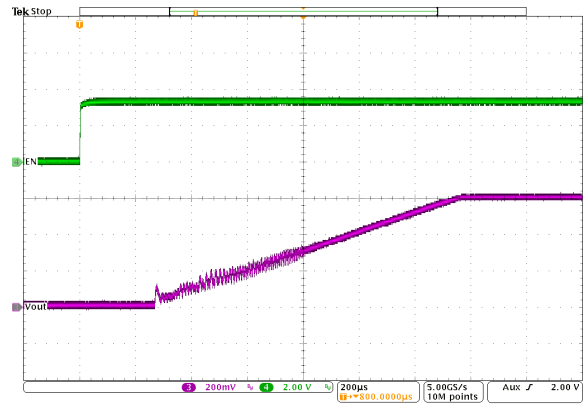
$V_{OUT} = 1.2\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5\text{ V}$        $C_{SS} = 4.7\text{ nF}$

**10-54. Start-Up Timing**



$V_{OUT} = 1.0\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 5\text{ V}$        $C_{SS} = 4.7\text{ nF}$

**10-55. Start-Up Timing**



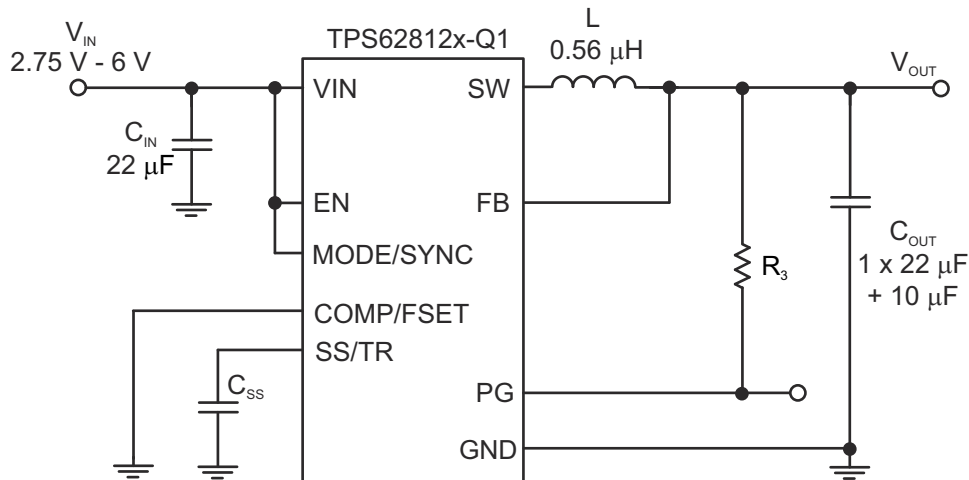
$V_{OUT} = 0.6\text{ V}$       PWM       $T_A = 25^\circ\text{C}$   
 $I_{OUT} = 4\text{ A}$        $V_{IN} = 3.3\text{ V}$        $C_{SS} = 4.7\text{ nF}$

**10-56. Start-up Timing**

## 10.3 System Examples

### 10.3.1 Fixed Output Voltage Versions

Versions with an internally fixed output voltage allow you to remove the external feedback voltage divider. This not only allows you to reduce the total solution size but also provides higher accuracy as there is no additional error caused by the external resistor divider. The FB pin must be tied to the output voltage directly as shown in [10-57](#). Independent of that, the application shown runs with an internally defined switching frequency of 2.25 MHz by connecting COMP/FSET to GND.



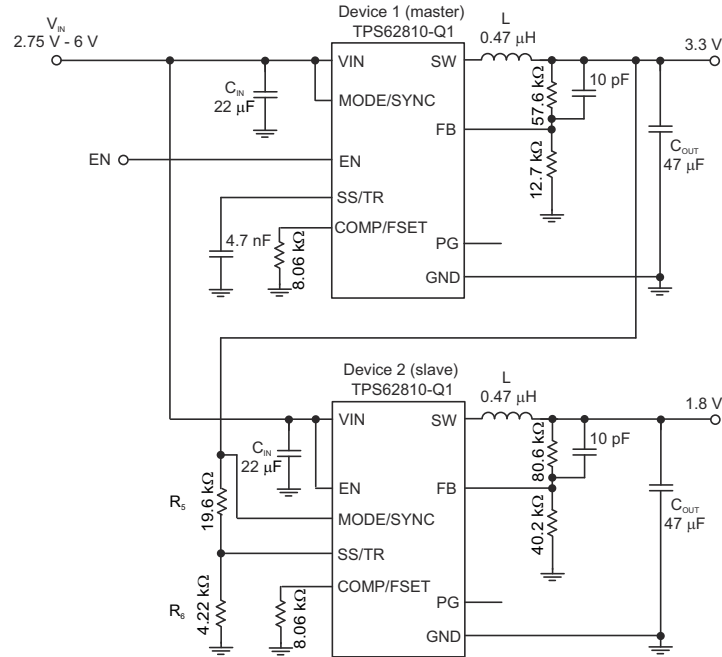
**10-57. Schematic for Fixed Output Voltage Versions**

### 10.3.2 Voltage Tracking

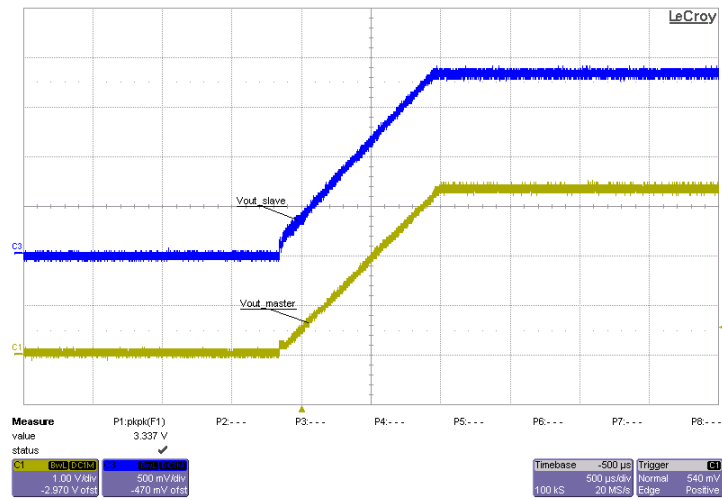
The TPS6281x-Q1 follows the voltage applied to the SS/TR pin. A voltage ramp on SS/TR to 0.6 V ramps the output voltage according to the 0.6 V feedback voltage.

Tracking the 3.3 V of device 1, such that both rails reach their target voltage at the same time, requires a resistor divider on SS/TR of device 2 equal to the output voltage divider of device 1. The output current of 2.5  $\mu$ A on the SS/TR pin causes an offset voltage on the resistor divider formed by  $R_5$  and  $R_6$ . The equivalent resistance of  $R_5 // R_6$ , so it must be kept below 15 k $\Omega$ . The current from SS/TR causes a slightly higher voltage across  $R_6$  than 0.6 V, which is desired because device 2 switches to its internal reference as soon as the voltage at SS/TR is higher than 0.6 V.

In case both devices must run in forced PWM mode, TI recommends to tie the MODE pin of device 2 to the output voltage or the power good signal of device 1, the master device. The TPS6281x-Q1 has a duty cycle limitation defined by the minimum on-time. For tracking down to low output voltages, device 2 cannot follow after the minimum duty cycle is reached. Enabling PFM mode while tracking is in progress allows you to ramp down the output voltage close to 0 V.



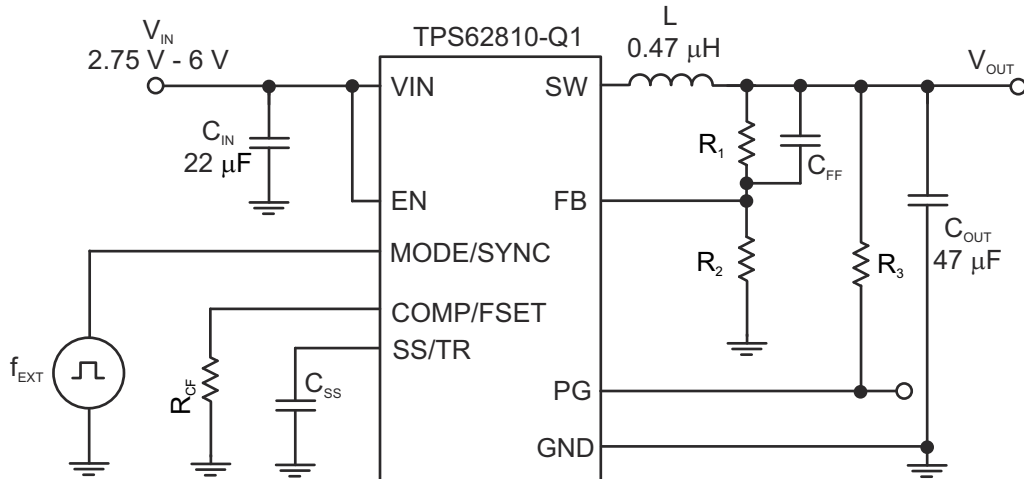
10-58. Schematic for Output Voltage Tracking



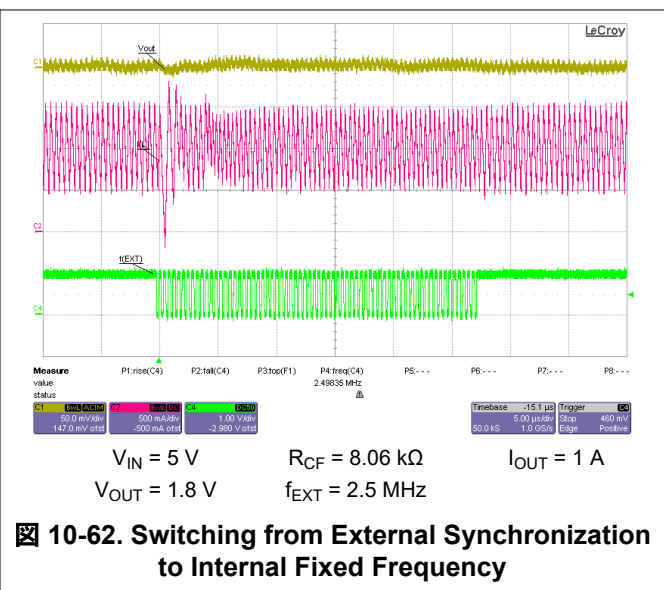
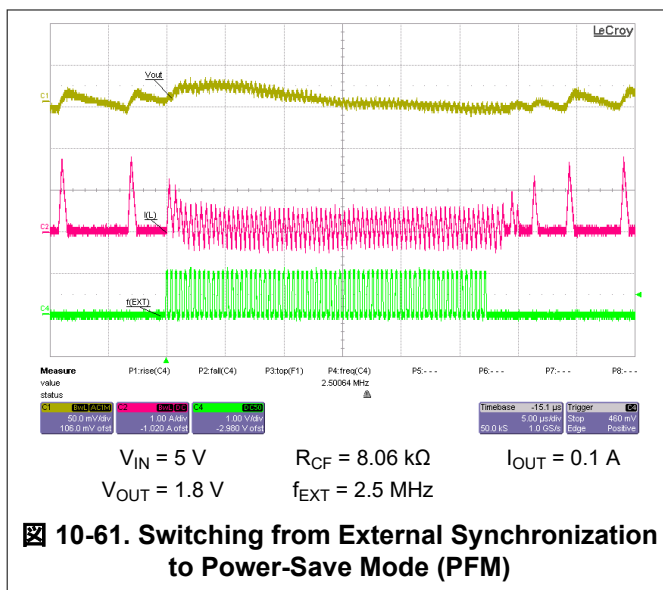
10-59. Scope Plot for Output Voltage Tracking

### 10.3.3 Synchronizing to an External Clock

The TPS6281x-Q1 can be externally synchronized by applying an external clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. The clock can be applied / removed during operation, allowing you to switch from an externally-defined fixed frequency to power-save mode or to internal fixed frequency operation. The value of the  $R_{CF}$  resistor must be chosen so that the internally defined frequency and the externally applied frequency are close to each other. This ensures a smooth transition from internal to external frequency and vice versa.



**FIG 10-60. Schematic Using External Synchronization**



## 10.4 Power Supply Recommendations

The TPS6281x-Q1 device family has no special requirements for its input power supply. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS6281x-Q1.

## 10.5 Layout

### 10.5.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6281x-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses increased EMI radiation and noise sensitivity.

See [Layout Example](#) for the recommended layout of the TPS6281x-Q1, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC



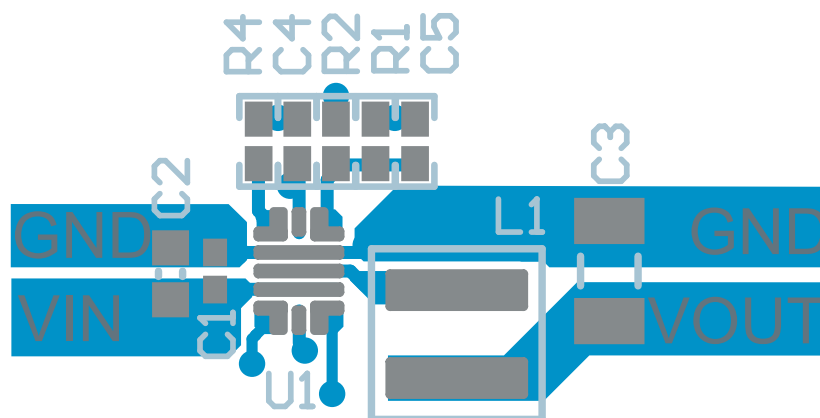
pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB must be connected with short wires and not nearby high dv/dt signals (for example SW). Because they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R<sub>1</sub> and R<sub>2</sub>, must be kept close to the IC and connect directly to those pins and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help spread the heat into the pcb.

The recommended layout is implemented on the EVM and shown in the [TPS62810EVM-015 Evaluation Module user's guide](#).

### 10.5.2 Layout Example



✎ 10-63. Example Layout

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, [TPS62810EVM-015 Evaluation Module user's guide](#)

### 11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.4 サポート・リソース

[TI E2E™ サポート・フォーラム](#) は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 11.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6281006QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81006Q	<a href="#">Samples</a>
TPS6281008QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81008Q	<a href="#">Samples</a>
TPS628100MQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8100MQ	<a href="#">Samples</a>
TPS6281020QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81020Q	<a href="#">Samples</a>
TPS62810QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	810Q	<a href="#">Samples</a>
TPS6281109QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81109Q	<a href="#">Samples</a>
TPS628110AQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8110AQ	<a href="#">Samples</a>
TPS6281120QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81120Q	<a href="#">Samples</a>
TPS6281126QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81126Q	<a href="#">Samples</a>
TPS628112AQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8112AQ	<a href="#">Samples</a>
TPS628112MQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8112MQ	<a href="#">Samples</a>
TPS628113HQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8113HQ	<a href="#">Samples</a>
TPS62811QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	811Q	<a href="#">Samples</a>
TPS6281206QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81206Q	<a href="#">Samples</a>
TPS6281208QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81208Q	<a href="#">Samples</a>
TPS628120MQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8120MQ	<a href="#">Samples</a>
TPS6281220QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81220Q	<a href="#">Samples</a>
TPS6281228QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81228Q	<a href="#">Samples</a>
TPS628122AQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8122AQ	<a href="#">Samples</a>
TPS628122GQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8122GQ	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6281240QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81240Q	<a href="#">Samples</a>
TPS62812QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	812Q	<a href="#">Samples</a>
TPS6281302QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81302Q	<a href="#">Samples</a>
TPS628130AQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8130AQ	<a href="#">Samples</a>
TPS6281320QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	81320Q	<a href="#">Samples</a>
TPS6281326QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 120	81326Q	<a href="#">Samples</a>
TPS628132DQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8132DQ	<a href="#">Samples</a>
TPS628132MQWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	8132MQ	<a href="#">Samples</a>
TPS62813QWRWYRQ1	ACTIVE	VQFN-HR	RWY	9	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	813Q	<a href="#">Samples</a>
XPS62810QWRWYRQ1	OBSOLETE	VQFN-HR	RWY	9		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6281006QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281008QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628100MQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281020QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62810QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281109QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628110AQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281120QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281126QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628112AQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628112MQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628113HQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62811QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281206QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281208QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628120MQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281220QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281228QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628122AQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628122GQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281240QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62812QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281302QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281302QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS628130AQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS628130AQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281320QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS6281326QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628132DQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS628132MQWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS62813QWRWYRQ1	VQFN-HR	RWY	9	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6281006QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281008QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628100MQWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281020QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS62810QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281109QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628110AQWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281120QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281126QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628112AQWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628112MQWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628113HQWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS62811QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281206QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281208QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628120MQWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281220QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281228QWRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628122AQRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628122GQRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281240QRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS62812QRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281302QRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281302QRWYRQ1	VQFN-HR	RWY	9	3000	213.0	191.0	35.0
TPS628130AQRWYRQ1	VQFN-HR	RWY	9	3000	213.0	191.0	35.0
TPS628130AQRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281320QRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS6281326QRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628132DQRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS628132MQRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0
TPS62813QRWYRQ1	VQFN-HR	RWY	9	3000	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

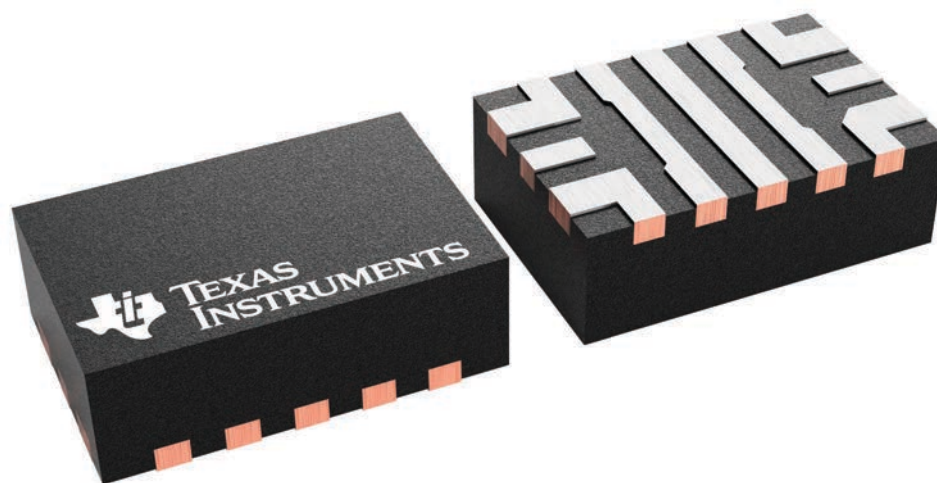
**RWY 9**

**VQFN-HR - 1 mm max height**

2 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



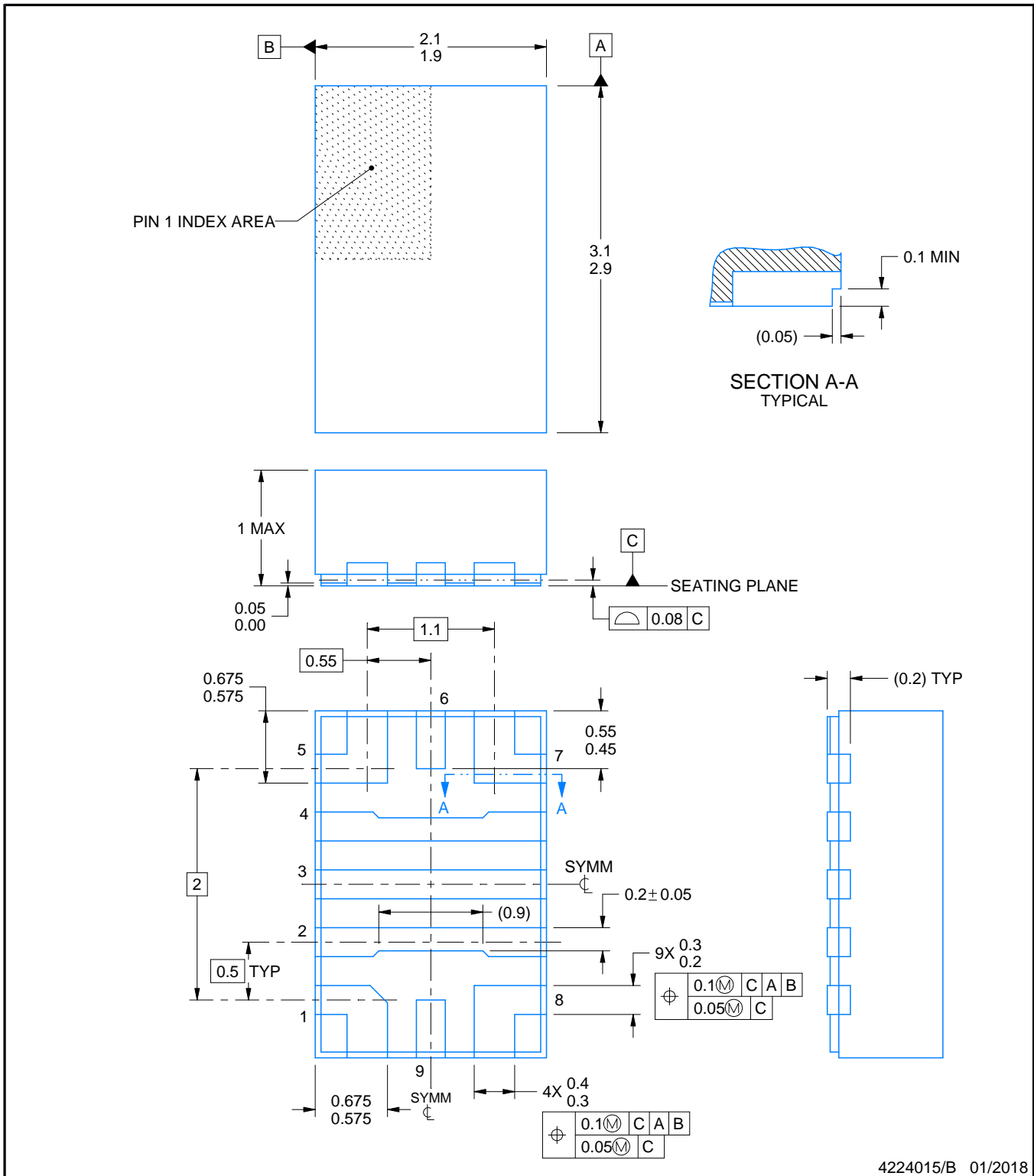
4226729/A

RWY0009A



**PACKAGE OUTLINE**  
**VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4224015/B 01/2018

**NOTES:**

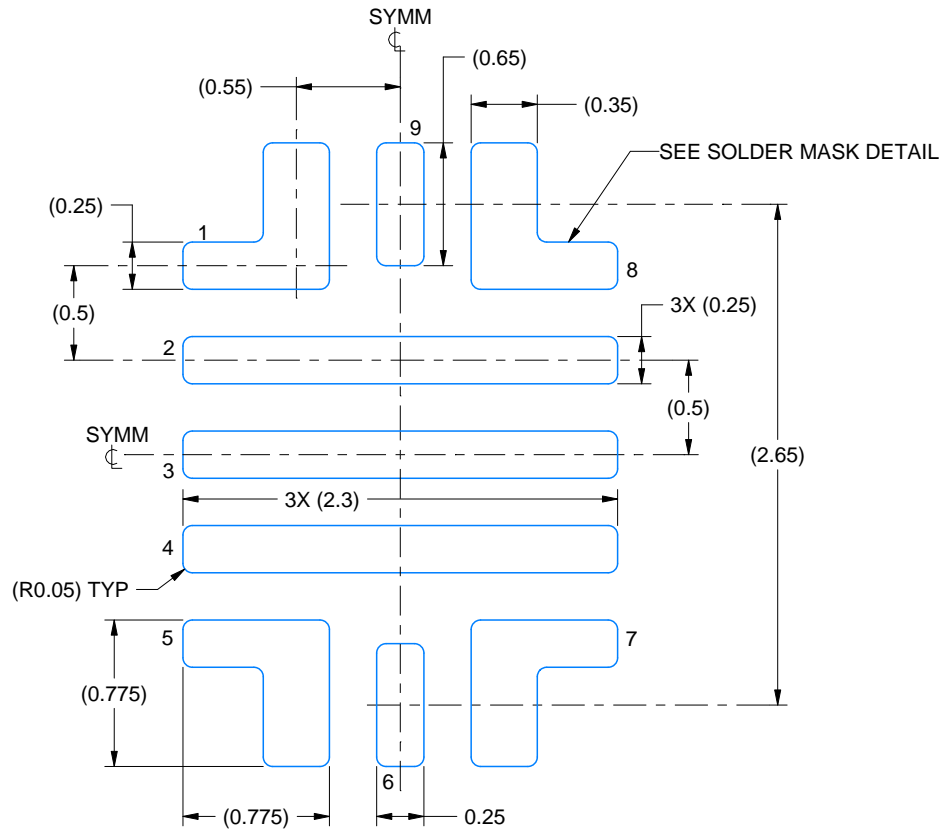
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

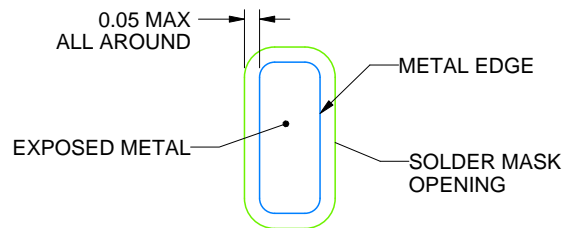
RWY0009A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



NON SOLDER MASK  
DEFINED

SOLDER MASK DETAIL

4224015/B 01/2018

NOTES: (continued)

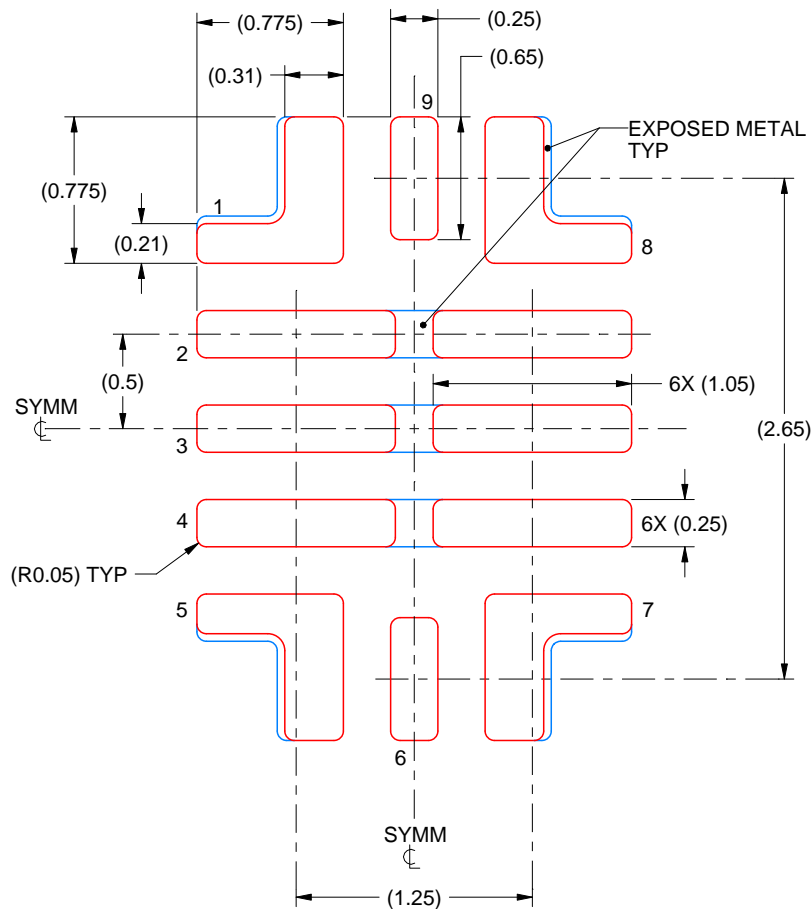
3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
4. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RWY0009A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

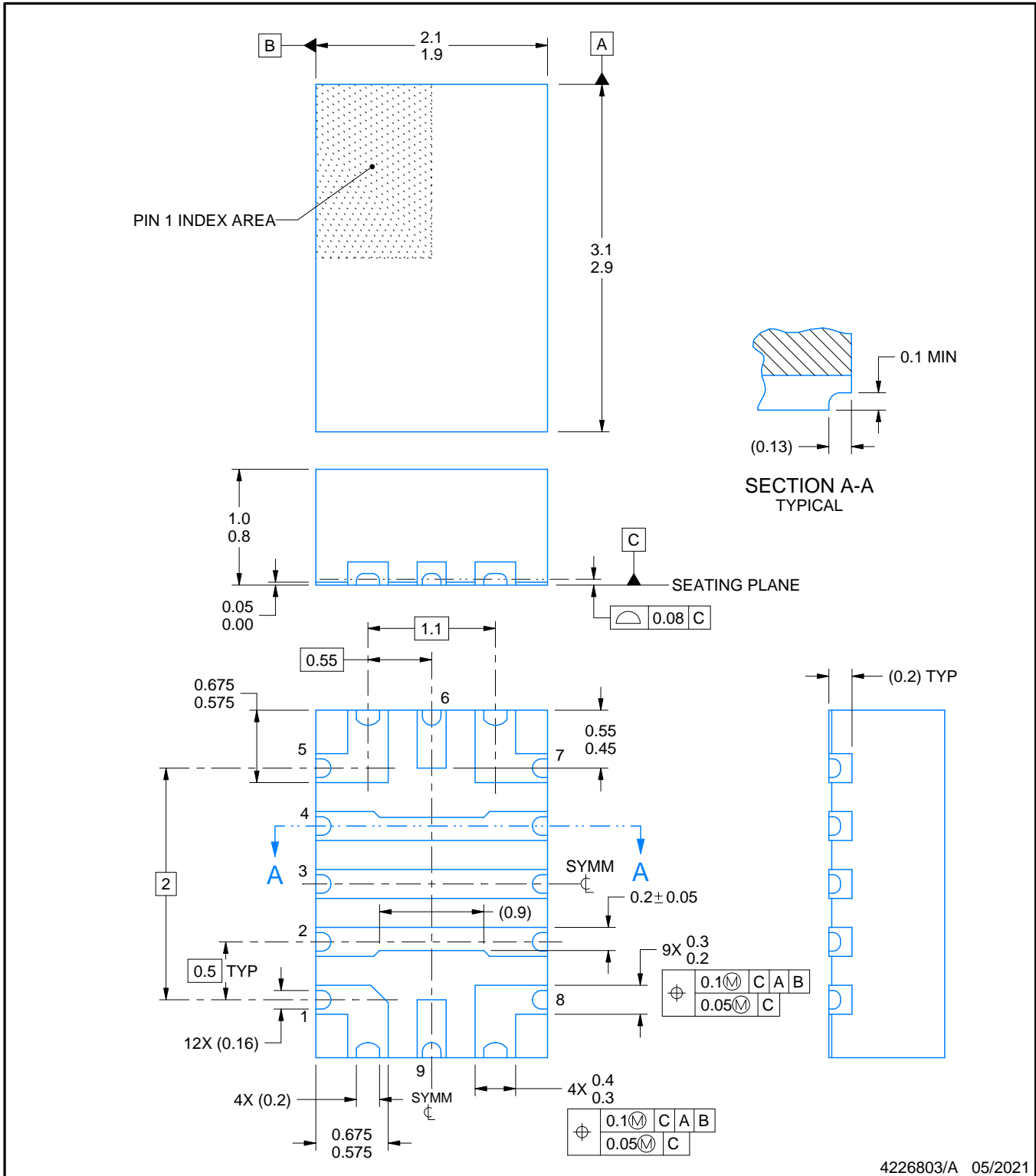


SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
PADS 1, 5, 7 & 8:  
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE: 25X

4224015/B 01/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

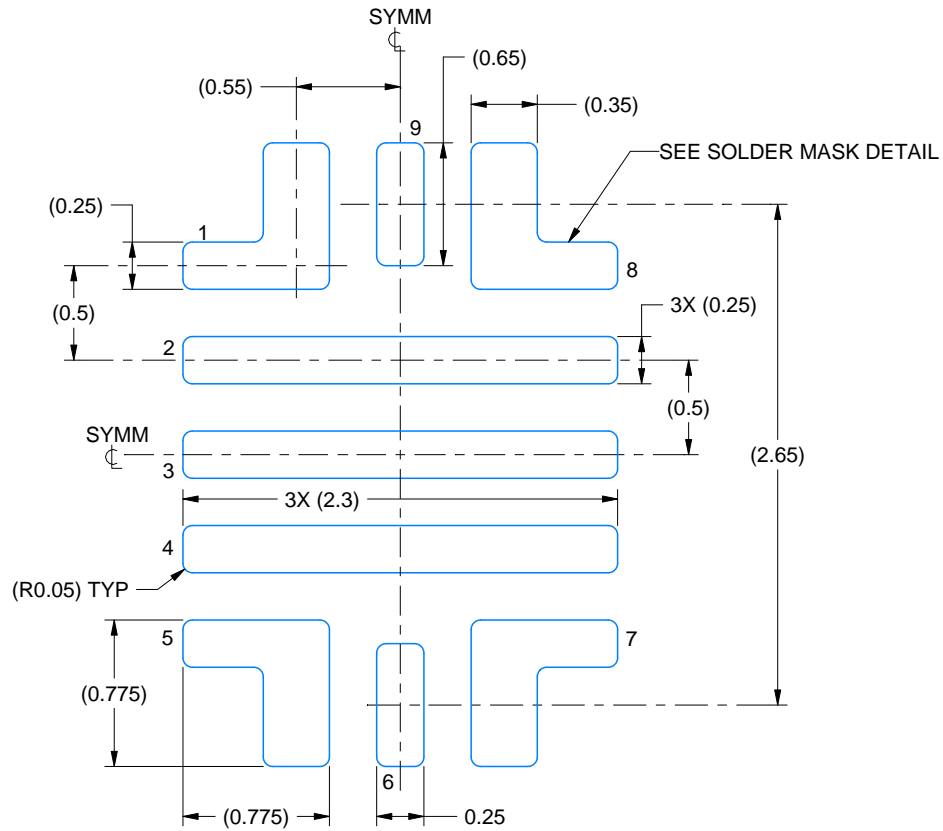
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

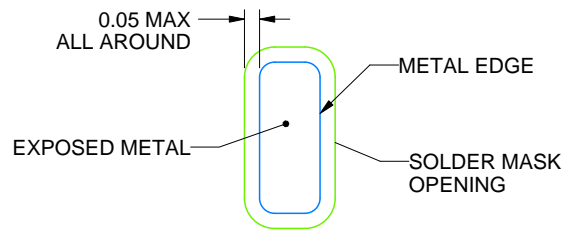
RWY0009C

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



NON SOLDER MASK  
DEFINED  
SOLDER MASK DETAIL

4226803/A 05/2021

NOTES: (continued)

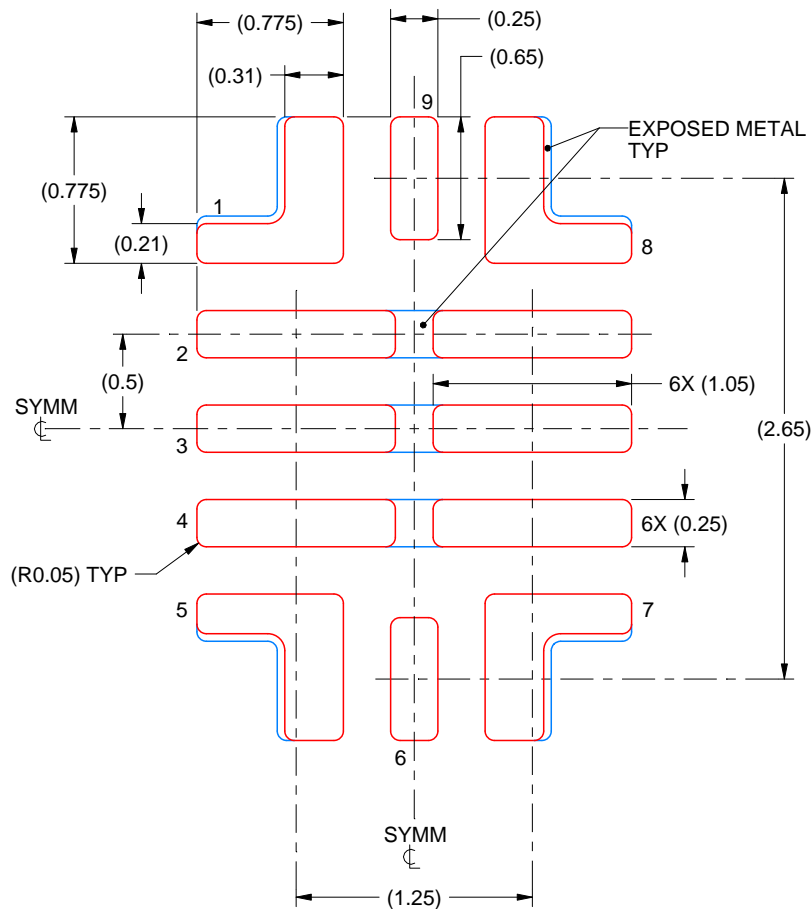
- This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RWY0009C

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
PADS 1, 5, 7 & 8:  
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE: 25X

4226803/A 05/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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