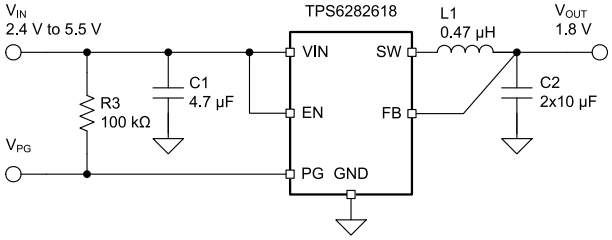
TPS6282x 出力精度 1%、2.4V～5.5V 入力、1、2、3、4A 降圧コンバータ

1 特長

- インダクタ内蔵パワー モジュールとして提供: TPSM82821、TPSM82822、TPSM82823
- DCS-Control トポロジ
- 1% の帰還または出力電圧精度 (全温度範囲)
- 最大 97% の効率
- 26mΩ/25mΩ のパワー MOSFET を内蔵
- 入力電圧範囲:2.4V～5.5V
- 動作時静止電流:4μA
- 2.2MHz のスイッチング周波数
- 調整可能な出力電圧:0.6V～4V
- パワー セーブ モードにより軽負荷時の効率を向上
- 100% デューティ サイクル動作による最小のドロップアウト電圧
- アクティブ出力放電
- パワー グッド出力
- サーマル シャットダウン保護機能
- ヒカップ短絡保護機能
- CCM 動作用の強制 PWM バージョン
- WEBENCH® Power Designer により、TPS6282x を使用するカスタム設計を作成

2 アプリケーション

- ソリッド・ステート・ドライブ (SSD)
- ポータブル・エレクトロニクス
- アナログ・セキュリティおよび IP ネットワーク・カメラ
- 産業用 PC
- マルチファンクション・プリンタ
- 一般的なポイント・オブ・ロード (POL)



代表的なアプリケーション回路図

3 概要

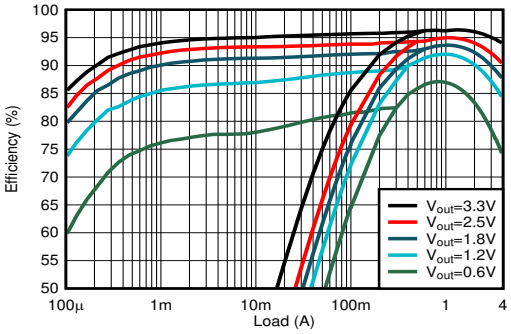
TPS6282x は使いやすい同期整流降圧型 DC/DC コンバータ ファミリであり、静止電流が 4μA と非常に小さいのが特長です。このデバイスは DCS-Control トポロジを基礎としており、過渡応答が高速です。内部基準電圧により、最低 0.6V まで出力電圧をレギュレートでき、接合部温度が –40℃～125℃の範囲で 1% の高い帰還電圧精度を維持します。このファミリのデバイスはピン互換および BOM 互換です。設計全体で、小さな 1 つの 470nH のインダクタ、1 つの 4.7μF の入力コンデンサ、2 つの 10μF または 1 つの 22μF 出力コンデンサしか必要としません。

TPS6282x には 2 種類のバージョンがあります。第 1 のバージョンにはパワーセーブ モードがあり、自動的にこのモードに移行して、非常に軽い負荷までの範囲で高い効率を維持し、システムのバッテリ動作時間を延長します。第 2 のバージョンは、出力電圧のリップルを最小限に抑え、スイッチング周波数をほぼ一定に保つため、連続導通モードを維持する強制 PWM で動作します。このデバイスは、パワー グッド信号と、内部ソフト スタート回路を備えています。このデバイスは 100% モードで動作可能です。障害保護の目的で、本デバイスは HICCUP (ヒカップ、間欠型) 短絡保護機能やサーマル シャットダウン機能を搭載しています。このデバイスは 6 ピンの 1.5mm × 1.5mm QFN パッケージで供給され、高電力密度の設計を実現できます。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS6282xx	DMQ (VSON-HR、6)	1.5mm × 1.5mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



V_{IN} = 5V での効率

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4 Device Options

PART NUMBER	OUTPUT VOLTAGE	OPERATION MODE	OUTPUT CURRENT
TPS62824DMQ	Adjustable	PSM/PWM	1A
TPS62825DMQ	Adjustable		2A
TPS6282518DMQ	1.8V		
TPS6282533DMQ	3.3V		
TPS62826DMQ	Adjustable		3A
TPS6282618DMQ	1.8V		
TPS62827DMQ	Adjustable		4A
TPS62824ADMQ	Adjustable	Forced-PWM	1A
TPS62825ADMQ	Adjustable		2A
TPS62826ADMQ	Adjustable		3A
TPS62827ADMQ	Adjustable		4A

5 Pin Configuration and Functions

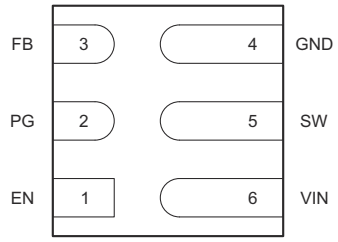


図 5-1. DMQ Package, 6-Pin VSON-HR (Bottom View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
PG	2	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5V. If unused, leave the pin floating.
FB	3	I	Feedback pin. For the fixed output voltage versions, this pin must be connected to the output.
GND	4		Ground pin
SW	5	PWR	Switch pin of the power stage
VIN	6	PWR	Input voltage pin

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage at Pins (2)	VIN, FB, EN, PG	–0.3	6	V
	SW (DC) (4)	–0.3	V_{IN} + 0.3	
	SW (DC, in current limit)	–1.0	V_{IN} + 0.3	
	SW (AC, less than 10ns) (3)	–2.5	10	
	SW (AC, PFM Mode, less than 100ns) (3)	–1.0	V_{IN} + 1.0	
Temperature	Operating junction temperature, T_J	–40	150	°C
	Storage temperature, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.
(4) After disabling the device, the SW voltage may exceed the MIN specification until the inductor and output capacitor are fully discharged.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range, TPS62824x, TPS62825x and TPS62826x	2.4		5.5	V
V_{IN}	Input voltage range, TPS62827x	2.5		5.5	V
V_{OUT}	Output voltage range	0.6		4.0	V
I_{OUT}	Output current range, TPS62824x	0		1	A
I_{OUT}	Output current range, TPS62825x	0		2	A
I_{OUT}	Output current range, TPS62826x	0		3	A
I_{OUT}	Output current range, TPS62827x	0		4	A
I_{SINK_PG}	Sink current at PG pin			1	mA
V_{PG}	Pull-up resistor voltage			5.5	V
T_J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE		UNIT
		TPS6282x, JEDEC	TPS62826EVM-794	
		6 pins	6 pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.5	71.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.9	n/a (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	n/a (2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	3.9	°C/W

6.4 Thermal Information (続き)

THERMAL METRIC(1)		DEVICE		UNIT
		TPS6282x, JEDEC	TPS62826EVM-794	
		6 pins	6 pins	
ψ_{JB}	Junction-to-board characterization parameter	33.1	38.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching		4	10	µA
I_Q	Quiescent current	EN = High, no load, FPWM devices		8		mA
I_{SD}	Shutdown current	EN = Low, T_J = -40 ℃ to 85 ℃		0.05	0.5	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level threshold voltage		1.0			V
V_{IL}	Low-level threshold voltage				0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin	EN = High		0.01	0.1	µA
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal, TPS62827		1.75		ms
		Time from EN high to 95% of V_{OUT} nominal, TPS62824x/5x/6x/7A		1.25		ms
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	94	96	98	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	90	92	94	%
	Power good upper threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	108	110	112	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	103	105	107	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01	0.1	µA
$t_{PG,DLY}$	Power good deglitch delay	PG rising edge		100		µs
		PG falling edge		20		
OUTPUT						
V_{OUT}	Output voltage accuracy	TPS6282533, PWM mode	3.267	3.3	3.333	V
V_{OUT}	Output voltage accuracy	TPS6282x18, PWM mode	1.78	1.8	1.82	V
V_{FB}	Feedback regulation voltage	PWM mode	594	600	606	mV
$I_{FB,LKG}$	Feedback input leakage current for adjustable output voltage	V_{FB} = 0.6 V		0.01	0.05	µA
R_{FB}	Internal resistor divider connected to FB pin, for fixed output votlage	TPS6282518, TPS6282618, TPS6282533		7.5		MΩ
I_{DIS}	Output discharge current	V_{SW} = 0.4V; EN = LOW	75	400		mA
	Load regulation	I_{OUT} = 0.5 A to 3 A, V_{OUT} = 1.8 V		0.1		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			25		mΩ

6.5 Electrical Characteristics (続き)

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM}	High-side FET switch current limit, DC	TPS62824A	1.7	2.1	2.4	A
		TPS62825x	2.74	3.3	3.9	A
		TPS62826x	3.7	4.3	5.0	A
		TPS62827x	4.8	5.6	6.4	A
I_{LIM}	Low-side FET negative current limit, DC	TPS62824A/5A/6A/7A		–1.6		A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.2		MHz

6.6 Typical Characteristics

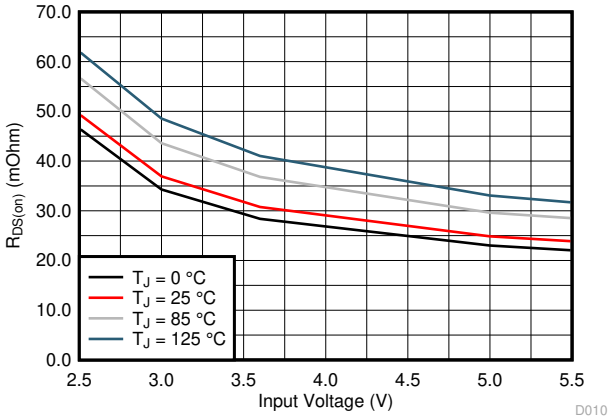


図 6-1. High-Side FET On-Resistance

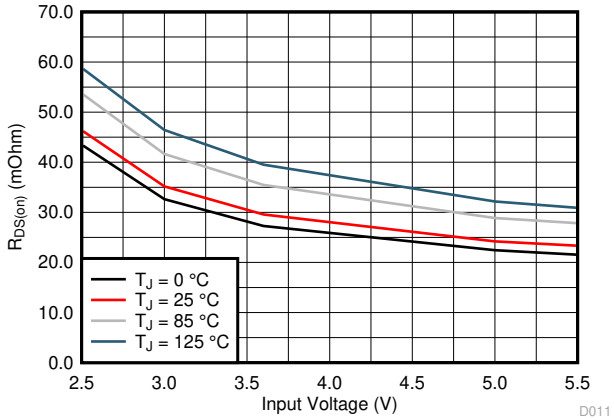


図 6-2. Low-Side FET On-Resistance

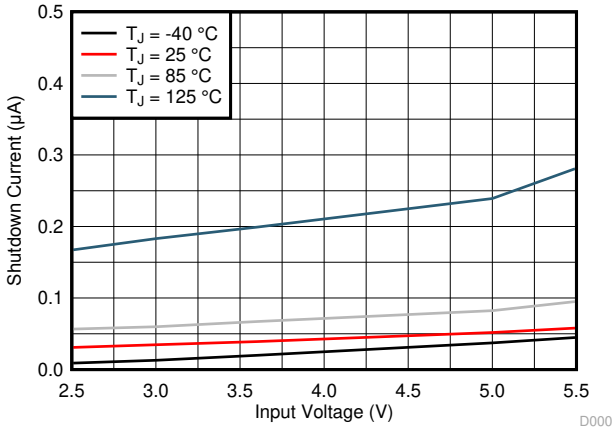


図 6-3. Shutdown Current

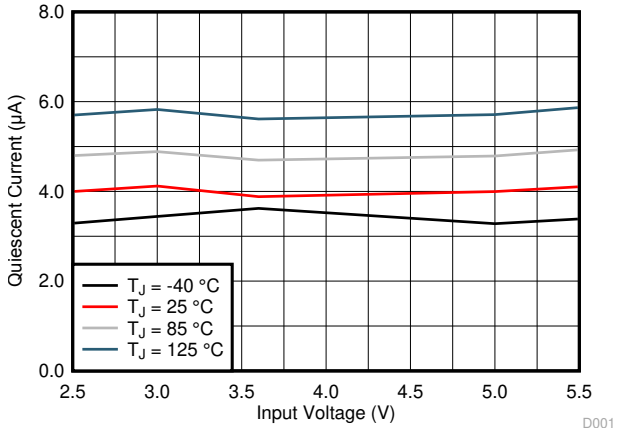


図 6-4. Quiescent Current

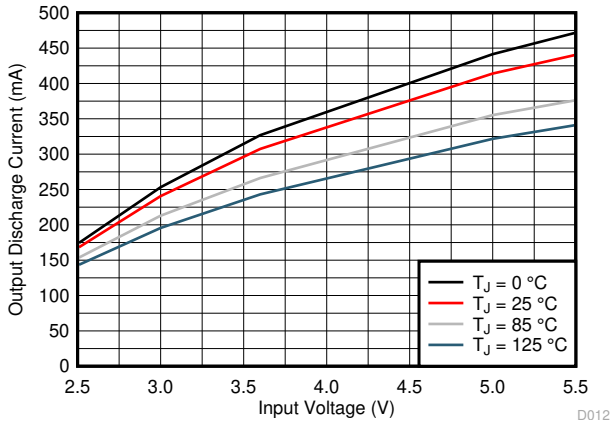


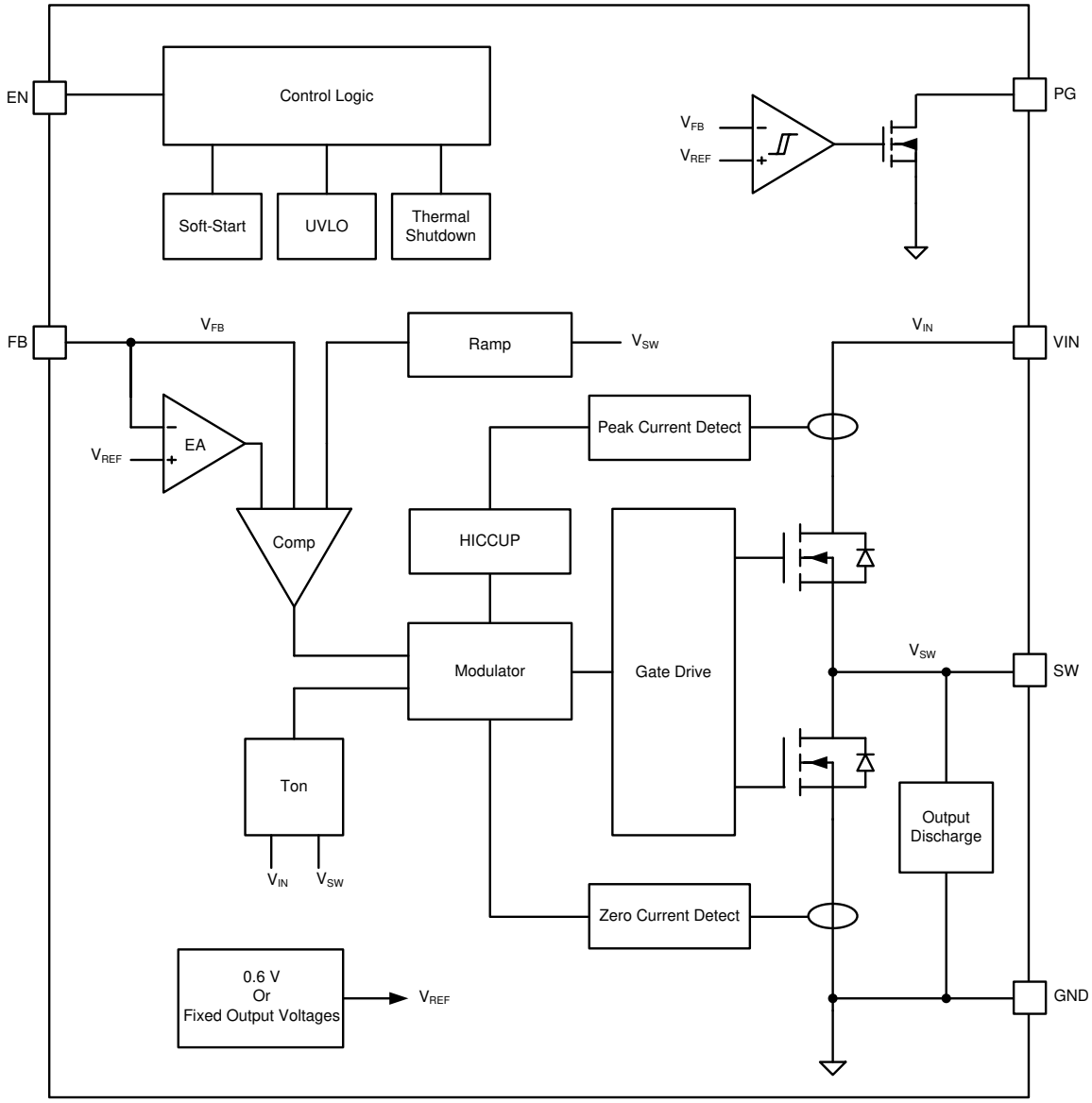
図 6-5. Output Discharge Current

7 Detailed Description

7.1 Overview

The TPS6282x are synchronous step-down converters based on the DCS-Control topology with an adaptive constant on-time control and a stabilized switching frequency. The devices operate in PWM (pulse width modulation) mode for medium to heavy loads and in PSM (power save mode) at light load conditions, keeping the output voltage ripple small. The nominal switching frequency is about 2.2MHz with a small and controlled variation over the input voltage range. As the load current decreases, the converter enters PSM, reducing the switching frequency to keep efficiency high over the entire load current range. Because combining both PWM and PSM within a single building block, the transition between modes is seamless and without effect on the output voltage. In forced-PWM devices, the converter maintains a continuous conduction mode operation and keeps the output voltage ripple very low across the whole load range and at a nominal switching frequency of 2.2MHz. The devices offer both excellent dc voltage and fast load transient regulation, combined with a very low output voltage ripple.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse Width Modulation (PWM) Operation

At load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM). The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 450ns \quad (1)$$

In forced-PWM devices, the device always operates in pulse width modulation in continuous conduction mode (CCM).

7.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This event happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates now with a fixed on-time and the switching frequency further decreases proportional to the load current. Use the following equation to calculate:

$$f_{PSM} = \frac{2 \times I_{OUT}}{T_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \quad (2)$$

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device can not enter PSM. The device maintains output regulation in PWM mode.

7.3.3 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles, because even at very low duty cycles, the switching frequency is reduced as needed to always make sure of a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between VIN and VOUT is determined by the voltage drop across the high-side FET and the DC resistance of the inductor. The minimum VIN that is needed to maintain a specific VOUT value is estimated as:

$$V_{IN,min} = V_{OUT} + I_{OUT,MAX} \times \left(R_{DS(on)} + R_L \right) \quad (3)$$

where

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.4 Soft Start

About 250µs after EN goes High, the internal soft-start circuitry controls the output voltage during start-up. This action avoids excessive inrush current and makes sure of a controlled output voltage ramp. This action also prevents unwanted voltage drops from high-impedance power sources or batteries. The TPS6282x can start into a prebiased output.

7.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from drawing excessive current in case of externally-caused overcurrent or short-circuit condition. Due to an internal propagation delay (typically 60ns), the actual AC peak current can exceed the static current limit during that time.

If the current limit threshold is reached, the device delivers maximum output current. Detecting this condition for 32 switching cycles (about 13µs), the device turns off the high-side MOSFET for about 100µs which allows the inductor current to decrease through the low-side MOSFET body diode and then restarts again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

In forced PWM devices, a negative current limit (I_{LIMN}) is enabled to prevent excessive current flowing backwards to the input. When the inductor current reaches I_{LIMN}, the low-side MOSFET turns off and the high-side MOSFET turns on and kept on until T_{ON} time expires.

7.3.6 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device if the input voltage drops below the UVLO threshold. The undervoltage lockout is set to about 2.2V with a hysteresis of typically 160mV.

7.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. After T_J has decreased enough, the device resumes normal operation.

7.4 Device Functional Modes

7.4.1 Enable, Disable, and Output Discharge

The device starts operation when Enable (EN) is set High. The input threshold levels are typically 0.9V for rising and 0.7V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 50nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore VIN must remain present for the discharge to function.

7.4.2 Power Good

The TPS6282x has a built-in power-good (PG) function. The PG pin goes high impedance when the output voltage has reached the nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see 表 7-1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge has a 100µs blanking time and the PG falling edge has a deglitch delay of 20µs.

表 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, V_{FB} ≥ 0.576V	√	
	EN = High, V_{FB} ≤ 0.552V		√
	EN = High, V_{FB} ≤ 0.63V	√	
	EN = High, V_{FB} ≥ 0.66V		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 0.7V$	√	

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

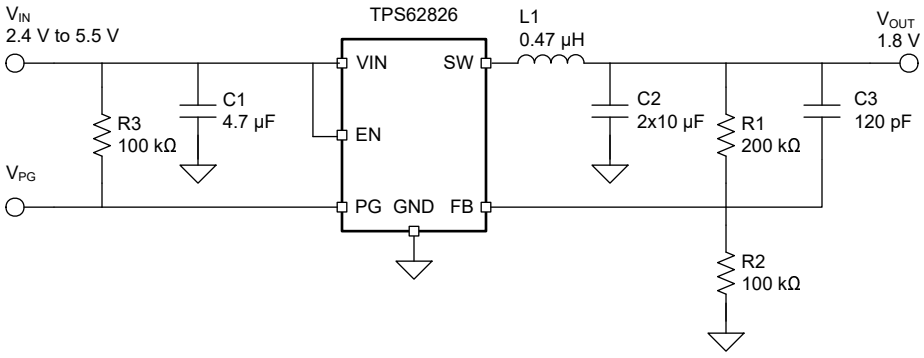


図 8-1. Typical Application of TPS62826x

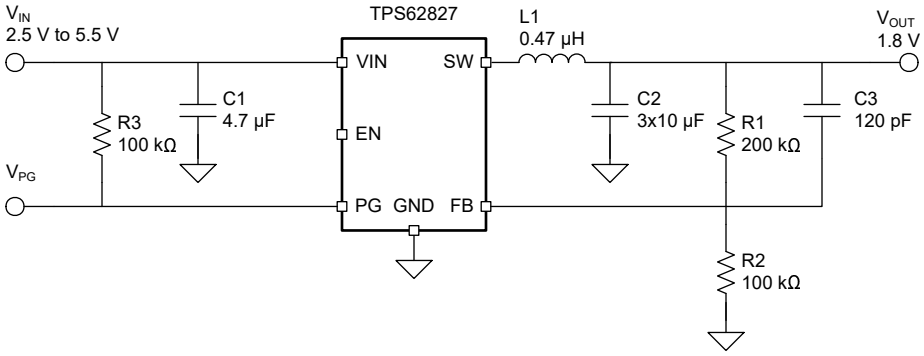


図 8-2. Typical Application of TPS62827

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, TPS62826x	2.4V to 5.5V
Input voltage, TPS62827x	2.5V to 5.5V
Output voltage	1.8V
Output ripple voltage	< 20mV
Maximum output current, TPS62826x	3A
Maximum output current, TPS62827x	4A

表 8-2 lists the components used for the example.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7µF, Ceramic capacitor, 6.3V, X7R, size 0603, JMK107BB7475MA	Taiyo Yuden
C2, TPS62824x/5x/6x/7A	2 × 10µF, Ceramic capacitor, 10V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C2, TPS62827	3 × 10µF, Ceramic capacitor, 10V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C3	120pF, Ceramic capacitor, 50V, size 0402	Std
L1	0.47µH, Power Inductor, XFL4015-471MEB	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	100kΩ, Chip resistor, 1/16W, 1%, size 0402	Std
R3	100kΩ, Chip resistor, 1/16W, 1%, size 0402	Std

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6282x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 式 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (4)$$

R2 must not be higher than 100kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. 式 5 shows how to compute the value of the feedforward capacitor for a given R2 value. For the recommended 100k value for R2, a 120pF feedforward capacitor is used.

$$C_3 = \frac{12\mu}{R2} \quad (5)$$

For the fixed output voltage versions, connect the FB pin to the output. R1, R2, and C3 are not needed. The fixed output voltage devices have an internal feedforward capacitor.

8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 8-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. check further combinations for each individual application.

表 8-3. Matrix of Output Capacitor and Inductor Combinations, TPS62824x, TPS62825x, TPS62826x, and TPS62827A

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	10	2 × 10 or 22	47	100
0.33				
0.47	+	+(1)	+	
1.0				

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –35%.

表 8-4. Matrix of Output Capacitor and Inductor Combinations, TPS62827

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	22	3 × 10	47	100
0.33				
0.47		+(1)	+	+
1.0				

8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 6 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \tag{6}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

TI recommends to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. 表 8-5 lists recommended inductors.

表 8-5. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS [L × W × H mm]	MAX. DC RESISTANCE [mΩ]	MFR PART NUMBER(1)
0.47	4.8	2.0 × 1.6 × 1.0	32	HTEN20161T-R47MDR, Cyntec
	4.6	2.0 × 1.2 × 1.0	25	HTEH20121T-R47MSR, Cyntec
	4.8	2.0 × 1.6 × 1.0	32	DFE201610E - R47M, MuRata
	4.8	2.0 × 1.6 × 1.0	32	DFE201210S - R47M, MuRata
	5.1	2.0 × 1.6 × 1.0	34	TFM201610ALM-R47MTAA, TDK
	5.2	2.0 × 1.6 × 1.0	25	TFM201610ALC-R47MTAA, TDK
	6.6	4.0 × 4.0 × 1.6	8.36	XFL4015-471ME, Coilcraft
	8.0	3.5 × 3.2 × 2.0	10.85	XEL3520-471ME, Coilcraft
	6.8	4.5 × 4 × 1.8	11.2	WE-LHMI-744373240047, Würth

(1) See the *Third-party Products Disclaimer*.

8.2.2.5 Capacitor Selection

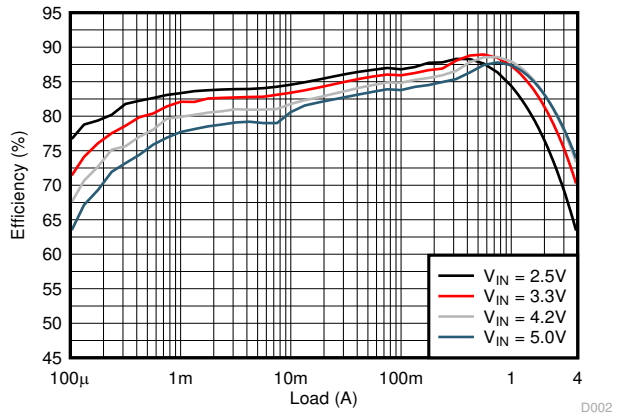
The input capacitor is the low-impedance energy source for the converters which helps provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, a minimum effective input capacitance of 3µF must be present, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. Considering the DC-bias derating the capacitance, the minimum effective output capacitance is 10µF for TPS62824x, TPS62825x, TPS62826x. and TPS62827A and 20µF for TPS62827.

A feed forward capacitor is required for the adjustable version, as described in *Setting the Output Voltage*. This capacitor is not required for the fixed output voltage versions.

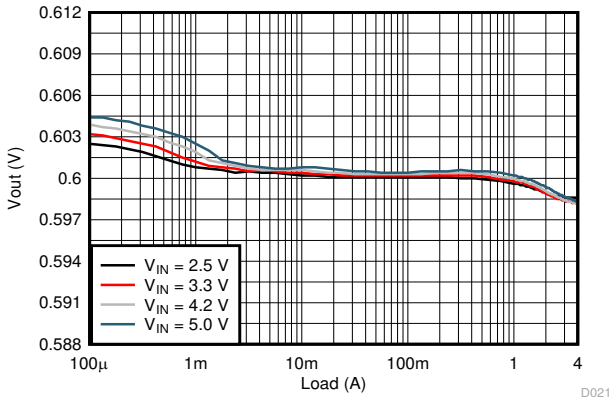
8.2.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 1.8V, T_A = 25°C, BOM = 表 8-2, unless otherwise noted.



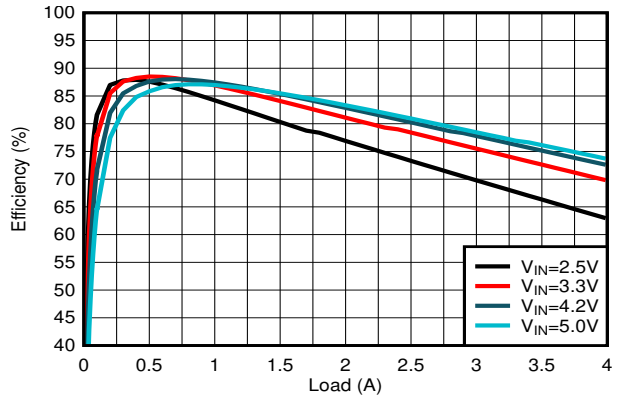
V_{OUT} = 0.6V

図 8-3. Efficiency



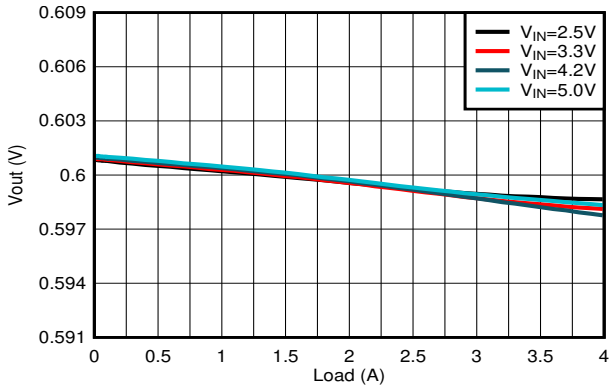
V_{OUT} = 0.6V

図 8-4. Load Regulation



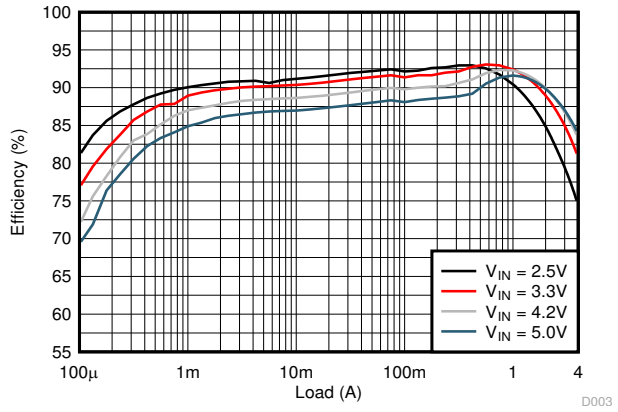
V_{OUT} = 0.6V F-PWM devices

図 8-5. PWM Efficiency



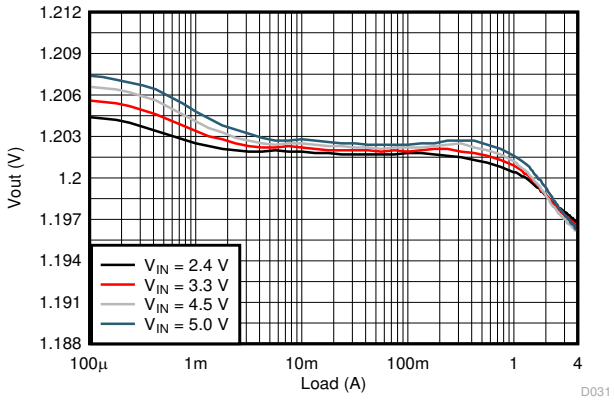
V_{OUT} = 0.6V F-PWM devices

図 8-6. Load Regulation



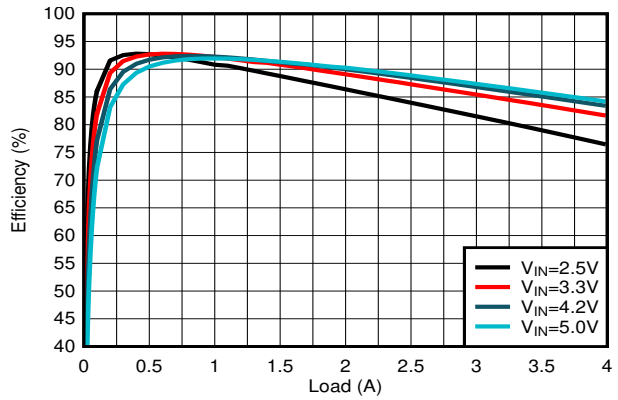
V_{OUT} = 1.2V

図 8-7. Efficiency



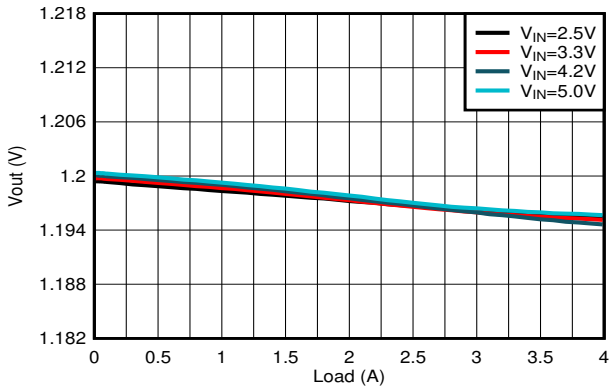
V_{OUT} = 1.2V

図 8-8. Load Regulation



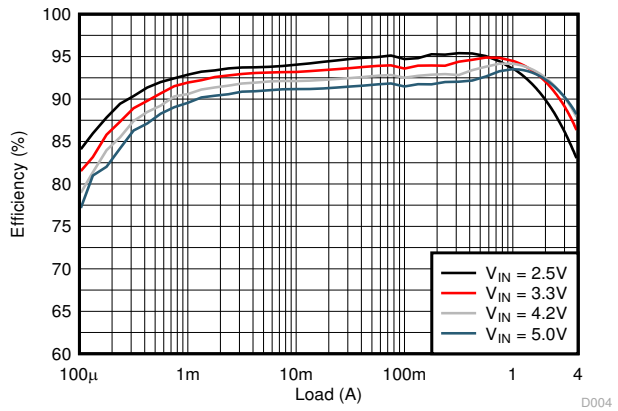
V_{OUT} = 1.2V F-PWM devices

図 8-9. PWM Efficiency



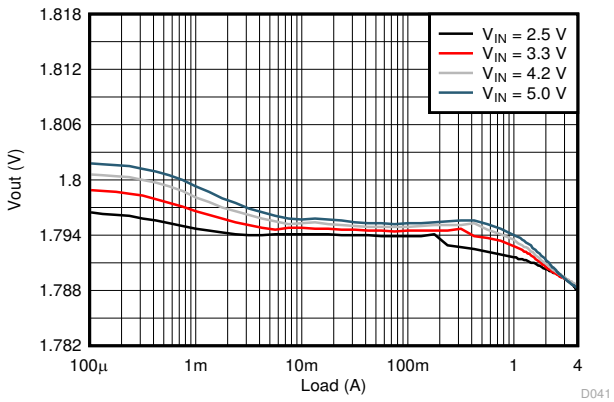
V_{OUT} = 1.2V F-PWM devices

図 8-10. Load Regulation



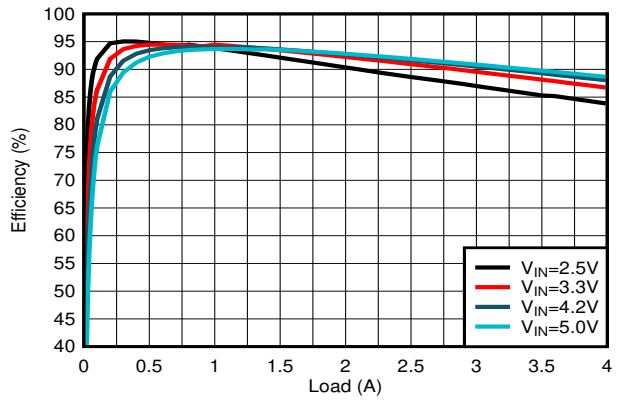
V_{OUT} = 1.8V

図 8-11. Efficiency



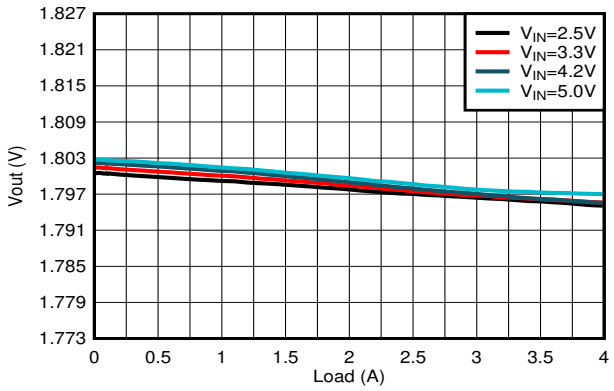
V_{OUT} = 1.8V

図 8-12. Load Regulation



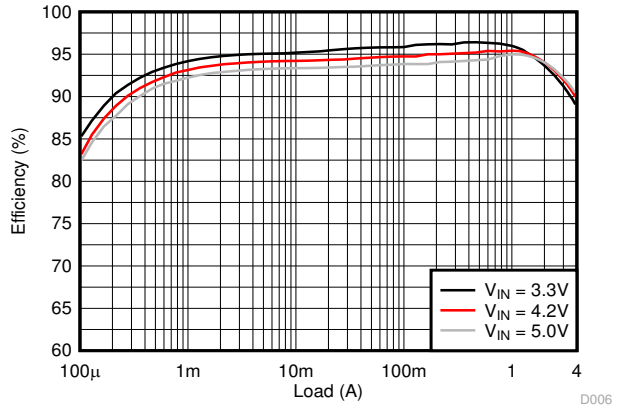
V_{OUT} = 1.8V F-PWM devices

図 8-13. PWM Efficiency



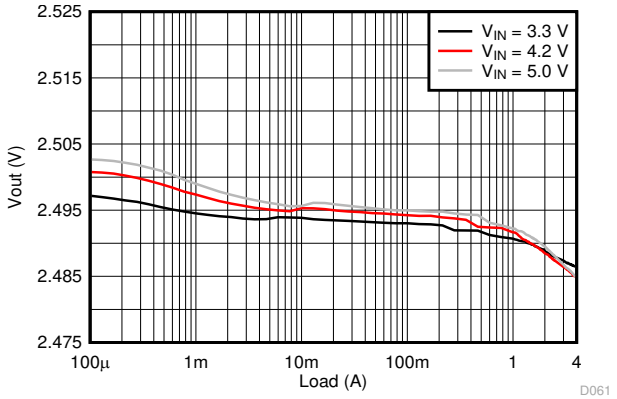
V_{OUT} = 1.8V F-PWM devices

図 8-14. Load Regulation



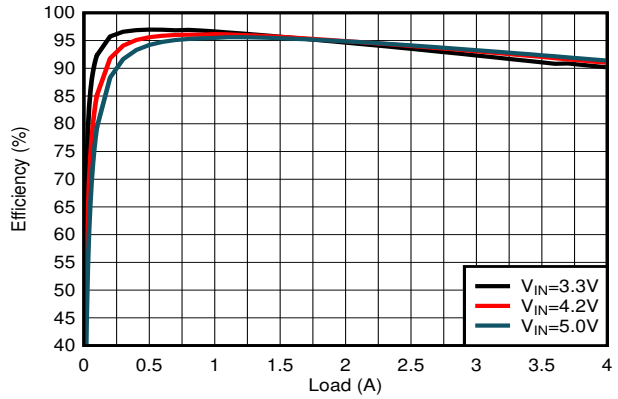
V_{OUT} = 2.5V

図 8-15. Efficiency



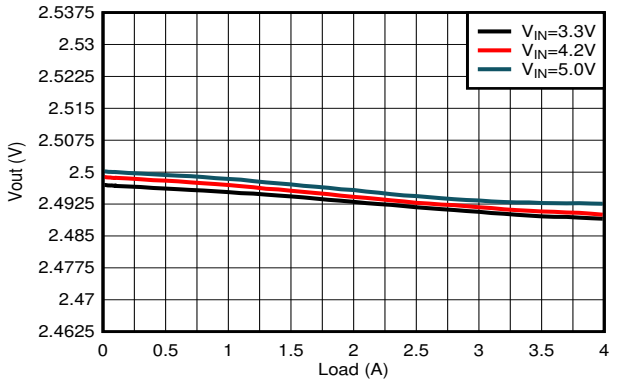
V_{OUT} = 2.5V

図 8-16. Load Regulation



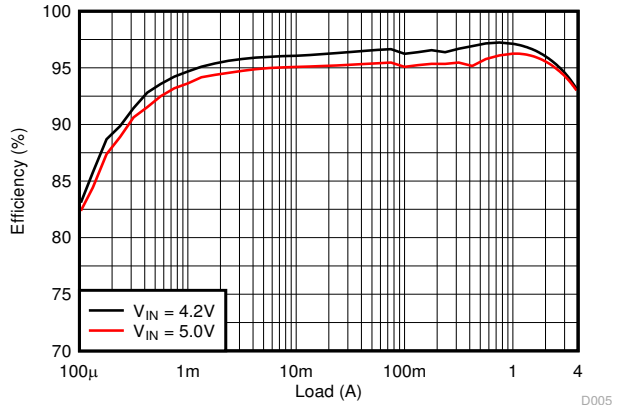
V_{OUT} = 2.5V F-PWM devices

図 8-17. PWM Efficiency



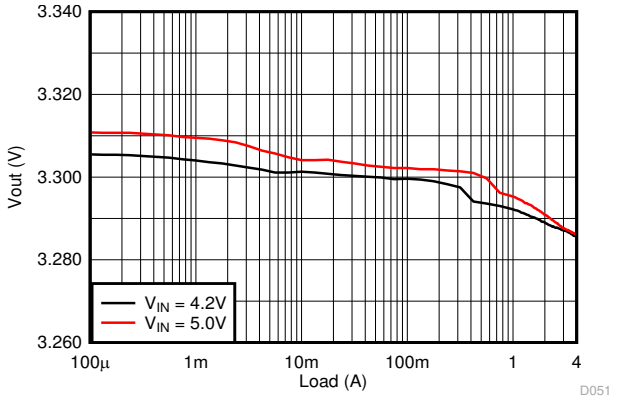
V_{OUT} = 2.5V F-PWM devices

図 8-18. Load Regulation



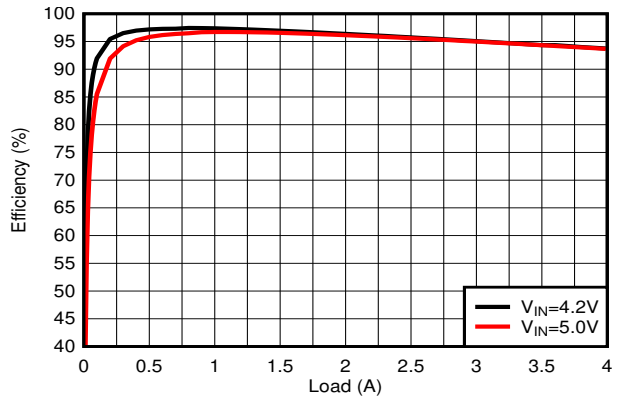
V_{OUT} = 3.3V

図 8-19. Efficiency



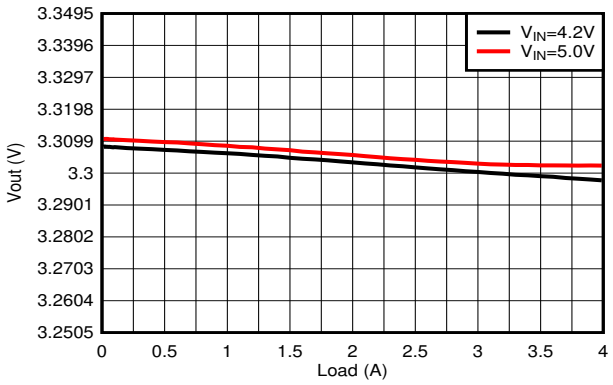
V_{OUT} = 3.3V

図 8-20. Load Regulation



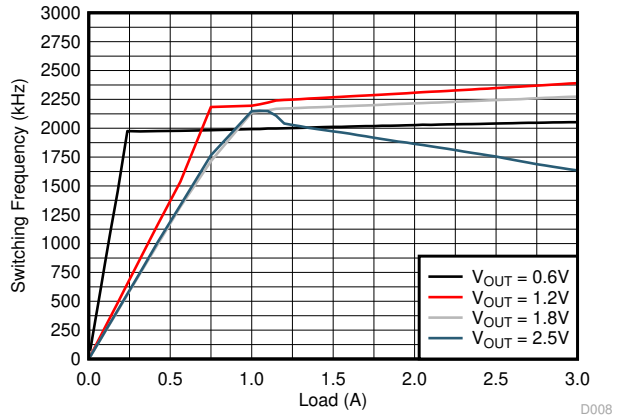
V_{OUT} = 3.3V F-PWM devices

図 8-21. PWM Efficiency



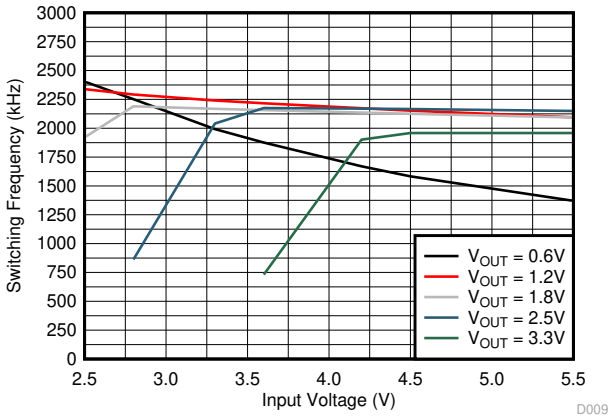
V_{OUT} = 3.3V F-PWM devices

図 8-22. Load Regulation



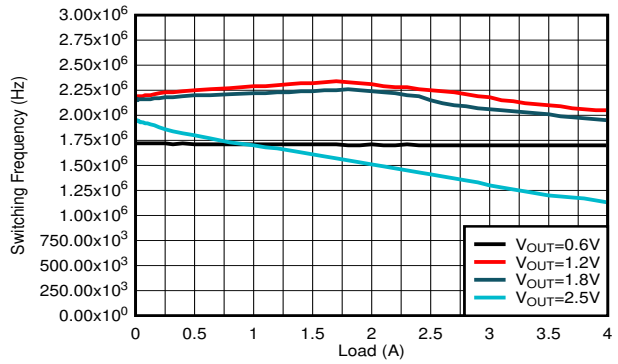
V_{IN} = 3.3V TPS62824, TPS62825, TPS62826

図 8-23. Switching Frequency



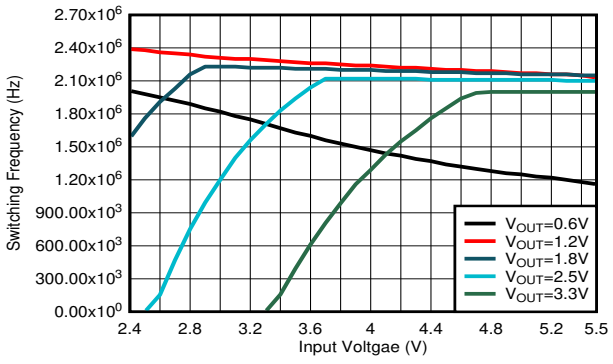
I_{OUT} = 1.0A TPS62824, TPS62825, TPS62826

図 8-24. Switching Frequency



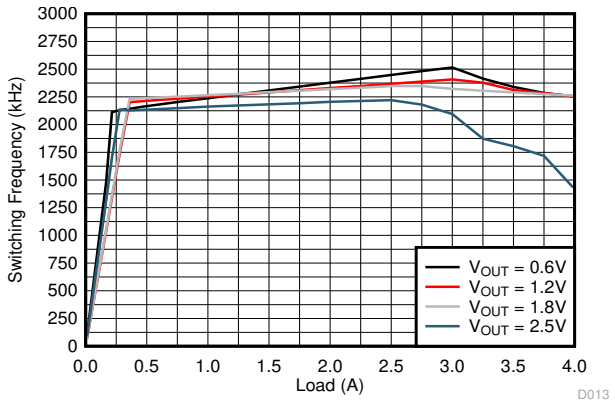
V_{IN} = 3.3V TPS62824A/5A/6A/7A

図 8-25. Switching Frequency



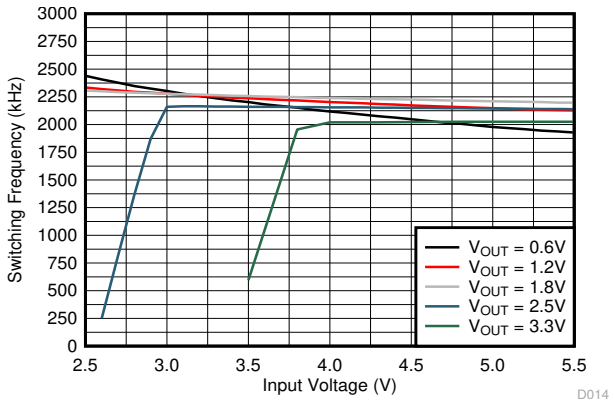
I_{OUT} = 1.0A TPS62824A/5A/6A/7A

図 8-26. Switching Frequency



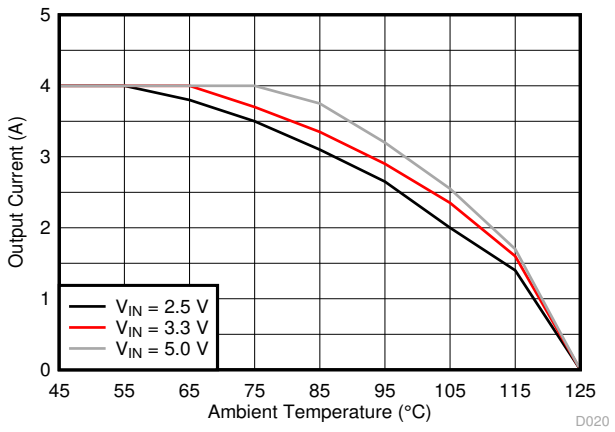
V_{IN} = 3.3V TPS62827

図 8-27. Switching Frequency



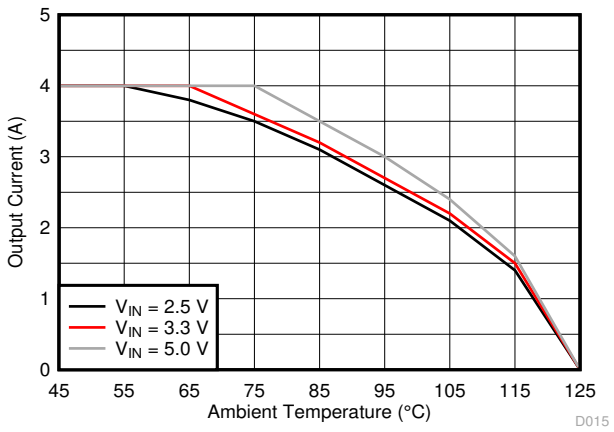
I_{OUT} = 1.0A TPS62827

図 8-28. Switching Frequency



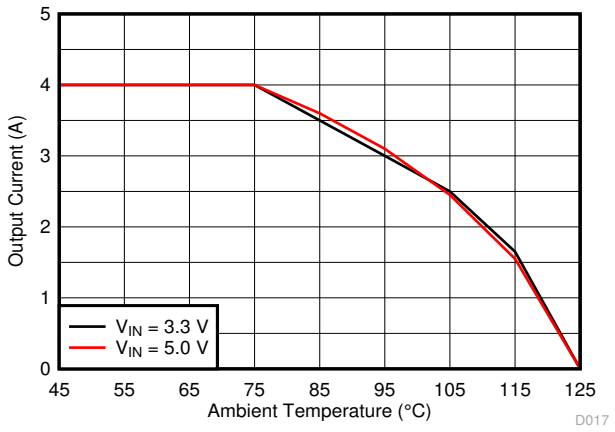
V_{OUT} = 1.2V θ_{JA}= 71.4°C/W

図 8-29. Thermal Derating



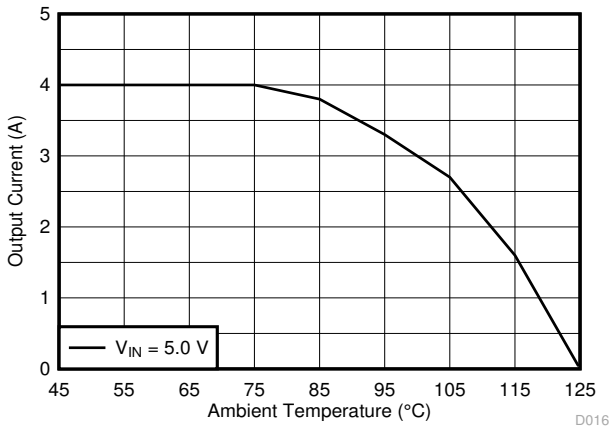
V_{OUT} = 1.8V θ_{JA}= 71.4°C/W

図 8-30. Thermal Derating



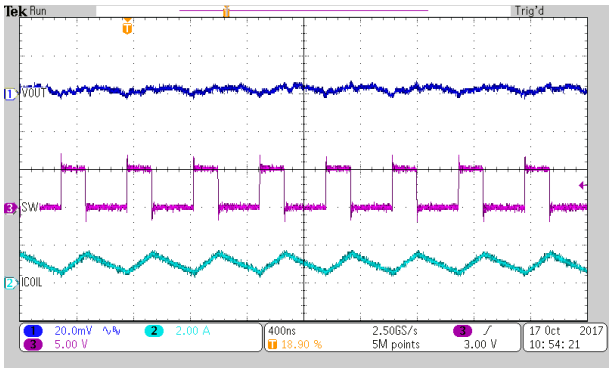
V_{OUT} = 2.5V θ_{JA}= 71.4°C/W

図 8-31. Thermal Derating



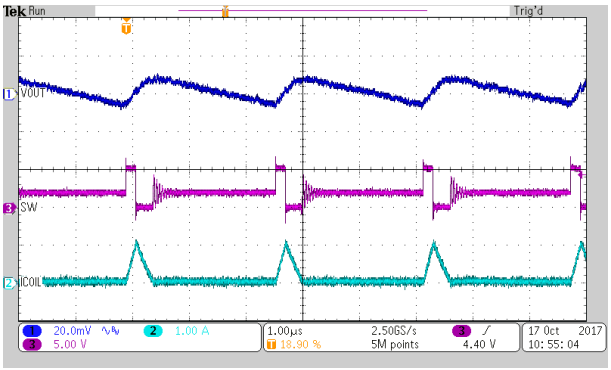
V_{OUT} = 3.3V θ_{JA}= 71.4°C/W

図 8-32. Thermal Derating



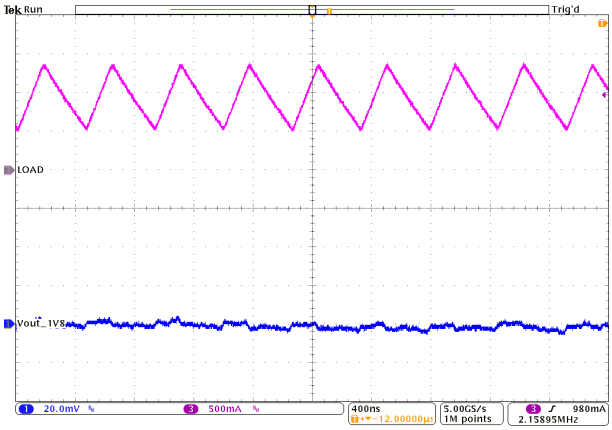
I_{OUT} = 1.0A TPS62824/5/6/7

図 8-33. PWM Operation



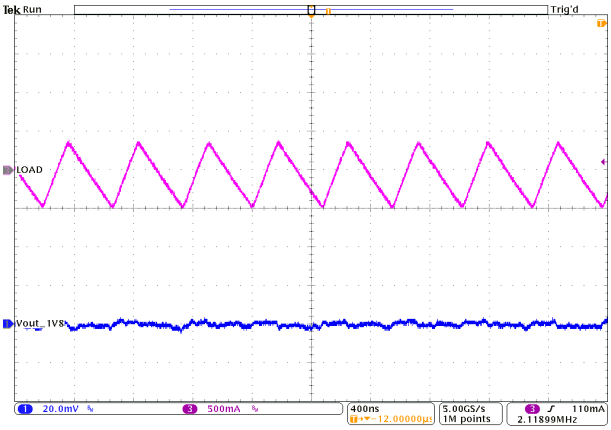
I_{OUT} = 0.1A TPS62824/5/6/7

図 8-34. PSM Operation



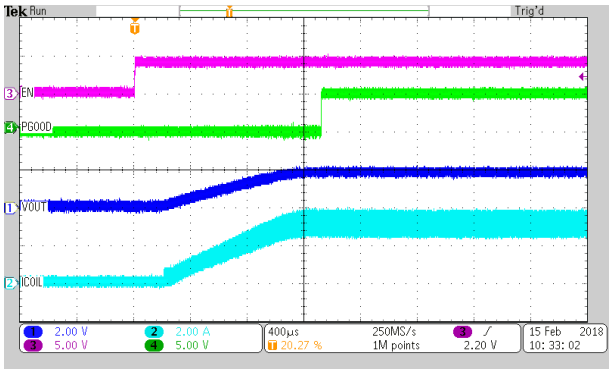
I_{OUT} = 1.0A TPS62824A/5A/6A/7A

図 8-35. PWM Operation at F-PWM



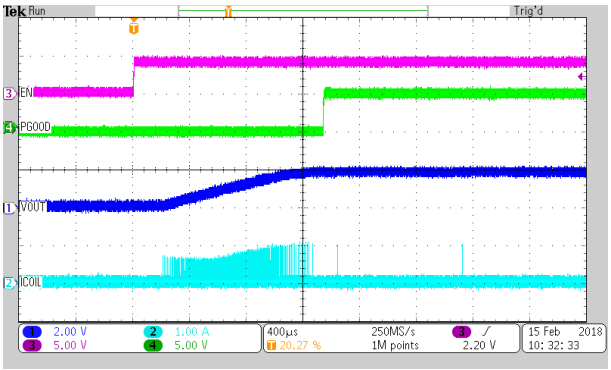
No load TPS62824A/5A/6A/7A

図 8-36. PWM Operation at F-PWM



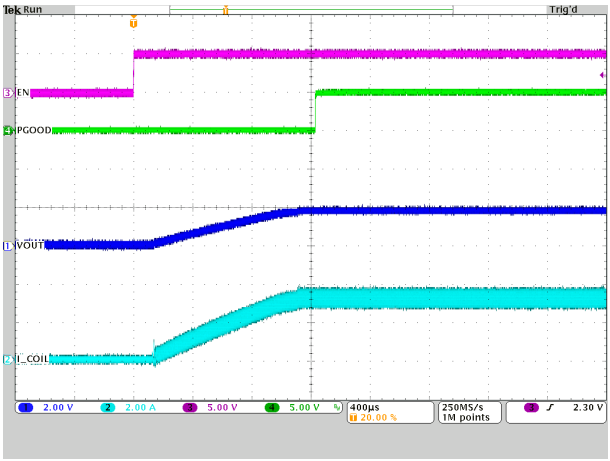
Load = 0.6Ω TPS62826

図 8-37. Start-Up With Load



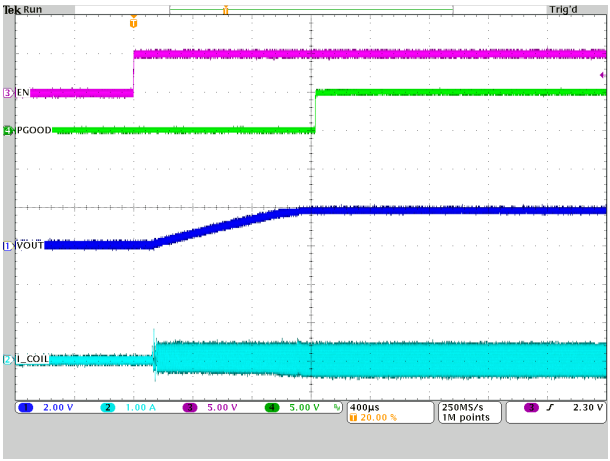
TPS62824/5/6

図 8-38. Start-Up With No Load



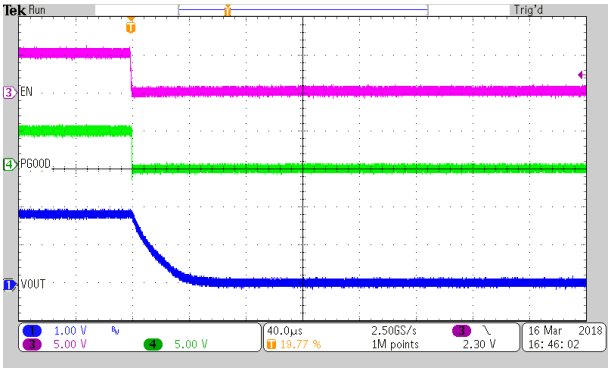
Load = 0.6Ω TPS62826A/7A

図 8-39. Start-Up With Load



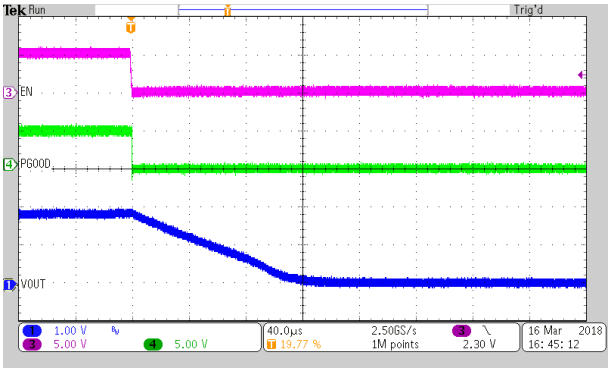
TPS62824A/5A/6A/7A

図 8-40. Start-Up With No Load



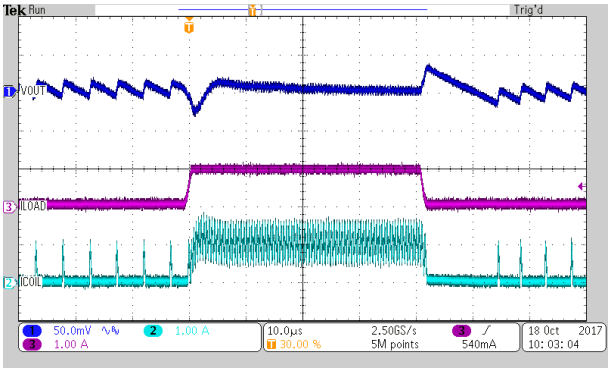
Load = 1.8Ω TPS6282x

図 8-41. Disable, Active Output Discharge



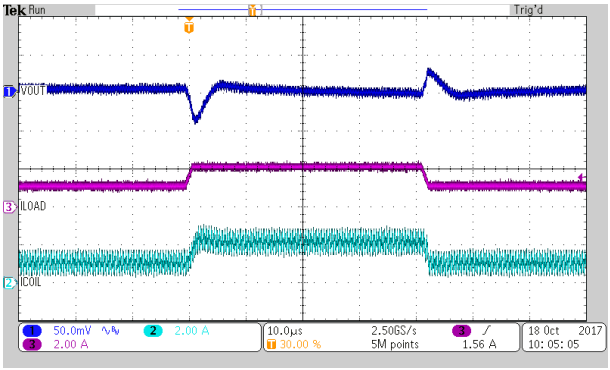
TPS6282x

図 8-42. Disable, Active Output Discharge at No Load



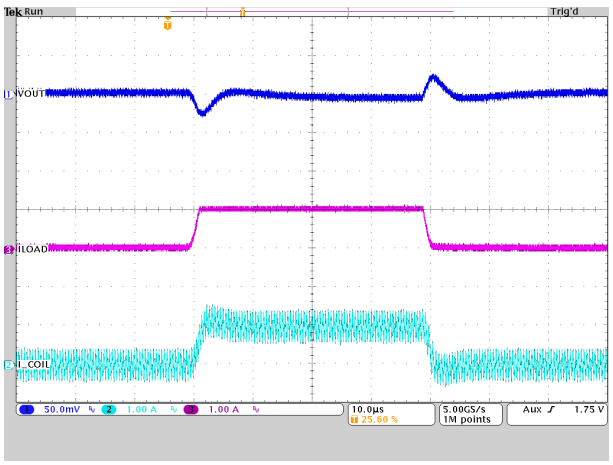
I_{OUT} = 0.05A to 1A TPS62824/5/6/7

図 8-43. Load Transient



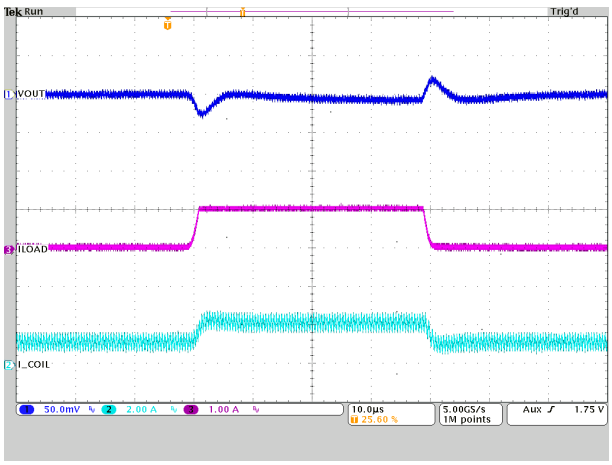
I_{OUT} = 1A to 2A TPS62825/6/7

図 8-44. Load Transient



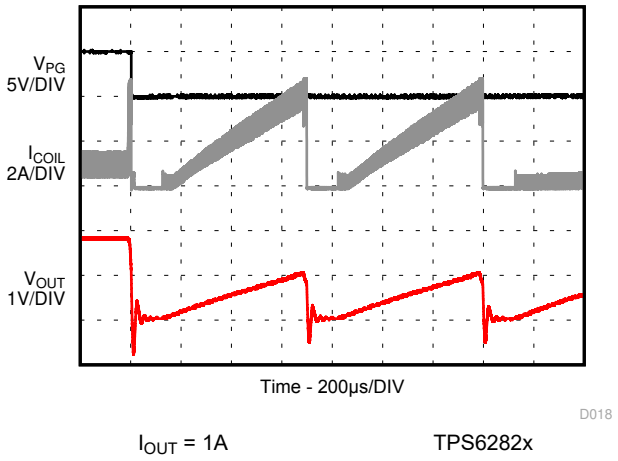
I_{OUT} = 0.05A to 1A TPS62824A/5A/6A/7A

図 8-45. Load Transient



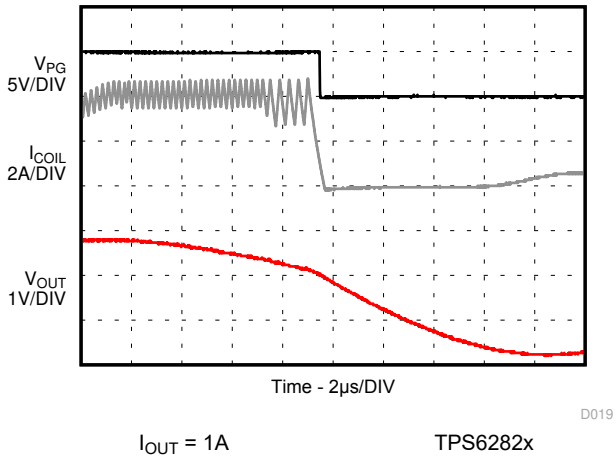
I_{OUT} = 1A to 2A TPS62825A/6A/7A

図 8-46. Load Transient



I_{OUT} = 1A TPS6282x

図 8-47. HICCUP Short-Circuit Protection



I_{OUT} = 1A TPS6282x

図 8-48. HICCUP Short-Circuit Protection (Zoom In)

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See *Layout Example* for the recommended PCB layout.

- Place the input, output capacitors and the inductor as close as possible to the IC. This placement keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- Note that the sense traces connected to FB is a signal trace. Take special care to avoid noise being induced. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors must be made at the output capacitor.
- Refer to *Layout Example* for an example of component placement, routing, and thermal design.

8.4.2 Layout Example

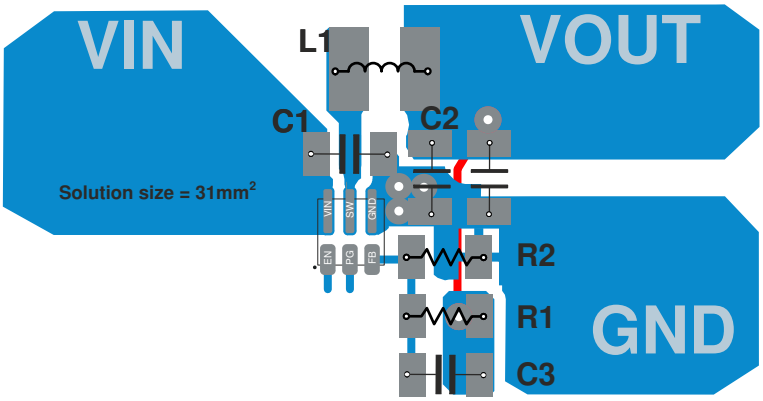


図 8-49. PCB Layout Recommendation

8.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in *Thermal Information* provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note and *Semiconductor and IC Package Thermal Metrics* application note.

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS6282x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision H (August 2023) to Revision I (March 2024)	Page
• Added foot note to include turnoff behavior	4
• Updated incorrect Power good upper threshold (swapped rising/falling)	5
• Updated description of start-up figures to show correct device versions	15

Changes from Revision G (March 2022) to Revision H (August 2023)	Page
• モジュールの提案に TPSM82823 を追加	1
• 式の書式を変更	1
• 文書全体にわたって画像から 4 方向接続を削除	1
• DCS-Control から商標を削除	1
• 最初のページの表を更新	1
• Added an SW pin voltage specification at PFM mode in the *Absolute Maximum Ratings* table	4
• Added the *Absolute Maximum Ratings* standard table note	4

Changes from Revision F (September 2021) to Revision G (March 2022)	Page
• データシートのタイトルから「1.5mm × 1.5mm QFN パッケージで供給」を削除	1

Changes from Revision E (December 2020) to Revision F (September 2021)	Page
• Changed the status of the TPS62824DMQ to Production Data	3
• Added the TPS6282533	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62824ADMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	JM	Samples
TPS62824DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	JL	Samples
TPS6282518DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
TPS6282518DMQT	ACTIVE	VSON-HR	DMQ	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
TPS6282533DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	L1	Samples
TPS62825ADMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	JN	Samples
TPS62825DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CI	Samples
TPS62825DMQT	ACTIVE	VSON-HR	DMQ	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CI	Samples
TPS6282618DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CK	Samples
TPS6282618DMQT	ACTIVE	VSON-HR	DMQ	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CK	Samples
TPS62826ADMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	JO	Samples
TPS62826DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CL	Samples
TPS62826DMQT	ACTIVE	VSON-HR	DMQ	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	CL	Samples
TPS62827ADMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	JP	Samples
TPS62827DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	EH	Samples
TPS62827DMQT	ACTIVE	VSON-HR	DMQ	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	EH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

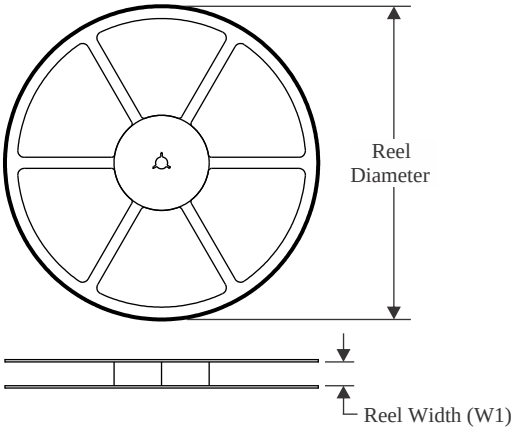
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

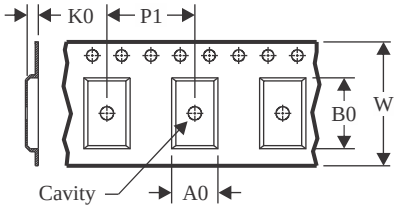
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

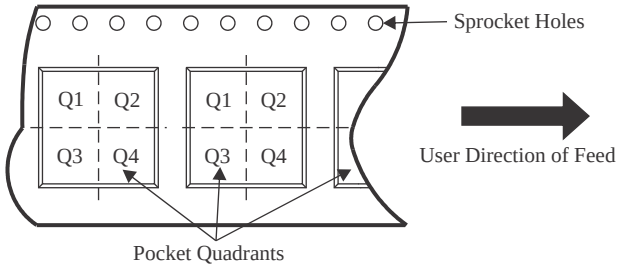


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

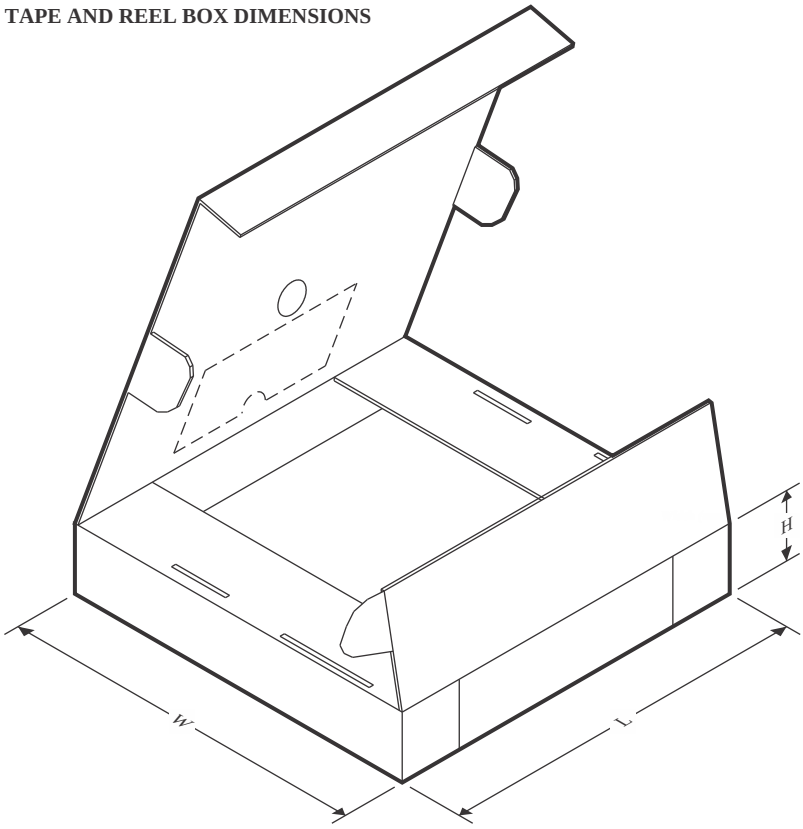


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62824DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS6282518DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS6282518DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS6282533DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS62825ADMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS62825DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS6282618DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS6282618DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2
TPS62826ADMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62827DMQT	VSON-HR	DMQ	6	250	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

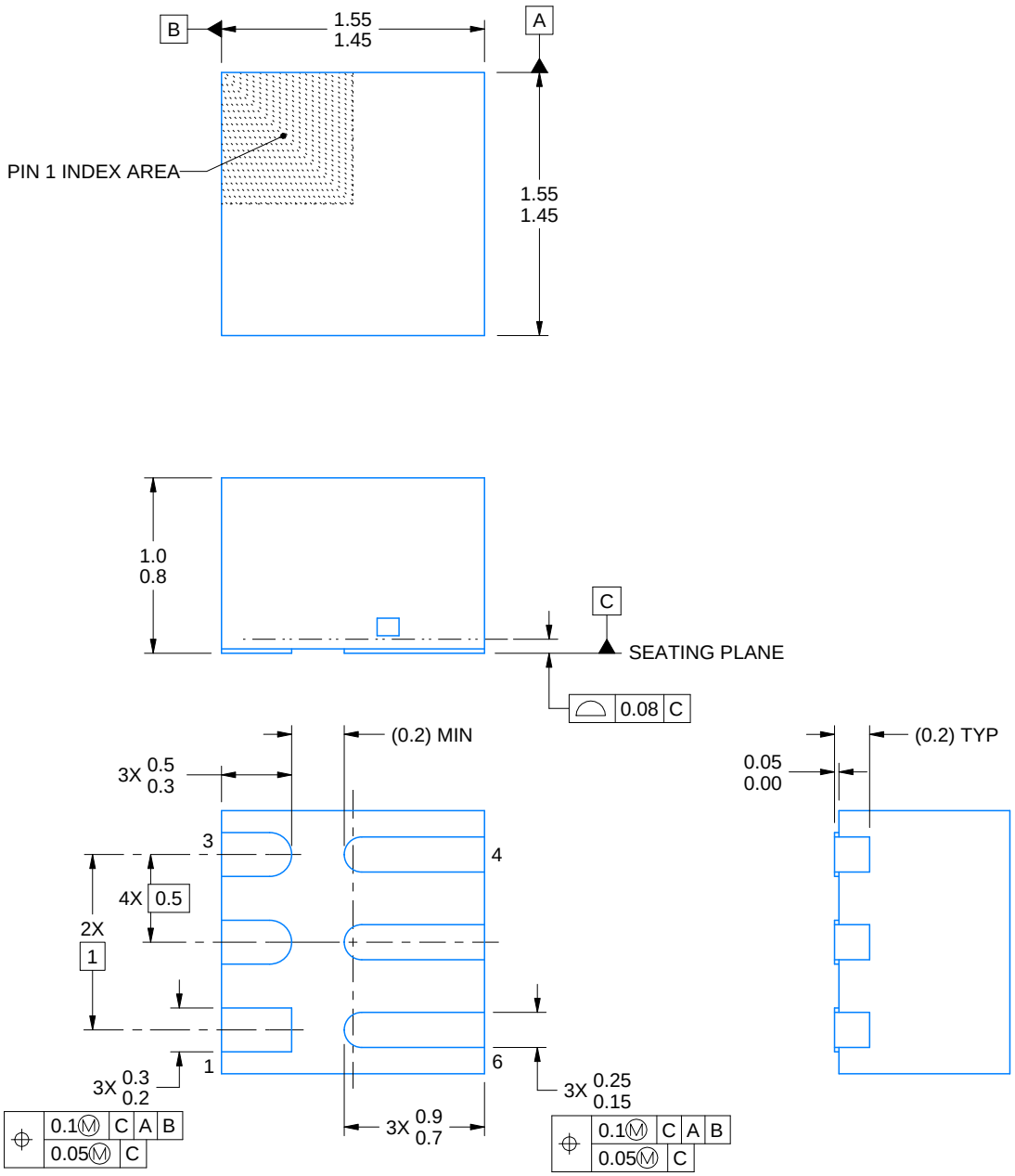
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62824DMQR	VSON-HR	DMQ	6	3000	341.0	182.0	80.0
TPS6282518DMQR	VSON-HR	DMQ	6	3000	210.0	185.0	35.0
TPS6282518DMQT	VSON-HR	DMQ	6	250	210.0	185.0	35.0
TPS6282533DMQR	VSON-HR	DMQ	6	3000	182.0	182.0	20.0
TPS62825ADMQR	VSON-HR	DMQ	6	3000	210.0	185.0	35.0
TPS62825DMQR	VSON-HR	DMQ	6	3000	210.0	185.0	35.0
TPS6282618DMQR	VSON-HR	DMQ	6	3000	341.0	182.0	80.0
TPS6282618DMQT	VSON-HR	DMQ	6	250	341.0	182.0	80.0
TPS62826ADMQR	VSON-HR	DMQ	6	3000	210.0	185.0	35.0
TPS62827DMQT	VSON-HR	DMQ	6	250	341.0	182.0	80.0

PACKAGE OUTLINE

DMQ0006A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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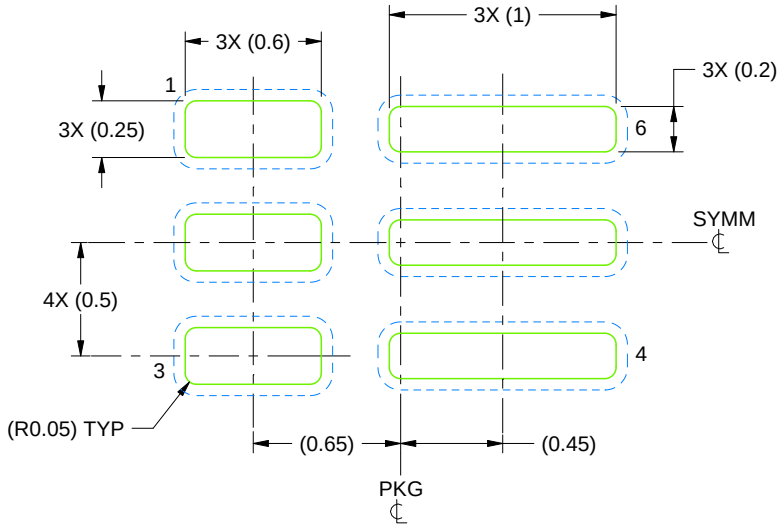
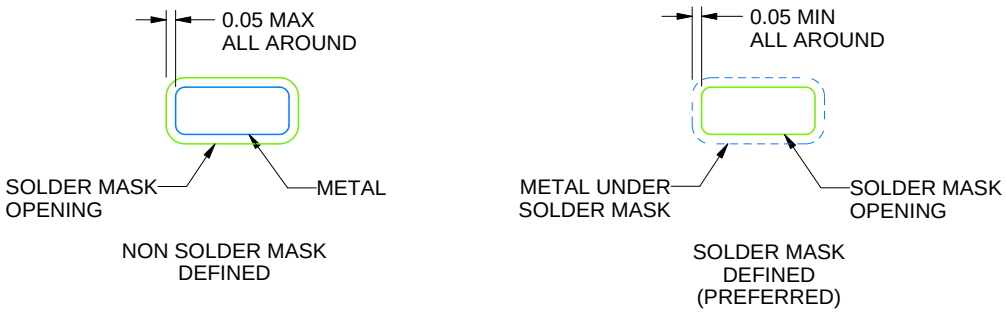
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

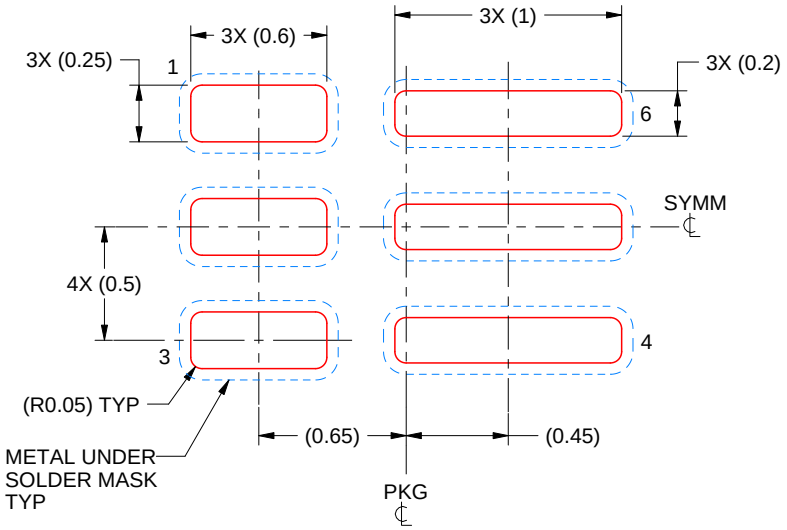


SOLDER MASK DETAILS

4222645/E 09/2023

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:30X

4222645/E 09/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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