TPS65263 入力電圧 4.5V～18V、出力電流 3A / 2A / 2A、トリプル同期整流降圧型コンバータ、I²C 制御の動的電圧スケーリング搭載

1 特長

- 動作入力電圧範囲 4.5～18V、連続出力電流 3A / 2A / 2A
- 各バックの出力電圧は I²C 制御の 7 ビット VID により 0.68～1.95V の範囲で 10mV 刻みにプログラム可能
- I²C により VID 電圧遷移スルーレートを制御
- I²C により各バックのパワー・グッド・ステータス、過電流警告を読み出し
- I²C によりバックのダイ温度警告を読み出し
- I²C 互換のインターフェイス、スタンダード・モード (100kHz) とファスト・モード (400kHz) に対応
- 帰還基準電圧：0.6V±1%
- 600kHz の固定周波数
- 各バックに専用のイネーブル・ピンとソフト・スタート・ピン
- 過熱保護

2 アプリケーション

- DTV LCD パネル
- セット・トップ・ボックス
- ホーム・ゲートウェイおよびアクセス・ポイント・ネットワーク
- 監視機器

3 概要

TPS65263 には、入力電圧範囲が 4.5V～18V と広く、5、9、12、15V の電力バスまたはバッテリから動作するほとんどの中間バス電圧を網羅したトリプル同期整流降圧型コンバータが組み込まれています。定周波数ピーク電流モードを備えたこのコンバータは、目的のアプリケーションに合わせてシステムを最適化するための選択肢を設計者に与えると同時に、アプリケーションが簡単になるよう設計されています。このデバイスは 600kHz で動作し、buck1 と buck2 / buck3 の位相差は 180 度です（buck2 と buck3 は同相動作）。

各バックの初期スタートアップ電圧は、外付けのフィードバック抵抗で設定できます。各バックの出力電圧は、0.68～1.95V の範囲で、I²C 制御の 7 ビット VID を使用して 10mV 刻みで動的に設定可能です。VID 電圧の遷移スルーレートは、I²C バスによる 3 ビットの制御によりプログラム可能なため、VID 電圧遷移時のオーバーシュートやアンダーシュートを最適化できます。

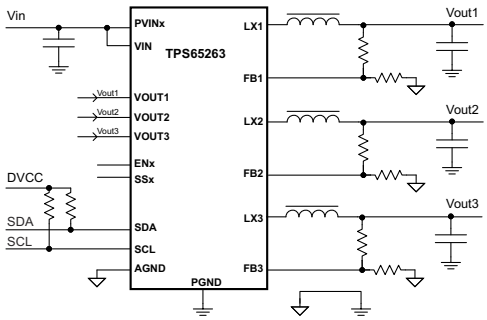
TPS65263 の各バックについて、出力電圧のイネーブルとディセーブル、軽負荷時のパルス・スキップ・モード (PSM) または強制連続電流モード (FCC) の設定、パワー・グッド・ステータス、過電流警告、ダイ温度警告の読み出しを、I²C で制御できます。

TPS65263 には過電圧、過電流、短絡、過熱保護が搭載されています。

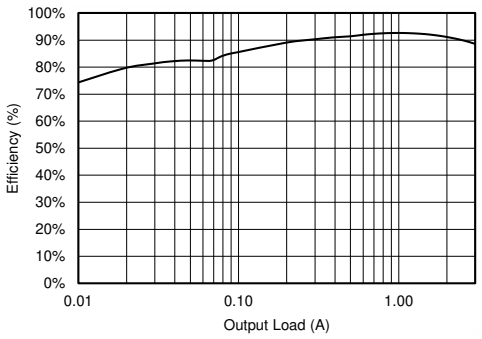
パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPS65263	RHB (VQFN、32)	5.00mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション



V_{IN} = 12V、V_{OUT} = 3.3V

効率と出力負荷との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (May 2023) to Revision C (May 2023)	Page
• Changed the value of capacitor from V7V pin to power ground in *V7V Low Dropout Regulator and Bootstrap*	20

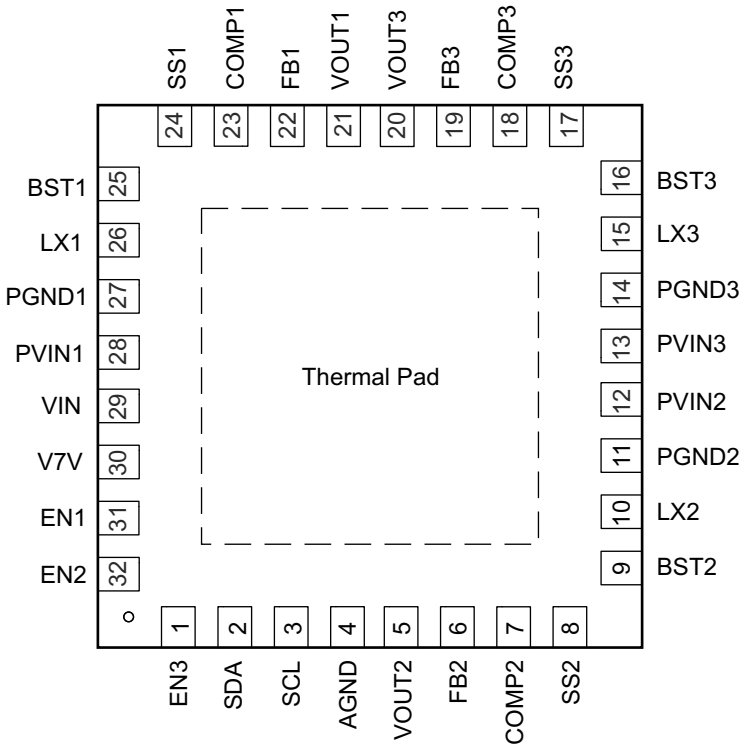
Changes from Revision A (September 2014) to Revision B (May 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Changed the description of V7V pin in 表 6-1	4
• Renamed *Handling Ratings* to *ESD Ratings*	6
• Moved the storage temperature row in the *ESD Ratings* table to the *Absolute Maximum Ratings* table	6
• Changed the recommended value of capacitor from V7V pin to power ground in *V7V Low Dropout Regulator and Bootstrap*	20
• Changed all instances of legacy terminology to controller and target where I^2C is mentioned	23
• Changed the recommended value of C9 in the typical application schematic	29

Changes from Revision * (June 2014) to Revision A (September 2014)	Page
• デバイスのステータスを製品プレビューから量産データへ変更	1

5 Device Comparison Table

PART NUMBER	DESCRIPTION	COMMENTS
TPS65261/-1	4.5 to 18 V, triple bucks with input voltage power failure indicator	Triple bucks 3-A/2-A/2-A output current, features an open drain RESET signal to monitor input power failure, automatic power sequencing
TPS65262/-1	4.5 to 18 V, triple bucks with dual adjustable LDOs	Triple bucks 3-A/1-A/1-A output current, automatic power sequencing. dual LDOs: TPS65262, 200 mA/100 mA; TPS65262-1, 350 mA/150 mA
TPS65287	4.5 to 18 V, triple bucks with power switch and push button control	Triple bucks 3-A/2-A/2-A output current, up to 2.1-A USB power with over current setting by external resistor, push button control for intelligent system power-on/ power-off operation
TPS65288	4.5 to 18 V, triple bucks with dual power switches	Triple bucks 3-A/2-A/2-A output current, 2 USB power switches current limiting at typical 1.2 A (0.8, 1.0, 1.4, 1.6, 1.8, 2.0, 2.2 A available with manufacture trim options)

6 Pin Configuration and Functions



(There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.)

図 6-1. RHB Package 32 Pin Top View

表 6-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
EN3	1	Enable for buck3. Float to enable. Can use this pin to adjust the input undervoltage lockout (UVLO) of buck3 with a resistor divider.
SDA	2	I^2C interface data pin
SCL	3	I^2C interface clock pin
AGND	4	Analog ground common to buck controllers and other analog circuits. It must be routed separately from high current power grounds to the (–) terminal of bypass capacitor of input voltage VIN.
VOUT2	5	Buck2 output voltage sense pin.
FB2	6	Feedback Kelvin sensing pin for buck2 output voltage. Connect this pin to buck2 resistor divider.
COMP2	7	Error amplifier output and Loop compensation pin for buck2. Connect a series resistor and capacitor to compensate the control loop of buck2 with peak current PWM mode.
SS2	8	Soft-start and tracking input for buck2. An internal 5uA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
BST2	9	Boot strapped supply to the high side floating gate driver in buck2. Connect a capacitor (recommend 47nF) from BST2 pin to LX2 pin.
LX2	10	Switching node connection to the inductor and bootstrap capacitor for buck2. The voltage swing at this pin is from a diode voltage below the ground up to PVIN2 voltage.
PGND2	11	Power ground connection of buck2. Connect PGND2 pin as close as practical to the (–) terminal of PVIN2 input ceramic capacitor.
PVIN2	12	Input power supply for buck2. Connect PVIN2 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 µF).

表 6-1. Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
PVIN3	13	Input power supply for buck3. Connect PVIN3 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
PGND3	14	Power ground connection of buck3. Connect PGND3 pin as close as practical to the (–) terminal of PVIN3 input ceramic capacitor.
LX3	15	Switching node connection to the inductor and bootstrap capacitor for buck3. The voltage swing at this pin is from a diode voltage below the ground up to PVIN3 voltage.
BST3	16	Boot strapped supply to the high side floating gate driver in buck3. Connect a capacitor (recommend 47 nF) from BST3 pin to LX3 pin.
SS3	17	Soft-start and tracking input for buck3. An internal 5-µA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
COMP3	18	Error amplifier output and Loop compensation pin for buck3. Connect a series resistor and capacitor to compensate the control loop of buck3 with peak current PWM mode.
FB3	19	Feedback Kelvin sensing pin for buck3 output voltage. Connect this pin to buck3 resistor divider.
VOUT3	20	Buck3 output voltage sense pin.
VOUT1	21	Buck1 output voltage sense pin.
FB1	22	Feedback Kelvin sensing pin for buck1 output voltage. Connect this pin to buck1 resistor divider.
COMP1	23	Error amplifier output and Loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck1 with peak current PWM mode.
SS1	24	Soft-start and tracking input for buck1. An internal 5-µA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
BST1	25	Boot strapped supply to the high side floating gate driver in buck1. Connect a capacitor (recommend 47 nF) from BST1 pin to LX1 pin.
LX1	26	Switching node connection to the inductor and bootstrap capacitor for buck1. The voltage swing at this pin is from a diode voltage below the ground up to PVIN1 voltage.
PGND1	27	Power ground connection of Buck1. Connect PGND1 pin as close as practical to the (–) terminal of PVIN1 input ceramic capacitor.
PVIN1	28	Input power supply for buck1. Connect PVIN1 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
VIN	29	Buck controller power supply.
V7V	30	Internal LDO for gate driver and internal controller. Connect a 10-µF capacitor from the pin to power ground.
EN1	31	Enable for buck1. Float to enable. Can use this pin to adjust the input UVLO of buck1 with a resistor divider.
EN2	32	Enable for buck2. Float to enable. Can use this pin to adjust the input UVLO of buck2 with a resistor divider.
PAD	—	There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	PVIN1, PVIN2, PVIN3,VIN	–0.3	20	V
	LX1, LX2, LX3 (maximum withstand voltage transient <20 ns)	–1.0	20	
	BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.3	7	
	EN1, EN2, EN3, V7V, VOUT1, VOUT2, VOUT3, SCL, SDA	–0.3	7	
	FB1, FB2, FB3, COMP1, COMP2, COMP3, SS1, SS2, SS3	–0.3	3.6	
	AGND, PGND1, PGND2, PGND3	–0.3	0.3	
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature range	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	PVIN1, PVIN2, PVIN3,VIN	4.5	18	V
	LX1, LX2, LX3 (Maximum withstand voltage transient <20 ns)	–0.8	18	
	BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.1	6.8	
	EN1, EN2, EN3, V7V, VOUT1, VOUT2, VOUT3, SCL, SDA	–0.1	6.3	
	FB1, FB2, FB3, COMP1, COMP2, COMP3, SS1, SS2, SS3	–0.1	3	
T_A	Operating ambient temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS65263 RHB (32 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	7.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range		4.5		18	V
UVLO	VIN undervoltage lockout	VIN rising	4	4.25	4.5	V
		VIN falling	3.5	3.75	4	V
		Hysteresis		500		mV
IDD_{SDN}	Shutdown supply current	EN1 = EN2 = EN3 = 0 V		8		µA
IDD_{Q_NSW}	Input quiescent current without buck1/2/3 switching	EN1 = EN2 = EN3 = 5 V, FB1 = FB2 = FB3 = 0.8 V		740		µA
IDD_{Q_NSW1}		EN1 = 5 V, EN2 = EN3 = 0 V, FB1 = 0.8 V		360		µA
IDD_{Q_NSW2}		EN2 = 5 V, EN1 = EN3 = 0 V, FB2 = 0.8 V		380		µA
IDD_{Q_NSW3}		EN3 = 5 V, EN1 = EN2 = 0 V, FB3 = 0.8 V		380		µA
V_{7V}	V7V LDO output voltage	V_{7V} load current = 0 A	6	6.3	6.6	V
I_{OCP_V7V}	V7V LDO current limit			185		mA
FEEDBACK VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{COMP} = 1.2 V, T_J = 25°C	0.595	0.6	0.605	V
		V_{COMP} = 1.2 V, T_J = –40°C to 125°C	0.594	0.6	0.606	V
$V_{LINEREG\_BUCK}$	Line regulation-DC(1)	I_{OUT1} = 1.5 A, I_{OUT2} = 1 A, I_{OUT3} = 1 A, 5 V < PVINx < 18 V		0.002		%/V
$V_{LOADREG\_BUCK}$	Load regulation-DC(1)	I_{OUTx} = (10-100%) × I_{OUTx_max}		0.02		%/A
BUCK1, BUCK2, BUCK3						
V_{ENXH}	EN1/2/3 high level input voltage			1.2	1.26	V
V_{ENXL}	EN1/2/3 low level input voltage		1.1	1.15		V
I_{ENX1}	EN1/2/3 pullup current	ENx = 1 V		3.8		µA
I_{ENX2}	EN1/2/3 pullup current	ENx = 1.5 V		6.8		µA
I_{ENhys}	Hysteresis current			3		µA
I_{SSX}	Soft start charging current		4.3	5	6	µA
T_{ON_MIN}	Minimum on time			80	100	ns
G_{m_EA}	Error amplifier trans-conductance	–2 µA < I_{COMPX} < 2 µA		300		µS
$G_{m\_PS1/2/3}$	COMP1/2/3 voltage to inductor current Gm(1)	I_{LX} = 0.5 A		7.4		A/V
I_{LIMIT1}	Buck1 peak inductor current limit		4.5	5.5	6.5	A
$I_{LIMITSOURCE1}$	Buck1 low side source current limit			4.4		A
$I_{LIMITSINK1}$	Buck1 low side sink current limit			1.3		
$I_{LIMIT2/3}$	buck2/3 peak inductor current limit		2.6	3.3	4	A
$I_{LIMITSOURCE2/3}$	Buck2/3 low side source current limit			2.5		
$I_{LIMITSINK2/3}$	Buck2/3 low side sink current limit			1		A
Rdson_HS1	Buck1 high-side switch resistance	VIN = 12 V		105		mΩ
Rdson_LS1	Buck1 low-side switch resistance	VIN = 12 V		65		mΩ
Rdson_HS2	Buck2 high-side switch resistance	VIN = 12 V		140		mΩ
Rdson_LS2	Buck2 low-side switch resistance	VIN = 12 V		90		mΩ
Rdson_HS3	Buck3 high-side switch resistance	VIN = 12 V		140		mΩ
Rdson_LS3	Buck3 low-side switch resistance	VIN = 12 V		90		mΩ
HICCUP TIMING						
T_{Hiccup_wait}	Over current wait time(1)			0.5		ms
T_{Hiccup_re}	Hiccup time before restart(1)			14		ms
OSCILLATOR						
F_{SW}	Switching frequency		550	600	650	kHz

7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL PROTECTION						
T_{TRIP_OTP}	Thermal protection trip point(1)	Temperature rising		160		°C
T_{HYST_OTP}	Thermal protection Hysteresis(1)	Hysteresis		20		°C
I²C INTERFACE						
Addr	Address(2)	0x60H				
V_{IH} SDA,SCL	Input high voltage				2	V
V_{IL} SDA,SCL	Input low voltage		0.4			V
I_I	Input current	SDA, SCL, V_I = 0.4 to 4.5 V	–10		10	µA
V_{OL} SDA	SDA output low voltage	SDA open drain, I_{OL} = 4 mA			0.4	V
$f_{(SCL)}$	Maximum SCL clock frequency(2)		400			kHz
t_{BUF}	Bus free time between a STOP and START condition(2)		1.3			µs
t_{HD_STA}	Hold time (repeated) START condition(2)		0.6			µs
t_{SU_STO}	Setup time for STOP condition(2)		0.6			µs
t_{LOW}	LOW Period of the SCL Clock(2)		1.3			µs
t_{HIGH}	HIGH period of the SCL clock(2)		0.6			µs
t_{SU_STA}	Setup time for a repeated START condition(2)		0.6			µs
t_{SU_DAT}	Data setup time(2)		0.1			µs
t_{HD_DAT}	Data hold time(2)		0		0.9	µs
t_{RCL}	Rise time of SCL signal(2)	Capacitance of one bus line (pF)	20 + 0.1CB		300	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT(2)	Capacitance of one bus line (pF)	20 + 0.1CB		300	ns
t_{FCL}	Fall time of SCL signal(2)	Capacitance of one bus line (pF)	20 + 0.1CB		300	ns
t_{RDA}	Rise time of SDA signal(2)	Capacitance of one bus line (pF)	20 + 0.1CB		300	ns
t_{FDA}	Fall time of SDA signal(2)	Capacitance of one bus line (pF)	20 + 0.1CB		300	ns
C_B	Capacitance of bus line(SCL and SDA)(2)				400	pF

(1) Lab validation result.
(2) Not production tested.

7.6 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, V_{OUT1}= 1.5 V, V_{OUT2}= 1.2 V, V_{OUT3}= 2.5 V, F_{SW} = 600 kHz (unless otherwise noted)

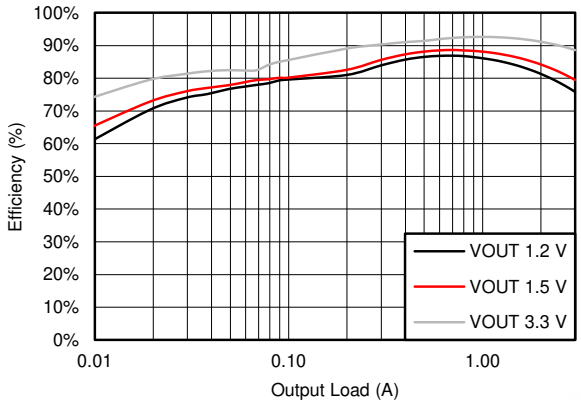


図 7-1. BUCK1 Efficiency

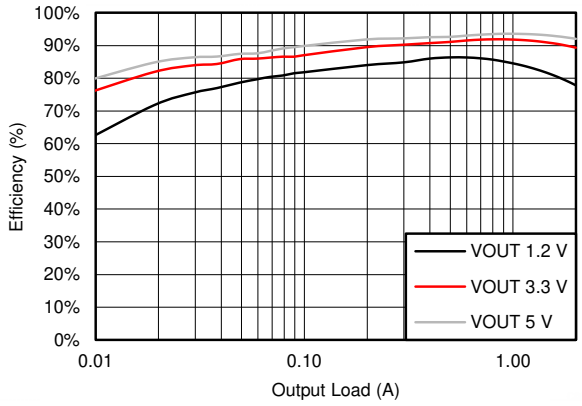


図 7-2. BUCK2 Efficiency

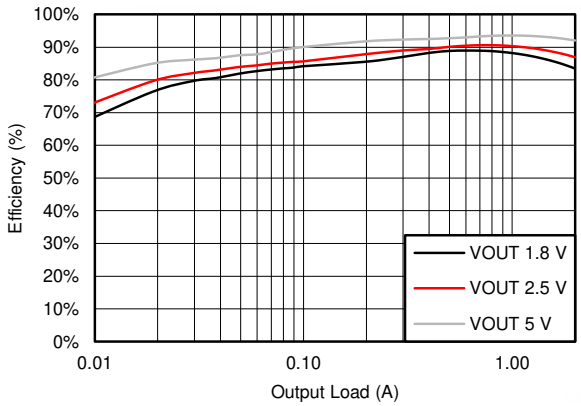


図 7-3. BUCK3 Efficiency

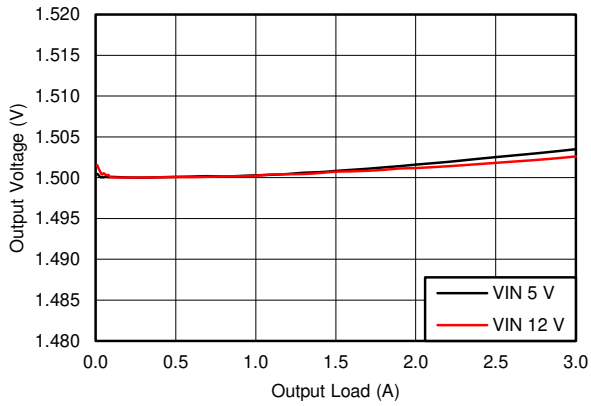


図 7-4. BUCK1 Load Regulation

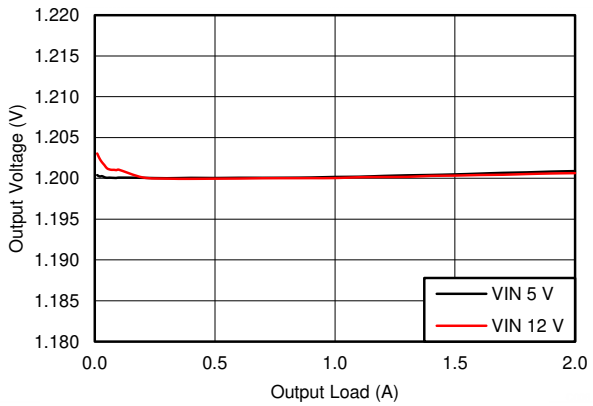


図 7-5. BUCK2 Load Regulation

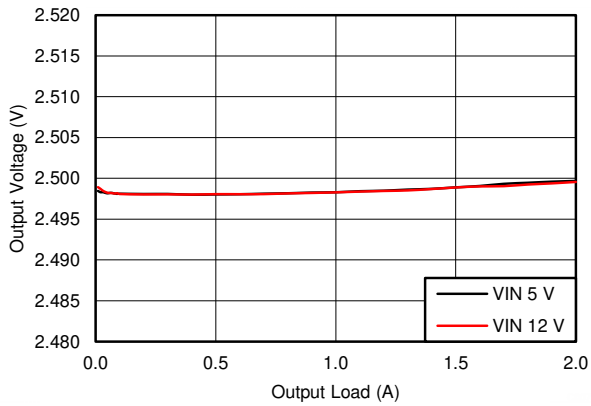


図 7-6. BUCK3 Load Regulation

7.6 Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, V_{OUT1}= 1.5 V, V_{OUT2}= 1.2 V, V_{OUT3}= 2.5 V, F_{SW} = 600 kHz (unless otherwise noted)

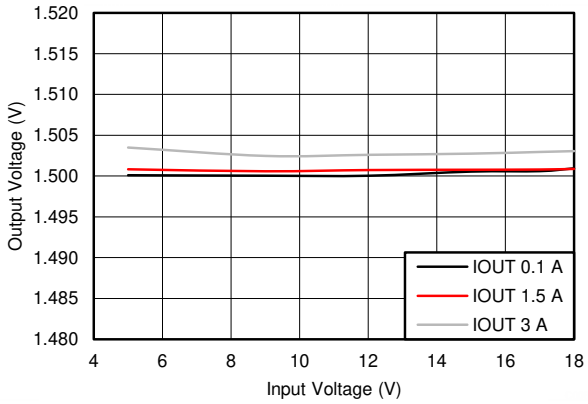


図 7-7. BUCK1, Line Regulation

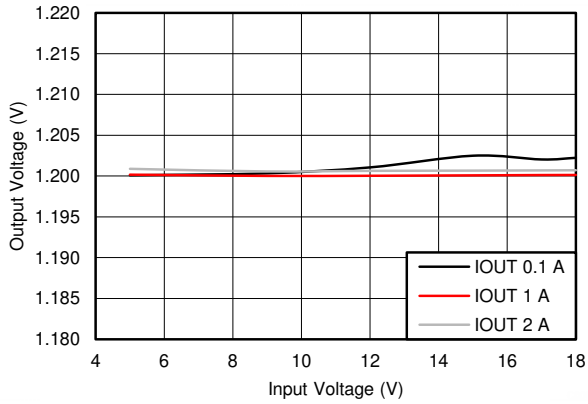


図 7-8. BUCK2, Line Regulation

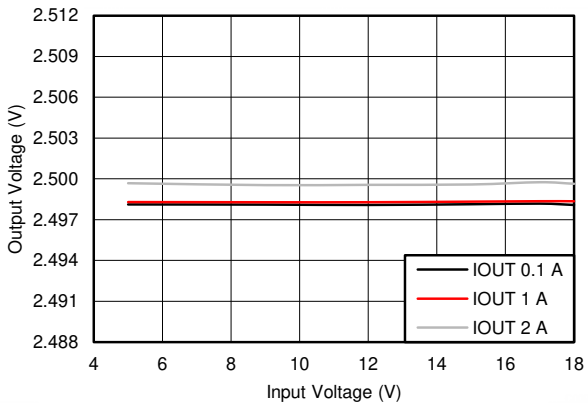


図 7-9. BUCK3, Line Regulation

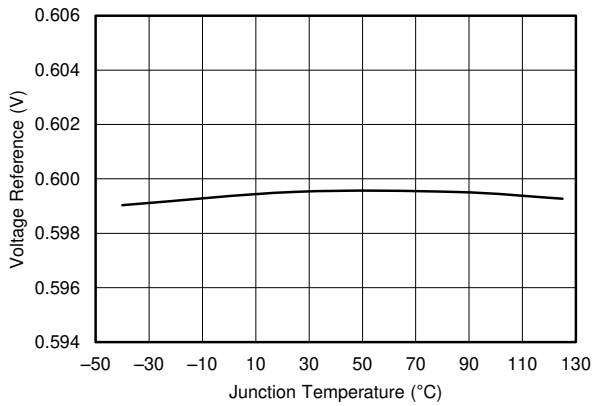


図 7-10. Voltage Reference vs Temperature

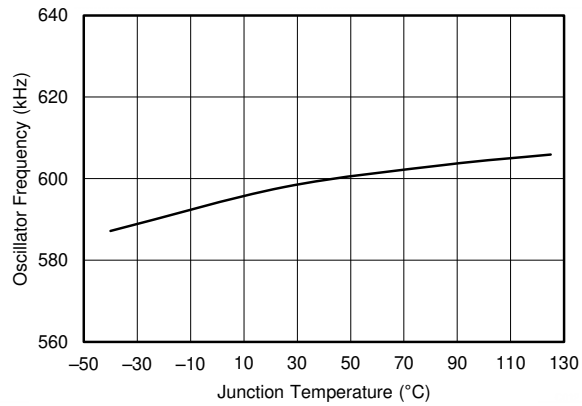


図 7-11. Oscillator Reference vs Temperature

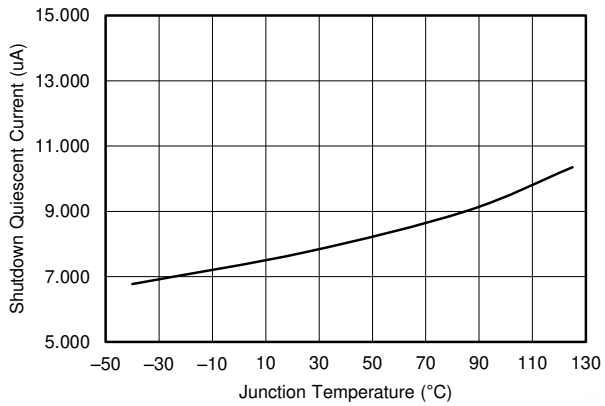


図 7-12. Shurtdown Quiescent Current vs Temperature

7.6 Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, V_{OUT1}= 1.5 V, V_{OUT2}= 1.2 V, V_{OUT3}= 2.5 V, F_{SW} = 600 kHz (unless otherwise noted)

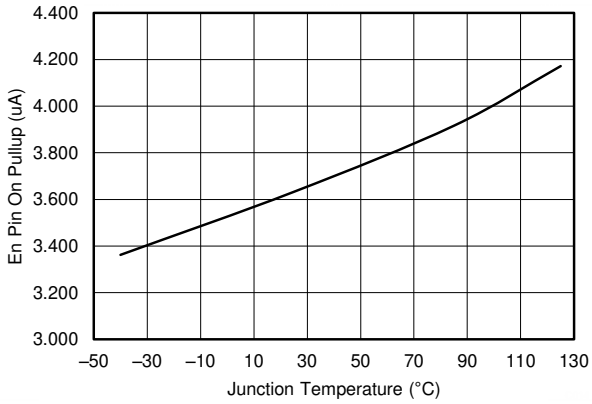


図 7-13. EN Pin Pullup Current vs Temperature, EN = 1 V

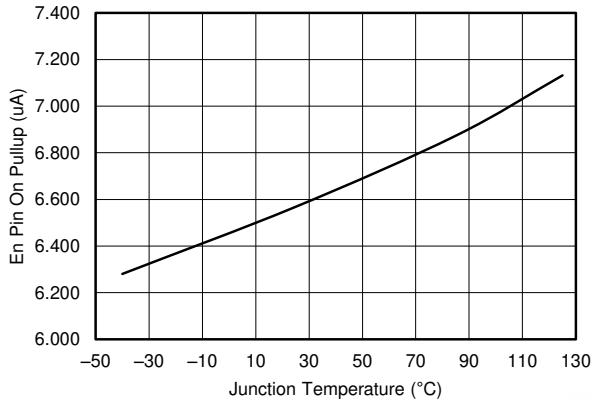


図 7-14. EN Pin Pullup Current vs Temperature, EN = 1.5 V

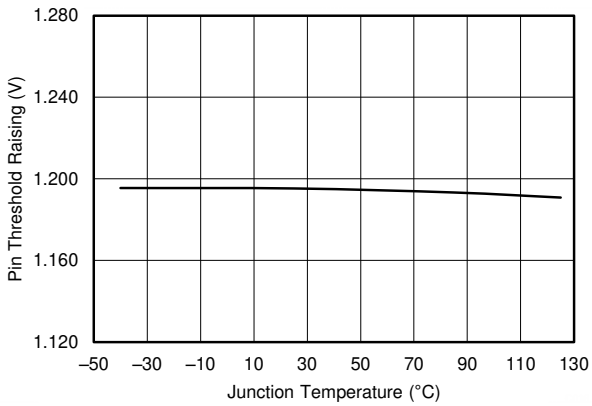


図 7-15. EN Pin Threshold Rising vs Temperature

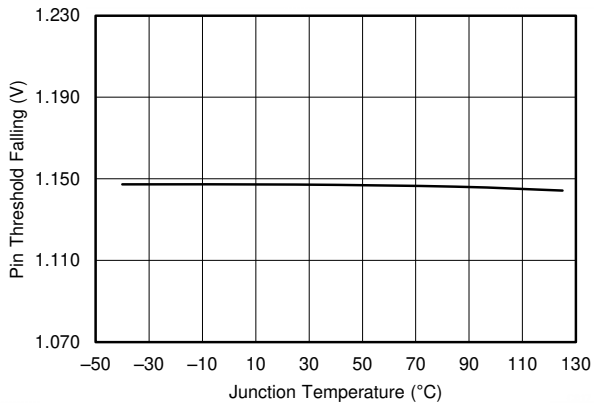


図 7-16. EN Pin Threshold Falling vs Temperature

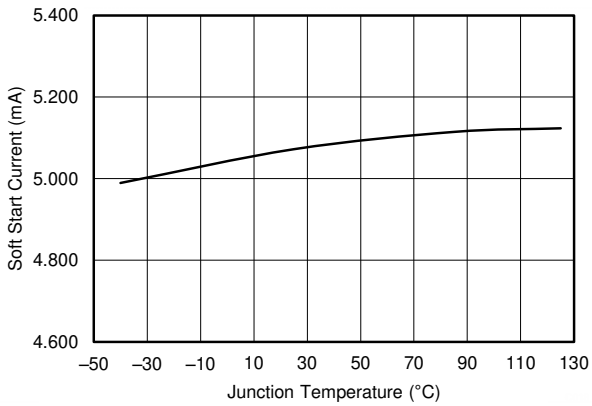


図 7-17. SS Pin Charge Current vs Temperature

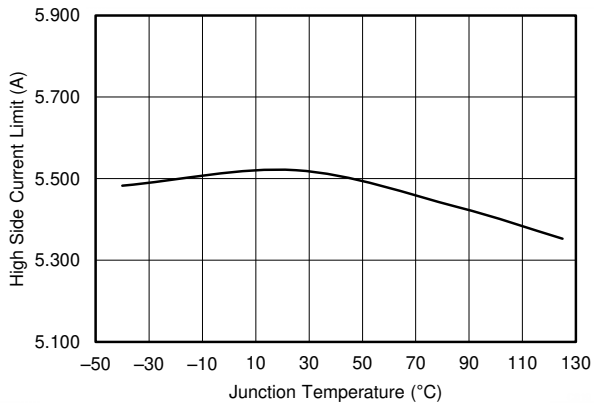


図 7-18. Buck1 High-Side Current Limit vs Temperature

7.6 Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, V_{OUT1}= 1.5 V, V_{OUT2}= 1.2 V, V_{OUT3}= 2.5 V, F_{SW} = 600 kHz (unless otherwise noted)

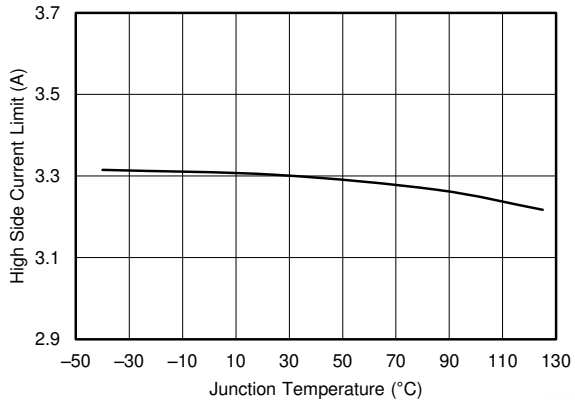


図 7-19. Buck2 High-Side Current Limit vs Temperature

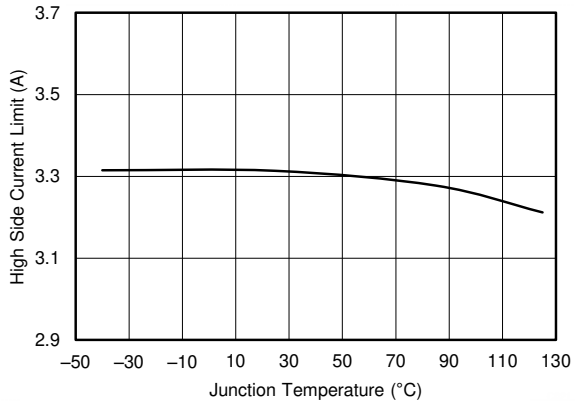


図 7-20. Buck3 High-Side Current Limit vs Temperature

8 Detailed Description

8.1 Overview

The TPS65263 is a monolithic triple synchronous step-down (buck) converter with 3-A/2-A/2-A output currents. A wide 4.5- to 18-V input supply voltage range encompasses most intermediate bus voltages operating off 5-, 9-, 12-, or 15-V power bus. The feedback voltage reference for each buck is 0.6 V. Each buck is independent with dedicated enable, soft-start and loop compensation pins.

The TPS65263 is equipped with I^2C compatible bus for communication with SoC to control buck converters. Through I^2C interface, SoC can enable or disable the buck converters, set output voltage and read status registers. External feedback divider resistors can set the initial start-up voltage of the buck regulators. After the voltage identification VID DAC is updated via the I^2C, output voltage of the buck regulators can be independently programmed with 7 bits VID from 0.68 to 1.95 V in 10-mV voltage step resolution. Output voltage of the buck regulators transition begins after the I^2C interface receives the command for GO bit in command register.

In light loading condition, the converter will automatically operate in pulse skipping mode (PSM) to save power. The PSM can be disabled through I^2C so that the converter operates at continuous current mode (CCM) at light load with a fixed frequency for optimized output ripple.

The TPS65263 implements a constant frequency, peak current mode control that simplifies external loop compensation. The device operates in fixed 600 kHz. The switch clock of buck1 is 180° out-of-phase operation from the clock of buck2 and buck3 channels to reduce input current ripple, input capacitor size and power supply induced noise.

The TPS65263 is designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 4.25 V. The ENx pin also can be used to adjust the input voltage UVLO with an external resistor divider. In addition, the ENx pin has an internal 3.8-µA current source, so the EN pin can be floating for automatically powering up the converters.

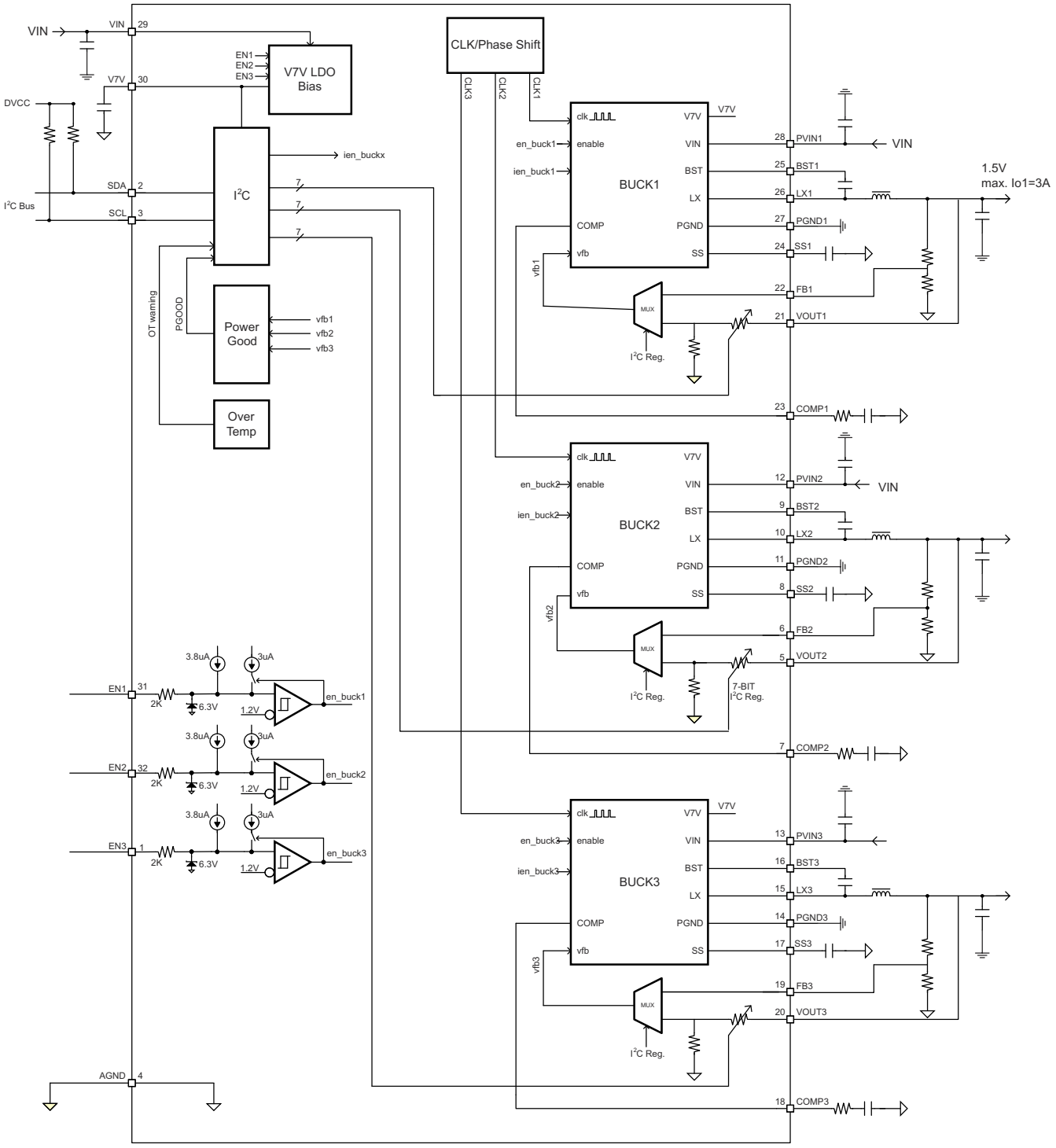
The TPS65263 reduces the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LX pins. A UVLO circuit monitors the bootstrap capacitor voltage VBST-VLX in each buck. When VBST-VLX voltage drops to the threshold, LX pin is pulled low to recharge the bootstrap capacitor. The TPS65263 can operate at 100% duty cycle as long as the bootstrap capacitor voltage is higher than the BOOT-LX UVLO threshold which is typically 2.1 V.

The TPS65263 has power good comparators with hysteresis, which monitor the output voltages through internal feedback voltages. I^2C can read the power good status with commanding register.

The SS (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider is connected the pin for soft start or voltage tracking.

The TPS65263 is protected from overload and over temperature fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the output is over, the high-side MOSFET is turned off until the internal feedback voltage is lower than 105% of the 0.6-V reference voltage. The TPS65263 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections to avoid inductor current runaway. If the overcurrent condition has lasted for more than the OC wait time (0.5ms typical), the converter will shut down and re-start after the hiccup time (14ms typical). The TPS65263 shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the TPS65263 will be restarted under control of the soft start circuit automatically.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjusting the Output Voltage

The output voltage of each buck is set with a resistor divider from the output of buck to the FB pin. TI recommends to use 1% tolerance or better resistors.

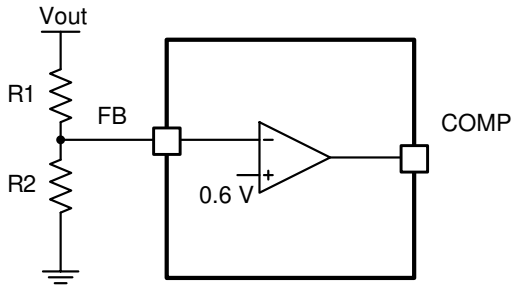


図 8-1. Voltage Divider Circuit

$$R_2 = R_1 \times \frac{0.6}{V_{out} - 0.6} \quad (1)$$

To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. The recommended resistor values are shown in 表 8-1.

表 8-1. Output Resistor Divider Selection

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

The output voltage of buck converter can be dynamically scaled by I^2C controlled 7-bit register VOUTx_SEL. Before I^2C communication, the output voltage is set with the resistor divider from the output of buck to the FB pin. When GO bit is set to 1 through I^2C interface, the buck converter switches external resistor divider to the internal resistor divider as shown in 図 8-2. The output voltage can be selected among 128 voltages with voltage identifications (VID) shown in 表 8-2. The output voltage range of dynamic voltage scaling is 0.68 to 1.95 V with 10-mV resolution of each voltage step.

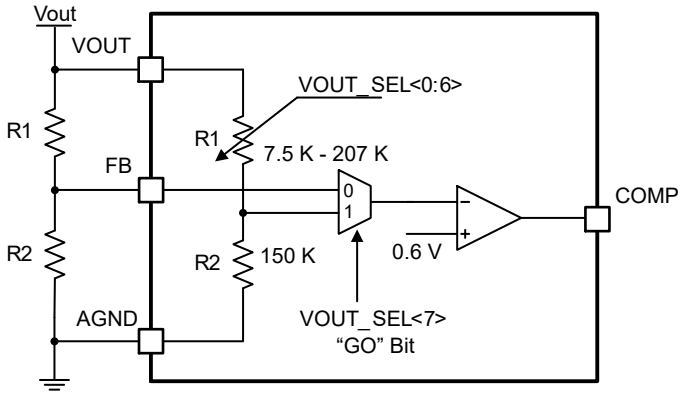


図 8-2. Voltage Divider Circuit

表 8-2. Vout Output Voltage Setting

OUT_SEL <7:0>	V_{OUT} (V)	VOUT_SEL <7:0>	V_{OUT} (V)	VOUT_SEL <7:0>	V_{OUT} (V)	VOUT_SEL <7:0>	V_{OUT} (V)
0	0.68	20	1	40	1.32	60	1.64
1	0.69	21	1.01	41	1.33	61	1.65
2	0.7	22	1.02	42	1.34	62	1.66
3	0.71	23	1.03	43	1.35	63	1.67
4	0.72	24	1.04	44	1.36	64	1.68
5	0.73	25	1.05	45	1.37	65	1.69
6	0.74	26	1.06	46	1.38	66	1.7
7	0.75	27	1.07	47	1.39	67	1.71
8	0.76	28	1.08	48	1.4	68	1.72
9	0.77	29	1.09	49	1.41	69	1.73
A	0.78	2A	1.1	4A	1.42	6A	1.74
B	0.79	2B	1.11	4B	1.43	6B	1.75
C	0.8	2C	1.12	4C	1.44	6C	1.76
D	0.81	2D	1.13	4D	1.45	6D	1.77
E	0.82	2E	1.14	4E	1.46	6E	1.78
F	0.83	2F	1.15	4F	1.47	6F	1.79
10	0.84	30	1.16	50	1.48	70	1.8
11	0.85	31	1.17	51	1.49	71	1.81
12	0.86	32	1.18	52	1.5	72	1.82
13	0.87	33	1.19	53	1.51	73	1.83
14	0.88	34	1.2	54	1.52	74	1.84
15	0.89	35	1.21	55	1.53	75	1.85
16	0.9	36	1.22	56	1.54	76	1.86
17	0.91	37	1.23	57	1.55	77	1.87
18	0.92	38	1.24	58	1.56	78	1.88
19	0.93	39	1.25	59	1.57	79	1.89
1A	0.94	3A	1.26	5A	1.58	7A	1.9
1B	0.95	3B	1.27	5B	1.59	7B	1.91
1C	0.96	3C	1.28	5C	1.6	7C	1.92
1D	0.97	3D	1.29	5D	1.61	7D	1.93
1E	0.98	3E	1.3	5E	1.62	7E	1.94

表 8-2. Vout Output Voltage Setting (continued)

OUT_SEL <7:0>	V_{OUT} (V)	VOUT_SEL <7:0>	V_{OUT} (V)	VOUT_SEL <7:0>	V_{OUT} (V)	VOUT_SEL <7:0>	V_{OUT} (V)
1F	0.99	3F	1.31	5F	1.63	7F	1.95

8.3.2 Enable and Adjusting UVLO

The EN1, EN2, and EN3 pin provide electrical on and off control of the device. When the EN1, EN2, EN3 pin voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500 mV. If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVINx, in split rail applications, then the ENx pin can be configured as shown in 図 8-3, 図 8-4, and 図 8-5 . When using the external UVLO function TI recommends to set the hysteresis to be greater than 500 mV.

The EN pin has a small pullup current Ip which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using 式 2 and 式 3.

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1\left(I_h + I_p\right)} \quad (3)$$

where

- I_h = 3 µA
- I_p = 3.8 µA
- $V_{ENRISING}$ = 1.2 V
- $V_{ENFALLING}$ = 1.15 V

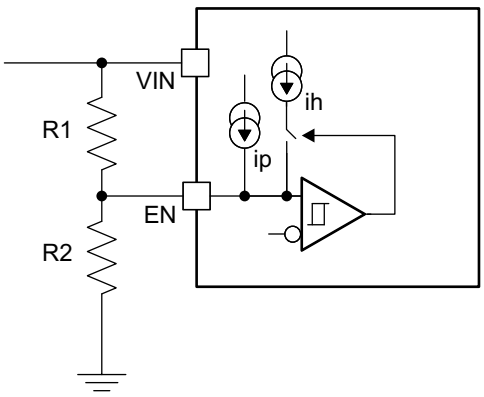


図 8-3. Adjustable VIN UVLO

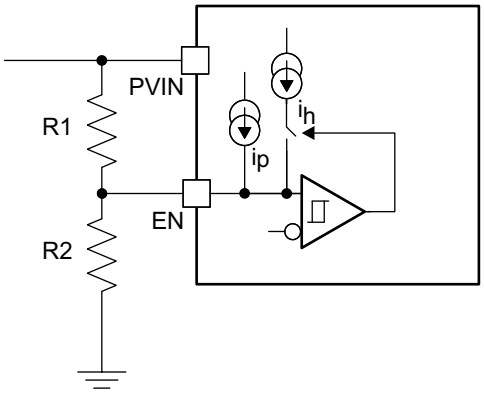


図 8-4. Adjustable PVIN UVLO, VIN > 4.5 V

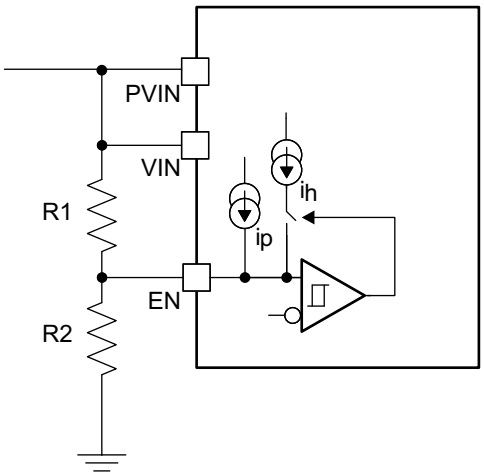


図 8-5. Adjustable VIN and PVIN UVLO

8.3.3 Soft-Start Time

The voltage on the respective SS pin controls the start-up of buck output. When the voltage on the SS pin is less than the internal 0.6-V reference, The TPS65263 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6 V. The SS pin can be used to program an external soft-start function or to allow output of buck to track another supply during start-up. The device has an internal pullup current source of 5 µA (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at SS pin. The TPS65263 regulates the internal feedback voltage to the voltage on the SS pin, allowing VOUT to rise smoothly from 0V to its regulated voltage without inrush current. The soft-start time can be calculated approximately by 式 4 .

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)} \quad (4)$$

Many of the common power supply sequencing methods can be implemented using the SSx and ENx pins. 図 8-6 shows the method implementing ratiometric sequencing by connecting the SSx pins of three buck channels together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pullup current source must be tripled in 式 4.

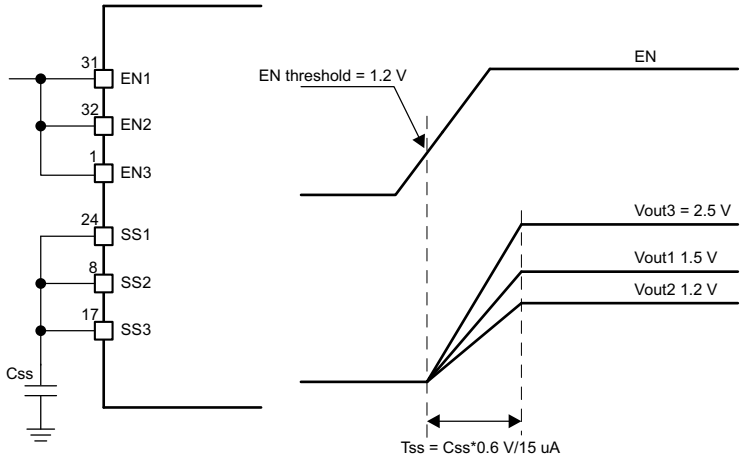


図 8-6. Ratiometric Power-Up Using SSx Pins

Simultaneous power supply sequencing can be implemented by connecting capacitor to SSx pin, shown in 図 8-7. Using 式 4 and 式 5, the capacitors can be calculated.

$$\frac{Css1}{Vout1} = \frac{Css2}{Vout2} = \frac{Css3}{Vout3} \quad (5)$$

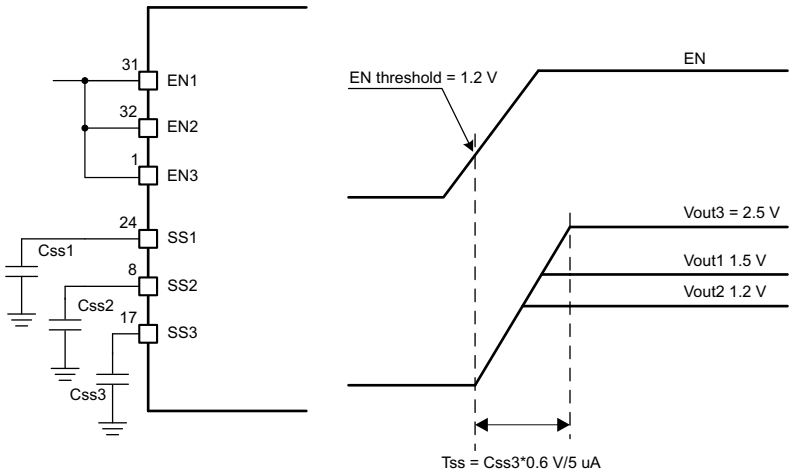


図 8-7. Simultaneous Startup Sequence Using SSx Pins

8.3.4 Power-Up Sequencing

The TPS65263 has dedicated enable pin and soft-start pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing by the addition of an external capacitor. Disabling the converter with an active pull-down transistor on the ENs pin allows for a predictable power-down timing operation. 図 8-8 shows the timing diagram of a typical buck power-up sequence with connecting a capacitor at ENx pin.

A typical 1.4-µA current is charging ENx pin from input supply. When ENx pin voltage rise to typical 0.4 V, the internal V7V LDO turns on. A 3.8-µA pullup current is sourcing ENx. After ENx pin voltage reaches to ENx enabling threshold, 3-µA hysteresis current sources to the pin to improve noise sensitivity. The internal soft-start comparator compares SS pin voltage to 1.2 V. When SS pin voltage ramps up to 1.2 V, PGOOD monitor is enabled. After PGOOD deglitch time, PGOOD is deasserted. SS pin voltage eventually is clamped around 2.1 V.

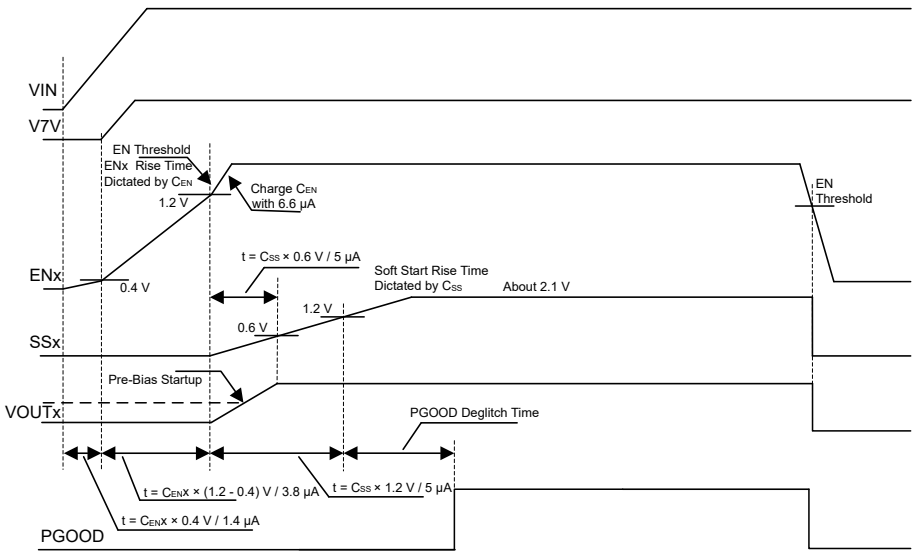


図 8-8. Startup Power Sequence

8.3.5 V7V Low Dropout Regulator and Bootstrap

Power for the high-side and low-side MOSFET drivers and most other internal circuitry is derived from the V7V pin. The internal built-in low dropout linear regulator (LDO) supplies 6.3 V (typical) from VIN to V7V. A 10-µF ceramic capacitor must be connected from V7V pin to power ground.

If the input voltage, VIN decreases to UVLO threshold voltage, the UVLO comparator detects V7V pin voltage and forces the converter off.

Each high-side MOSFET driver is biased from the floating bootstrap capacitor CB, shown in 図 8-9, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than VIN and BST-LX voltage is below regulation. The recommended value of this ceramic capacitor is 47 nF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage. Each low-side MOSFET driver is powered from V7V pin directly.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1 V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

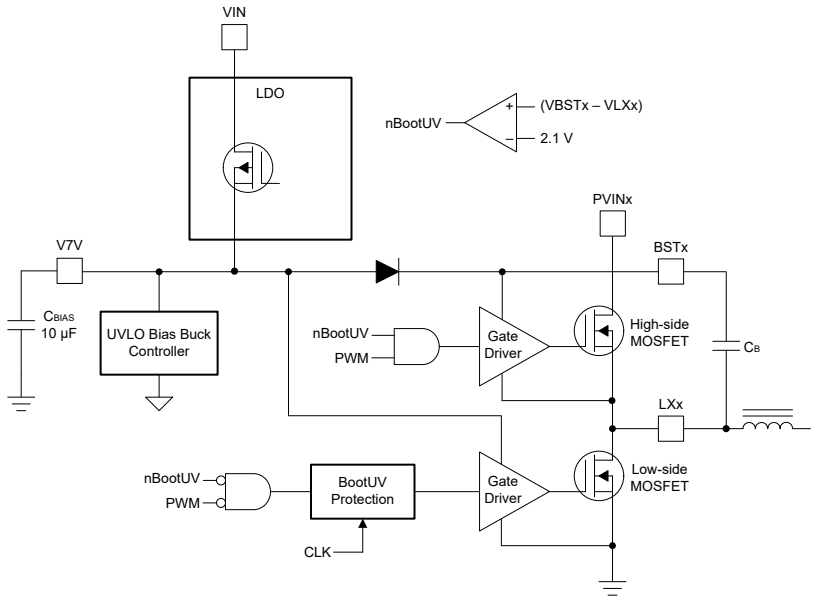


図 8-9. V7V Linear Dropout Regulator and Bootstrap Voltage Diagram

8.3.6 Out-of-Phase Operation

To reduce input ripple current, the switch clock of buck1 is 180° out-of-phase from the clock of buck2 and buck3. This enables the system having less input current ripple to reduce input capacitors' size, cost, and EMI.

8.3.7 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. When the output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the load can respond faster than the error amplifier. This leads to the possibility of an output overshoot. Each buck compares the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

8.3.8 Pulse Skipping Mode (PSM)

The TPS65263 can enter high-efficiency PSM operation at light load current. To disable PSM operation, set VOUTx_COM registers' bit 1 to 1 through I^2C interface.

When a controller is enabled for PSM operation, the peak inductor current is sensed and compared with 230-mA current typically. Because the integrated current comparator catches the peak inductor current only, the average load current entering PSM varies with the applications and external output filters. In PSM, the sensed peak inductor current is clamped at 230 mA, shown in 図 8-10.

When a controller operates in PSM, the inductor current is not allowed to reverse. The reverse current comparator turns off the low-side MOSFET when the inductor current reaches zero, preventing it from reversing and going negative.

Due to the delay in the circuit and current comparator tdly (typical 50 nS at Vin = 12 V), the real peak inductor current threshold to turn off high-side power MOSFET can shift higher depending on inductor inductance and input/output voltages. The threshold of peak inductor current to turn off high-side power MOSFET can be calculated by 式 6.

$$IL_{PEAK} = 230mA + \frac{vin - vout}{L} \times tdly \quad (6)$$

When the charge accumulated on Vout capacitor is more than loading need, COMP pin voltage drops to low voltage driven by error amplifier. There is an internal comparator at COMP pin. If comp voltage is lower than 0.35 V, power stage stops switching to save power.

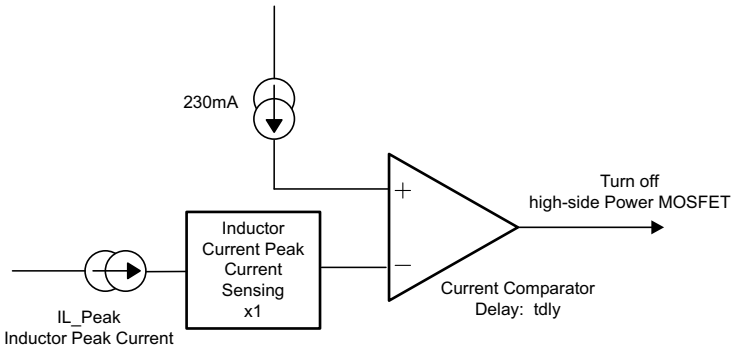


図 8-10. PSM Current Comparator

8.3.9 Slope Compensation

To prevent the sub-harmonic oscillations when the device operates at duty cycles greater than 50%, the TPS65263 adds built-in slope compensation, which is a compensating ramp to the switch current signal.

8.3.10 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

8.3.10.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

8.3.10.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 0.5 ms (typical) shown in 図 8-11, the device will shut down itself and restart after the hiccup time of 14 ms (typical). The hiccup mode helps to reduce the device power dissipation under severe overcurrent condition.

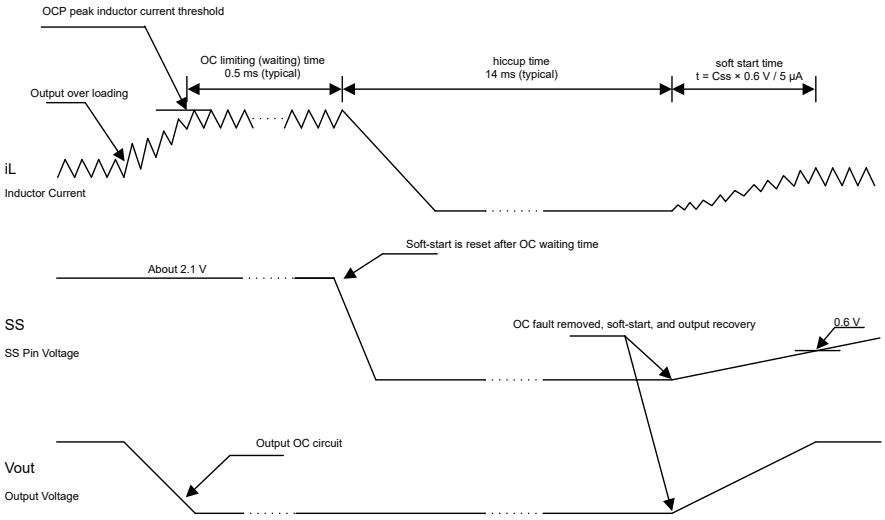


図 8-11. Overcurrent Protection

8.3.11 Power Good

The power good indicator for each buck channel can be read back through I^2 C.

When feedback voltage of the buck is between 95% (rising) and 105% (falling) of the internal voltage reference, the bit0, bit1 and bit2 in SYS_STATUS (address 0x06H) present the feedback voltage in regulation (logic 1) for buck1, buck2 and buck3 respectively. When feedback voltage of the buck is lower than 92.5% (falling) or greater than 107.5% (rising) of the nominal internal reference voltage, the bit0, bit1 and bit2 in SYS_STATUS (address 0x06H) present the feedback voltage beyond regulation (logic 0) for buck1, buck2 and buck3 respectively.

8.3.12 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power up sequence when the junction temperature drops below 140°C typically.

8.4 Device Functional Modes

8.4.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by NXP™ Semiconductors (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A controller device, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target device receives and/or transmits data on the bus under control of the controller device.

The TPS65263 device works as a target and supports the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), and fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 4.25 V (typical).

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The TPS65263 device supports 7-bit addressing. Ten-bit addressing and general call address are not supported.

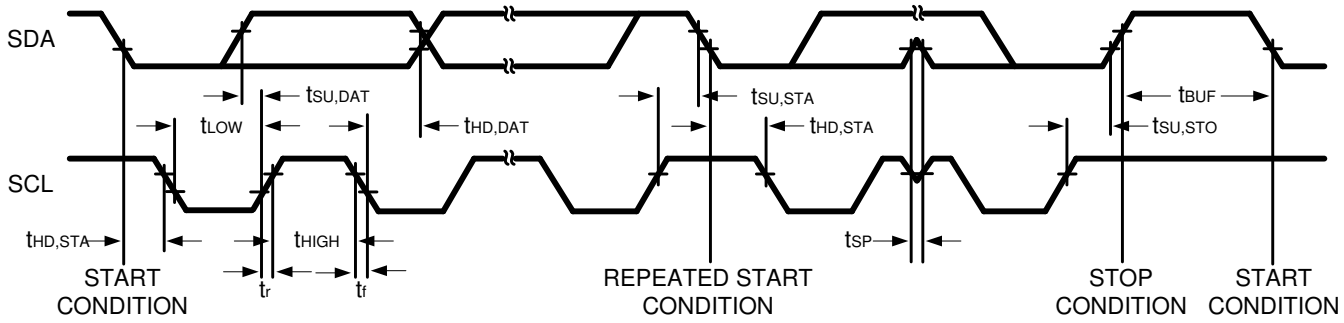


図 8-12. I²C Interface Timing Diagram

8.4.2 I²C Update Sequence

The TPS65263 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS65263 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS65263. TPS65263 performs an update on the falling edge of the LSB byte.

When the TPS65263 is in hardware shutdown (EN1, EN2, and EN3 pin tied to ground) the device cannot be updated through the I²C interface. Conversely, the I²C interface is fully functional during software shutdown (EN1, EN2, and EN3 bit = 0).

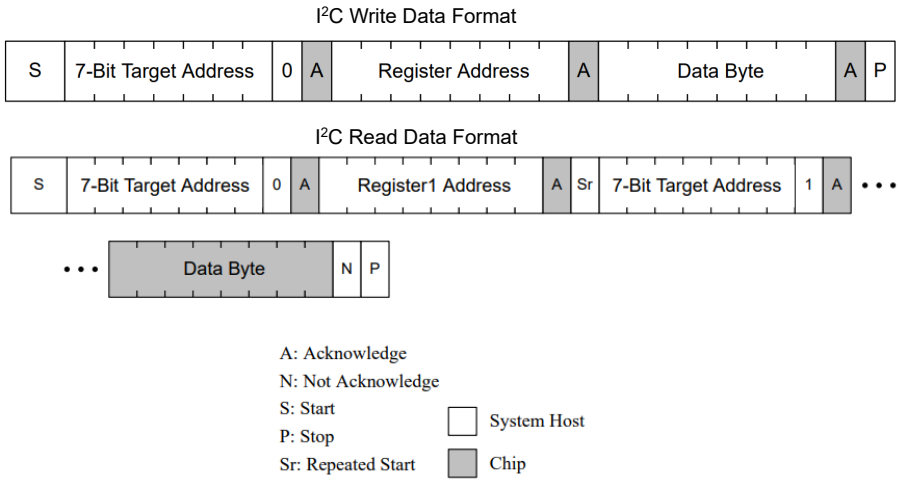


図 8-13. I²C Write and Read Data Format

8.5 Register Maps

8.5.1 Register Description

Register descriptions are shown in the following tables.

表 8-3. Register Addresses

NAME	BITS	ADDRESS
VOUT1_SEL	8	0x00H
VOUT2_SEL	8	0x01H
VOUT3_SEL	8	0x02H
VOUT1_COM	8	0x03H
VOUT2_COM	8	0x04H
VOUT3_COM	8	0x05H
SYS_STATUS	8	0x06H

8.5.2 VOUT1_SEL: Vout1 Voltage Selection Register (offset = 0x00H)

図 8-14. VOUT1_SEL

7	6	5	4	3	2	1	0
Vout1_Bit7	Vout1_Bit6	Vout1_Bit5	Vout1_Bit4	Vout1_Bit3	Vout1_Bit2	Vout1_Bit1	Vout1_Bit0
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-4. VOUT1_SEL Field Descriptions

Bit	Field	Type	Reset	Description
7	Vout1_Bit7	R/W		GO bit, must set to 1 to enable I^2C controlled VID voltages (default 0)
6	Vout1_Bit6	R/W		128 voltage selections with 7-bits control (default 0) Voltage range: 0.68 to 1.95 V Voltage step resolution: 10 mV 0x00H: Vout1 = 0.68 V; 0x7FH: Vout1 = 1.95 V
5	Vout1_Bit5			
4	Vout1_Bit4			
3	Vout1_Bit3			
2	Vout1_Bit2			
1	Vout1_Bit1			
0	Vout1_Bit0			

8.5.3 VOUT2_SEL: Vout2 Voltage Selection Register (offset = 0x01H)

図 8-15. VOUT2_SEL

7	6	5	4	3	2	1	0
Vout2_Bit7	Vout2_Bit6	Vout2_Bit5	Vout2_Bit4	Vout2_Bit3	Vout2_Bit2	Vout2_Bit1	Vout2_Bit0
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-5. VOUT2_SEL Field Descriptions

Bit	Field	Type	Reset	Description
7	Vout2_Bit7	R/W		GO bit, must set to 1 to enable I²C controlled VID voltages (default 0)
6	Vout2_Bit6	R/W		128 voltage selections with 7-bits control (default 0) Voltage range: 0.68 to 1.95 V Voltage step resolution: 10 mV 0x00H: Vout2 = 0.68 V; 0x7FH: Vout2 = 1.95 V
5	Vout2_Bit5			
4	Vout2_Bit4			
3	Vout2_Bit3			
2	Vout2_Bit2			
1	Vout2_Bit1			
0	Vout2_Bit0			

8.5.4 VOUT3_SEL: Vout3 Voltage Selection Register (offset = 0x02H)

図 8-16. VOUT3_SEL

7	6	5	4	3	2	1	0
Vout3_Bit7	Vout3_Bit6	Vout3_Bit5	Vout3_Bit4	Vout3_Bit3	Vout3_Bit2	Vout3_Bit1	Vout3_Bit0
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-6. VOUT3_SEL Field Descriptions

Bit	Field	Type	Reset	Description
7	Vout3_Bit7	R/W		GO bit, must set to 1 to enable I²C controlled VID voltages (default 0)
6	Vout3_Bit6	R/W		128 voltage selections with 7-bits control (default 0) Voltage range: 0.68 to 1.95 V Voltage step resolution: 10 mV 0x00H: Vout3 = 0.68 V; 0x7FH: Vout3 = 1.95 V
5	Vout3_Bit5			
4	Vout3_Bit4			
3	Vout3_Bit3			
2	Vout3_Bit2			
1	Vout3_Bit1			
0	Vout3_Bit0			

8.5.5 VOUT1_COM: Buck1 Command Register (offset = 0x03H)

図 8-17. VOUT1_COM

7	6	5	4	3	2	1	0
N/A	SR3	SR2	SR1	N/A	N/A	Mode1	nEN1
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-7. VOUT1_COM Field Descriptions

Bit	Field	Type	Reset	Description
7	N/A	R/W		Not used (default 0)
6	SR3	R/W		Vout1 VID voltage transition slew rate control (default 0)
5	SR2	R/W		000: 10 mV/cycle; 001: 10 mV/2 cycles; 010: 10 mV/4 cycles; 011: 10 mV/8 cycles; 100: 10 mV/16 cycles; 101: 10 mV/32 cycles; 110: 10 mV/64 cycles; 111: 10 mV/128 cycles
4	SR1	R/W		
3	N/A	R/W		Not used (default 0)
2	N/A	R/W		Not used (default 0)
1	Mode1	R/W		0: Enable buck1 PSM operation at light load (default); 1: Forced buck1 PWM mode operation
0	nEN1	R/W		0: Enable buck1 (default); 1: Disable buck1

8.5.6 VOUT2_COM: Buck2 Command Register (offset = 0x04H)

図 8-18. VOUT2_COM

7	6	5	4	3	2	1	0
N/A	SR3	SR2	SR1	N/A	N/A	Mode2	nEN2
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-8. VOUT2_COM Field Descriptions

Bit	Field	Type	Reset	Description
7	N/A	R/W		Not used (default 0)
6	SR3	R/W		Vout2 VID voltage transition slew rate control (default 0)
5	SR2	R/W		000: 10 mV/cycle; 001: 10 mV/2 cycles; 010: 10 mV/4 cycles; 011: 10 mV/8 cycles; 100: 10 mV/16 cycles; 101: 10 mV/32 cycles; 110: 10 mV/64 cycles; 111: 10 mV/128 cycles
4	SR1	R/W		
3	N/A	R/W		Not used (default 0)
2	N/A	R/W		Not used (default 0)
1	Mode2	R/W		0: Enable buck2 PSM operation at light load (default); 1: Forced buck2 PWM mode operation
0	nEN2	R/W		0: Enable buck2 (default); 1: Disable buck2

8.5.7 VOUT3_COM: Buck3 Command Register (offset = 0x05H)

図 8-19. VOUT3_COM

7	6	5	4	3	2	1	0
N/A	SR3	SR2	SR1	N/A	N/A	Mode3	nEN3
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-9. VOUT3_COM Field Descriptions

Bit	Field	Type	Reset	Description
7	N/A	R/W		Not used (default 0)
6	SR3	R/W		Vout3 VID voltage transition slew rate control. 000: 10 mV/cycle; 001: 10 mV/2 cycles; 010: 10 mV/4 cycles; 011: 10 mV/8 cycles; 100: 10 mV/16 cycles; 101: 10 mV/32 cycles; 110: 10 mV/64 cycles; 111: 10 mV/128 cycles
5	SR2	R/W		
4	SR1	R/W		
3	N/A	R/W		Not used (default 0)
2	N/A	R/W		Not used (default 0)
1	Mode3	R/W		0: Enable buck3 PSM operation at light load (default); 1: Forced buck3 PWM mode operation
0	nEN3	R/W		0: Enable buck3 (default); 1: Disable buck3

8.5.8 SYS_STATUS: System Status Register (offset = 0x06H)

図 8-20. SYS_STATUS

7	6	5	4	3	2	1	0
OTP	OC3	OC2	OC1	OTW	PGOOD3	PGOOD2	PGOOD1
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-10. SYS_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7	OTP	R		0: Die overtemperature protection is not triggered (default); 1: Die temperature over 160°C, which triggers overtemperature protection.
6	OC3	R		0: Buck3 current not beyond the current limit (default); 1: Buck3 overcurrent limiting and hiccup protection is triggered.
5	OC2	R		0: Buck2 current not beyond the current limit (default); 1: Buck2 overcurrent limiting and hiccup protection is triggered.
4	OC1	R		0: Buck1 current not beyond the current limit (default); 1: Buck1 overcurrent limiting and hiccup protection is triggered.
3	OTW	R		0: Die temperature below 125°C (default); 1: Die temperature over 125°C.
2	PGOOD3	R		0: Vout3 not in power good monitor's range (default); 1: Vout3 in power good monitor's range.
1	PGOOD2	R		0: Vout2 not in power good monitor's range (default); 1: Vout2 in power good monitor's range.
0	PGOOD1	R		0: Vout1 not in power good monitor's range (default); 1: Vout1 in power good monitor's range.

9 Application and Implementation

注

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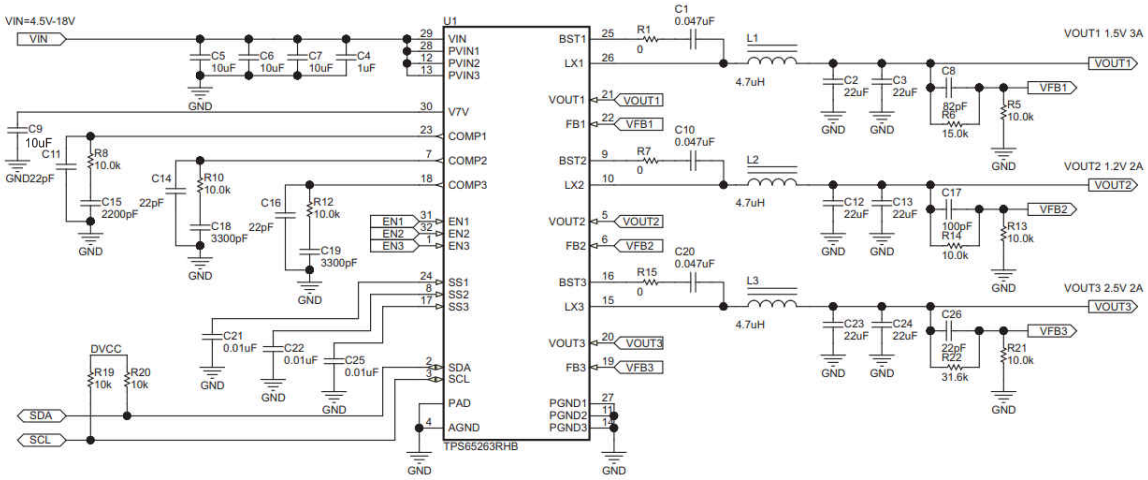
9.1 Application Information

The device is triple synchronous step down dc/dc converter with I^{2}C interface. It is typically used to convert a higher dc voltage to lower dc voltages with continuous available output current of 3 A / 2 A / 2 A. The following design procedure can be used to select component values for the TPS65263. This section presents a simplified discussion of the design process.

9.2 Typical Application



9.2.1 Design Requirements

This example details the design of triple synchronous step-down converter. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, start with the following known parameters:

表 9-1. Design Parameters

PARAMETER	VALUE
Vout1	1.5 V
Iout1	3 A
Vout2	1.2 V
Iout2	2 A
Vout3	2.5 V
Iout3	2 A
Transient response 1-A load step	±5%
Input voltage	12 V normal, 4.5 to 18 V
Output voltage ripple	±1%
Switching frequency	600 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use 式 7. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \tag{7}$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from 式 9 and 式 10.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \tag{8}$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times f_{sw}}\right)^2}{12}} \tag{9}$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \tag{10}$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.2 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation can occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. 式 11 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}} \tag{11}$$

Where ΔIout is the change in output current, f_{SW} is the regulators switching frequency and ΔV_{out} is the allowable change in the output voltage.

式 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, V_{ripple} is the maximum allowable output voltage ripple, and I_{ripple} is the inductor ripple current.

$$C_o > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_{oripple}}{I_{oripple}}} \tag{12}$$

式 13 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{oripple}}{I_{oripple}} \tag{13}$$

Additional capacitance de-ratings for aging, temperature and DC bias must be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. 式 14 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times f_{sw}} \tag{14}$$

9.2.2.3 Input Capacitor Selection

The TPS65263 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the PVIN input voltage pins. In some applications additional bulk capacitance can also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of The TPS65263. The input ripple current can be calculated using 式 15.

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \tag{15}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 16.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \tag{16}$$

9.2.2.4 Loop Compensation

The TPS65263 incorporates a peak current mode control scheme. The error amplifier is a trans-conductance amplifier with a gain of 300 µS. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow the following steps.

1. Select switching frequency f_{SW} that is appropriate for application depending on L and C sizes, output ripple, EMI, and etc. Switching frequency between 500 kHz to 1 MHz gives best trade-off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up cross over frequency, f_c, which is typically between 1/5 and 1/20 of f_{SW}.
3. R_C can be determined by

$$R_C = \frac{2\pi \times fc \times Vo \times Co}{G_{m-EA} \times Vref \times G_{m-PS}} \tag{17}$$

4. Calculate CC by placing a compensation zero at or before the dominant pole $\left(fp = \frac{1}{C_o \times R_L \times 2\pi} \right)$.

$$C_C = \frac{R_L \times Co}{R_C} \tag{18}$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \times Co}{R_C} \tag{19}$$

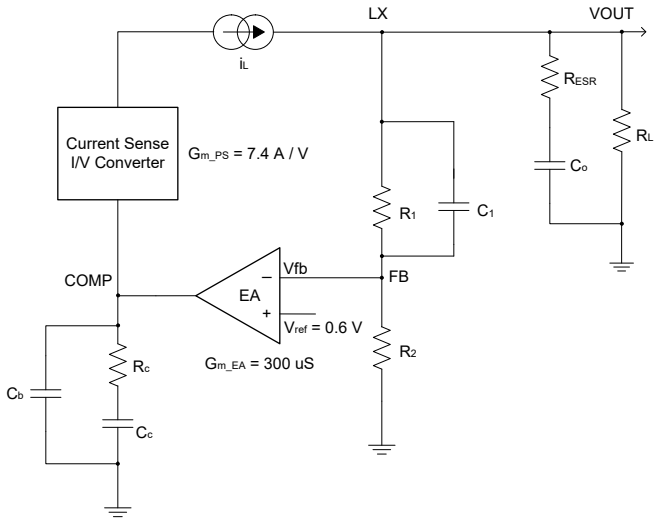


図 9-1. DC/DC Loop Compensation

9.2.3 Application Curves

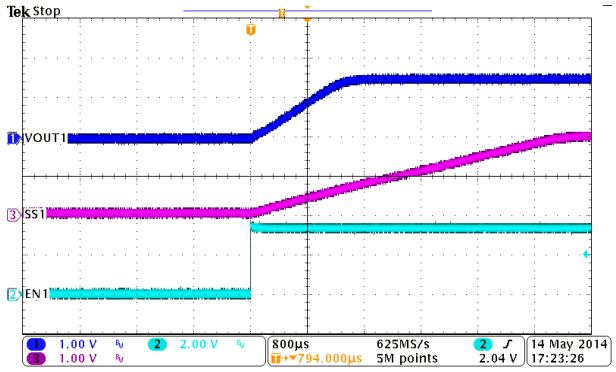


図 9-2. BUCK1, Soft-Start, Iout = 3 A

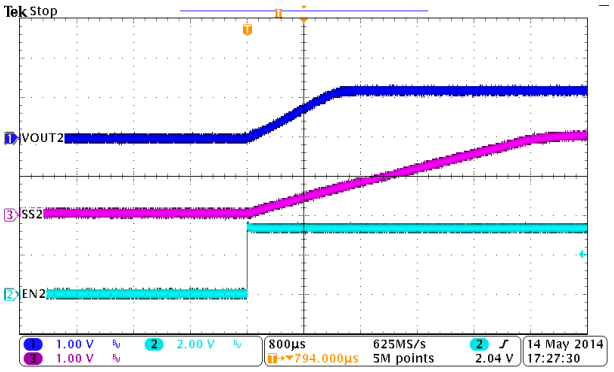


図 9-3. BUCK2, Soft-Start, Iout = 2 A

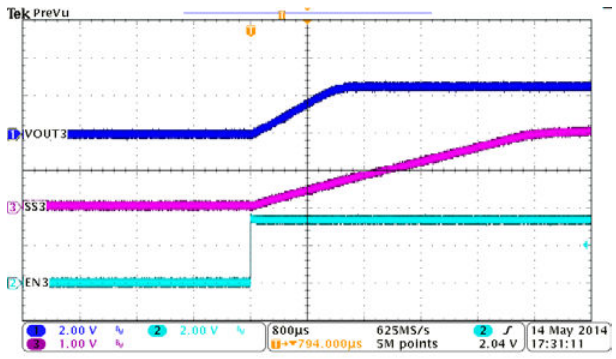


図 9-4. BUCK3, Soft-Start, Iout = 2 A

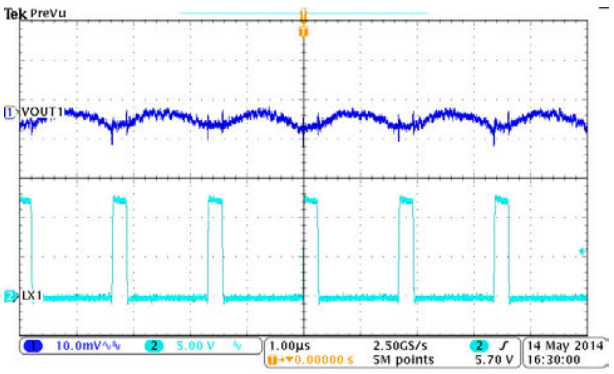


図 9-5. BUCK1, Output Voltage Ripple, Iout = 3 A

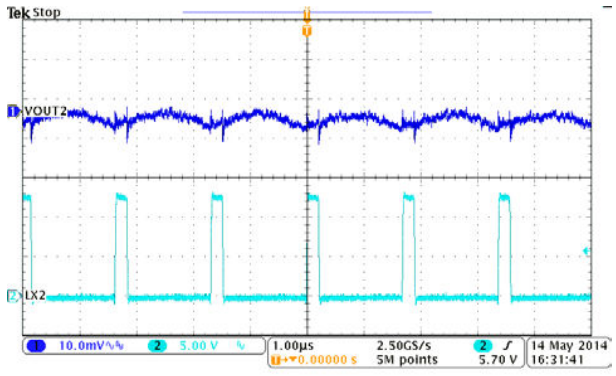


図 9-6. BUCK2, Output Voltage Ripple, Iout = 3 A

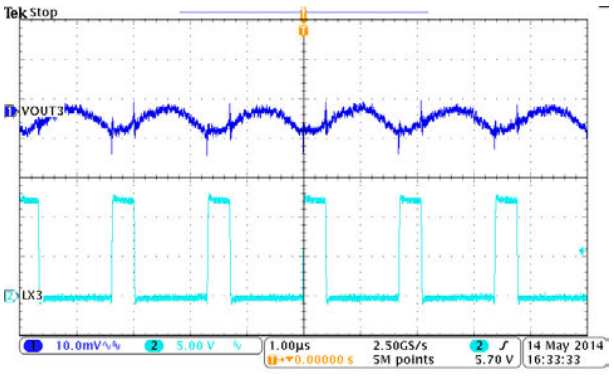


図 9-7. BUCK3, Output Voltage Ripple, Iout = 2 A

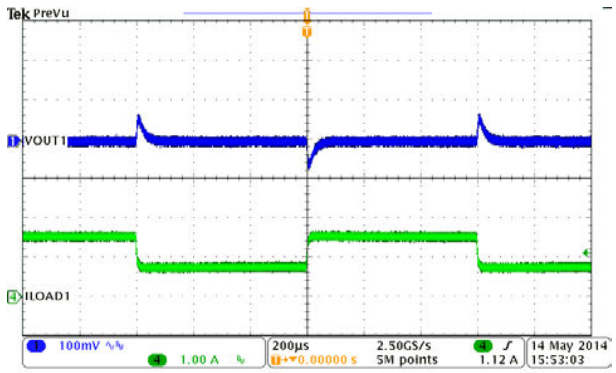


図 9-8. BUCK1, Load Transient, 0.75 to 1.5 A SR = 0.25 A/µs

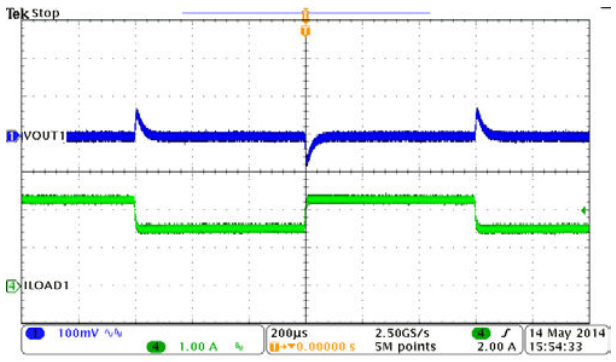


図 9-9. BUCK1, Load Transient, 1.5 to 2.25 A SR = 0.25 A/µs

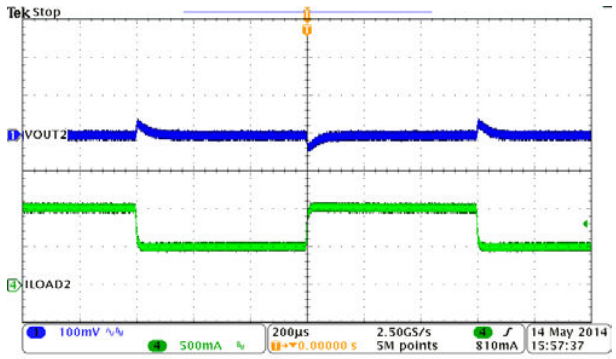


図 9-10. BUCK2, Load Transient, 0.5 to 1 A SR = 0.25 A/µs

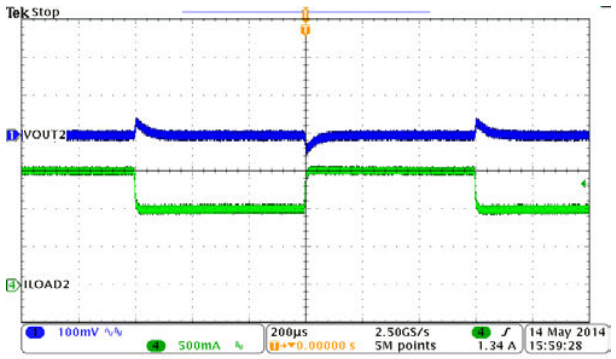


図 9-11. BUCK2, Load Transient, 1 to 1.5 A SR = 0.25 A/µs

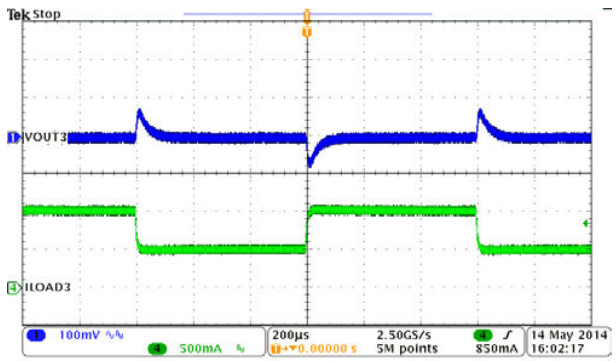


図 9-12. BUCK3, Load Transient, 0.5 to 1 A SR = 0.25 A/µs

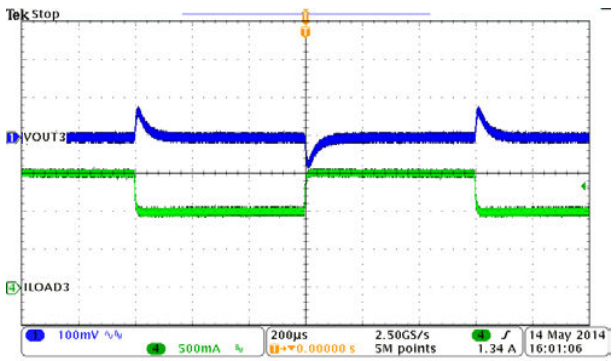


図 9-13. BUCK3, Load Transient, 1 to 1.5 A SR = 0.25 A/µs

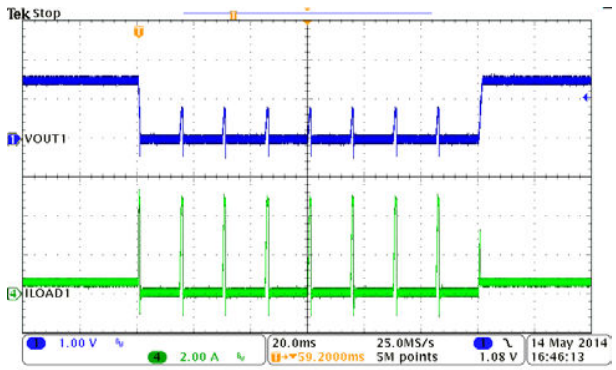


図 9-14. BUCK1, Hiccup and Recovery

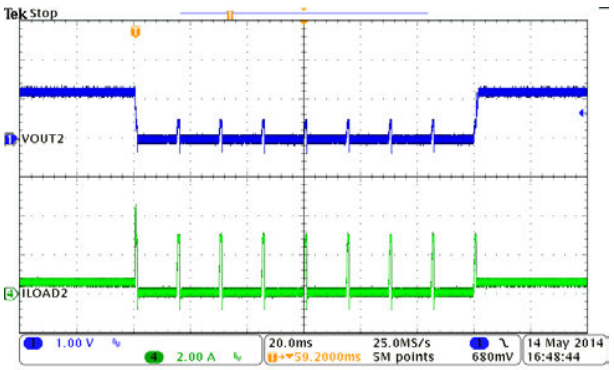


図 9-15. BUCK2, Hiccup and Recovery

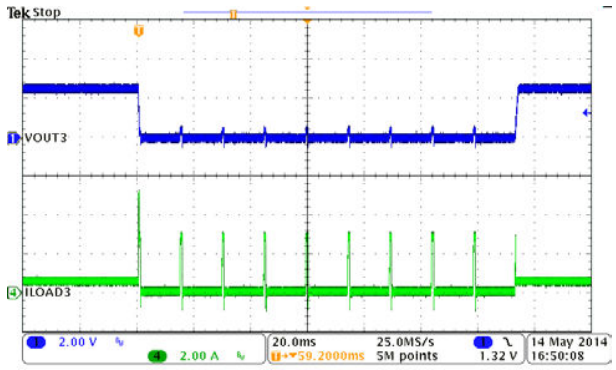


図 9-16. BUCK3, Hiccup and Recovery

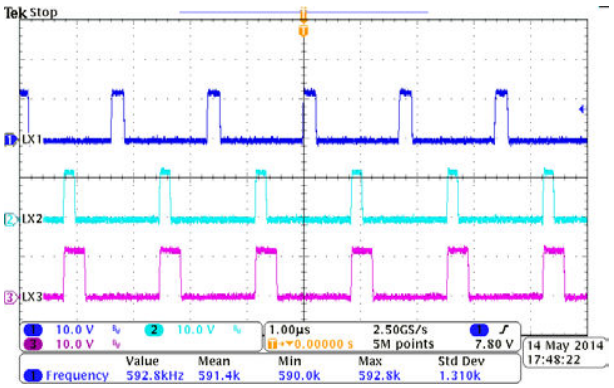


図 9-17. 180° Out-of-Phase

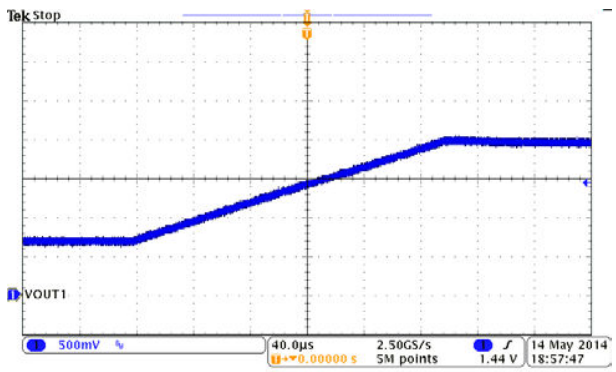


図 9-18. VID1 from 00 to 7F, SR = 10 mV/cycle

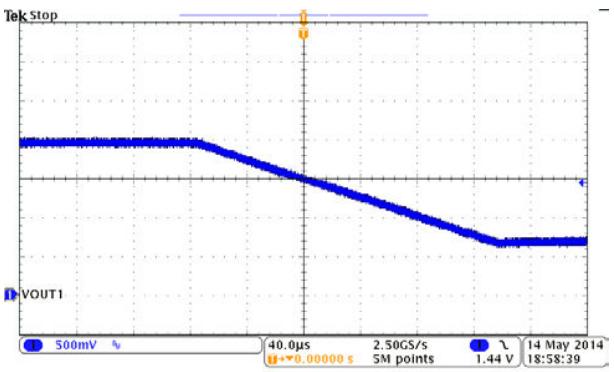


図 9-19. VID1 from 7F to 00, SR = 10 mV/cycle

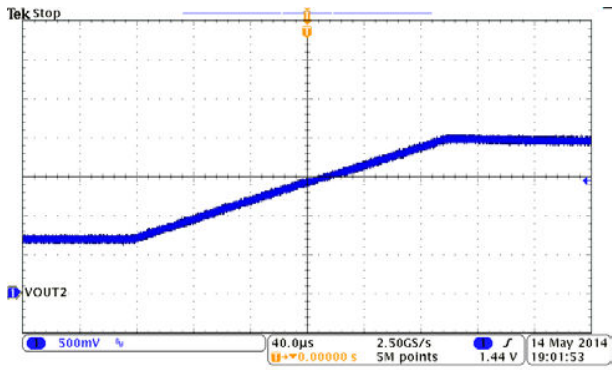


図 9-20. VID2 from 00 to 7F, SR = 10 mV/cycle

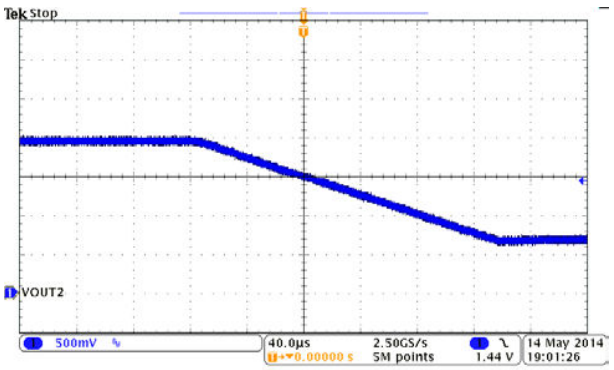


図 9-21. VID2 from 7F to 00, SR = 10 mV/cycle

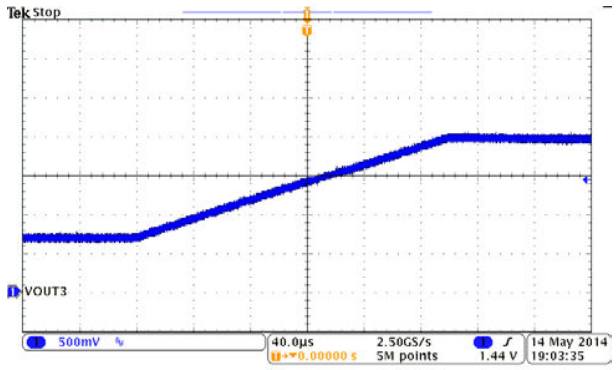


図 9-22. VID3 from 00 to 7F, SR = 10 mV/cycle

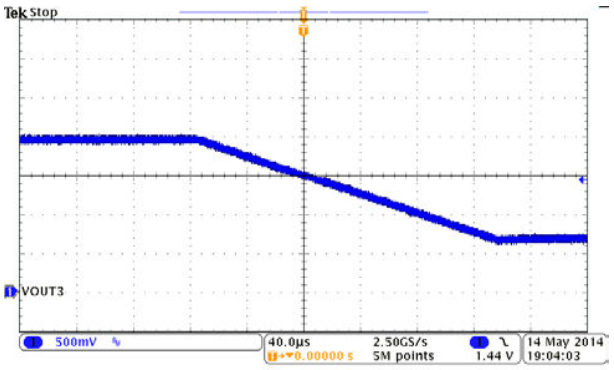
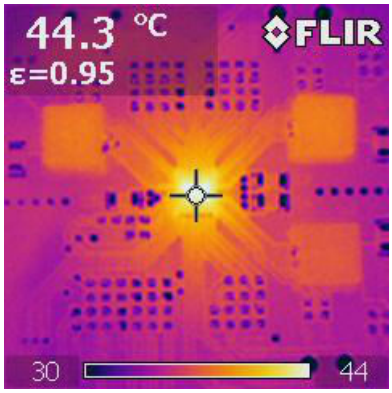
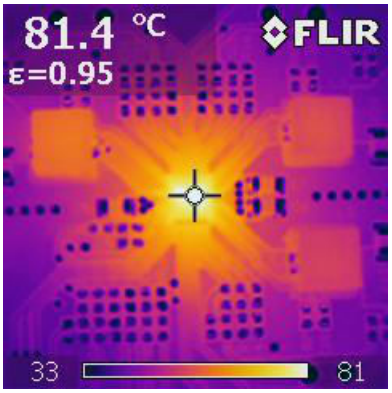


図 9-23. VID3 from 7F to 00, SR = 10 mV/cycle



VIN = 12 V; VOUT1 = 1.5 V / 1.5 A; VOUT2 = 1.2 V / 1 A
VOUT3 = 2.5 V / 1 A T_A = 26.8°C

図 9-24. Thermal Signature of TPS65263EVM, 4-Layer EVM Condition, 75 mm × 75 mm



VIN = 12 V; VOUT1 = 1.5 V / 3 A; VOUT2 = 1.2 V / 2 A
VOUT3 = 2.5 V / 2 A T_A = 26.8°C

図 9-25. Thermal Signature of TPS65263EVM, 4-Layer EVM Condition, 75 mm × 75 mm

9.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 to 18 V. This input power supply must be well regulated. If the input supply is located more than a few inches from the TPS65263 converter additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

9.4 Layout

9.4.1 Layout Guidelines

The TPS65263 can be layout on 2-layer PCB, shown in 図 9-26.

Layout is a critical portion of good power supply design. See 図 9-26 for a PCB layout example. The top contains the main power traces for PVIN, VOUT, and LX. Also on the top layer are connections for the remaining pins of the TPS65263 and a large top side area filled with ground. The top layer ground area must be connected to the bottom layer ground using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65263 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

For operation at full rated load, the top side ground area together with the bottom side ground plane must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care must be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor must be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground must use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components must be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors must be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown.

9.4.2 Layout Example

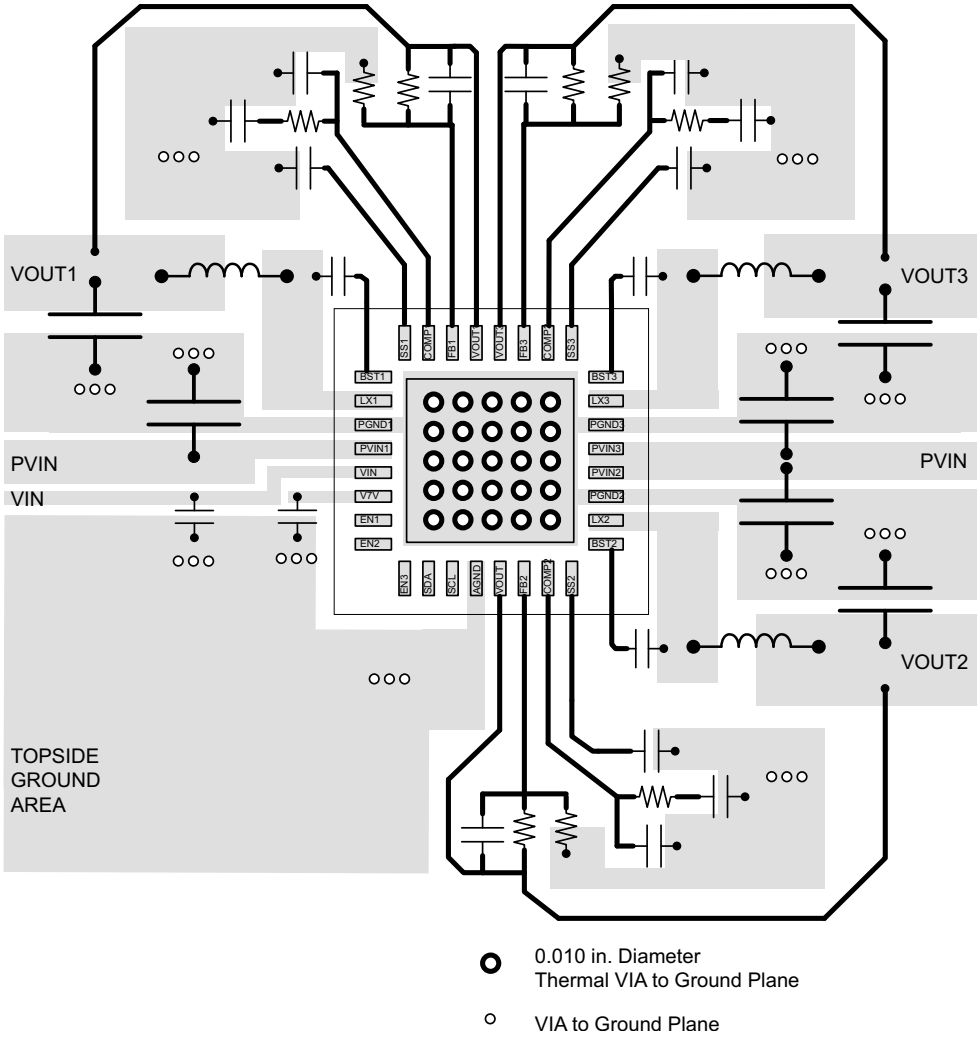


図 9-26. PCB Layout

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

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TI E2E™ is a trademark of Texas Instruments.
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10.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65263RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65263	Samples
TPS65263RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TPS 65263	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS65263 :

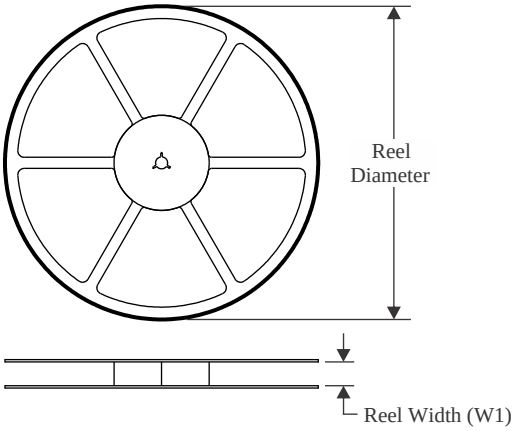
- Automotive : TPS65263-Q1

NOTE: Qualified Version Definitions:

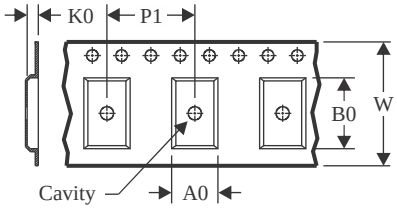
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

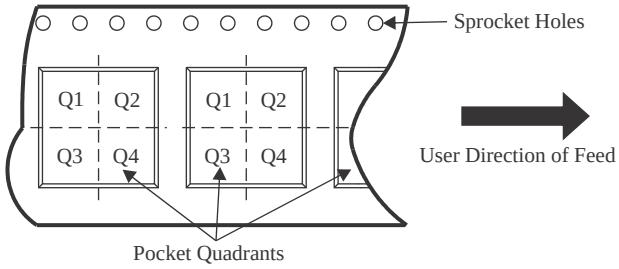


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

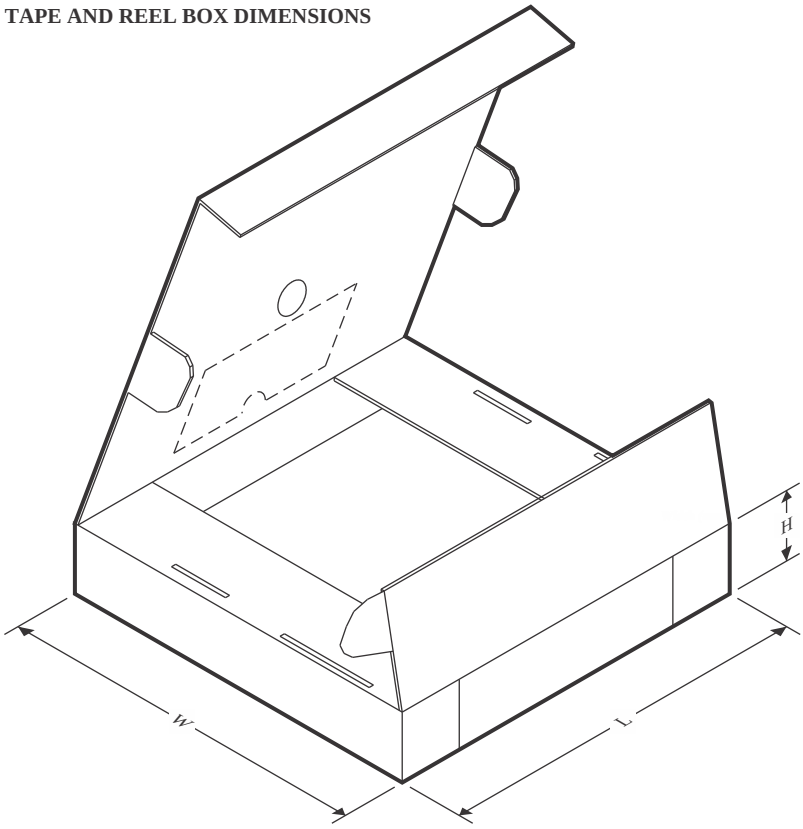
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65263RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65263RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65263RHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
TPS65263RHBT	VQFN	RHB	32	250	182.0	182.0	20.0

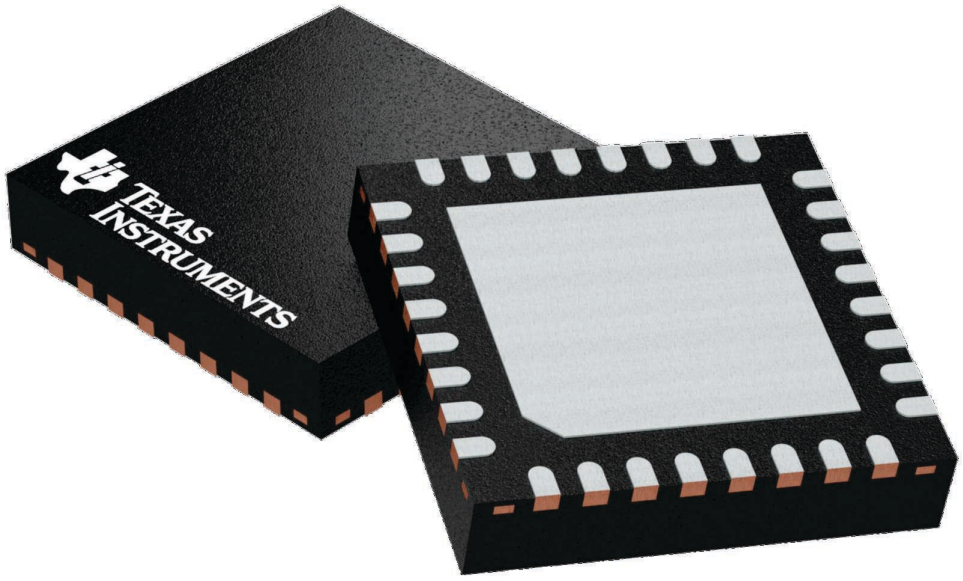
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

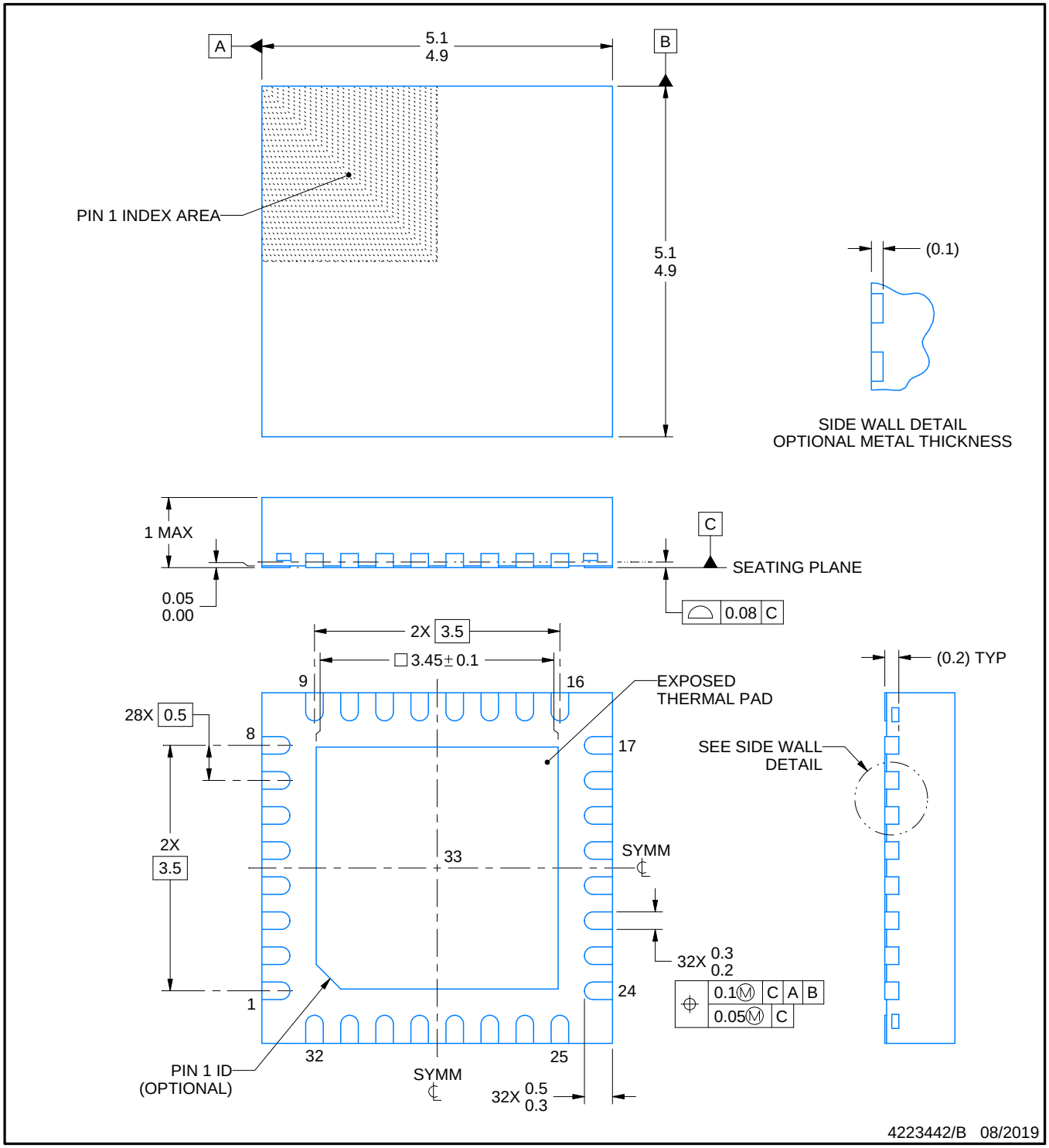
4224745/A

RHB0032E

PACKAGE OUTLINE

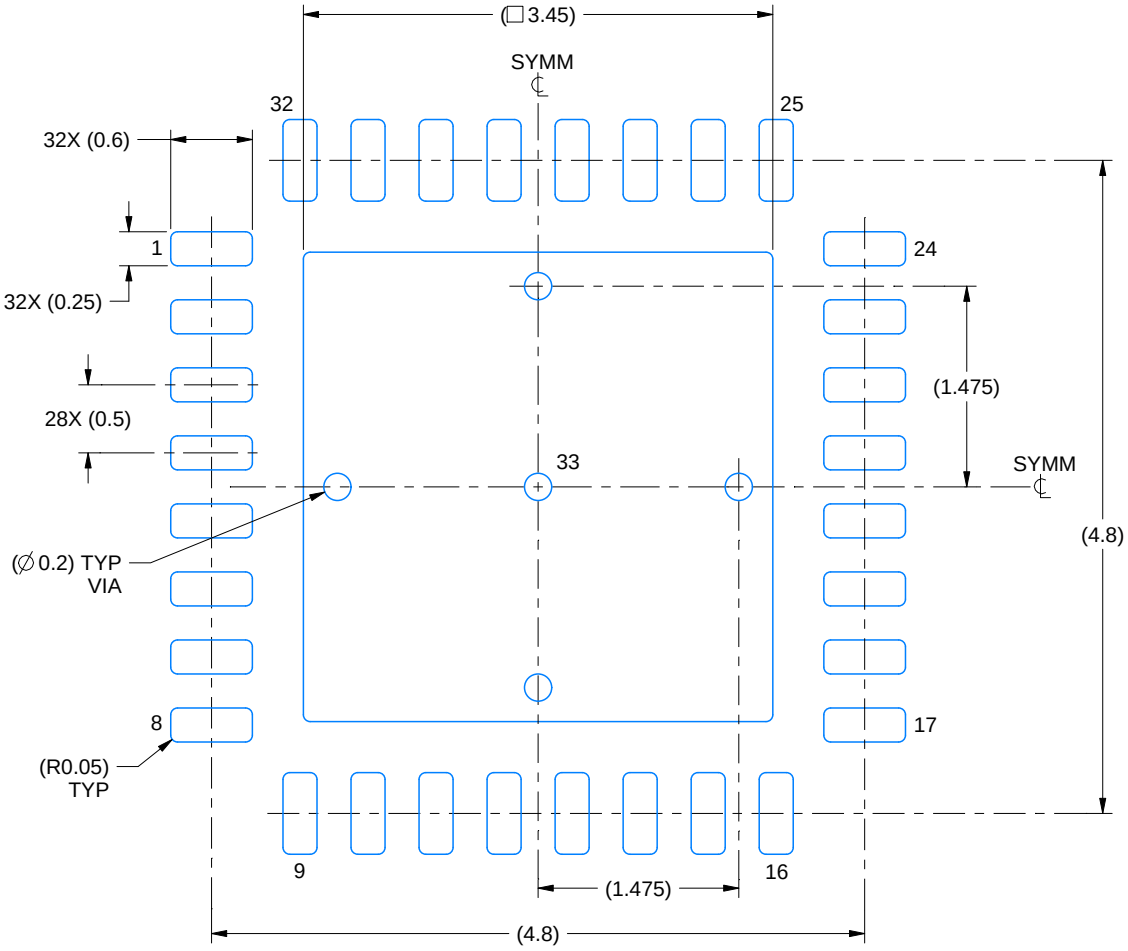
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

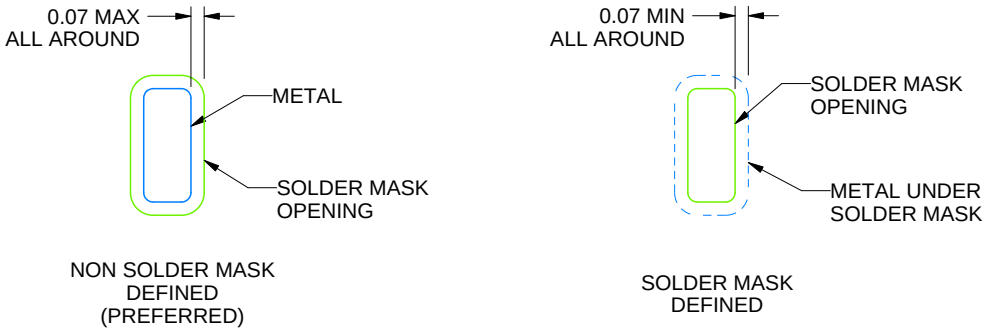


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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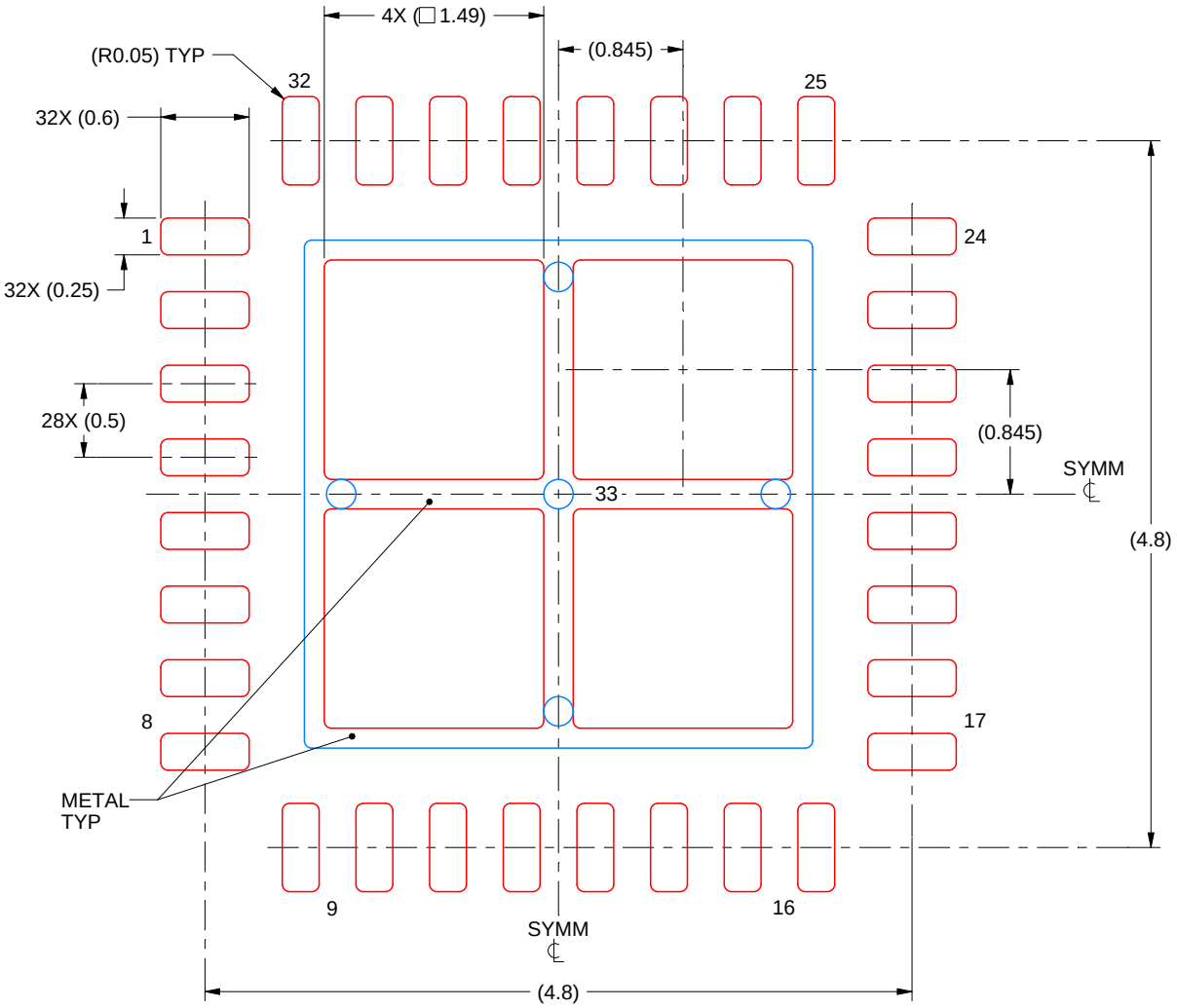
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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