

# TPS65987DDJ Thunderbolt 3 デバイス向け、パワー・スイッチ内蔵 USB Type-C® および USB PD コントローラ

## 1 特長

- USB-IF による PD3.0 認証済みデバイス
  - 新しい USB PD 設計の認証には PD3.0 シリコンが必要
    - TID#: 1067
  - [PD2.0 と PD3.0 の比較](#)の記事
- TPS65987DDJ は Thunderbolt 3 (TBT3) デバイスの PD3.0 コントローラです。
  - この PD コントローラは TBT3 デバイスの設計でのみ使用できます。
  - インテル社のリファレンス・デザイン (文書番号 569174) を参照してください。
  - TBT3 デバイス以外の設計に使う場合、[www.ti.com/usb-c](http://www.ti.com/usb-c) と [E2E ガイド](#)を参照してください。
- 完全に管理されたパワー・パスを内蔵
  - 2 つの 5~20V、5A、25mΩ 双方向スイッチを内蔵
  - UL 2367 認証番号: 20190107-E169910
  - IEC 62368-1 認証番号: US-34617-UL
- 堅牢なパワー・パス保護機能を内蔵
  - シンクに構成した場合、両方の 20V/5A パワー・パスの逆電流保護、低電圧保護、過電圧保護、スルーレート制御機能を内蔵
  - ソースに構成した場合、両方の 20V/5A パワー・パスの低電圧保護、過電圧保護、突入電流保護のための電流制限機能を内蔵
- USB Type-C® 電力供給 (PD) コントローラ
  - 13 本の構成可能な GPIO
  - BC1.2 充電対応
  - USB PD 3.0 認証済み
  - USB Type-C 仕様に準拠

- ケーブルの取り付けと方向の検出
- VCONN スイッチ内蔵
- 物理レイヤおよびポリシー・エンジン
- デッド・バッテリ・サポート用の 3.3V LDO 出力
- 3.3V または VBUS 電源からの電力供給
- 1 つの I2C プライマリまたはセカンダリ・ポート
- 1 つの I2C プライマリ専用ポート
- 1 つの I2C セカンダリ専用ポート

## 2 アプリケーション

- [ドッキング・システム](#)
- [モニタ](#)
- Thunderbolt 3 システム

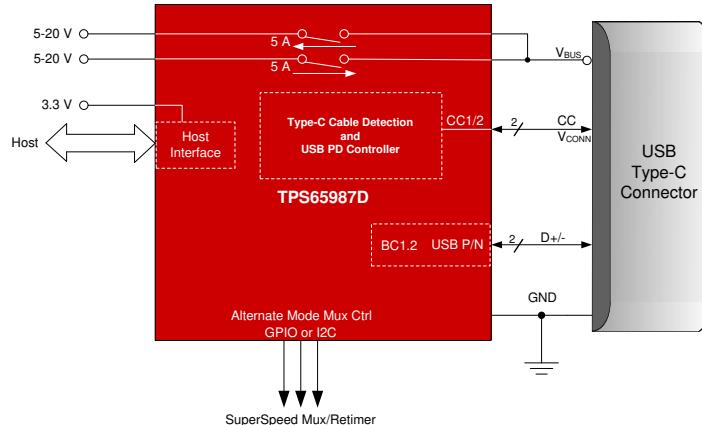
## 3 概要

TPS65987DDJ は、ドッキング・ステーションまたはモニタ向けに最適化されたシングル・ポート高集積スタンダードアロン USB Type-C および PD (Power Delivery) コントローラです。TPS65987DDJ は、完全に管理されたパワー・パスを堅牢な保護機能と統合することで包括的な USB-C PD ソリューションを実現しています。このデバイスは、インテル社の TBT3 デバイス最終製品リファレンス・デザインに採用されています。このリファレンス・デザインは、この種の設計において本 PD コントローラがシステム・レベルで適切に機能することを保証しています。これにより、システム設計の複雑さが大幅に緩和され、その結果、開発期間を大幅に短縮できます。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
TPS65987DDJ	QFN (56)	7.00mm × 7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、必ず最新版の英語版をご参照ください。

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## 4 Revision History

Changes from Revision A (August 2021) to Revision B (October 2022)	Page
• Updated pin image to read Pin 36: SPI_POCI (GPIO8) and Pin 37: SPI_PICO (GPIO9)	3
• Updated pin 36 name to read SPI_POCI (GPIO8)	3

Changes from Revision * (May 2019) to Revision A (August 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「特長」一覧を更新	1
• ドキュメントのタイトルを更新	1
• 文書全体で、SPI に言及している場合、従来の用語をコントローラ / ペリフェラルに変更	1
• 「アプリケーション」セクションを更新	1
• 「概要」セクションを更新	1

## 5 Pin Configuration and Functions

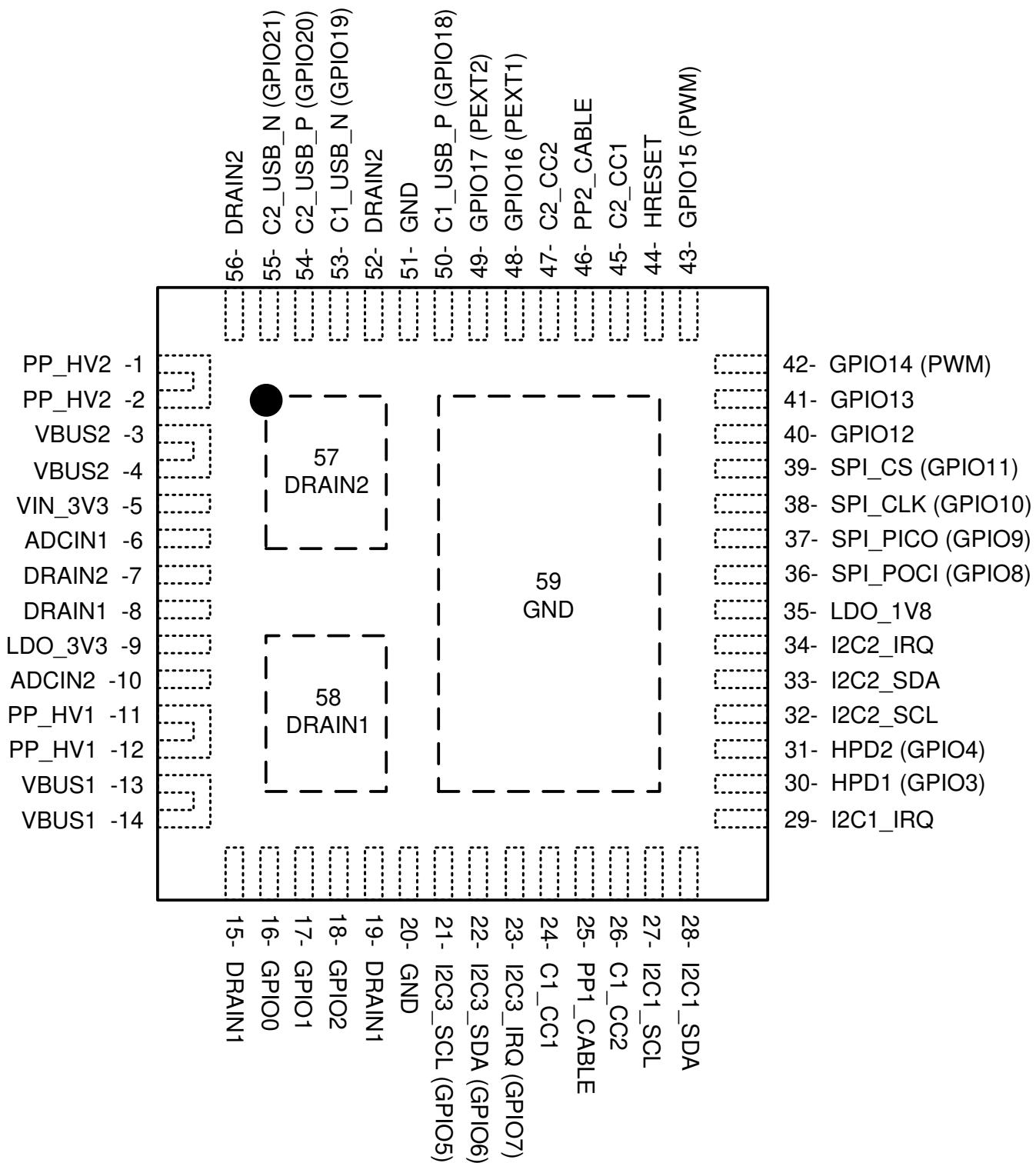


图 5-1. RSH Package 56-Pin QFN Top View

表 5-1. Pin Functions

PIN		TYPE <sup>(2)</sup>	RESET STATE <sup>(1)</sup>	DESCRIPTION
NAME	NO.			
ADCIN1	6	I	Input	Boot configuration Input. Connect to resistor divider between LDO_3V3 and GND.
ADCIN2	10	I	Input	I2C address configuration Input. Connect to resistor divider between LDO_3V3 and GND.
C_CC1	24	I/O	High-Z	Output to Type-C CC or VCONN pin . Filter noise with capacitor to GND
C_CC2	26	I/O	High-Z	Output to Type-C CC or VCONN pin . Filter noise with capacitor to GND
C_USB_N (GPIO19)	53	I/O	Input (High-Z)	USB D- connection for BC1.2 support
C_USB_P (GPIO18)	50	I/O	Input (High-Z)	USB D+ connection for BC1.2 support
DRAIN1	8, 15, 19, 58	—	—	Drain of internal power path 1. Connect thermal pad 58 to as big of pad as possible on PCB for best thermal performance. Short the other pins to this thermal pad
DRAIN2	7, 52, 56, 57	—	—	Drain of internal power path 2. Connect thermal pad 57 to as big of pad as possible on PCB for best thermal performance. Short the other pins to this thermal pad
GND	20, 45 , 46, 47, 51	—	—	Unused pin. Tie to GND.
GPIO0	16	I/O	Input (High-Z)	General Purpose Digital I/O 0. Float pin when unused. GPIO0 is asserted low during the TPS65987DDJ boot process. Once device configuration and patches are loaded GPIO0 is released
GPIO1	17	I/O	Input (High-Z)	General Purpose Digital I/O 1. Ground pin with a 1-MΩ resistor when unused in the application
GPIO2	18	I/O	Input (High-Z)	General Purpose Digital I/O 2. Float pin when unused
GPIO3 (HPD)	30	I/O	Input (High-Z)	General Purpose Digital I/O 3. Configured as Hot Plug Detect (HPD) TX and RX when DisplayPort alternate mode is enabled. Float pin when unused
GPIO4	31	I/O	Input (High-Z)	General Purpose Digital I/O 4. Float pin when unused
I2C3_SCL (GPIO5)	21	I/O	Input (High-Z)	I2C port 3 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used. Float pin when unused
I2C3_SDA (GPIO6)	22	I/O	Input (High-Z)	I2C port 3 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used. Float pin when unused
I2C3_IRQ (GPIO7)	23	I/O	Input (High-Z)	I2C port 3 interrupt detection (port 3 operates as an I2C Master Only). Active low detection. Connect to the I2C slave's interrupt line to detect when the slave issues an interrupt. Float pin when unused
GPIO12	40	I/O	Input (High-Z)	General Purpose Digital I/O 12. Float pin when unused
GPIO13	41	I/O	Input (High-Z)	General Purpose Digital I/O 13. Float pin when unused
GPIO14 (PWM)	42	I/O	Input (High-Z)	General Purpose Digital I/O 14. May also function as a PWM output. Float pin when unused
GPIO15 (PWM)	43	I/O	Input (High-Z)	General Purpose Digital I/O 15. May also function as a PWM output. Float pin when unused

**表 5-1. Pin Functions (continued)**

PIN		TYPE <sup>(2)</sup>	RESET STATE <sup>(1)</sup>	DESCRIPTION
NAME	NO.			
GPIO16 (PP_EXT1)	48	I/O	Input (High-Z)	General Purpose Digital I/O 16. May also function as single wire enable signal for external power path 1. Pull-down with external resistor when used for external path control. Float pin when unused
GPIO17 (PP_EXT2)	49	I/O	Input (High-Z)	General Purpose Digital I/O 17. May also function as single wire enable signal for external power path 2. Pull-down with external resistor when used for external path control. Float pin when unused
GPIO20	54	I/O	Input (High-Z)	General Purpose Digital I/O 20. Float pin when unused
GPIO21	55	I/O	Input (High-Z)	General Purpose Digital I/O 21. Float pin when unused
HRESET	44	I/O	Input	Active high hardware reset input. Will reinitialize all device settings. Ground pin when HRESET functionality will not be used
I2C1_IRQ	29	O	High-Z	I2C port 1 interrupt. Active low. Implement externally as an open drain with a pull-up resistance. Float pin when unused
I2C1_SCL	27	I/O	High-Z	I2C port 1 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
I2C1_SDA	28	I/O	High-Z	I2C port 1 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
I2C2_IRQ	34	O	High-Z	I2C port 2 interrupt. Active low. Implement externally as an open drain with a pull-up resistance. Float pin when unused
I2C2_SCL	32	I/O	High-Z	I2C port 2 serial clock. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
I2C2_SDA	33	I/O	High-Z	I2C port 2 serial data. Open-drain output. Tie pin to I/O voltage through a 10-kΩ resistance when used or unused
LDO_1V8	35	PWR	—	Output of the 1.8-V LDO for internal circuitry. Bypass with capacitor to GND
LDO_3V3	9	PWR	—	Output of the VBUS to 3.3-V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power external flash memory. Bypass with capacitor to GND
PP_CABLE	25	PWR	—	5-V supply input for port 1 C_CC pins. Bypass with capacitor to GND
PP_HV1	11, 12	PWR	—	System side of first VBUS power switch. Bypass with capacitor to ground. Tie to ground when unused
PP_HV2	1, 2	PWR	—	System side of second VBUS power switch. Bypass with capacitor to ground. Tie to ground when unused
SPI_CLK	38	I/O	Input	SPI serial clock. Ground pin when unused
SPI_POCI	36	I/O	Input	SPI serial controller input from peripheral. Ground pin when unused
SPI_PICO	37	I/O	Input	SPI serial controller output to peripheral. Ground pin when unused
SPI_CS	39	I/O	Input	SPI chip select. Ground pin when unused
VBUS1	13, 14	PWR	—	Port side of first VBUS power switch. Bypass with capacitor to ground. Tie to VBUS2

**表 5-1. Pin Functions (continued)**

PIN		TYPE <sup>(2)</sup>	RESET STATE <sup>(1)</sup>	DESCRIPTION
NAME	NO.			
VBUS2	3, 4	PWR	—	Port side of second VBUS power switch. Bypass with capacitor to ground. Tie to VBUS1
VIN_3V3	5	PWR	—	Supply for core circuitry and I/O. Bypass with capacitor to GND
Thermal Pad (PPAD)	59	GND	—	Ground reference for the device as well as thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad must be connected to a ground plane

(1) Reset State indicates the state of a given pin immediately following power application, prior to any configuration from firmware.

(2) I = input, O = output, I/O = bidirectional, GND = ground, PWR = power, NC = no connect

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage <sup>(2)</sup>	PP_CABLE	-0.3	6	V
	VIN_3V3	-0.3	3.6	
Output voltage <sup>(2)</sup>	LDO_1V8	-0.3	2	V
	LDO_3V3	-0.3	3.6	
I/O voltage <sup>(2)</sup>	I2Cx IRQ, SPI_PICO, SPI_CLK, SPI_CS, SWD_CLK	-0.3	LDO_3V3 + 0.3 <sup>(3)</sup>	V
	PP_HVx, VBUSx <sup>(4)</sup>	-0.3	24	
	I2Cx_SDA, I2Cx_SCL, SPI_POCI, GPIOn, HRESET, ADCINx	-0.3	LDO_3V3 + 0.3 <sup>(3)</sup>	
	C_USB_P, C_USB_N	-0.5	6	
C_CC1, C_CC2		-0.5	6	
Operating junction temperature, T <sub>J</sub>		-10	125	°C
Operating junction temperature PPHV switch, T <sub>J</sub>		-10	150	°C
Storage temperature, T <sub>stg</sub>		-55	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to underside power pad. The underside power pad should be directly connected to the ground plane of the board.
- (3) Not to exceed 3.6V
- (4) For VBUSx a TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Input voltage, V <sub>I</sub> <sup>(1)</sup>	VIN_3V3	3.135		3.45	V
	PP_CABLE	2.95		5.5	
	PP_HV	4.5		22	
I/O voltage, V <sub>IO</sub> <sup>(1)</sup>	VBUS	4		22	V
	C_USB_P, C_USB_N	0		LDO_3V3	
	C_CC1, C_CC2	0		5.5	
	GPIOn, I2Cx_SDA, I2Cx_SCL, SPI, ADCIN1, ADCIN2	0		LDO_3V3	
Operating ambient temperature, T <sub>A</sub>		-10		75	°C
Operating junction temperature, T <sub>J</sub>		-10		125	

- (1) All voltage values are with respect to underside power pad. Underside power pad must be directly connected to ground plane of the board.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65987	UNIT
		RSH (QFN)	
		56 PINS	
R <sub>θJA</sub> <sup>(2)</sup>	Junction-to-ambient thermal resistance	57.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	65.4	°C/W
R <sub>θJB</sub> <sup>(2)</sup>	Junction-to-board thermal resistance	30	°C/W
Ψ <sub>JT</sub> <sup>(2)</sup>	Junction-to-top characterization parameter	34.1	°C/W
Ψ <sub>JB</sub> <sup>(2)</sup>	Junction-to-board characterization parameter	29.9	°C/W
R <sub>θJC(bot_Controller)</sub>	Junction-to-case (bottom GND pad) thermal resistance	0.7	°C/W
R <sub>θJC(bot_FET)</sub>	Junction-to-case (bottom DRAIN 1/2 pad) thermal resistance	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) Thermal metrics are not JDEC standard values and are based on the TPS65988 evaluation board.

## 6.5 Power Supply Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>EXTERNAL</b>						
V <sub>IN_3V3</sub>	Input 3.3-V supply	3.135	3.3	3.45	V	
PP_CABLE	Input to power Vconn output on C_CC pins	2.95	5	5.5	V	
PP_HV	Source power from PP_HV to VBUS	4.5	5	22	V	
VBUS	Sink power from VBUS to PP_HV	4	5	22	V	
C <sub>VIN_3V3</sub>	Recommended capacitance on the VIN_3V3 pin	5	10		µF	
C <sub>PP_CABLE</sub>	Recommended capacitance on PPx_CABLE pins	2.5	4.7		µF	
C <sub>PP_HV_SRC</sub>	Recommended capacitance on PP_HVx pin when configured as a source	2.5	4.7		µF	
C <sub>PP_HV_SNK</sub>	Recommended capacitance on PP_HVx pin when configured as a sink	1	47	120	µF	
C <sub>VBUS</sub>	Recommended capacitance on VBUSx pins	0.5	1	12	µF	
<b>INTERNAL</b>						
V <sub>LDO_3V3</sub>	Output voltage of LDO from VBUS to LDO_3V3	VIN_3V3 = 0 V, VBUS1 ≥ 4 V, 0 ≤ I <sub>LOAD</sub> ≤ 50mA	3.15	3.3	3.45	V
V <sub>DO_LDO_3V3</sub>	Drop out voltage of LDO_3V3 from VBUS	I <sub>LOAD</sub> = 50mA	250	500	850	mV
I <sub>LDO_3V3_EX</sub>	Allowed External Load current on LDO_3V3 pin			25	mA	
V <sub>LDO_1V8</sub>	Output voltage of LDO_1V8	0 ≤ I <sub>LOAD</sub> ≤ 20mA	1.75	1.8	1.85	V
V <sub>FWD_DROP</sub>	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	I <sub>LOAD</sub> = 50 mA		200	mV	
C <sub>LDO_3V3</sub>	Recommended capacitance on LDO_3V3 pin		5	10	25	µF
C <sub>LDO_1V8</sub>	Recommended capacitance on LDO_1V8 pin		2.2	4.7	6	µF
<b>SUPERVISORY</b>						
UV_LDO3V3	Undervoltage threshold for LDO_3V3. Locks out 1.8-V LDOs	LDO_3V3 rising	2.2	2.325	2.45	V

## 6.5 Power Supply Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVH_LDO3V3	Undervoltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_PCBL	Undervoltage threshold for PP_CABLE	PP_CABLE rising	2.5	2.625	2.75	V
UVH_PCBL	Undervoltage hysteresis for PP_CABLE	PP_CABLE falling	20	50	80	mV
OV_VBUS	Ovvoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS rising	5		24	V
OVLSB_VBUS	Ovvoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS rising			328	mV
OVH_VBUS	Ovvoltage hysteresis for VBUS	VBUS falling, % of OV_VBUS	1.4	1.65	1.9	%
UV_VBUS	Undervoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS falling	2.5		18.21	V
UVLSB_VBUS	Undervoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS falling			249	mV
UVH_VBUS	Undervoltage hysteresis for VBUS	VBUS rising, % of UV_VBUS	0.9	1.3	1.7	%

## 6.6 Power Consumption Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>VIN_3V3</sub> <sup>(1)</sup>	Sleep (Sink)	VIN_3V3 = 3.3 V, VBUS = 0 V, No cable connected, T <sub>j</sub> = 25C, configured as sink, BC1.2 disabled		45		µA
	Sleep (Source/DRP)	VIN_3V3 = 3.3 V, VBUS = 0 V, No cable connected, T <sub>j</sub> = 25C, configured as source or DRP, BC1.2 disabled		55		µA
I <sub>VIN_3V3</sub> <sup>(1)</sup>	Idle (Attached)	VIN_3V3 = 3.3 V, Cable connected, No active PD communication, T <sub>j</sub> = 25C		5		mA
I <sub>VIN_3V3</sub> <sup>(1)</sup>	Active	VIN_3V3 = 3.3 V, T <sub>j</sub> = 25C		8		mA

(1) Does not include current draw due to GPIO loading

## 6.7 Power Switch Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>PPCC</sub>	PP_CABLE to C_CCn power switch resistance	4.7 ≤ PP_CABLE ≤ 5.5		222	325	mΩ
		2.95 ≤ PP_CABLE < 4.7		269	414	mΩ
R <sub>PPHV</sub>	PP_HVx to VBUSx power switch resistance	T <sub>j</sub> = 25C		25	33	mΩ
I <sub>PPHV</sub>	Continuous current capability of power path from PP_HVx to VBUSx				5	A
I <sub>PPCC</sub>	Continuous current capability of power path from PP_CABLE to C_CCn	T <sub>j</sub> = 125C			320	mA
		T <sub>j</sub> = 85C			600	mA
I <sub>HVACT</sub>	Active quiescent current from PP_HV pin, EN_HV = 1	Source Configuration, Comparator RCP function enabled, I <sub>LOAD</sub> = 100mA			1	mA
I <sub>HVSD</sub>	Shutdown quiescent current from PP_HV pin, EN_HV = 0	V <sub>PPHV</sub> = 20V			100	µA

## 6.7 Power Switch Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>occ</sub>	Over Current Clamp Firmware Selectable Settings		1.140	1.267	1.393	A
			1.380	1.533	1.687	A
			1.620	1.800	1.980	A
			1.860	2.067	2.273	A
			2.100	2.333	2.567	A
			2.34	2.600	2.860	A
			2.580	2.867	3.153	A
			2.820	3.133	3.447	A
			3.060	3.400	3.74	A
			3.300	3.667	4.033	A
			3.540	3.933	4.327	A
			3.780	4.200	4.620	A
			4.020	4.467	4.913	A
			4.260	4.733	5.207	A
			4.500	5.00	5.500	A
			4.740	5.267	5.793	A
			4.980	5.533	6.087	A
			5.220	5.800	6.380	A
			5.460	6.067	6.673	A
			5.697	6.330	6.963	A
I <sub>OCP</sub>	PP_HV Quick Response Current Limit			10		A
I <sub>LIMPPCC</sub>	PP_CABLE current limit		0.6	0.75	0.9	A
I <sub>HV_ACC 1</sub>	PP_HV current sense accuracy	I = 100 mA, Reverse current blocking disabled	3.9	6	8.1	A/V
I <sub>HV_ACC 1</sub>	PP_HV current sense accuracy	I = 200 mA	4.8	6	7.2	A/V
I <sub>HV_ACC 1</sub>	PP_HV current sense accuracy	I = 500 mA	5.28	6	6.72	A/V
I <sub>HV_ACC 1</sub>	PP_HV current sense accuracy	I ≥ 1 A	5.4	6	6.6	A/V
t <sub>ON_HV</sub>	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage	Configured as a source or as a sink with soft start disabled. PP_HV = 20 V, CVBUS = 10 µF, I <sub>LOAD</sub> = 100 mA			8	ms
t <sub>ON_FRS</sub>	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage during an FRS enable	Configured as a source. PP_HV = 5 V, CVBUS = 10 µF, I <sub>LOAD</sub> = 100 mA			150	µs
t <sub>ON_CC</sub>	PP_CABLE path turn on time from enable to C_CCn = 95% of the PP_CABLE voltage	PP_CABLE = 5 V, C_CCn = 500 nF, I <sub>LOAD</sub> = 100 mA			2	ms
SS	Configurable soft start slew rate for sink configuration	I <sub>LOAD</sub> = 100mA, setting 0	0.270	0.409	0.45	V/ms
		I <sub>LOAD</sub> = 100mA, setting 1	0.6	0.787	1	V/ms
		I <sub>LOAD</sub> = 100mA, setting 2	1.2	1.567	1.7	V/ms
		I <sub>LOAD</sub> = 100mA, setting 3	2.3	3.388	3.6	V/ms
V <sub>REVPHV</sub>	Reverse current blocking voltage threshold for PP_HV switch	Diode Mode			6	mV
		Comparator Mode			3	mV
V <sub>SAFE0V</sub>	Voltage that is a safe 0 V per USB-PD specification		0		0.8	V
t <sub>SAFE0V</sub>	Voltage transition time to VSAFE0V				650	ms

## 6.7 Power Switch Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SRPOS	Maximum slew rate for positive voltage transitions			0.03	V/µs
SRNEG	Maximum slew rate for negative voltage transitions		-0.03		V/µs
$t_{STABLE}$	EN to stable time for both positive and negative voltage transitions			275	ms
$V_{SRCVALID}$	Supply output tolerance beyond $V_{SRCNEW}$ during time $t_{STABLE}$		-0.5	0.5	V
$V_{SRCNEW}$	Supply output tolerance		-5	5	%
$t_{VCONNDIS}$	Time from cable detach to $V_{VCONNDIS}$			250	ms
$V_{VCONNDIS}$	Voltage at which $V_{CONN}$ is considered discharged			150	mV

## 6.8 Cable Detection Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{H\_CC\_USB}$	Source Current through each C_CC pin when in a disconnected state and Configured as a Source advertising Default USB current to a peripheral device		73.6	80	86.4	µA
$I_{H\_CC\_1P5}$	Source Current through each C_CC pin when in a disconnected state when Configured as a Source advertising 1.5A to a UFP		165.6	180	194.4	µA
$I_{H\_CC\_3P0}$	Source Current through each C_CC pin when in a disconnected state and Configured as a Source advertising 3.0A to a UFP.	$V_{IN\_3V3} \geq 3.135 \text{ V}$ , $V_{CC} < 2.6 \text{ V}$	303.6	330	356.4	µA
$V_{D\_CCH\_USB}$	Voltage Threshold for detecting a Source attach when configured as a Sink and the Source is advertising Default USB current source capability		0.15	0.2	0.25	V
$V_{D\_CCH\_1P5}$	Voltage Threshold for detecting a Source advertising 1.5A source capability when configured as a Sink		0.61	0.66	0.7	V
$V_{D\_CCH\_3P0}$	Voltage Threshold for detecting a Source advertising 3A source capability when configured as a Sink		1.16	1.23	1.31	V
$V_{H\_CCD\_USB}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising Default USB current source capability.	$I_{H\_CC} = I_{H\_CC\_USB}$	1.5	1.55	1.65	V
$V_{H\_CCD\_1P5}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising 1.5A source capability	$I_{H\_CC} = I_{H\_CC\_1P5}$	1.5	1.55	1.65	V
$V_{H\_CCD\_3P0}$	Voltage Threshold for detecting a Sink attach when configured as a Source and advertising 3.0A source capability.	$I_{H\_CC} = I_{H\_CC\_3P0}$ $V_{IN\_3V3} \geq 3.135V$	2.45	2.55	2.615	V
$V_{H\_CCA\_USB}$	Voltage Threshold for detecting an active cable attach when configured as a Source and advertising Default USB current capability.		0.15	0.2	0.25	V
$V_{H\_CCA\_1P5}$	Voltage Threshold for detecting active cables attach when configured as a Source and advertising 1.5A capability.		0.35	0.4	0.45	V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>H_CCA_3P0</sub>	Voltage Threshold for detecting active cables attach when configured as a Source and advertising 3A capability.		0.75	0.8	0.85	V
R <sub>D_CC</sub>	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a Sink. LDO_3V3 powered.	V = 1V, 1.5V	4.59	5.1	5.61	kΩ
R <sub>D_CC_OPEN</sub>	Pulldown resistance through each C_CC pin when in a disabled state. LDO_3V3 powered.	V = 0V to LDO_3V3	500			kΩ
R <sub>D_DB</sub>	Pulldown resistance through each C_CC pin when LDO_3V3 unpowered	V = 1.5V, 2.0V	4.08	5.1	6.12	kΩ
R <sub>FRSWAP</sub>	Fast Role Swap signal pull down				5	Ω
V <sub>TH_FRS</sub>	Fast role swap request detection voltage threshold		490	520	550	mV

## 6.9 USB-PD Baseband Signal Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>COMMON</b>						
PD_BITRATE	PD data bit rate		270	300	330	Kbps
UI <sup>(2)</sup>	Unit interval (1/PD_BITRATE)		3.03	3.33	3.7	μs
CCBLPLUG <sup>(1)</sup>	Capacitance for a cable plug (each plug on a cable may have up to this value)				25	pF
ZCABLE	Cable characteristic impedance		32	65		Ω
CRECEIVER <sup>(3)</sup>	Receiver capacitance. Capacitance looking into C_CCn pin when in receiver mode.			100		pF
<b>TRANSMITTER</b>						
ZDRIVER	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750kHz) while the source is driving the C_CCn line.		33	75		Ω
t <sub>RISE</sub>	Rise time. 10 % to 90 % amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
t <sub>FALL</sub>	Fall time. 90 % to 10 % amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300			ns
V <sub>TX</sub>	Transmit high voltage		1.05	1.125	1.2	V
<b>RECEIVER</b>						
V <sub>RXTR</sub>	Rx receive rising input threshold	Port configured as Source	840	875	910	mV
V <sub>RXTR</sub>	Rx receive rising input threshold	Port configured as Sink	504	525	546	mV
V <sub>RXTF</sub>	Rx receive falling input threshold	Port configured as Sink	240	250	260	mV
V <sub>RXTF</sub>	Rx receive falling input threshold	Port configured as Source	576	600	624	mV
NCOUNT	Number of transitions for signal detection (number to count to detect non-idle bus).		3			
TTRANWIN	Time window for detecting non-idle bus.		12	20		μs

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZBMCRX	Receiver input impedance	Does not include pull-up or pulldown resistance from cable detect. Transmitter is Hi-Z.	5			MΩ
TRXFILTER <sup>(4)</sup>	Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingression		100			ns

- (1) The capacitance of the bulk cable is not included in the CCBLPLUG definition. It is modeled as a transmission line.
- (2) UI denotes the time to transmit an unencoded data bit not the shortest high or low times on the wire after encoding with BMC. A single data bit cell has duration of 1 UI, but a data bit cell with value 1 will contain a centrally place 01 or 10 transition in addition to the transition at the start of the cell.
- (3) RECEIVER includes only the internal capacitance on a C\_CCn pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications. TI recommends adding capacitance to bring the total pin capacitance to 300 pF for improved TX behavior.
- (4) Broadband noise ingression is because of coupling in the cable interconnect.

## 6.10 BC1.2 Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DATA CONTACT DETECT</b>						
ID <sub>P_SRC</sub>	DCD source current	LDO_3V3 = 3.3 V	7	10	13	μA
R <sub>DM_DWN</sub>	DCD pulldown resistance		14.25	20	24.8	kΩ
R <sub>DP_DWN</sub>	DCD pulldown resistance		14.25	20	24.8	kΩ
V <sub>LGC_HI</sub>	Threshold for no connection	C_USB_P ≥ VLGC_HI, LDO_3V3 = 3.3 V	2			V
V <sub>LGC_LO</sub>	Threshold for connection	C_USB_P ≤ VLGC_LO			0.8	V
<b>PRIMARY AND SECONDARY DETECT</b>						
V <sub>DX_SRC</sub>	Source voltage		0.55	0.6	0.65	V
V <sub>DX_ILIM</sub>	V <sub>DX_SRC</sub> current limit		250	400		μA
I <sub>DX_SNK</sub>	Sink Current	V <sub>C_USB_TN/BN</sub> ≥ 250 mV	25	75	125	μA
R <sub>DCP_DAT</sub>	Dedicated Charging Port Resistance				200	Ω
<b>DIVIDER MODE</b>						
VC <sub>x_USB_P_2.7V</sub>	C <sub>x_USB_P</sub> Output Voltage	No load on C <sub>x_USB_P</sub>	2.57	2.7	2.79	V
VC <sub>x_USB_N_2.7V</sub>	C <sub>x_USB_N</sub> Output Voltage	No load on C <sub>x_USB_N</sub>	2.57	2.7	2.79	V
RC <sub>x_USB_P_30k</sub>	C <sub>x_USB_P</sub> Output Impedance	5μA pulled from C <sub>x_USB_P</sub> pin	24	30	36	kΩ
RC <sub>x_USB_N_30k</sub>	C <sub>x_USB_N</sub> Output Impedance	5μA pulled from C <sub>x_USB_N</sub> pin	24	30	36	kΩ
<b>1.2V MODE</b>						
RC <sub>x_USB_N_102k</sub>	C <sub>x_USB_N</sub> Output Impedance	5μA pulled from C <sub>x_USB_N</sub> pin	80	102	130	kΩ
VC <sub>x_USB_P_1.2V</sub>	C <sub>x_USB_P</sub> Output Voltage	No load on C <sub>x_USB_P</sub>	1.12	1.2	1.28	V
VC <sub>x_USB_N_1.2V</sub>	C <sub>x_USB_N</sub> Output Voltage	No load on C <sub>x_USB_N</sub>	1.12	1.2	1.28	V
RC <sub>x_USB_P_102k</sub>	C <sub>x_USB_P</sub> Output Impedance	5μA pulled from C <sub>x_USB_P</sub> pin	80	102	130	kΩ

## 6.11 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>SD_MAIN</sub>	Thermal Shutdown Temperature of the main thermal shutdown	Temperature rising	145	160	175	°C
T <sub>SDH_MAIN</sub>	Thermal Shutdown hysteresis of the main thermal shutdown	Temperature falling		20		°C
T <sub>SD_PWR</sub>	Thermal Shutdown Temperature of the power path block	Temperature rising	145	160	175	°C
T <sub>SDH_PWR</sub>	Thermal Shutdown hysteresis of the power path block	Temperature falling		20		°C

## 6.12 Oscillator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<i>f</i> <sub>OSC_24M</sub>	24-MHz oscillator		22.8	24	25.2	MHz
<i>f</i> <sub>OSC_100K</sub>	100-kHz oscillator		95	100	105	kHz

## 6.13 I/O Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SPI</b>						
SPI_VIH	High-level input voltage	LDO_1V8 = 1.8V		1.3		V
SPI_VIL	Low input voltage	LDO_1V8 = 1.8V			0.63	V
SPI_HYS	Input hysteresis voltage	LDO_1V8 = 1.8V		0.09		V
SPI_ILKG	Leakage current	Output is Hi-Z, VIN = 0 to LDO_3V3	-1		1	µA
SPI_VOH	SPI output high voltage	IO = -2 mA, LDO_3V3 = 3.3 V	2.88			V
SPI_VOL	SPI output low voltage	IO = 2 mA			0.4	V
<b>SWDIO</b>						
<b>SWDCLK</b>						
<b>GPIO</b>						
GPIO_VIH	High-level input voltage	LDO_1V8 = 1.8 V		1.3		V
GPIO_VIL	Low input voltage	LDO_1V8 = 1.8 V			0.63	V
GPIO_HYS	Input hysteresis voltage	LDO_1V8 = 1.8 V		0.09		V
GPIO_ILKG	I/O leakage current	INPUT = 0 V to VDD	-1		1	µA
GPIO_RPU	Pullup resistance	Pullup enabled	50	100	150	kΩ
GPIO_RPD	Pulldown resistance	Pulldown enabled	50	100	150	kΩ
GPIO_DG	Digital input path deglitch			20		ns
GPIO_VOH	GPIO output high voltage	IO = -2 mA, LDO_3V3 = 3.3 V	2.88			V
GPIO_VOL	GPIO output low voltage	IO = 2 mA, LDO_3V3 = 3.3 V			0.4	V
<b>I2C_IRQx</b>						
OD_VOL	Low-level output voltage	I <sub>OL</sub> = 2 mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, VIN = 0 to LDO_3V3	-1		1	µA

## 6.14 I<sup>2</sup>C Requirements and Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SDA AND SCL COMMON CHARACTERISTICS</b>						
I <sub>LEAK</sub>	Input leakage current	Voltage on Pin = LDO_3V3	-3	3	µA	
V <sub>OL</sub>	SDA output low voltage	I <sub>OL</sub> = 3 mA, LDO_3V3 = 3.3 V		0.4	V	
I <sub>OL</sub>	SDA max output low current	V <sub>OL</sub> = 0.4 V	3		mA	
		V <sub>OL</sub> = 0.6 V	6		mA	
V <sub>IL</sub>	Input low signal	LDO_3V3 = 3.3 V		0.99	V	
		LDO_1V8 = 1.8 V		0.54	V	
V <sub>IH</sub>	Input high signal	LDO_3V3 = 3.3 V	2.31		V	
		LDO_1V8 = 1.8 V	1.3		V	
V <sub>HYS</sub>	Input hysteresis	LDO_3V3 = 3.3 V	0.17		V	
		LDO_1V8 = 1.8 V	0.09		V	
t <sub>SP</sub>	I <sup>2</sup> C pulse width suppressed			50	ns	
C <sub>I</sub>	Pin capacitance			10	pF	
<b>SDA AND SCL STANDARD MODE CHARACTERISTICS</b>						
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency		0	100	kHz	
t <sub>HIGH</sub>	I <sup>2</sup> C clock high time		4		µs	
t <sub>LOW</sub>	I <sup>2</sup> C clock low time		4.7		µs	
t <sub>SU;DAT</sub>	I <sup>2</sup> C serial data setup time		250		ns	
t <sub>HD;DAT</sub>	I <sup>2</sup> C serial data hold time		0		ns	
t <sub>VD;DAT</sub>	I <sup>2</sup> C valid data time	SCL low to SDA output valid		3.45	µs	
t <sub>VD;ACK</sub>	I <sup>2</sup> C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs	
t <sub>OCF</sub>	I <sup>2</sup> C output fall time	10 pF to 400 pF bus		250	ns	
t <sub>BUF</sub>	I <sup>2</sup> C bus free time between stop and start		4.7		µs	
t <sub>SU;STA</sub>	I <sup>2</sup> C start or repeated Start condition setup time		4.7		µs	
t <sub>HD;STA</sub>	I <sup>2</sup> C Start or repeated Start condition hold time		4		µs	
t <sub>SU;STO</sub>	I <sup>2</sup> C Stop condition setup time		4		µs	
<b>SDA AND SCL FAST MODE CHARACTERISTICS</b>						
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	Configured as Slave	0	400	kHz	
f <sub>SCL_MASTER</sub>	I <sup>2</sup> C clock frequency	Configured as Master	0	320	400	kHz
t <sub>HIGH</sub>	I <sup>2</sup> C clock high time		0.6		µs	
t <sub>LOW</sub>	I <sup>2</sup> C clock low time		1.3		µs	
t <sub>SU;DAT</sub>	I <sup>2</sup> C serial data setup time		100		ns	
t <sub>HD;DAT</sub>	I <sup>2</sup> C serial data hold time		0		ns	
t <sub>VD;DAT</sub>	I <sup>2</sup> C Valid data time	SCL low to SDA output valid		0.9	µs	
t <sub>VD;ACK</sub>	I <sup>2</sup> C Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs	
t <sub>OCF</sub>	I <sup>2</sup> C output fall time	10 pF to 400 pF bus, V <sub>DD</sub> = 3.3 V	12	250	ns	
		10 pF to 400 pF bus, V <sub>DD</sub> = 1.8 V	6.5	250	ns	

## 6.14 I<sup>2</sup>C Requirements and Characteristics (continued)

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>BUF</sub>	I <sup>2</sup> C bus free time between stop and start		1.3			μs
t <sub>SU;STA</sub>	I <sup>2</sup> C start or repeated Start condition setup time		0.6			μs
t <sub>HD;STA</sub>	I <sup>2</sup> C Start or repeated Start condition hold time		0.6			μs
t <sub>SU;STO</sub>	I <sup>2</sup> C Stop condition setup time		0.6			μs

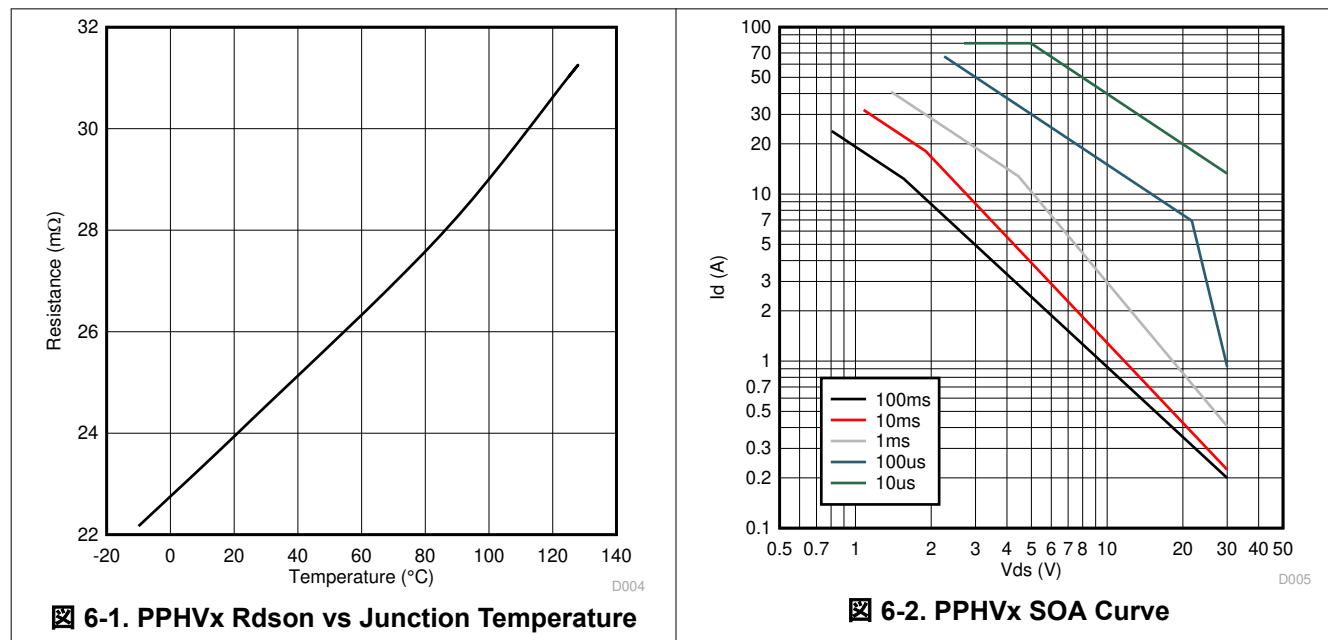
## 6.15 SPI Controller Timing Requirements

		MIN	NOM	MAX	UNIT
f <sub>SPI</sub>	Frequency of SPI_CLK	11.4	12	12.6	MHz
t <sub>PER</sub>	Period of SPI_CLK (1/F <sub>SPI</sub> )	79.36	83.33	87.72	ns
t <sub>WHI</sub>	SPI_CLK high width	30			ns
t <sub>WLO</sub>	SPI_CLK low width	30			ns
t <sub>DACT</sub>	SPI_SZZ falling to SPI_CLK rising delay time	30	50		ns
t <sub>DINACT</sub>	SPI_CLK falling to SPI_CSZ rising delay time	158	180		ns
t <sub>DPICO</sub>	SPI_CLK falling to SPI_PICO Valid delay time	-10	10		ns
t <sub>SUPOCI</sub>	SPI_POCI valid to SPI_CLK falling setup time	33			ns
t <sub>HDMSIO</sub>	SPI_CLK falling to SPI_POCI invalid hold time	0			ns
t <sub>RIN</sub>	SPI_POCI input rise time			5	ns
t <sub>RSPI</sub>	SPI_CSZ/CLK/PICO rise time	10% to 90%, C <sub>L</sub> = 5 to 50 pF, LDO_3V3 = 3.3 V	1	25	ns
t <sub>FSPI</sub>	SPI_CSZ/CLK/PICO fall time	90% to 10%, C <sub>L</sub> = 5 to 50 pF, LDO_3V3 = 3.3 V	1	25	ns

## 6.16 HPD Timing Requirements

		MIN	NOM	MAX	UNIT	
<b>DP SOURCE SIDE (HPD TX)</b>						
t <sub>IRQ_MIN</sub>	HPD IRQ minimum assert time	675	750	825	μs	
t <sub>2 MS_MIN</sub>	HPD assert 2-ms min time	3	3.33	3.67	ms	
<b>DP SINK SIDE (HPD RX)</b>						
t <sub>HPD_HDB</sub>	HPD high debounce time	HPD_HDB_SEL = 0	300	375	450	μs
		HPD_HDB_SEL = 1	100	111	122	ms
t <sub>HPD_LDB</sub>	HPD low debounce time		300	375	450	μs
t <sub>HPD_IRQ</sub>	HPD IRQ limit time		1.35	1.5	1.65	ms

## 6.17 Typical Characteristics



## 7 Parameter Measurement Information

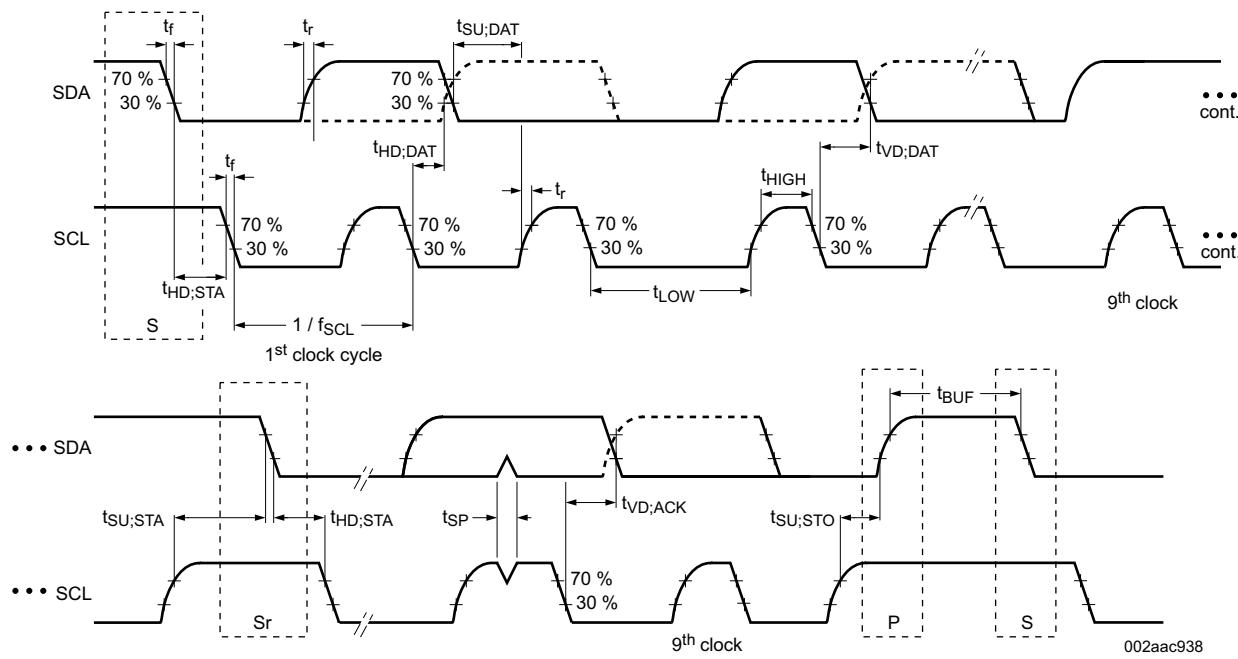


图 7-1. I<sup>2</sup>C Slave Interface Timing

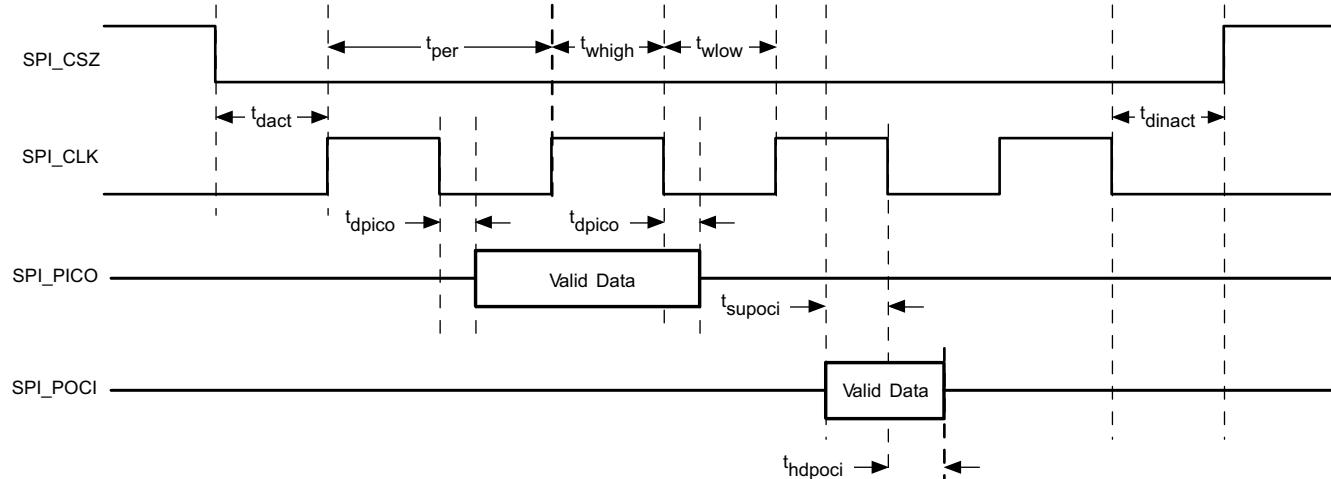


图 7-2. SPI Controller Timing

## 8 Detailed Description

### 8.1 Overview

The TPS65987DDJ is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for a USB Type-C and PD plug or receptacles. The TPS65987DDJ communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port power switch, controls an external high current port power switch and negotiates alternate modes. The TPS65987DDJ may also control an attached super-speed multiplexer via GPIO or I<sup>2</sup>C to simultaneously support USB3.0/3.1 data rates and DisplayPort video.

The TPS65987DDJ is divided into five main sections:

- USB-PD controller
- cable plug and orientation detection circuitry
- port power switches
- power management circuitry
- digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the C\_CC1 pin or the C\_CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features and more detailed circuitry, see the [USB-PD Physical Layer](#) section.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see the [Port Power Switches](#) section.

The port power switches provide power to the system port through the VBUS pin and also through the C\_CC1 or C\_CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, see the [Port Power Switches](#) section.

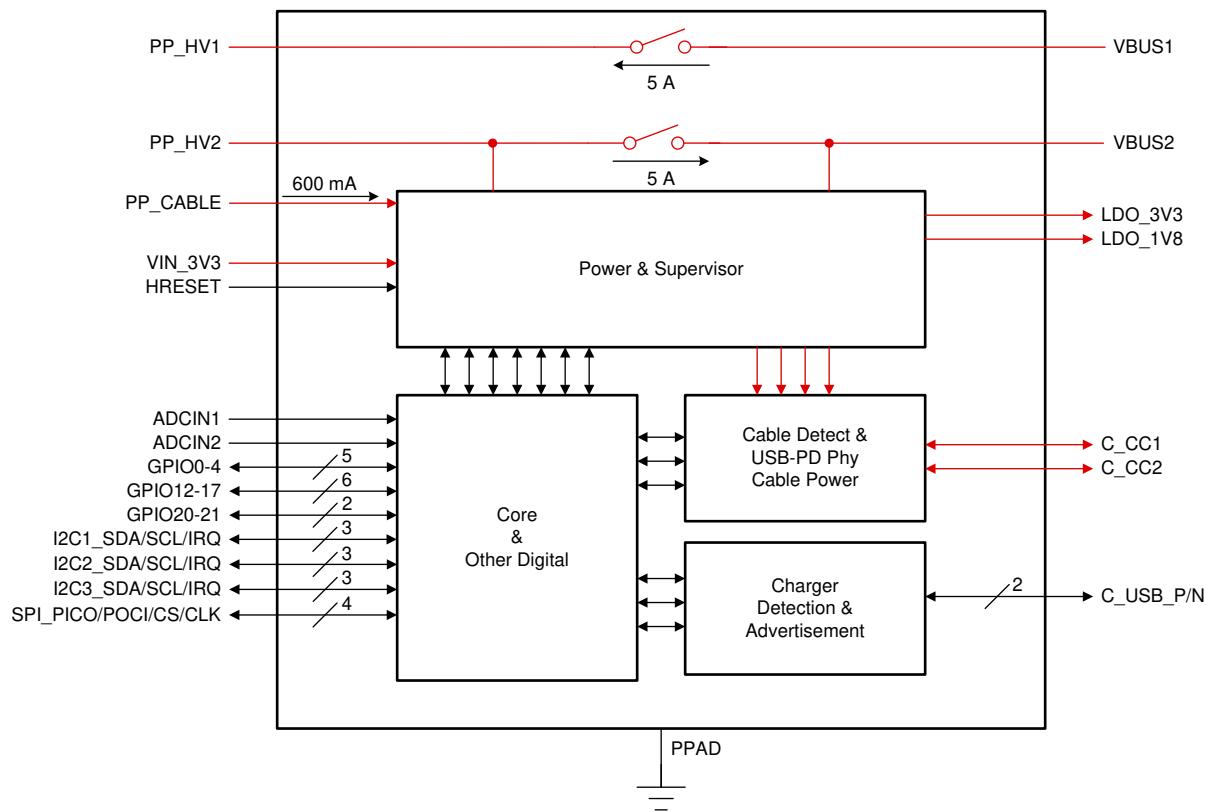
The power management circuitry receives and provides power to the TPS65987DDJ internal circuitry and to the LDO\_3V3 output. For a high-level block diagram of the power management circuitry, a description of its features and more detailed circuitry, see the [Power Management](#) section.

The digital core provides the engine for receiving, processing and sending all USB-PD packets as well as handling control of all other TPS65987DDJ functionality. A portion of the digital core contains ROM memory which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM called boot code, is capable of initializing the TPS65987DDJ, loading of device configuration information and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features and more detailed circuitry, see the [Digital Core](#) section.

The TPS65987DDJ is an I<sup>2</sup>C slave to be controlled by a host processor (see the [I<sup>2</sup>C Interfaces](#) section), and an SPI controller to write to and read from an optional external flash memory (see the [SPI Controller Interface](#) section).

The TPS65987DDJ also integrates a thermal shutdown mechanism (see the [Thermal Shutdown](#) section) and runs off of accurate clocks provided by the integrated oscillators (see the [Oscillators](#) section).

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 USB-PD Physical Layer

図 8-1 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

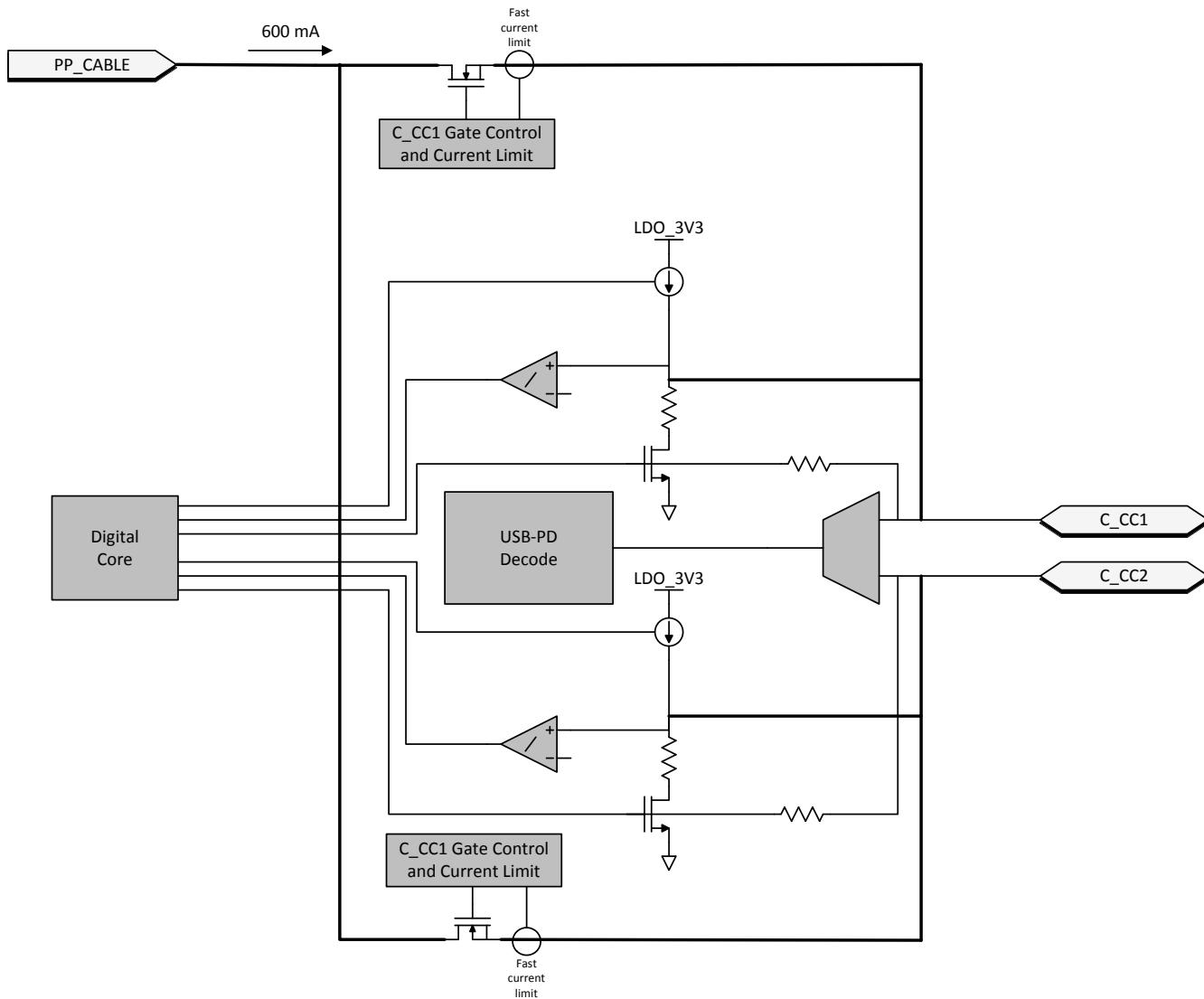


図 8-1. USB-PD Physical Layer, Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (C\_CC1 or C\_CC2) that is DC biased due to the DFP (or UFP) cable attach mechanism shown in [Port Power Switches](#).

### 8.3.1.1 USB-PD Encoding and Signaling

図 8-2 illustrates the high-level block diagram of the baseband USB-PD transmitter. 図 8-3 illustrates the high-level block diagram of the baseband USB-PD receiver.

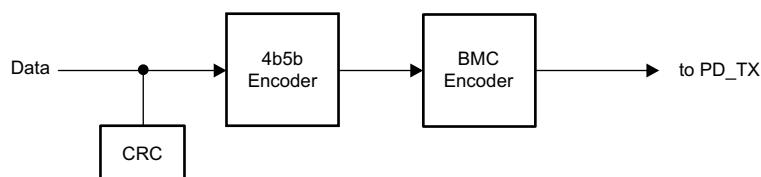


図 8-2. USB-PD Baseband Transmitter Block Diagram

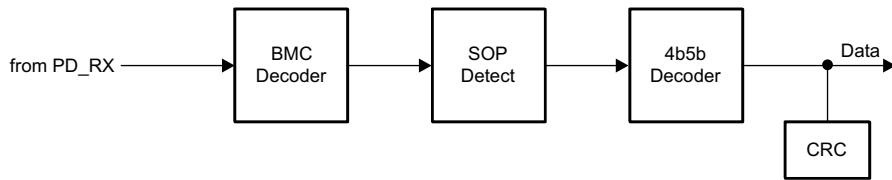


图 8-3. USB-PD Baseband Receiver Block Diagram

The USB-PD baseband signal is driven on the C\_CCn pins with a tri-state driver. The tri-state driver is slew rate limited to reduce the high frequency components imparted on the cable and to avoid interference with frequencies used for communication.

#### 8.3.1.2 USB-PD Bi-Phase Mark Coding

The USB-PD physical layer implemented in the TPS65987DDJ is compliant to the [USB-PD Specifications](#). The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). [图 8-4](#) illustrates Biphase Mark Coding.

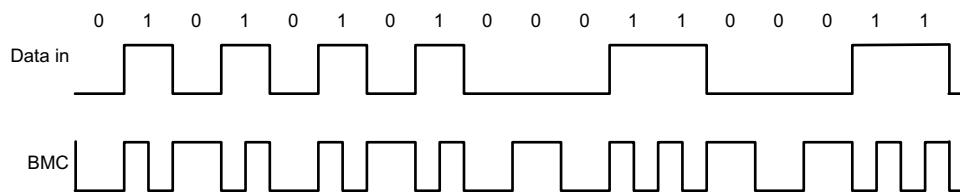


图 8-4. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the C\_CC1 or C\_CC2 pins with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D- and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

#### 8.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the [USB-PD Specifications](#) for more details.

#### 8.3.1.4 USB-PD BMC Transmitter

The TPS65987DDJ transmits and receives USB-PD data over one of the C\_CCn pins for a given CC pin pair (one pair per USB Type-C port). The C\_CCn pins are also used to determine the cable orientation (see [Port Power Switches](#)) and maintain the cable/device attach detection. Thus, a DC bias exists on the C\_CCn pins. The transmitter driver overdrives the C\_CCn DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the C\_CCn pin when not transmitting. [图 8-5](#) shows the USB-PD BMC TX and RX driver block diagram.

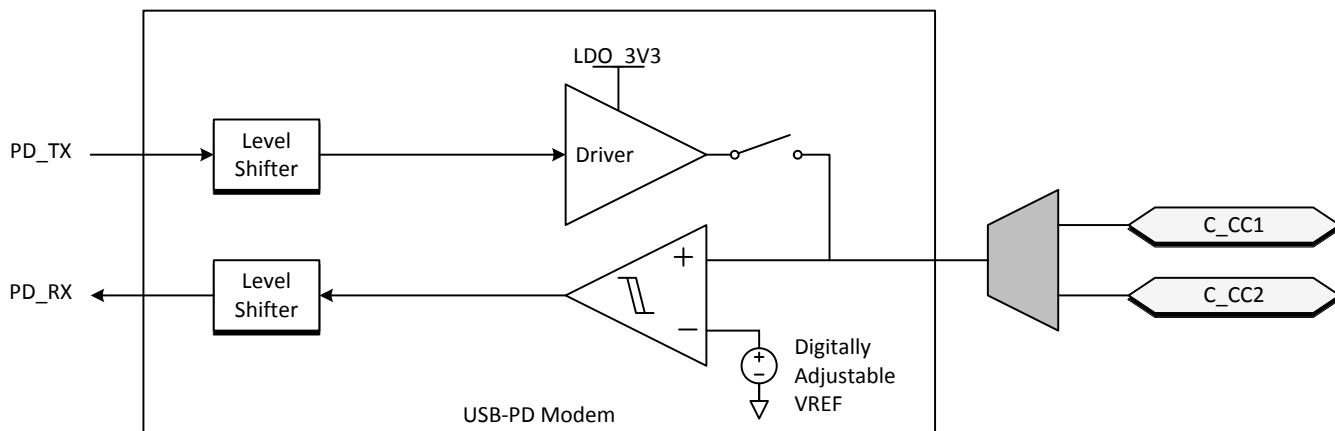


图 8-5. USB-PD BMC TX/Rx Block Diagram

图 8-6 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum threshold for detecting a UFP attach (VD\_CCH\_USB) and the maximum threshold for detecting a UFP attach to a DFP (VD\_CCH\_3P0). This means that the DC bias can be below VOH of the transmitter driver or above VOH.

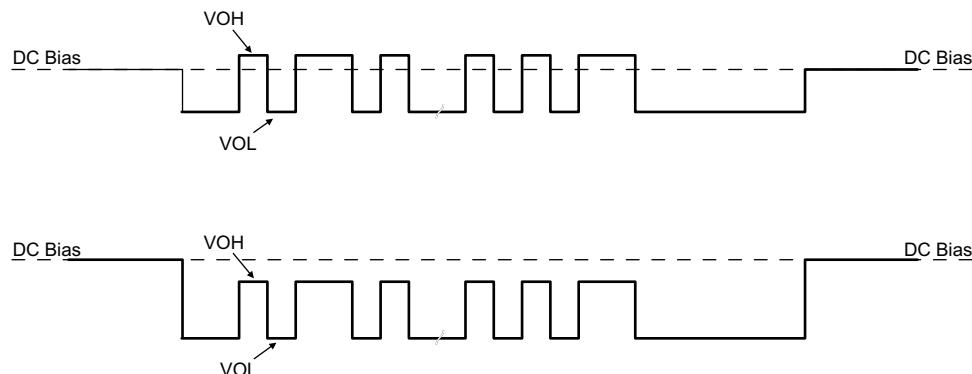


图 8-6. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the C\_CCN lines. The signal peak, VTXP, is set to meet the TX masks defined in the [USB-PD Specifications](#).

When driving the line, the transmitter driver has an output impedance of ZDRIVER. ZDRIVER is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. ZDRIVER impacts the noise ingress in the cable.

图 8-7 shows the simplified circuit determining ZDRIVER. It is specified such that noise at the receiver is bounded.

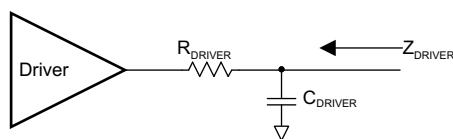


图 8-7. ZDRIVER Circuit

### 8.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS65987DDJ receives a signal that falls within the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

图 8-8 shows an example of a multi-drop USB-PD connection. This connection has the typical UFP (device) to DFP (host) connection, but also includes cable USB-PD TX/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (ZBMRX). The [USB-PD Specification](#) also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

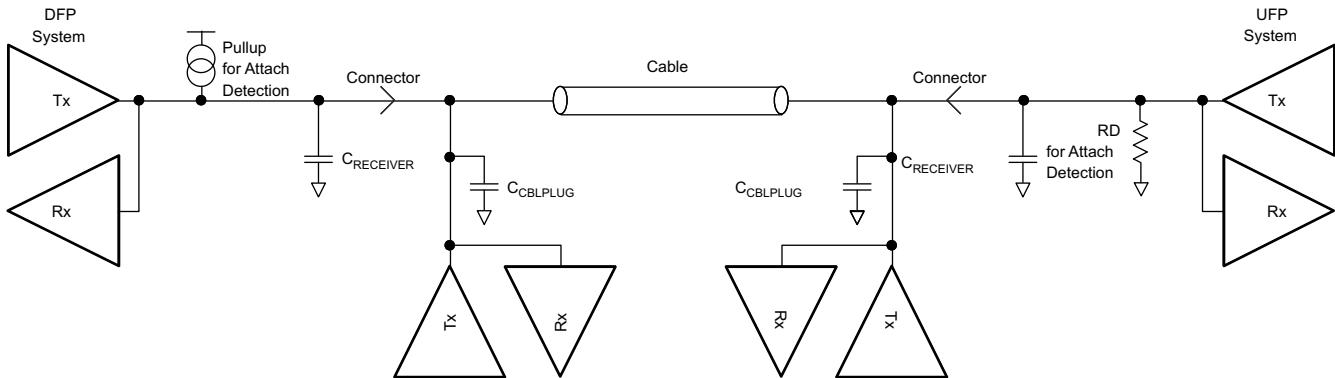


图 8-8. Example USB-PD Multi-Drop Configuration

### 8.3.2 Power Management

The TPS65987DDJ power management block receives power and generates voltages to provide power to the TPS65987DDJ internal circuitry. These generated power rails are LDO\_3V3 and LDO\_1V8. LDO\_3V3 may also be used as a low power output for external flash memory. The power supply path is shown in 图 8-9.

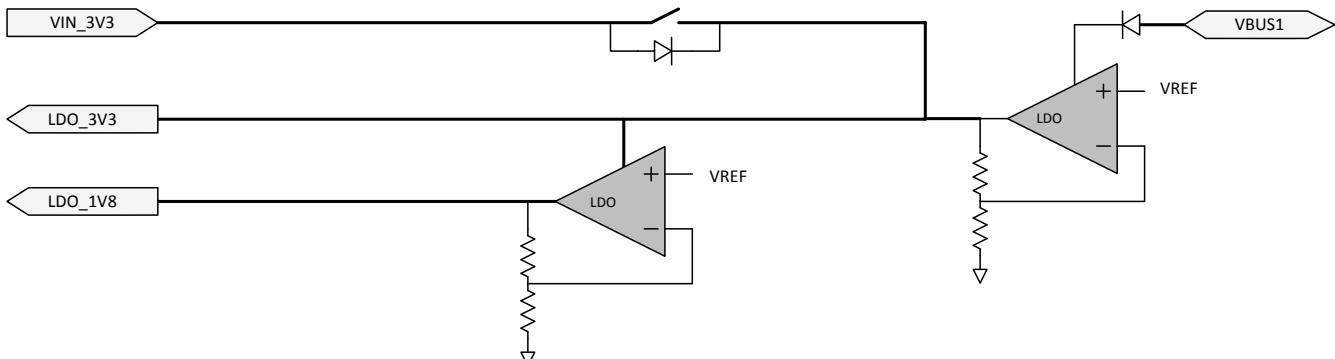


图 8-9. Power Supplies

The TPS65987DDJ is powered from either VIN\_3V3, VBUS1, or VBUS2. The normal power supply input is VIN3V3. In this mode, current flows from VIN\_3V3 to LDO3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO\_3V3 to LDO\_1V8 to power the 1.8-V core digital circuitry. When VIN\_3V3 power is unavailable and power is available on VBUS1 or VBUS2, the TPS65987DDJ is powered from VBUS. In this mode, the voltage on VBUS1 or VBUS 2 is stepped down through an LDO to LDO\_3V3.

#### 8.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

#### 8.3.2.2 VBUS LDO

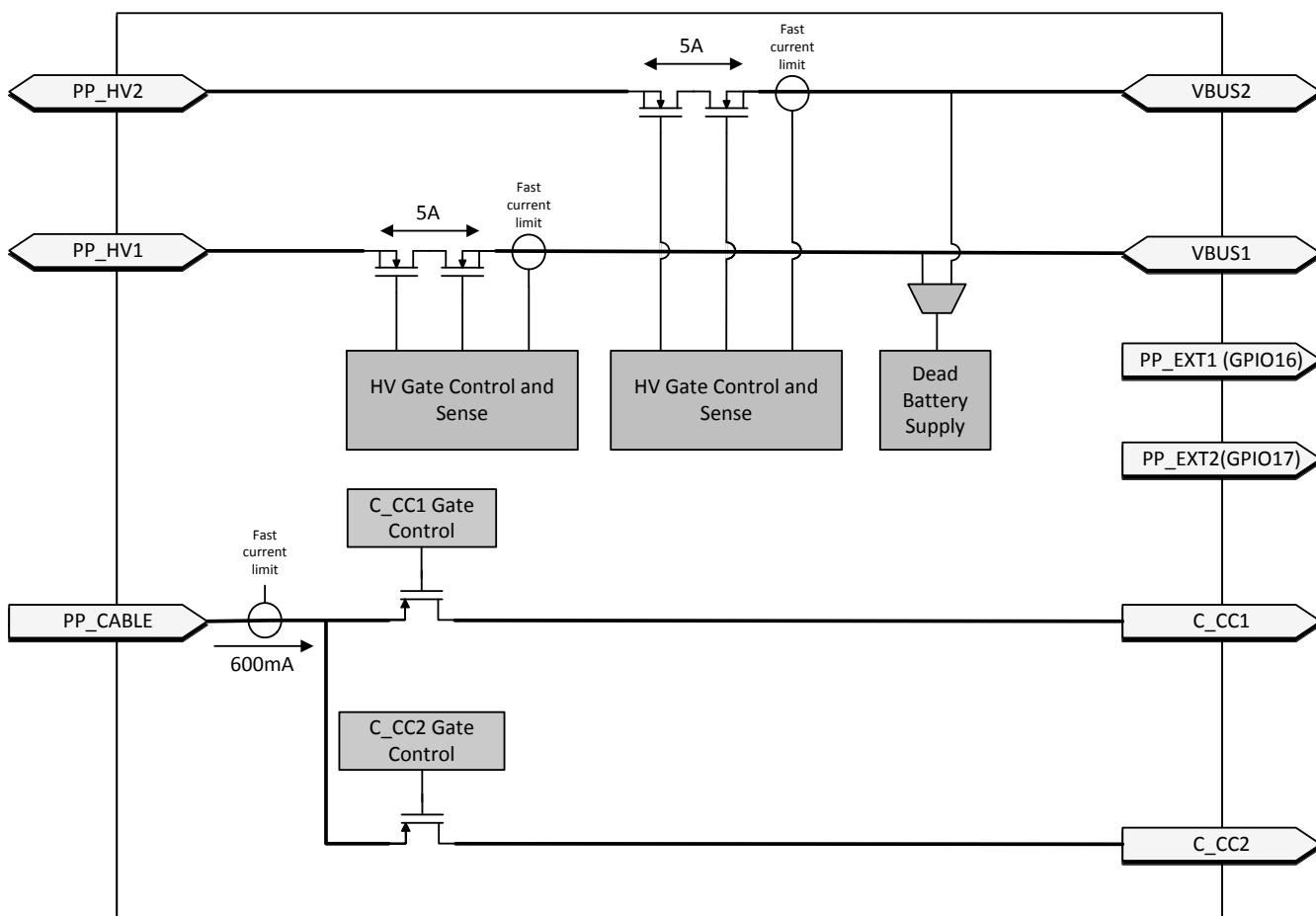
The TPS65987DDJ contains an internal high-voltage LDO which is capable of converting up to 22 V from VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used during dead battery operation while the VIN\_3V3 supply is not present. The VBUS LDO may be powered from either VBUS1 or VBUS2. The path connecting each VBUS to the internal LDO blocks reverse current, preventing power on one VBUS from leaking to the other. When power is present on both VBUS inputs, the internal LDO draws current from both VBUS pins.

### 8.3.2.3 Supply Switch Over

VIN\_3V3 takes precedence over VBUS, meaning that when both supply voltages are present the TPS65987DDJ powers from VIN\_3V3. See [图 8-9](#) for a diagram showing the power supply path block. There are two cases in which a power supply switch-over occurs. The first is when VBUS is present first and then VIN\_3V3 becomes available. In this case, the supply automatically switches over to VIN\_3V3 and brown-out prevention is verified by design. The other way a supply switch-over occurs is when both supplies are present and VIN\_3V3 is removed and falls below 2.85 V. In this case, a hard reset of the TPS65987DDJ is initiated by device firmware, prompting a re-boot.

### 8.3.3 Port Power Switches

The figure below shows the TPS65987DDJ internal power paths. The TPS65987DDJ features two internal high-voltage power paths. Each path contains two back to back common drain N-Fets, current monitor, overvoltage monitor, undervoltage monitor, and temperature sensing circuitry. Each path may conduct up to 5 A safely. Additional external paths may be controlled through the TPS65987DDJ GPIOs.



**图 8-10. Port Power Switches**

#### 8.3.3.1 PP\_HV Power Switch

The TPS65987DDJ has two integrated bi-directional high-voltage switches that are rated for up to 5 A of current. Each switch may be used as either a sink or source path for supporting USB-PD power up to 20 V at 5 A of current.

**注**

The power paths can sustain up to 5 A of continuous current as long as the internal junction temperature of each path remains below 150°C. Care should be taken to follow the layout recommendations described in [Thermal Dissipation for FET DRAIN Pads](#)

**注**

It is recommended to use PPHV1 as a sink path and PPHV2 as a source path.

**8.3.3.1.1 PP\_HV Overcurrent Clamp**

The internal source PP\_HV path has an integrated overcurrent clamp circuit. The current through the internal PP\_HV paths are current limited to  $I_{OCC}$ . The  $I_{OCC}$  value is selected by application firmware and only enabled while acting as a source. When the current through the switch exceeds  $I_{OCC}$ , the current clamping circuit activates and the path behaves as a constant current source. If the duration of the overcurrent event exceeds the deglitch time, the switch is latched off.

**8.3.3.1.2 PP\_HV Overcurrent Protection**

The TPS65987DDJ continuously monitors the forward voltage drop across the internal power switches. When a forward drop corresponding to a forward current of  $I_{OCP}$  is detected the internal power switch is latched off to protect the internal switches as well as upstream power supplies.

**8.3.3.1.3 PP\_HV OVP and UVP**

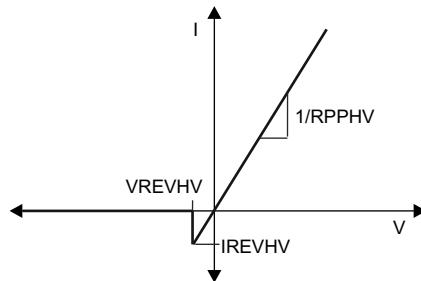
Both the overvoltage and undervoltage protection levels are configured by application firmware. When the voltage on a port's VBUS pin exceeds the set overvoltage threshold or falls below the set undervoltage threshold the associated PP\_HV path is automatically disabled.

**8.3.3.1.4 PP\_HV Reverse Current Protection**

The TPS65987DDJ reverse current protection has two modes of operation: Comparator Mode and Ideal Diode Mode. Both modes disable the power switch in cases of reverse current. The comparator protection mode is enabled when the switch is operating as a source, while the ideal diode protection is enabled while operating as a sink.

In the Comparator mode of reverse current protection, the power switch is allowed to behave resistively until the current reaches the amount calculated in [式 1](#) and then blocks reverse current from VBUS to PP\_HV. [图 8-11](#) shows the diode behavior of the switch with comparator mode enabled.

$$I_{REVHV} = V_{REVHV}/R_{PPHV} \quad (1)$$



**图 8-11. Comparator Mode (Source) Internal HV Switch I-V Curve**

In the Ideal Diode mode of reverse current protection, the switch behaves as an ideal diode and blocks reverse current from PP\_HV to VBUS. [图 8-12](#) shows the diode behavior of the switch with ideal diode mode enabled.

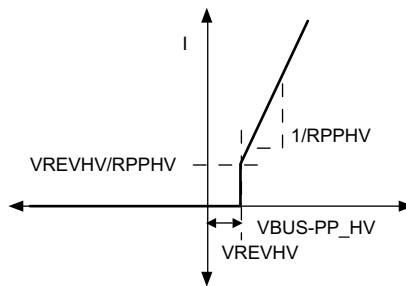


图 8-12. Ideal Diode Mode (Sink) Internal HV Switch I-V Curve

### 8.3.3.2 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS65987DDJ during sudden disconnects due to inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to ground as shown in [图 8-13](#).

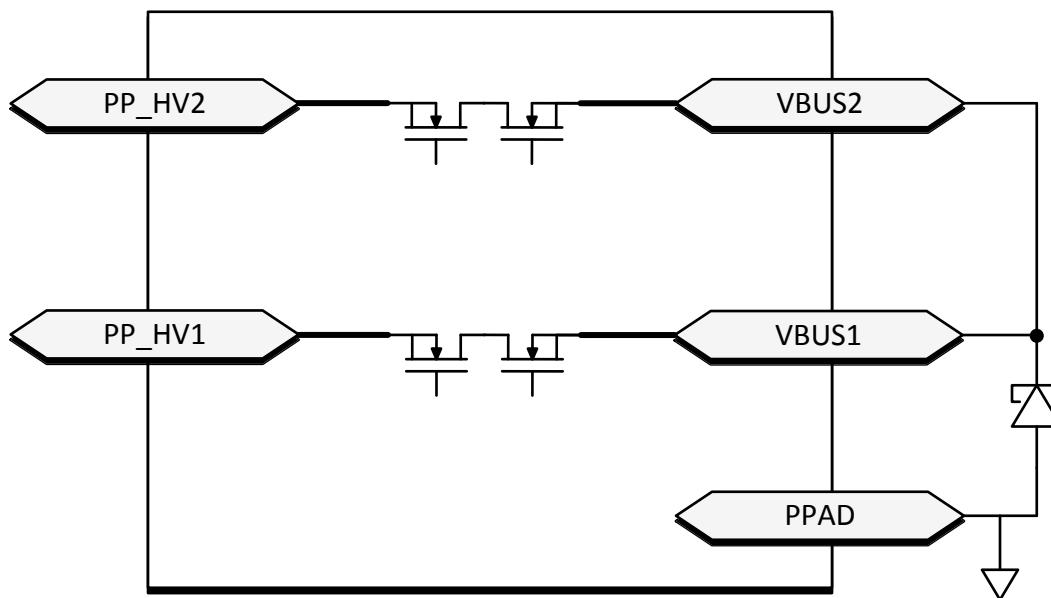


图 8-13. Schottky for Current Surge Protection

### 8.3.3.3 PP\_EXT Power Path Control

GPIO16 and GPIO17 of the TPS65987DDJ are intended for control of additional external power paths. These GPIO are active high when configured for external path control and disables in response to an OVP or UVP event. Overcurrent protection and thermal shutdown are not available for external power paths controlled by GPIO16 and GPIO17.

注

GPIO16 and GPIO17 must be pulled to ground through an external pull-down resistor when used as external path control signals.

### 8.3.3.4 PP\_CABLE Power Switch

The TPS65987DDJ has an integrated 5-V unidirectional power mux that is rated for up to 600 mA of current. The mux may supply power to either of the port CC pins for use as VCONN power.

#### 8.3.3.4.1 PP\_CABLE Overcurrent Protection

When enabled and providing VCONN power the TPS65987DDJ PP\_CABLE power switches have a 600-mA current limit. When the current through the PP\_CABLE switch exceeds 600 mA, the current limiting circuit activates and the switch behaves as a constant current source. The switches do not have reverse current blocking when the switch is enabled and current is flowing to either C\_CC1 or C\_CC2.

#### 8.3.3.4.2 PP\_CABLE Input Good Monitor

The TPS65987DDJ monitors the voltage at the PP\_CABLE pins prior to enabling the power switch. If the voltage at PP\_CABLE exceeds the input good threshold the switch is allowed to close, otherwise the switch remains open. Once the switch has been enabled, PP\_CABLE is allowed to fall below the input good threshold.

#### 8.3.3.5 VBUS Transition to VSAFE5V

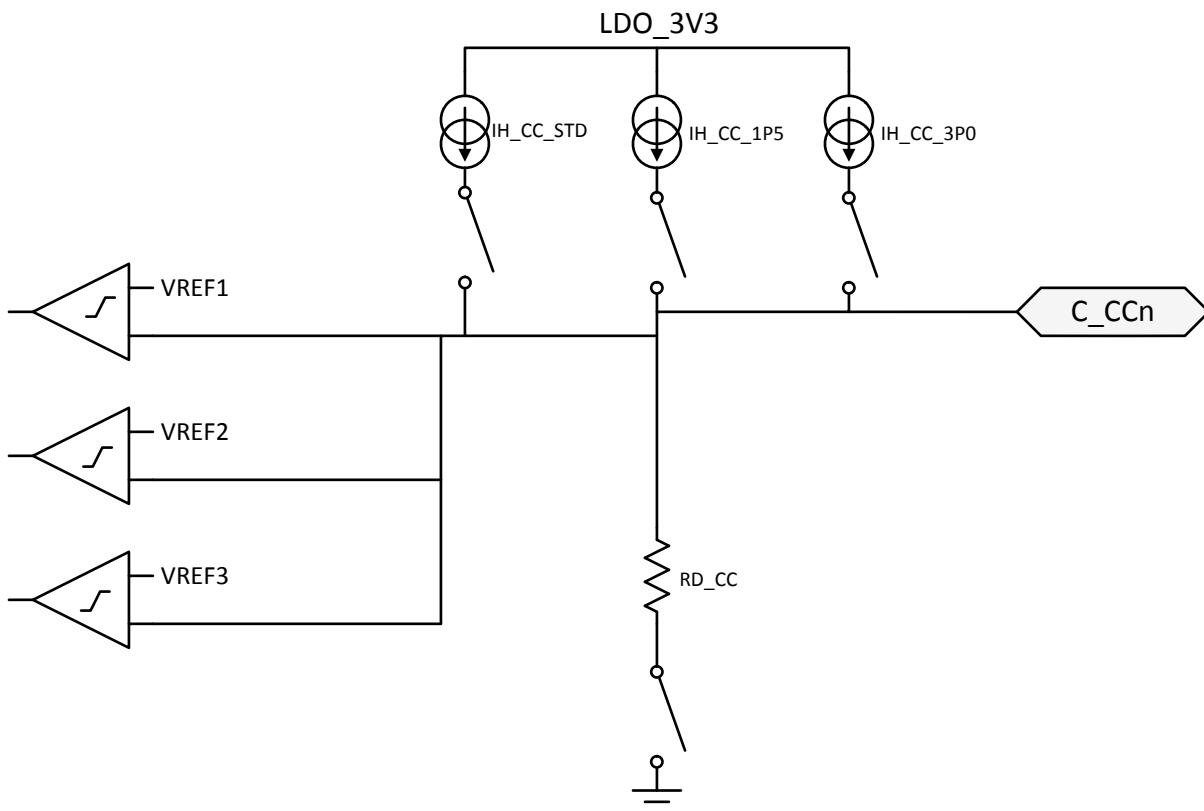
The TPS65987DDJ has an integrated active pull-down on VBUS for transitioning from high voltage to VSAFE5V. When the high voltage switch is disabled and VBUS > VSAFE5V, an amplifier turns on a current source and pulls down on VBUS. The amplifier implements active slew rate control by adjusting the pull-down current to prevent the slew rate from exceeding specification. When VBUS falls to VSAFE5V, the pull-down is turned off.

#### 8.3.3.6 VBUS Transition to VSAFE0V

When VBUS transitions to near 0 V (VSAFE0V), the pull-down circuit mentioned in [VBUS Transition to VSAFE5V](#) is turned on until VBUS reaches VSAFE0V. This transition occurs within time TSafe0V.

#### 8.3.4 Cable Plug and Orientation Detection

 8-14 shows the plug and orientation detection block at each C\_CCn pin (C\_CC1, C\_CC2). Each pin has identical detection circuitry.



 8-14. Plug and Orientation Detection Block

### 8.3.4.1 Configured as a DFP

When one of the TPS65987DDJ ports is configured as a DFP, the device detects when a cable or a UFP is attached using the C\_CC1 and C\_CC2 pins. When in a disconnected state, the TPS65987DDJ monitors the voltages on these pins to determine what, if anything, is connected. See [USB Type-C Specification](#) for more information.

表 8-1 shows the Cable Detect States for a DFP.

**表 8-1. Cable Detect States for a DFP**

C_CC1	C_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both C_CC pins for attach. Power is not applied to VBUS or VCONN until a UFP connect is detected.
Rd	Open	UFP attached	Monitor C_CC1 for detach. Power is applied to VBUS but not to VCONN (C_CC2).
Open	Rd	UFP attached	Monitor C_CC2 for detach. Power is applied to VBUS but not to VCONN (C_CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor C_CC2 for a UFP attach and C_CC1 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Open	Ra	Powered Cable-No UFP attached	Monitor C_CC1 for a UFP attach and C_CC2 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN (C_CC1) then monitor C_CC2 for a UFP detach. C_CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (C_CC2) then monitor C_CC1 for a UFP detach. C_CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either C_CC pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either C_CC pin for detach.

When a TPS65987DDJ port is configured as a DFP, a current IH\_CC is driven out each C\_CCn pin and each pin is monitored for different states. When a UFP is attached to the pin a pull-down resistance of Rd to GND exists. The current IH\_CC is then forced across the resistance Rd generating a voltage at the C\_CCn pin.

When configured as a DFP advertising Default USB current sourcing capability, the TPS65987DDJ applies IH\_CC\_USB to each C\_CCn pin. When a UFP with a pull-down resistance Rd is attached, the voltage on the C\_CCn pin pulls below VH\_CCD\_USB. The TPS65987DDJ can be configured to advertise default (500 mA or 900 mA), 1.5-A and 3-A sourcing capabilities when acting as a DFP.

When the C\_CCn pin is connected to an active cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the C\_CCn pin will pull below VH\_CCA\_USB/1P5/3P0 and the system recognizes the active cable.

The VH\_CCD\_USB/1P5/3P0 thresholds are monitored to detect a disconnection from each of these cases respectively. When a connection has been recognized and the voltage on the C\_CCn pin rises above the VH\_CCD\_USB/1P5/3P0 threshold, the system registers a disconnection.

### 8.3.4.2 Configured as a UFP

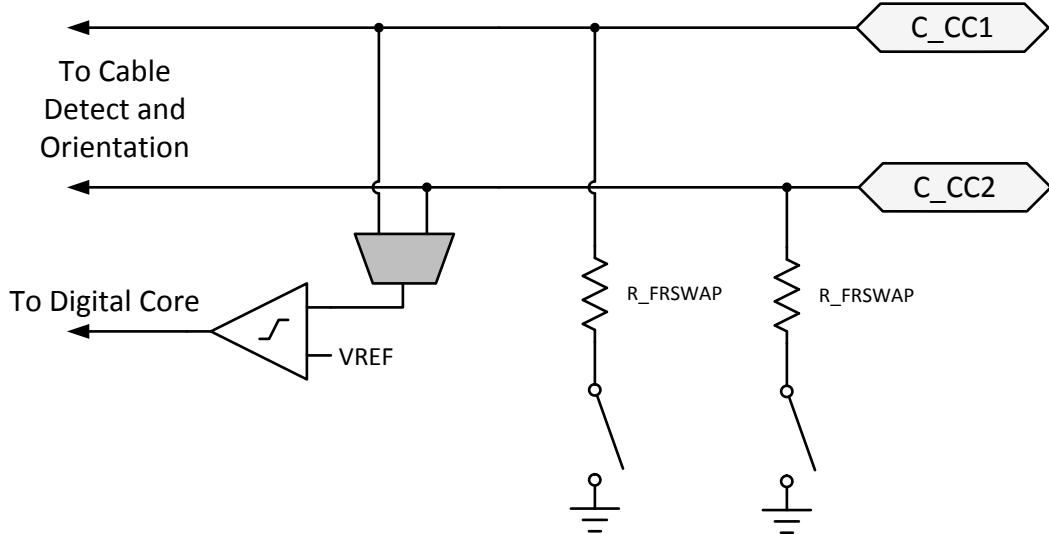
When a TPS65987DDJ port is configured as a UFP, the TPS65987DDJ presents a pull-down resistance RD\_CC on each C\_CCn pin and waits for a DFP to attach and pull-up the voltage on the pin. The DFP pulls-up the C\_CCn pin by applying either a resistance or a current. The UFP detects an attachment by the presence of VBUS. The UFP determines the advertised current from the DFP by the pull-up applied to the C\_CCn pin.

### 8.3.4.3 Configured as a DRP

When a TPS65987DDJ port is configured as a DRP, the TPS65987DDJ alternates the port's C\_CCn pins between the pull-down resistance, Rd, and pull-up current source, Rp.

### 8.3.4.4 Fast Role Swap Signaling

The TPS65987DDJ cable plug block contains additional circuitry that may be used to support the Fast Role Swap (FRS) behavior defined in the [USB Power Delivery Specification](#). The circuitry provided for this functionality is detailed in [图 8-15](#).



**图 8-15. Fast Role Swap Detection and Signaling**

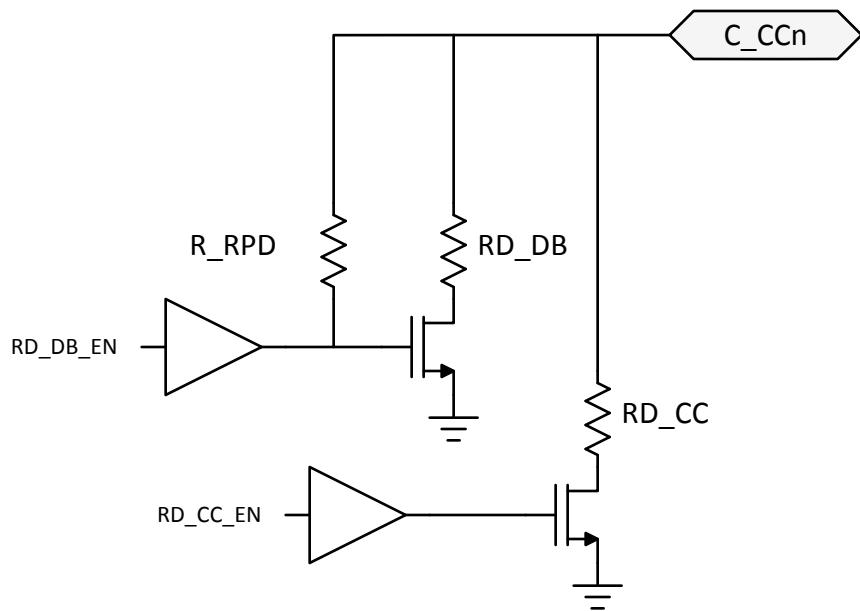
When a TPS65987DDJ port is operating as a sink with FRS enabled, the TPS65987DDJ monitors the CC pin voltage. If the CC voltage falls below  $V_{TH\_FRS}$  a fast role swap situation is detected and signaled to the digital core. When this signal is detected the TPS65987DDJ ceases operating as a sink and begin operating as a source.

When a TPS65987DDJ port is operating as a source with FRS enabled, the TPS65987DDJ digital core can signal to the connected port partner that a fast role swap is required by enabling the R\_FRSWAP pull down on the connected CC pin. When this signal is sent the TPS65987DDJ ceases operating as the source and begin operating as a sink.

### 8.3.5 Dead Battery Operation

#### 8.3.5.1 Dead Battery Advertisement

The TPS65987DDJ supports booting from no-battery or dead-battery conditions by receiving power from VBUS. Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source provides a voltage on VBUS. The TPS65987DDJ hardware is configured to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd once the device no longer requires power from VBUS. [图 8-16](#) shows the configuration of the C\_CCn pins, and elaborates on the basic cable plug and orientation detection block shown in [图 8-14](#). A resistance R\_RPD is connected to the gate of the pull-down FET on each C\_CCn pin. During normal operation when configured as a sink, RD is RD\_CC; however, while dead-battery or no-battery conditions exist, the resistance is un-trimmed and is RD\_DB. When RD\_DB is presented during dead-battery or no-battery, application code switches to RD\_CC.



**图 8-16. Dead Battery Pull-Down Resistor**

In this case, the gate driver for the pull-down FET is Hi-Z at its output. When an external connection pulls up on C\_CCn (the case when connected to a DFP advertising with a pull-up resistance Rp or pull-up current), the connection through R\_RPD pulls up on the FET gate turning on the pull-down through RD\_DB. In this condition, the C\_CCn pin acts as a clamp VTH\_DB in series with the resistance RD\_DB.

### 8.3.5.2 BUSPOWER (ADCIN1)

The BUSPOWER input to the internal ADC controls the behavior of the TPS65987DDJ in response to VBUS being supplied during a dead battery condition. The pin must be externally tied to the LDO\_3V3 output via a resistive divider. At power-up the ADC converts the BUSPOWER voltage and the digital core uses this value to determine start-up behavior. It is recommended to tie ADCin1 to LDO\_3V3 through a resistor divider as shown in [图 8-17](#). For more information about how to use the ADCin1 pin to configure the TPS65987DDJ, see the [Boot](#) section.

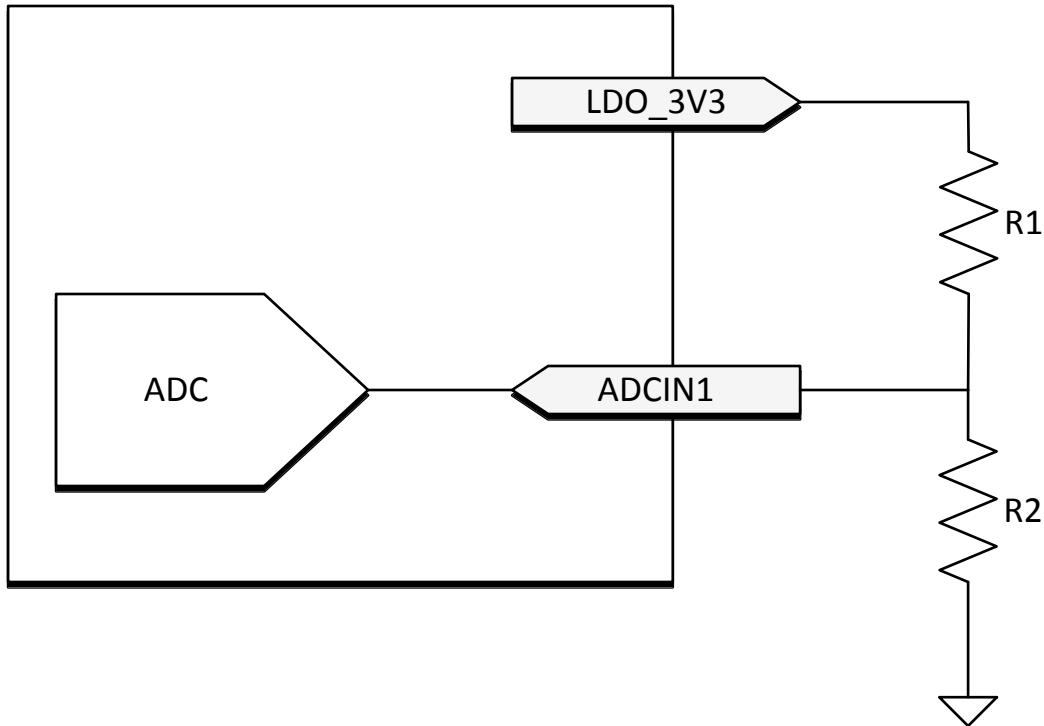


図 8-17. ADCIN1 Resistor Divider

注

Devices implementing the BP\_WaitFor3V3\_External configuration must use GPIO16 for external sink path control.

### 8.3.6 Battery Charger Detection and Advertisement

The battery charger (BC1.2) block integrates circuitry to detect when the connected entity on the USB D+/D- pins is a BC1.2 compliant charger, as well as advertise BC1.2 charging capabilities to connected devices. To enable the required detection and advertisement mechanisms, the block integrates various voltage sources, currents, and resistances. 図 8-18 shows the connection of these elements to the TPS65987DDJ C\_USB\_P and C\_USB\_N pins.

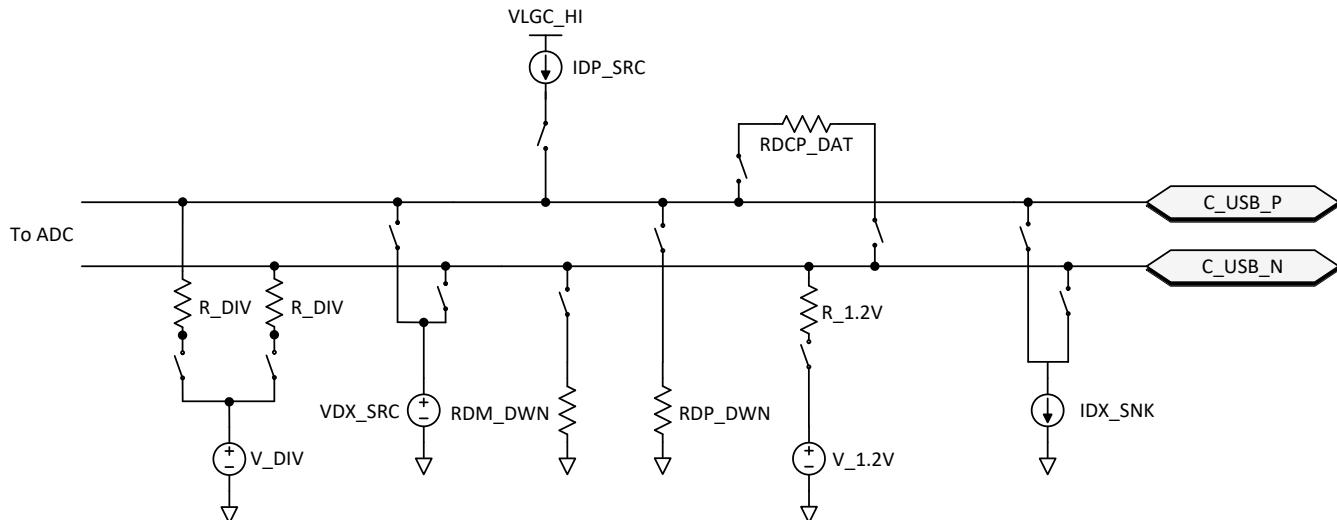


図 8-18. Battery Charger Detection and Advertisement

## 注

The pull-up and pull-down resistors required by the USB2 standard for a USB host or device are not provided by the TPS65987DDJ and must be provided externally to the device in final applications.

### 8.3.6.1 BC1.2 Data Contact Detect

The Data Contact Detect follows the definition in the USB BC1.2 specification. The detection scheme sources a current IDP\_SRC into the D+ pin of the USB connection. The current is sourced into the C\_USB\_P D+ pin. A resistance RDM\_DWN is connected between the D- pin and GND. The current source IDP\_SRC and the pull-down resistance RDM\_DWN, is activated during data contact detection.

### 8.3.6.2 BC1.2 Primary and Secondary Detection

The Primary and Secondary Detection follow the USB BC1.2 specification. This detection scheme looks for a resistance between D+ and D- lines by forcing a known voltage on the first line, forcing a current sink on the second line and then reading the voltage on the second line using the ADC integrated in the TPS65987DDJ. The voltage source VDX\_SRC and the current source IDX\_SNK, are activated during primary and secondary detection.

### 8.3.6.3 Charging Downstream Port Advertisement

The Charging Downstream Port (CDP) advertisement follows the USB BC1.2 specification. The advertisement scheme monitors the D+ line using the ADC. When a voltage of 0.6 V is seen on the D+ line, TPS65987DDJ forces a voltage of 0.6 V on the D- line until the D+ goes low. The voltage source VDX\_SRC and the current source IDX\_SNK, are activated during CDP advertisement. CDP advertisement takes place with the USB Host 15-k $\Omega$  pull-down resistors on the D+ and D- lines from the USB Host Transceiver, because after CDP negotiation takes place on the D+/D- lines, USB2.0 data transmission begins.

### 8.3.6.4 Dedicated Charging Port Advertisement

The Dedicated Charging Port (DCP) advertisement follows the USB BC1.2 specification (Shorted Mode per BC1.2) and the YD/T 1591-2009 specification. The advertisement scheme shorts the D+ and D- lines through the RDCCP\_DAT resistor.

### 8.3.6.5 2.7-V Divider3 Mode Advertisement

The 2.7-V Divider3 Mode is a proprietary advertisement scheme used to charge popular devices in the market. This advertisement places V\_DIV on D+ with an R\_DIV output impedance and V\_DIV on D- with an R\_DIV output impedance. With this advertisement scheme present on D+ and D-, specific popular devices are allowed to pull more than 1.5 A of current from VBUS. If enabling 2.7-V Divider3 Mode advertisement on a port, it is recommended that VBUS be able to supply at least 2.4 A of current.

### 8.3.6.6 1.2-V Mode Advertisement

The 1.2-V Mode is a proprietary advertisement scheme used to charge popular devices in the market. This advertisement places V\_1.2 V on D- with an R\_1.2 V output impedance and shorts D+ and D- together through the RDCCP\_DAT resistor. With this advertisement scheme present on D+ and D-, specific popular devices are allowed to pull more than 1.5 A of current from VBUS. If enabling 1.2-V Mode advertisement on a port, it is recommended that VBUS be able to supply at least 2 A of current.

### 8.3.6.7 DCP Auto Mode Advertisement

The DCP Auto Mode Advertisement scheme is a special scheme that automatically advertises the correct charging scheme depending on the device attached to the USB port. If a device that detects Dedicated Charging Port Advertisement is connected, the DCP Advertising scheme will automatically be placed on D+/D-. If a device that detects 2.7-V Divider3 Mode Advertisement is connected, the 2.7-V Divider3 Mode Advertising scheme will automatically be placed on D+/D-. Likewise, if a device that detects 1.2-V Mode Advertisement is connected, the 1.2-V Mode Advertising scheme will automatically be placed on D+/D-. The TPS65987DDJ DCP Auto Mode Advertisement circuit is able to place the correct advertisement scheme on D+/D- without needing to discharge VBUS.

### 8.3.7 ADC

The TPS65987DDJ integrated ADC is accessible to internal firmware only. The ADC reads are not available for external use.

### 8.3.8 DisplayPort HPD

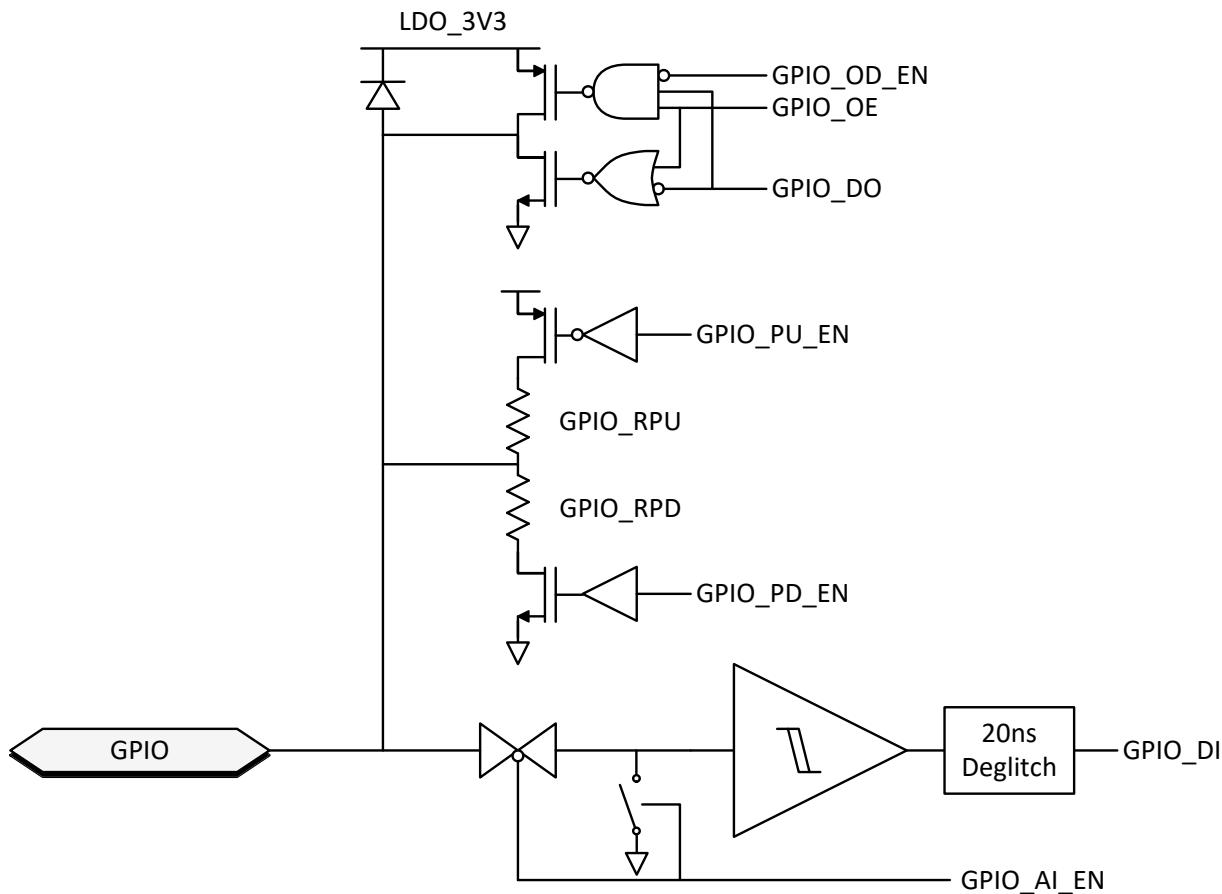
To enable HPD signaling through PD messaging, a single pin is used as the HPD input and output for each port. When events occur on these pins during a DisplayPort connection through the Type-C connector (configured by firmware), hardware timers trigger and interrupt the digital core to indicate needed PD messaging. When one of the TPS65987DDJ's ports is operating as a DP source, its corresponding HPD pin operates as an output (HPD TX), and when a port is operating as a DP sink, its corresponding HPD pin operates as an input (HPD RX). When DisplayPort is not enabled via firmware the HPD pin operates as a generic GPIO (GPIO3).

### 8.3.9 Digital Interfaces

The TPS65987DDJ contains several different digital interfaces which may be used for communicating with other devices. The available interfaces include three I<sup>2</sup>C ports (I<sup>2</sup>C1 is a Master/Slave, I<sup>2</sup>C2 is a Slave, and I<sup>2</sup>C3 is a Master), one SPI controller, and 12 additional GPIOs.

#### 8.3.9.1 General GPIO

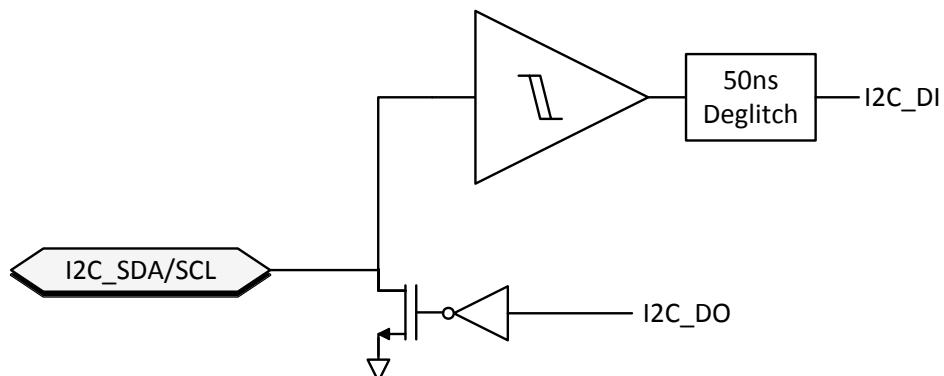
图 8-19 shows the GPIO I/O buffer for all GPIOOn pins. GPIOOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input. The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO\_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO\_3V3 and LDO\_1V8 to the input buffer. When interfacing with non 3.3-V I/O devices the output buffer may be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.



## 8-19. General GPIO Buffer

### 8.3.9.2 I2C

The TPS65987DDJ features three I<sup>2</sup>C interfaces. The I<sup>2</sup>C1 interface is configurable to operate as a master or slave. The I<sup>2</sup>C2 interface may only operate as a slave. The I<sup>2</sup>C3 interface may only operate as a master. The I<sup>2</sup>C I/O driver is shown in [FIG 8-20](#). This I/O consists of an open-drain output and an input comparator with de-glitching. The I<sup>2</sup>C input thresholds are set by LDO 1V8 and by default.



## 8-20. I<sup>2</sup>C Buffer

### 8.3.9.3 SPI

The TPS65987DDJ has a single SPI controller interface for use with external memory devices. [Figure 8-21](#) shows the I/O buffers for the SPI interface.

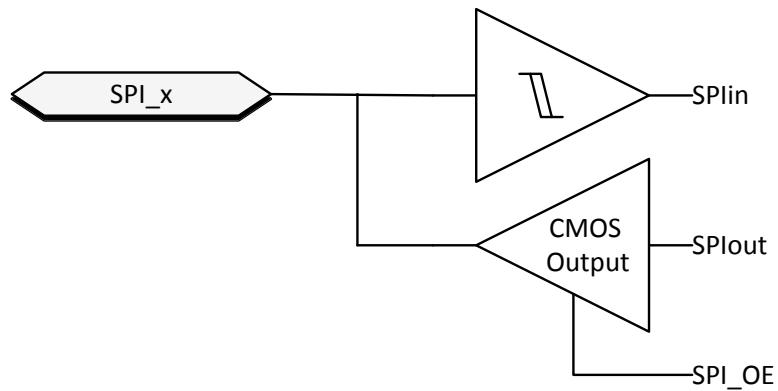


図 8-21. SPI Buffer

### 8.3.10 Digital Core

The figure below shows a simplified block diagram of the digital core.

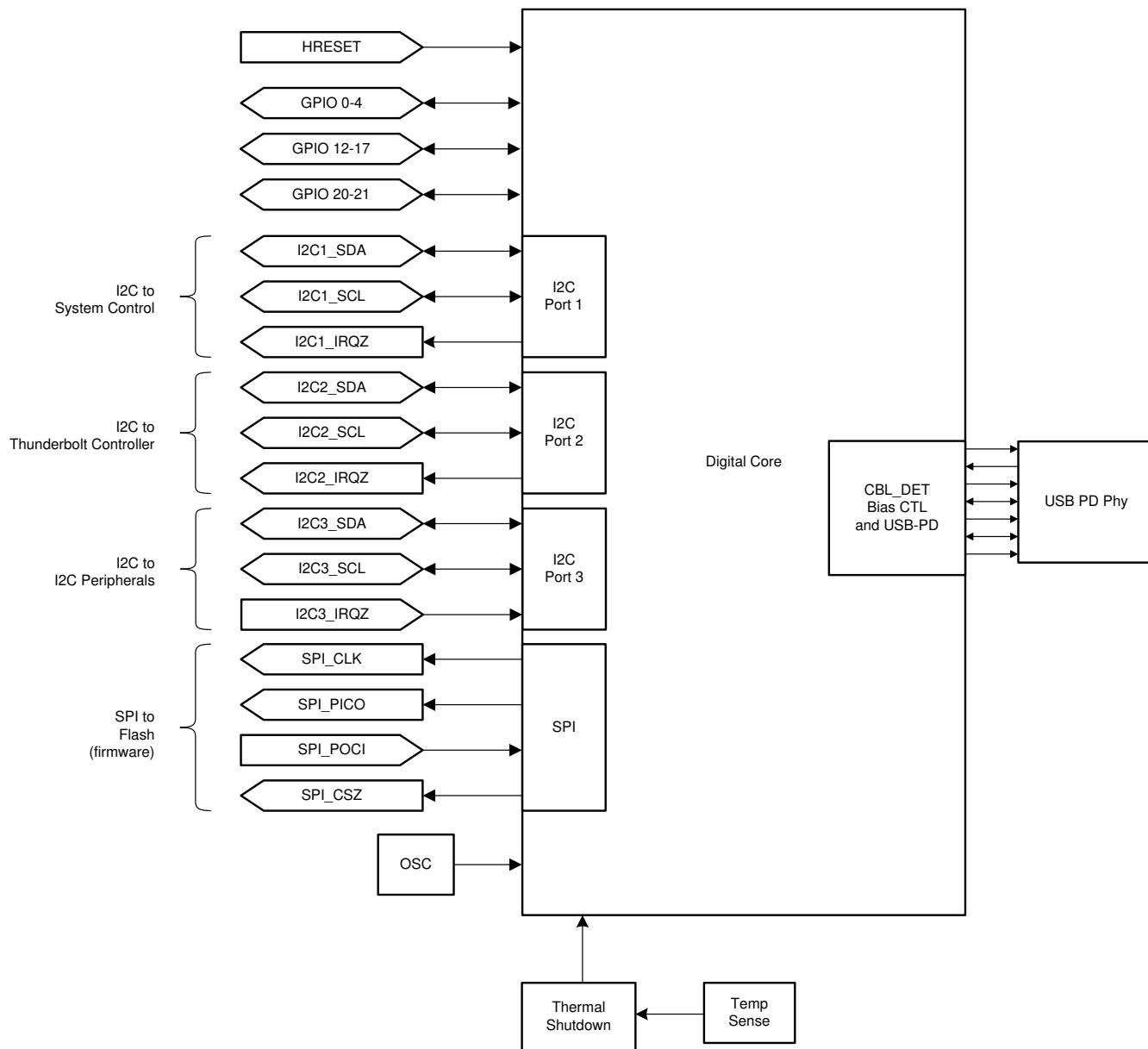


図 8-22. Digital Core Block Diagram

### 8.3.11 I<sup>2</sup>C Interfaces

The TPS65987DDJ has three I<sup>2</sup>C interface ports. I<sup>2</sup>C Port 1 is comprised of the I2C1\_SDA, I2C1\_SCL, and I2C1\_IRQ1 pins. I<sup>2</sup>C Port 2 is comprised of the I2C2\_SDA, I2C2\_SCL, and I2C2\_IRQ1 pins. These interfaces provide general status information about the TPS65987DDJ, as well as the ability to control the TPS65987DDJ behavior, as well as providing information about connections detected at the USB-C receptacle and supporting communications to/from a connected device and/or cable supporting BMC USB-PD. I<sup>2</sup>C Port 3 is comprised of the I2C3\_SDA, I2C3\_SCL, and I2C3\_IRQ1 pins. This interface is used as a general I<sup>2</sup>C master to control external I<sup>2</sup>C devices such as a super-speed mux or re-timer.

The first port can be a master or a slave, but the default behavior is to be a slave. The second port operates as a slave only. Port 1 and Port 2 are interchangeable as slaves. Both Port1 and Port2 operate in the same way and has the same access in and out of the core. An interrupt mask is set for each that determines what events are interrupted on that given port. Port 3 operates as a master only.

### 8.3.11.1 I<sup>2</sup>C Interface Description

The TPS65987DDJ support Standard and Fast mode I<sup>2</sup>C interface. The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high initiates I<sup>2</sup>C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input and output during the high of the ACK-related clock pulse. On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

图 8-23 shows the start and stop conditions of the transfer. 图 8-24 shows the SDA and SCL signals for transferring a bit. 图 8-25 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

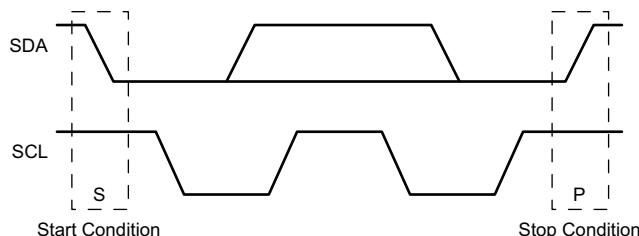


图 8-23. I<sup>2</sup>C Definition of Start and Stop Conditions

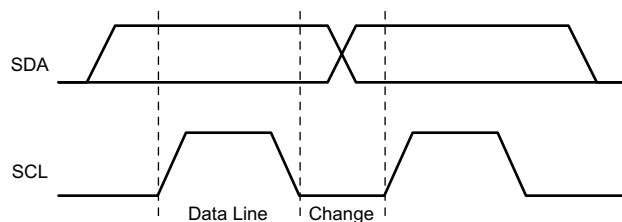


图 8-24. I<sup>2</sup>C Bit Transfer

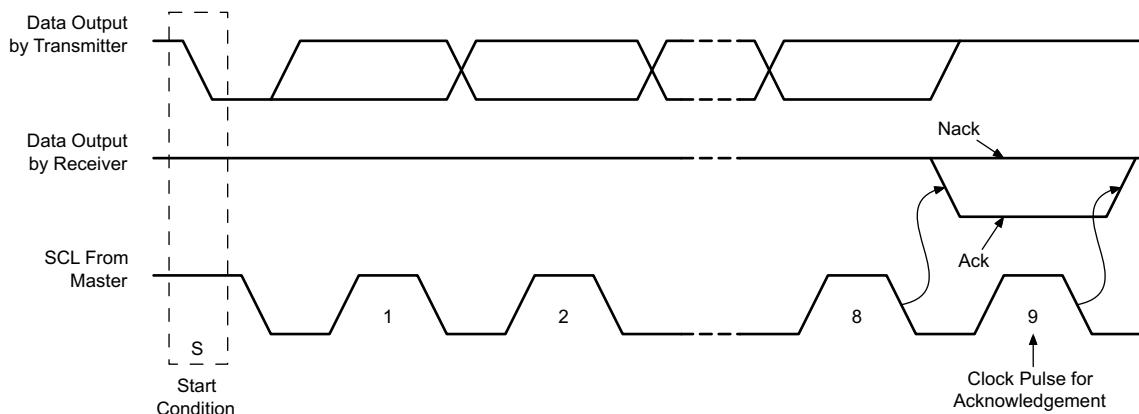


图 8-25. I<sup>2</sup>C Acknowledgment

### 8.3.11.2 I<sup>2</sup>C Clock Stretching

The TPS65987DDJ features clock stretching for the I<sup>2</sup>C protocol. The TPS65987DDJ slave I<sup>2</sup>C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4  $\mu$ s for standard 100 kbps I<sup>2</sup>C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

### 8.3.11.3 I<sup>2</sup>C Address Setting

The boot flow sets the hardware configurable unique I<sup>2</sup>C address of the TPS65987DDJ before the port is enabled to respond to I<sup>2</sup>C transactions. For the I<sup>2</sup>C1 interface, the unique I<sup>2</sup>C address is determined by the analog level set by the analog ADCIN2 pin (three bits) as shown in 表 8-2 .

表 8-2. I<sup>2</sup>C Default Unique Address I2C1

Default I <sup>2</sup> C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I <sup>2</sup> C address.							

For the I<sup>2</sup>C2 interface, the unique I<sup>2</sup>C address is a fixed value as shown in 表 8-3 .

表 8-3. I<sup>2</sup>C Default Unique Address I2C2

Default I <sup>2</sup> C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I <sup>2</sup> C address.							

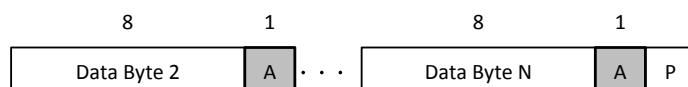
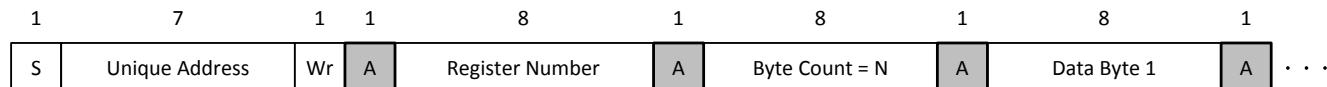
### 注

The TPS65987DDJ I<sup>2</sup>C address values are set and controlled by device firmware. Certain firmware configurations may override the presented address settings.

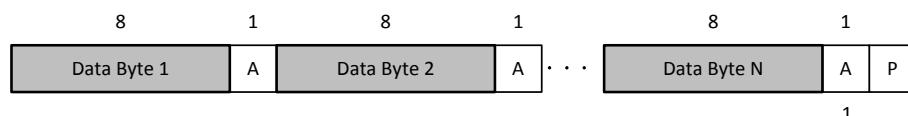
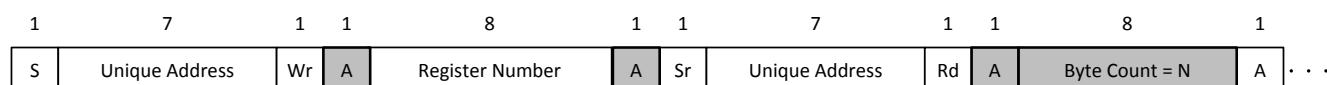
### 8.3.11.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I<sup>2</sup>C master and a single TPS65987DDJ. The I<sup>2</sup>C Slave sub-address is used to receive or respond to Host Interface protocol commands.

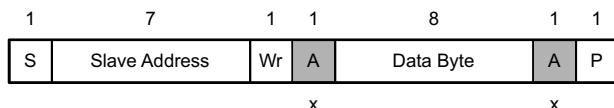
图 8-26 和 图 8-27 展示了 I<sup>2</sup>C 从机接口的写和读协议，其中包含一个键以解释图 8-28 中的术语。该键在 SMBus 规格中包含，并在此部分重复。



**图 8-26. I<sup>2</sup>C Unique Address Write Register Protocol**



**图 8-27. I<sup>2</sup>C Unique Address Read Register Protocol**



S	Start Condition
SR	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
x	Field is required to have the value x
A	Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)
P	Stop Condition
	Master-to-Slave
	Slave-to-Master
-----	Continuation of protocol

**图 8-28. I<sup>2</sup>C Read/Write Protocol Key**

### 8.3.11.5 I<sup>2</sup>C Pin Address Setting (ADCIN2)

为了通过单个 TPS65987DDJ 引脚设置多个 I<sup>2</sup>C 地址，外部在 ADCIN2 引脚上放置一个电阻分压器。内部 ADC 从该分压器值进行解码。图 8-29 展示了解码。

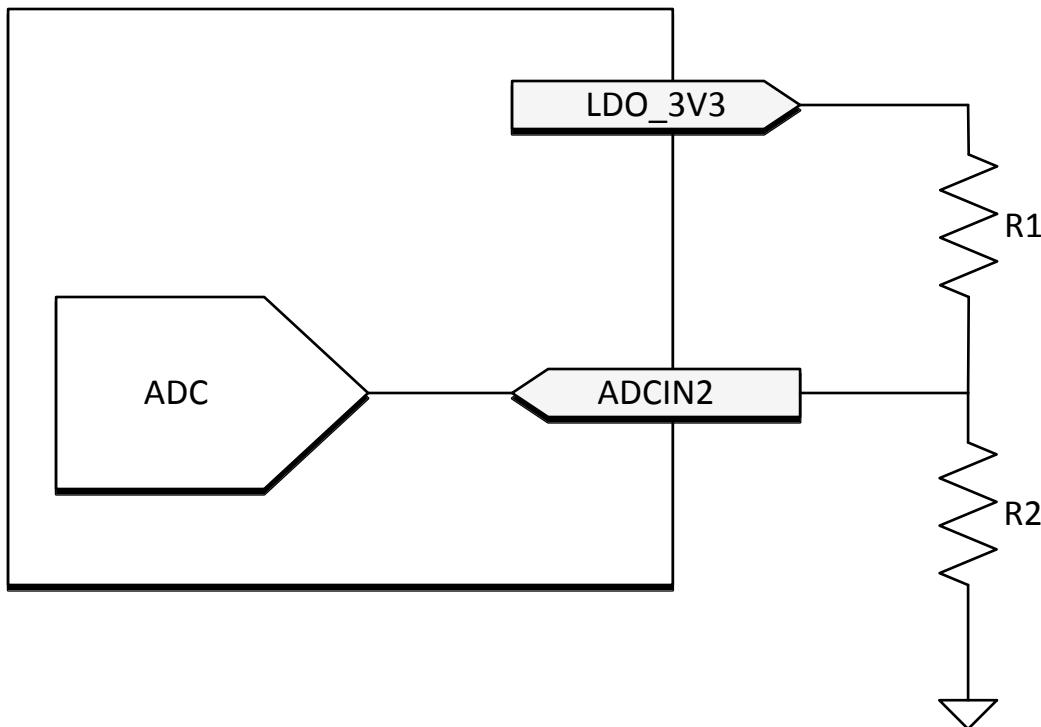


图 8-29. I<sup>2</sup>C Address Divider

表 8-4 lists the external divider needed to set bits [3:1] of the I<sup>2</sup>C Unique Address.

表 8-4. I<sup>2</sup>C Address Selection

DIV = R2/(R1+R2) <sup>(1)</sup>		I <sup>2</sup> C UNIQUE ADDRESS [3:1]
DIV_min	DIV_max	I2C_ADDR_DECODE
Short ADCIN2 to GND		000b
0.20	0.38	001b
0.40	0.58	010b
Short ADCIN2 to LDO_3V3		011b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

### 8.3.12 SPI Controller Interface

The TPS65987DDJ loads any ROM patch and-or configuration from flash memory during the boot sequence. The TPS65987DDJ is designed to power the flash from LDO\_3V3 in order to support dead-battery or no-battery conditions, and therefore pull-up resistors used for the flash memory must be tied to LDO\_3V3. The flash memory IC must support 12 MHz SPI clock frequency. The size of the flash must be at least 64 kB. The SPI controller of the TPS65987DDJ supports SPI Mode 0. For Mode 0, data delay is defined so that data is output on the same cycle as chip select (SPI\_CS pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI\_POCI and SPI\_PICO pins) is shifted out on the falling edge of the clock (SPI\_CLK pin) and data is sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI\_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 KB. The W25X05CL or similar is recommended.

### 8.3.13 Thermal Shutdown

The TPS65987DDJ features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all

functions except for supervisory circuitry when die temperature goes above a rising temperature of TSD\_MAIN. The temperature shutdown has a hysteresis of TSDH\_MAIN and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal power path and disables the power path in response to an overtemperature event. Once the temperature falls below TSDH\_PWR the path can be configured to resume operation or remain disabled until re-enabled by firmware.

### 8.3.14 Oscillators

The TPS65987DDJ has two independent oscillators for generating internal clock domains. A 24-MHz oscillator generates clocks for the core during normal operation. A 100-kHz oscillator generates clocks for various timers and clocking the core during low power states.

## 8.4 Device Functional Modes

### 8.4.1 Boot

At initial power on the device goes through a boot routine. This routine is responsible for initializing device register values and loading device patch and configuration bundles. The device's functional behavior after boot can be configured through the use of pin straps on the SPI\_POCI and ADCIN1 pins as shown in [表 8-5](#).

**表 8-5. Boot Mode Pin Strapping**

SPI_POCI	ADCIN1 DIV = R2/(R1+R2) <sup>(1)</sup>		Dead Battery Mode	Device Configuration
	DIV MIN	DIV MAX		
1	0.00	0.18	BP_NoResponse	Safe Configuration
1	0.20	0.28	BP_WaitFor3V3_Internal	Safe Configuration
1	0.30	0.38	BP_ECWait_Internal	Infinite Wait
1	0.40	0.48	BP_WaitFor3V3_External	Safe Configuration
1	0.50	0.58	BP_ECWait_External	Infinite Wait
1	0.60	1.00	BP_NoWait	Safe Configuration
0	0.10	0.18	BP_NoResponse	Configuration 1
0	0.20	0.28	BP_NoResponse	Configuration 2
0	0.30	0.38	BP_ECWait_Internal	Infinite Wait
0	0.40	0.48	BP_NoWait	Configuration 3
0	0.50	0.58	BP_ECWait_External	Infinite Wait
0	0.60	0.68	BP_NoResponse	Configuration 4
0	0.70	0.78	BP_NoWait	Reserved
0	0.80	0.88	BP_NoResponse	Reserved
0	0.90	1.00	BP_NoWait	Configuration 5

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

The pin strapping configures two different parameters, Dead battery mode and device configuration. The dead battery mode selects device behavior when powered from VBUS. The dead battery mode behaviors are detailed in [表 8-6](#).

**表 8-6. Dead Battery Configurations**

CONFIGURATION	DESCRIPTION
BP_NoResponse	No power switch is enabled and the device does not start-up until VIN_3V3 is present
BP_WaitFor3V3_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.

**表 8-6. Dead Battery Configurations (continued)**

CONFIGURATION	DESCRIPTION
BP_WaitFor3V3_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.
BP_ECWait_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_ECWait_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_NoWait	The device continues to start-up and attempts to load configurations while receiving power from VBUS. Once configuration is loaded the appropriate power switch is closed based on the loaded configuration.

### 注

Devices implementing the BP\_WaitFor3V3\_External or BP\_ECWait\_External configuration must use GPIO16 for external sink path control, while devices implementing the BP\_WaitFor3V3\_Internal or BP\_ECWait\_Internal must use PPHV1 as the sink path.

When powering up from VIN\_3V3 or VBUS the device will attempt to load configuration information from the SPI or I2C digital interfaces. The device configuration settings select the device behavior should configuration information not be available during the device boot process. 表 8-7 shows the device behavior for each device configuration setting.

**表 8-7. Device Default Configurations**

Configuration	Description
Safe	Ports disabled, if powered from VBUS operates a legacy sink
Infinite Wait	Device infinitely waits in boot state for configuration information
Configuration 1	DFP only (Internal Switch) 5 V at 3-A Source capability USB Type-C Only (No PD)
Configuration 2	DFP only (Internal Switch) 45-W Source (5/9/15/20-V Output) TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 3	UFP only (Internal Switch) 5-20 V at 0.9 - 3.0-A Sink capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 4	DFP only (Internal Switch) 60-W Source (5/9/15/20-V Output) TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 5	UFP only (External Switch)) 5-20 V at 0.9-3.0-A Sink capability 5 V at 3.0-A Source capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled

### 8.4.2 Power States

The TPS65987DDJ may operate in one of three different power states: Active, Idle, or Sleep. The functionality available in each state is summarized in 表 8-8.

**表 8-8. Power States**

	ACTIVE	IDLE	SLEEP
Type-C State			

**表 8-8. Power States (continued)**

	ACTIVE	IDLE	SLEEP
Type-C State	Connected or Unconnected	Connected or Unconnected	Unconnected
Type-C Port 2 State	Connected or Unconnected	Connected or Unconnected	Unconnected
LDO_3V3 <sup>(1)</sup>	Valid	Valid	Valid
LDO_1V8	Valid	Valid	Valid
Oscillator Status			
Digital Core Clock Frequency	12 MHz	4 MHz - 6 MHz	100 kHz
100-kHz Oscillator Status	Enabled	Enabled	Enabled
24-MHz Oscillator Status	Enabled	Enabled	Disabled
Available Features			
Type-C Detection	Yes	Yes	Yes
PD Communication	Yes	No	No
I2C Communication	Yes	Yes	No
SPI Communication	Yes	No	No
Wake Events			
Wake on Attach/Detach	N/A	Yes	Yes
Wake on PD Communication	N/A	Yes <sup>(2)</sup>	No
Wake on I2C Communication	N/A	Yes	Yes

(1) LDO\_3V3 may be generated from either VIN\_3V3 or VBUS. If LDO\_3V3 is generated from VBUS, TPS65987DDJ port only operate as sinks.

(2) Wake up from Idle to Active upon a PD message is supported however the first PD message received is lost.

## 9 Application and Implementation

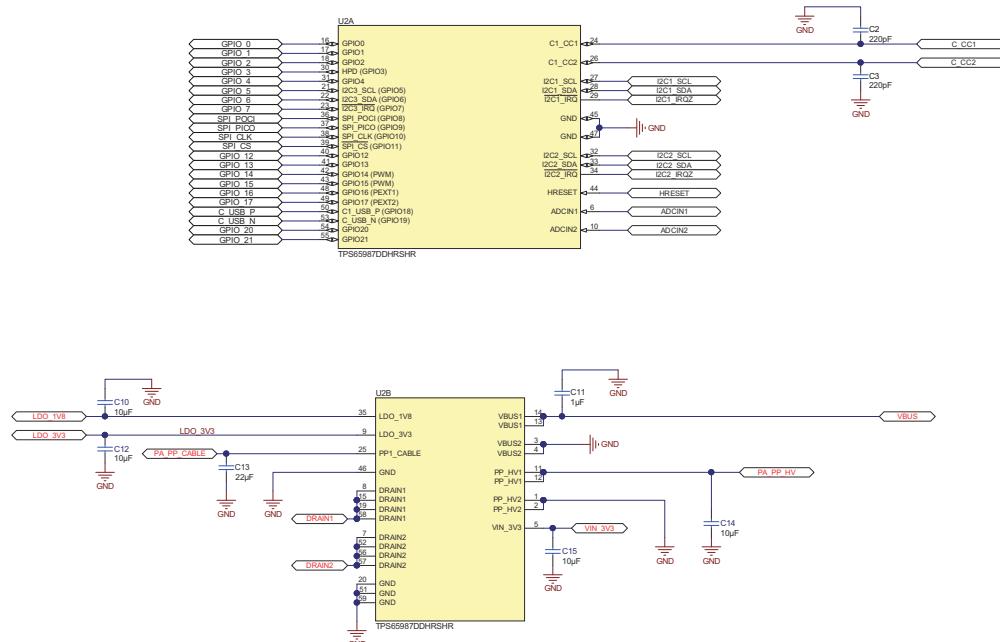
注

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## 9.1 Application Information

The TPS65987DDJ firmware implements a host interface over I<sup>2</sup>C to allow for the configuration and control of all device options. Initial device configuration is configured through a configuration bundle loaded onto the device during boot. The bundle may be loaded via I<sup>2</sup>C or SPI. The TPS65987DDJ configuration bundle and host interface allow the device to be customized for each specific application. The configuration bundle can be generated through the Application Customization Tool.

## 9.2 Typical Applications



## ☒ 9-1. Example Schematic

### 9.2.1 Type-C VBUS Design Considerations

USB Type-C and PD allows for voltages up to 20 V with currents up to 5 A. This introduces power levels that could damage components touching or hanging off of VBUS. Under normal conditions, all high power PD contracts should start at 5 V and then transition to a higher voltage. However, there are some devices that are not compliant to the USB Type-C and Power Delivery standards and could have 20 V on VBUS. This could cause a 20-V hot plug that can ring above 30 V. Adequate design considerations are recommended below for these non-compliant devices.

### **9.2.1.1 Design Requirements**

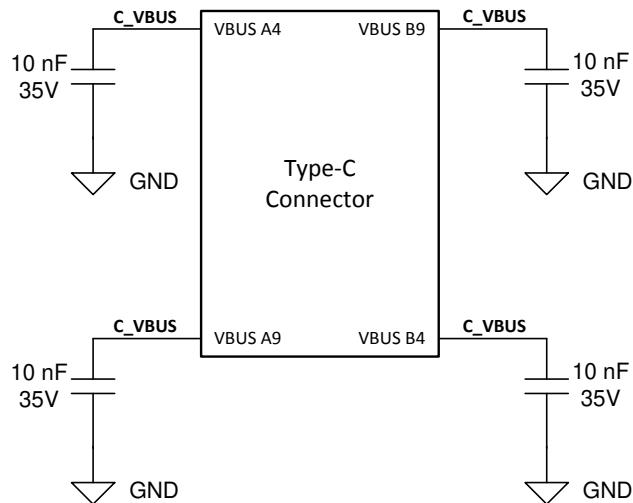
表 9-1 shows VBUS conditions that can be introduced to a USB Type-C and PD Sink. The system should be able to handle these conditions to ensure that the system is protected from non-compliant and/or damaged USB PD sources. A USB Sink should be able to protect from the following conditions being applied to its VBUS. The *Detailed Design Procedure* section explains how to protect from these conditions.

**表 9-1. VBUS Conditions**

CONDITION	VOLTAGE APPLIED
Abnormal VBUS Hot Plug	4 V - 21.5 V
VBUS Transient Spikes	4 V - 43 V

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Type-C Connector VBUS Capacitors

**图 9-2. Type-C Connector VBUS Capacitors**

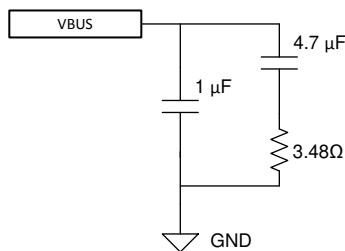
The first level of protection starts at the Type-C connector and the VBUS pin capacitors. These capacitors help filter out high frequency noise but can also help absorb short voltage transients. Each VBUS pin should have a 10-nF capacitor rated at or above 25 V and placed as close to the pin as possible. The GND pin on the capacitors should have very short path to GND on the connector. The derating factor of ceramic capacitors should be taken into account as they can lose more than 50% of their effective capacitance when biased. Adding the VBUS capacitors can help reduce voltage spikes by 2 V to 3 V.

#### 9.2.1.2.2 VBUS Schottky and TVS Diodes

Schottky diodes are used on VBUS to help absorb large GND currents when a Type-C cable is removed while drawing high current. The inductance in the cable will continue to draw current on VBUS until the energy stored is dissipated. Higher currents could cause the body diodes on IC devices connected to VBUS to conduct. When the current is high enough it could damage the body diodes of IC devices. Ideally a VBUS Schottky diode should have a lower forward voltage so it can turn on before any other body diodes on other IC devices. Schottky diodes on VBUS also help during hard shorts to GND which can occur with a faulty Type-C cable or damaged Type-C PD device. VBUS could ring below GND which could damage devices hanging off of VBUS. The Schottky diode will start to conduct once VBUS goes below the forward voltage. When the TPS65987DDJ is the only device connected to VBUS place the Schottky Diode close to the VBUS pin of the TPS65987DDJ. The two figures below show a short condition with and without a Schottky diode on VBUS. In [图 9-4](#) without the Schottky diode, VBUS rings 2 V below GND and oscillates after settling to 0 V. In [图 9-5](#) with the Schottky diode, VBUS drops 750 mV below GND (Schottky diode  $V_f$ ) and the oscillations are minimized.

TVS Diodes help suppress and clamp transient voltages. Most TVS diodes can fully clamp around 10 ns and can keep the VBUS at their clamping voltage for a period of time. Looking at the clamping voltage of TVS diodes after they settle during a transient will help decide which TVS diode to use. The peak power rating of a TVS diode must be able to handle the worst case conditions in the system. A TVS diode can also act as a "pseudo schottky diode" as they will also start to conduct when VBUS goes below GND.

### 9.2.1.2.3 VBUS Snubber Circuit

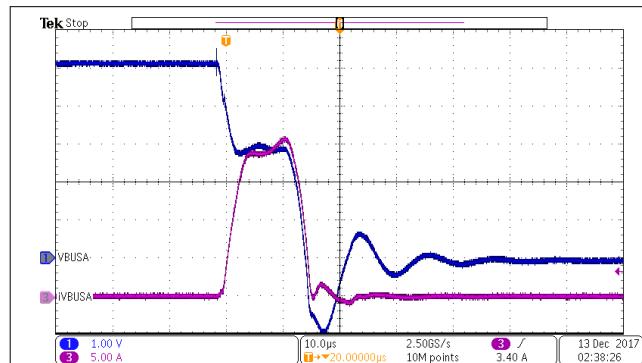


**图 9-3. VBUS Snubber**

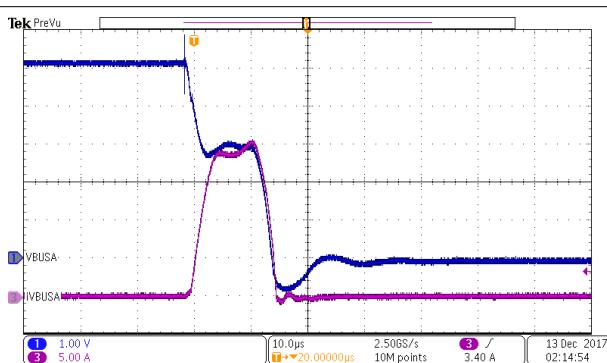
Another method of clamping the USB Type-C VBUS is to use a VBUS RC Snubber. An RC Snubber is a great solution because in general it is much smaller than a TVS diode, and typically more cost effective as well. An RC Snubber works by modifying the characteristic of the total RLC response in the USB Type-C cable hot-plug from being under-damped to critically-damped or over-damped. So rather than clamping the overvoltage directly, it actually changes the hot-plug response from under-damped to critically-damped, so the voltage on VBUS does not ring at all; so the voltage is limited, but without requiring a clamping element like a TVS diode.

However, the USB Type-C and Power Delivery specifications limit the range of capacitance that can be used on VBUS for the RC snubber. VBUS capacitance must have a minimum 1  $\mu$ F and a maximum of 10  $\mu$ F. The RC snubber values chosen support up to 4 m USB Type-C cable (maximum length allowed in the USB Type-C specification) being hot plugged, is to use 4.7- $\mu$ F capacitor in series with a 3.48- $\Omega$  resistor. In parallel with the RC Snubber a 1 $\mu$ F capacitor is used, which always ensures the minimum USB Type-C VBUS capacitance specification is met. This circuit can be seen in the figure above.

### 9.2.1.3 Application Curves



**图 9-4. VBUS Short without Schottky Diode**



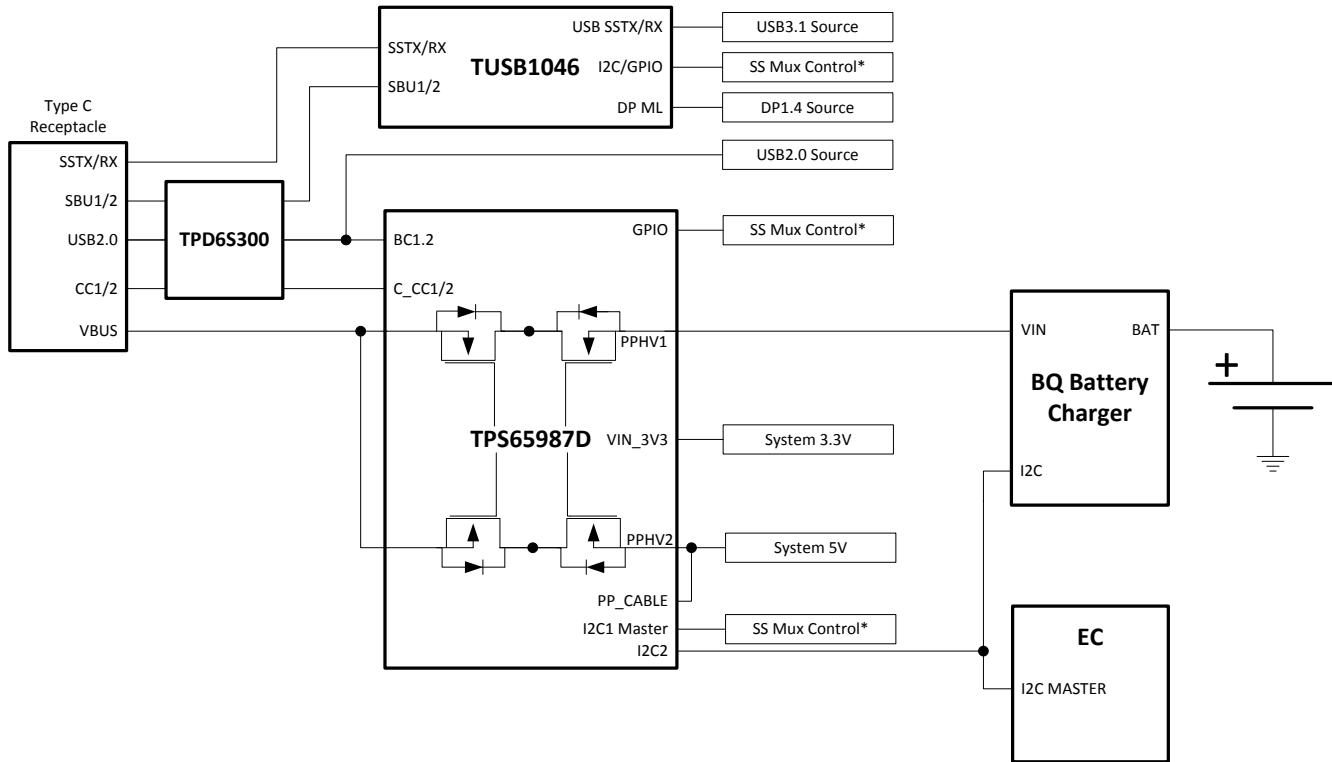
**图 9-5. VBUS Short with Schottky Diode**

### 9.2.2 Notebook Design Supporting PD Charging

The TPS65987DDJ works very well in single port Notebooks that support PD charging. The two internal power paths for the TPS65987DDJ source System 5 V on VBUS through the PPHV2 path and sink VBUS up to 20 V on PPHV1. The TPS65987DDJ integrated reverse current protection allows the designer to connect PPHV1 to another power source such as a standard barrel jack or proprietary dock connector power to charge the notebook battery. The System 5-V supplies power to PP\_CABLE on the TPS65987DDJ to supply VCONN to Type-C e-marked cables and Type-C accessories. An embedded controller EC is used for additional control of the TPS65987DDJ and to relay information back to the operating system. An embedded controller enables features such as entering and exiting sleep modes, changing source and sink capabilities depending on the state of the battery, UCSI support, control alternate modes, etc.

### 9.2.2.1 USB and DisplayPort Notebook Supporting PD Charging

For systems that support USB and DisplayPort Data, the USB and DisplayPort sources are muxed to the Type-C connector through the TUSB1046 Super Speed mux. The TPS65987DDJ is capable of controlling the Super Speed Mux over I<sup>2</sup>C and will configure it according to the connection at the Type-C connector. The TPS65987DDJ can also set the configurations for the Super Speed mux equalizer settings for the USB Super Speed and DisplayPort Lanes through an initializing set of I<sup>2</sup>C writes. Note that I<sup>2</sup>C1 is the I<sup>2</sup>C master controlling the SS Mux and I<sup>2</sup>C2 is connected to the embedded controller. I<sup>2</sup>C1 can operate as an I<sup>2</sup>C master/slave and I<sup>2</sup>C2 can only operate as an I<sup>2</sup>C slave. Alternatively the Super Speed mux can be controlled through GPIO instead of I<sup>2</sup>C. The TPD6S300 provides Type-C protection features such as short to VBUS on the CC and SBU pins and ESD protection for the USB2 DN/P. See the figure below for the system block diagram.



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**図 9-6. USB and DisplayPort Notebook Supporting PD Charging**

#### 9.2.2.1.1 Design Requirements

The table below summarizes the Power Design parameters for an USB Type-C PD Notebook.

**表 9-2. Power Design Parameters**

POWER DESIGN PARAMETERS	VALUE	CURRENT PATH
PPHV2 Input Voltage, Current	5 V, 1.5 A	VBUS Source
PP_CABLE1/2 Input Voltage, Current	5 V, 500 mA	VCONN Source
PPHV1 Voltage, Current	5 V – 20 V, 3 A (5 A Max)	VBUS Sink
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65987DDJ Circuitry

#### 9.2.2.1.2 Detailed Design Procedure

##### 9.2.2.1.2.1 USB Power Delivery Source Capabilities

Most Type-C dongles (video and data) draw less than 900 mA and supplying 1.5 A on each Type-C port is sufficient for a notebook supporting USB and DisplayPort. 表 9-3 shows the PDO for the Type-C port.

**表 9-3. Source PDOs**

SOURCE PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	1.5 A

#### 9.2.2.1.2.2 USB Power Delivery Sink Capabilities

Most notebooks support buck and boost charging which allows them to charge the battery from 5 V to 20 V. USB PD sources must also follow the Source Power Rules defined by the USB Power Delivery specification. It is recommended for notebooks to support all the voltages in the Source Power Rules to ensure compatibility with most PD chargers and adapters.

**表 9-4. Sink PDOs**

SINK PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A (5 A Max)

#### 9.2.2.1.2.3 f

The table below summarizes the data capabilities of the notebook supporting USB3 and DisplayPort.

**表 9-5. Data Capabilities**

PROTOCOL	DATA	DATA ROLE
USB Data	USB3.1 Gen2	Host
DisplayPort	DP1.4	Host DFP_D (Pin Assignment C, D, and E)

#### 9.2.2.1.2.4 TUSB1046 Super Speed Mux GPIO Control

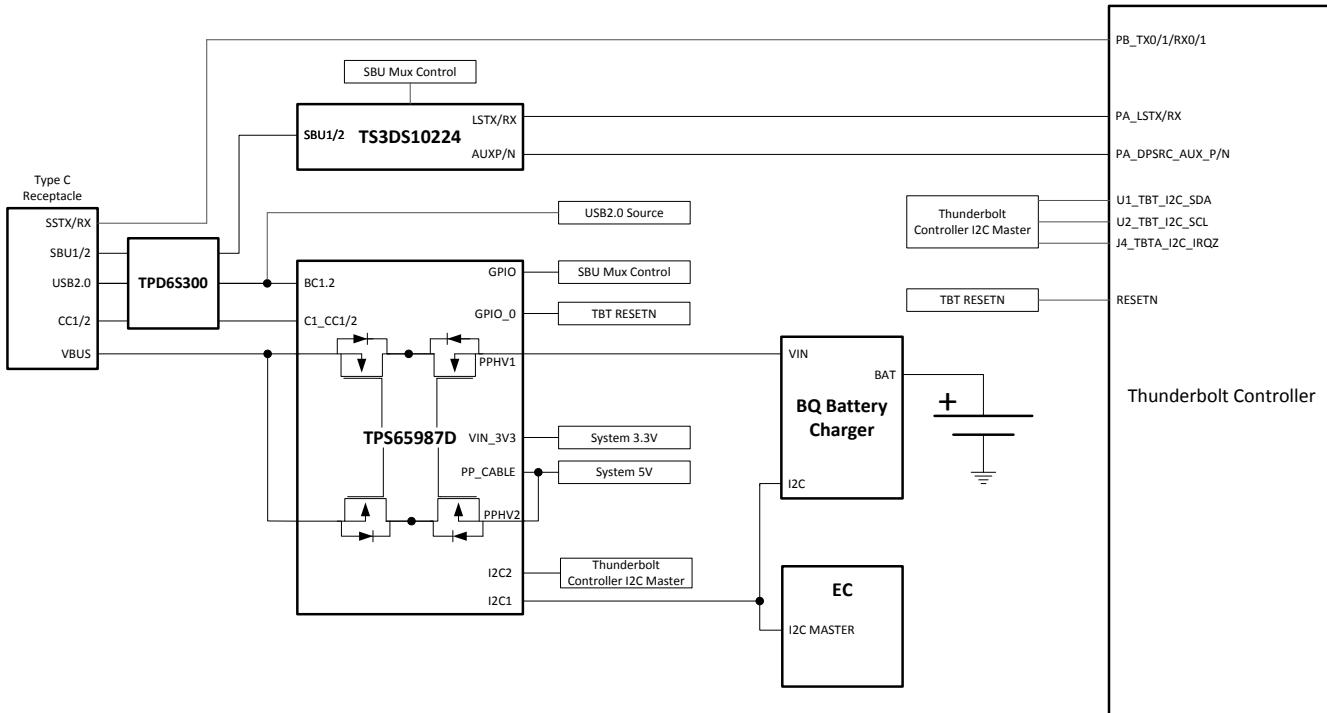
The TUSB1046 requires GPIO control in GPIO control mode to determine whether if there is USB or DisplayPort data connection. 表 9-6 summarizes the TPS65987DDJ GPIO Events and the control pins for the TUSB1046. Note that the pin strapping on the TUSB1046 will set the GPIO control mode and the required equalizer settings. For more details refer to the [TUSB1046 data sheet](#).

**表 9-6. GPIO Events for Super Speed Mux**

TPS65987DDJ GPIO EVENT	TUSB1046 CONTROL
Port 0 Cable Orientation Event	FLIP
Port 0 USB3 Event	CTL0
Port 0 DP Mode Selection Event	CTL1

#### 9.2.2.2 Thunderbolt Notebook Supporting PD Charging

A Thunderbolt system is capable of source USB, DisplayPort, and Thunderbolt data. There is an I<sup>2</sup>C connection between the TPS65987DDJ and the Thunderbolt controller. The TPS65987DDJ will determine the connection on the Type-C and will generate an interrupt to the Thunderbolt controller to generate the appropriate data output. An external mux for SBU may be needed to mux the LSTX/RX and AUX\_P/N signal from the Thunderbolt controller to the Type-C Connector. The TPD6S300 provides additional protection such as short to VBUS on the CC and SBU pins and ESD for the USB2 DN/P. See 图 9-7 for a block diagram of the system.



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**图 9-7. Thunderbolt Notebook Supporting PD Charging**

### 9.2.2.2.1 Design Requirements

表 9-7 summarizes the Power Design parameters for an USB Type-C PD Thunderbolt Notebook.

**表 9-7. Power Design Parameters**

POWER DESIGN PARAMETERS	VALUE	CURRENT PATH
PPH2 Input Voltage, Current	5 V, 3 A	VBUS Source
PP_CABLE1/2 Input Voltage, Current	5 V, 500 mA	VCONN Source
PPH1 Voltage, Current	5 V – 20 V, 3 A (5 A Max)	VBUS Sink
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65987DDJ Circuitry

### 9.2.2.2.2 Detailed Design Procedure

#### 9.2.2.2.2.1 USB Power Delivery Source Capabilities

All Thunderbolt systems must support sourcing 5 V at 3 A (15 W). See the 表 9-8 for the PDO information.

**表 9-8. Source PDOs**

SOURCE PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A

#### 9.2.2.2.2.2 USB Power Delivery Sink Capabilities

Most notebooks support buck/boost charging which allows them to charge the battery from 5 V to 20 V. USB PD sources must also follow the Source Power Rules defined by the USB Power Delivery specification. It is recommended for notebooks to support all the voltages in the Source Power Rules to ensure compatibility with most PD chargers and adapters.

**表 9-9. Sink PDOs**

SINK PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A

**表 9-9. Sink PDOs (continued)**

SINK PDO	PDO TYPE	VOLTAGE	CURRENT
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A (5 A Max)

#### 9.2.2.2.3 Thunderbolt Supported Data Modes

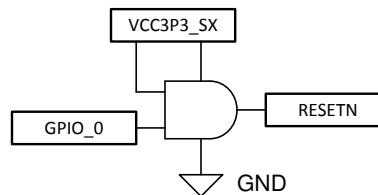
Thunderbolt Controllers are capable of generating USB3, DisplayPort and Thunderbolt Data. The Thunderbolt controller is also capable of muxing the appropriate super speed signal to the Type-C connector. Thunderbolt systems do not need a super speed mux for the Type-C connector. 表 9-10 summarizes the data capabilities of each Type-C port supporting Thunderbolt.

**表 9-10. Data Capabilities**

PROTOCOL	DATA	DATA ROLE
USB Data	USB3.1 Gen2	Host
DisplayPort	DP1.4	Host DFP_D (Pin Assignment C, D, and E)
Thunderbolt	PCIe/DP	Host/Device

#### 9.2.2.2.4 RESETN

The TPS65987DDJ and the Thunderbolt controller share the same flash and they must be able to access it at different times. The TPS65987DDJ will access the flash first to load its configuration and then the Thunderbolt controller will read the flash for its firmware. The TPS65987DDJ will hold the Thunderbolt controller in reset until it has read its configuration from the flash. GPIO\_0 is reserved to act as the reset signal for the Thunderbolt controller. The RESET\_N (Thunderbolt Controller Master Reset) signal must also be gated by the 3.3-V supply to the Thunderbolt controller (VCC3P3\_SX). When the RESET\_N signal is de-asserted before the supply has come up it may put the Thunderbolt controller in a latched state. The RESET\_N signal must be de-asserted at least 100  $\mu$ s after the Thunderbolt Controller supply has come up. For dead battery operation the GPIO\_0 signal should be “ANDed” with the 3.3-V supply to avoid de-asserting the RESETN when the Thunderbolt controller is not powered. The figure below shows the RESET\_N control with GPIO\_0 and the 3.3-V supply. Alternatively, the EC could configure GPIO\_0 to de-assert RESETN when the system has successfully booted.


**图 9-8. RESETN Circuit**

#### 9.2.2.2.5 I<sup>2</sup>C Design Requirements

The I<sup>2</sup>C connection from the TPS65987DDJ and the Thunderbolt control allows the Thunderbolt controller to read the current data status from the TPS65987DDJ when there is a connection on the Type-C port. The Thunderbolt controller has an interrupt assigned for TPS65987DDJ and the Thunderbolt controller will read the I<sup>2</sup>C address corresponding to the Type-C port. The I<sup>2</sup>C2 on the TPS65987DDJ is always connected to the Thunderbolt controller and the I<sup>2</sup>C channel will respond to the 0x38 address.

#### 9.2.2.2.6 TS3DS10224 SBU Mux for AUX and LSTX/RX

The SBU signals must be muxed from the Type-C connector to the Thunderbolt controller. The AUX for DisplayPort and LSTX/RX for Thunderbolt are connected to the TS3DS10224 and then muxed to the SBU pins. The SBU mux is controlled through GPIOs from the TPS65987DDJ. The table below shows the TPS65987DDJ GPIO events and the control signals from the TS3DS10224.

**表 9-11. GPIO Events for SBU Mux**

TPS65987DDJ GPIO EVENT	TS3DS10224 CONTROL
Port 0 Cable Orientation Event	SAO, SBO
Port 0 DP Mode Selection Event	ENA
Port 0 TBT Event	ENB
N/A	SAI tied to VCC
N/A	SBI tied to GND

The table below shows the connections for the AUX, LSTXRX, and SBU pins for the TS3DS10224.

**表 9-12. TS3DS10224 Pin Connections**

TS3DS10224 PIN	SIGNAL
INA+	SBU1
INA-	SBU2
OUTB0+	LSTX
OUTB0-	LSRX
OUTB1+	LSRX
OUTB1-	LSTX
OUTA0+	AUX_P
OUTA0-	AUX_N
OUTA1+	AUX_N
OUTA1-	AUX_P

#### 9.2.2.2.7 Thunderbolt Flash Options

In most Thunderbolt systems the TPS65987DDJ will share the flash with the Thunderbolt controller. The flash contains the Thunderbolt Controller firmware and the configuration data for the TPS65987DDJ. 表 9-13 shows the supported SPI flash options for Thunderbolt systems.

**表 9-13. Flash Supported for Thunderbolt Systems**

MANUFACTURER	PART NUMBER	SIZE
Winbond	W25Q80JVNIQ	8 Mb
Spansion	S25FL208K	8 Mb
AMIC	A25L080	8 Mb
Macronix	MX25L8006EM1I	8 Mb
Micron	M25PE80-VMN6TP	8 Mb
Micron	M25PX80-VMN6TP	8 Mb

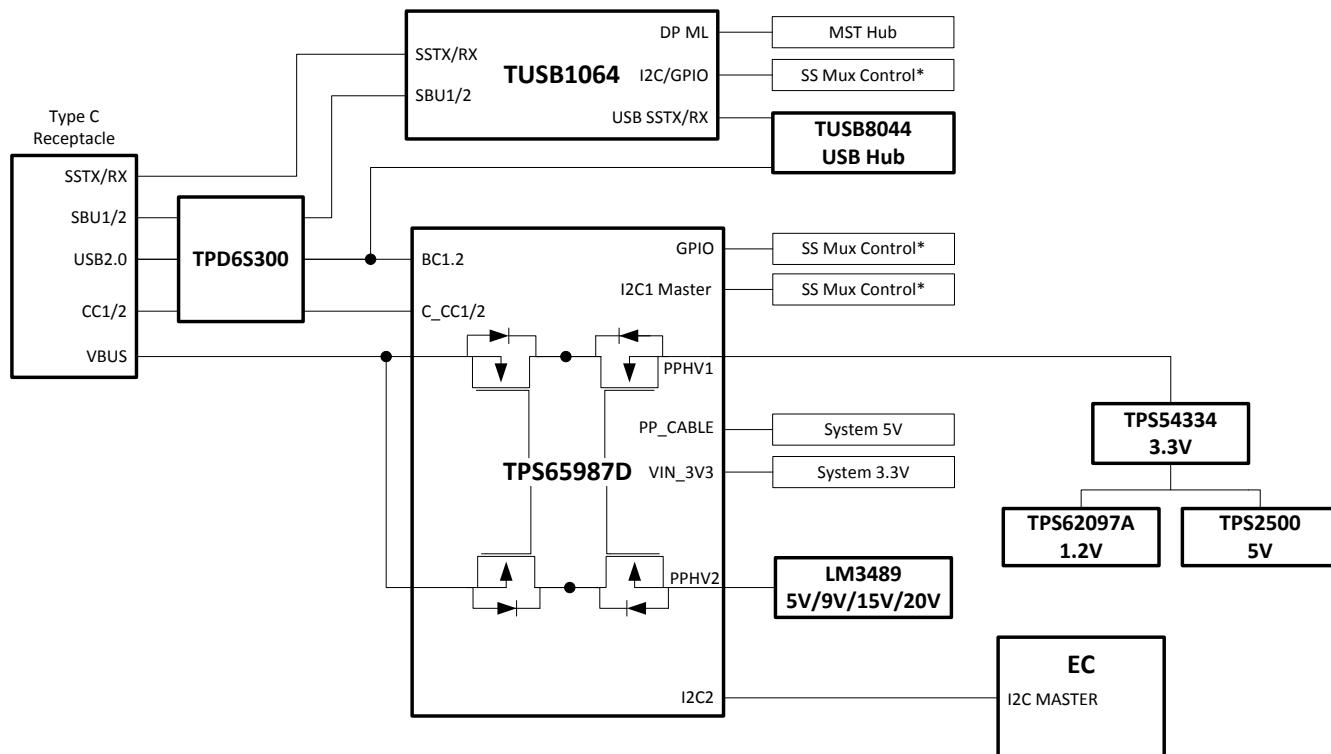
#### 9.2.2.3 USB and DisplayPort Dock with Bus-Powered and Self-Powered Support

A flexible dock application that can work either on Bus-Power or Self-Power takes advantage of the two integrated power paths. PPHV1 will sink power into the system when operating off Bus-Power and PPHV2 will source power on VBUS when powered. When the dock can operate in both modes it allows the end-user to use the dock in and out of an office.

The regulators that generate the required system voltages are powered from PPHV1 or the external dock supply. These rails powered from a main 3.3-V rail to ensure that the all the voltages required are valid in Bus-Powered and Self-Powered operation. This will also help for systems that support USB PD3.0 Fast Role Swap. There is a variable regulator to provide 5 V, 9 V, 15 V, and 20 V per the Power Delivery Rules.

The Super Speed signals from the Type-C connector are muxed to USB and MST Hubs through the TUSB1064. The DisplayPort and USB signals from the Super Speed Mux will go to a MST and USB HUB to enable additional video and USB connectors. The TPS65987DDJ can control the TUSB1064 Super Speed mux through

I<sup>2</sup>C or GPIO. The TPD6S300 provides additional protection such as short to VBUS on the CC and SBU pins and ESD for the USB2 DN/P. See [图 9-9](#) for the system block diagram.



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**图 9-9. USB and DisplayPort Dock Block Diagram**

#### 9.2.2.3.1 Design Requirements

The table below summarizes the Power Design parameters for a USB Type-C PD docking system.

**表 9-14. Power Design Parameters**

POWER DESIGN PARAMETERS	VALUE	CURRENT PATH
PPHV2 Input Voltage, Current	5 V/9 V/15 V/20 V, 3 A	VBUS Source
PP_CABLE1/2 Input Voltage, Current	5 V, 500 mA	VCONN Source
PPHV1 Voltage, Current	5 V, 1.5 A	VBUS Sink
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65987DDJ Circuitry

#### 9.2.2.3.2 Detailed Design Procedure

##### 9.2.2.3.2.1 USB Power Delivery Source Capabilities

When operating in Self-Powered mode the dock is recommended to support 60-W Power Delivery Rules to charge most systems. The table below shows the source PDO for the Type-C port.

**表 9-15. Source PDOs**

SOURCE PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A

#### 9.2.2.3.2.2 USB Power Delivery Sink Capabilities

Most Type-C notebooks will support 1.5 A at 5 V on VBUS which should require the dock should be able to operate at this current level. 表 9-16 shows the sink PDO for the Type-C port.

**表 9-16. Sink PDOs**

SINK PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	1.5 A

#### 9.2.2.3.2.3 USB and DisplayPort Supported Data Modes

The table below summarizes the data capabilities of the Type-C port supporting USB3 and DisplayPort.

**表 9-17. Data Capabilities**

PROTOCOL	DATA	DATA ROLE
USB Data	USB3.1 Gen2	Device
DisplayPort	DP1.4	Host UFP_D (Pin Assignment C and D)

#### 9.2.2.3.2.4 TUSB1064 Super Speed Mux GPIO Control

The TUSB1064 requires GPIO control in GPIO control mode to determine whether if there is USB or DisplayPort data connection. 表 9-18 summarizes the TPS65987DDJ GPIO Events and the control pins for the TUSB1064. Note that the pin strapping on the TUSB1064 will set the GPIO control mode and the required equalizer settings. For more details refer to the [TUSB1064 data sheet](#).

**表 9-18. GPIO Events for Super Speed Mux**

TPS65987DDJ GPIO EVENT	TUSB1064 CONTROL
Port 0 Cable Orientation Event	FLIP
Port 0 USB3 Event	CTL0
Port 0 DP Mode Selection Event	CTL1

## 10 Power Supply Recommendations

### 10.1 3.3-V Power

#### 10.1.1 VIN\_3V3 Input Switch

The VIN\_3V3 input is the main supply to the TPS65987DDJ device. The VIN\_3V3 switch (see [图 8-9](#)) is a unidirectional switch from VIN\_3V3 to LDO\_3V3, not allowing current to flow backwards from LDO\_3V3 to VIN\_3V3. This switch is on when 3.3 V is available. See [表 10-1](#) for the recommended external capacitance on the VIN\_3V3 pin.

#### 10.1.2 VBUS 3.3-V LDO

The 3.3-V LDO from VBUS steps down voltage from VBUS to LDO\_3V3 which allows the TPS65987DDJ device to be powered from VBUS when VIN\_3V3 is unavailable. This LDO steps down any recommended voltage on the VBUS pin. When VBUS is 20 V, as is allowable by USB PD, the internal circuitry of the TPS65987DDJ device operates without triggering thermal shutdown; however, a significant external load on the LDO\_3V3 pin can increase the temperature enough to trigger a thermal shutdown. The VBUS 3.3-V LDO blocks reverse current from LDO\_3V3 back to VBUS allowing VBUS to be unpowered when LDO\_3V3 is driven from another source. See [表 10-1](#) for the recommended external capacitance on the VBUS and LDO\_3V3 pins.

#### 10.2 1.8-V Power

The internal circuitry is powered from 1.8 V. The 1.8-V LDO steps the voltage down from LDO\_3V3 to 1.8 V. The 1.8-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, memory and other digital circuits. The 1.8-V LDO also provides power to all internal low-voltage analog circuits. See [表 10-1](#) for the recommended external capacitance on the LDO\_1V8 pin.

### 10.3 Recommended Supply Load Capacitance

[表 10-1](#) lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

**表 10-1. Recommended Supply Load Capacitance**

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABSOLUTE)	TYP (PLACED)	MAX (ABSOLUTE)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 $\mu$ F	10 $\mu$ F	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 $\mu$ F	10 $\mu$ F	25 $\mu$ F
CLDO_1V8	Capacitance on LDO_1V8	4 V	2.2 $\mu$ F	4.7 $\mu$ F	12 $\mu$ F
CVBUS1	Capacitance on VBUS1	25 V	0.5 $\mu$ F	1 $\mu$ F	12 $\mu$ F
CVBUS2	Capacitance on VBUS2	25 V	0.5 $\mu$ F	1 $\mu$ F	12 $\mu$ F
CPP_HV_SRC	Capacitance on PP_HV when configured as a 5-V source	10 V	2.5 $\mu$ F	4.7 $\mu$ F	
CPP_HV_SNK	Capacitance on PP_HV when configured as a 20-V sink	25 V	1 $\mu$ F	47 $\mu$ F	120 $\mu$ F
CPP_CABLE	Capacitance on PP_CABLE. When shorted to PP_HV configured as a 5-V source, the CPP_HV_SRC capacitance may be shared.	10 V	2.5 $\mu$ F	4.7 $\mu$ F	

## 11 Layout

## 11.1 Layout Guidelines

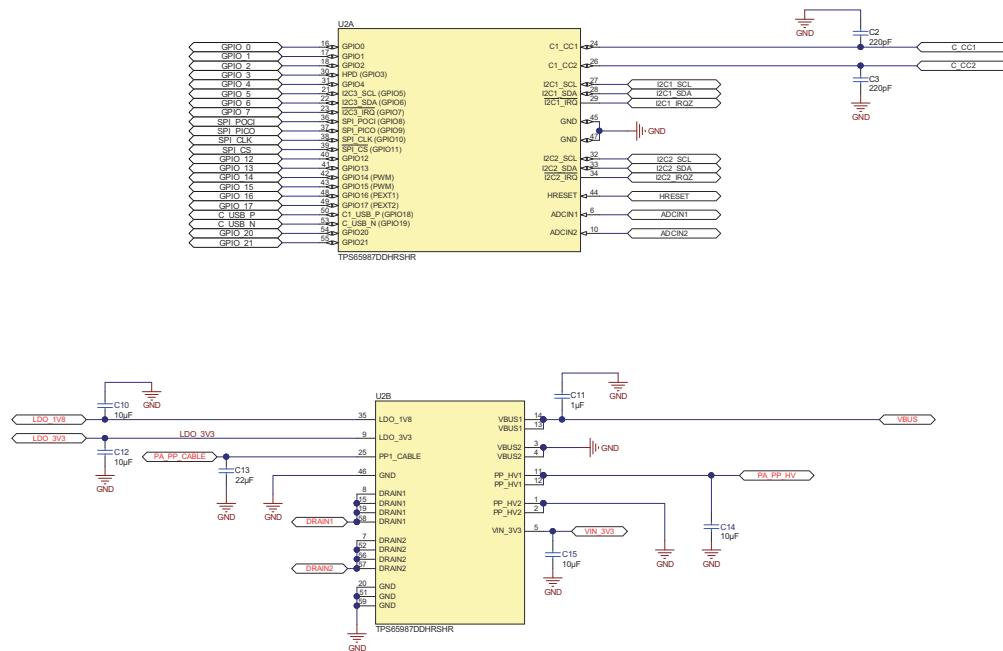
Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the TPS65987DDJ power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

### 11.1.1 Top TPS65987DDJ Placement and Bottom Component Placement and Layout

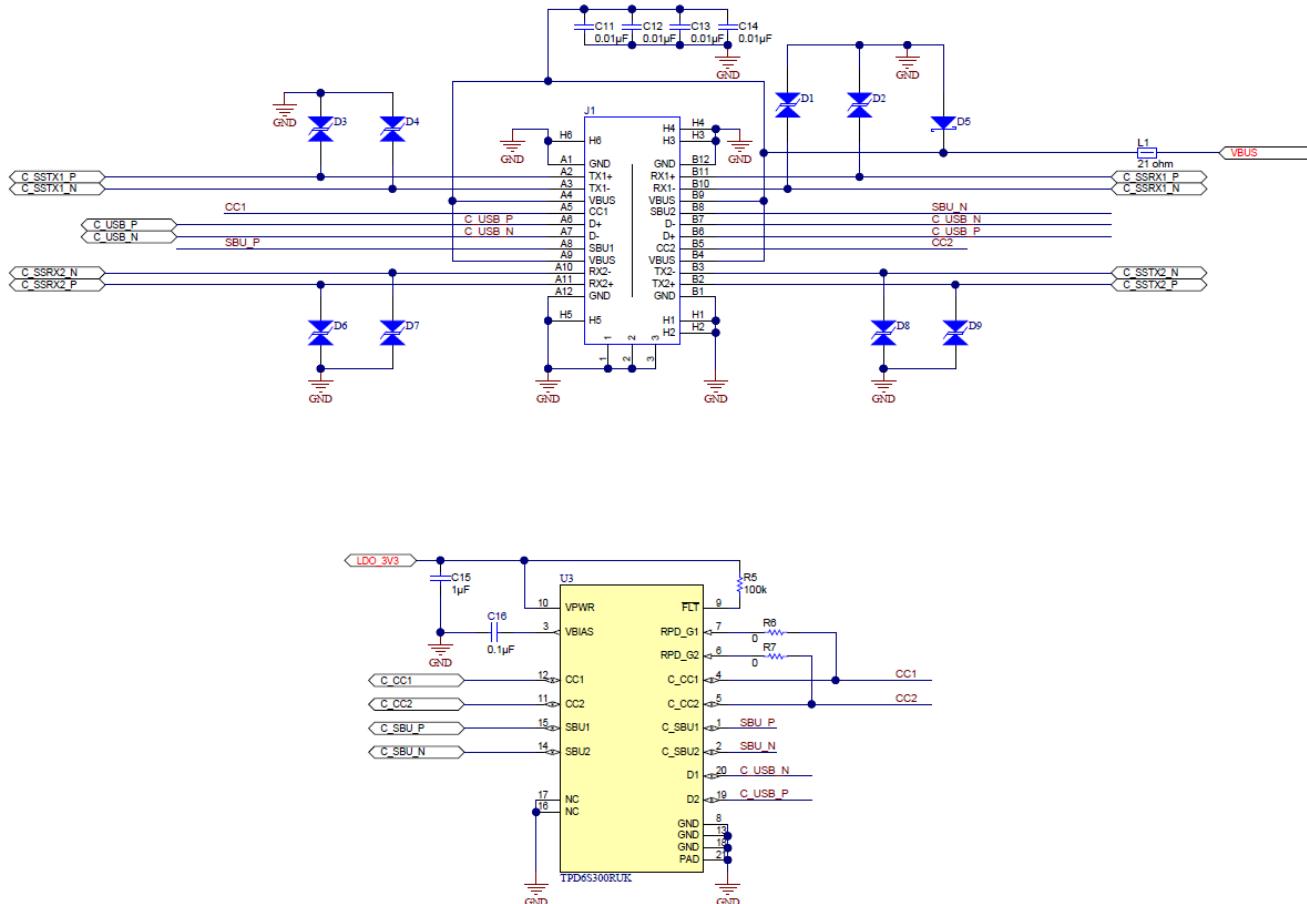
When the TPS65987DDJ is placed on top and its components on bottom the solution size will be at its smallest.

## 11.2 Layout Example

Follow the differential impedances for Super and High Speed signals defined by their specifications (DisplayPort - AUXN/P and USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will use all of the I/O on the TPS65987DDJ.



## FIG 11-1. Example Schematic



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图 11-2. Example Schematic2

### 11.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS65987DDJ is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, it is recommended that they are placed directly under the TPS65987DDJ. When placing the VBUS and PPHV capacitors it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS65987DDJ or to the side since the drain connection pads on the bottom layer should not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS65987DDJ should be placed where the GND terminal is underneath the GND pad.

The CC capacitors must be placed on the same side as the TPS65987DDJ close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

The ADCIN1/2 voltage divider resistors can be placed where convenient. In this layout example they are placed on the opposite layer of the TPS65987DDJ close to the LDO\_3V3 pin to simplify routing.

The figures below show the placement in 2-D and 3-D.

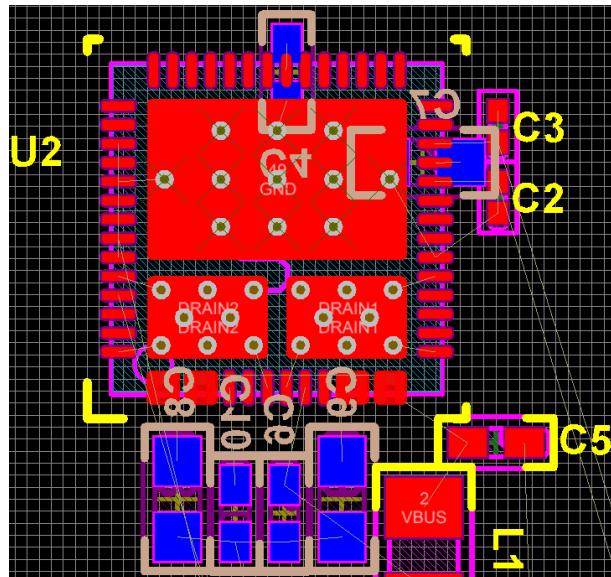


図 11-3. Top View Layout

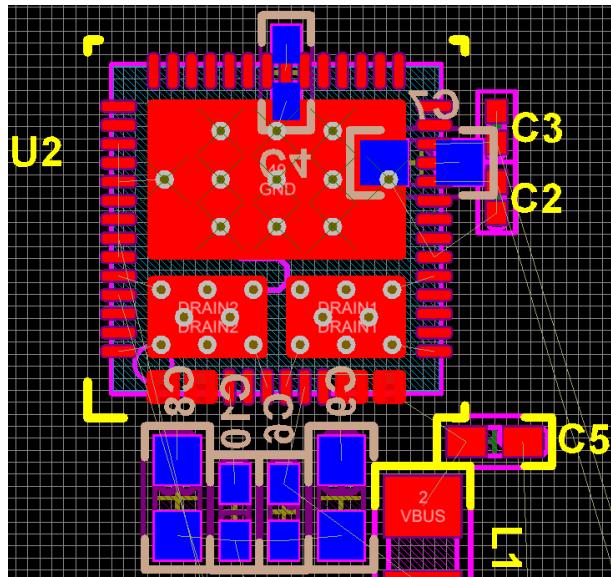


図 11-4. Bottom View Layout

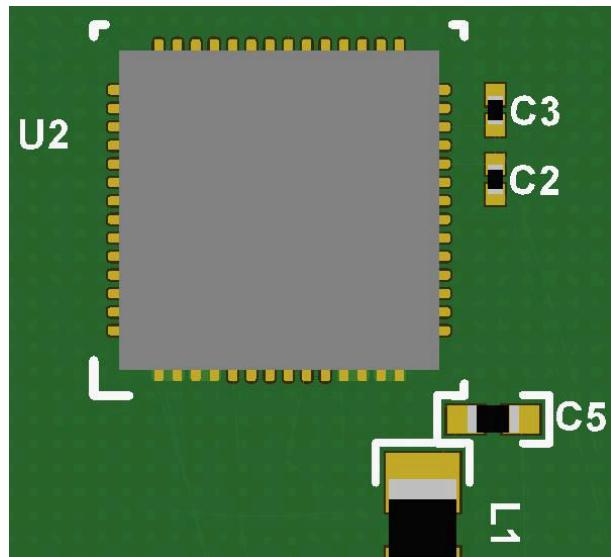


図 11-5. Top View 3-D

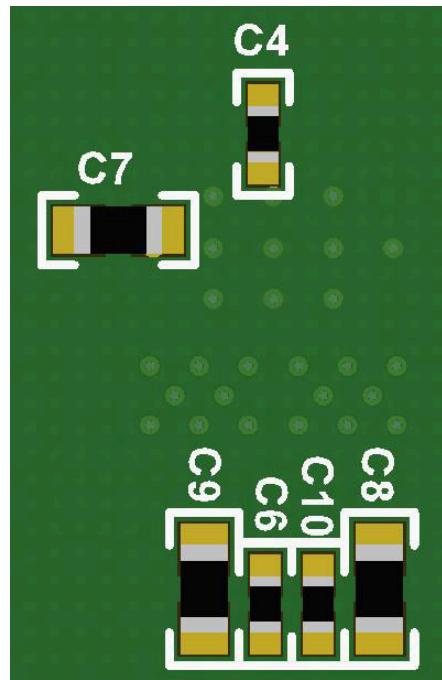


図 11-6. Bottom View 3-D

#### 11.4 Routing PP\_HV1/2, VBUS, PP\_CABLE, VIN\_3V3, LDO\_3V3, LDO\_1V8

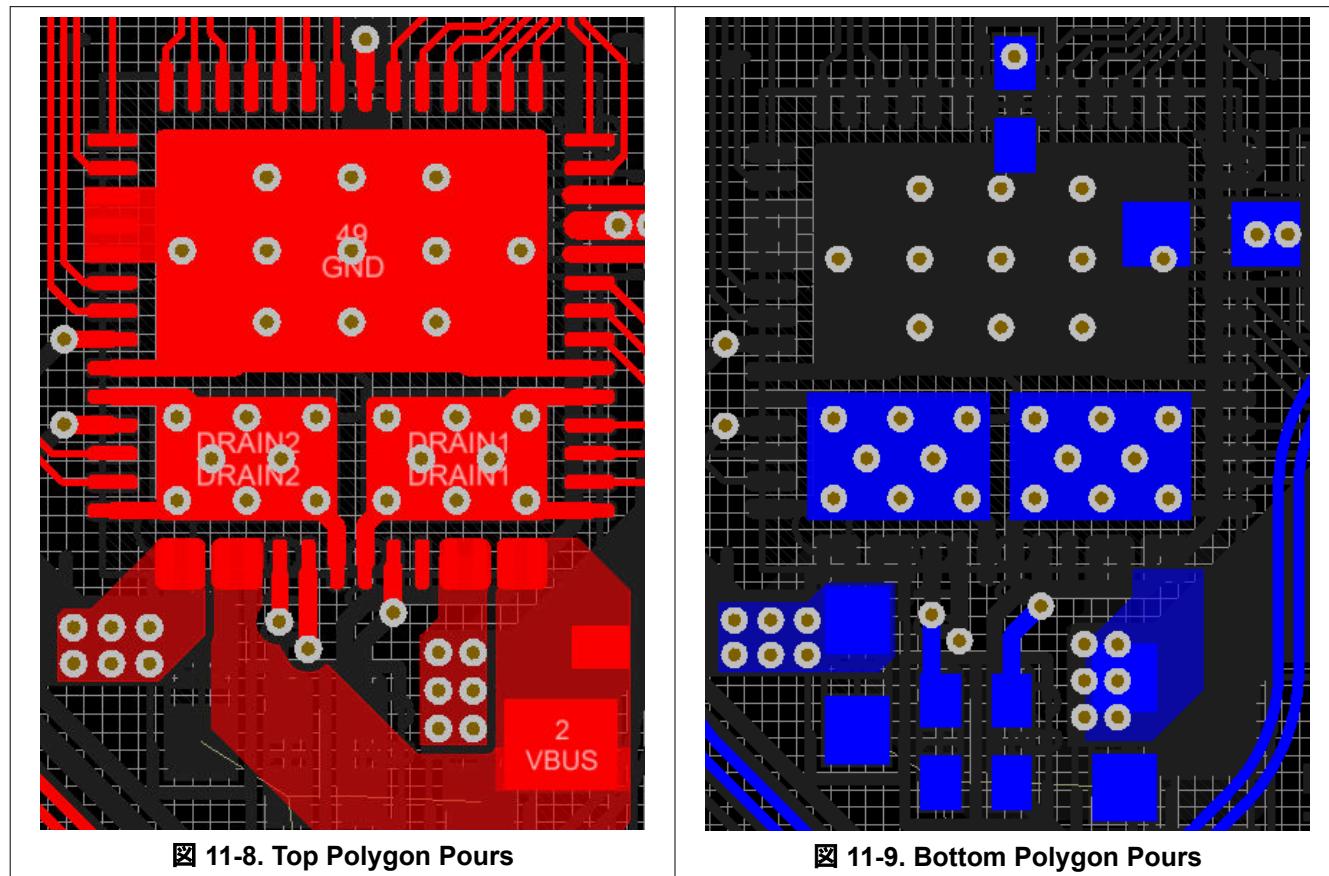
On the top side, create pours for PP\_HV1/2 and VBUS1/2 to extend area to place 8-mil hole and 16-mil diameter vias to connect to the bottom layer. See the figure below for the recommended via sizing.



図 11-7. Recommended Minimum Via Sizing

A minimum of four vias should be used to connect between the top and bottom layer power paths. For the bottom layer, place pours that will connect the PP\_HV1/2 and VBUS capacitors to their respective vias. For 5-A systems, special consideration must be taken for ensuring enough copper is used to handle the higher current. For 0.5-oz copper, top or bottom pours, with 0.5-oz plating will require about 120-mil pour width for 5-A support. When routing the 5 A through a 0.5-oz internal layer, more than 200 mil will be required to carry the current.

The figures below show the pours used in this example.



For PP\_CABLE, it is recommended to connect the capacitor to the pin with two vias. They should be placed side by side and as close to the pin as possible to allow for routing the CC lines.

Connect the bottom side VIN\_3V3 and LDO\_3V3 capacitors with traces through a via. The vias should have a straight connection to the respective pins. LDO\_1V8 is connected through a via on the outside of the pin and connected with a trace on the bottom side capacitor.

## 11.5 Routing CC and GPIO

Routing the CC lines with a 8-mil trace will ensure the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top layer with a 4-mil trace. The PP\_EXT1/2 GPIO control go through a via to be routed on another layer.

FIG 11-10 below shows the CC and GPIO routing.

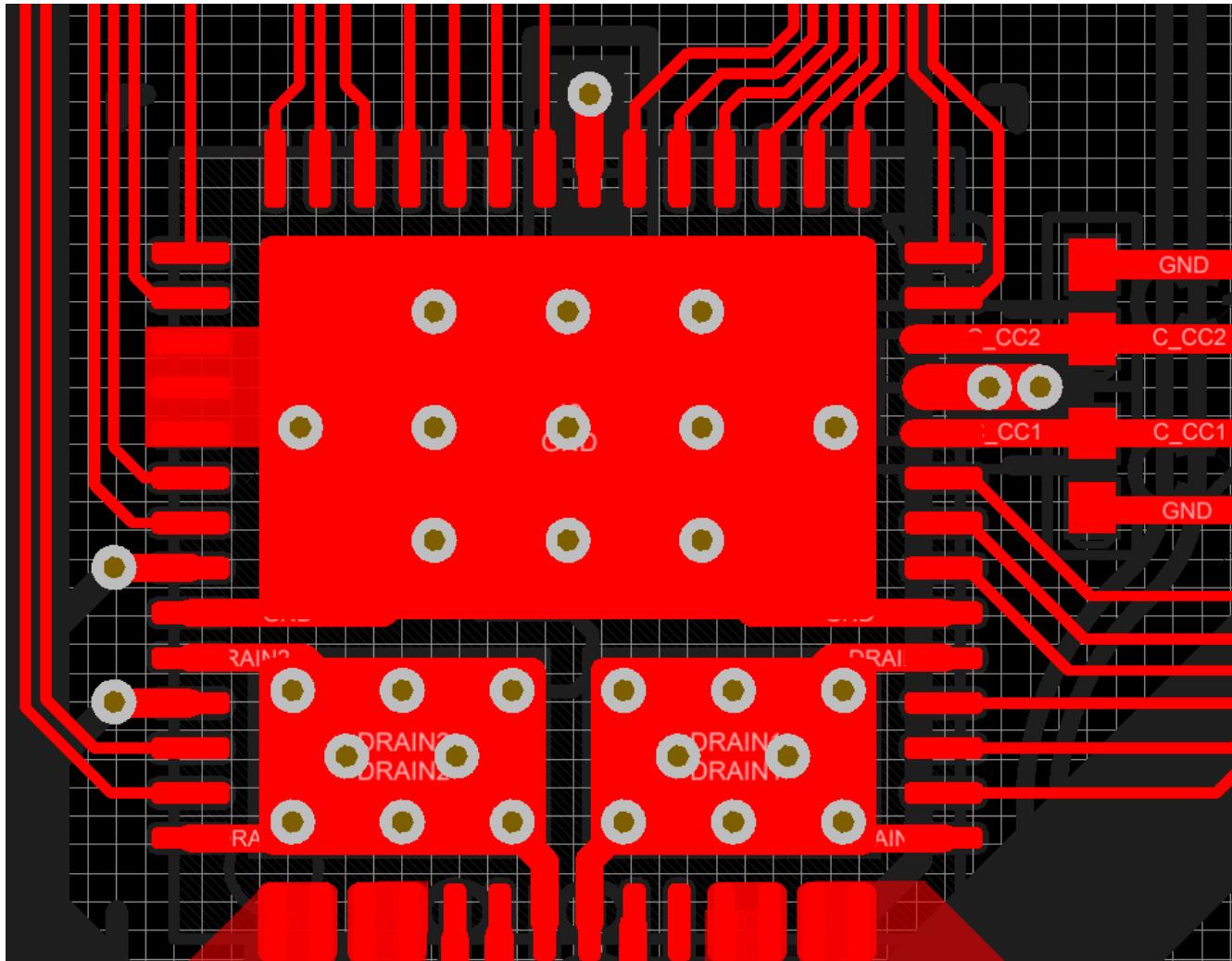


図 11-10. CC Routing and GPIO Fan-Out

表 11-1. Routing Widths

ROUTE	WIDTH (mil minimum)
CC1, CC2, PP_CABLE1, PP_CABLE2	8
VIN_3V3, LDO_3V3, LDO_1V8	6
Component GND	10
GPIO	4

## 11.6 Thermal Dissipation for FET Drain Pads

The TPS65987DDJ contains two internal FETs. To assist with thermal dissipation of these FETs, the drains of the FETs are connected to two metal pads underneath the IC. When completing a board layout for the TPS65987DDJ, it is important to provide copper pours on the top and bottom layer of the PCB for the thermal pads of each FET.

When looking at the footprint for the TPS65987DDJ, pins 57 and 58 are two smaller pads underneath the device. These are the drain pads for the two internal FETs. The dimensions are 1.75 mil x 2.6 mil and 1.75 mil x 2.55 mil for pins 57 and 58 respectively. Each of these FET pads should contain a minimum of six thermal vias through the PCB. This layout example contains 8 thermal vias through the PCB. On the bottom side of the PCB, the 1.75 mil x 2.6 mil and 1.75 mil x 2.55 mil thermal pads are mirrored to assist with thermal dissipation.

The figures below show the copper fills for the FET Drain pads.

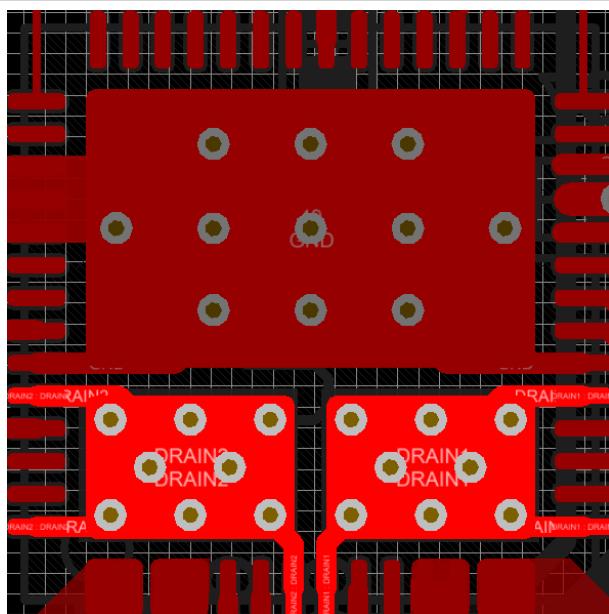


図 11-11. Top Layer FET Pads

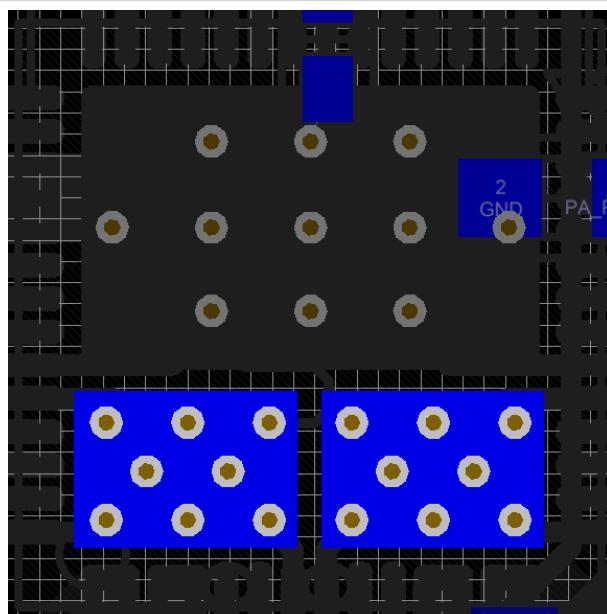


図 11-12. Bottom Layer FET Pads

As seen in the figures above, it is recommended to connect the Drain pins to their respective Drain pads underneath the IC. This will help with thermal dissipation by moving some of the heat away from the device. To further assist with thermal dissipation, it is possible to add copper fins on the top layer for both of the FET Drain Pads. When calculating the relative thermal dissipation, the first 3 mm of copper away from the device contribute largely to the thermal performance. Once the copper expands beyond 3 mm from the IC, there are diminishing returns in thermal performance.

図 11-13 highlights an example with copper fins to improve thermal dissipation.

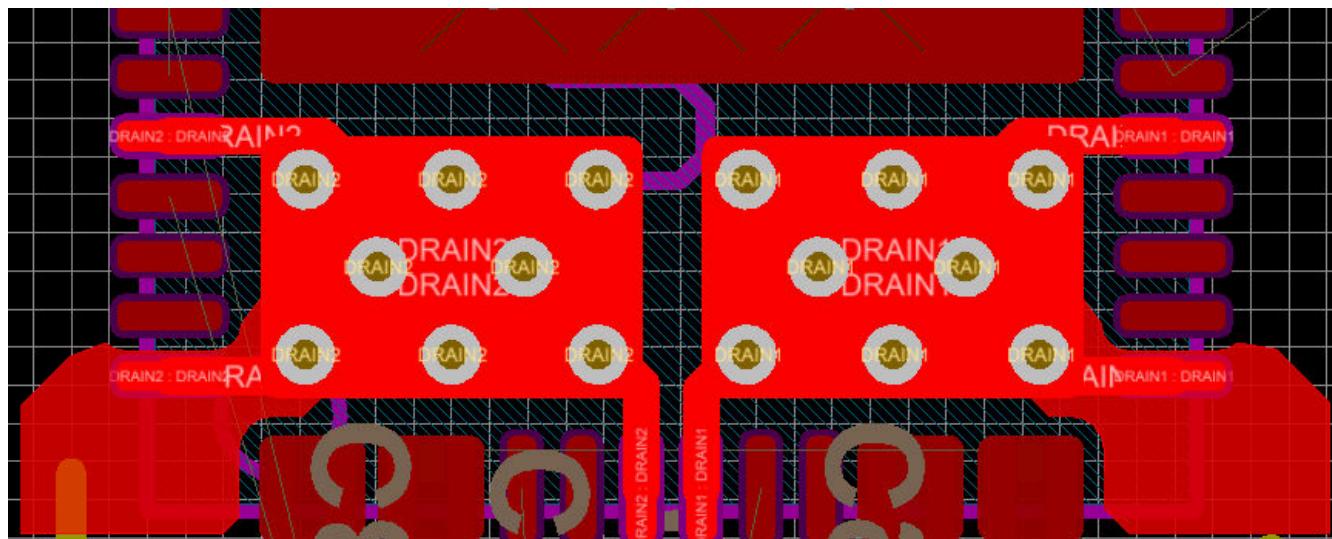


図 11-13. Copper Fins on Drain Pad

The thermal vias under each of the FET Drain Pads should be filled. Filling the vias will greatly improve the thermal dissipation on the FETs as there is significantly more copper that is connecting the top layer pad to the bottom layer copper. Alternatively, the vias can be epoxy filled but they will have higher thermal resistance. Each

8-/16-mil to 10-/20-mil via could have a thermal resistance ranging from 175°C/W to 200°C/W with board manufacturing variation. When doing thermal calculations it is recommended to use the worst case 200°C/W which will give a set of six vias a thermal resistance of approximately 33°C/W from the top to bottom pad. The vias in the FET pads should only be connected to copper pads on the top and bottom layers of the PCB. These should not be connected to GND. Refer to the image below to see which layers should be connected for the GND vias and FET Pad vias.

图 11-7 shows a common stack-up for systems that require Super Speed and high power routing.

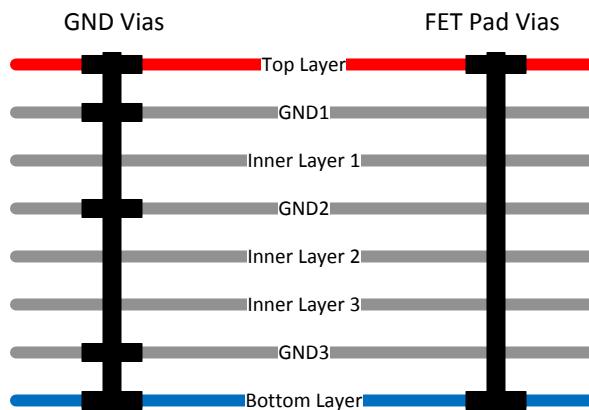


图 11-14. PCB Stack-Up

## 11.7 USB2 Recommended Routing For BC1.2 Detection/Advertisement

When routing the USB2 signals to the TPS65987DDJ BC1.2 detection pins it is recommended to reduce the amount of excess trace to get to the TPS65987DDJ pins, as this will cause antennae and degrade signal integrity. The USB top/bottom signals are shorted together in this example and the same approach can be used if an external USB mux is used. There are several approaches that can be used to get optimal routing; “tap” the USB2 signals with vias that connect the TPS65987DDJ pins, via up to the layer where the pins are located and continue to route on that layer, or a combination of both.

In this layout example, the D+/D- lines are routed to an internal layer from the connector. They are then via'd up to the TPS65987DDJ directly at the pins. There is a small trace that is connecting the via to the pin on the top layer. When routing the D+/D- in this manner, the added stub is minimal.

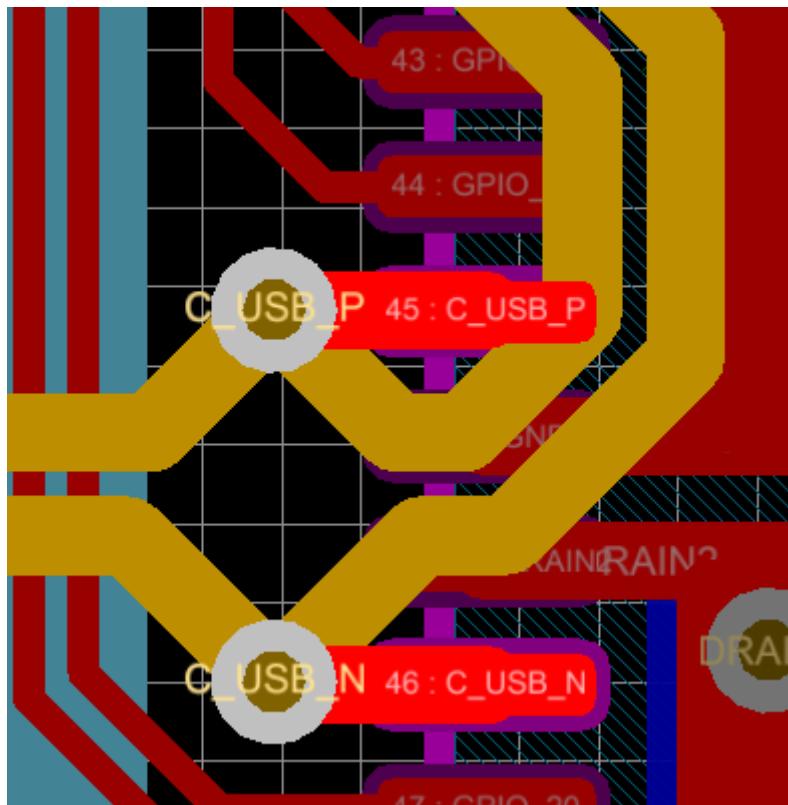


图 11-15. Via Connection for USB2

图 11-16 shows the entire routing from the Type-C connector, ESD Protection, and TPS65987DDJ BC1.2 Detection. This example does not take length matching into consideration but it is recommended to follow standard USB2 rules for routing and length matching.

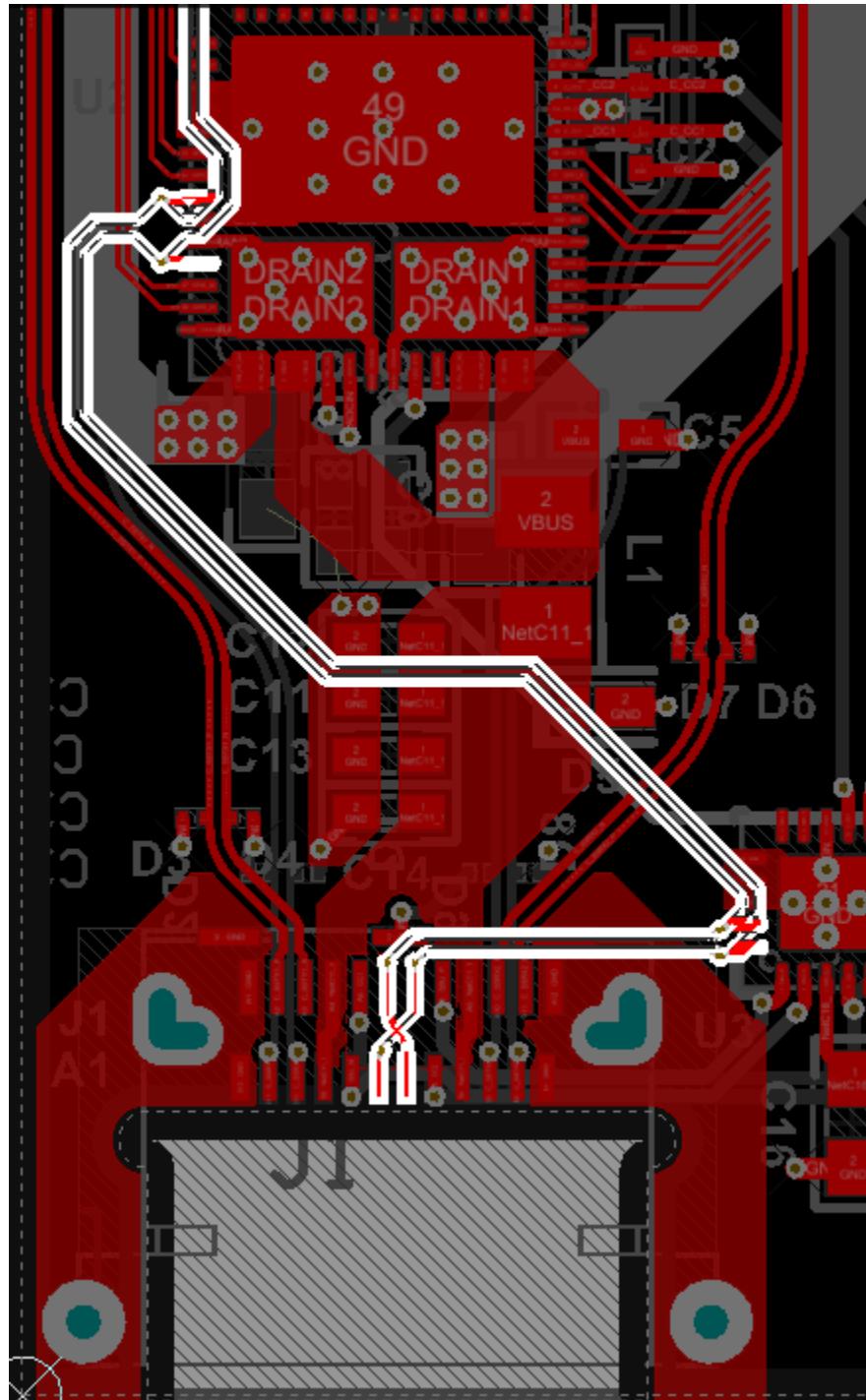


図 11-16. Complete USB2 Routing

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

- [TUSB1064 USB TYPE-C™ DP Alt Mode 10 Gbps Sink-Side Linear Redriver Crosspoint Switch](#) data sheet

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 サポート・リソース

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 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65987DDJRSR	NRND	Production	VQFN (RSH)   56	2500   LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-10 to 75	TPS65987D DJ
TPS65987DDJRSR.A	NRND	Production	VQFN (RSH)   56	2500   LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-10 to 75	TPS65987D DJ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

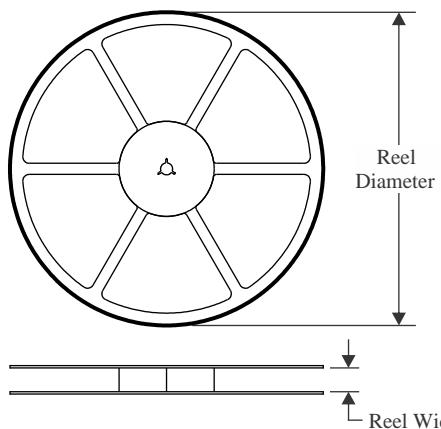
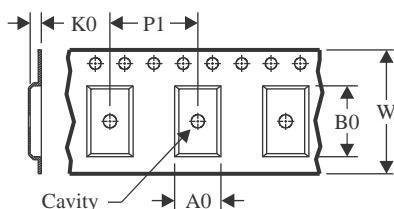
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

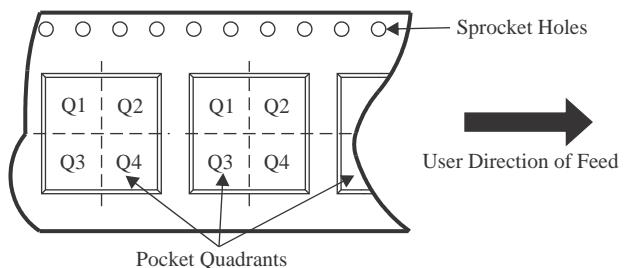
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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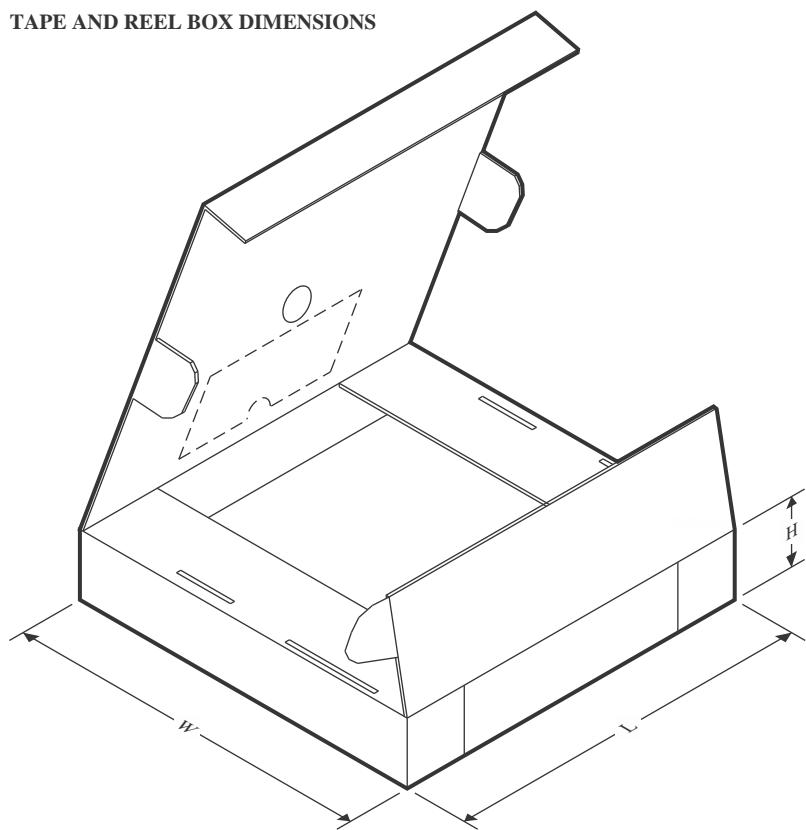
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65987DDJRSR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

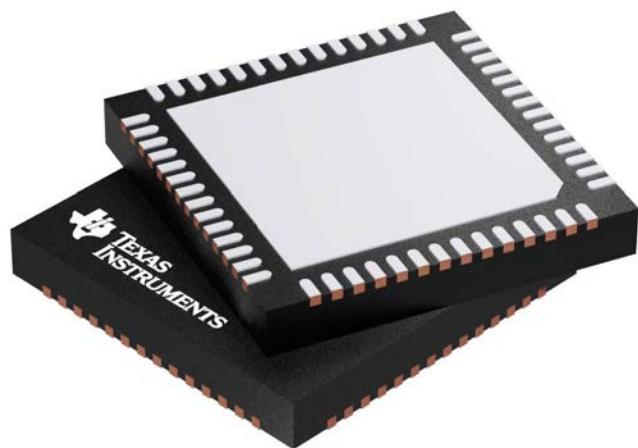
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65987DDJRSR	VQFN	RSH	56	2500	367.0	367.0	38.0

## GENERIC PACKAGE VIEW

**RSH 56**

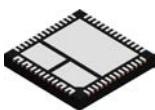
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

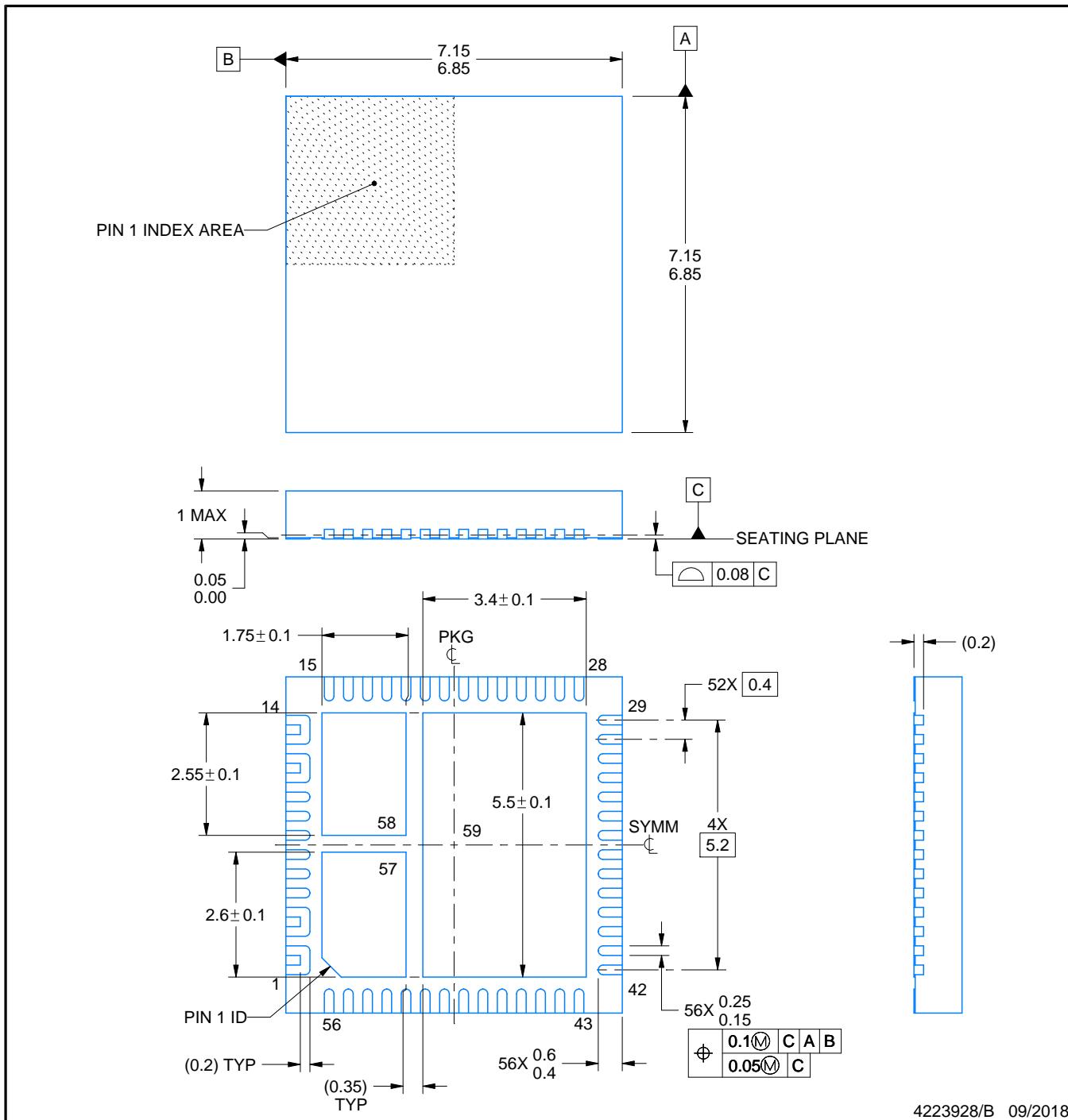
4207513/D



## PACKAGE OUTLINE

## VQFN - 1 mm max height

#### PLASTIC QUAD FLATPACK - NO LEAD



## NOTES:

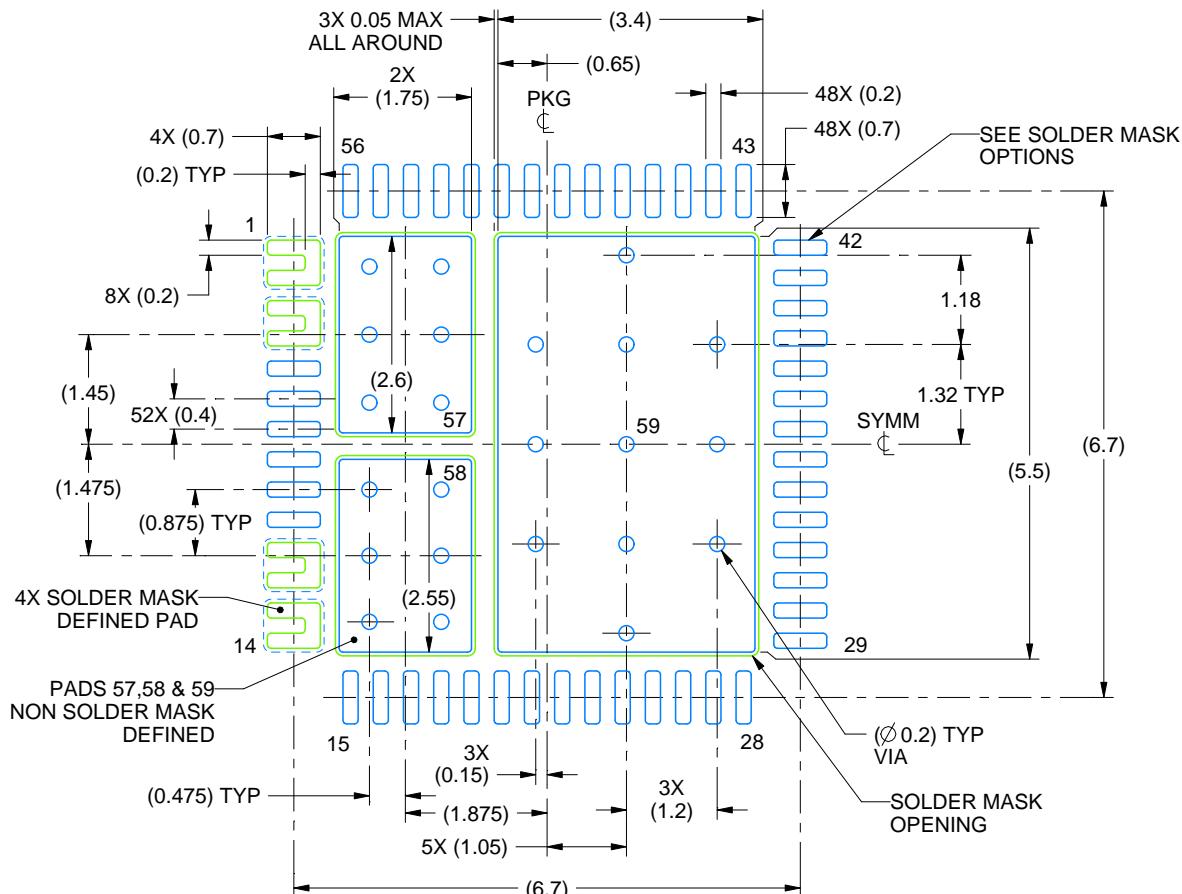
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

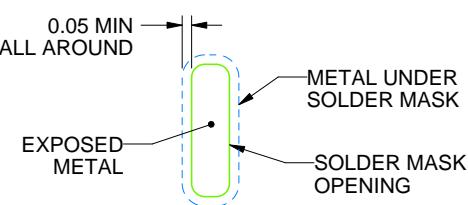
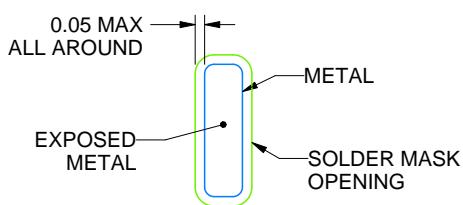
**RSH0056E**

## VQFN - 1 mm max height

#### PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK OPTIONS NOT TO SCALE

4223928/A 09/2018

#### NOTES: (continued)

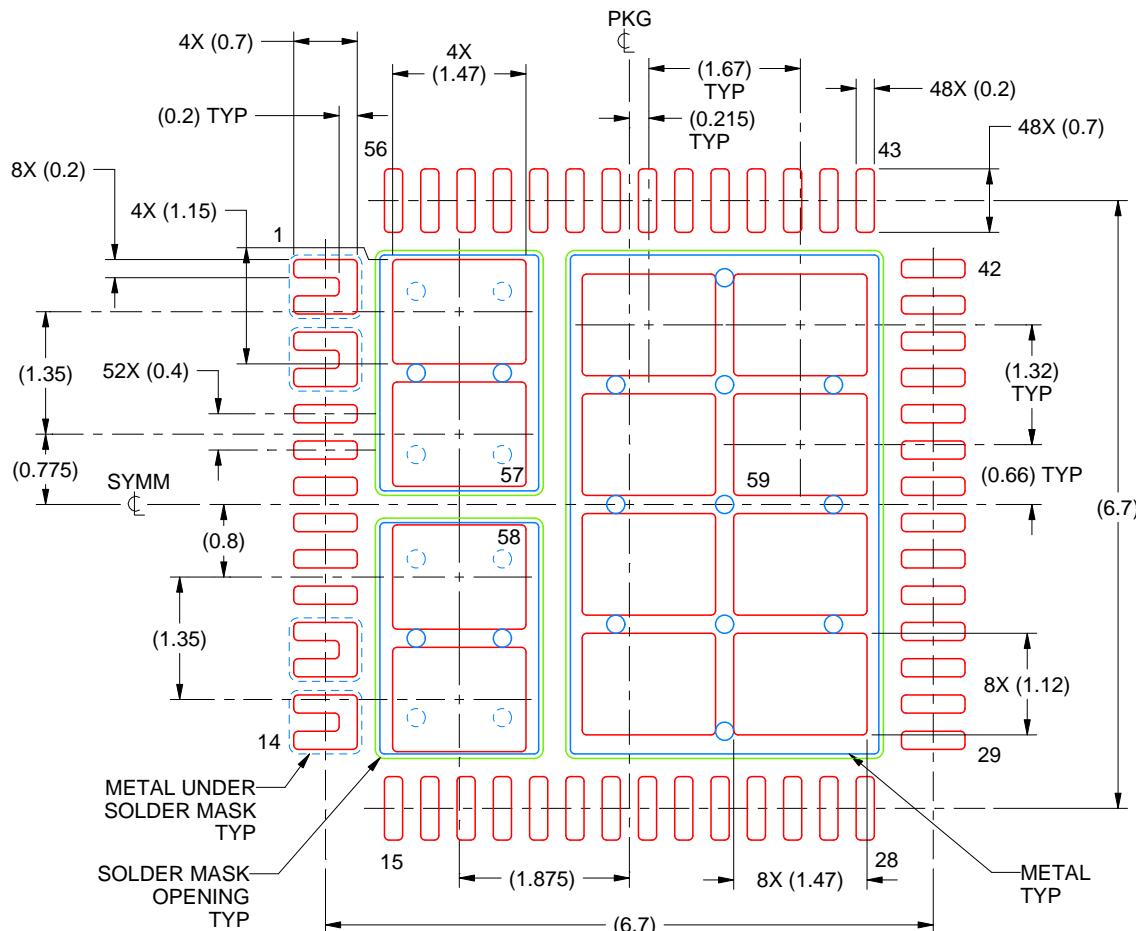
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**RSH0056E**

## VQFN - 1 mm max height

## PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 MM THICK STENCIL

EXPOSED PAD PRINTED SOLDER COVERAGE BY AREA  
PAD 57 & 58: 75%  
PAD 59: 70%  
SCALE: 12X

4223928/B 09/2018

#### NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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