

# TPS748 プログラマブル ソフトスタート機能付き、1.5A 低ドロップアウト リニア レギュレータ

## 1 特長

- $V_{OUT}$  範囲: 0.8V ~ 3.6V
- 非常に低い  $V_{IN}$  範囲: 0.8V ~ 5.5V
- $V_{BIAS}$  範囲: 2.7V ~ 5.5V
- 低いドロップアウト: 60 mV (標準値)、(1.5A、 $V_{BIAS} = 5V$  時)
- パワー グッド (PG) 出力により、電源電圧の監視や、他の電源のためのシーケンシング信号の供給が可能
- ライン、負荷、温度の全範囲にわたって 1% の精度 (新チップ)
- ライン、負荷、温度の全範囲にわたって 2% の精度 (レガシー チップ)
- プログラム可能なソフトスタートにより、直線的に電圧が立ち上がるようにスタートアップさせることが可能
- $V_{BIAS}$  により、過渡応答性に優れた低  $V_{IN}$  動作を実現
- 2.2 $\mu$ F 以上の出力コンデンサで安定動作
- 小型の 3mm × 3mm × 1mm VSON-10 および 5mm × 5mm VQFN-20 パッケージで供給

## 2 アプリケーション

- ネットワーク接続ストレージ (NAS) - エンタープライズ
- ラック・サーバー
- ネットワーク・インターフェイス・カード (NIC)
- 商用ネットワークとサーバーの PSU (電源)

## 3 概要

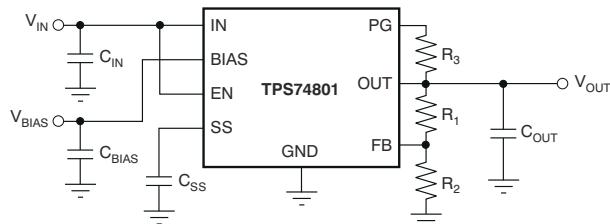
TPS748 低ドロップアウト (LDO) リニア レギュレータは、広範なアプリケーション向けの使いやすく堅牢な電力管理ソリューションです。ソフトスタートをユーザーがプログラムできるので、スタートアップ時の容量性突入電流を低減して、入力電源のストレスを最小限に抑えることができます。ソフトスタートは単調性で、多くの種類のプロセッサや ASIC の電源供給向けに設計されています。イネーブル入力とパワー グッド出力により、外部レギュレータとの間でシーケンシングを簡単に行えます。この優れた柔軟性により、FPGA、DSP、および特殊なスタートアップ要件を持つ他のアプリケーションのシーケンス要件を満たすソリューションを構成できます。

高精度の基準電圧およびエラー アンプは、負荷、ライン、温度、プロセスの全体にわたって 1% の精度 (新チップ) を維持します。本デバイスは 2.2 $\mu$ F 以上の任意のタイプのコンデンサで安定して動作し、 $T_J = -40^{\circ}\text{C} \sim +125^{\circ}\text{C}$  で仕様が規定されています。TPS748 は、小型の 3mm × 3mm VSON-10 パッケージで供給されるため、非常に小さいトータル ソリューション サイズを実現できます。このデバイスは、TPS742 との互換性を確保するため、5mm × 5mm の VQFN-20 パッケージでも供給されます。

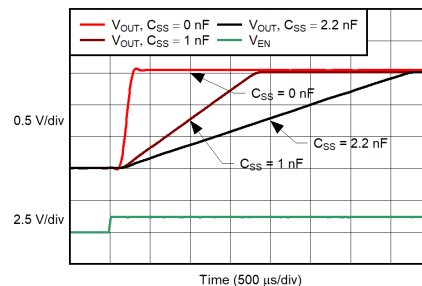
### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TPS748	DRC (VSON, 10)	3mm × 3mm
	RGW (VQFN, 20)	5mm × 5mm

- (1) 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路 (可変)



ターンオン応答



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## 4 Pin Configuration and Functions

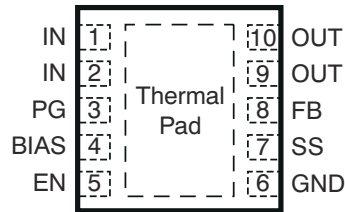


図 4-1. DRC Package, 10-Pin VSON With Thermal Pad (Top View)

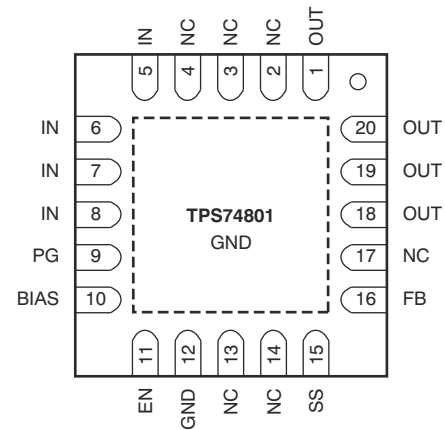


図 4-2. RGW Package, 20-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSON	VQFN		
BIAS	4	10	I	Bias input voltage for error amplifier, reference, and internal control circuits. A 1-μF or larger input capacitor is recommended for optimal performance. If IN is connected to BIAS, a 4.7-μF or larger capacitor must be used.
EN	5	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
FB	8	16	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	6	12	—	Ground
IN	1, 2	5-8	I	Input to the device. A 1-μF or larger input capacitor is recommended for optimal performance.
NC	N/A	2-4, 13, 14, 17	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	9, 10	1, 18-20	O	Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2 μF, ceramic) is needed from this pin to ground to assure stability.
PG	3	9	O	Power Good pin. An open-drain, active-high output that indicates the status of V <sub>OUT</sub> . When V <sub>OUT</sub> exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V <sub>OUT</sub> is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply of up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
SS	7	15	—	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 μs.
Thermal pad			—	Must be soldered to the ground plane for increased thermal performance. Internally connected to ground.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{IN}$ , $V_{BIAS}$	Input voltage	-0.3	6	V
$V_{EN}$	Enable voltage	-0.3	6	V
$V_{PG}$	Power-good voltage	-0.3	6	V
$I_{PG}$	PG sink current	0	1.5	mA
$V_{SS}$	Soft-start voltage	-0.3	6	V
$V_{FB}$	Feedback voltage	-0.3	6	V
$V_{OUT}$	Output voltage	-0.3	$V_{IN} + 0.3$	V
$I_{OUT}$	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
$P_{DISS}$	Continuous total power dissipation	See Thermal Information		
$T_J$	Junction Temperature	-40	150	°C
$T_{stg}$	Storage Temperature	-55	150	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input supply voltage	$V_{OUT} + V_{DO}$ ( $V_{IN}$ )	$V_{OUT} + 0.3$	5.5	V
$V_{EN}$	Enable supply voltage		$V_{IN}$	5.5	V
$V_{BIAS}$ <sup>(1)</sup>	BIAS supply voltage	$V_{OUT} + V_{DO}$ ( $V_{BIAS}$ ) <sup>(2)</sup>	$V_{OUT} + 1.6$ <sup>(2)</sup>	5.5	V
$V_{OUT}$	Output voltage	0.8		3.3	V
$I_{OUT}$	Output current	0		1.5	A
$C_{OUT}$	Output capacitor	2.2			μF
$C_{IN}$	Input capacitor <sup>(3)</sup>	1			μF
$C_{BIAS}$	Bias capacitor	0.1	1		μF
$T_J$	Operating junction temperature	-40		125	°C

- (1) BIAS supply is required when  $V_{IN}$  is below  $V_{OUT} + 1.62$  V.

- (2)  $V_{BIAS}$  has a minimum voltage of 2.7 V or  $V_{OUT} + V_{DO}$  ( $V_{BIAS}$ ), whichever is higher.

- (3) If  $V_{IN}$  and  $V_{BIAS}$  are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 μF.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS748				UNIT
		RGW (VQFN)	RGW (VQFN) <sup>(2)</sup>	DRC (VSON)	DRC (VSON) <sup>(2)</sup>	
		20 PINS	20 PINS	10 PINS	10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	35.6	34.7	44.2	47.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	33.3	31.0	50.3	63.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	15	13.5	19.6	19.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	1.4	0.7	4.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	15.2	13.5	17.8	19.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.8	3.6	4.3	3.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application note](#).  
 (2) New Chip.

## 5.5 Electrical Characteristics

at  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ ,  $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{NR} = 1\text{ nF}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5.0\text{ V}$ , and  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF}$	Internal reference (Adj.)	$T_A = 25^\circ\text{C}$	0.796	0.8	0.804	V
$V_{OUT}$	Output voltage range	$V_{IN} = 5\text{ V}$ , $I_{OUT} = 1.5\text{ A}$	$V_{REF}$		3.6	V
	Accuracy <sup>(1)</sup>	$2.97\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$ (Legacy Chip)	-2	$\pm 0.5$	2	%
		$2.97\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$ (New Chip)	-1	$\pm 0.3$	1	
$\Delta V_{OUT} (\Delta V_{IN})$	Line regulation	$V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$ (Legacy Chip)		0.03		% / V
		$V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$ (New Chip)		0.001		
$\Delta V_{OUT} (\Delta I_{OUT})$	Load regulation	$50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		0.09		% / A
$V_{DO}$	$V_{IN}$ dropout voltage <sup>(2)</sup>	$I_{OUT} = 1.5\text{ A}$ , $V_{BIAS} - V_{OUT(nom)} \geq 3.25\text{ V}$ (Legacy Chip) <sup>(3)</sup>		60	165	mV
		$I_{OUT} = 1.5\text{ A}$ , $V_{BIAS} - V_{OUT(nom)} \geq 3.25\text{ V}$ (New Chip) <sup>(3)</sup>		50	100	
	$V_{BIAS}$ dropout voltage <sup>(2)</sup>	$I_{OUT} = 1.5\text{ A}$ , $V_{IN} = V_{BIAS}$ (Legacy Chip)		1.31	1.6	V
		$I_{OUT} = 1.5\text{ A}$ , $V_{IN} = V_{BIAS}$ (New Chip)		1.31	1.43	
$I_{CL}$	Output current limit	$V_{OUT} = 80\% \times V_{OUT(nom)}$	2		5.5	A
$I_{BIAS}$	BIAS pin current	(Legacy Chip)		1	2	mA
		(New Chip)		1	1.2	
$I_{SHDN}$	Shutdown supply current ( $I_{GND}$ )	$V_{EN} \leq 0.4\text{ V}$ (Legacy Chip)		1	50	$\mu\text{A}$
		$V_{EN} \leq 0.4\text{ V}$ (New Chip)		0.85	2.75	
$I_{FB}$	Feedback pin current	(Legacy Chip)	-1	0.15	1	$\mu\text{A}$
		(New Chip)	-30	0.15	30	nA
PSRR	Power-supply rejection ( $V_{IN}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$		60		dB
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$		30		
	Power-supply rejection ( $V_{BIAS}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (Legacy Chip)		50		
		1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (New Chip)		59		
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (Legacy Chip)		30		
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (New Chip)		50		
$V_n$	Output noise voltage	BW = 100 Hz to 100 kHz, $I_{OUT} = 1.5\text{ A}$ , $C_{SS} = 1\text{ nF}$ (Legacy Chip)		$25 \times V_{OUT}$		$\mu\text{Vrms}$
		BW = 100 Hz to 100 kHz, $I_{OUT} = 1.5\text{ A}$ , $C_{SS} = 1\text{ nF}$ (New Chip)		$20 \times V_{OUT}$		
$t_{STR}$	Minimum startup time	$R_{LOAD}$ for $I_{OUT} = 1.0\text{ A}$ , $C_{SS} = \text{open}$ (Legacy Chip)		200		$\mu\text{s}$
		$R_{LOAD}$ for $I_{OUT} = 1.0\text{ A}$ , $C_{SS} = \text{open}$ (New Chip)		250		
$I_{SS}$	Soft-start charging current	$V_{SS} = 0.4\text{ V}$ (Legacy Chip)		440		nA
		$V_{SS} = 0.4\text{ V}$ (New Chip)		530		
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis	(Legacy Chip)		50		mV
		(New Chip)		55		
$V_{EN(dg)}$	Enable pin deglitch time			20		$\mu\text{s}$

## 5.5 Electrical Characteristics (続き)

at  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ ,  $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{NR} = 1\text{ nF}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5.0\text{ V}$ , and  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{EN}$	Enable pin current	$V_{EN} = 5\text{ V}$ (Legacy Chip)		0.1	1	$\mu\text{A}$
		$V_{EN} = 5\text{ V}$ (New Chip)		0.1	0.3	
$V_{IT}$	PG trip threshold	$V_{OUT}$ decreasing	85	90	94	$\%V_{OUT}$
$V_{HYS}$	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG(lo)}$	PG output low voltage	$I_{PG} = 1\text{ mA}$ (sinking), $V_{OUT} < V_{IT}$ (Legacy Chip)			0.3	V
		$I_{PG} = 1\text{ mA}$ (sinking), $V_{OUT} < V_{IT}$ (New Chip)			0.125	
$I_{PG(lkg)}$	PG leakage current	$V_{PG} = 5.25\text{ V}$ , $V_{OUT} > V_{IT}$ (Legacy Chip)		0.1	1	$\mu\text{A}$
		$V_{PG} = 5.25\text{ V}$ , $V_{OUT} > V_{IT}$ (New Chip)		0.001	0.05	
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		$^\circ\text{C}$
		Reset, temperature decreasing		140		
$R_{PULLDOWN}$	Output pulldown resistance	$V_{BIAS} = 5\text{ V}$ , $V_{EN} = 0\text{ V}$		0.83	1	$\text{k}\Omega$

- (1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
- (2) Dropout is defined as the voltage from  $V_{IN}$  to  $V_{OUT}$  when  $V_{OUT}$  is 3% below nominal.
- (3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 5-11.

## 5.6 Typical Characteristics: $I_{OUT} = 50\text{ mA}$

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

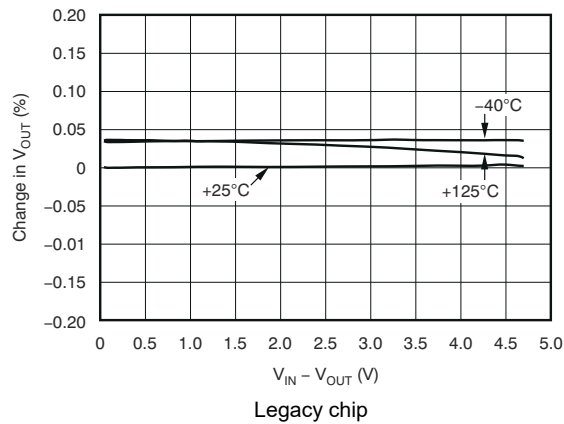


图 5-1.  $V_{IN}$  Line Regulation

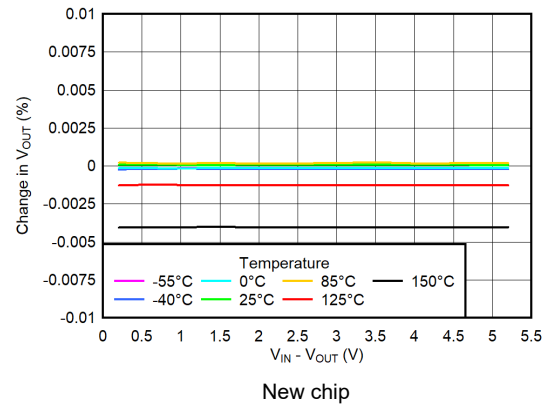


图 5-2.  $V_{IN}$  Line Regulation

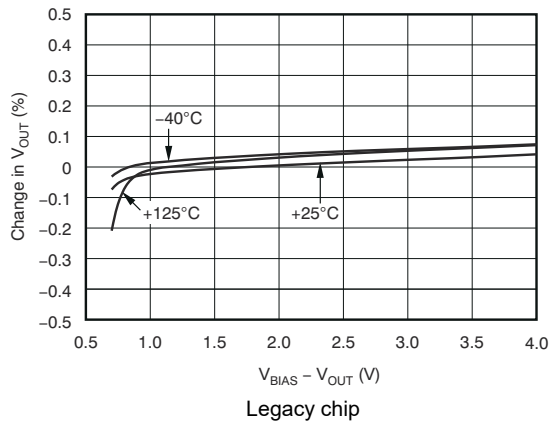


图 5-3.  $V_{BIAS}$  Line Regulation

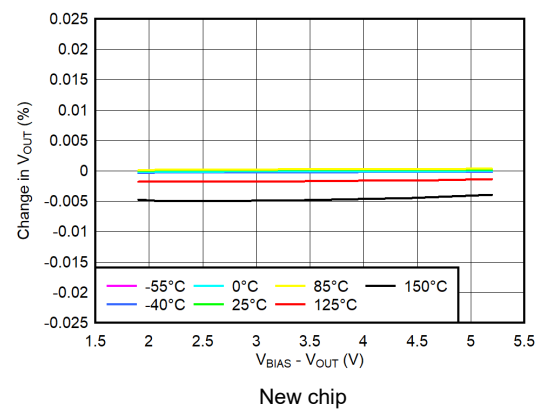


图 5-4.  $V_{BIAS}$  Line Regulation

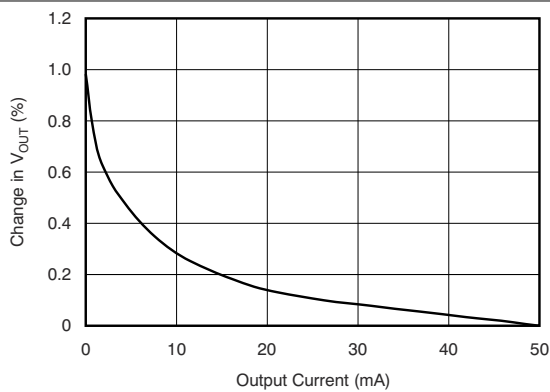


图 5-5. Load Regulation at Light Load

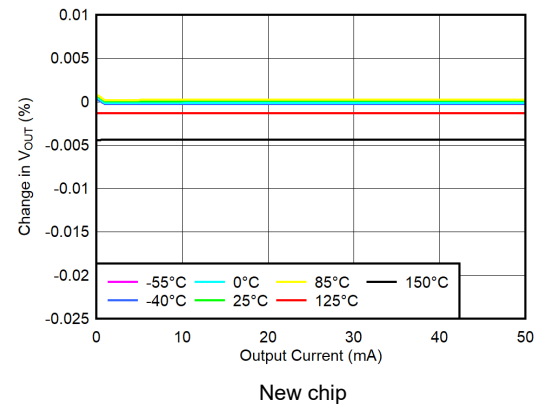


图 5-6. Load Regulation at Light Load



## 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

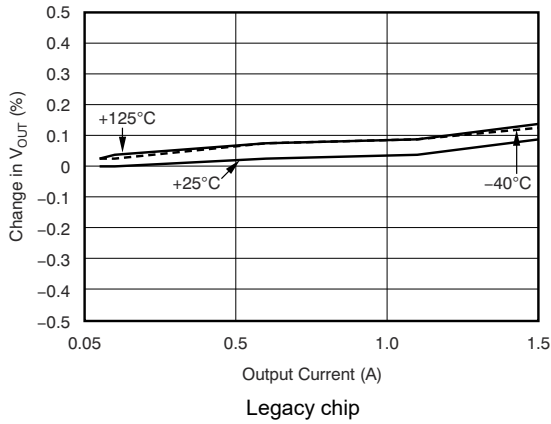


Figure 5-7. Load Regulation

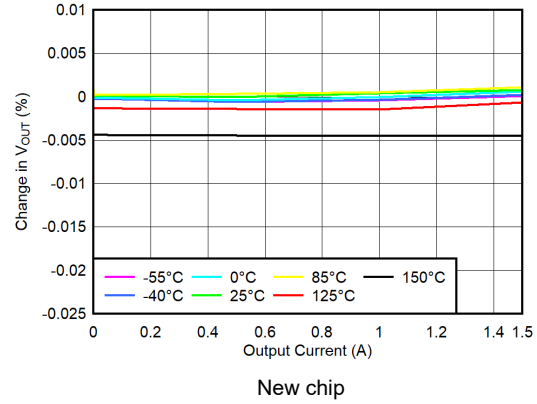


Figure 5-8. Load Regulation

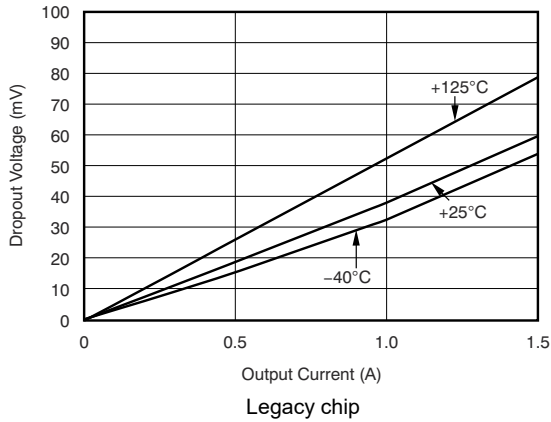


Figure 5-9.  $V_{IN}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

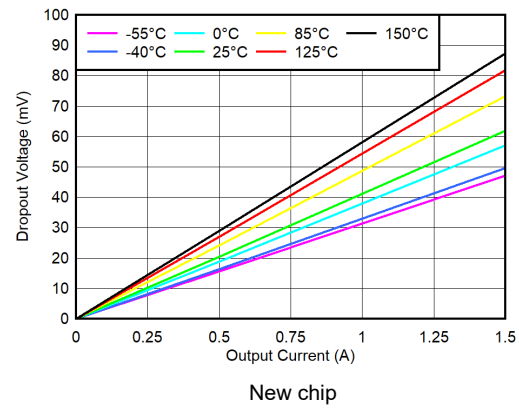


Figure 5-10.  $V_{IN}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

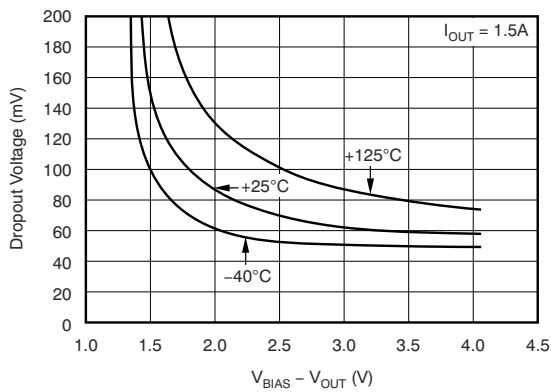


Figure 5-11.  $V_{IN}$  Dropout Voltage vs  $(V_{BIAS} - V_{OUT})$  and Temperature ( $T_J$ )

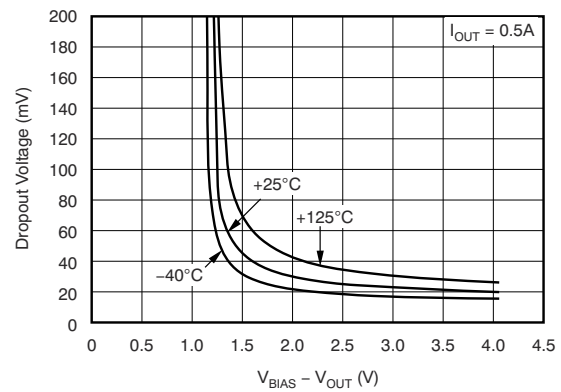


Figure 5-12.  $V_{IN}$  Dropout Voltage vs  $(V_{BIAS} - V_{OUT})$  and Temperature ( $T_J$ )

## 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

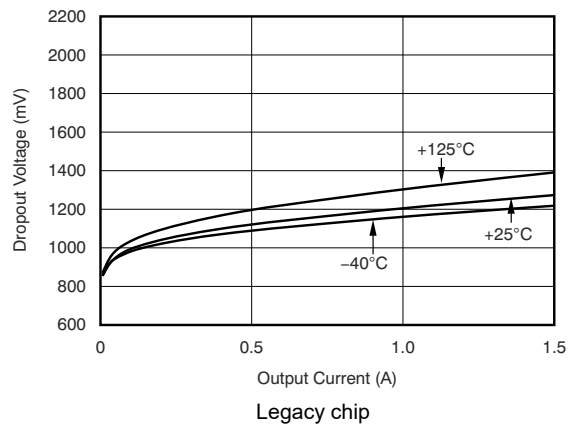


Figure 5-13.  $V_{BIAS}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

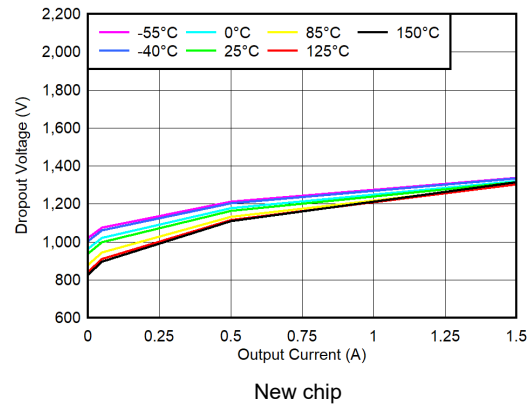


Figure 5-14.  $V_{BIAS}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

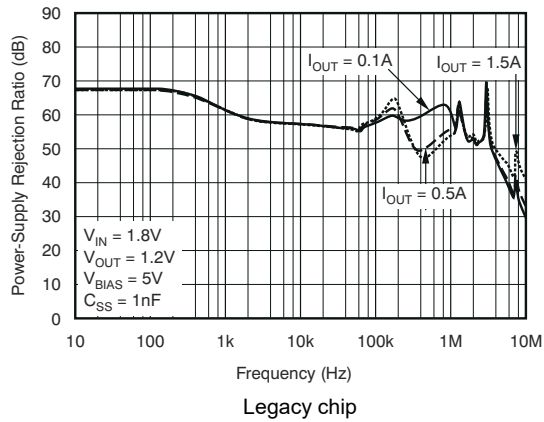


Figure 5-15.  $V_{BIAS}$  PSRR vs Frequency

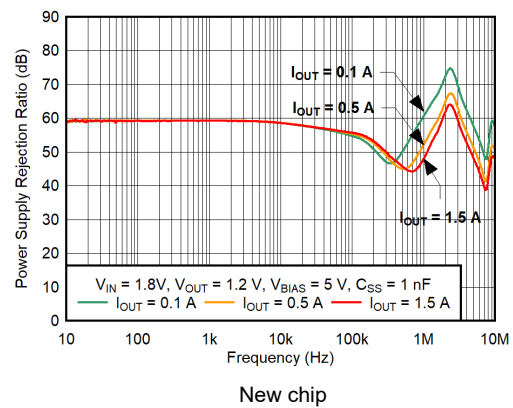


Figure 5-16.  $V_{BIAS}$  PSRR vs Frequency

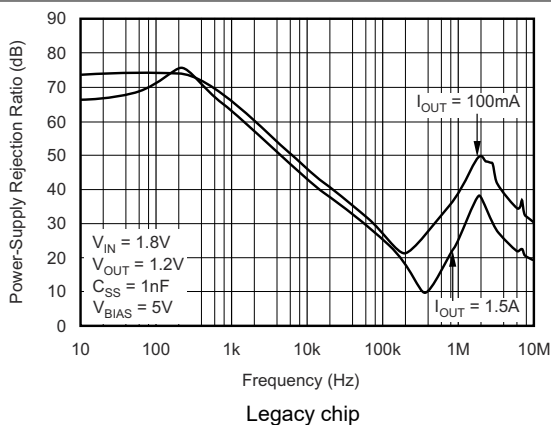


Figure 5-17.  $V_{IN}$  PSRR vs Frequency

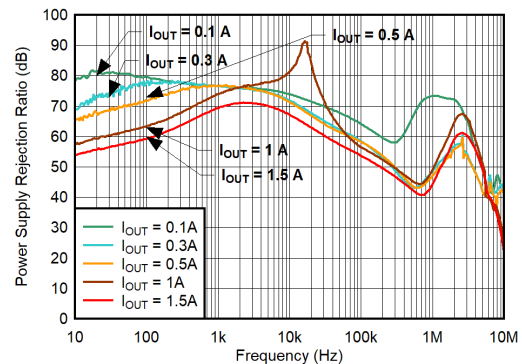


Figure 5-18.  $V_{IN}$  PSRR vs Frequency

## 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

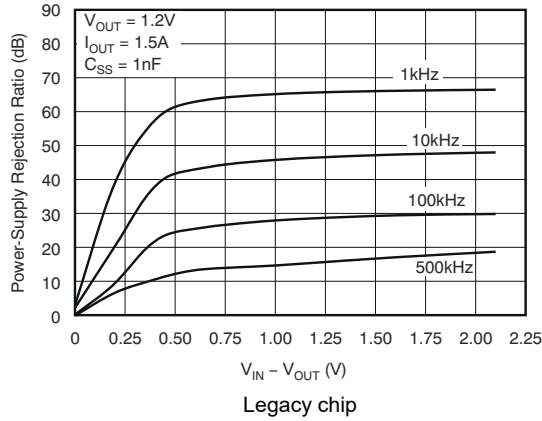


Figure 5-19.  $V_{IN}$  PSRR vs  $(V_{IN} - V_{OUT})$

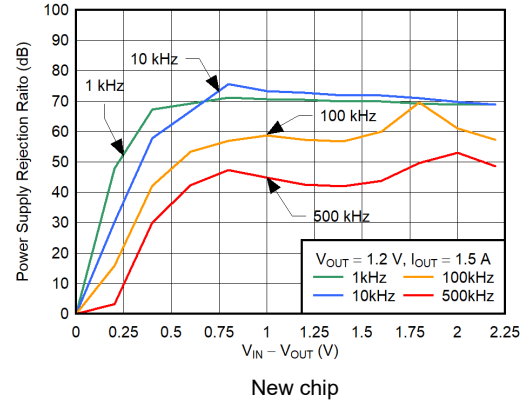


Figure 5-20.  $V_{IN}$  PSRR vs  $(V_{IN} - V_{OUT})$

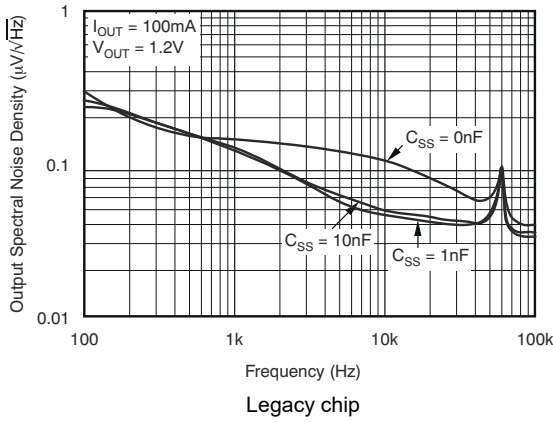


Figure 5-21. Noise Spectral Density

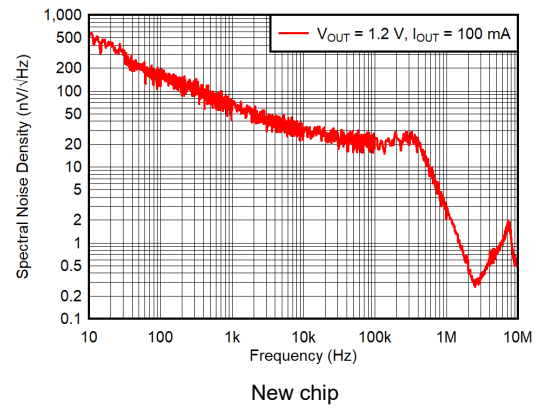


Figure 5-22. Noise Spectral Density

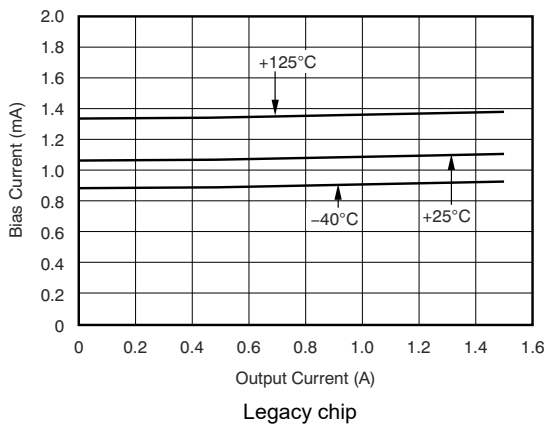


Figure 5-23. BIAS Pin Current vs Output Current and Temperature ( $T_J$ )

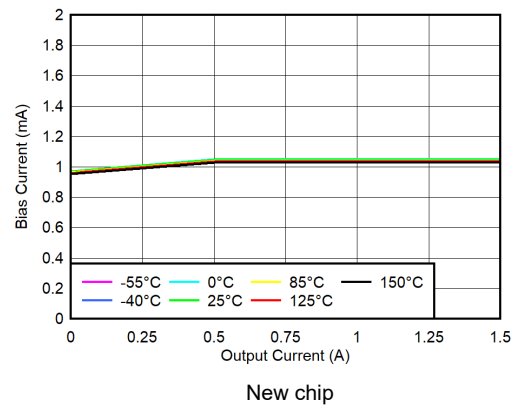


Figure 5-24. BIAS Pin Current vs Output Current and Temperature ( $T_J$ )

## 5.6 Typical Characteristics: $I_{OUT} = 50$ mA (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3$  V,  $V_{BIAS} = 5$  V,  $I_{OUT} = 50$  mA,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1$   $\mu\text{F}$ ,  $C_{BIAS} = 4.7$   $\mu\text{F}$ , and  $C_{OUT} = 10$   $\mu\text{F}$  (unless otherwise noted)

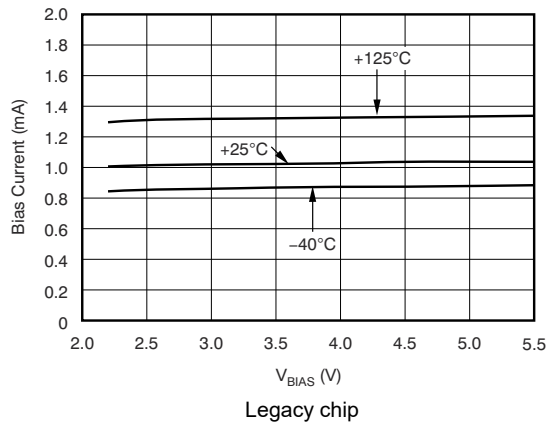


Figure 5-25. BIAS Pin Current vs  $V_{BIAS}$  and Temperature ( $T_J$ )

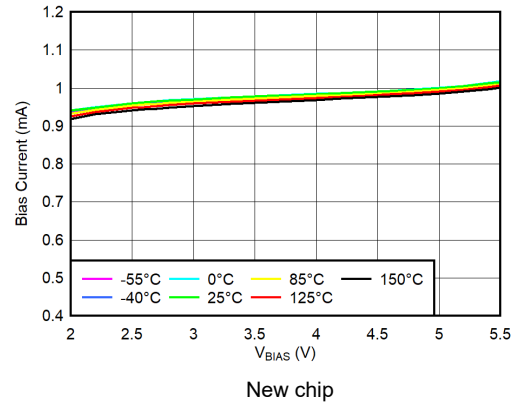


Figure 5-26. BIAS Pin Current vs  $V_{BIAS}$  and Temperature ( $T_J$ )

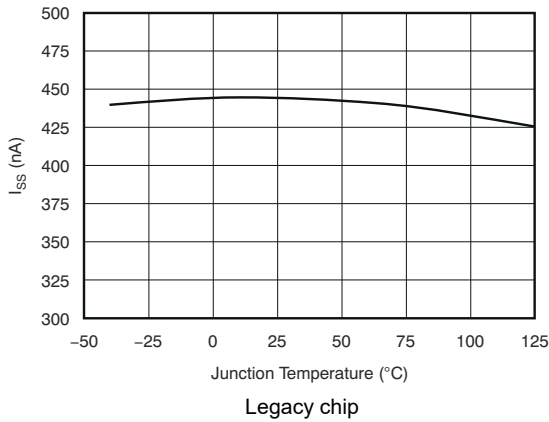


Figure 5-27. Soft-Start Charging Current ( $I_{SS}$ ) vs Temperature ( $T_J$ )

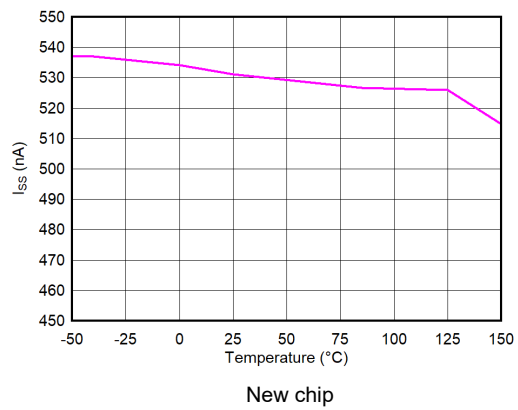


Figure 5-28. Soft-Start Charging Current ( $I_{SS}$ ) vs Temperature ( $T_J$ )

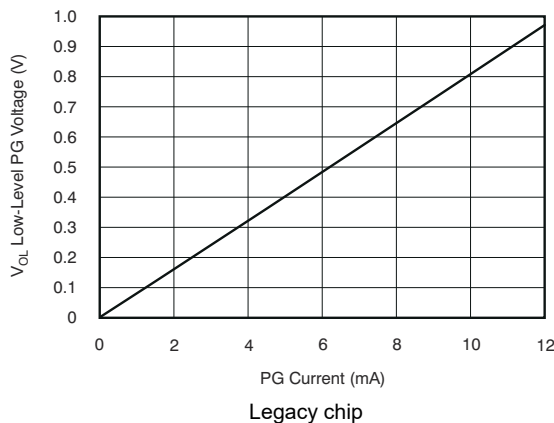


Figure 5-29. Low-Level PG Voltage vs Current

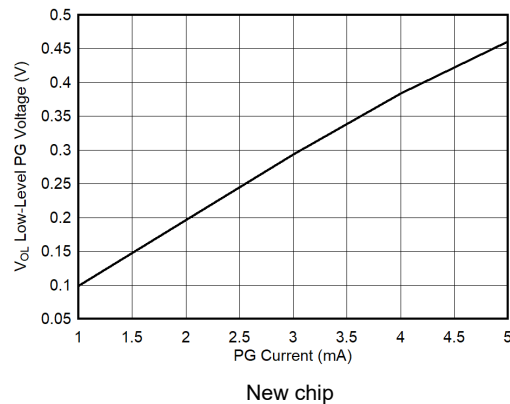
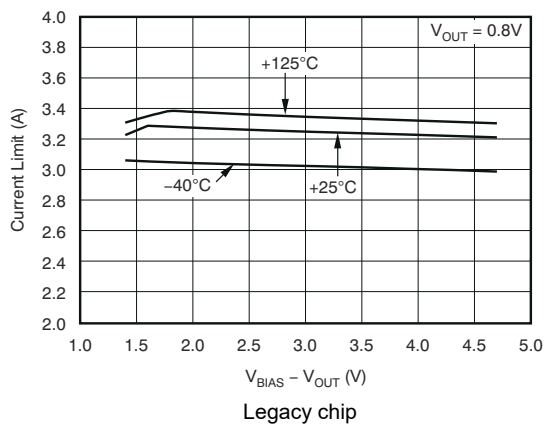


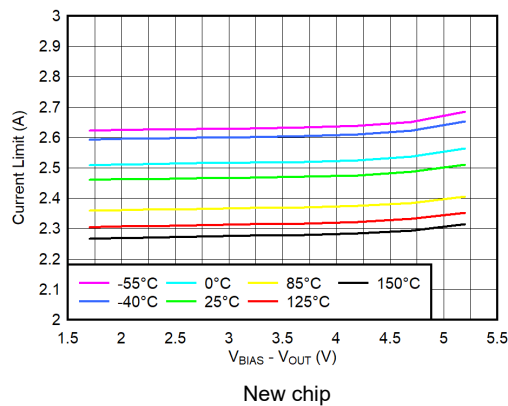
Figure 5-30. Low-Level PG Voltage vs Current

## 5.6 Typical Characteristics: $I_{OUT} = 50\text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)



5-31. Current Limit vs ( $V_{BIAS} - V_{OUT}$ )



5-32. Current Limit vs ( $V_{BIAS} - V_{OUT}$ )

## 5.7 Typical Characteristics: $I_{OUT} = 1\text{ A}$

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ ,  $V_{EN} = V_{IN} = 1.8\text{ V}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

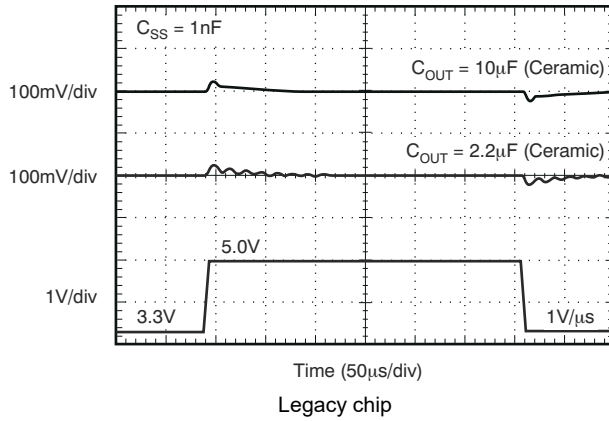


Figure 5-33.  $V_{BIAS}$  Line Transient

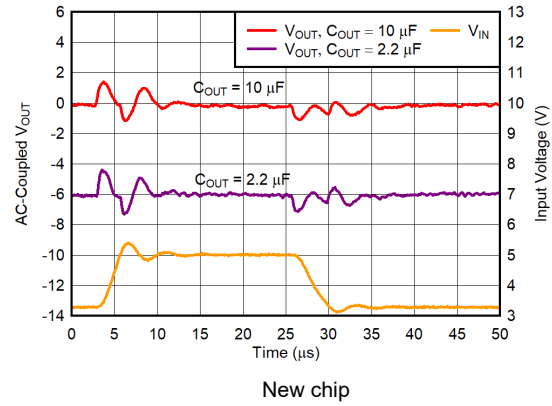


Figure 5-34.  $V_{BIAS}$  Line Transient

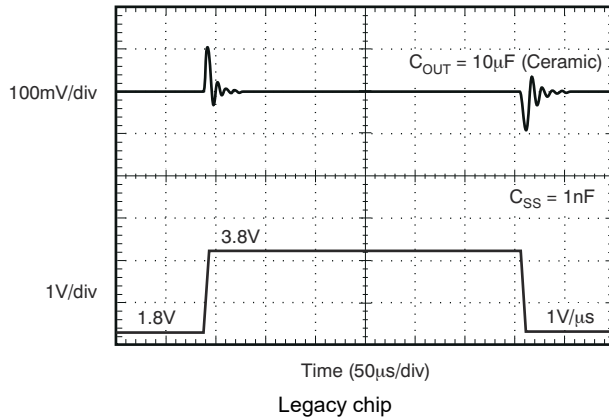


Figure 5-35.  $V_{IN}$  Line Transient

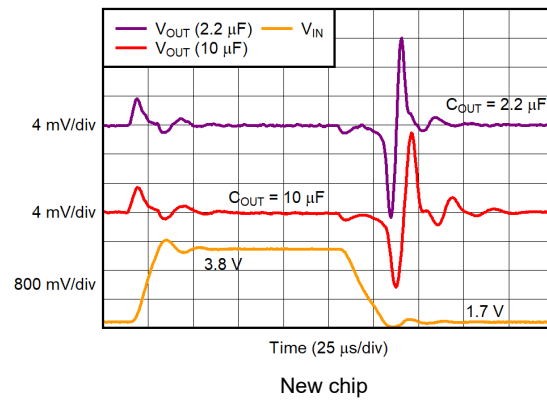


Figure 5-36.  $V_{IN}$  Line Transient

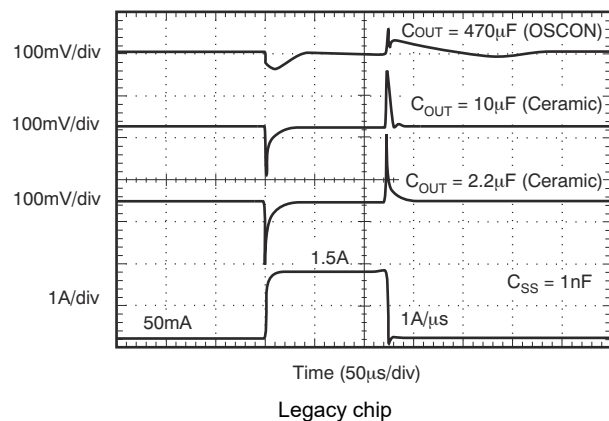


Figure 5-37. Output Load Transient Response

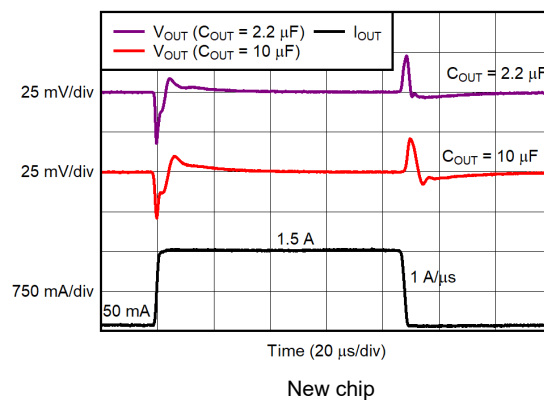


Figure 5-38. Output Load Transient Response

## 5.7 Typical Characteristics: $I_{OUT} = 1\text{ A}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ ,  $V_{EN} = V_{IN} = 1.8\text{ V}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

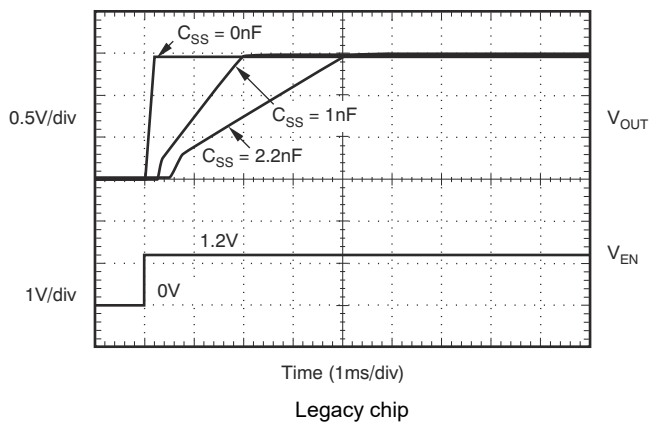


Figure 5-39. Turn-On Response

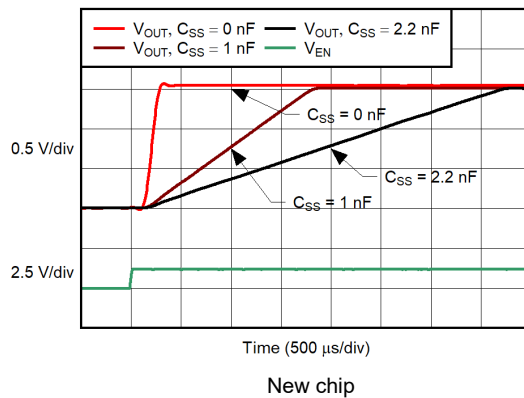


Figure 5-40. Turn-On Response

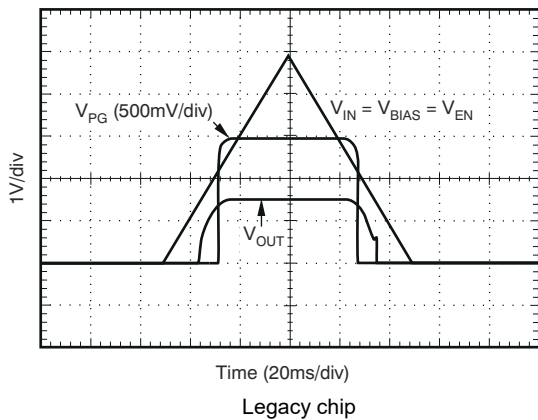


Figure 5-41. Power-Up, Power-Down

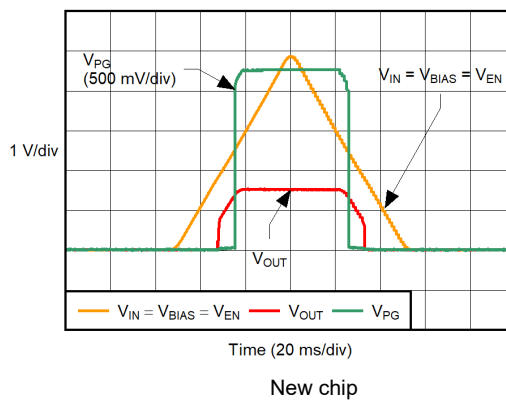


Figure 5-42. Power-Up, Power-Down

## 6 Detailed Description

### 6.1 Overview

The TPS748 is a low-dropout regulator that features soft-start capability. This regulator uses a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS748 to be stable with any capacitor type of value 2.2  $\mu\text{F}$  or greater. Transient response is also superior to PMOS topologies, particularly for low  $V_{\text{IN}}$  applications.

The TPS748 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low  $V_{\text{IN}}$  and  $V_{\text{OUT}}$  capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

### 6.2 Functional Block Diagrams

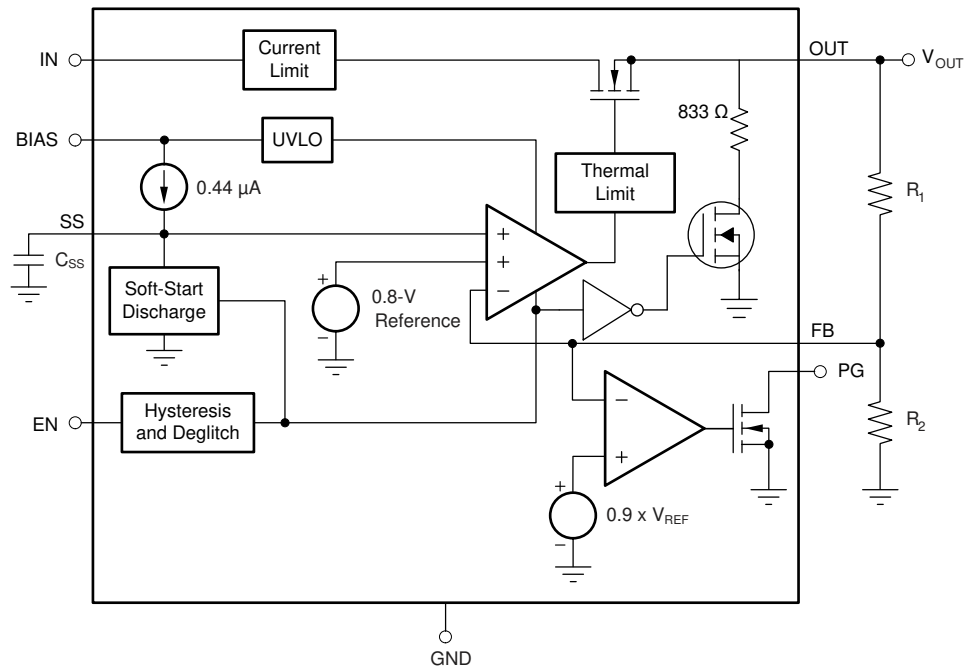
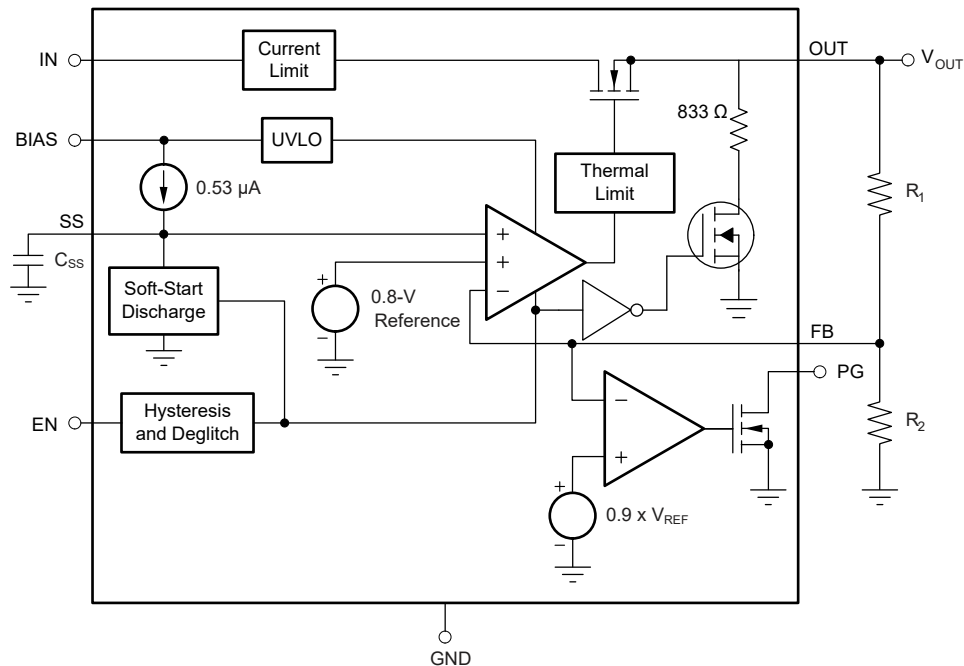


図 6-1. Legacy Chip Functional Block Diagram





**6-2. New Chip Functional Block Diagram**

## 6.3 Feature Description

### 6.3.1 Enable/Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels.  $V_{EN}$  below 0.4 V turns the regulator off, while  $V_{EN}$  above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS748 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the  $V_{EN}$  signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately  $-1$  mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS748.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, connect this pin as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

The TPS748 has an internal active pulldown circuit that connects the output to GND through an 833-Ω resistor when the device is disabled. This resistor discharges the output with a time constant of:

$$\tau = \left( \frac{833 \times R_L}{833 + R_L} \right) \times C_{OUT} \quad (1)$$

### 6.3.2 Power Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on  $V_{BIAS}$  in order to have a valid output. The PG output is high-impedance when  $V_{OUT}$  is greater than  $V_{IT} + V_{HYS}$ . If  $V_{OUT}$  drops below  $V_{IT}$  or if  $V_{BIAS}$  drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 kΩ to 1 MΩ. If output voltage monitoring is not needed, the PG pin can be left floating.

### 6.3.3 Internal Current Limit

The TPS748 features a factory-trimmed current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 2 A and maintain regulation. The current limit responds in approximately 10  $\mu$ s to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS748 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS748 above the rated current degrades device reliability.

### 6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heat sinking. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS748 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS748 into thermal shutdown degrades device reliability.

## 6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation.

**表 6-1. Device Functional Mode Comparison**

OPERATING MODE	PARAMETER				
	$V_{IN}$	$V_{EN}$	$V_{BIAS}$	$I_{OUT}$	$T_J$
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geq V_{OUT} + 1.6 \text{ V}$	$I_{OUT} < I_{CL}$	$T_J < 125^\circ\text{C}$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + 1.6 \text{ V}$	—	$T_J < 125^\circ\text{C}$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 165^\circ\text{C}$

### 6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass transistor is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

### 6.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

## 6.5 Programming

### 6.5.1 Programmable Soft-Start

The TPS74801 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ( $C_{SS}$ ). This feature is important for many applications because soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74801 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current ( $I_{SS}$ ), soft-start capacitance ( $C_{SS}$ ), and the internal reference voltage ( $V_{REF}$ ), and can be calculated using 式 2:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (2)$$

If large output capacitors are used, the device current limit ( $I_{CL}$ ) and the output capacitor can set the start-up time. In this case, the start-up time is given by 式 3:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \quad (3)$$

where:

- $V_{OUT(nom)}$  is the nominal output voltage
- $C_{OUT}$  is the output capacitance
- $I_{CL(min)}$  is the minimum current limit for the device

In applications where monotonic start up is required, the soft-start time given by 式 2 must be set greater than 式 3.

The maximum recommended soft-start capacitor is 15 nF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit can possibly be unable to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 15 nF can be a problem in applications where the enable pin must be rapidly pulsed and with the device still required to soft-start from ground.  $C_{SS}$  must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See 表 6-2 for suggested soft-start capacitor values.

**表 6-2. Standard Capacitor Values for Programming the Soft-Start Time**

$C_{SS}$	SOFT-START TIME <sup>(1)</sup> (Legacy Chip)	SOFT-START TIME <sup>(1)</sup> (New Chip)
Open	0.1 ms	0.25ms
270 pF	0.5 ms	0.4ms
560 pF	1 ms	0.8ms
2.7 nF	5 ms	4.1ms
5.6 nF	10 ms	8.5ms
10 nF	18 ms	15ms

(1)  $t_{SS}(s) = 0.8 \times C_{SS}(F) / I_{SS}$ , where  $t_{SS}(s)$  = soft-start time in seconds.

Another option to set the start-up rate is to use a feedforward capacitor; see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note](#) for more information.

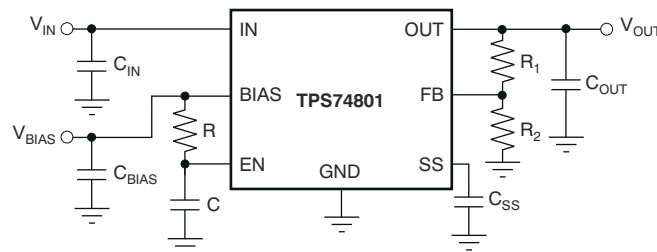
### 6.5.2 Sequencing Requirements

$V_{IN}$ ,  $V_{BIAS}$ , and  $V_{EN}$  can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as  $V_{IN}$  is greater than 1.1 V and the ramp rate of  $V_{IN}$  and  $V_{BIAS}$  is faster than the set soft-start ramp rate.

There are several different start-up responses that are possible, but not typical:

- If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until reaching the set output voltage
- If EN is connected to BIAS, the device soft-starts as programmed, provided that  $V_{IN}$  is present before  $V_{BIAS}$
- If  $V_{BIAS}$  and  $V_{EN}$  are present before  $V_{IN}$  is applied and the set soft-start time has expired, then  $V_{OUT}$  tracks  $V_{IN}$
- If the soft-start time has not expired, the output tracks  $V_{IN}$  until  $V_{OUT}$  reaches the value set by the charging soft-start capacitor

Figure 6-3 shows the use of an RC-delay circuit to hold off  $V_{EN}$  until  $V_{BIAS}$  has ramped. This technique can also be used to drive EN from  $V_{IN}$ . An external control signal can also be used to enable the device after  $V_{IN}$  and  $V_{BIAS}$  are present.



**Figure 6-3. Soft-Start Delay Using an RC Circuit to Enable the Device**

## 7 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 7.1 Application Information

The TPS748 is a low-dropout regulator that features soft-start capability. This regulator uses a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS748 to be stable with any capacitor type of value 2.2  $\mu\text{F}$  or greater. Transient response is also superior to PMOS topologies, particularly for low  $V_{\text{IN}}$  applications.

The TPS748 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low  $V_{\text{IN}}$  and  $V_{\text{OUT}}$  capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

#### 7.1.1 Adjusting the Output Voltage

図 7-1 shows the typical application circuit for the TPS748 adjustable output device.

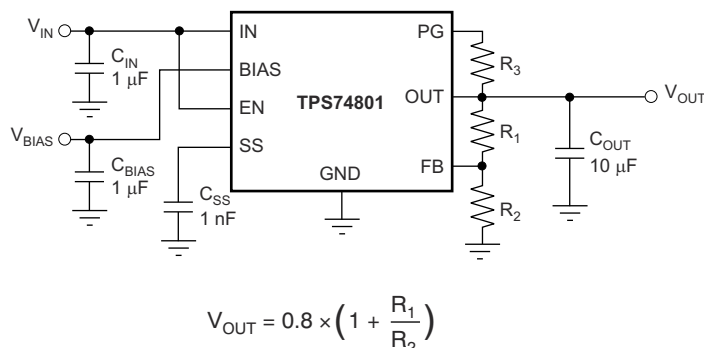


図 7-1. Typical Application Circuit for the TPS748 (Adjustable)

$R_1$  and  $R_2$  can be calculated for any output voltage using the formula shown in 図 7-1. 表 7-1 lists sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications,  $R_2$  must be  $\leq 4.99 \text{ k}\Omega$ .

**表 7-1. Standard 1% Resistor Values for Programming the Output Voltage<sup>(1)</sup>**

$R_1$ (k $\Omega$ )	$R_2$ (k $\Omega$ )	$V_{OUT}$ (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1)  $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$ .

#### 注

When  $V_{BIAS}$  and  $V_{EN}$  are present and  $V_{IN}$  is not supplied, this device outputs approximately 50  $\mu\text{A}$  of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 k $\Omega$ .

### 7.1.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors  $\geq 2.2 \mu\text{F}$ . The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for  $V_{IN}$  is 1  $\mu\text{F}$  and minimum recommended capacitor for  $V_{BIAS}$  is 0.1  $\mu\text{F}$ . If  $V_{IN}$  and  $V_{BIAS}$  are connected to the same supply, the recommended minimum capacitor for  $V_{BIAS}$  is 4.7  $\mu\text{F}$ . Use good-quality, low-ESR capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close to the pins as possible for optimum performance.

### 7.1.3 Transient Response

The TPS748 was designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance does. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see 図 5-37 in the *Typical Characteristics* section. Because the TPS748 is stable with output capacitors as low as 2.2  $\mu\text{F}$ , many applications can then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

### 7.1.4 Dropout Voltage

The TPS748 offers very low dropout performance, making the device designed for high-current, low  $V_{IN}$ , low  $V_{OUT}$  applications. The low dropout of the TPS748 allows the device to be used in place of a dc/dc converter and still achieve good efficiency. 式 4 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times (I_{IN} + I_Q)} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} \gg I_Q \quad (4)$$

This efficiency provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solutions.

There are two different specifications for dropout voltage with the TPS748. The first specification (see 図 7-2) is referred to as  $V_{IN}$  dropout and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that  $V_{BIAS}$  is at least 3.25 V<sup>1</sup> above  $V_{OUT}$ , which is the case for  $V_{BIAS}$  when powered by a 5.0-V rail with 5% tolerance and with  $V_{OUT} = 1.5$  V. If  $V_{BIAS}$  is higher than  $V_{OUT} + 3.25$  V<sup>1</sup>,  $V_{IN}$  dropout is less than specified.<sup>1</sup>

The second specification (illustrated in 図 7-8) is referred to as  $V_{BIAS}$  dropout and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because  $V_{BIAS}$  provides the gate drive to the pass transistor; therefore,  $V_{BIAS}$  must be 1.6 V above  $V_{OUT}$ . Because of this usage, IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the device package.

### 7.1.5 Output Noise

The TPS748 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 1-nF soft-start capacitor, the output noise is reduced by half and is typically 30  $\mu V_{RMS}$  for a 1.2-V output (10 Hz to 100 kHz). Further increasing  $C_{SS}$  has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 1-nF soft-start capacitor is given in 式 5:

$$V_N(\mu V_{RMS}) = 25 \left( \frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (5)$$

The low output noise of the TPS748 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

<sup>1</sup> 3.25 V is a test condition of this device and can be adjusted by referring to 図 5-11.



## 7.2 Typical Applications

### 7.2.1 FPGA I/O Supply at 1.5 V With a Bias Rail

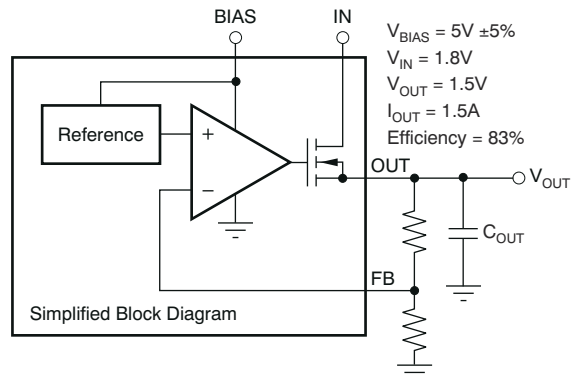


Figure 7-2. Typical Application of the TPS748 Using an Auxiliary Bias Rail

#### 7.2.1.1 Design Requirements

This application powers the I/O rails of an FPGA, at  $V_{OUT(nom)} = 1.5\text{ V}$  and  $I_{OUT(dc)} = 1.5\text{ A}$ . The available external supply voltages are 1.8 V, 3.3 V, and 5 V.

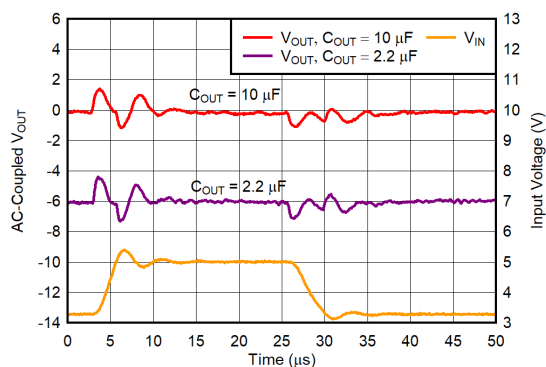
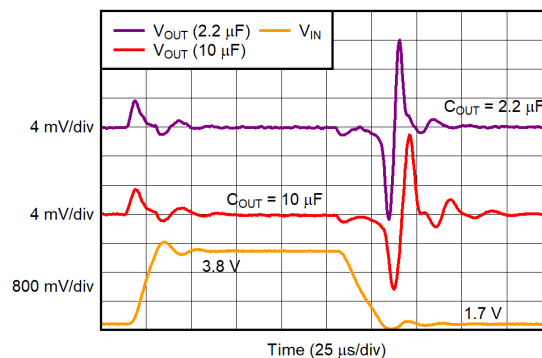
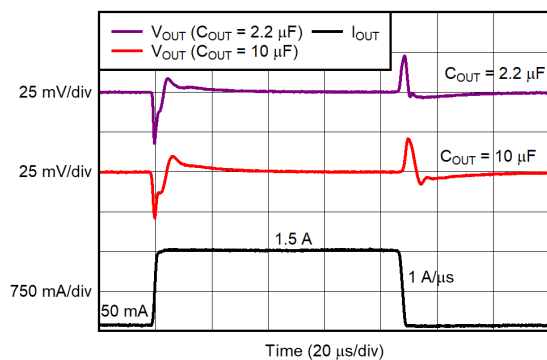
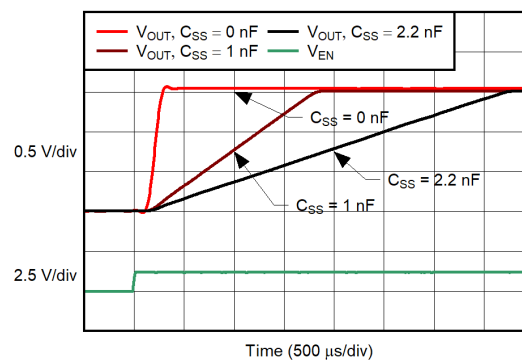
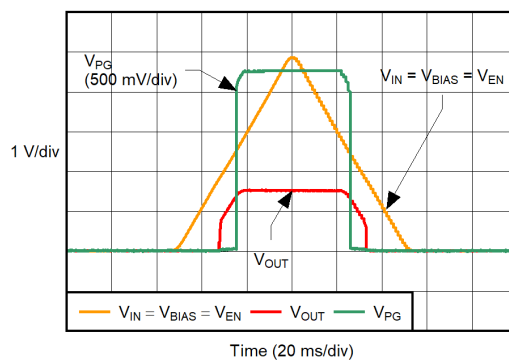
#### 7.2.1.2 Detailed Design Procedure

First, determine what supplies to use for the input and bias rails. A 1.8-V input can be stepped down to 1.5 V at 1.5 A if an external bias is provided, because the maximum dropout voltage is 165 mV if  $V_{BIAS}$  is at least 3.25 V higher than  $V_{OUT}$ . To achieve this voltage step, the bias rail is supplied by the 5-V supply. The approximation in Equation 4 estimates the efficiency at 83.3%.

The output voltage then must be set to 1.5 V. As Table 7-1 describes, set  $R_1 = 4.12\text{ k}\Omega$  and  $R_2 = 4.75\text{ k}\Omega$  to obtain the required output voltage. The minimum capacitor sizing is desired to reduce the total solution size footprint; see the [Input, Output, and Bias Capacitor Requirements](#) section for  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 1\text{ }\mu\text{F}$ , and  $C_{OUT} = 2.2\text{ }\mu\text{F}$ . Use  $C_{SS} = 1\text{ nF}$  for a typical 1.8-ms start-up time.

Figure 7-2 shows a simplified version of the final circuit.

## 7.2.1.3 Application Curves


 7-3.  $V_{BIAS}$  Line Transient

 7-4.  $V_{IN}$  Line Transient

 7-5. Output Load Transient Response

 7-6. Turn-On Response

 7-7. Power-Up, Power-Down

## 7.2.2 FPGA I/O Supply at 1.5 V Without a Bias Rail

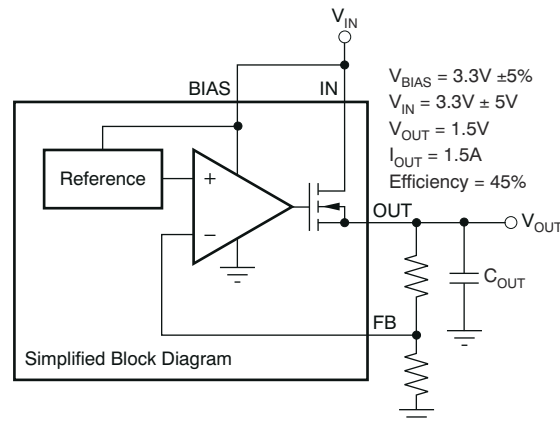


図 7-8. Typical Application of the TPS748 Without an Auxiliary Bias Rail

### 7.2.2.1 Design Requirements

The application powers the I/O rails of an FPGA, at  $V_{\text{OUT(nom)}} = 1.5\text{ V}$  and  $I_{\text{OUT(max)}} = 1.5\text{ A}$ . The only available rail is 3.3 V. The I/O pins are driven for only short durations with a 5% duty cycle, so thermal issues are not a concern.

### 7.2.2.2 Detailed Design Procedure

There is only one available rail; therefore, the input supply and the bias supply are connected together on the 3.3-V input supply.

The output voltage must be set to 1.5 V. As 表 7-1 describes, set  $R_1 = 4.12\text{ k}\Omega$  and  $R_2 = 4.75\text{ k}\Omega$  to obtain the required output voltage. The minimum capacitor sizing is desired to reduce the total solution size footprint; see the [Input, Output, and Bias Capacitor Requirements](#) section for  $C_{\text{IN}} = C_{\text{BIAS}} = 4.7\text{ }\mu\text{F}$ , and  $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$ . Use  $C_{\text{SS}} = 1\text{ nF}$  for a typical 1.8-ms start-up time.

図 7-8 shows the TPS748 configured without a bias rail.

### 7.2.2.3 Application Curves

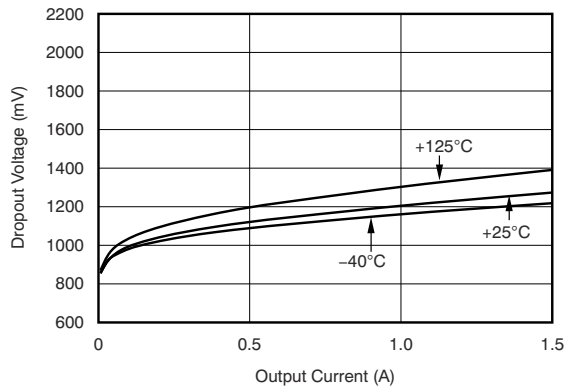


図 7-9.  $V_{BIAS}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

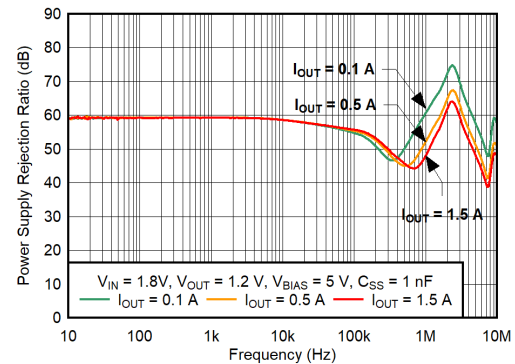


図 7-10.  $V_{BIAS}$  PSRR vs Frequency

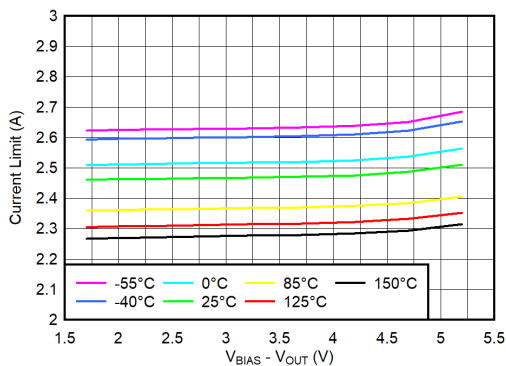


図 7-11. Current Limit vs ( $V_{BIAS} - V_{OUT}$ )

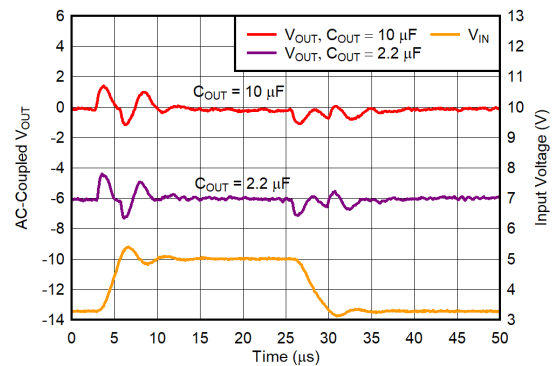


図 7-12.  $V_{BIAS}$  Line Transient

## 7.3 Power Supply Recommendations

The TPS748 is designed to operate from an input voltage up to 5.5 V, provided the bias rail is at least 1.62 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin of the TPS748. This supply must have at least 1  $\mu$ F of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1- $\mu$ F or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7  $\mu$ F of capacitance is needed for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

## 7.4 Layout

### 7.4.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of  $R_1$  in 図 7-1 must be connected as close as possible to the load. If BIAS is connected to IN, connect

BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using 式 6:

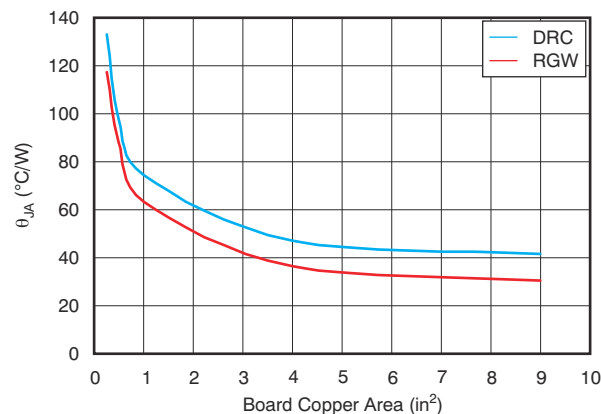
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both the VSON (DRC) and VQFN (RGW) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, the pad be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using 式 7:

$$R_{\theta JA} = \frac{(+125^{\circ}\text{C} - T_A)}{P_D} \quad (7)$$

Knowing the maximum  $R_{\theta JA}$ , the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using 図 7-13.



$R_{\theta JA}$  value at board size of 9 in<sup>2</sup> (that is, 3 in × 3 in) is a JEDEC standard.

**図 7-13.  $R_{\theta JA}$  vs Board Size**

図 7-13 shows the variation of  $R_{\theta JA}$  as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not intended to be used to estimate actual thermal performance in real application environments.

注

When the device is mounted on an application PCB, TI strongly recommends using  $\Psi_{JT}$  and  $\Psi_{JB}$ , as explained in the [Estimating Junction Temperature](#) section.

#### 7.4.1.1 Estimating Junction Temperature

Using the thermal metrics  $\Psi_{JT}$  and  $\Psi_{JB}$ , as shown in the [Thermal Information](#) table, the junction temperature can be estimated with corresponding formulas (given in [式 8](#)). For backwards compatibility, an older  $\theta_{JC, Top}$  parameter is listed as well.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

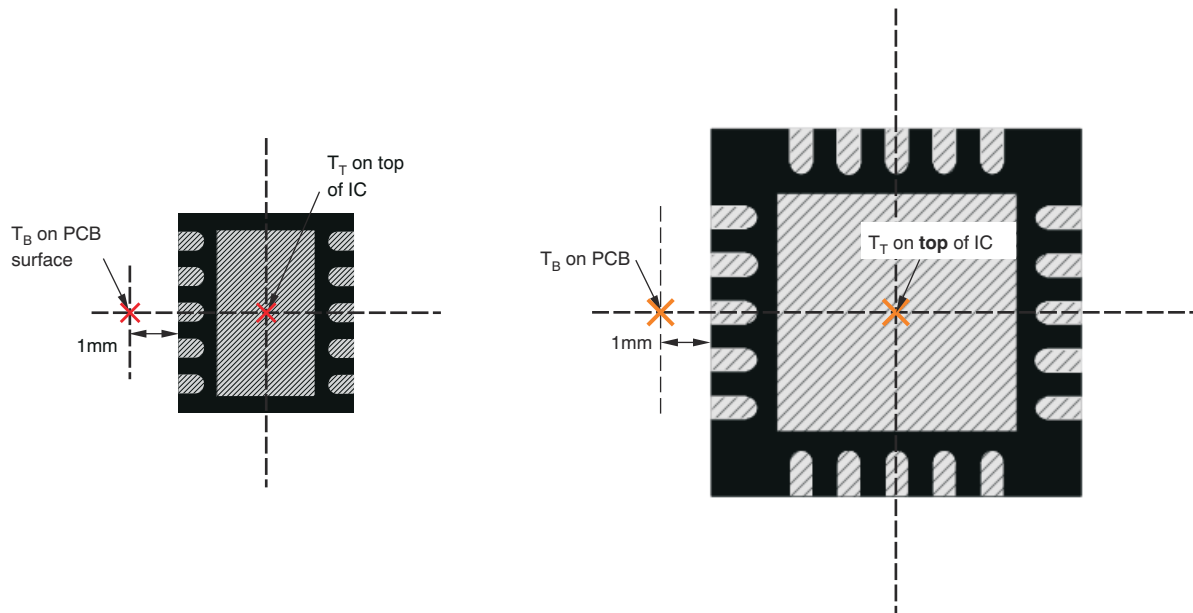
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D \quad (8)$$

Where  $P_D$  is the power dissipation shown by [式 6](#),  $T_T$  is the temperature at the center-top of the device package, and  $T_B$  is the PCB temperature measured 1 mm away from the device package *on the PCB surface* ([図 7-14](#)).

注

Both  $T_T$  and  $T_B$  can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring  $T_T$  and  $T_B$ , see the [Using New Thermal Metrics](#) application note, available for download at [www.ti.com](http://www.ti.com).

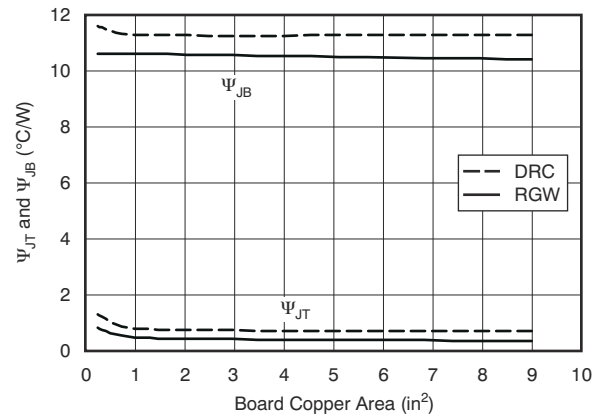


(a) Example DRC (SON) Package Measurement

(b) Example RGW (QFN) Package Measurement

**図 7-14. Measuring Points for  $T_T$  and  $T_B$**

By looking at 図 7-15, the new thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) have very little dependency on board size. That is, using  $\Psi_{JT}$  or  $\Psi_{JB}$  with 式 8 is a good way to estimate  $T_J$  by simply measuring  $T_T$  or  $T_B$ , regardless of the application board size.



**図 7-15.  $\Psi_{JT}$  and  $\Psi_{JB}$  vs Board Size**

For a more detailed discussion of why TI does not recommend using  $\theta_{JC(top)}$  to determine thermal characteristics, see the [Using New Thermal Metrics application note](#), available for download at [www.ti.com](http://www.ti.com). For further information, see the [IC Package Thermal Metrics application note](#), also available on the TI website.

### 7.4.2 Layout Example

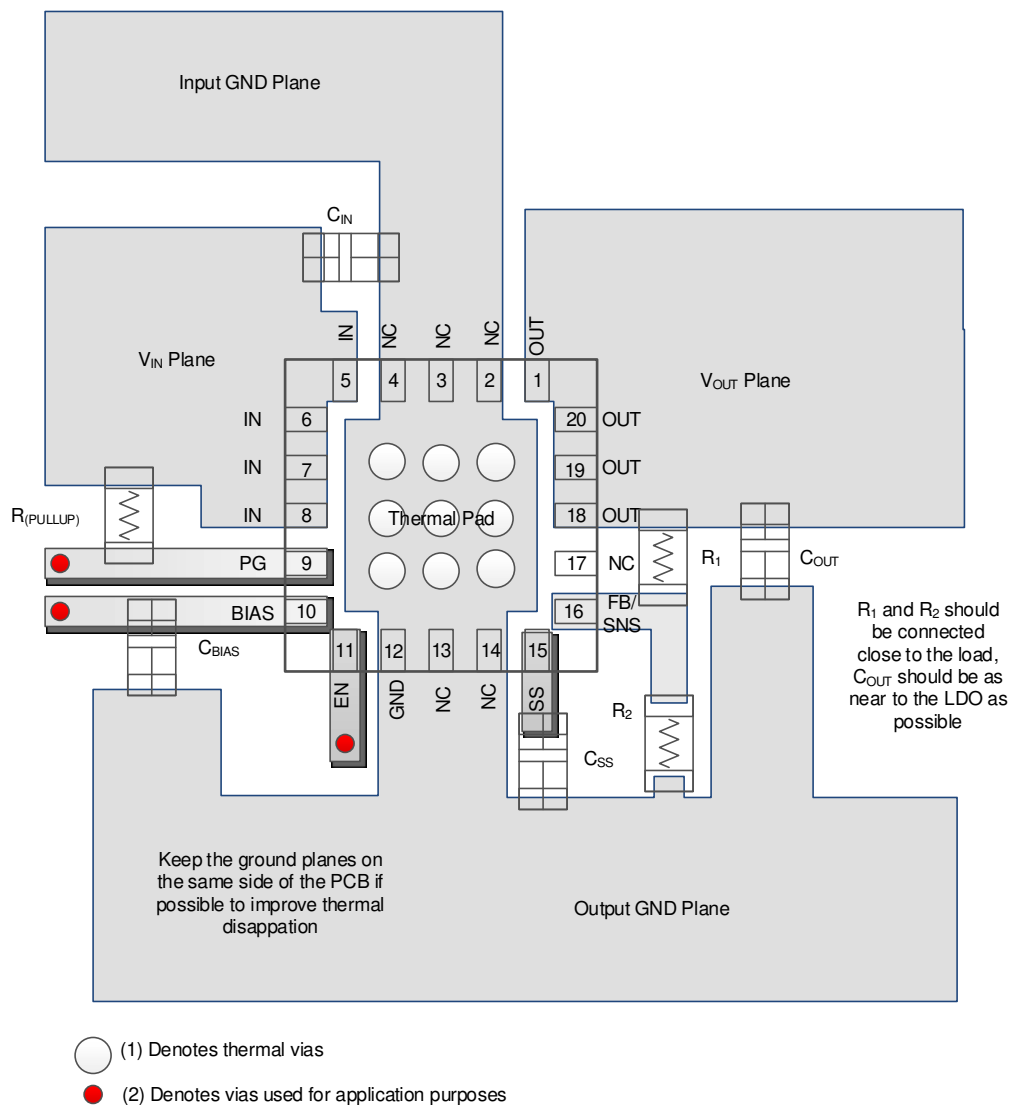


図 7-16. Layout Example (RGW Package)



## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Device Nomenclature

**表 8-1. Device Nomenclature**

PRODUCT <sup>(1)</sup>	V <sub>OUT</sub>
TPS74801yyyzM3	<p><b>yyy</b> is the package designator.  <b>z</b> is the package quantity.  <b>M3</b> is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. The device performance for new and legacy chips is denoted throughout the document.</p>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).

#### 8.1.2 Development Support

##### 8.1.2.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS48. The [TPS74801EVM-177 evaluation module](#) (and related [user's guide](#)) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#).

##### 8.1.2.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS748 is available through the product folders under *Tools & Software*.

## 8.2 Documentation Support

### 8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Using New Thermal Metrics application note](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application note](#)
- Texas Instruments, [Ultimate Regulation with Fixed Output Versions of TPS742xx, TPS743xx, and TPS744xx application note](#)
- Texas Instruments, [Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator application note](#)
- Texas Instruments, [TPS74701EVM-177 and TPS74801EVM-177 user's guide](#)

## 8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 8.4 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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## 8.5 Trademarks

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## 8.6 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 8.7 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (April 2023) to Revision N (June 2024)	Page
• M3 への参照を新しいチップに変更 .....	1
• 「概要」セクションの精度 2% を精度 1% (新チップ) に変更 .....	1
• Added new chip plots to <i>Typical Characteristics</i> sections.....	8
• Added <i>New Chip Functional Block Diagram</i> to <i>Functional Block Diagrams</i> section.....	16
• Changed <i>Standard Capacitor Values for Programming the Soft-Start Time</i> table: corrected equation in footnote and added <i>soft-start time</i> column for new chip.....	20
• Changed both <i>Application Curves</i> sections in <i>Typical Applications</i> to use new chip curves.....	26
• Added <i>Device Nomenclature</i> section.....	33

Changes from Revision L (March 2017) to Revision M (April 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新 .....	1
• ドキュメント全体を通して QFN を VQFN に変更.....	1
• M3 デバイスをドキュメントに追加し、M3 固有の「電気的特性」表と「代表的特性」セクションを追加 .....	1
• 「アプリケーション」セクションにリンクを追加 .....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS74801DRCR</a>	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCRG4	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
<a href="#">TPS74801DRCRM3</a>	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCRM3.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
<a href="#">TPS74801DRCT</a>	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCTG4	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
<a href="#">TPS74801RGWR</a>	Active	Production	VQFN (RGW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWR.A	Active	Production	VQFN (RGW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWRG4	Active	Production	VQFN (RGW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
<a href="#">TPS74801RGWRM3</a>	Active	Production	VQFN (RGW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWRM3.A	Active	Production	VQFN (RGW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
<a href="#">TPS74801RGWT</a>	Active	Production	VQFN (RGW)   20	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWT.A	Active	Production	VQFN (RGW)   20	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWTG4	Active	Production	VQFN (RGW)   20	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPS74801 :**

- Automotive : [TPS74801-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74801DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801DRCRM3	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74801RGWRM3	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74801RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74801DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74801DRCRM3	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74801DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS74801RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801RGWRM3	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**RGW 20**

**VQFN - 1 mm max height**

5 x 5, 0.65 mm pitch

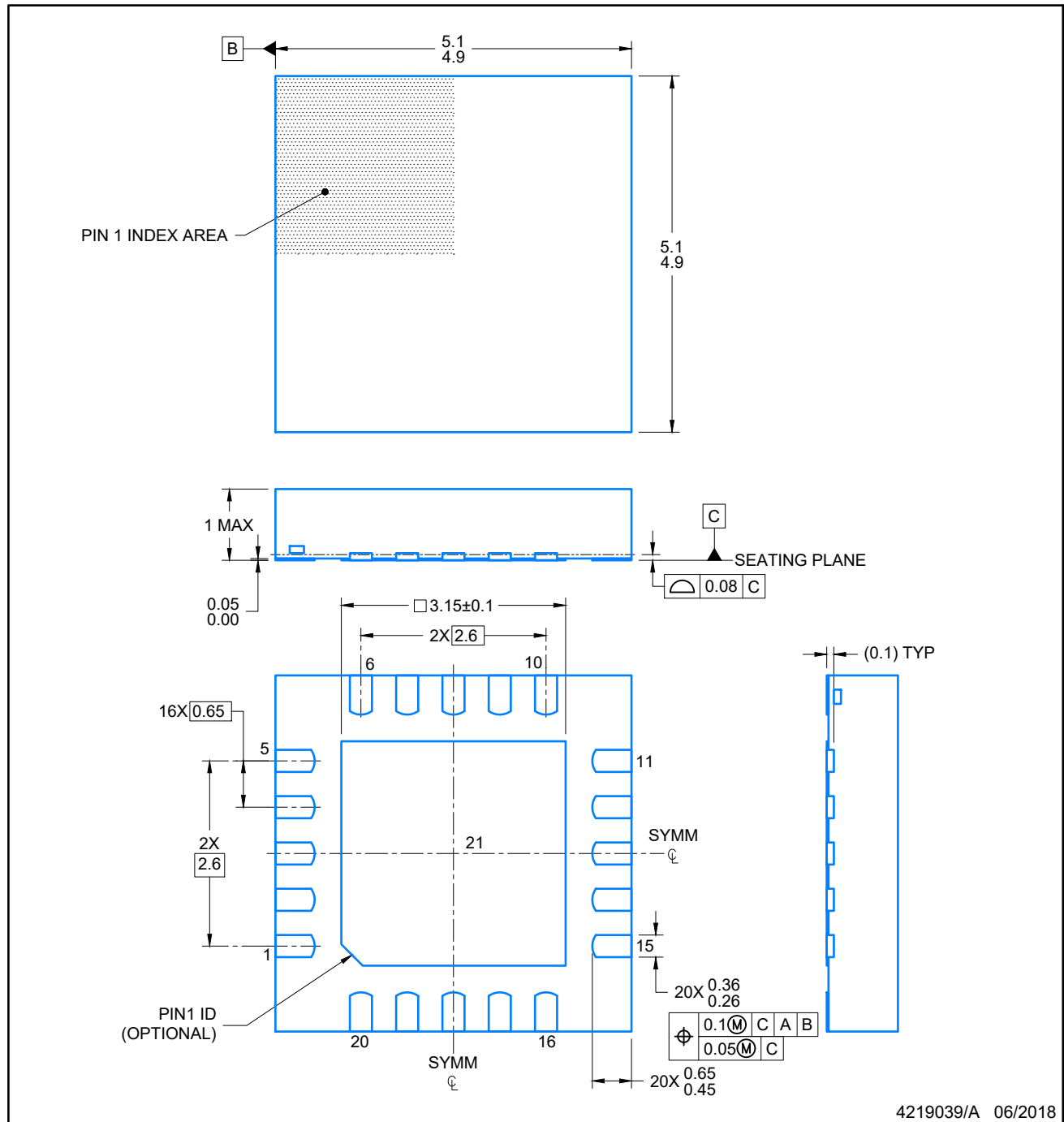
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



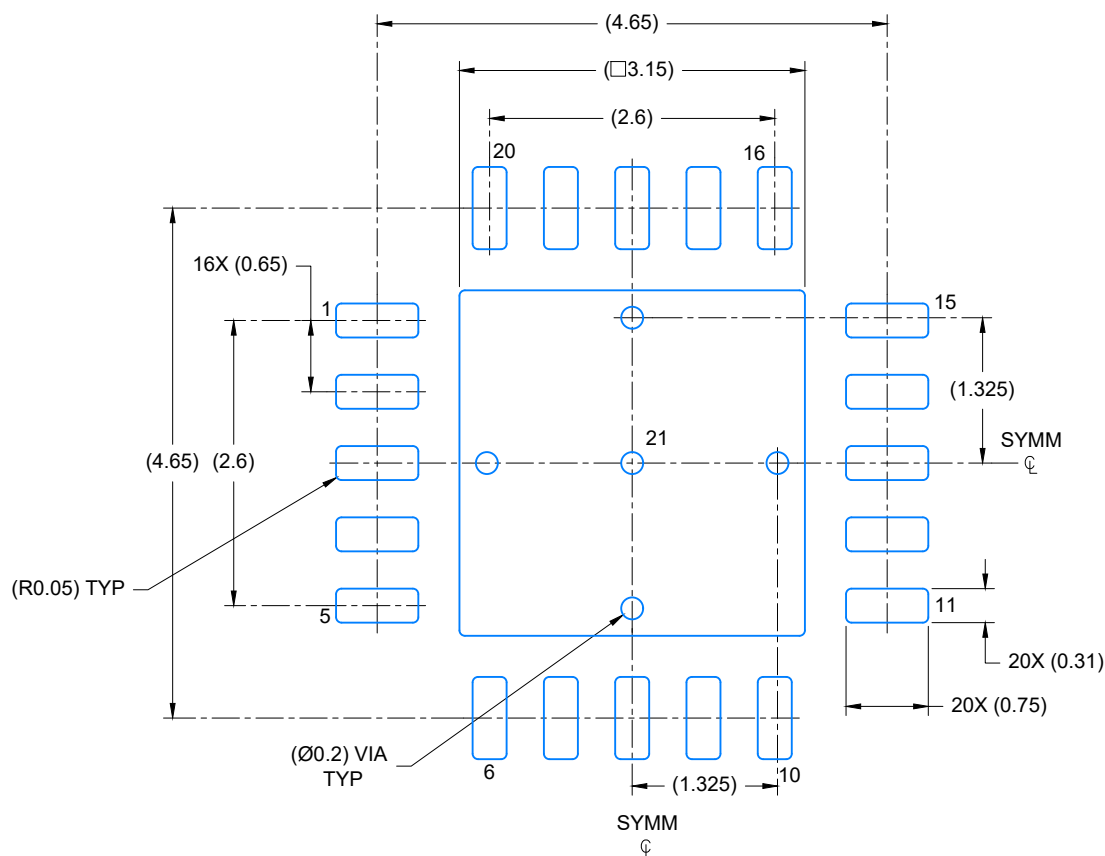
4227157/A





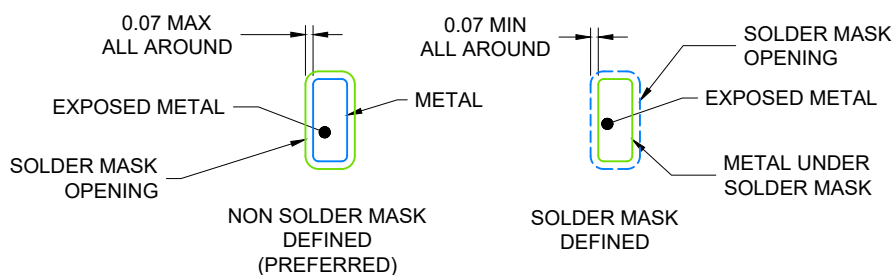
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



## LAND PATTERN EXAMPLE

SCALE: 15X

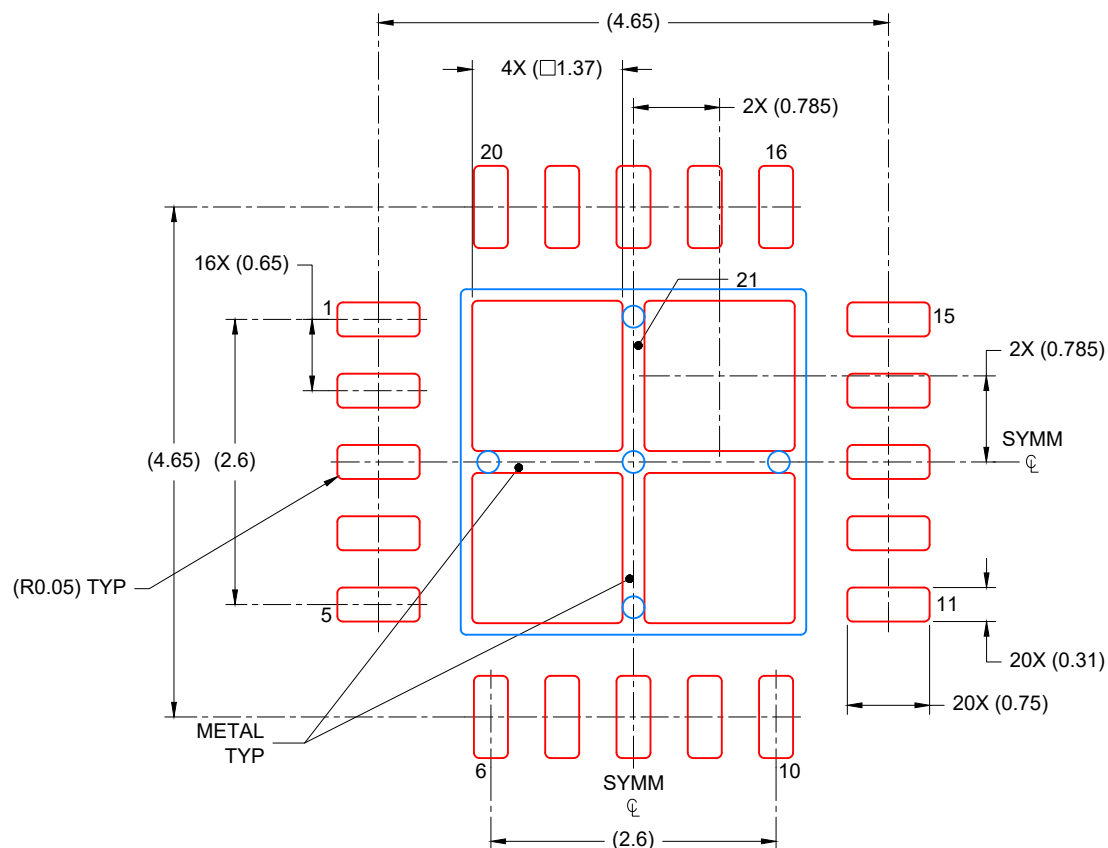


## SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 75% PRINTED COVERAGE BY AREA  
 SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

**DRC 10**

**VSON - 1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226193/A



4218878/B 07/2018

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

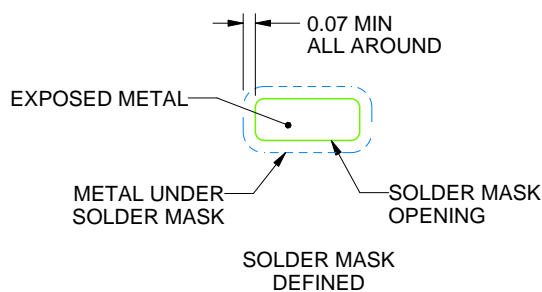
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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