TPS767xxQ Fast-Transient-Response 1-A Low-Dropout Linear Regulators

1 Features

- 1 A Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Down to 230 mV at 1 A (TPS76750)
- Ultralow 85 µA Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power-On Reset With 200-ms Delay (See TPS768xx for PG Option)
- 8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

2 Description

This device is designed to have a fast transient response and be stable with 10 µF low ESR capacitors. This combination provides high performance at a reasonable cost.

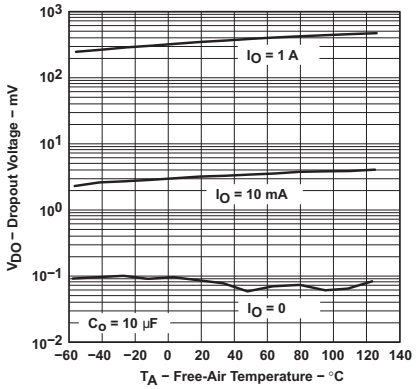
Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76750) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 µA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to 1 µA at T_J = 25°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS767xx	SOIC (8)	4.90 mm × 3.91 mm
	HTSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

TPS76733 Dropout Voltage vs Free-air Temperature



TPS76733 Load Transient Response

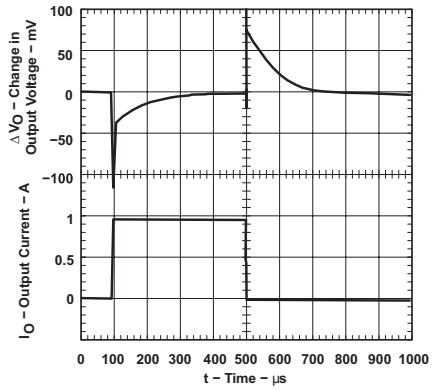


Table of Contents

3 Revision History

Changes from Revision I (January 2004) to Revision J **Page**

- Added *ESD Ratings* table, *Overview* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

4 Description (Continued)

The $\overline{\text{RESET}}$ output of the TPS767xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767xx family is available in 8-pin SOIC and 20-pin PWP packages.

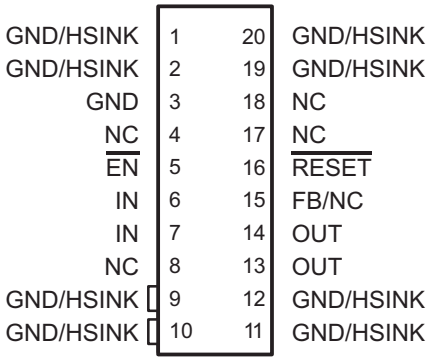
5 Device Options

PART NO. (1)		VOLTAGE OPTIONS (V)
TSSOP (PWP)	SOIC (D)	TYP
TPS76750Q	TPS76750Q	5
TPS76733Q	TPS76733Q	3.3
TPS76730Q	TPS76730Q	3
TPS76728Q	TPS76728Q	2.8
TPS76727Q	TPS76727Q	2.7
TPS76725Q	TPS76725Q	2.5
TPS76718Q	TPS76718Q	1.8
TPS76715Q	TPS76715Q	1.5
TPS76701Q	TPS76701Q	Adjustable 1.5 V to 5.5 V

(1) The TPS76701 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS76701QDR).

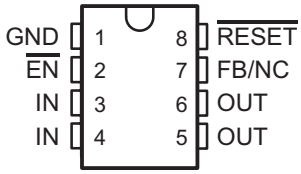
6 Pin Configuration and Functions

PWP Package
20 Pin HTSSOP
Top View



NC − No internal connection

D Package
8 Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SOIC PACKAGE			
$\overline{EN}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
$\overline{RESET}$	8	O	RESET output
HTSSOP PACKAGE			
$\overline{EN}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
$\overline{RESET}$	16	O	RESET output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Input voltage range (2)	–0.3	13.5	V
	Voltage range at EN	–0.3	V_I + 0.3	V
	Maximum $\overline{\text{RESET}}$ voltage		16.5	
	Peak output current	Internally limited		
V_O	Output voltage (OUT, FB)		7	V
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature range	–40	125	°C
T_{stg}	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I (1)	Input voltage	2.7	10	V
V_O	Output voltage range	1.2	5.5	V
I_O (2)	Output current	0	1.0	A
T_J (2)	Operating junction temperature	–40	125	°C

(1) Maximum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V, whichever is greater.
(2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

7.4 Thermal Information

THERMAL METRIC (1)		TPS767xxQ		UNIT
		PWP (HTSSOP) (20 PINS)	D (SOIC) (8 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.8	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	52.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	47.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	9.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	47.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

$V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_o = 10$ µF (over recommended operating free-air temperature range, unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (10 µA to 1 A load)	TPS76701	1.5 V ≤ V_O ≤ 5.5 V,	T_J = 25°C		V_O		V
		1.5 V ≤ V_O ≤ 5.5 V,	T_J = −40°C to 125°C	0.98V_O		1.02V_O	
	TPS76715	T_J = 25°C,	2.7 V < V_{IN} < 10 V		1.5		V
		T_J = −40°C to 125°C,	2.7 V < V_{IN} < 10 V	1.470		1.530	
	TPS76718	T_J = 25°C,	2.8 V < V_{IN} < 10 V		1.8		V
		T_J = −40°C to 125°C,	2.8 V < V_{IN} < 10 V	1.7646		1.836	
	TPS76725	T_J = 25°C,	3.5 V < V_{IN} < 10 V		2.5		V
		T_J = −40°C to 125°C,	3.5 V < V_{IN} < 10 V	2.450		2.550	
	TPS76727	T_J = 25°C,	3.7 V < V_{IN} < 10 V		2.7		V
		T_J = −40°C to 125°C,	3.7 V < V_{IN} < 10 V	2.646		2.754	
	TPS76728	T_J = 25°C,	3.8 V < V_{IN} < 10 V		2.8		V
		T_J = −40°C to 125°C,	3.8 V < V_{IN} < 10 V	2.7446		2.856	
	TPS76730	T_J = 25°C,	4.0 V < V_{IN} < 10 V		3		V
		T_J = −40°C to 125°C,	4.0 V < V_{IN} < 10 V	2.9400		3.060	
	TPS76733	T_J = 25°C,	4.3 V < V_{IN} < 10 V		3.3		
		T_J = −40°C to 125°C,	4.3 V < V_{IN} < 10 V	3.2346		3.366	
	TPS76750	T_J = 25°C,	6.0 V < V_{IN} < 10 V		5		
		T_J = −40°C to 125°C,	6.0 V < V_{IN} < 10 V	4.900		5.100	
Quiescent current (GND current) $\overline{EN}$ = 0V		10 µA < I_O < 1 A,	T_J = 25°C		85		µA
		I_O = 1 A,	T_J = −40°C to 125°C			125	
Output voltage line regulation (ΔVO/VO)		V_O + 1 V < VI ≤ 10 V,	T_J = 25°C		0.01		%/V
Load regulation					3		mV
Output noise voltage	TPS76718	BW = 200 Hz to 100 kHz, C_o = 10 µF,	I_C = 1 A, T_J = 25°C		55		µVrms
Output current limit		V_O = 0 V		1.2	1.7	2	A
Thermal shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = VI,	T_J = 25°C, 2.7 V < V_I < 10 V		1		µA
		$\overline{EN}$ = VI,	T_J = −40°C to 125°C, 2.7 V < V_I < 10 V			10	µA
FB input current	TPS76701	FB = 1.5 V			2		nA
High level enable input voltage				1.7			V
Low level enable input voltage						0.9	V
Power supply ripple rejection		f = 1 kHz, C_o = 10 µF,	T_J = 25°C		60		dB
Reset	Minimum input voltage for valid $\overline{RESET}$	$I_{O(RESET)}$ = 300 µA			1.1		
	Trip threshold voltage	V_O decreasing		92		98	
	Hysteresis voltage	Measured at V_O			0.5		
	Output low voltage	V_I = 2.7 V,	$I_{O(RESET)}$ = 1 mA		0.15	0.4	
	Leakage current	$V_{(RESET)}$ = 5 V				1	
	RESET time-out delay				200		
Input current ($\overline{EN}$)		$\overline{EN}$ = 0 V		–1	0	1	µA
		$\overline{EN}$ = VI		–1		1	

Electrical Characteristics (continued)

$V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_o = 10$ µF (over recommended operating free-air temperature range, unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage (1)	TPS76728	I_O = 1 A	T_J = 25°C		500		mV
			T_J = −40°C to 125°C			825	
	TPS76730	I_O = 1 A	T_J = 25°C		450		mV
			T_J = −40°C to 125°C			675	
	TPS76733	I_O = 1 A	T_J = 25°C		350		mV
			T_J = −40°C to 125°C			575	
	TPS76750	I_O = 1 A	T_J = 25°C		230		mV
			T_J = −40°C to 125°C			380	

(1) IN voltage equals V_O(typ) − 100 mV; TPS76701 output voltage set to 3.3 V nominal with external resistor divider. TPS76715, TPS76718, TPS76725, and TPS76727 dropout voltage limited by input voltage range limitations (i.e., TPS76730 input voltage needs to drop to 2.9 V for purpose of this test).

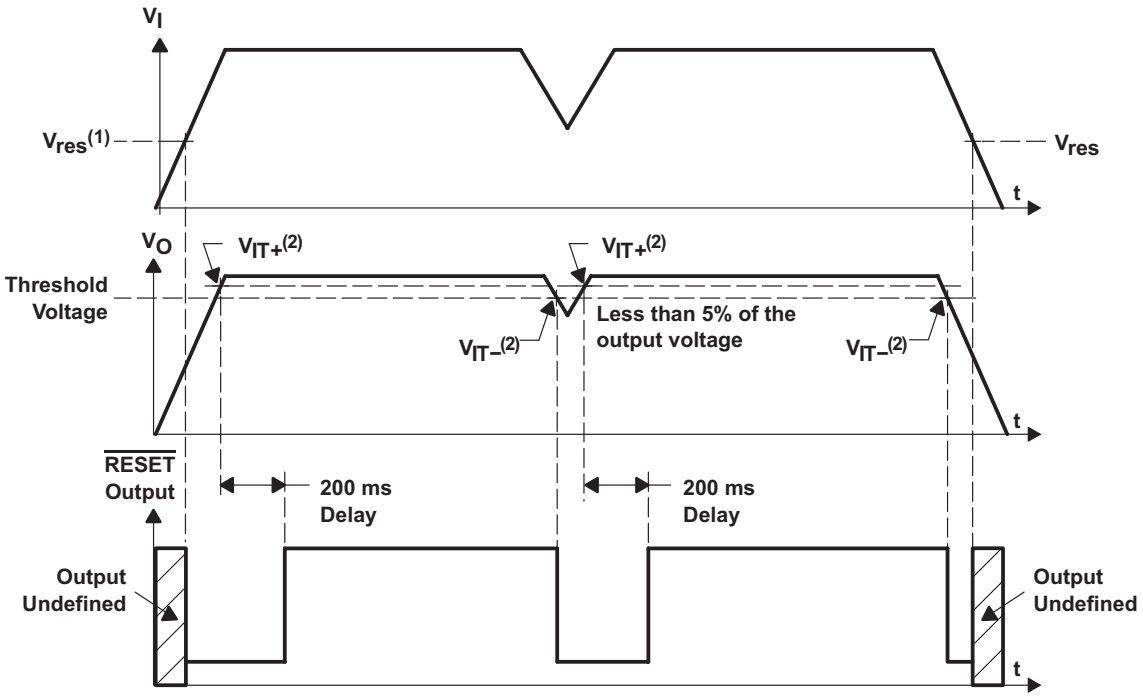


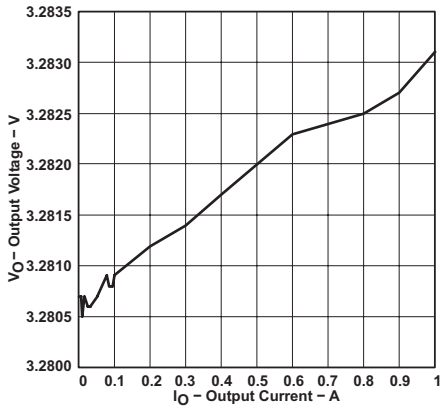
Figure 1. Timing Diagram

7.6 Typical Characteristics

Table 1. Table of Graphs

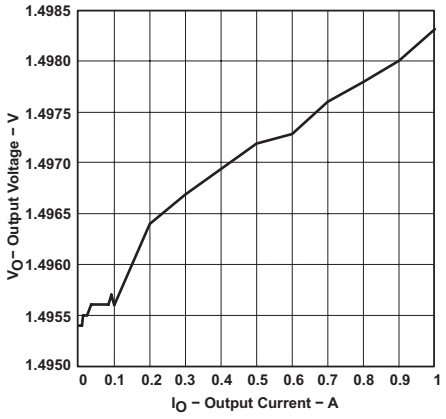
			FIGURE
V_O	Output voltage	vs Output current	Figure 2, Figure 3, Figure 4
		vs Free-air temperature	Figure 5, Figure 6, Figure 7
	Ground current	vs Free-air temperature	Figure 8, Figure 9
	Power supply ripple rejection	vs Frequency	Figure 10
	Output spectral noise density	vs Frequency	Figure 11
	Input voltage (min)	vs Output voltage	Figure 12
Z_o	Output impedance	vs Frequency	Figure 13
V_{DO}	Dropout voltage	vs Free-air temperature	Figure 14
	Line transient response		Figure 15, Figure 16
	Load transient response		Figure 17, Figure 18
V_O	Output voltage	vs Time	Figure 19
	Dropout voltage	vs Input voltage	Figure 20
	Equivalent series resistance (ESR)(1)	vs Output current	Figure 21–Figure 24

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_o.



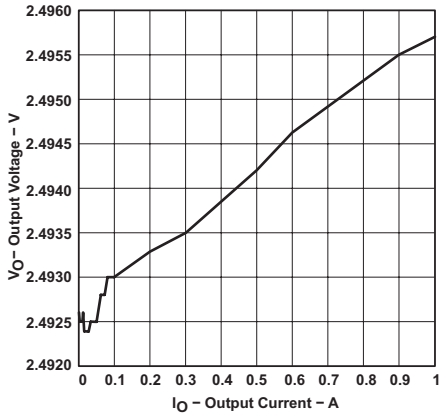
V_I = 4.3 V T_A = 25°C

Figure 2. TPS76733 Output Voltage vs Output Current



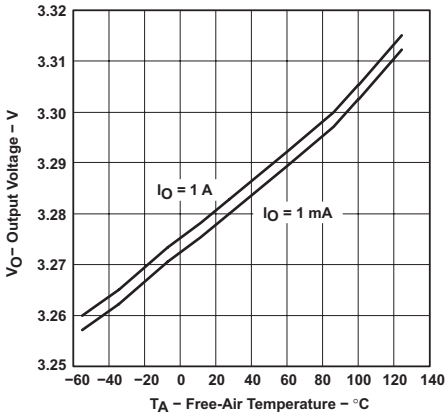
V_I = 2.7 V T_A = 25°C

Figure 3. TPS76715 Output Voltage vs Output Current



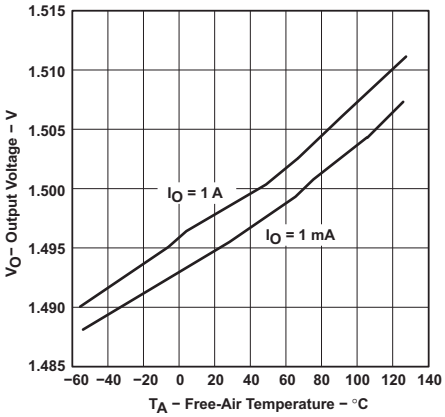
V_I = 3.5 V T_A = 25°C

Figure 4. TPS76725 Output Voltage vs Output Current



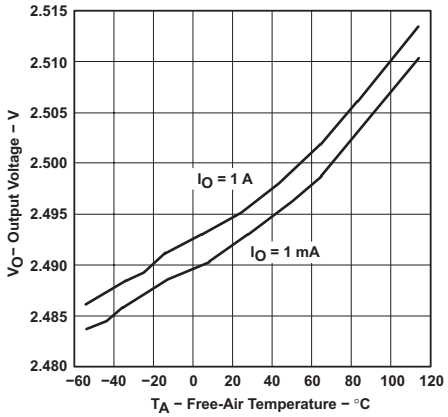
V_I = 4.3 V

Figure 5. TPS76733 Output Voltage vs Free-Air Temperature



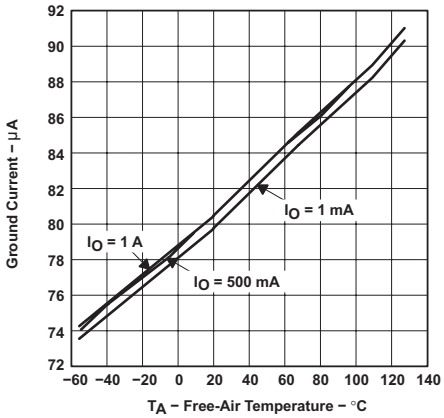
V_I = 2.7 V

Figure 6. TPS76715 Output Voltage vs Free-Air Temperature



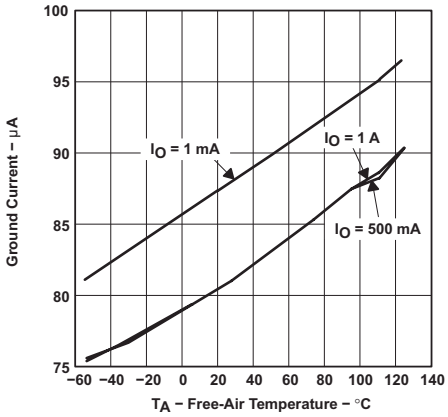
V_I = 3.5 V

Figure 7. TPS767125 Output Voltage vs Free-Air Temperature



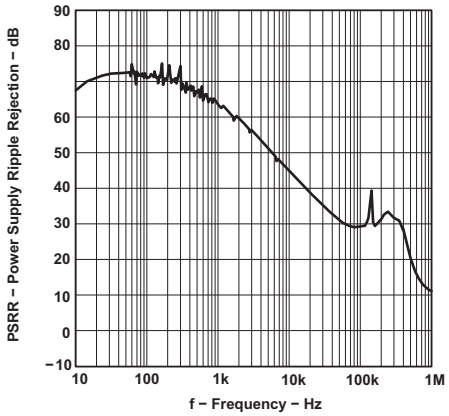
V_I = 4.3 V

Figure 8. TPS76733 Ground Current vs Free-Air Temperature



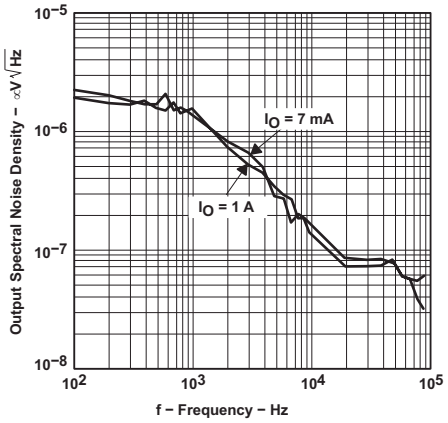
V_I = 2.7 V

Figure 9. TPS76715 Ground Current vs Free-Air Temperature



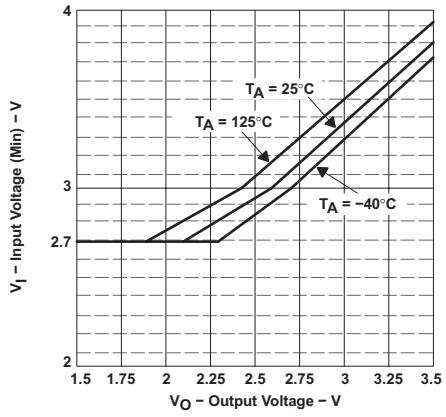
V_I = 4.3 V C_o = 10 µF
I_O = 1 A T_A = 25°C

Figure 10. TPS76733 Power Supply Ripple Rejection vs Frequency



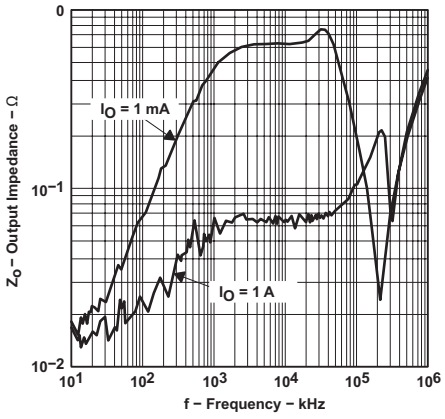
V_I = 4.3 V C_o = 10 µF T_A = 25°C

Figure 11. TPS76733 Output Spectral Noise Density vs Frequency



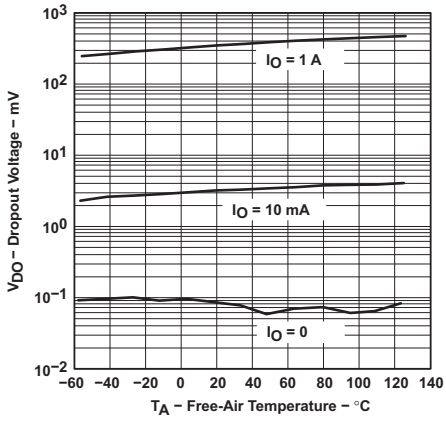
I_O = 1 A

Figure 12. Input Voltage (MIN) vs Output Voltage



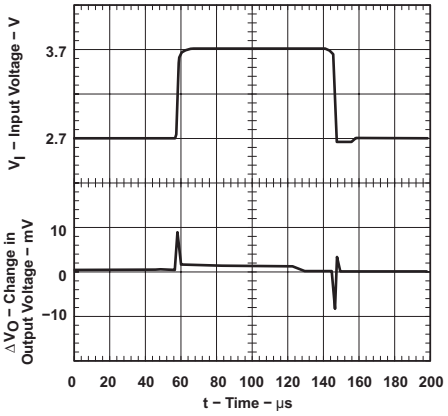
V_I = 4.3 V C_o = 10 µF T_A = 25°C

Figure 13. TPS76733 Output Impedance vs Frequency



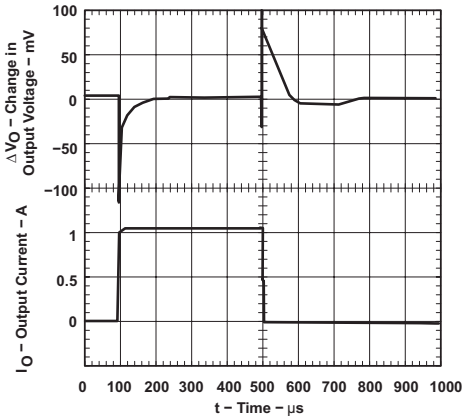
C_O = 10 µF

Figure 14. TPS76733 Dropout Voltage vs Free-Air Temperature



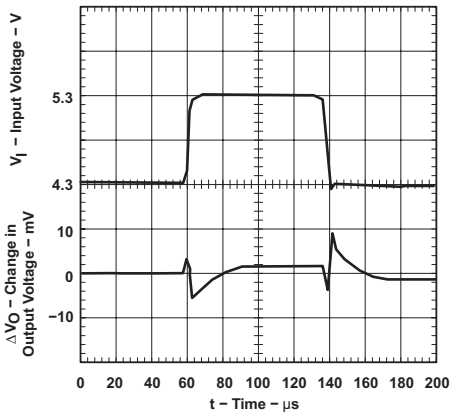
C_O = 10 µF T_A = 25°C

Figure 15. TPS76715 Line Transient Response



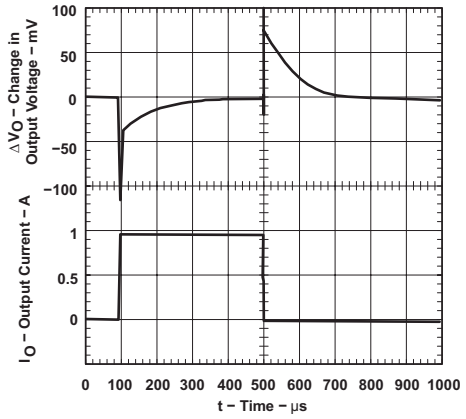
C_O = 10 µF T_A = 25°C

Figure 16. TPS76715 Load Transient Response



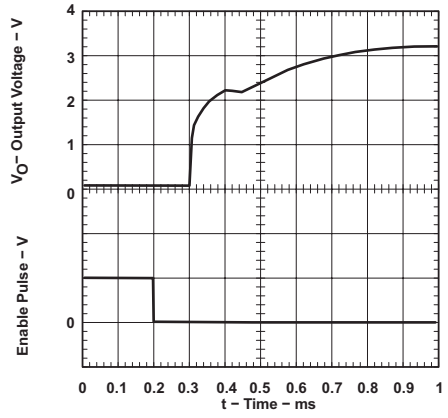
C_O = 10 µF T_A = 25°C

Figure 17. TPS76733 Line Transient Response



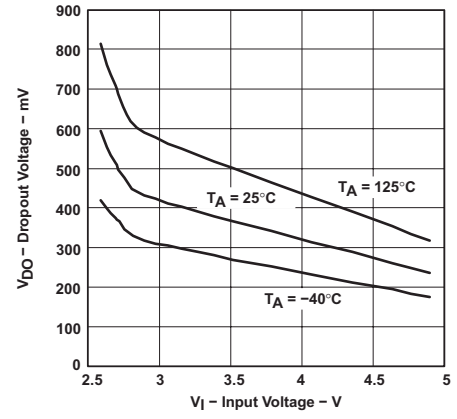
C_O = 10 µF T_A = 25°C

Figure 18. TPS76733 Load Transient Response



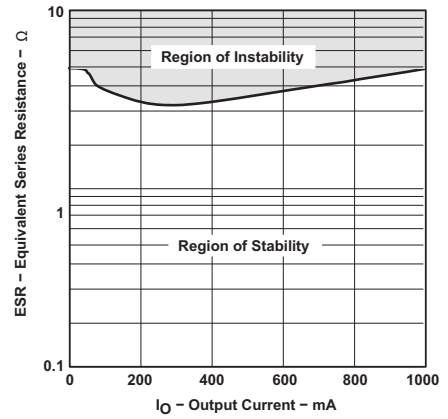
C_O = 10 µF I_O = 1 A T_A = 25°C

Figure 19. TJPS7633 Output Voltage vs Time (At Startup)



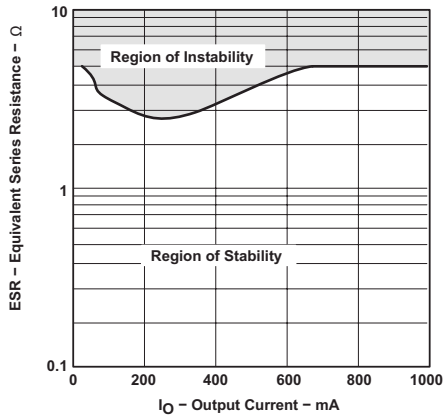
I_O = 1 A

Figure 20. TPS76701 Dropout Voltage vs Input Voltage



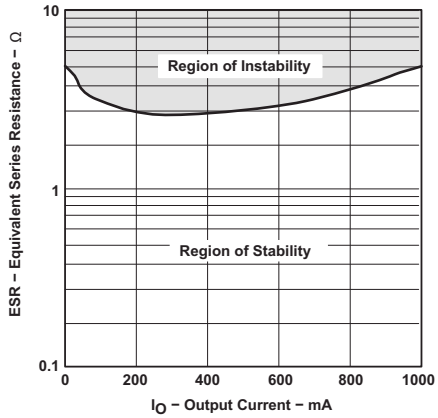
V_O = 3.3 V C_o = 4.7 µF
V_I = 4.3 A T_A = 25°C

Figure 21. Typical Region of Stability Equivalent Series Resistance vs Output Current



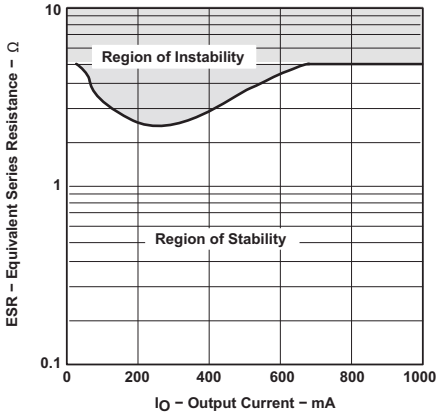
V_O = 3.3 V C_o = 4.7 µF
V_I = 4.3 A T_A = 125°C

Figure 22. Typical Region of Stability Equivalent Series Resistance vs Output Current



V_O = 3.3 V C_o = 22 µF
V_I = 4.3 A T_A = 25°C

Figure 23. Typical Region of Stability Equivalent Series Resistance vs Output Current



V_O = 3.3 V C_o = 22 µF
V_I = 4.3 A T_A = 125°C

Figure 24. Typical Region of Stability Equivalent Series Resistance vs Output Current

8 Parameter Measurement Information

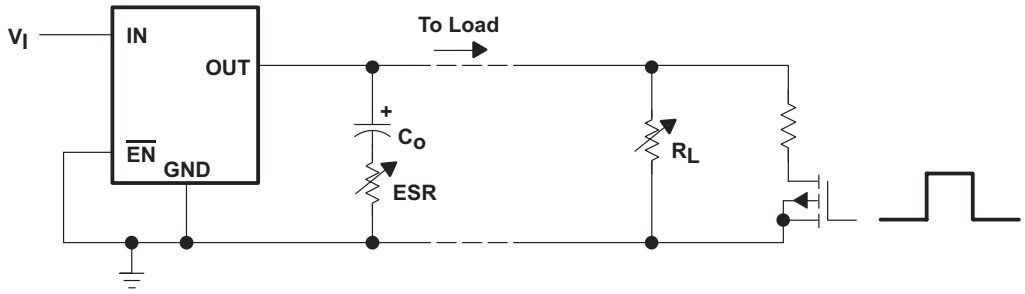


Figure 25. Test Circuit for Typical Regions of Stability (Figure 21 through Figure 24) (Fixed Output Options)

9 Detailed Description

9.1 Overview

The TPS767xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS767xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 µA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground.

9.2 Functional Block Diagram

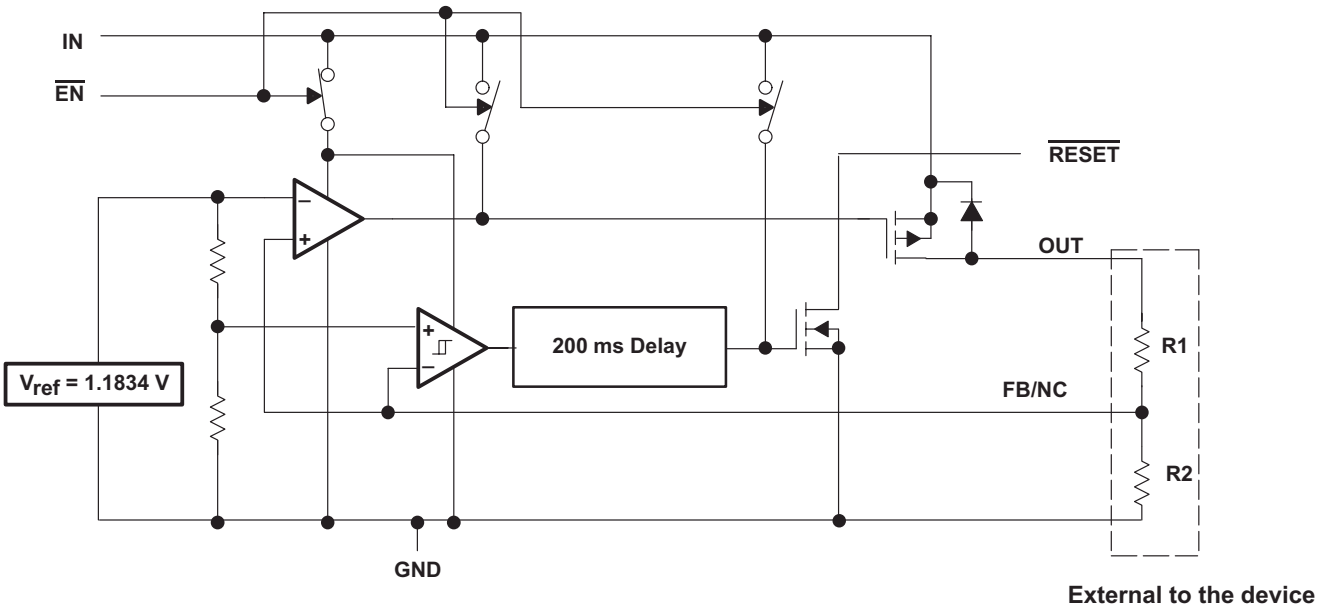


Figure 26. Adjustable Version

Functional Block Diagram (continued)

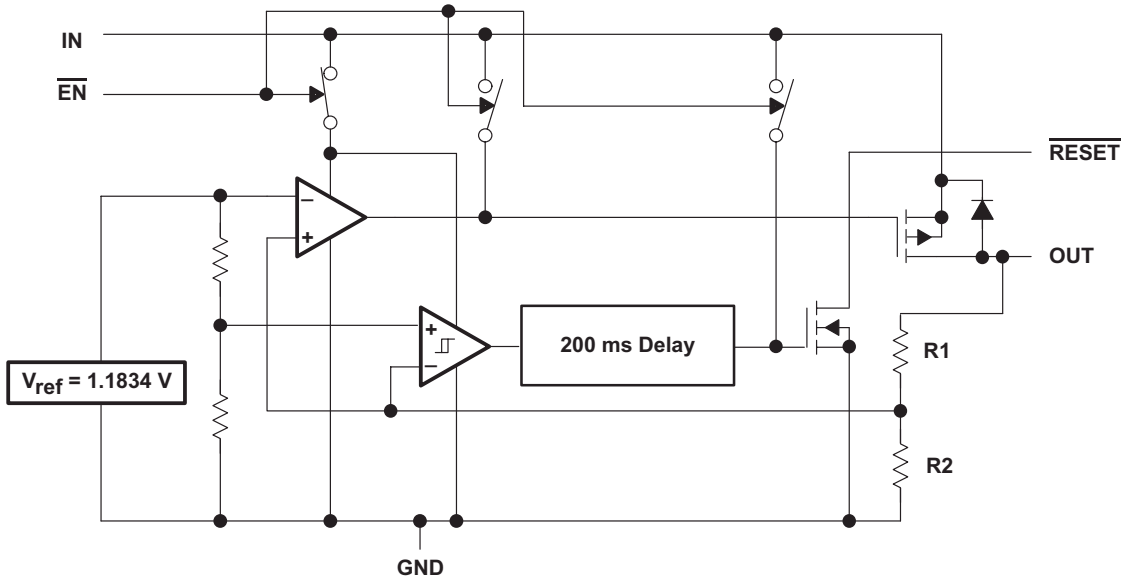


Figure 27. Fixed-Voltage Version

9.3 Feature Description

9.3.1 FB—Pin Connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option . The output voltage is sensed through a resistor divider network to close the loop as shown in Figure 28. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

9.3.2 Reset Indicator

The TPS767xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to Figure 1 timing diagram for start-up sequence).

9.3.3 Regulator Protection

The TPS767xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767xx also features internal current limiting and thermal protection. During normal operation, the TPS767xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

9.4 Device Functional Modes

9.4.1 Minimum Load Requirements

The TPS767xx family is stable even at zero load; no minimum load is required for operation.

9.5 Programming

9.5.1 Programming the TPS76701 Adjustable LDO Regulator

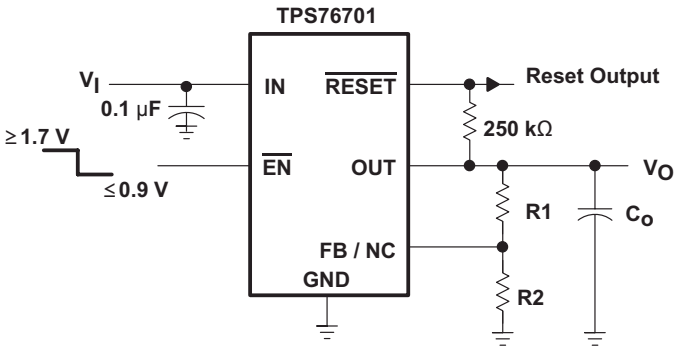
The output voltage of the TPS76701 adjustable regulator is programmed using an external resistor divider as shown in Figure 28. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where: f = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.2	30.1	kΩ
3.3 V	53.6	30.1	kΩ
3.6 V	61.9	30.1	kΩ
4.75 V	90.8	30.1	kΩ

Figure 28. TPS76701 Adjustable LDO Regulator Programming

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS767xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76701 (adjustable from 1.5 V to 5.5 V).

10.1.1 External Capacitor Requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 µF or larger) improves load transient response and noise rejection if the TPS767xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 µF and the ESR (equivalent series resistance) must be between 50 mΩ and 1.5 Ω. Capacitor values 10 µF or larger are acceptable, provided the ESR is less than 1.5 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10 µF surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.

10.2 Typical Application

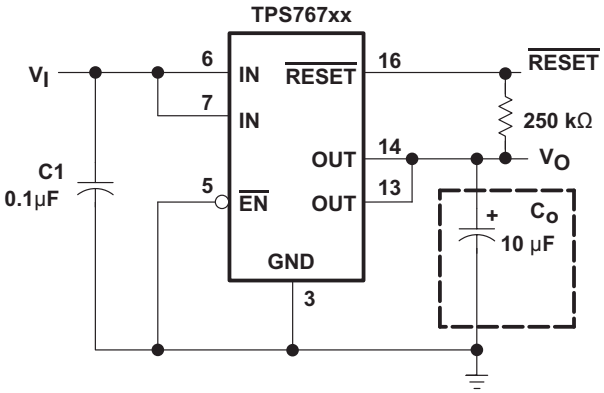
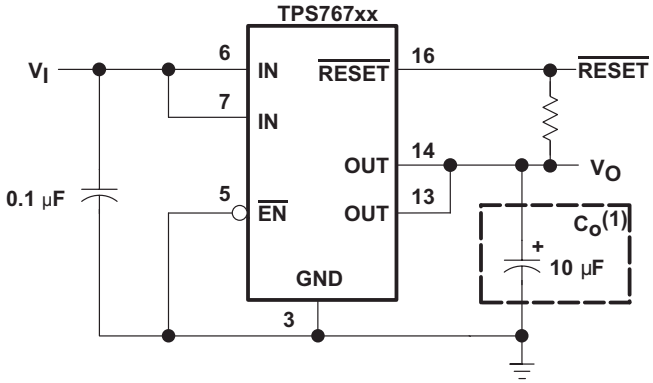


Figure 29. Typical Application Circuit (Fixed Versions)

Typical Application (continued)



(1) See application information section for capacitor selection details.

Figure 30. Typical Application Configuration (For Fixed Output Options)

11 Layout

11.1 Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (3)$$

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS76715	Click here	Click here	Click here	Click here	Click here
TPS76718	Click here	Click here	Click here	Click here	Click here
TPS76725	Click here	Click here	Click here	Click here	Click here
TPS76727	Click here	Click here	Click here	Click here	Click here
TPS76728	Click here	Click here	Click here	Click here	Click here
TPS76730	Click here	Click here	Click here	Click here	Click here
TPS76733	Click here	Click here	Click here	Click here	Click here
TPS76750	Click here	Click here	Click here	Click here	Click here
TPS76701	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76701QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76701
TPS76701QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76701
TPS76701QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76701
TPS76701QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76701
TPS76701QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701
TPS76701QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701
TPS76701QPWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701
TPS76701QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701
TPS76701QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701
TPS76701QPWPRG4	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76701
TPS76715QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76715
TPS76715QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76715
TPS76715QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76715
TPS76715QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76715
TPS76715QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76715
TPS76715QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76715
TPS76718QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76718
TPS76718QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76718
TPS76718QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76718 X
TPS76718QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76718 X
TPS76718QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76718
TPS76718QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76718
TPS76718QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76718
TPS76718QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76718
TPS76725QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76725
TPS76725QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76725
TPS76725QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725
TPS76725QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76725QPWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725
TPS76725QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725
TPS76725QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76725
TPS76727QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76727
TPS76727QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76727
TPS76727QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76727
TPS76727QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76727
TPS76728QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76728
TPS76728QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76728
TPS76730QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76730
TPS76730QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76730
TPS76730QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730
TPS76730QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730
TPS76730QPWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730
TPS76730QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730
TPS76730QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76730
TPS76733QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76733
TPS76733QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76733
TPS76733QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76733
TPS76733QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76733
TPS76733QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733
TPS76733QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733
TPS76733QPWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733
TPS76733QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733
TPS76733QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733
TPS76733QPWPRG4	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76733
TPS76750QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76750
TPS76750QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76750
TPS76750QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76750
TPS76750QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76750
TPS76750QPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76750

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76750QPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76750
TPS76750QPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76750
TPS76750QPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT76750

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS767 :

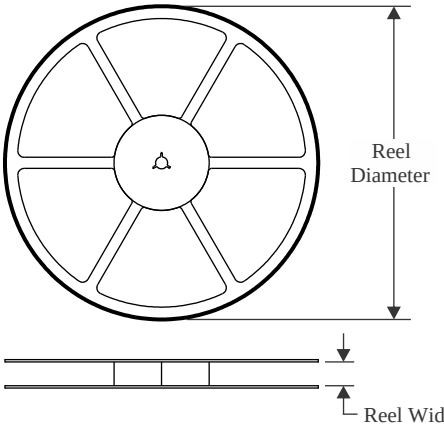
- Automotive : TPS767-Q1

NOTE: Qualified Version Definitions:

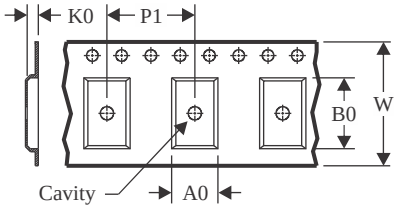
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

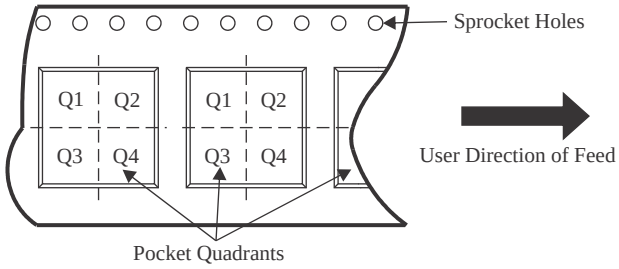


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

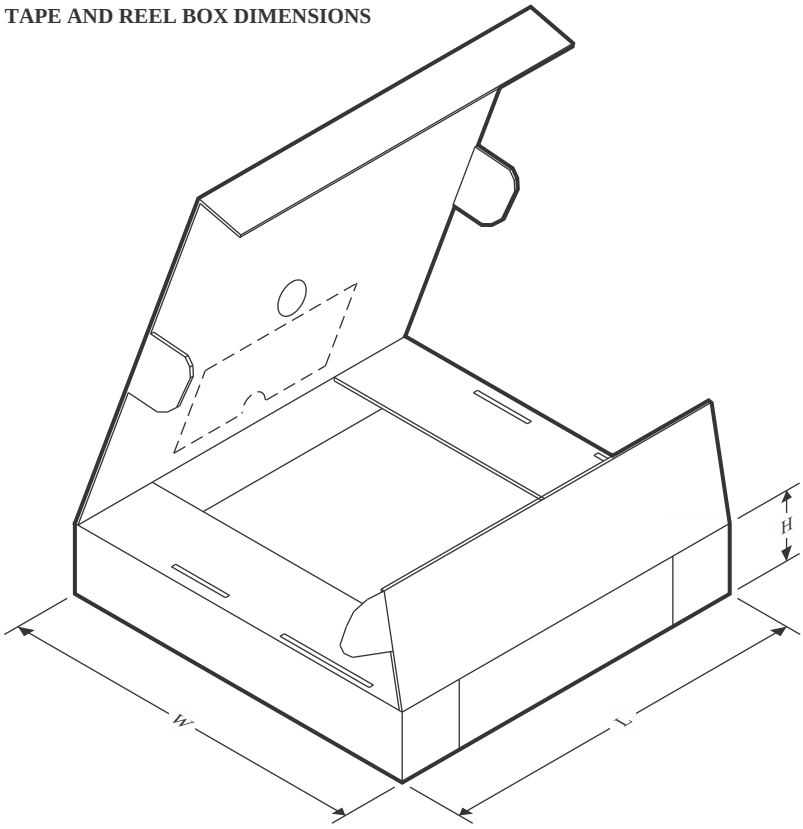
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76701QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76701QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76715QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76718QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76718QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76725QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76730QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76733QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76733QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76750QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76750QPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

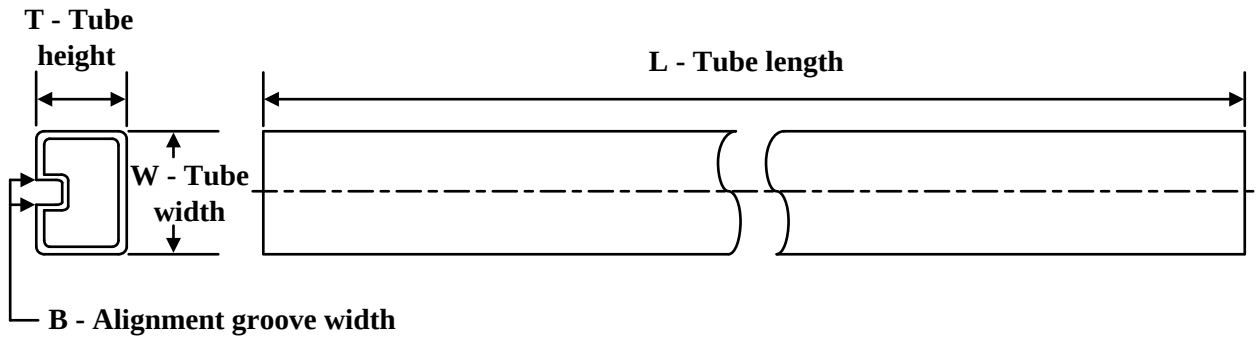
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76701QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76701QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76715QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76718QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76718QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76725QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76730QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76733QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76733QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76750QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76750QPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS76701QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76701QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76701QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76701QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76701QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76715QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76715QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76715QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76715QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76718QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76718QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76718QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76718QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76725QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76725QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76725QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76725QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76725QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76727QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76727QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76727QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76727QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76728QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76728QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76730QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76730QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76730QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76730QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76730QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS76733QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76733QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76733QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76733QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76733QPWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76750QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS76750QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS76750QPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS76750QPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

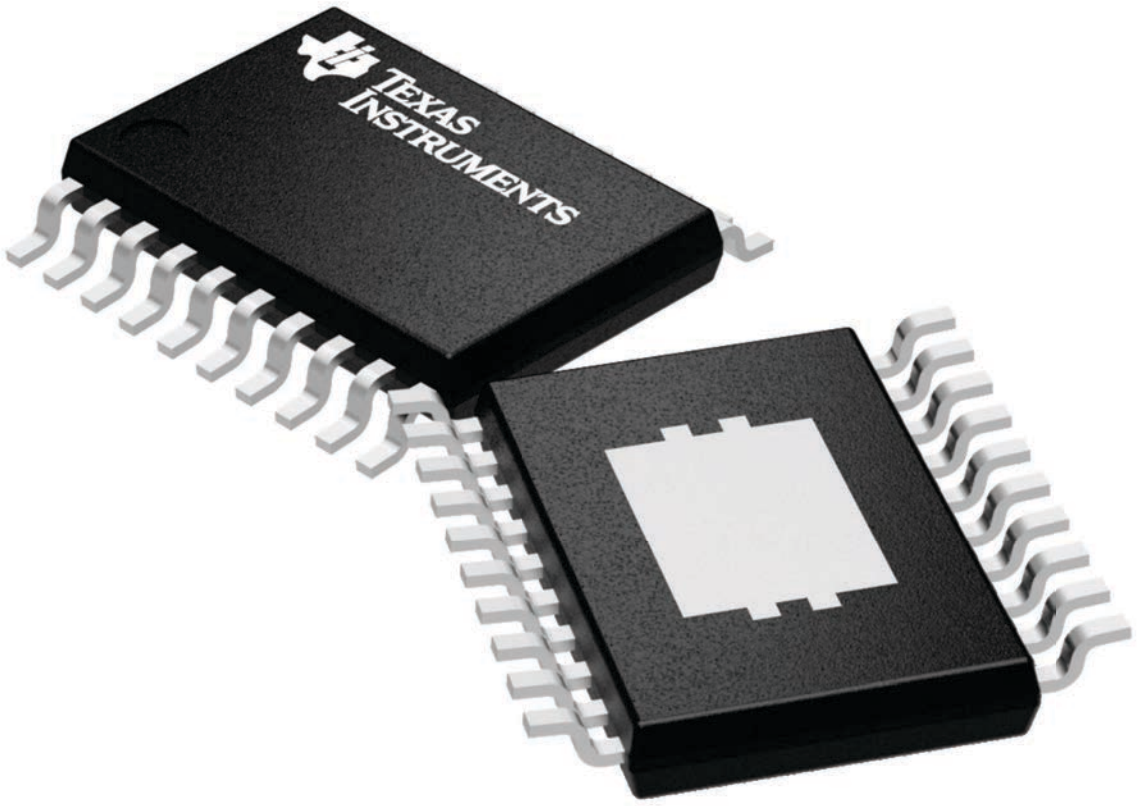
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

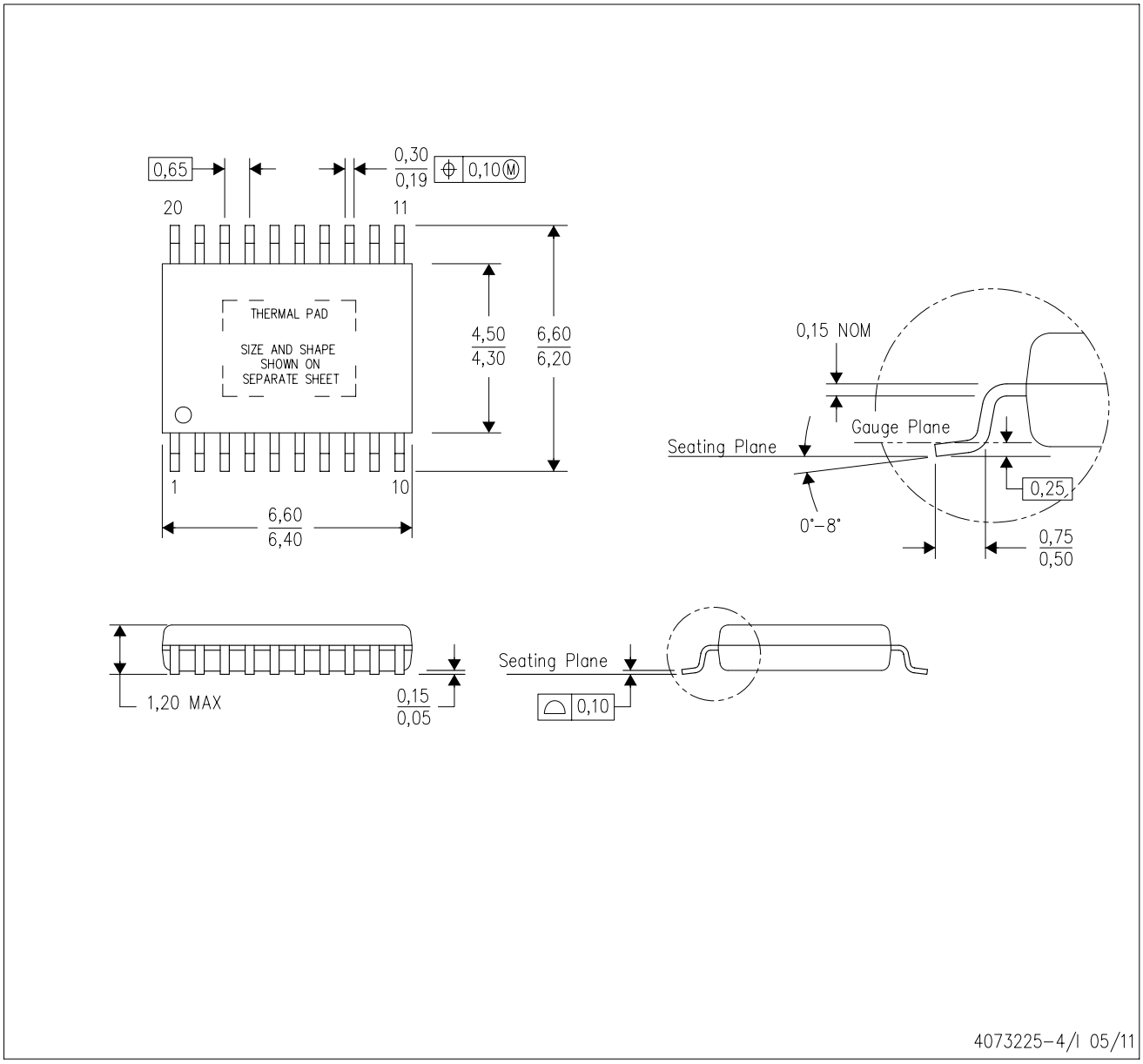
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

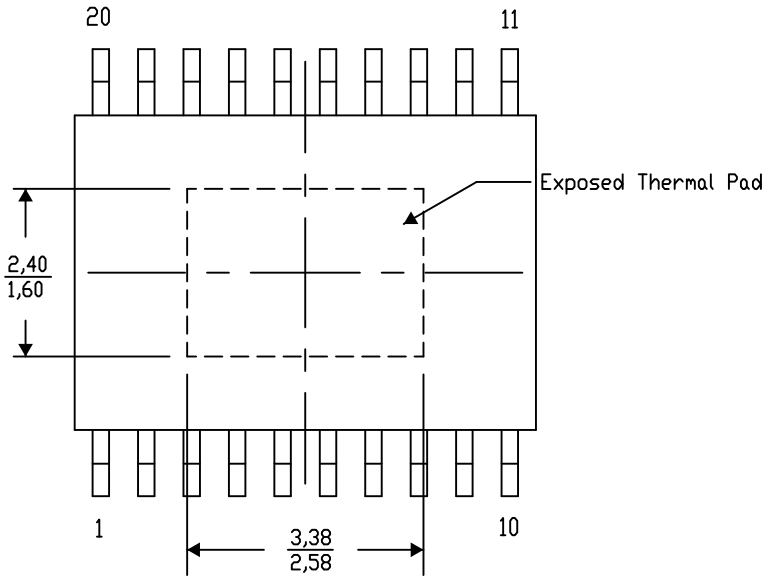
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

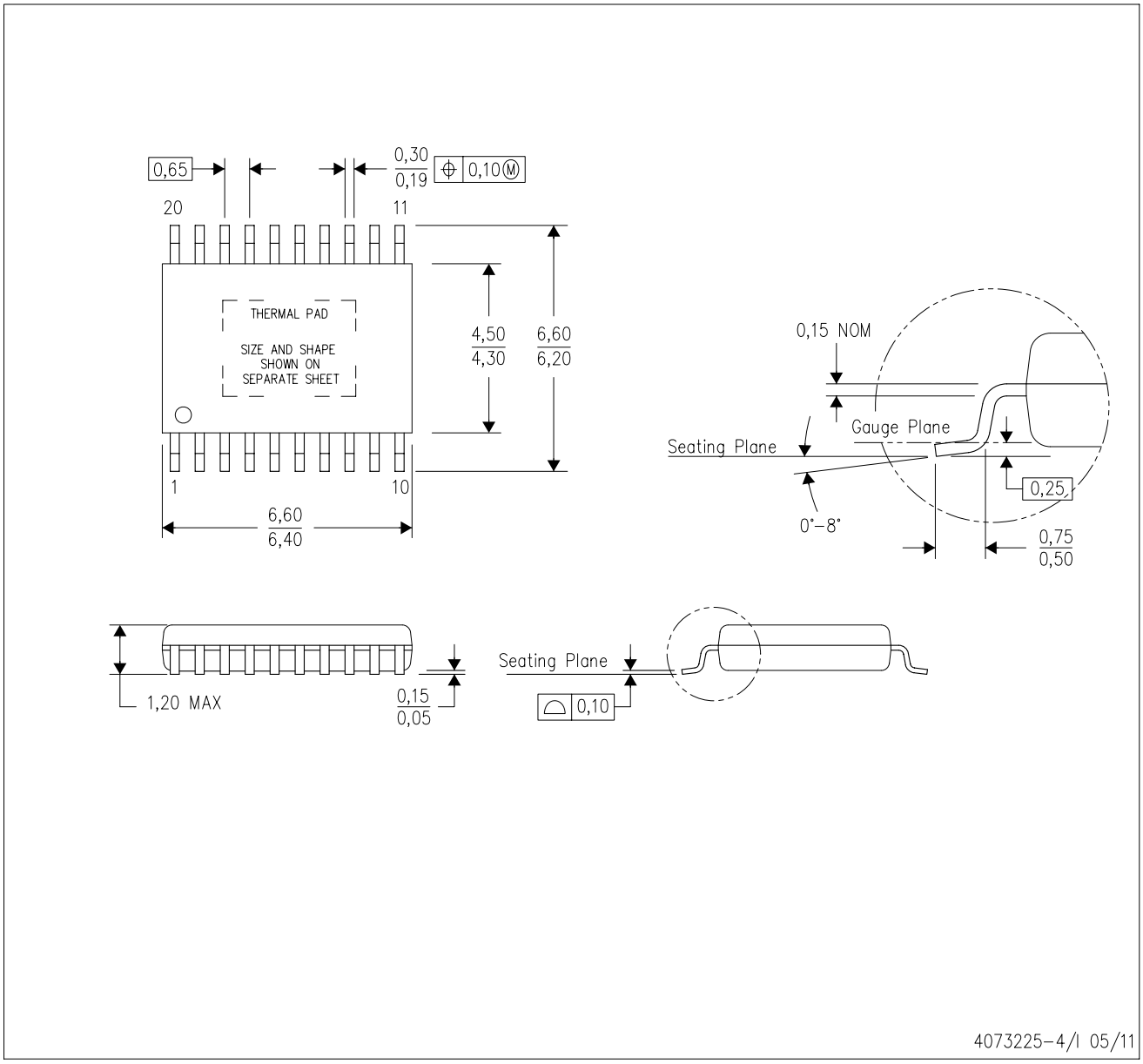
Exposed Thermal Pad Dimensions

4206332–21/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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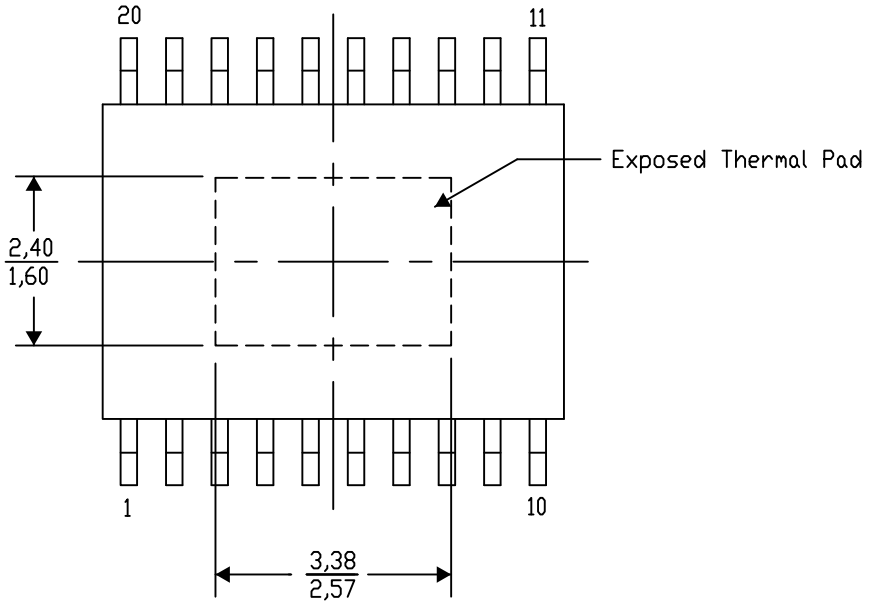
The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

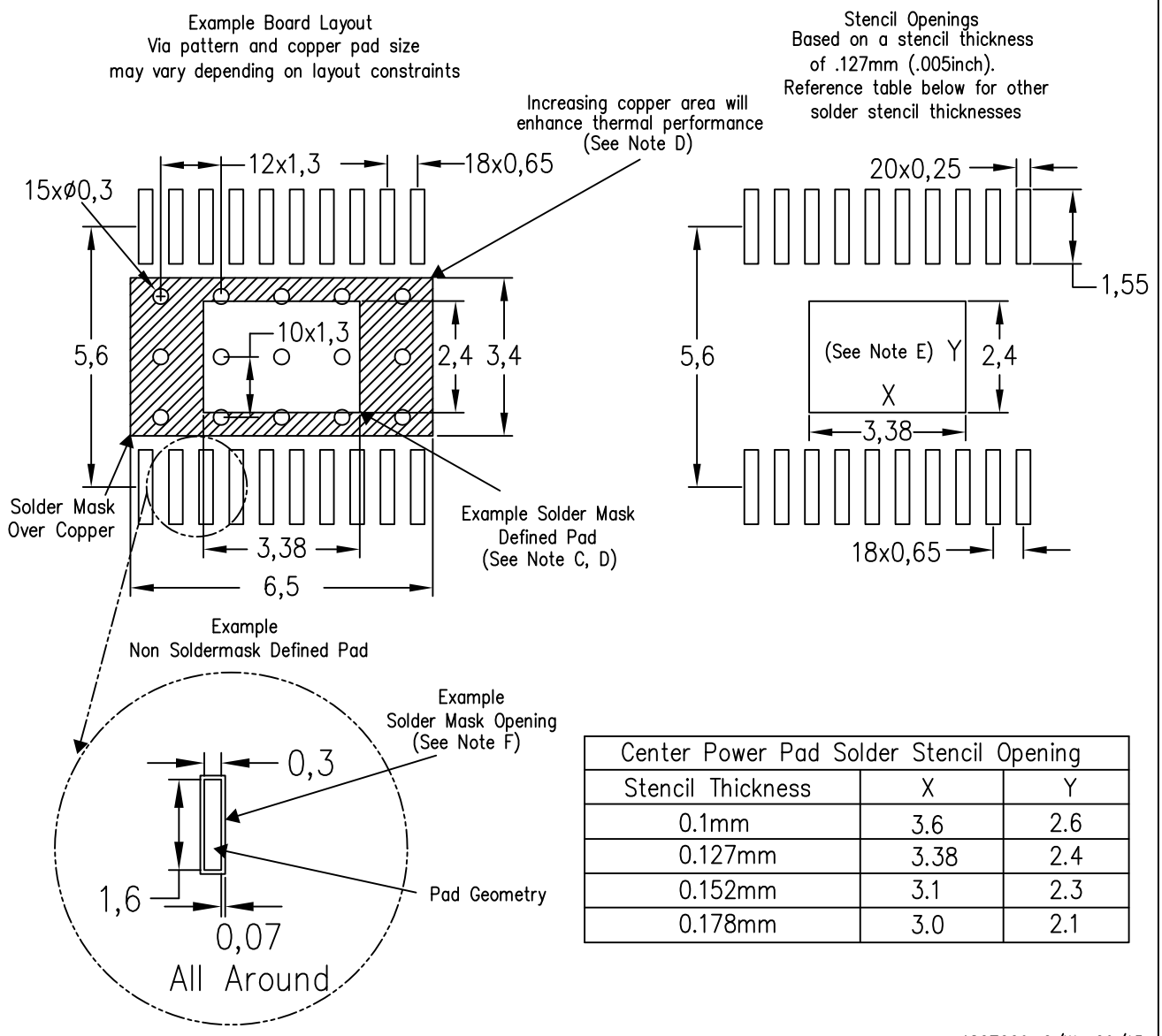
Exposed Thermal Pad Dimensions

4206332–13/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

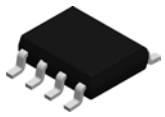
PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.6	2.6
0.127mm	3.38	2.4
0.152mm	3.1	2.3
0.178mm	3.0	2.1

4207609–6/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

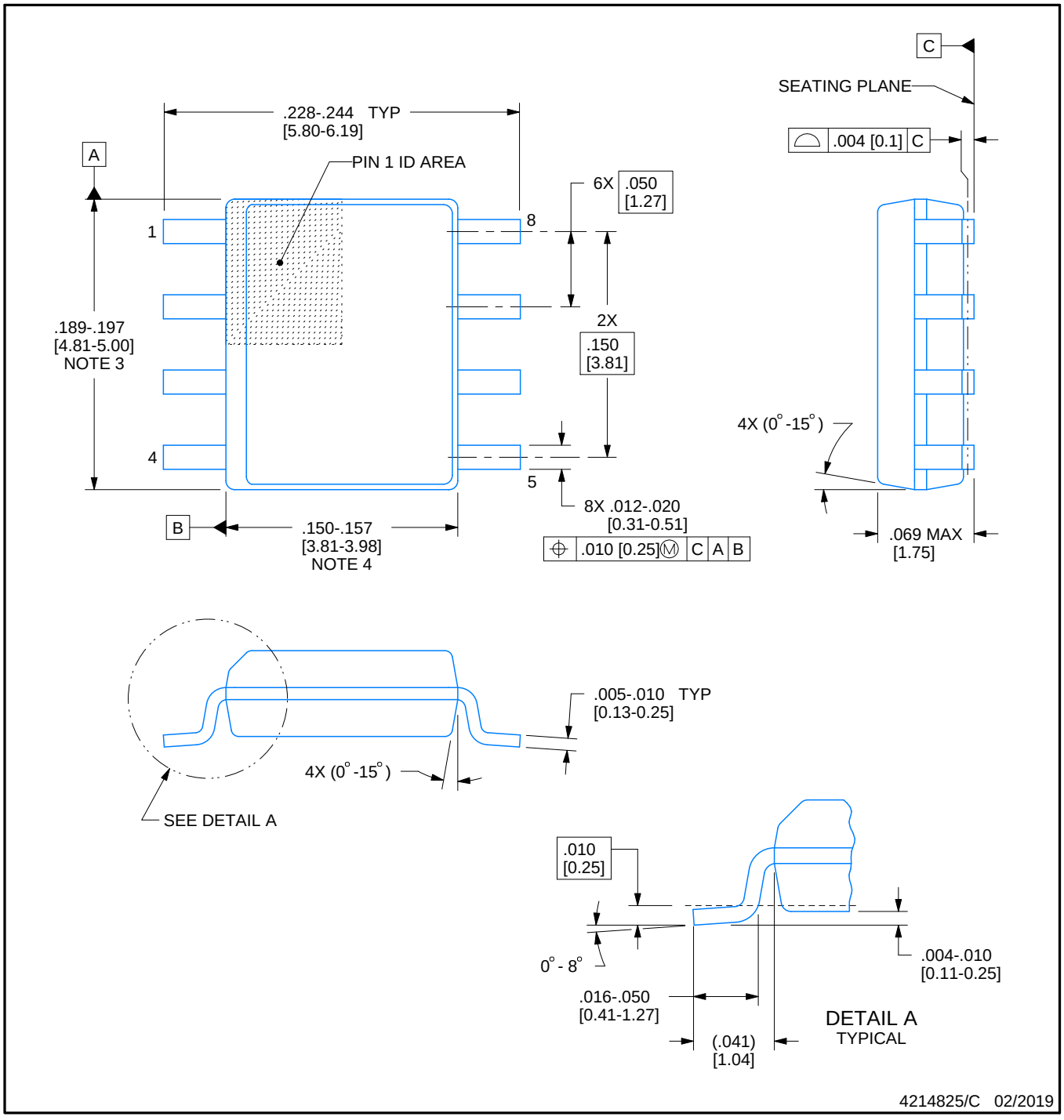


PACKAGE OUTLINE

D0008A

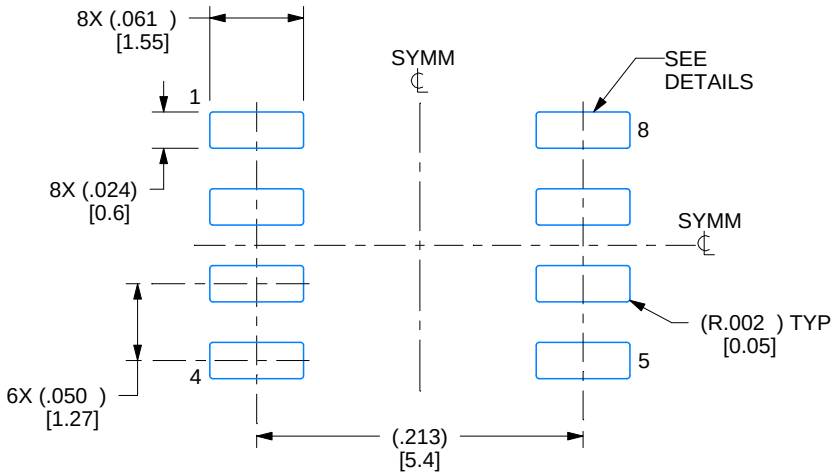
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

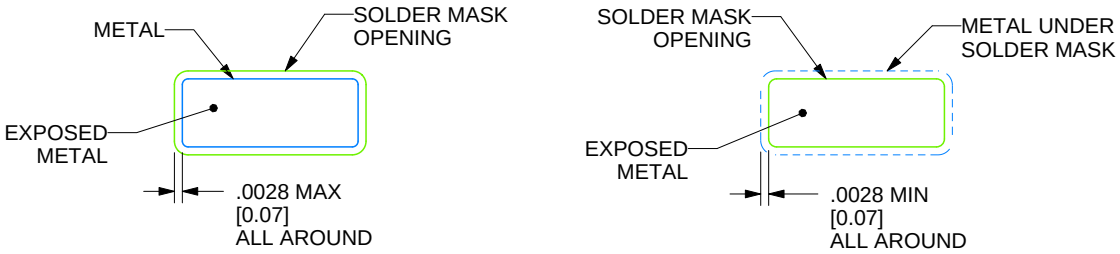


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

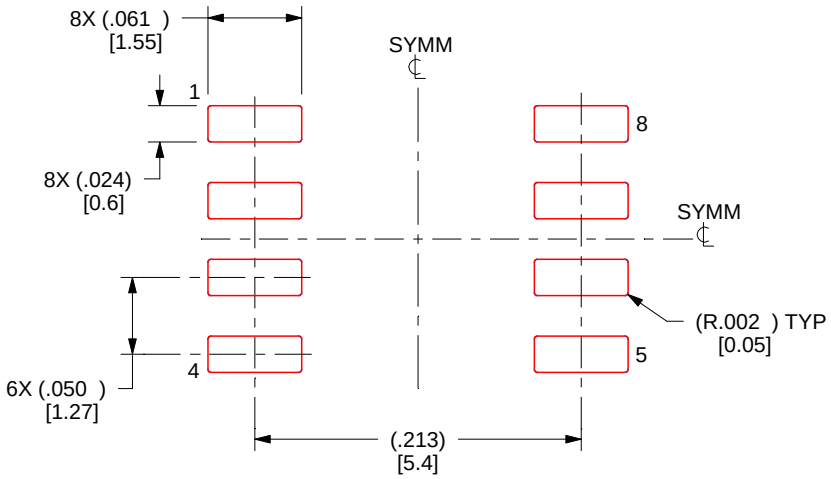
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025